RC21008A/RC31008A/RC21012A/RC31012A

The RC21008A/RC31008A and RC21012A/RC31012A Evaluation Boards (EVB) are designed to support users evaluating the clock generation in synthesizer mode for PCIe Gen compliance or jitter attenuation mode. Instructions in this manual that reference RC21008A/RC31008A also pertain to RC21012A/RC31012A.

Specifications

Best in class performance for various frequencies.

- Less than 1W typical power dissipation
- 150fs RMS phase jitter (12kHz–20MHz, integer)
- 200fs RMS phase jitter (12kHz–20MHz, fraction)

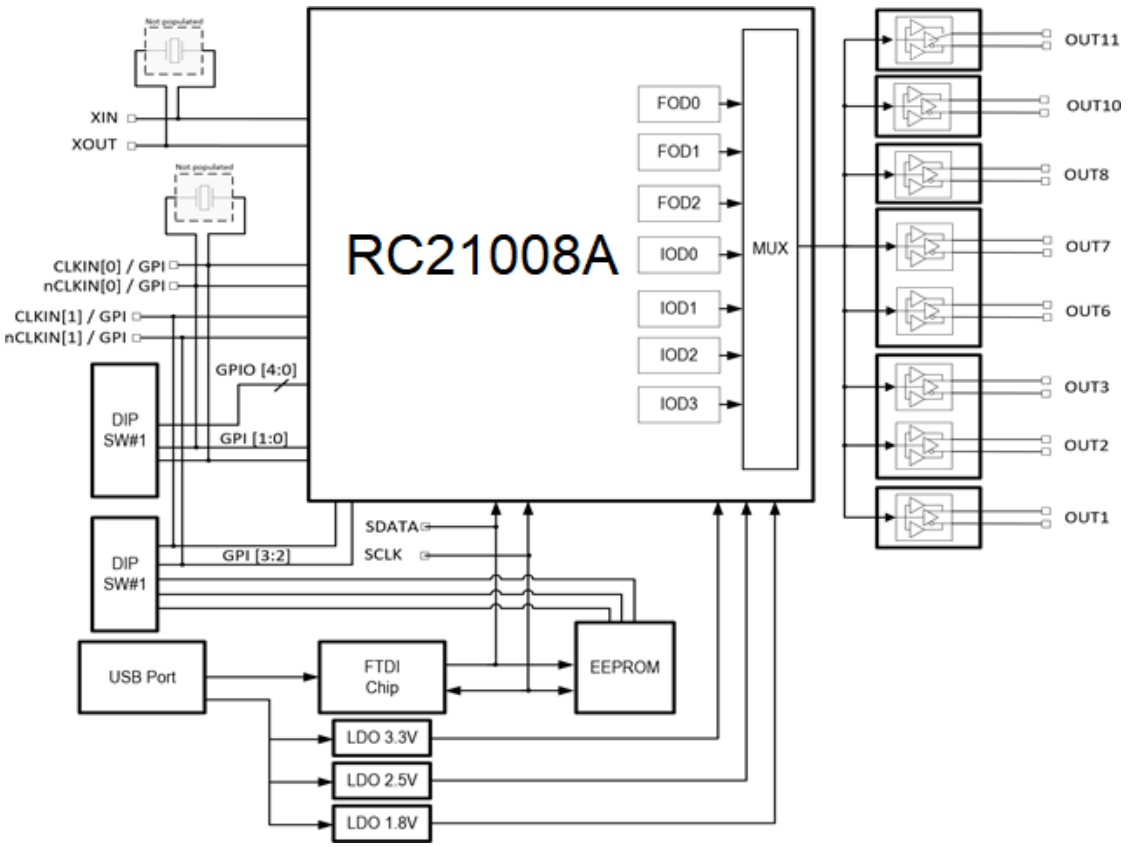
Board Contents

Items shipped with the EVB kit:

- Evaluation board
- USB-C cable

Features

- Crystal or Crystal overdrive (REFIN) via SMA
- Available sense lines on Crystal Overdrive and CLKIN
- Onboard I^2C and SPI communications
- Four GPIs and five GPIOs
- GPI/GPIO LED indicator and DIP switch
- Test points on outputs for Hi-Z probes
- Jumper selectable voltage setting for 3.3V/2.5V/1.8V powered from USB-C



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1. Functional Description

The RC21008A/RC31008A and RC21012A/RC31012A Evaluation Boards (EVB) are designed to support users evaluating the RC21008A, RC31008A, RC21012A and RC31012A devices using clock generation in synthesizer mode for PCIe Gen compliance or in jitter attenuation mode. When the EVB is connected via USB to the user's computer running Renesas Integrated Circuit Toolbox (RICBox™) software, the devices can be configured in various frequencies with best-in-class performance. The devices offer various features with a total of eight to twelve pairs of differential outputs. Each pair of outputs can be programmed to LVCMOS style, LVDS style, and LP-HCSL style outputs. There are five general purpose input/output (GPIOs) and four general purpose input (GPIs) to support output enables, power down, configuration selection, and status outputs. Voltage levels for VDDX, VDDR, VDDA, VDDD, VDDO1, VDDO2, VDDO3, VDDO4, VDDO5, and VDDO6 can be set by a jumper. The EVB kit also has a socket to load a configuration from EEPROM (see Figure 2).

1.1 Operational Characteristics

The EVB is capable of functioning in a temperature range of -40C to 85C. The EVB is capable of operating in VDD values of 3.3V, 2.5V, and 1.8V. The VDD_J banana connection can be used to set any desired voltage within the range of 1.71V to 3.63V.

1.2 Setup and Configuration

The following sections explain the Crystal, Input Clock, Serial, GPI/GPIO and Output and Power functions used for setting up and configuring the devices using RICBox software.

1.2.1. RC21008A/RC31008A vs RC21012A/RC31012A

RC21008A is an 8-output device and RC21012A is a 12-output device. Likewise, RC31008A and RC31012A are 8-output and 12-output devices, respectively. The difference between RC210xx and RC310xx is that RC210xx is a synthesizer only while RC310xx supports jitter attenuator (JA) operations.

The following table summarizes the differences between the devices.

Table 1. Summary of RC21008A/RC31008A and RC21012A/RC31012A

Device	Crystal interface	Input Clocks	JA Support	Output Clocks
RC21008A	Yes	CLKIN0/nCLKIN0 CLKIN1/nCLKIN1	No	OUT1, OUT2, OUT3, OUT6, OUT7, OUT8, OUT10, OUT11
RC21012A	Yes	CLKIN0/nCLKIN0 CLKIN1/nCLKIN1	No	OUT1–OUT11
RC31008A	Yes	CLKIN0/nCLKIN0 CLKIN1/nCLKIN1	Yes	OUT1, OUT2, OUT3, OUT6, OUT7, OUT8, OUT10, OUT11
RC31012A	Yes	CLKIN0/nCLKIN0 CLKIN1/nCLKIN1	Yes	OUT1–OUT11

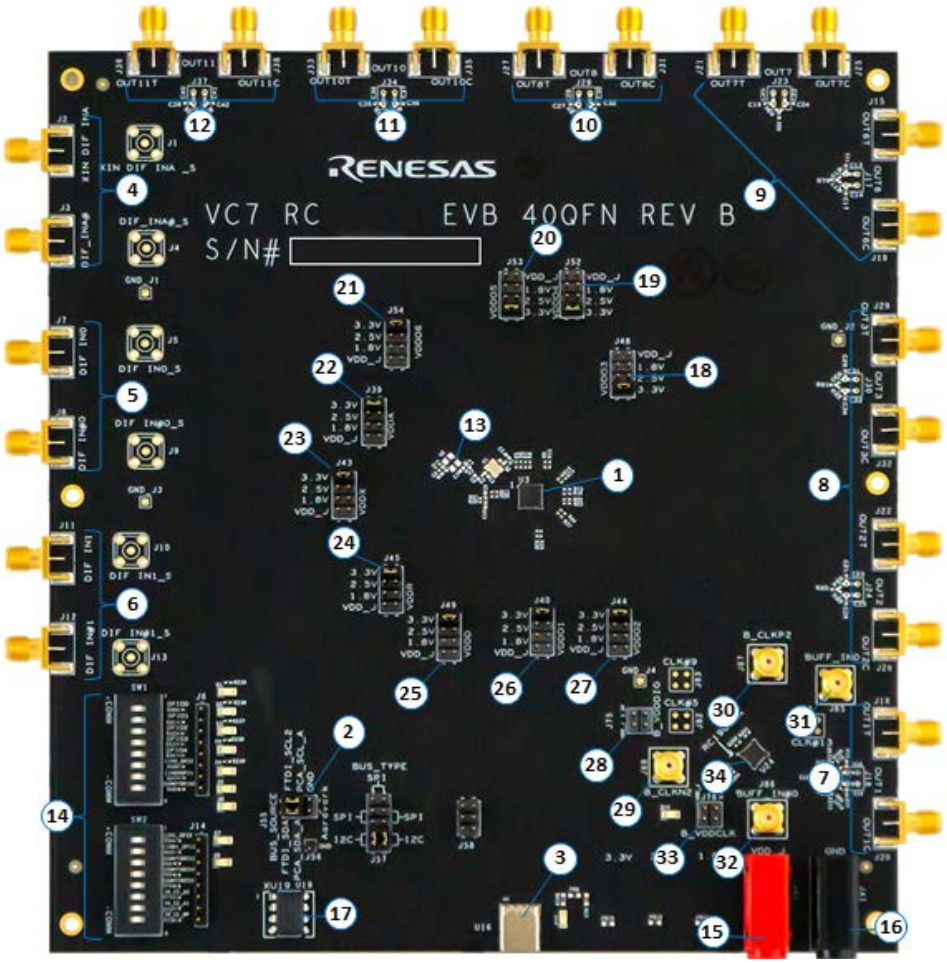


Figure 2. RC21008A/RC31008A VersaClock 7 Evaluation Board

Refer to Table 2 for the RC21008A/RC31008A evaluation board pin descriptions and functions.

Table 2. RC21008A/RC31008A–EVB Pins and Functions

Label No.	Name	On-Board Connector Label	Function
1	RC21008A/RC31008A	U3	Evaluation device, 5 x 5 x 0.9 mm 40-pin QFN.
2	I²C for FTDI or Aardvark Connector	J55	6 pins header of I²C connector for SCL and SDA pins.
3	USB Interface	U16	USB Type Jack for connection with the user's computer and interaction with RICBox software.
4	XIN / DIF_INA, DIF_INA#	J2, J3	Differential REF clock input positive on J3 and negative on J4/CMOS single-ended reference clock input. If J3 is connected to XIN as REFIN single-ended, J4 must be left unconnected.
5	CLKIN0, CLKIN0#	J7, J8	Differential Clock 0 input positive on J6 and negative on J7/CMOS single-ended reference clock input
6	CLKIN1, CLKIN1#	J11, J12	Differential Clock 1 input positive on J8 and negative on J9/CMOS single-ended reference clock input.

Label No.	Name	On-Board Connector Label	Function
7	Test Points for OUT1	J16, J20	SMA connectors for differential outputs using VDDO1 power rail (populated with a pair of SMA connector): J16, J20 for OUT1
8	Test Points for OUT2, OUT3	J22, J26, J29, J32	SMA connectors for differential outputs using VDDO2 power rail (populated with a pair of SMA connector): J22, J26 for OUT2 J29, J32 for OUT3
9	Test Points for OUT6, OUT7	J15, J19, J21, J25	SMA connectors for differential outputs using VDDO3 power rail (populated with a pair of SMA connector): J15, J19 for OUT6 J21, J25 for OUT7
10	Test Points for OUT8	J27, J31	SMA connectors for differential outputs using VDDO4 power rail (populated with a pair of SMA connector): J27, J31 for OUT8
11	Test Points for OUT10	J33, J35	SMA connectors for differential outputs using VDDO5 power rail (populated with a pair of SMA connector): J33, J35 for OUT10
12	Test Points for OUT11	J36, J38	SMA connectors for differential outputs using VDDO6 power rail (populated with a pair of SMA connector): J36, J38 for OUT11
13	Crystal Pads	U1, U2	To mount different quartz crystals.
14	DIP Switches	SW1, SW2	DIP switch devices are used to setup GPIO/GPI pins based on RC21008A/RC31008A device condition. See Figure 13 and Figure 14 for details.
15	Power VDD Jack	J42	External power supply, positive terminal. Apply 3.3V, 2.5V or 1.8V as default only.
16	Power GND Jack	J41	External power supply, negative terminal or ground.
17	EEPROM IC	XU19, U19	An external EEPROM IC and an 8-lead PDIP8 socket. Populated with AT24C04C 4-Kbit (512 x8) EEPROM as default.
18	VDDO3	J48	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 3.
19	VDDO4	J52	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 4.
20	VDDO5	J53	Power source selector, select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 5.
21	VDDO6	J54	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 6.
22	VDDA	J39	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for analog circuit power.
23	VDDX	J43	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for crystal circuit power.
24	VDDR	J45	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for reference input circuit power.

Label No.	Name	On-Board Connector Label	Function
25	VDDD	J49	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for digital circuit power.
26	VDDO1	J40	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 1.
27	VDDO2	J44	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 2.
28	B_VDDDIG	J75	Power source selector. Select in 3.3V or external power VDD_J for VDDIG digital power pin of RC19004A.
29	B_CLKN2	J88	Complementary clock output pin of RC19004A.
30	B_CLKP2	J87	True clock output pin of RC19004A.
31	BUFF_IN0	J85	Differential buffer Input 0.
32	BUFF_IN#0	J86	Differential buffer Input #0.
33	B_VDDCLK	J76	Power source selector, select in 3.3V or external power VDD_J for VDDCLK clock power supply pin of RC19004A.
34	RC19004A	U24	Fanout buffer.

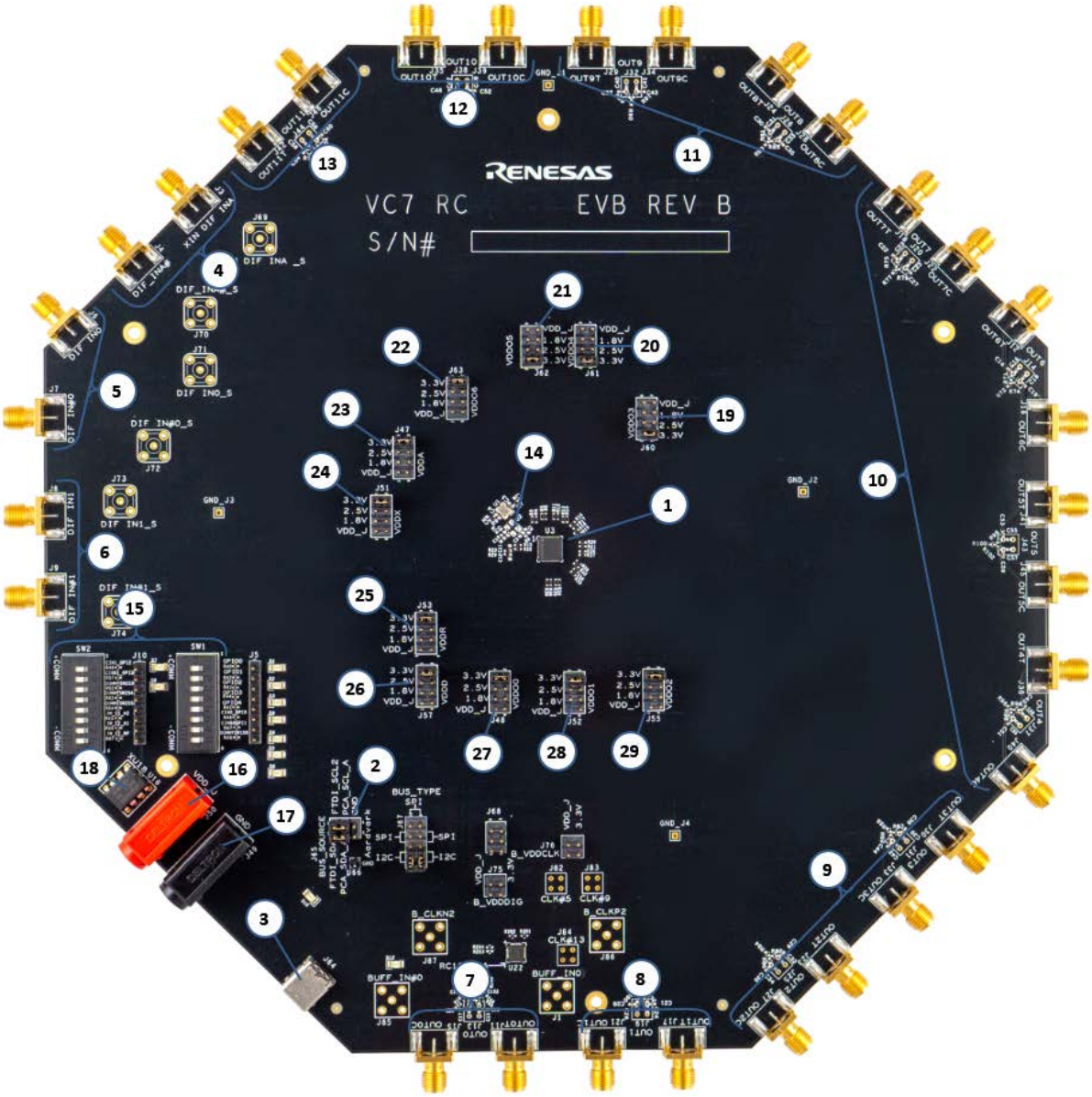


Figure 3. RC21012A/RC31012A VersaClock 7 Evaluation Board

Refer to Table 3 for the RC21012A/RC31012A evaluation board pin descriptions and functions.

Table 3. RC21012A/RC31012A–EVB Pins and Functions

Label No.	Name	On-Board Connector Label	Function
1	RC21012A/RC31012A	U3	Evaluation device, 48-pin QFN
2	I^2C for FTDI or Aardvark connector	J55	6 pins header of I^2C connector for SCL and SDA pins.
3	USB Interface	J64	USB type jack for connection with the user's computer and interaction with RICBox software.
4	XIN/DIF_INA, DIF_INA#	J3, J4	Differential REF clock input positive on J3 and negative on J4/CMOS single-ended reference clock input. If J3 is connected to XIN as REFIN single-ended, J4 must be left unconnected.

Label No.	Name	On-Board Connector Label	Function
5	CLKIN0, CLKIN0#	J6, J7	Differential Clock 0 input positive on J6 and negative on J7/CMOS single-ended reference clock input.
6	CLKIN1, CLKIN1#	J8, J9	Differential Clock 1 input positive on J8 and negative on J9/CMOS single-ended reference clock input.
7	Test Points for OUT0	J11, J15	SMA connectors for differential outputs using VDDO0 power rail (populated with a pair of SMA connector): J11, J15 for OUT0
8	Test Points for OUT1	J17, J21	SMA connectors for differential outputs using VDDO1 power rail (populated with a pair of SMA connector): J17, J21 for OUT1
9	Test Points for OUT2, OUT3	J23, J27, J30, J33	SMA connectors for differential outputs using VDDO2 power rail (populated with a pair of SMA connector): J23, J27 for OUT2 J30, J33 for OUT3
10	Test Points for OUT4, OUT5, OUT6, OUT7	J36, J40, J41, J45, J12, J16, J18, J22	SMA connectors for differential outputs using VDDO3 power rail (populated with a pair of SMA connector): J36, J40 for OUT4 J41, J45 for OUT5 J12, J16 for OUT6 J18, J22 for OUT7
11	Test Points for OUT8, OUT9	J24, J28, J29, J34	SMA connectors for differential outputs using VDDO4 power rail (populated with a pair of SMA connector): J24, J28 for OUT8 J29, J34 for OUT9
12	Test Points for Out#10	J35, J39	SMA connectors for differential outputs using VDDO5 power rail (populated with a pair of SMA connector): J35, J39 for OUT10
13	Test Points for OUT11	J42, J46	SMA connectors for differential outputs using VDDO6 power rail (populated with a pair of SMA connector): J42, J46 for OUT11
14	Crystal Pads	U1, U2	To mount different quartz crystals.
15	DIP Switches	SW1, SW2	DIP switch devices are used to setup GPIO/GPI pins based on RC21008A/RC31008A device condition. See Figure 13 and Figure 14 for details.
16	Power VDD Jack	J50	External power supply, positive terminal. Apply 3.3V, 2.5V or 1.8V as default only.
17	Power GND Jack	J49	External power supply, negative terminal or ground.
18	EEPROM IC	XU18, U18	An external EEPROM IC and an 8-lead PDIP8 socket. Populated with AT24C04C 4-Kbit (512 x8) EEPROM as default.
19	VDDO3	J60	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 3.
20	VDDO4	J61	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 4.

Label No.	Name	On-Board Connector Label	Function
21	VDDO5	J62	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 5.
22	VDDO6	J63	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 6.
23	VDDA	J47	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for analog circuit power.
24	VDDX	J51	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for crystal circuit power.
25	VDDR	J53	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for reference input circuit power.
26	VDDD	J57	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for digital circuit power.
27	VDDO0	J48	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 0.
28	VDDO1	J52	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 1.
29	VDDO2	J55	Power source selector. Select in 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 2.

1.2.2. On Board Crystal PAD and Reference Input

The EVB has two crystal pads U1 and U2. U1 is installed with an Abracon 50MHz crystal with C_L of 8pF. U2 has no use for RC21008A/RC31008A. Different crystal frequencies between 8MHz and 80MHz can be used to match the specific application where the RC21008A/RC31008A will be used. For example we recommend using a 48MHz or 60MHz crystal for Jitter Attenuator applications and a 39.0625MHz or 62.5MHz crystal for Ethernet applications with output frequencies like 156.25MHz or 312.5MHz. Please refer to the datasheet for more information on crystal recommendations. The RC21008A/RC31008A supports a range of C_L from 6pF to 12pF.

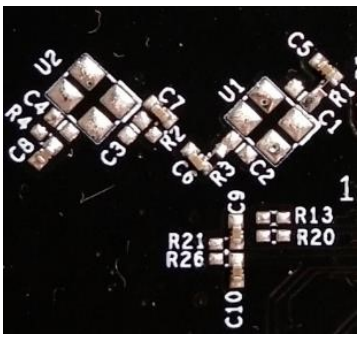


Figure 3. Crystal Footprints

The XIN DIF INA input (J2/J3) can be used to overdrive the XIN pin with an external clock with SMA connectors in single-ended or differential mode. Supported frequency ranges of the reference input are 1kHz to 650MHz in differential mode, and 1kHz to 200MHz. in single ended mode.

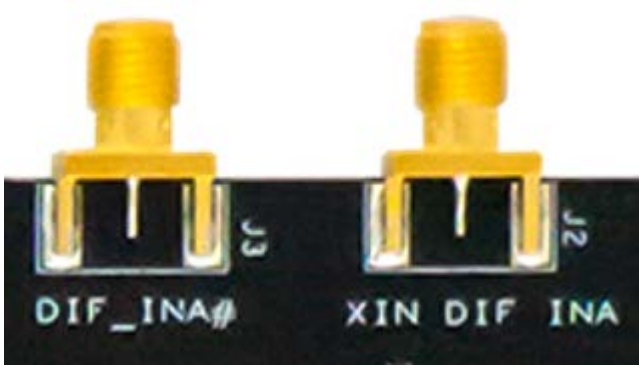


Figure 4. Single-ended/Differential Ref Input

1.2.3. CLKIN0/CLKIN1 Clock Inputs

The RC21008A/RC31008A can accept two differential clock inputs or four single-ended clock inputs (J7/J8) (J11/J12) to be used as an alternate reference for synth mode or a jitter attenuator source. To enable proper connection, make sure C7, C8, C9, and C10 are populated and R13, R20, R21, and R26 are unpopulated. The RC21008A/RC31008A contains internal termination for LVDS, HCSL, CML, LVPECL or CMOS levels. AC coupling is also available. Supported frequency ranges of the clock inputs are 1MHz to 650MHz in differential mode, and 8kHz to 250MHz in single ended mode. When CLKIN are not used, they can configured as GPI.

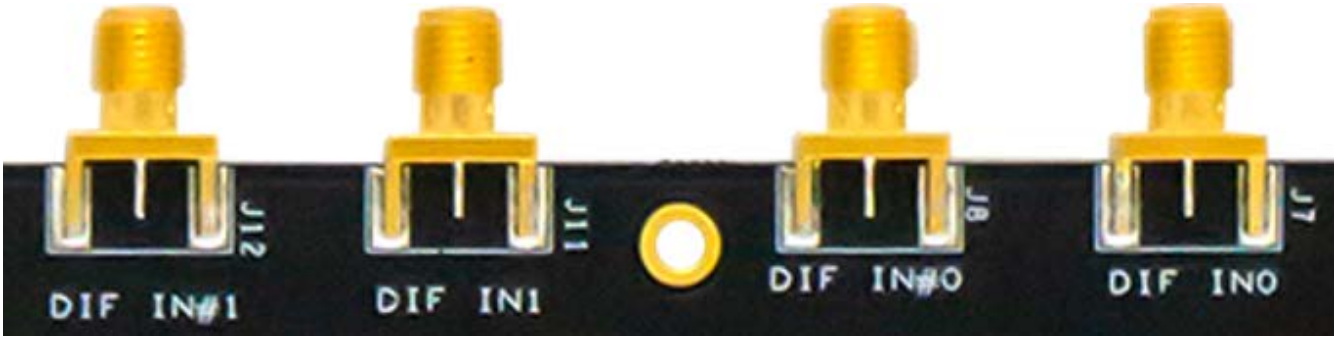


Figure 5. CLKIN0/CLKIN1 Inputs

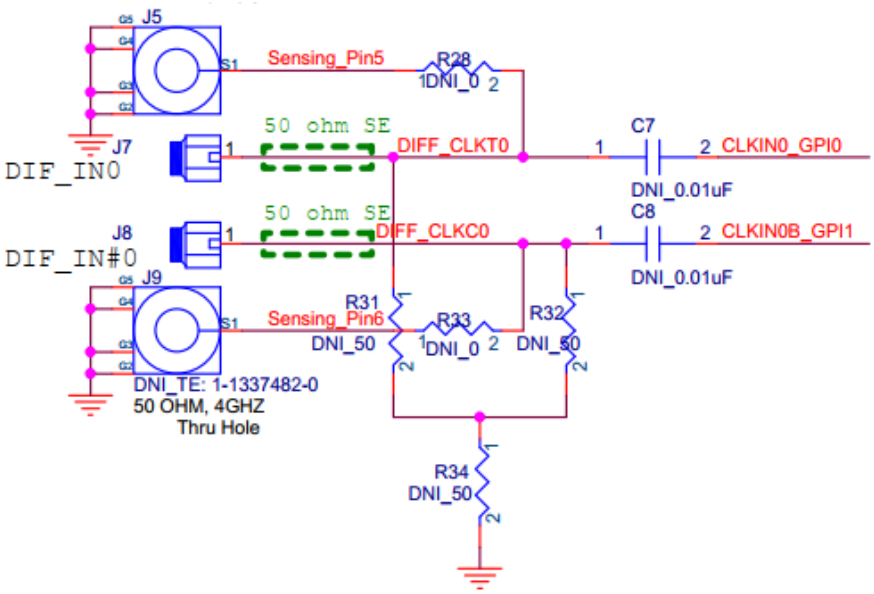


Figure 6. CLKIN0 Schematic

1.2.4. Serial Connection

The EVB can be connected to a computer via a USB3.0 to USB-C connector. The on-board USB-to-MPSSE Bridge (FTDI FT232HQ) can handle the data communication. The +5V from the USB-C powers the on-board regulators.

The Bus Source connector J55 and Bus Type connector J57 can be used to select the source of the communication bus. The bus will be I²C for most communication but can also be SPI for specific tests. Pins 1 and 2 in J55 are SDA and SCL from the FTDI chip. Pins 3 and 4 pass the SDA and SCL to the I²C level shifter. To use the on-board FTDI chip, install jumpers on pins 1–3 and 2–4. The board will be shipped with these jumpers installed. Theoretically, any I²C adapter can be connected to pins 3 and 4 for SDA and SCL. Pin 6 can be used as the ground connection for the I²C connection. Pins 3, 4, 5 and 6 are arranged such that an Aardvark connector can be plugged onto pins 3, 4, 5 and 6 only (see Figure 9). The Bus Type connector J57 is added to select between I²C or SPI protocol.

For default I²C operation, jumpers are installed on pins 1–3 and 2–4 (see Figure 7).

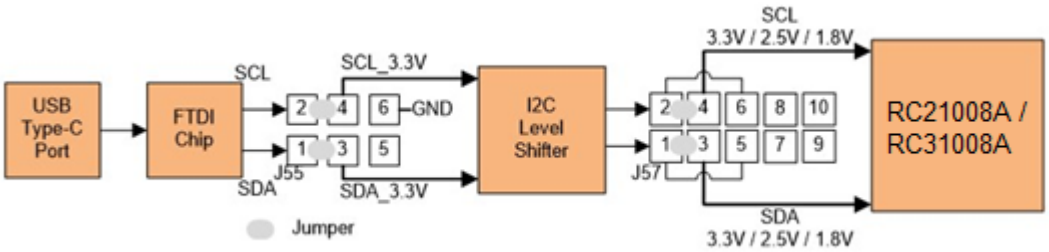


Figure 7. Communication Setup for I²C Mode

For SPI operation, RC21008A/RC31008A needs to be configured for SPI protocol on EVB Board. After RC21008A/RC31008A is configured for SPI, jumpers are installed on pins 5–7 and 6–8 for SPI SDA and SCL. SPI Chip Select is installed on pins 9–10 (see Figure 8).

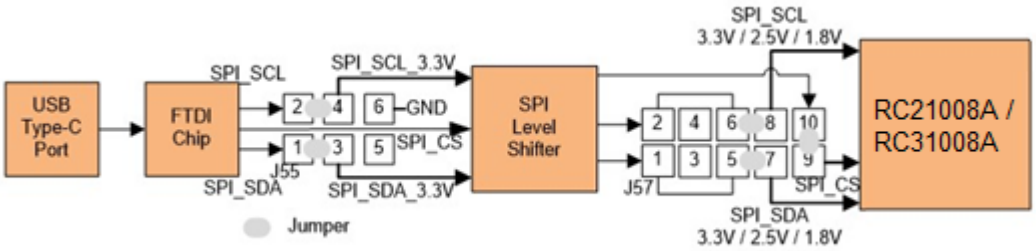


Figure 8. Communication Setup for SPI Mode

As shown in Figure 9, the Aardvark adapter communicates with the RC21008A/RC31008A.

Figure 9. Aardvark Adapter Connection to J55

1.2.5. On Board EEPROM

The EVB also supports an external EEPROM IC for loading of an RC21008A/RC31008A configuration programmed into the EEPROM as an option. The base address of the EEPROM is set in register 'eeprom_addr' and defaults to 0b101_0000. To be able to load the configurations from EEPROM, the serial interface mode must be set to I^2C in UserCfg in OTP. If not set to I^2C, the EEPROM load will be skipped.

The EVB provides a socket of 8-lead DIP8 for SOIC-8 package (Figure 10) of EPPROM IC so other EEPROMS of different memory size can be tested.

Figure 10. EEPROM in Socket

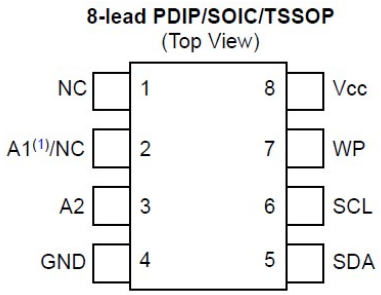


Figure 11. EEPROM Pin Description

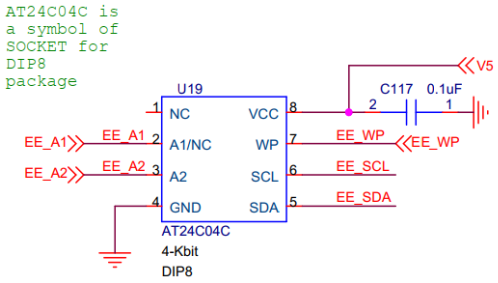


Figure 12. EEPROM Schematic

The A1, A2 pins are the EEPROM address inputs that can be pull either high or low using switch 6 and 7 on DIP switch SW2 to define the device address. By default both switches can be set in mid-position which means A1 and A2 are left floating as they are internally pulled down to GND.

The WP pin on pin 7 is the write-protect input. When WP pin is pulled down to GND (Low), the EEPROM is allowed to have normal write operations. When it is pulled up directly to VCC (High), all write operations are inhibited. Switch 8 on DIP switch SW2 on EVB is designed to support the function of write-protect to the EEPROM IC.

EEPROM support is available in RC21008A001/RC31008A001. This EVB does not support EEPROM. Please contact your local Renesas Sales for RC21008A001/RC31008A001.

1.2.6. GPI/GPIO DIP Switch Selectors

The EVB has two DIP switches (SW1, SW2) to support GPIO and GPI pins on RC21008A/RC31008A device. The middle position leaves the pin open so GPIO0, GPIO1, GPIO2, GPIO3, and GPIO4 could be configured to be 2-level (Hi / Low) as default selection on DIP switches. This is the default setting on EVB board for each switch. Move to the '+' side to pull the pin high and move to the '-' side to pull the pin low. In order for the GPI to function, populate C7, C8, C9, C10, R13, R20, R21, and R26 with 0 ohm. Dip switches SW1 and SW2 can be used to pull Hi or Low. LED D1–D8 can be used to indicate the state of the GPI/GPIO.

Table 4. SW1 Description

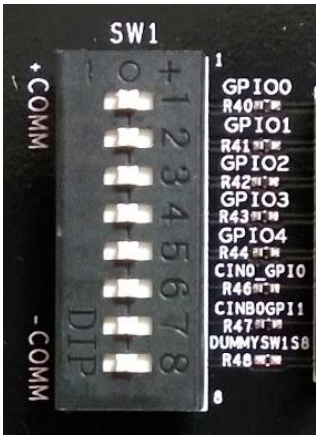


Figure 13. DIP Switch SW1

Switch 1 = GPIO0	Connects to pin 12 as General Purpose Input/Output 0. Set to middle position as default on EVB.
Switch 2 = GPIO1	Connects to pin 13 as General Purpose Input/Output 1. Set to middle position as default on EVB.
Switch 3 = GPIO2	Connects to pin 14 as General Purpose Input/Output 2. Set to middle position as default on EVB.
Switch 4 = GPIO3	Connects to pin 15 as General Purpose Input/Output 3. Set to middle position as default on EVB.
Switch 5 = GPIO4	Connects to pin 16 as General Purpose Input/Output 4. Set to middle position as default on EVB
Switch 6 = GPI0	Connects to pin 4 via R13 as General Purpose Input 0. Set to middle position as default on EVB.
Switch 7 = GPI1	Connects to pin 5 via R20 as General Purpose Input 1. Set to middle position as default on EVB.
Switch 8 = Dummy	No connection.

Table 5. SW2 Description

Figure 14. DIP Switch SW2

Switch 1 = GPI2	Connects to pin 7 via R21 as General Purpose Input 2. Set to middle position as default on EVB.
Switch 2 = GPI3	Connects to pin 8 via R26 as General Purpose Input 3. Set to middle position as default on EVB.
Switch 3 = Dummy	No connection.
Switch 4 = Dummy	No connection.
Switch 5 = Dummy	No connection.
Switch 6 = SW_EE_A2	Connects to pin 2 of an External EEPROM to set the I^2C address. Set to middle position as default on EVB.
Switch 7 = SW_EE_A1	Connects to pin 3 of an External EEPROM to set the I^2C address. Set to middle position as default on EVB.
Switch 8 = SW_EE_A0	Connects to pin 7 of an External EEPROM to set if the IC is set to write protection or not. Set to middle position as default on EVB.

1.2.7. Outputs

Each of the eight differential output pairs can be programmed (out_mode) to LVDS, LP-HCSL or CMOS logic type. CMOS is a single ended logic type and the output pair will essentially be two CMOS outputs of the same frequency.

LP-HCSL is the most versatile output because it can be customized. The LP-HCSL driver is simply a voltage push-pull driver. The RC21008A/RC31008A LP-HCSL can be programmed (out_lpamp) to two different amplitudes (800mV, and 900mV). The slew rate can be programmed (out_lpsr) to slow, 2–4 V/ns or fast, > 4V/ns. The output impedance can be programmed (out_lpimp) to 100Ω or 85Ω differential. When AC coupled, the LP-HCSL driver can be compatible with LVDS and LVPECL signal swing requirements.

For CMOS output type, output phase can be programmed (out_prog0 or out_prog1) to be out-of-phase or in-phase. Each output can also be tri-stated (out_prog2/out_prog3). The slew rate can also be programmed (out_cmdrv) to 4.2/2.7/3.4 V/ns for 3.3V, 2.7/1.5/2.0 V/ns for 2.5V, or 1.8/1.9 V/ns for 1.8V.

RC21008A/RC31008A is default with LP-HCSL output type on all outputs of EVB.

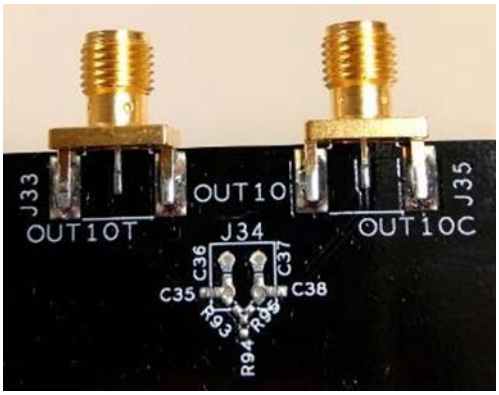


Figure 15. Output Termination with SMA Connector

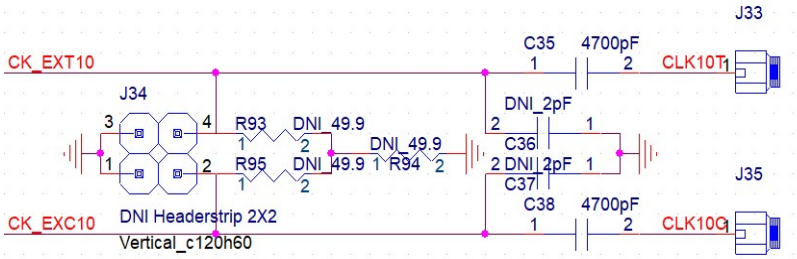


Figure 16. Output Termination with Bias Schematic

Figure 15 shows the default output termination for LP-HCSL with AC coupled SMA connectors (J33, J35).

1.2.8. Power and USB-C Connection to Computer Host

As mentioned in section 1.2.4, the EVB is connected to a computer via the USB3.0 to USB-C cable. It is recommended that the cable is connected to a USB3.0 port. However, a USB2.0 port acceptable due to the RC21008A/RC31008A part drawing less than 500mA. The USB-C provides +5V as power source to the on-board regulators. The on-board regulators support 3.3V, 2.5V and 1.8V voltages to the entire EVB. These voltages can be set by various jumpers found around the RC21008A/RC31008A.

The voltage source can be either from on-board voltage regulators for 3.3V, 2.5V, 1.8V or from VDD_J banana connector. The banana connector can connect to a bench supply and the connection can be used to measure total supply current into pins as reference. When all powers are selected from VDD_J power jack, the USB connection will still be needed in order to connect to computer for programming RC21008A / RC31008A using RICBox.

In Figure 17, the source for pin VDDO1 (J40) is chosen to be 3.3V. If VDD_J is provided, the jumper can be moved to the bottom of header J40.

Figure 17. Power Source from USB Connector

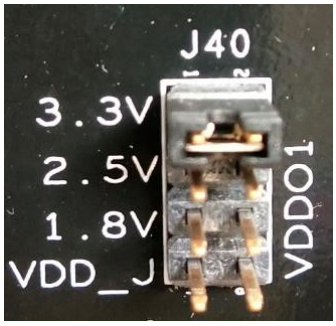


Figure 18. Power Source Selection

1.2.9. Renesas Integrated Circuit Toolbox (RICBox)

The Renesas Integrated Circuit Toolbox (RICBox) software can program the RC21008A/RC31008A on the EVB using either the on board FTDI chip or Aardvark tool. RICBox provides a user-friendly interface to support programming configurations into the RC21008A/RC31008A on the board. For more information about RICBox, see the Renesas IC Toolbox User Guide.

To program the RC21008A/RC31008A using RICBox software:

1. Connect U16 on the EVB to the user's computer using a USB cable.
2. Launch RICBox as described in the user guide.
   a. The software and guide are downloadable from the product page.
3. For a new configuration, click on "Create new project"

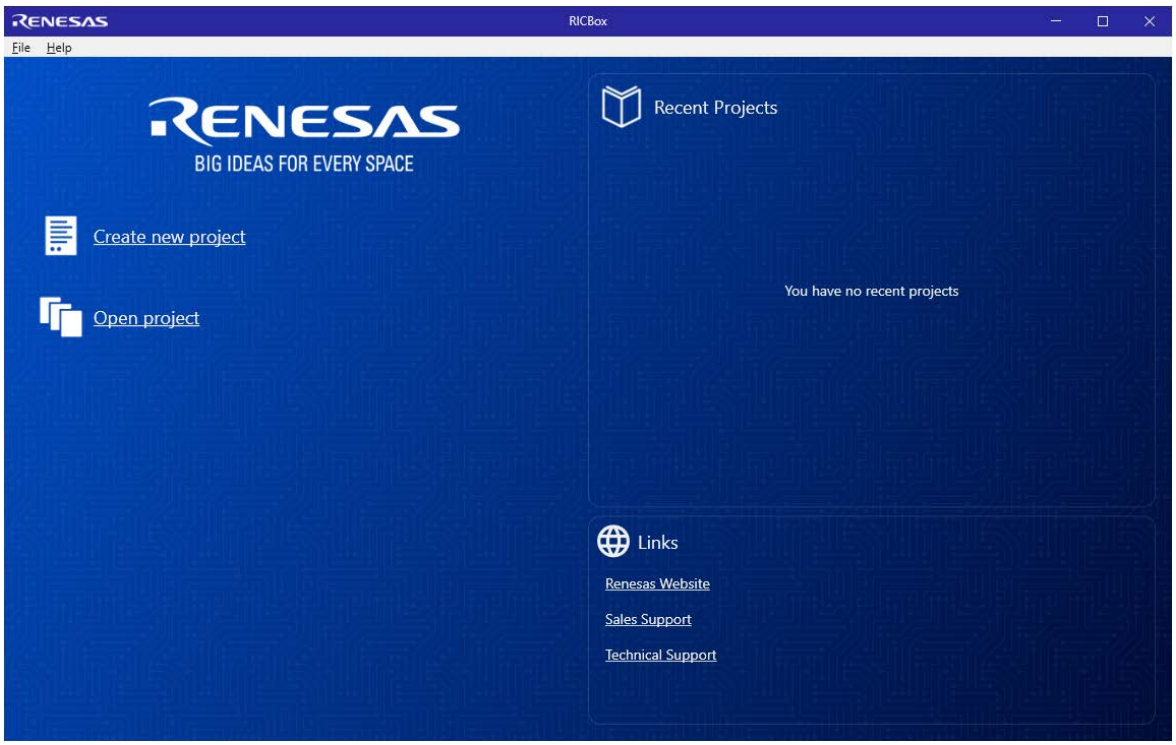


Figure 19. RICBox Start Page

4. Select the product family (VersaClock7), then select a product variant (part number) and click *OK*.

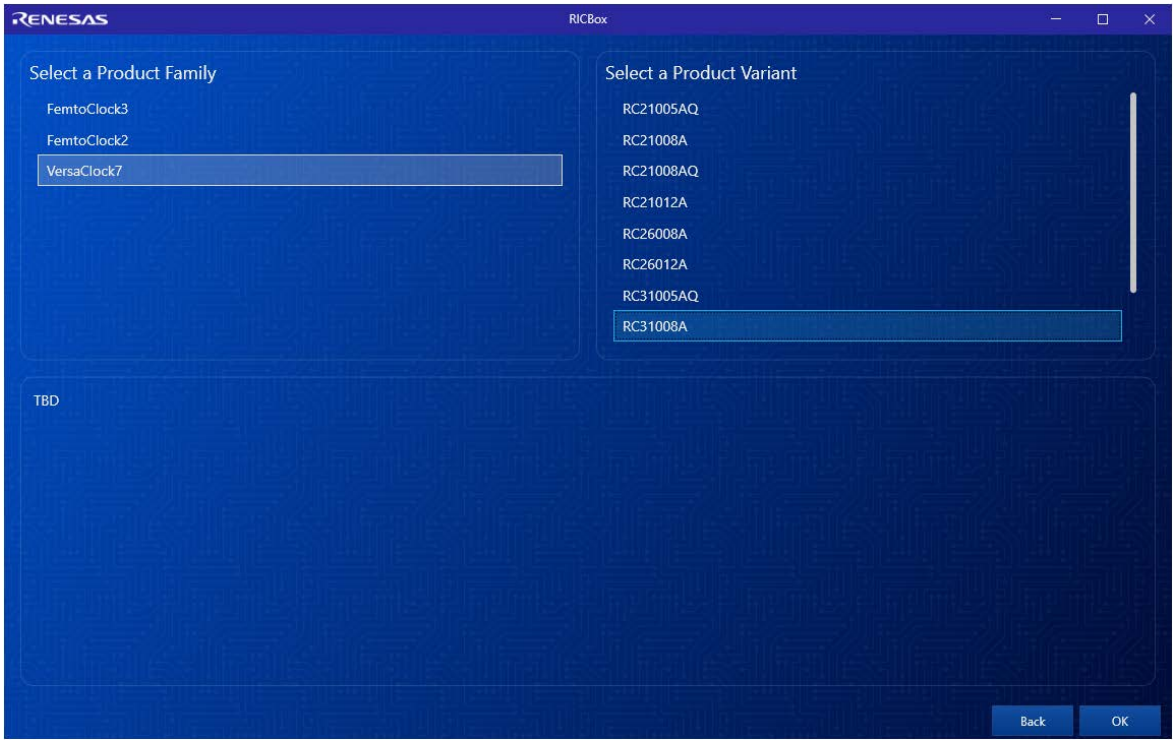


Figure 20. Select Product Family and Variant

5. On the Inputs wizard page (Figure 21), the operation mode can be chosen from Synthesizer, Jitter Attenuation, or DCO. Expected crystal frequency needs to be entered. The C_L can also be set internally between 6pF to 12pF. If a reference clock is needed as an alternate clock source or for jitter attenuation, the expected frequency and type can be set in the Reference Clocks section.

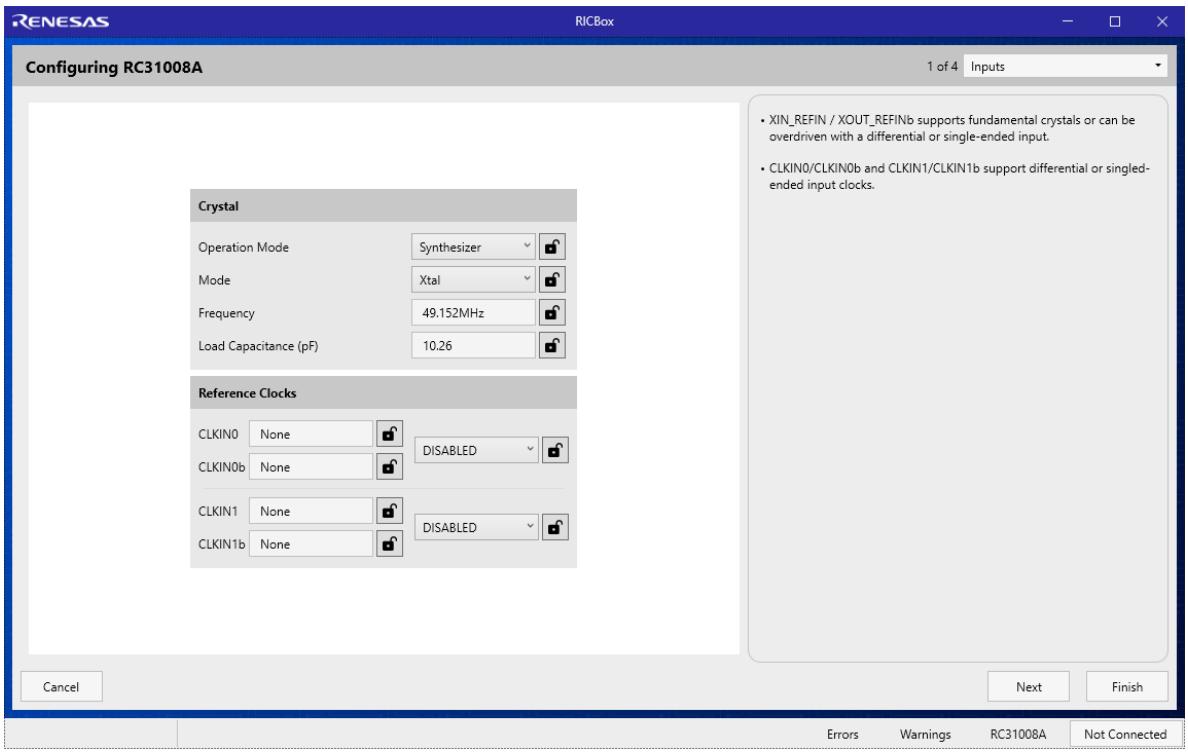


Figure 21. Inputs Wizard Page

6. There are two fractional output dividers (FOD0, FOD1) that support spread spectrum clocking (SSC). Any output bank that can utilize either FOD can be configure for SSC. First step is to “Enable” the feature. Then choose the “Mode” of SSC either down or center spread. Next, enter in the amount of spread. For down spread acceptable values range from 0 to 0.5%. For center spread, acceptable values range from -0.25% to 0.25%. Finally, choose a modulation frequency. Acceptable values range from 30kHz to 63kHz.

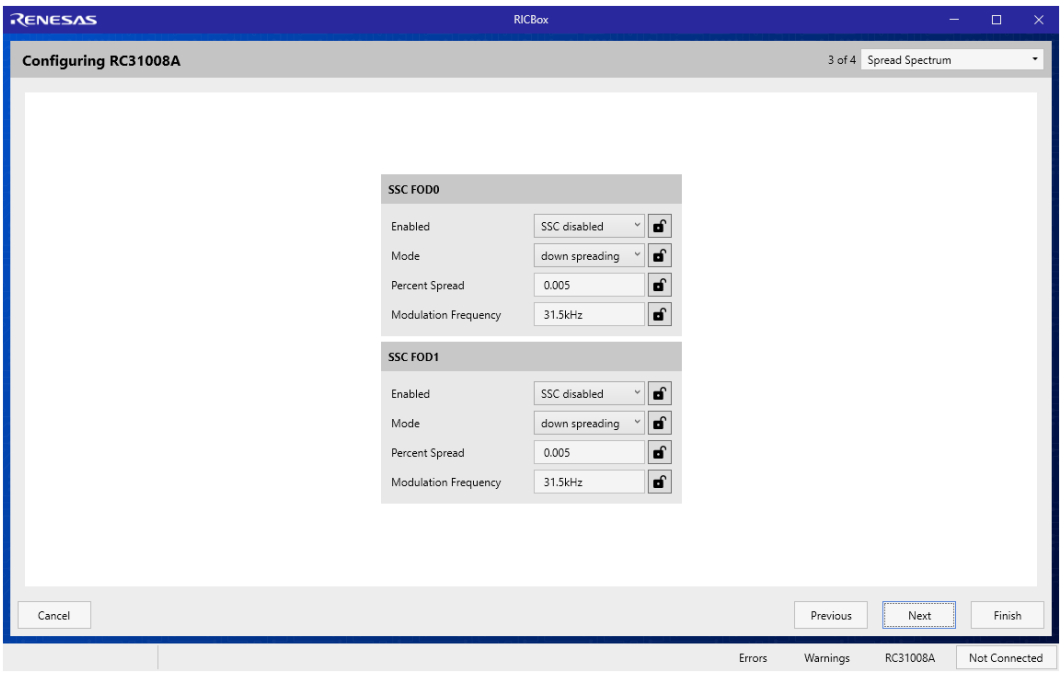


Figure 22. Spread Spectrum Clocking Wizard Page

7. Configure the output bank settings which includes the divider source (IOD0/1/2/3 or FOD0/1/2), output frequency and output mode (LPHCSL, LVDS, and CMOS). If a bank is to be unused, use the “Power Down” check box to turn off the bank. Click on the *Settings* icon to adjust amplitude, impedance, and slew rate for each output.

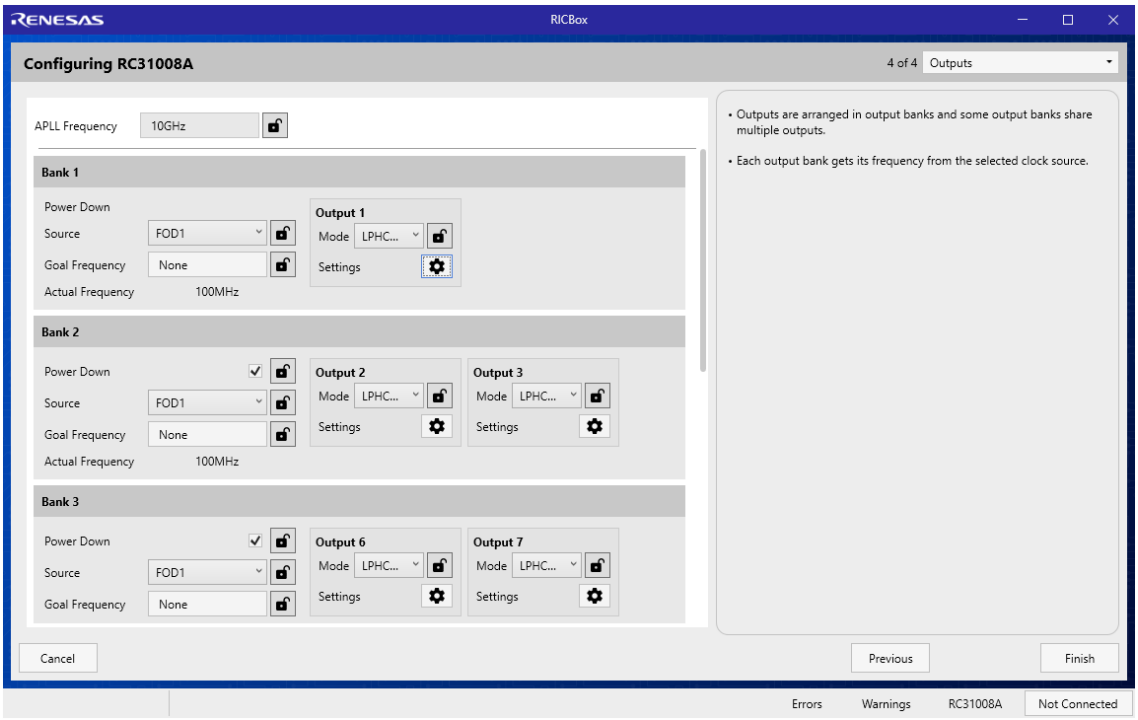


Figure 23. Outputs Wizard Page

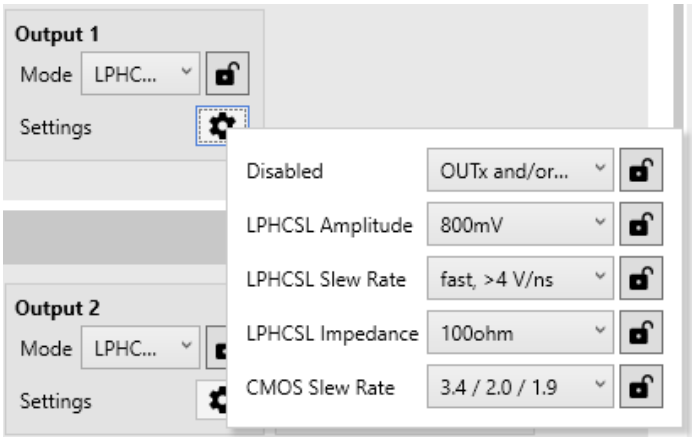


Figure 24. Advanced Output Settings

8. Click the *Finish* button to view the summary of the configuration.

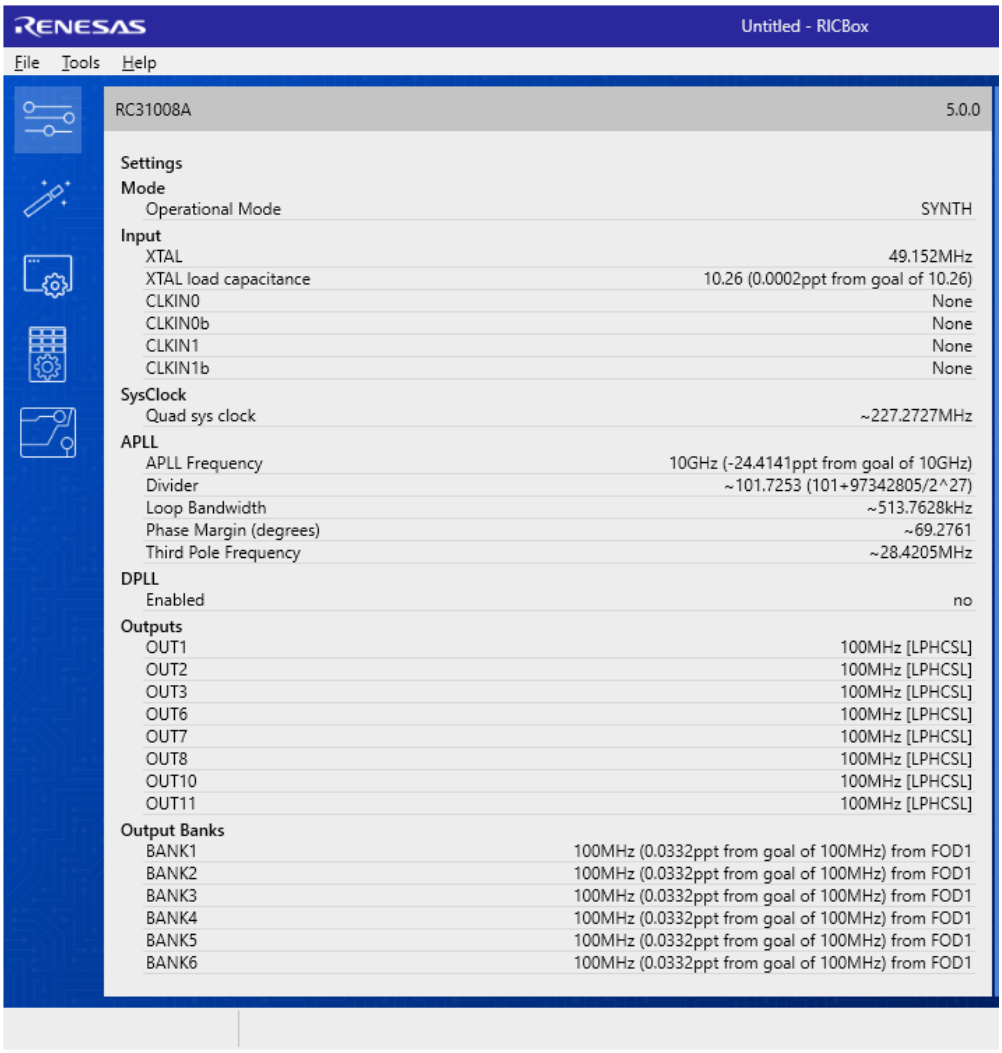


Figure 25. Configuration Summary

9. To go back to any of the previous wizard pages, click the wizard icon. 
10. RICBox is now ready to connect to RC21008A/RC31008A. Click the *Not Connected* button in the lower right part of RICBox tool. Then click *Connect*.

Figure 26. Connect to VC7

11. The “Not Connected” button will turn green and changed to “Connected”. Click the button again to “Program” the part.

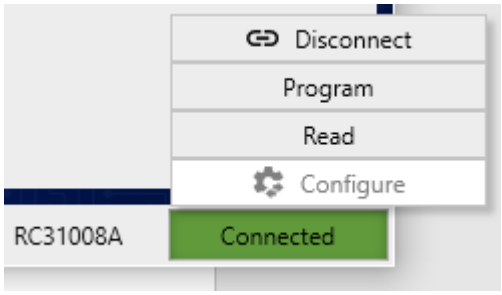


Figure 27. Program VC7

12. View the block diagram by clicking on the Block Diagram icon.

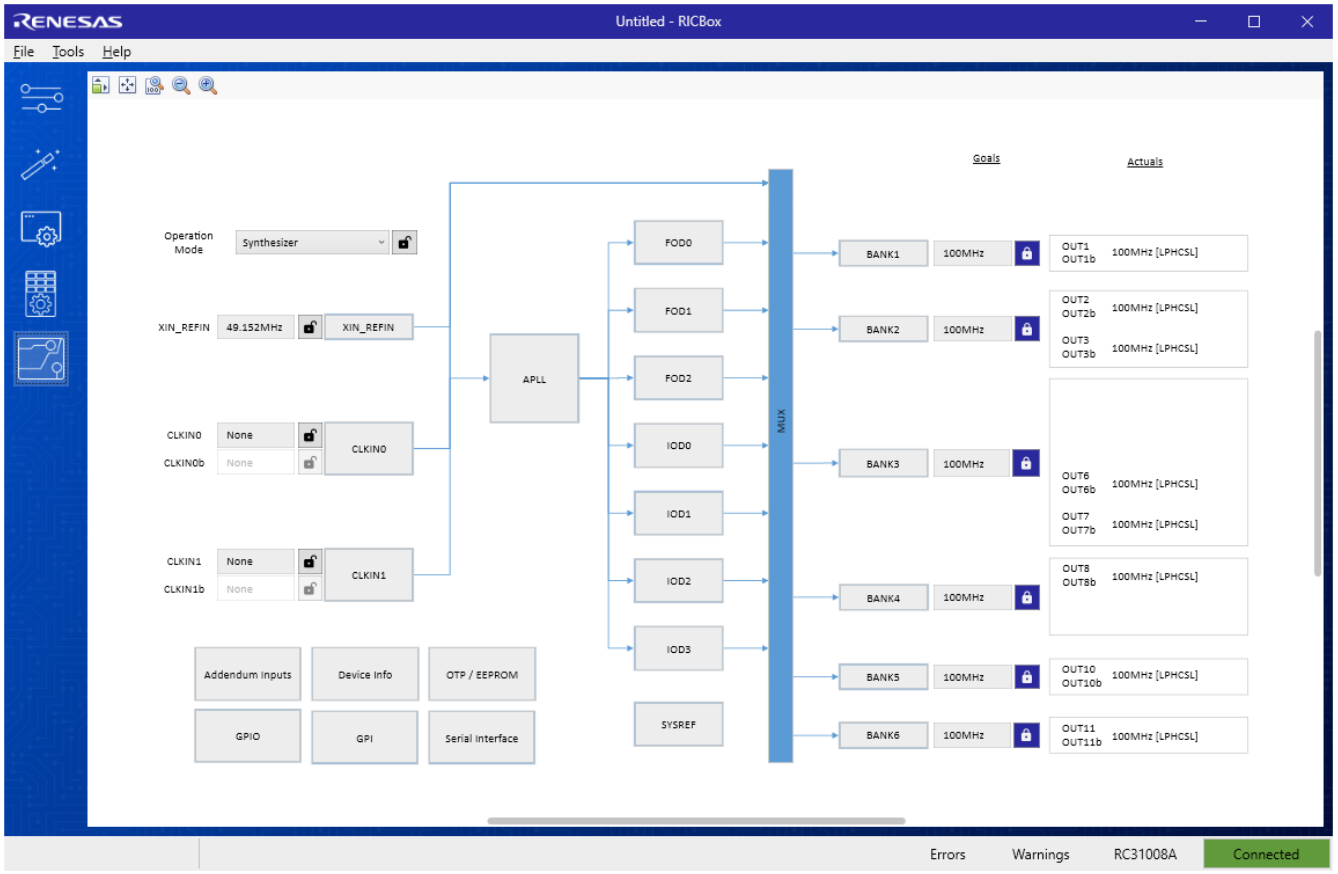


Figure 28. Block Diagram

13. From the “Operation Mode” pull-down, click “Jitter Attenuator” mode (for RC31008A and RC31012A). This selection will show DPLL.

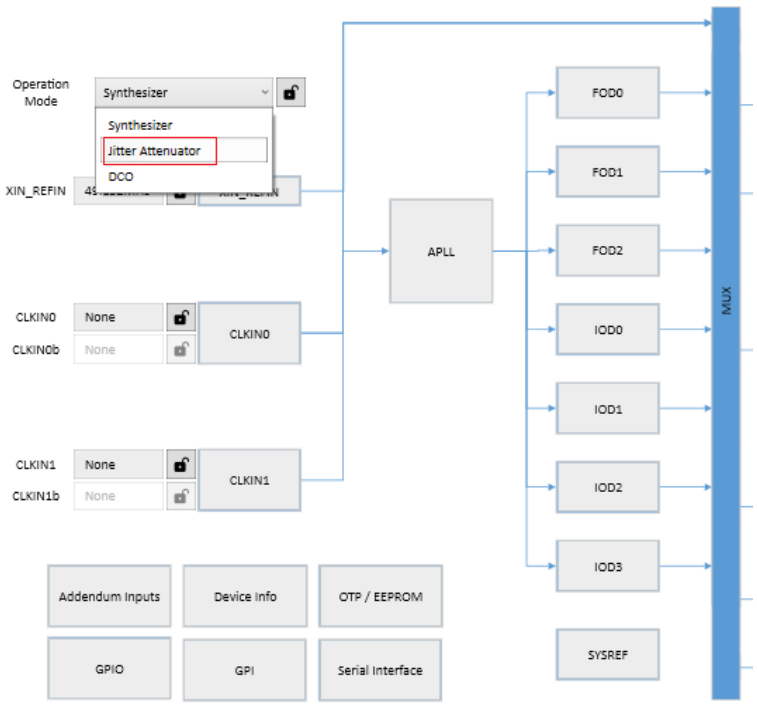


Figure 29. Selecting Jitter Attenuator Mode from Operation Mode Menu

14. Once JA mode is selected, if no input clock is configured, RICBox will flag a warning for missing input clock for DPLL, as shown below. This warning will disappear when one or both input clocks are configured.

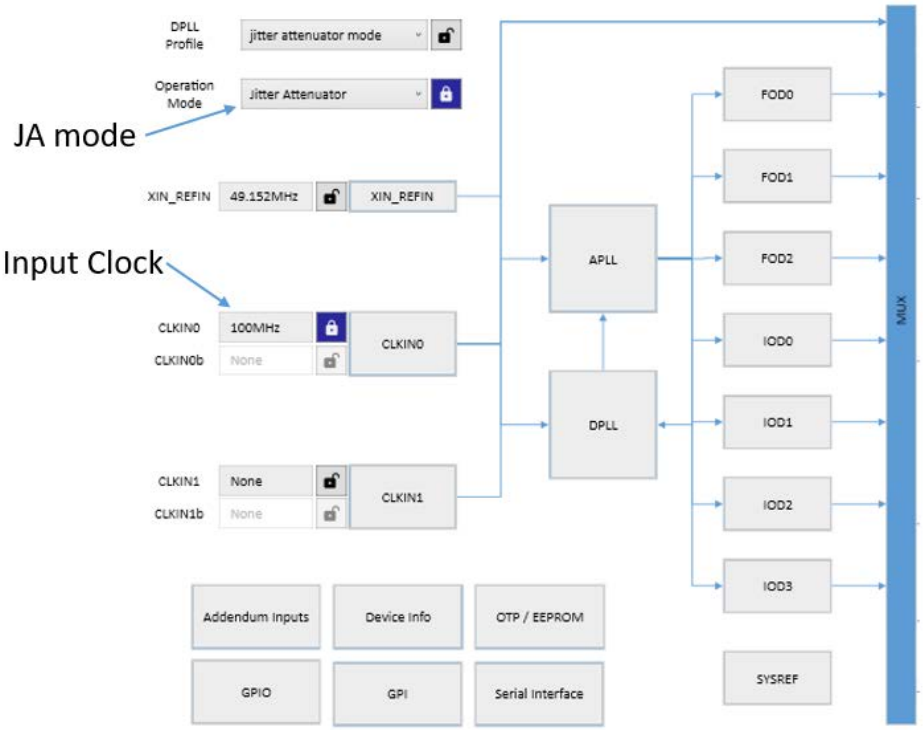


Figure 30. Input Clock is Required in JA mode

2. Evaluation Board Components

2.1 Layout Guidelines

For designing the layout around the RC21008A/RC31008A, the following items need to be considered.

2.1.1. EPAD

Make sure there are enough vias to allow for proper thermal dissipation. The EPAD may be connected to VEE (negative power supply) to allow for split power planes for different input/outputs styles.

2.1.2. Crystal/Reference Input

Place the crystal as close to VC7 device as possible. Make XIN/XOUT trace lengths the same. For external tuning caps, connect them from XIN/XOUT to EPAD reference voltage. For single-ended reference input, route only the REFIN trace as single ended 50Ω. For differential input, route differential 50Ω.

2.1.3. Clock Inputs

For a single-ended clock input, route traces single-ended 50Ω. For a differential input, route differential 50Ω. Add inline capacitors to support AC coupling if needed.

2.1.4. Serial Connection

The serial interface can function from 1.8V to 3.3V for VDDD. If serial communication is needed, the SCL and SDA pull-up resistor need to connect to VDDD. Use a level translator if needed. If loading from EEPROM, the logic levels must match VDDD. Acceptable values for pull-up resistors are 1kΩ to 10kΩ. It is recommended to route the serial signals close to each other.

2.1.5. GPI/GPIO

In order to utilize GPI, clock inputs must be disabled as they share the same pins. The logic levels are determined by VDDD relative VEE. The GPI/GPIO can be configured to have internal pull-up/down. Signals should be routed to minimize return loops.

2.1.6. Outputs

For CMOS outputs type, route a single-ended 50Ω and place an inline 33Ω resistor near the VC7 device. For differential outputs type, route a differential 50Ω. For LP-HCSL, an inline 7.5Ω resistor near the device is needed if output impedance is set to 85Ω. For LVDS, add 100Ω across P and N if the receiver does not have termination built in. Inline capacitors may be used to AC couple the outputs as needed.

2.1.7. Power

Please follow the recommended schematic for power filtering. Each 0.1µF needs to be placed as close as possible to the respective VC7 power pin.

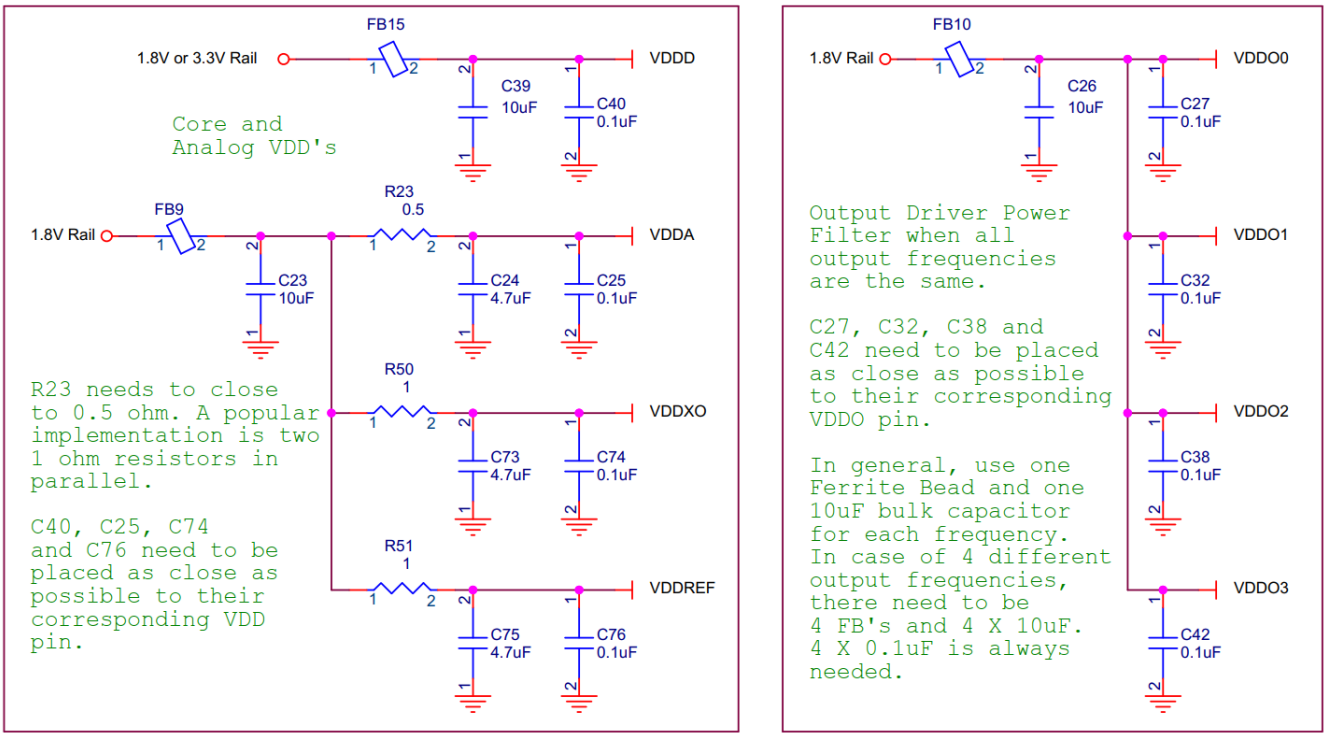


Figure 31. Power Supply Filtering

2.2 Schematic Diagrams

Schematic diagrams are located at the end of this document and accessible from the links below:

RC21008A/RC31008A Evaluation Board Schematics

RC21012A/RC31012A Evaluation Board Schematics

2.3 Bill of Materials

Qty	Reference	Description	Manufacturer	Part Number
22	C11,C12,C17,C18,C19,C21,C24,C26,C27,C29,C32,C34,C35,C38,C39,C42,C50,C59,C67,C75,C85,C93	CAP CER 4700PF 10V U2J 0402	Murata Electronics	GRM1557U1A472JA01D
50	C43,C46,C47,C49,C51,C54,C56,C58,C60,C63,C65,C66,C68,C71,C72,C74,C78,C80,C82,C84,C86,C88,C90,C92,C96,C98,C100,C102,C105,C106,C107,C108,C109,C110,C111,C114,C115,C116,C117,C118,C119,C120,C121,C144,C147,C148,C150,C151,C155,C156	CAP CER 0.1UF 16V X7R 0402	Murata Electronics	GRM155R71C104KA88D
21	C44,C45,C48,C52,C55,C57,C61,C64,C70,C73,C76,C77,C83,C87,C91,C95,C101,C103,C104,C145,C149	CAP CER 10UF 6.3V X7T 0603	Murata Electronics	GRM188D70J106MA73D
3	C53,C62,C146	CAP CER 4.7UF 10V X5R 0402	Murata Electronics	ZRB15XR61A475ME01
3	C79,C89,C97	CAP CER 22UF 6.3V X6S 0603	Murata Electronics	GRM188C80J226ME15D
2	C112,C113	CAP CER 27PF 25V C0G/NP0 0402	Murata Electronics	GRM1555C1E270J
3	C157,C158,C159	CAP CER 1UF 10V X7S 0402	Murata Electronics	GCM155C71A105KE38D
11	D1,D2,D3,D4,D5,D6,D7,D8,D9,D10,D12	LED GREEN CLEAR CHIP SMD	Kingbright	APT3216CGCK
1	D11	DIODE GEN PURP 80V 125MA 2DFN	Diodes Incorporated	1N4448HLP
18	FB1,FB2,FB3,FB4,FB5,FB6,FB7,FB8,FB9,FB10,FB11,FB12,FB13,FB14,FB15,FB16,FB18,FB19	FERRITE BEAD 600 OHM 0603 1LN	Murata Electronics	BLM18AG601SN1D
22	J2,J3,J7,J8,J11,J12,J15,J16,J19,J20,J21,J22,J25,J26,J27,J29,J31,J32,J33,J35,J36,J38	Conn SMA 0Hz to 18GHz 50Ohm Solder ST Edge Mount F Gold	Cinch Connectivity Solutions	142_0701_851
2	J6,J14	CONN HEADER VERT 8POS 2.54MM	Molex	22284083
10	J39,J40,J43,J44,J45,J48,J49,J52,J53,J54	CONN HEADER VERT 8POS 2.54MM	Molex	10-89-7080

Qty	Reference	Description	Manufacturer	Part Number
1	J41	Test Sockets SINGLE PCB SOCK BLK	Deltron	571-0100
1	J42	Test Sockets SINGLE PCB SOCK RED	Deltron	571-0500
4	J46,J47,J50,J51	HEX STANDOFF M3X0.5 NYLON 20MM	Harwin Inc.	R30-1612000
4	NA	MACH SCREW PAN HEAD PHILLIPS M3	Essentra Components	NMS-306
1	J55	CONN HEADER VERT 6POS 2.54MM	Molex	10897062
1	J58	CONN HEADER VERT 6POS 2.54MM	Molex	10897062
1	J56	CONN HEADER VERT 1POS	Amphenol ICC (FCI)	68000-401HLF
1	J57	CONN HEADER VERT 10POS 2.54MM	Molex	10-89-7100
2	J75,J76	CONN HEADER VERT 4POS 2.54MM	Molex	10897042
4	J85,J86,J87,J88	CONN SMA RCPT STR 50 OHM PCB	Molex	7.34E+08
33	R1,R3,R5,R6,R7,R8,R9,R10,R12,R13,R14,R15,R16,R20,R21,R22,R23,R24,R26,R27,R29,R30,R166,R167,R201,R202,R222,R223,R235,R236,R237,R238,R239	RES SMD 0 OHM JUMPER 1/10W 0402	Panasonic Electronic Components	ERJ-2GE0R00
12	R40,R41,R42,R43,R44,R46,R47,R54,R62,R71,R72,R73	RES 1K OHM 1% 1/16W 0402	Vishay Dale	CRCW04021K00FK
10	R55,R56,R57,R58,R59,R60,R61,R63,R67,R200	RES 220 OHM 1% 1/16W 0402	Vishay Dale	CRCW0402220RFKED
1	U24			Qbuffer
5	R101,R102,R103,R104,R183	RES SMD 1 OHM 1% 1/16W 0402	Yageo	RC0402FR-071RL
1	R108	RES 220 OHM 1% 1/10W 0603	Vishay Dale	CRCW0603220RFK
1	R111	RES 18 KOHM 0.1% 1/16W 0603	Susumu	RGT1608P-183-B-T5
18	R118,R120,R132,R133,R134,R135,R136,R137,R204,R206,R207,R210,R211,R213,R215,R216,R217,R221	RES 4.7K OHM 1% 1/16W 0402	Vishay Dale	CRCW04024K70FK
1	R119	RES SMD 5.1K OHM 1% 1/16W 0402	Vishay Dale	CRCW04025K10FK
4	R121,R122,R123,R124	RES SMD 10 OHM 1% 1/16W 0402	Yageo	RC0402FR-0710RL

Qty	Reference	Description	Manufacturer	Part Number
1	R130	RES 12K OHM 1% 1/16W 0402	Vishay Dale	CRCW040212K0FK
11	R131,R224,R225,R226,R227,R228,R229,R230,R231,R232,R233	RES SMD 10K OHM 1% 1/16W 0402	Vishay Dale	RCG040210K0FK
1	R234	RES 27K OHM 1% 1/16W 0402	Vishay Dale	CRCW040227K0FK
2	SW1,SW2	SWITCH SLIDE DIP SPDT 25MA 24V	E-Switch	KAT1108E
1	U1	CRYSTAL 50.0000MHZ 8PF SMD	TXC CORPORATION	TXC: 7M-50.000MAHV-T Abracon: ABM8W-50.0000MHZ-8-D2X-T3
1	U3			RC21008A
10	U4,U5,U6,U7,U8,U9,U10,U11,U12,U23	MOSFET N-CH 50V 220MA SOT23-3	ON Semiconductor	BSS138
3	U13,U14,U15			RAA214020
1	U16	CONN RCP USB3.1 TYPEC 24P SMD RA	Amphenol ICC	12401598E4#2A
1	U17	USB Interface IC USB HS to UART/FIFO SPI/JTAG/I2C QFN-48	FTDI	FT232HQ-REEL
1	U18	CRYSTAL 12.0000MHZ 18PF SMD	Abracon LLC	ABM8G-12.000MHZ-18-D2Y-T
1	U19	IC EEPROM 4KBIT I2C 1MHZ 8DIP	Microchip Technology	AT24C04C-PUM
3	U20,U21,U22	IC REDRIVER I2C 1CH 8VSSOP	Texas Instruments	PCA9517

2.4 Board Layout

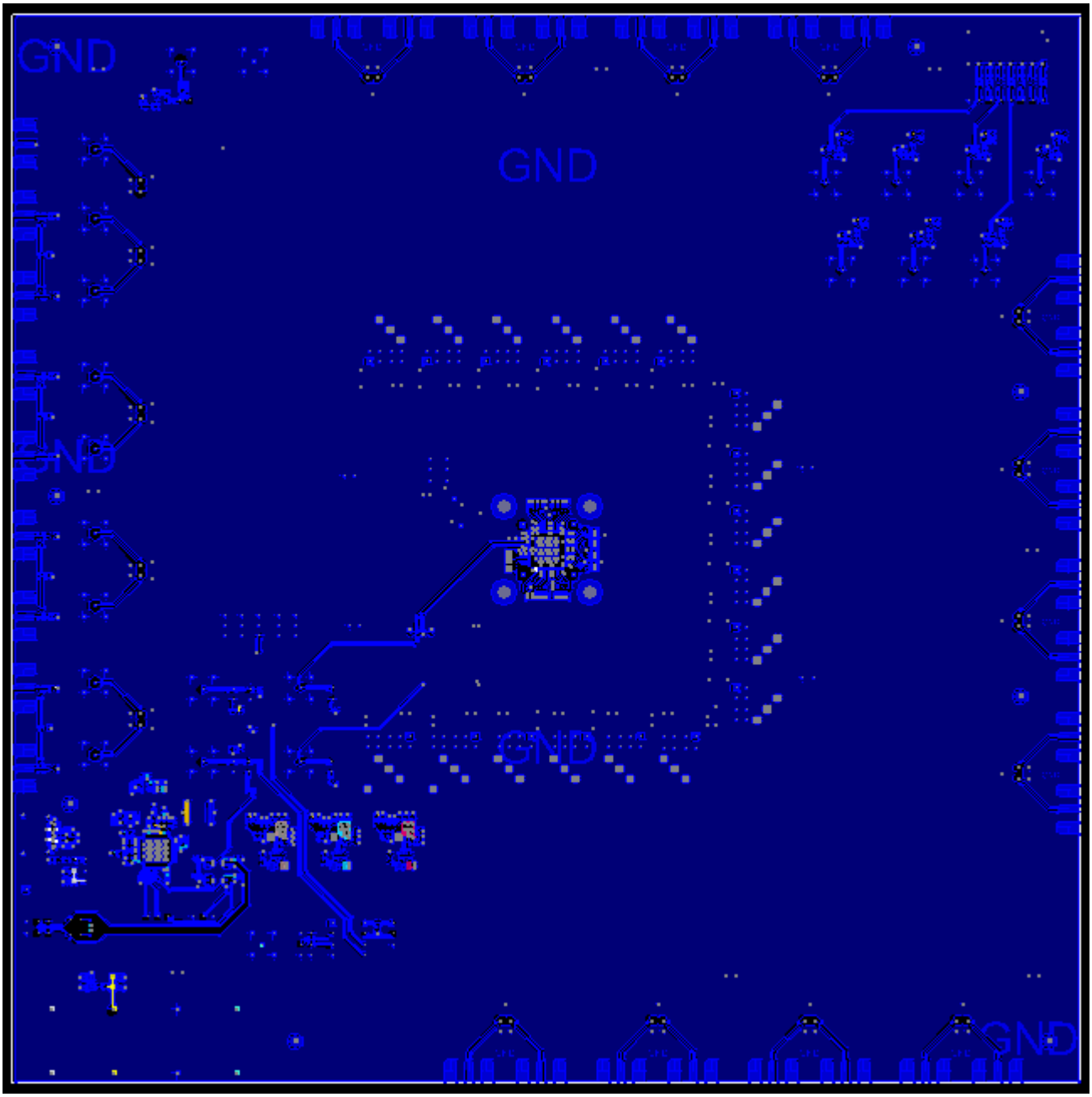


Figure 32. Layer 1–Top

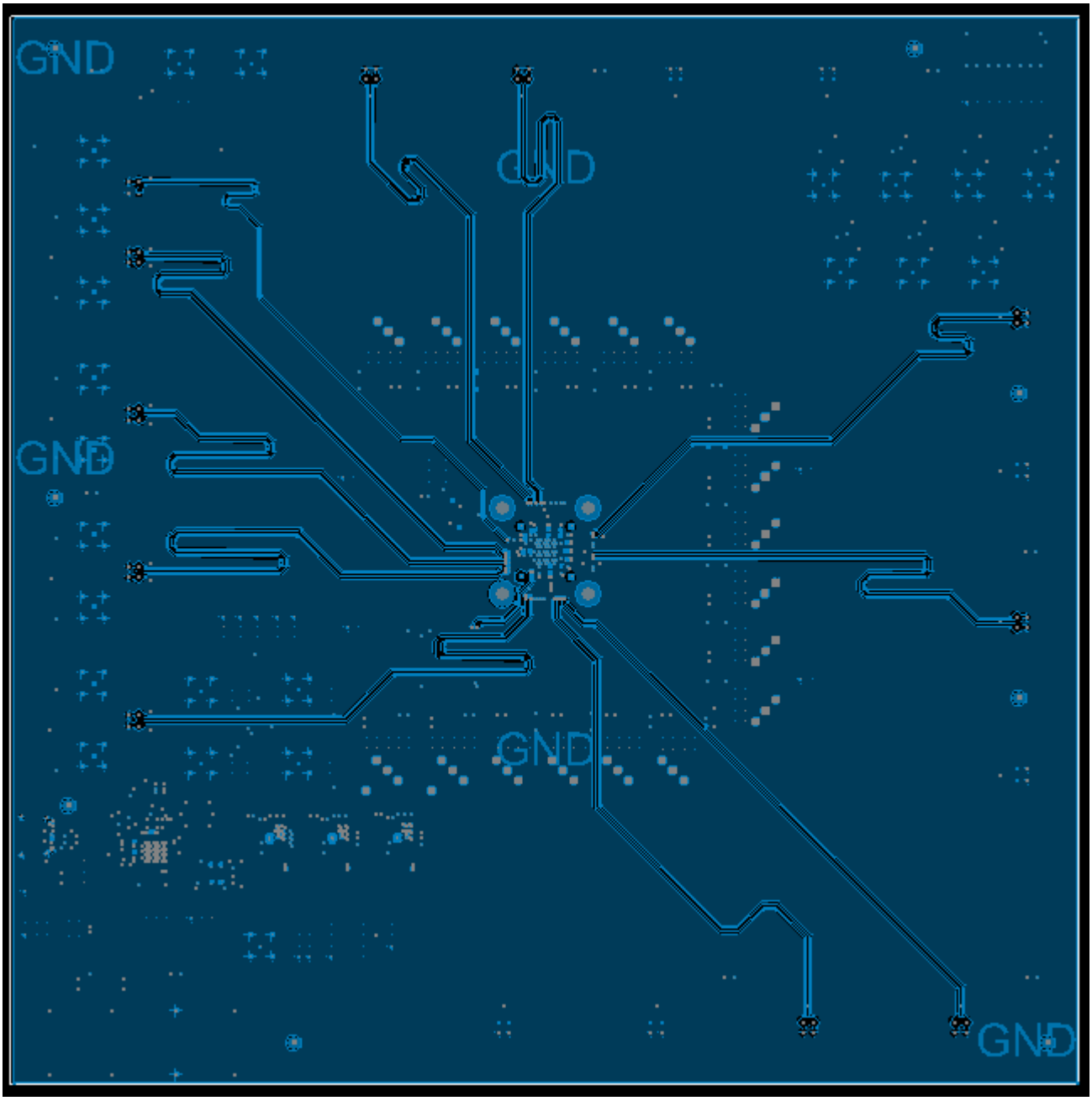


Figure 33. Layer 2–Signal

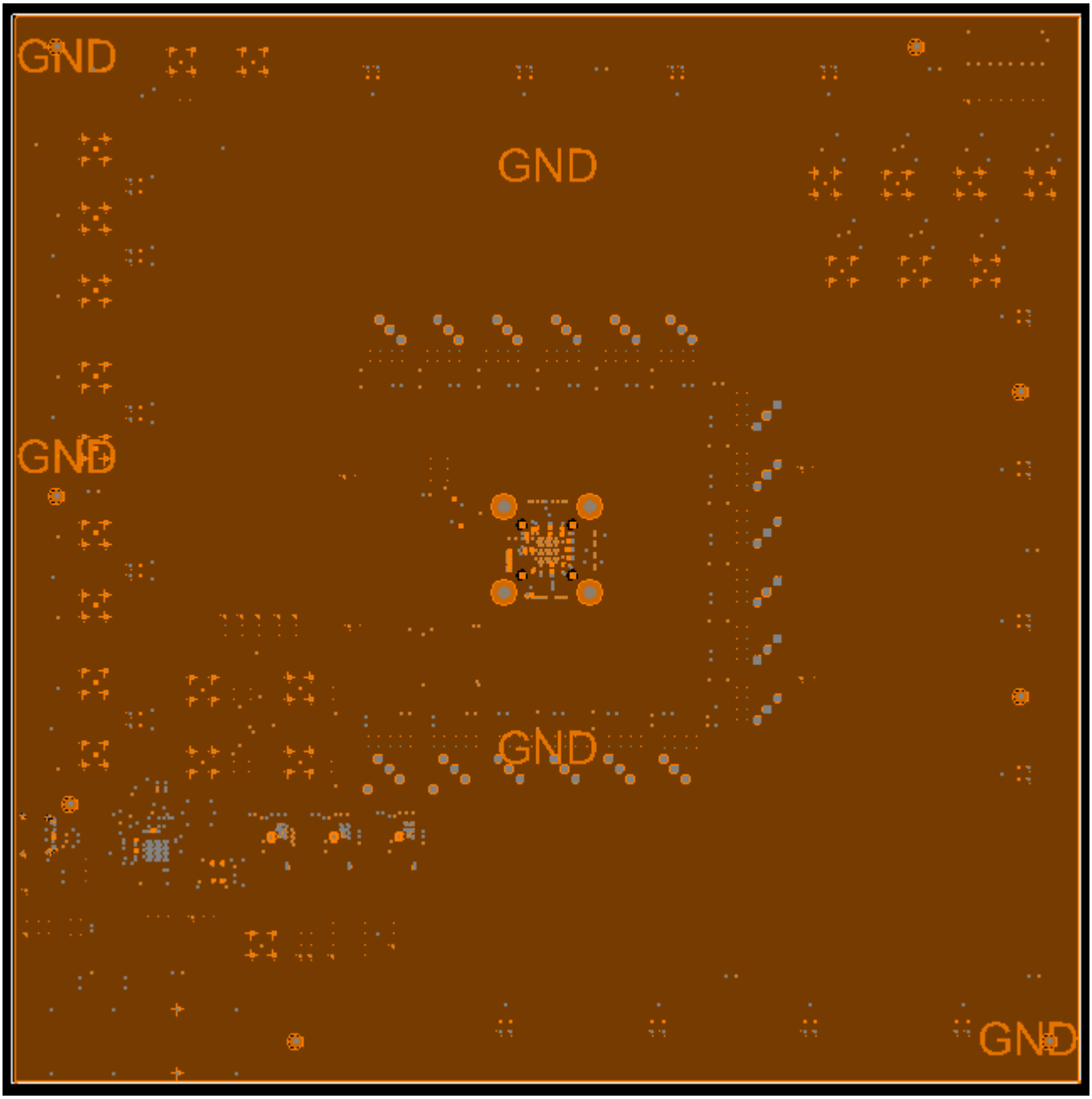


Figure 34. Layer 3–Ground Plane

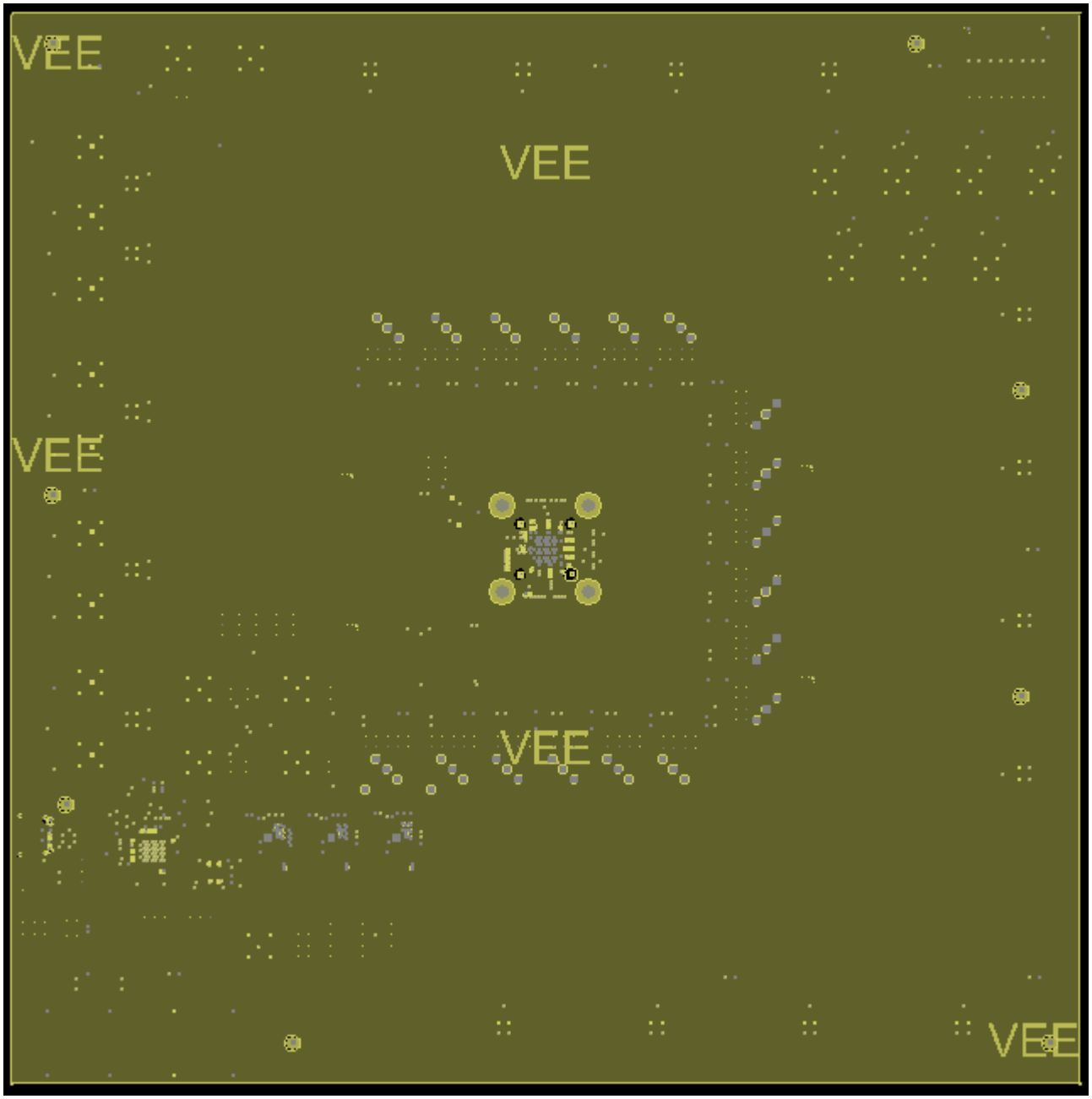


Figure 35. Layer 4–VEE Plane

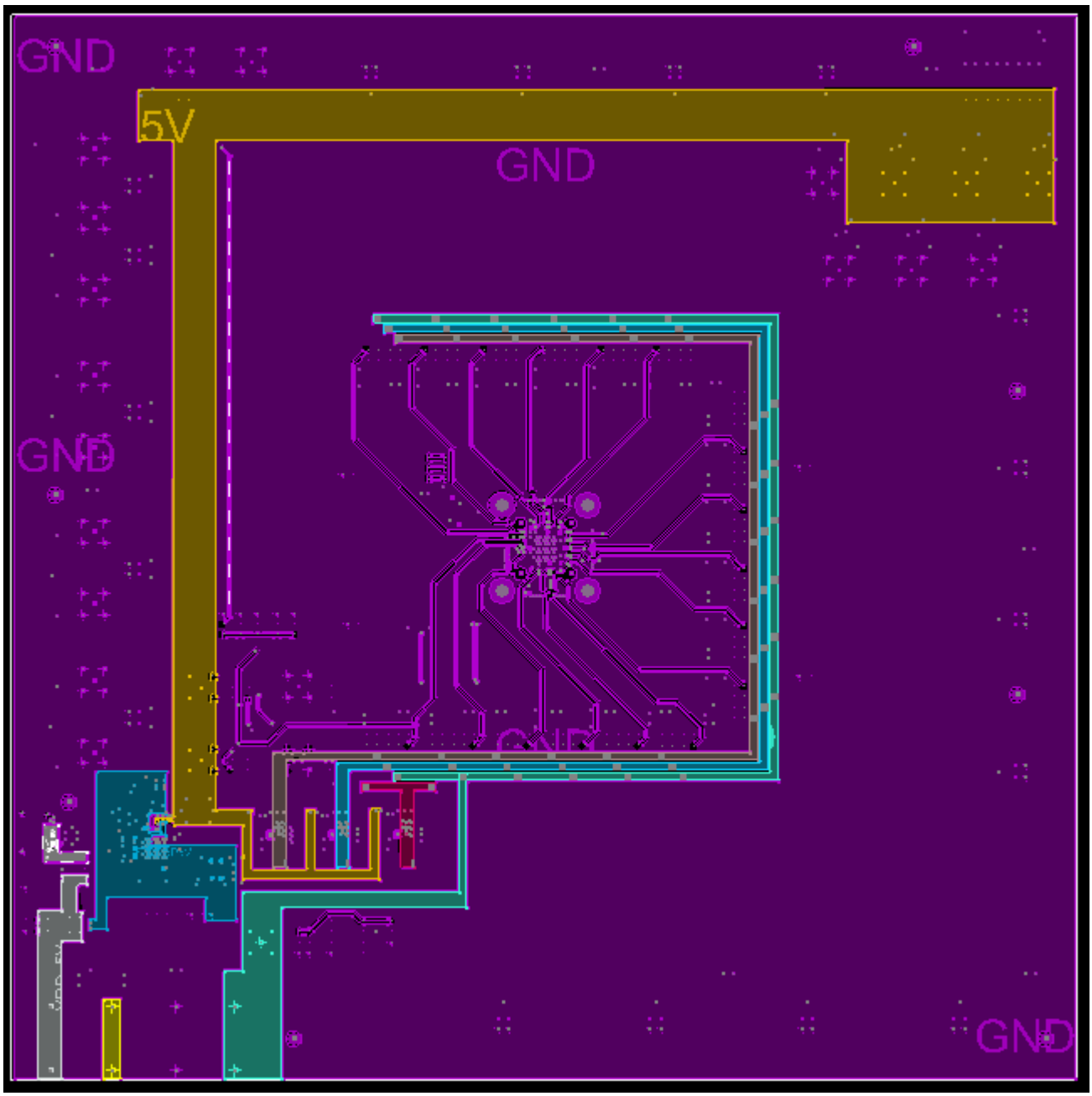


Figure 36. Layer 5–Power Plane

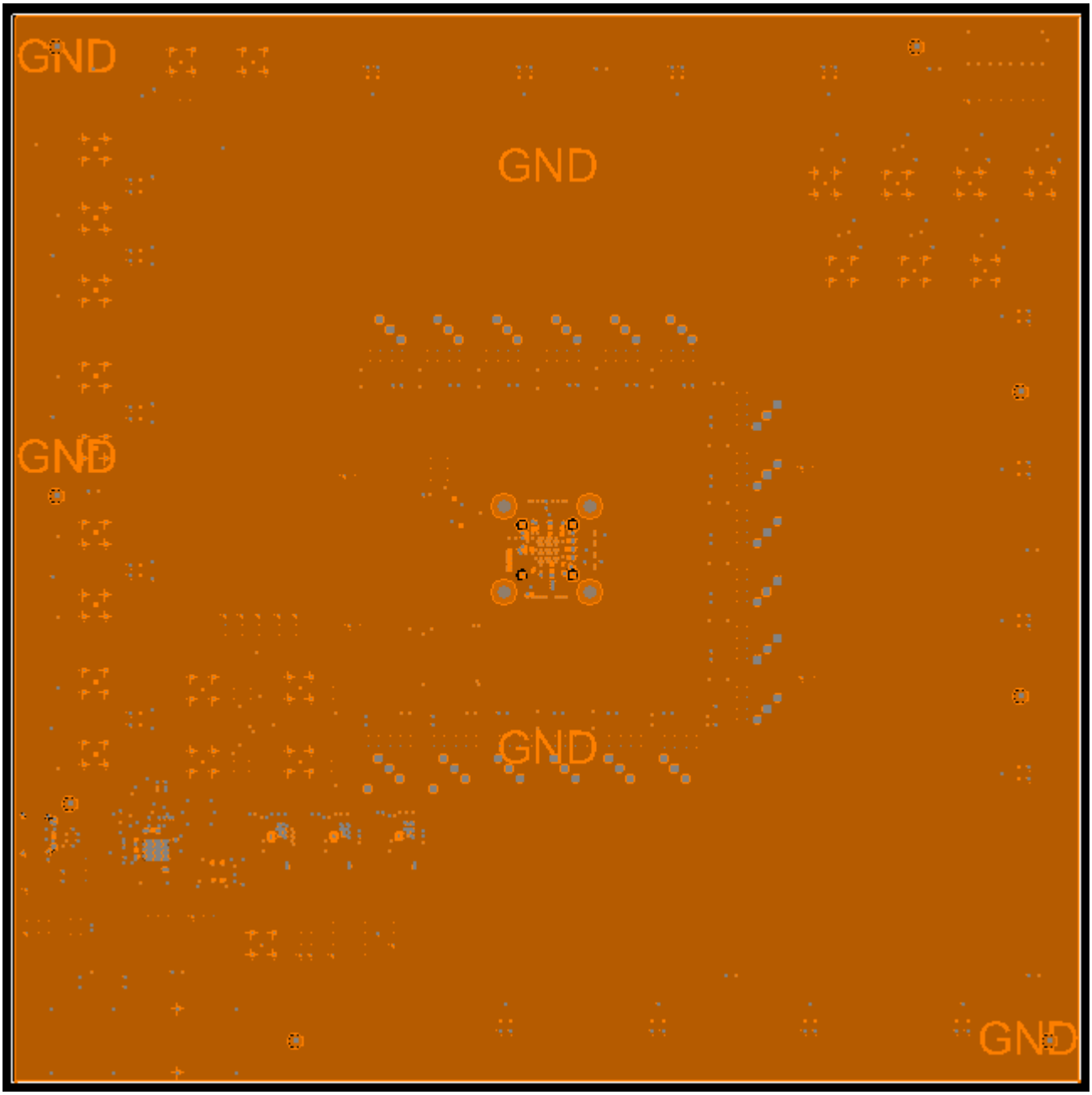


Figure 37. Layer 6–Ground Plane

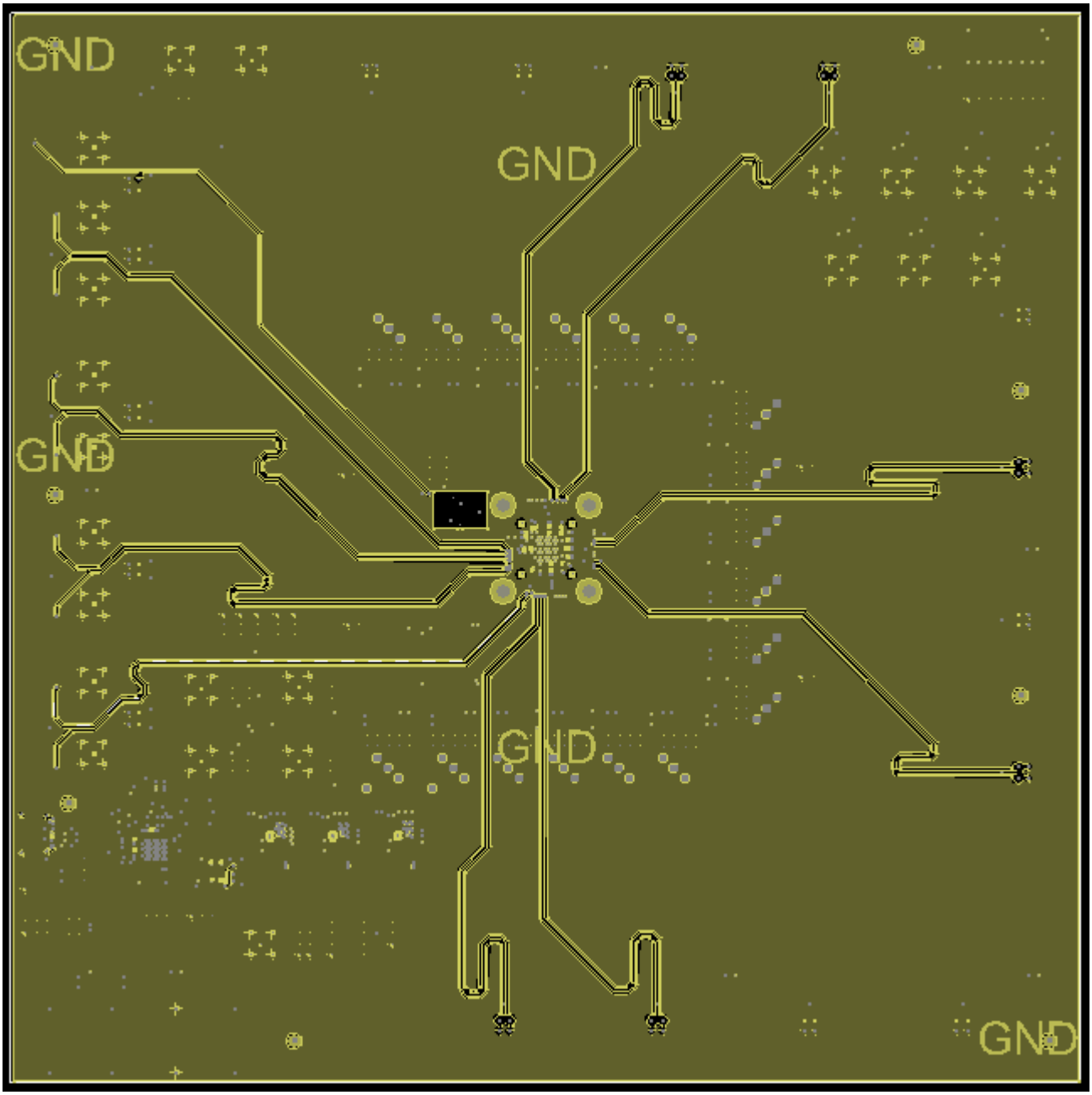


Figure 38. Layer 7–Signal

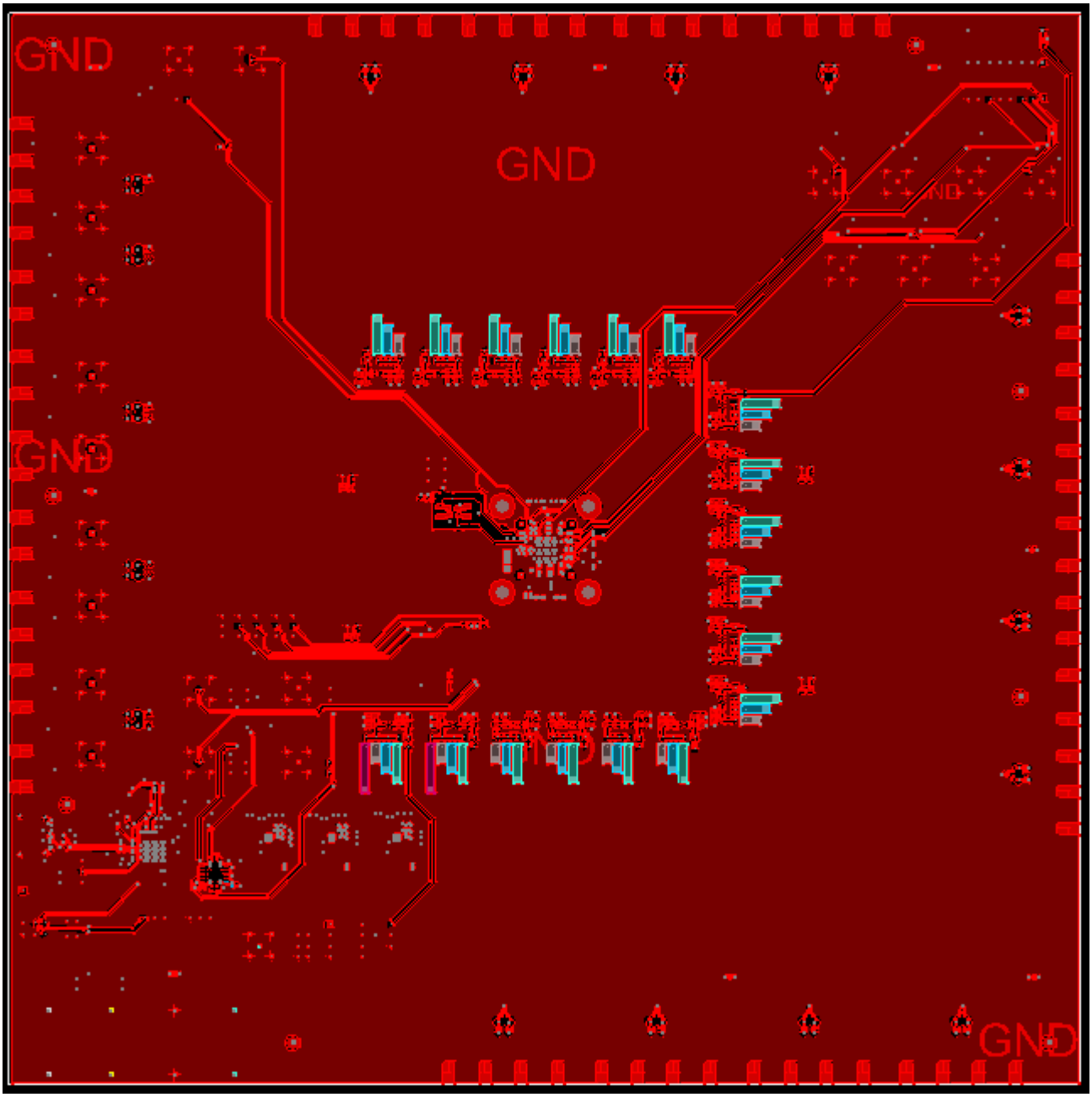


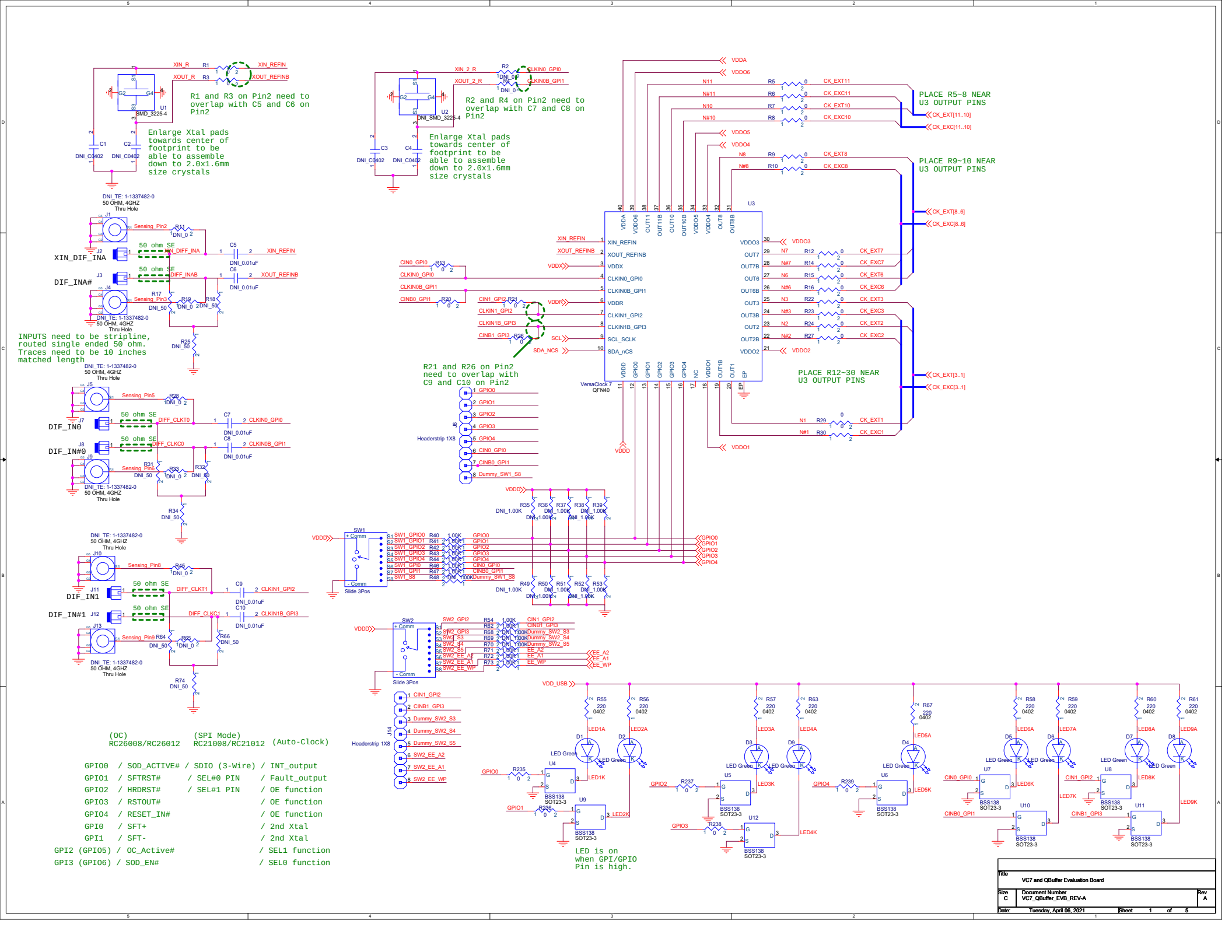
Figure 39. Layer 8–Bottom

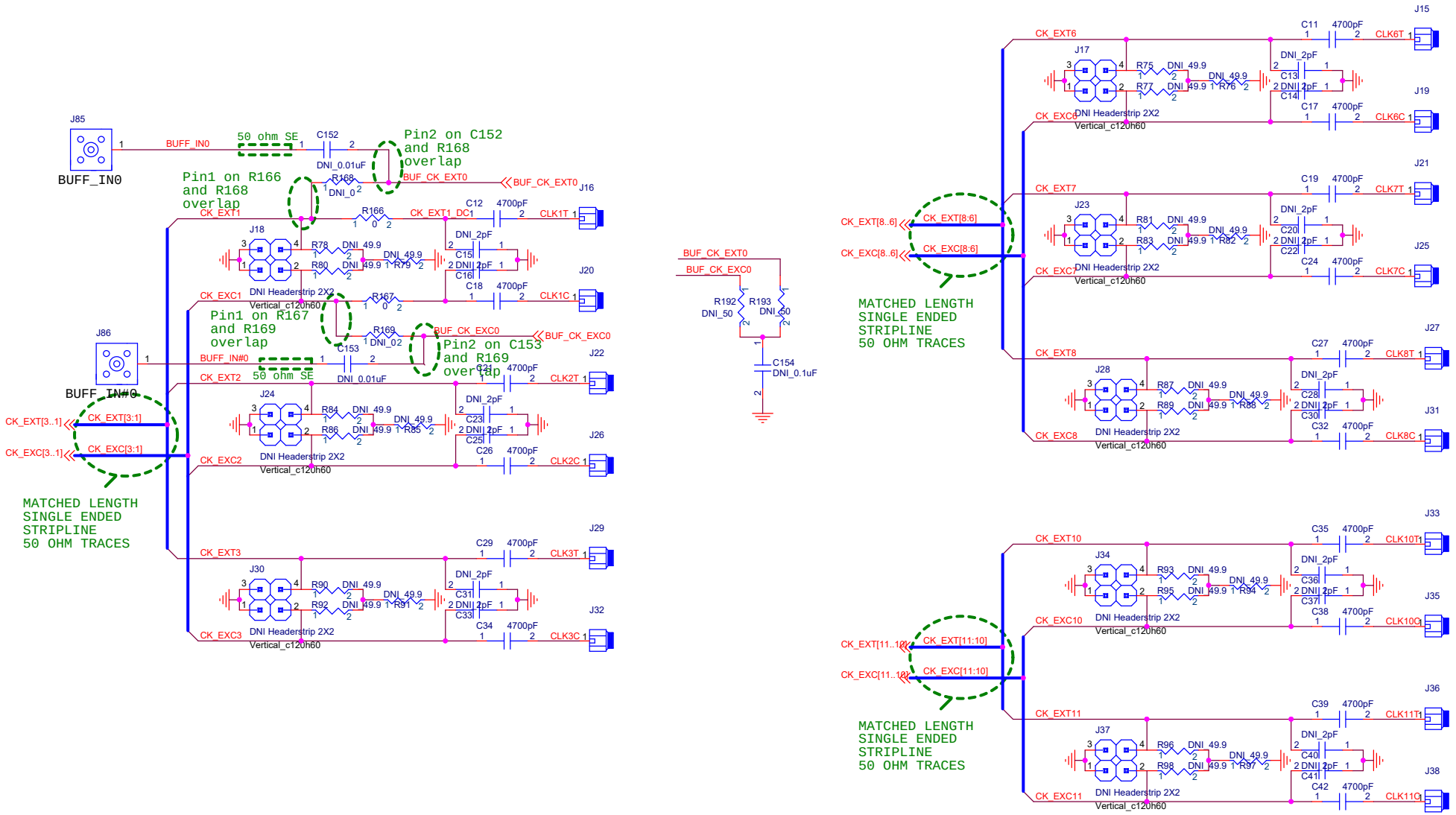
3. Ordering Information

Part Number	Description
RC21008-EVB	RC21008A Evaluation Board
RC31008-EVB	RC31008A Evaluation Board
RC21012-EVB	RC21012A Evaluation Board
RC31012-EVB	RC31012A Evaluation Board

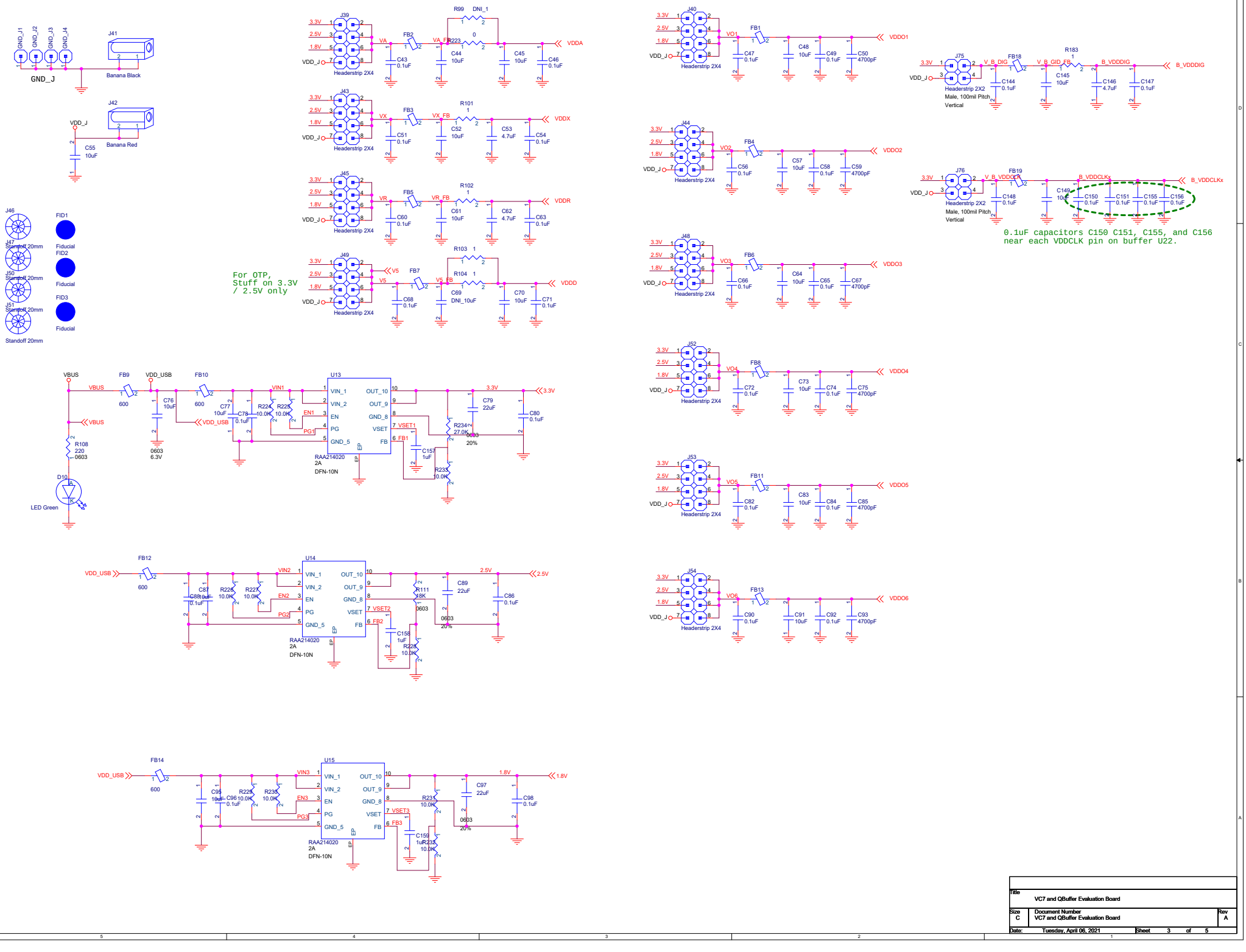
4. Revision History

Revision	Date	Description
1.00	Aug 25, 2022	Initial release.


R1 and R3 on Pin2 need to overlap with C5 and C6 on Pin2
Enlarge Xtal pads towards center of footprint to be able to assemble down to 2.0x1.6mm size crystals
R2 and R4 on Pin2 need to overlap with C7 and C8 on Pin2
Enlarge Xtal pads towards center of footprint to be able to assemble down to 2.0x1.6mm size crystals
PLACE R5~8 NEAR U3 OUTPUT PINS
PLACE R9~10 NEAR U3 OUTPUT PINS
PLACE R12~30 NEAR U3 OUTPUT PINS
INPUTS need to be stripline, routed single ended 50 ohm. Traces need to be 10 inches matched length
R21 and R26 on Pin2 need to overlap with C9 and C10 on Pin2
(OC) RC26008/RC26012
(SPI Mode) RC21008/RC21012
(Auto-Clock)
GPIO0 / SOD_ACTIVE# / SDIO (3-Wire) / INT_output
GPIO1 / SFTRST# / SEL#0 PIN / Fault_output
GPIO2 / HRDRST# / SEL#1 PIN / OE function
GPIO3 / RSTOUT# / OE function
GPIO4 / RESET_IN# / OE function
GPIO0 / SFT+ / 2nd Xtal
GPIO1 / SFT- / 2nd Xtal
GPI2 (GPIO5) / OC_Active# / SEL1 function
GPI3 (GPIO6) / SOD_EN# / SEL0 function
LED is on when GPI/GPIO Pin is high.
Title
VC7 and QBuffer Evaluation Board
Size C
Document Number VC7_QBuffer_EVB_REV-A
Rev A
Date: Tuesday, April 06, 2021
Sheet 1 of 5



Title	VC7 and QBuffer Evaluation Board	
Size B	Document Number VC7 and QBuffer Evaluation Board	Rev A
Date: Tuesday, April 06, 2021	Sheet 2 of 5	


GND_J
Banana Black
Banana Red
C55 10uF
Standoff 20mm
Fiducial
For OTP,
Stuff on 3.3V
/ 2.5V only
Headerstrip 2X4
Headerstrip 2X2
Male, 100mil Pitch
Vertical
0.1uF capacitors C150 C151, C155, and C156
near each VDDCLK pin on buffer U22.
LED Green
RAA214020
2A
DFN-10N
Title
VC7 and QBuffer Evaluation Board
Size
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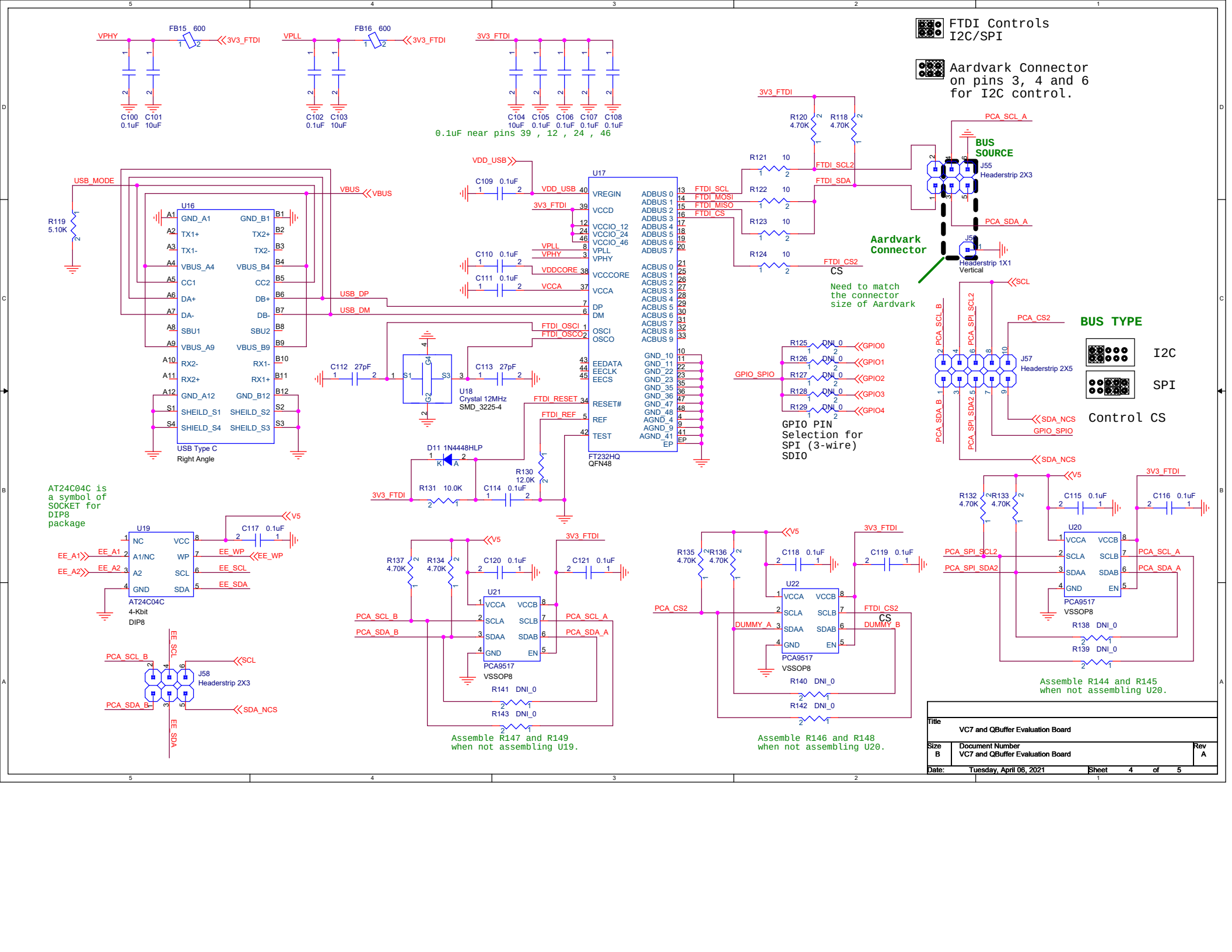
FTDI Controls I2C/SPI
Aardvark Connector on pins 3, 4 and 6 for I2C control.
0.1uF near pins 39 , 12 , 24 , 46
Aardvark Connector
Need to match the connector size of Aardvark
BUS SOURCE
BUS TYPE
I2C
SPI
Control CS
GPIO PIN Selection for SPI (3-wire) SDIO
AT24C04C is a symbol of SOCKET for DIP8 package
Assemble R147 and R149 when not assembling U19.
Assemble R146 and R148 when not assembling U20.
Assemble R144 and R145 when not assembling U20.
USB Type C Right Angle
Crystal 12MHz SMD_3225-4
FT232HQ QFN48
AT24C04C 4-Kbit DIP8
PCA9517 VSSOP8
Headerstrip 2X3
Headerstrip 1X1 Vertical
Headerstrip 2X5
Title
VC7 and QBuffer Evaluation Board
Size B
Document Number VC7 and QBuffer Evaluation Board
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Date: Tuesday, April 06, 2021
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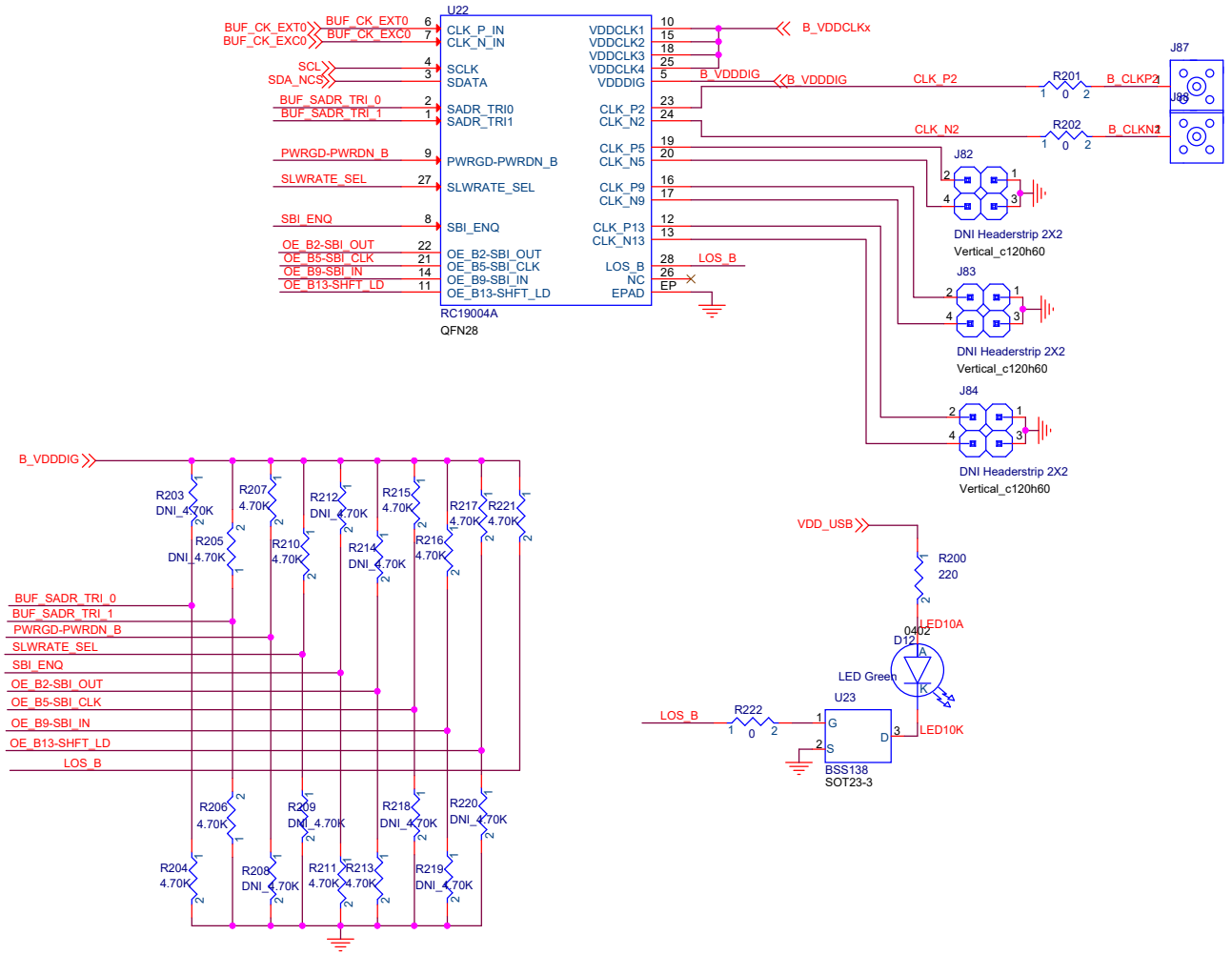

Title	VC7 and QBuffer Evaluation Board	
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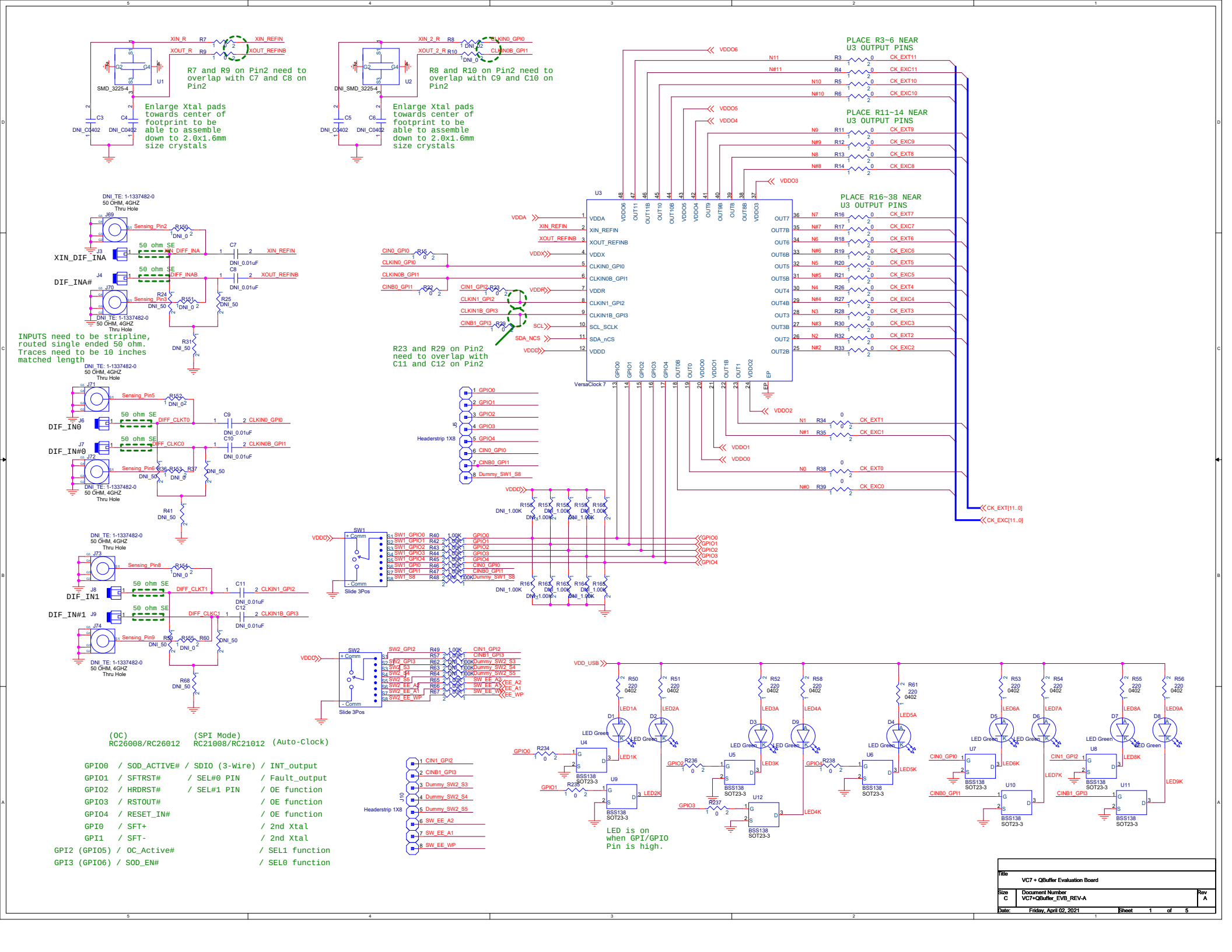
R7 and R9 on Pin2 need to overlap with C7 and C8 on Pin2
Enlarge Xtal pads towards center of footprint to be able to assemble down to 2.0x1.6mm size crystals
R8 and R10 on Pin2 need to overlap with C9 and C10 on Pin2
Enlarge Xtal pads towards center of footprint to be able to assemble down to 2.0x1.6mm size crystals
PLACE R3~6 NEAR U3 OUTPUT PINS
PLACE R11~14 NEAR U3 OUTPUT PINS
PLACE R16~38 NEAR U3 OUTPUT PINS
INPUTS need to be stripline, routed single ended 50 ohm. Traces need to be 10 inches matched length
R23 and R29 on Pin2 need to overlap with C11 and C12 on Pin2
LED is on when GPI/GPIO Pin is high.
(OC) RC26008/RC26012
(SPI Mode) RC21008/RC21012 (Auto-Clock)
GPIO0 / SOD_ACTIVE# / SDIO (3-Wire) / INT_output
GPIO1 / SFTRST# / SEL#0 PIN / Fault_output
GPIO2 / HRDRST# / SEL#1 PIN / OE function
GPIO3 / RSTOUT# / OE function
GPIO4 / RESET_IN# / OE function
GPIO0 / SFT+ / 2nd Xtal
GPI1 / SFT- / 2nd Xtal
GPI2 (GPIO5) / OC_Active# / SEL1 function
GPI3 (GPIO6) / SOD_EN# / SEL0 function
Title
VC7 + QBuffer Evaluation Board
Size C
Document Number VC7+QBufer_EVB_REV-A
Rev A
Date: Friday, April 02, 2021
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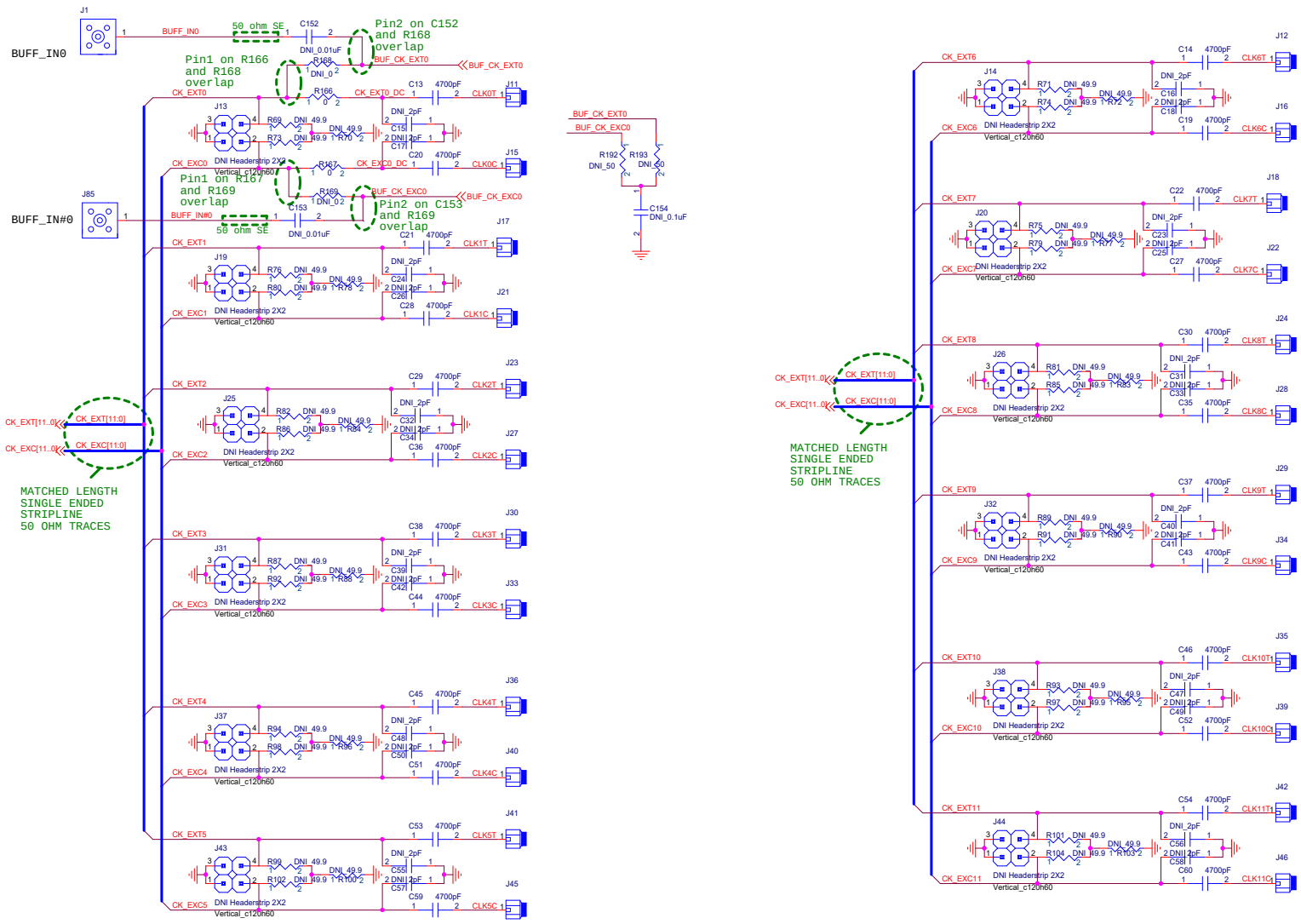

Title	VC7 + QBuffer Evaluation Board	
Size C	Document Number VC7+QBufer_EVB_REV-A	Rev A
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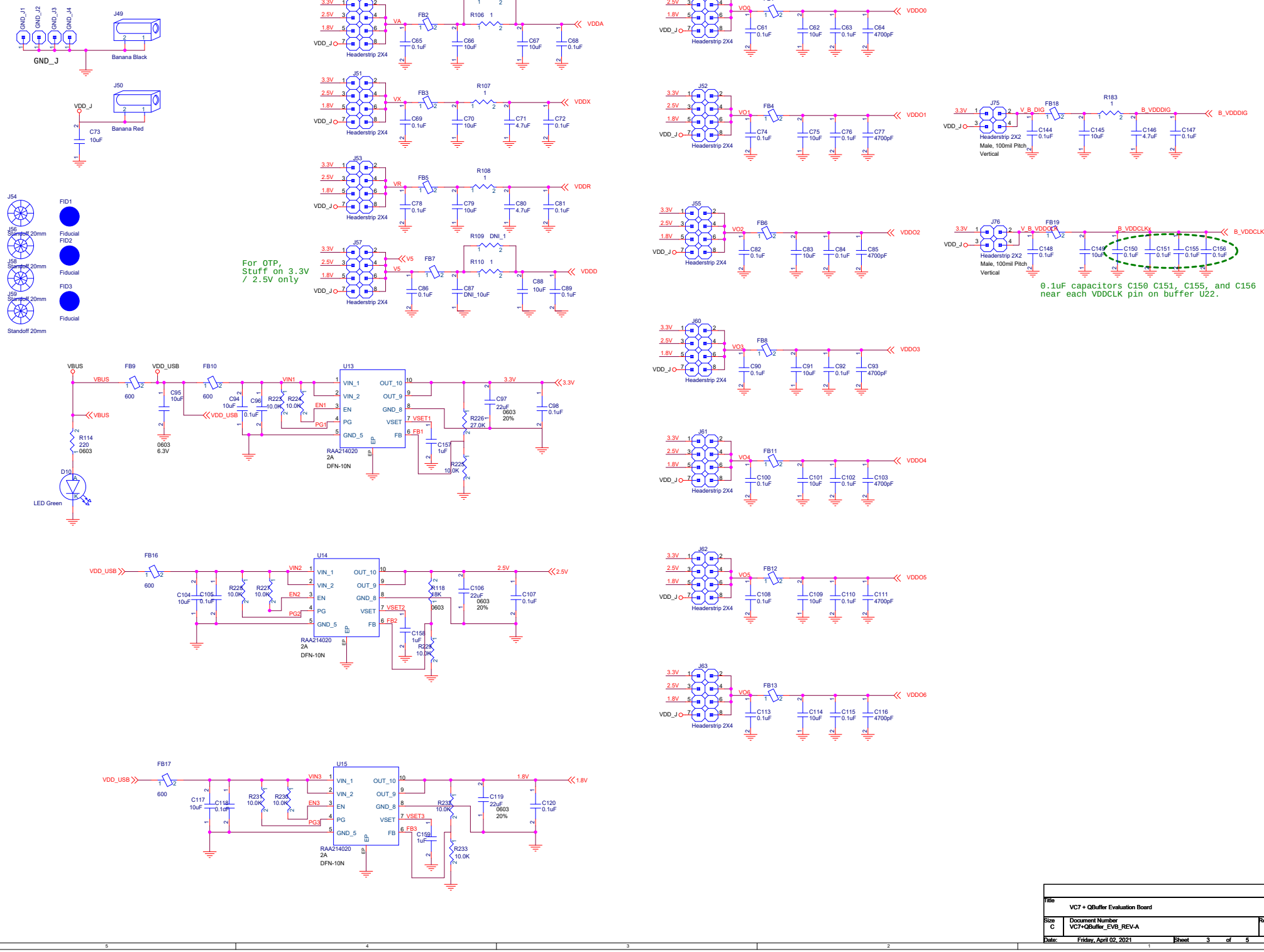

Title	VC7 + QBuffer Evaluation Board	
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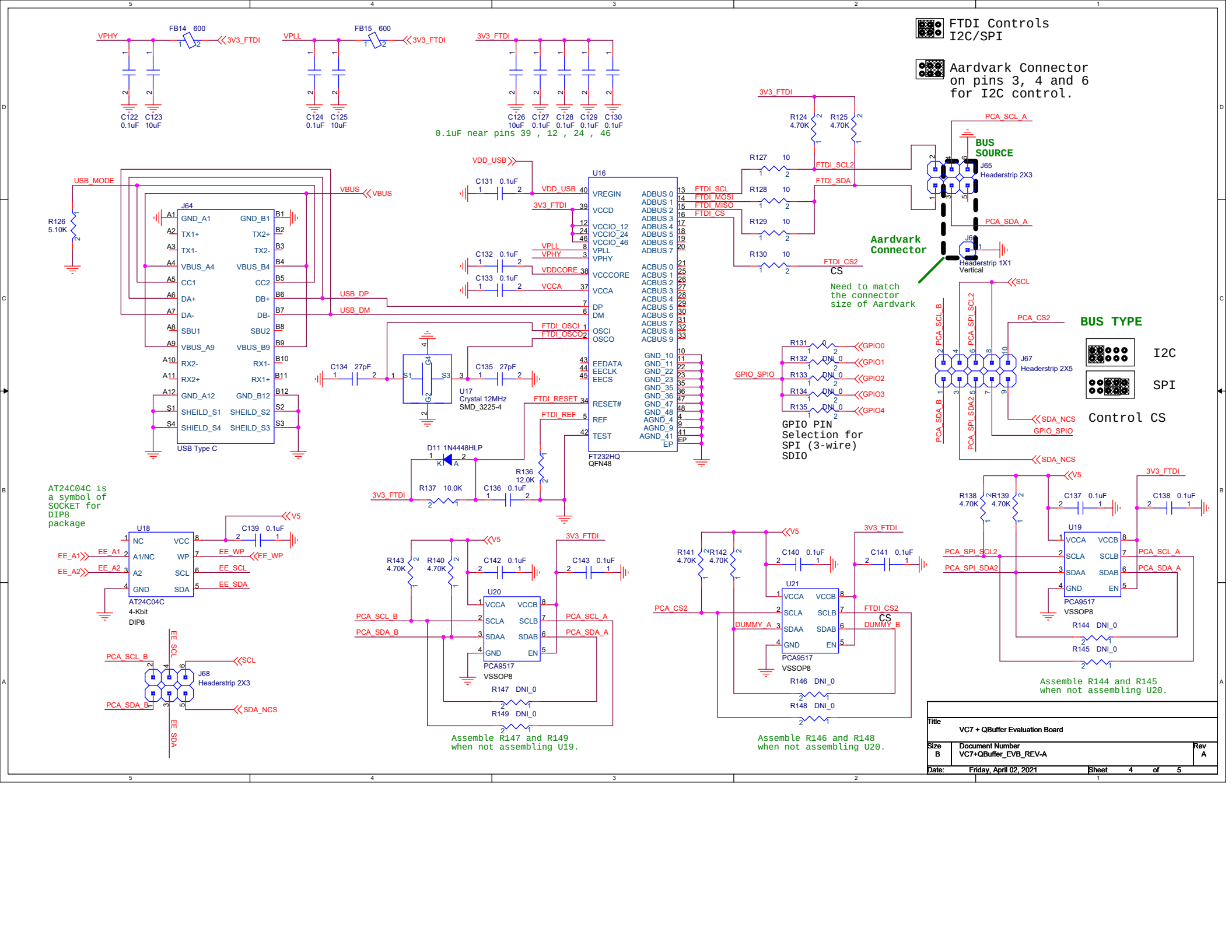
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VC7 + QBuffer Evaluation Board
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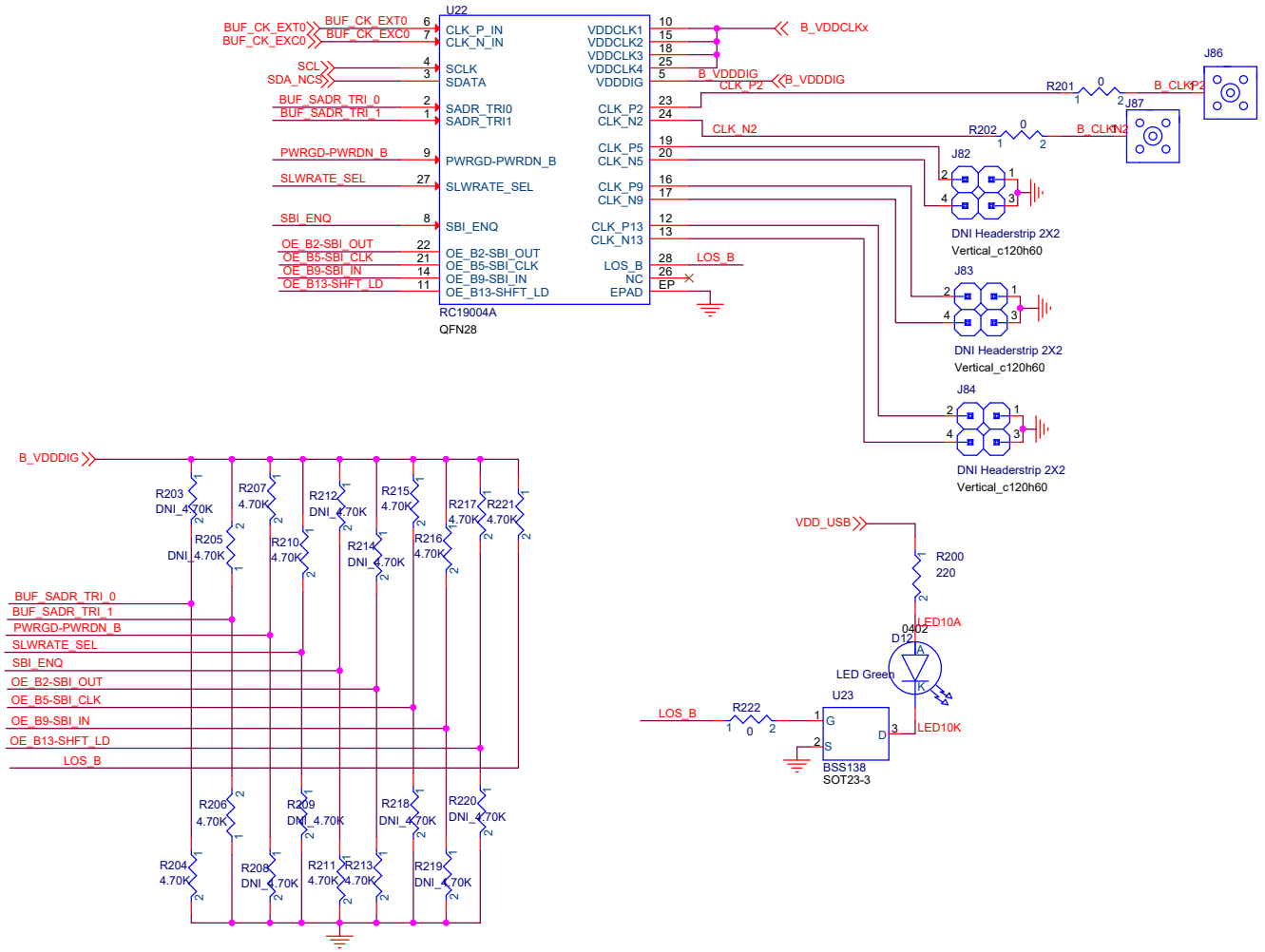

Title	VC7 + QBuffer Evaluation Board	
Size B	Document Number VC7+QBuffer_EVB_REV-A	Rev A
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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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