RC22312A/RC32312A

Evaluation Board

The RC22312A/RC32312A Evaluation Board (EVB) is designed to support users evaluating high performance synthesizer and jitter attenuator applications. This document describes the following:

- Basic hardware and GUI setup using Renesas IC Toolbox (RICBox™) software
- Board power-up instructions
- Instructions to get active output signals using a provided configuration file
- Hardware modifications required for different conditions

Board Contents

- RC22312A/RC32312A evaluation board
- EVB manual
- Configuration software (installable plugin for RICBox)
- Configuration example file for four built-in device settings
- Board schematic and BOM

Features

- Four differential clock inputs
- Twelve differential clock outputs
- On-board EEPROM stores startup-configuration data
- XIN terminal can use laboratory signal generator or OCXO/TCXO/XO components and board
- Laboratory power supply connectors
- USB-C power supply
- Serial port for configuration and register read out

Computer Requirements

- USB 2.0 or USB 3.0 interface
- Processor: minimum 1GHz
- Memory: minimum 512MB; recommended 1GB
- Available disk space: minimum 600MB (1.5GB 64-bit); recommended 1GB (2GB 64-bit)

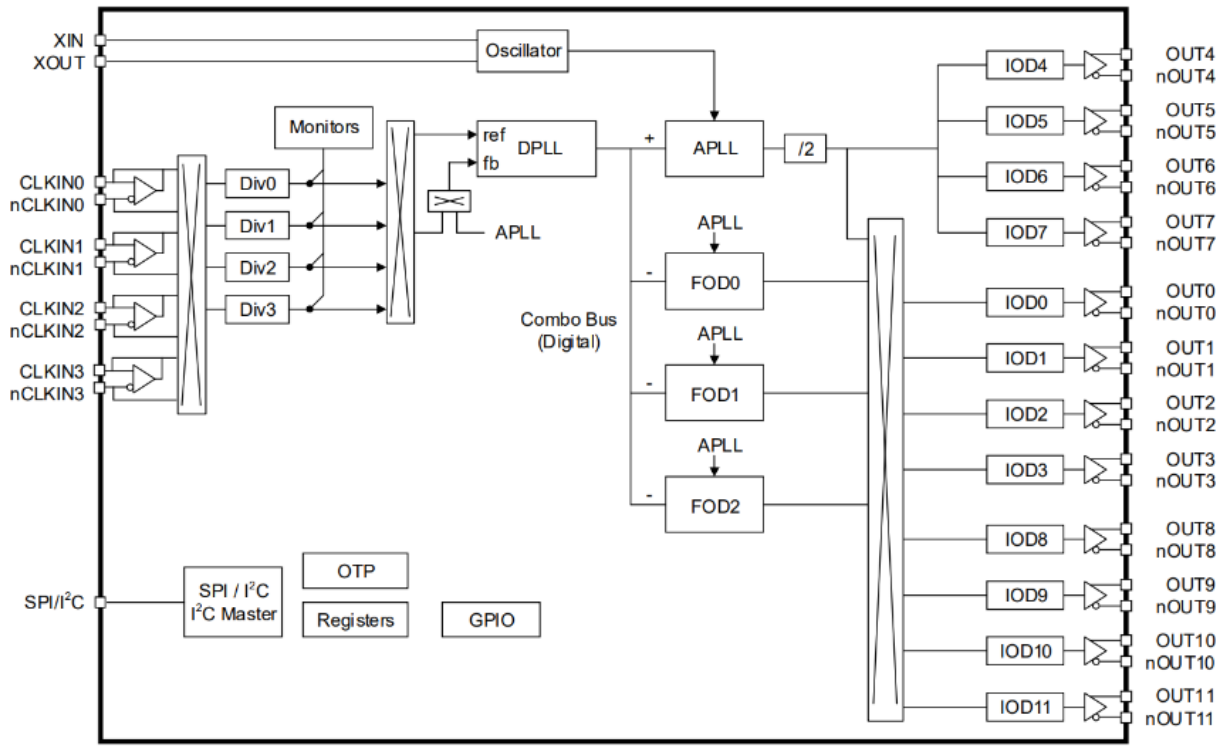

Figure 1. RC32312A Block Diagram

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1. Functional Description

The evaluation kit is used to demonstrate the RC22312A/RC32312A, a fully integrated clock synthesizer/generator and clock jitter attenuator. The kit can be used to evaluate major parameters including phase noise, spurious attenuation, clock frequency, output skew, phase alignment, device timing, and the signal waveform. The device on the board accepts any input frequency from 1kHz to 1GHz.

The RC22312A/RC32312A consists of a single APLL and DPLL design that allows for two separate frequency domains. The APLL can be used independently of the DPLL to generate synthesized clocks at the outputs that track the frequency of the input at the XIN pin. The DPLL can be used for jitter attenuation, clock filtering, and frequency translation while tracking clocks from the CLKIN pins. The DPLLs provide a programmable bandwidth and a DCO function for real-time frequency/phase adjustment.

1.1 Operational Characteristics

The board is equipped with on-board LDOs that require a 5V supply. If connecting to a high-speed USB interface, the evaluation board may be powered directly from the USB connection. The board is designed to operate over the industrial temperature range from -40°C to +85°C, ambient temperature.

It is recommended to use proper grounding during board operations to avoid ESD damage to the EVB.

1.2 Hardware Setup and Configuration

The following sections describe the crystal, input clock, serial, GPIO, and output and power functions used for setting up device testing.

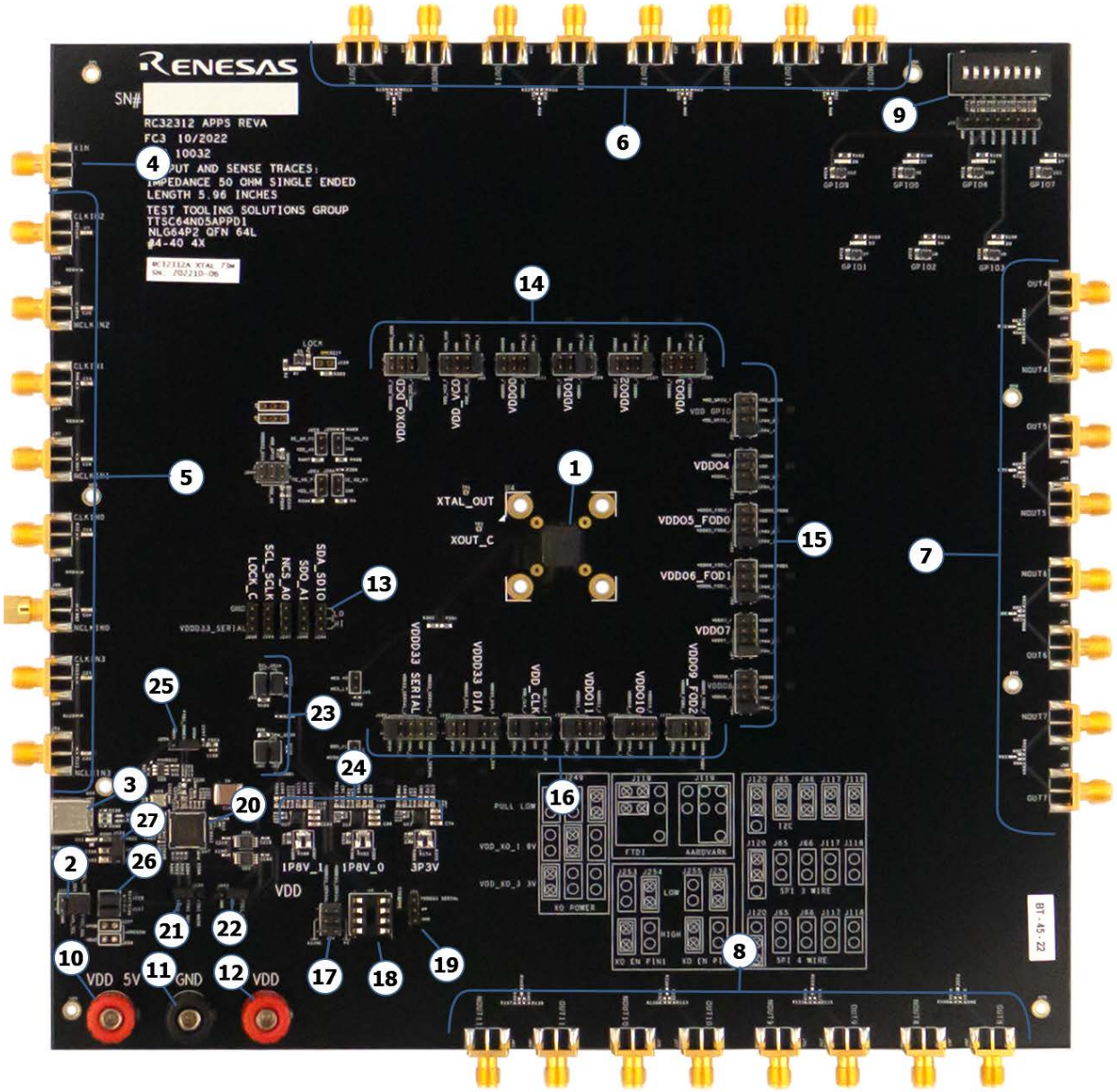

Figure 2. Evaluation Board

Refer to Table 1 and Figure 2 for the RC22312A/RC32312A evaluation board pin descriptions and functions.

Table 1. RC22312A/RC32312A Evaluation Board Pin Descriptions

Item No.	Name	On-Board Connector Label	Function
1	R22312A/RC32312A	U4	Evaluation device, 64-VFQFPN.
2	I^2C for FTDI or Aardvark Connector	J119	6-pin header of I^2C connector for SCL and SDA pins.
3	USB Interface	U16	USB type jack for connection with the computer and interaction with RICBox software.
4	XIN SMA Connector	J2	External clock input signal to XIN pin.

Item No.	Name	On-Board Connector Label	Function
5	CLKIN0/nCLKIN0 – CLKIN3/nCLKIN3	J15, J24, J27, J37, J39, J50, J59, J73	External clock input connectors for jitter attenuation functionality.
6	OUT[3:0]	J13, J16, J18, J22, J23, J27, J28, J33	SMA output test points.
7	OUT[7:4]	J35, J38, J40, J43, J47, J51, J54, J58	SMA output test points.
8	OUT[11:8]	J60, J67, J70, J75, J77, J79, J80, J83	SMA output test points.
9	DIP Switches	SW1	GPIO pull-up/down control.
10	VDD 5V Input Connector	J123	5V input supply to voltage regulators.
11	GND Connector	J125	Board ground for external supply.
12	Direct Supply Connector	J90	Voltage supply connector for direct pin supply.
13	I^2C/SPI Pin Control Pull-up/down Resistors	J244, J245, J246, J247, J248	SDA_SDIO, SCL_SCLK, SDO_A1, NCS_A0, LOCK pin 10kΩ to GND or VDDD33_SERIAL.
14	VDDXO_DCD, VDD_VCO, VDDO0, VDDO1_FOD0, VDDO2, VDDO3 Voltage Selection	J98, J100, J111, J109, J107, J105	1.8V regulator jumper selection.
15	VDD_GPIO, VDDO4, VDDO5, VDDO6, VDDO7, VDDO8_FOD1 Voltage Selection	J92, J103, J101, J99, J97, J94	1.8V regulator jumper selection.
16	VDDO9, VDDO10_FOD2, VDDO11, VDD_CLK, VDDD33_DIA, VDDD33_SERIAL Voltage Selection	J110, J108, J106, J104, J102, J100	1.8/3.3V regulator jumper selection.
17	EEPROM Address Selection	J74	EEPROM pins A1 and A2 pull-up/down to GND or VDDD33_SERIAL.
18	EEPROM Socket	U5	8-pin dip EEPROM socket.
19	EEPROM WP	J71	Pull-up/down EEPROM write-protect pin.
20	FTDI I^2C/SPI Controller	U17	I^2C/SPI control interface between PC and RC22312A/RC32312A.
21	I^2C/SPI Path Connection	J120	Combine or fanout SDI/SDO lines from the FTDI chip.
22	Level Translator Enable	J243	Enable/Disable I^2C level translators.
23	I^2C Pull-ups and Path Connectors	J61, J62, J65, J66	Connect level translators SDA/SCLK to RC22312A/RC32312A pins and pull-up to VDDD33_SERIAL.
24	Voltage Regulators	U13, U14, U15	Receive 5V input and supply 1.8/3.3V to EVB power domains.
25	FTDI Voltage Selection	J259	Control FTDI voltage source between USB input and 5V board supply.
26	I^2C Pull-up Resistors	J117, J118	Pull-up to FTDI 3.3V
27	LDO Voltage Input Selection	J124	Select EVB LDO input voltage source between bench or USB supply.

For proper functionality out of the box, the jumpers on board should be placed to allow the correct voltages at each LDO and domain. The jumpers should be arranged as described in Table 2.

Table 2. Default Jumper Configurations

Label/Function	Jumper	Default Orientation
Connect nCS_LS to IC from FTDI	J45	OFF
Connect MISO_LS to IC from FTDI	J46	OFF
Connect SCL_SCLK_LS to IC from FTDI	J61	ON
Connect SDA_SDIO_LS to IC from FTDI	J62	ON
I^2C Pull-up to VDDD33_SERIAL	J65	ON
I^2C Pull-up to VDDD33_SERIAL	J66	ON
EEPROM Write Protect	J71	OFF
EEPROM Address Select	J74	OFF
VDD_GPIO	J92	Either 1P8V_0 or 1P8V_1
VDDO8_FOD1	J94	Either 1P8V_0 or 1P8V_1
VDD_VCO	J96	Either 1P8V_0 or 1P8V_1
VDDO7	J97	Either 1P8V_0 or 1P8V_1
VDD_XO_DCD	J98	Either 1P8V_0 or 1P8V_1
VDDO6	J99	Either 1P8V_0 or 1P8V_1
VDDD33_SERIAL	J100	3P3V
VDDO5	J101	Either 1P8V_0 or 1P8V_1
VDDD33_DIA	J102	Either 1P8V_0 or 1P8V_1
VDDO4	J103	Either 1P8V_0 or 1P8V_1
VDD_CLK	J104	Either 1P8V_0 or 1P8V_1
VDDO3	J105	Either 1P8V_0 or 1P8V_1
VDDO11	J106	Either 1P8V_0 or 1P8V_1
VDDO2	J107	Either 1P8V_0 or 1P8V_1
VDDO10_FOD2	J108	Either 1P8V_0 or 1P8V_1
VDDO1_FOD0	J109	Either 1P8V_0 or 1P8V_1
VDDO9	J110	Either 1P8V_0 or 1P8V_1
VDDO0	J111	Either 1P8V_0 or 1P8V_1
I^2C Pull-up	J117	ON
I^2C Pull-up	J118	ON
Bus Communication Selection	J119	Between FTDI_SDO and AVK_SDA and between FTDI_SCL and AVK_SCL
SDO and SDI Connection for I^2C	J120	Between FTDI_SDO_J and FTDI_SDI_J

Label/Function	Jumper	Default Orientation
GND	J121	OFF
Enable I²C Pull-ups	J243	Between FTDI_3P3V and Center
SDA_SDIO	J244	OFF
SCL_SCLK	J245	OFF
SDO_A1	J246	OFF
NCS_A0	J247	Between center and HI
LOCK_C	J248	OFF

Note: 1P8V_0 and 1P8V_1 refer to separate LDO supply on the board. They can be used to isolate pin supplies from each other for performance optimization.

1.2.1. Power and USB-C Connections to Computer Host

The EVB is connected to a computer host via the USB3.0 to USB-C cable. It is recommended that the cable is connected to a USB3.0 port. However, a USB2.0 port acceptable due to the RC22312A/RC32312A for I²C/SPI communications only. The USB-C provides +5V as power source to the on-board regulators. The on-board regulators support 3.3V and 1.8V voltages to the entire EVB. These voltages can be set by various jumpers found around the RC22312A/RC32312A.

The RC22312A/RC32312A voltage source can be derived from the on-board voltage regulators for 3.3V, 1.8V, or directly from the J90 banana connector with an external supply. The J90 connection can be used to measure total supply current into pins as reference. When jumpers are used to select power from J90 connector, the USB connection will still be required to connect RICBox.

- Power connection
  - Set the power supply voltage to 5V and the current limit to 2A
  - +5V (J123) = +5V
  - GND (J125) = GND
- Expected current draw: ~ 0.7A
  - After programming the device ~0.6A to 1A during normal operation depending on the device configuration

1.2.1.1. Power the Device with USB Connection

- Set jumper on J124 between pins 1 and 2
- Set jumper on J259 between pins 1 and 2
- Ensure that the EVB connects to a USB 3.0 port or newer

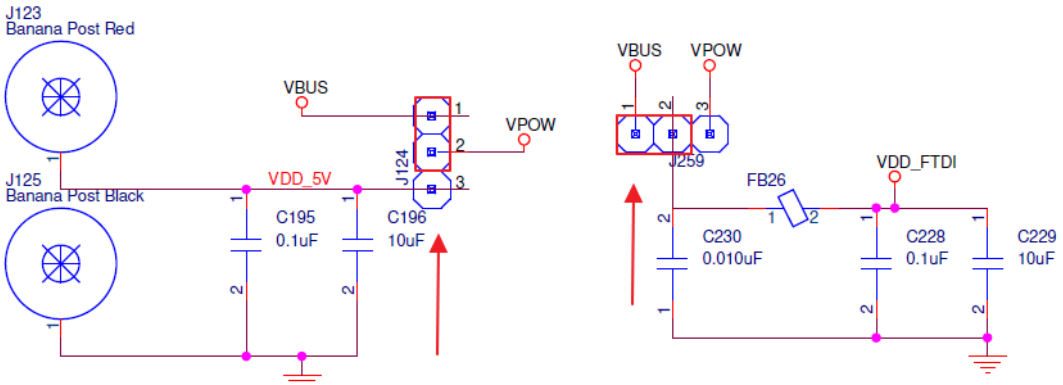

Figure 3. USB Power Jumpers

1.2.1.2. Power the Device with External Power Supply Connection and On-board Voltage Regulators

- Set jumper on J124 between pins 2 and 3
- Set jumper on J259 between pins 2 and 3
- Ensure 5V at banana jack J123 and GND connection

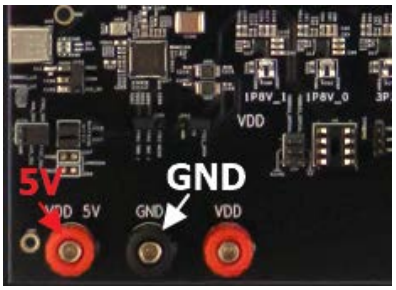

Figure 4. External 5V Board Input

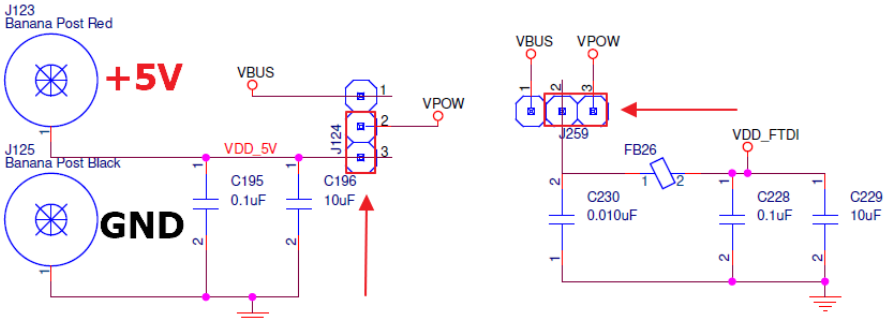

Figure 5. External 5V Schematic

Note: Allow for up to 2A of current with direct power supply. The device current will be increased during register write and calibration.

1.2.1.3. Power the Device Pins with External Power Supply Connection J90

- Ensure 1.8V or 3.3V at banana jack J90 and GND connection depending on the power pin
- Change the corresponding domain jumper selection to V_{DD}

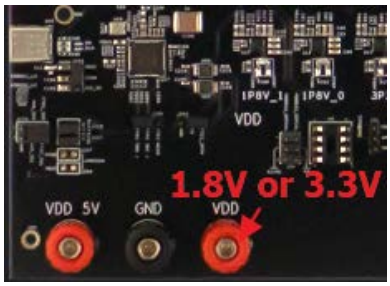

Figure 6. J90 Board Input

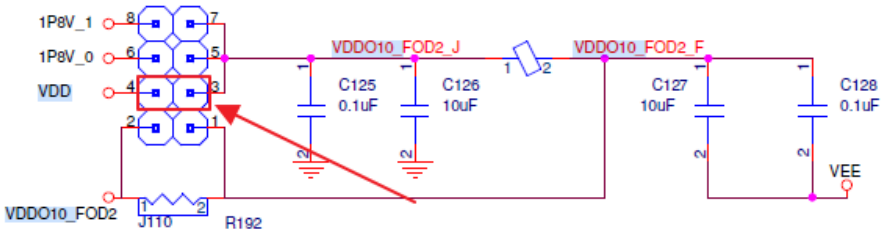

Figure 7. VDD Jumper Bypass Schematic

Note: J90 can supply voltage for the entire device. If all voltage pin jumper settings are configured for VDD and the input voltage is 1.8V.

Note: All individual voltage domains run at 1.8V. Only VDDD33_SERIAL and VDDD33_DIA are compatible with 3.3V. Supplying 3.3V to any other domain may cause damage to the RC22312A/RC32312A device.

1.2.2. Overdrive the XIN with an External Signal

The RC22312A/RC32312A device can support between 25MHz–80MHz on the XIN (crystal oscillator input) pin. There are four options for providing an input signal to the device XIN pin:

- An external signal (J2 SMA connector) typically from a signal generator; see section 1.2.1). This option is configured by default.
- An on-board crystal mount (U3); see section 1.2.2
- Two on-board XO mounts (U27, U29); see section 1.2.3

To overdrive XIN with an external signal (see Figure 8):

1. Populate C1 with 0.1µF capacitor to ensure that J2 has a connected path to the RC32312A device.

2. Depopulate C2, C3, R398, and R424 to ensure that excess trace is not used.
3. Populate R4 with 50Ω for input termination (ensure signal is >~1.3V amplitude).
4. Place input clock signal at J2 and ensure that the signal is within specification for the XIN pin.

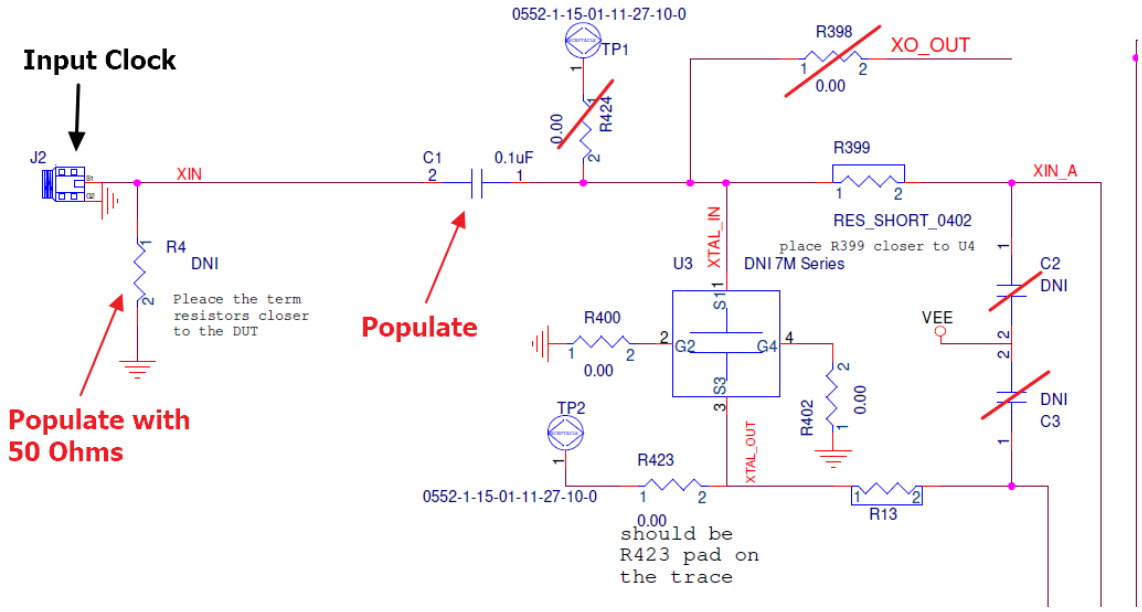

Figure 8. XIN Pin Overdrive Schematic

1.2.3. On-board Crystal Mount

The crystal mounting position can only be used if there is no other signal present on the XIN path (see Figure 9). In order to setup the evaluation board for crystal input:

1. Depopulate C1, R398, R423, and R424 to ensure there is no excess trace in the XIN pin.
2. Populate C2 and C3 to externally tune the input crystal frequency.

Note: The EVB stray capacitance has been measured to be ~8.24pF.

3. Mount crystal to U3. Remove R400 or R402 if the crystal only has 3 pads.

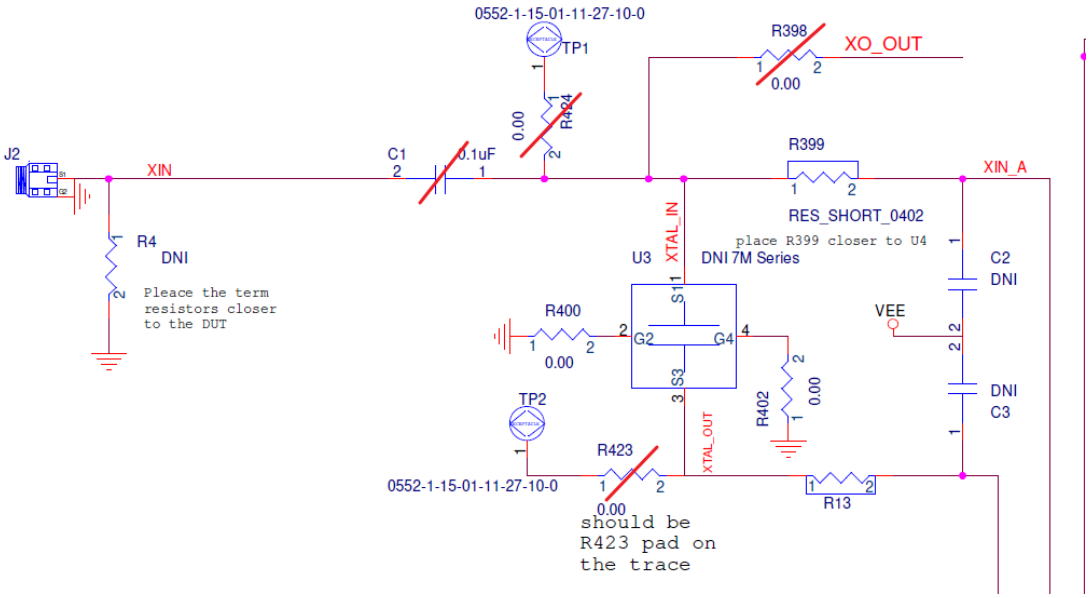

Figure 9. Crystal Mount Schematic

1.2.4. On-board XO Mount

There are two options on the evaluation board to allow for an XO to be mounted. Positions U27 and U29 are connected in parallel and should only be used one at a time. For an XO to work properly at U27 and U29, the following must be setup (see Figure 10, Figure 11, Figure 12 and Figure 13):

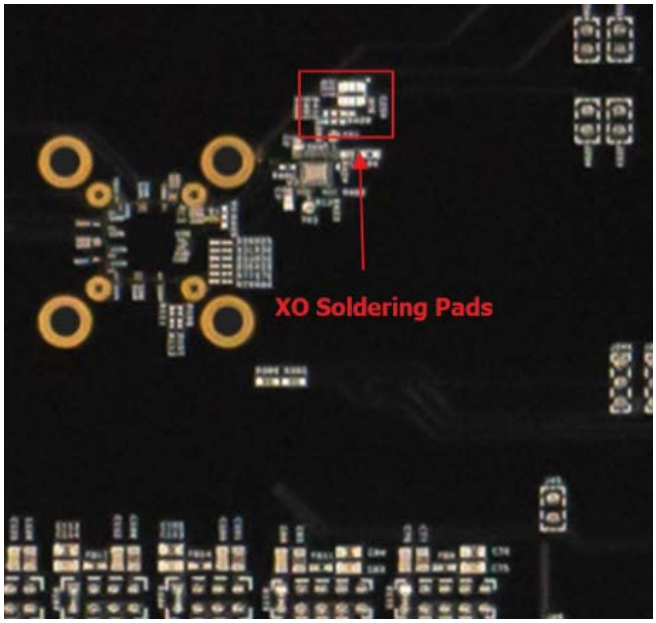

Figure 10. EVB XO Pads

1. Populate R398 with 0 Ohms.
2. Depopulate C1, U3, R423, R424, C1, and C2.

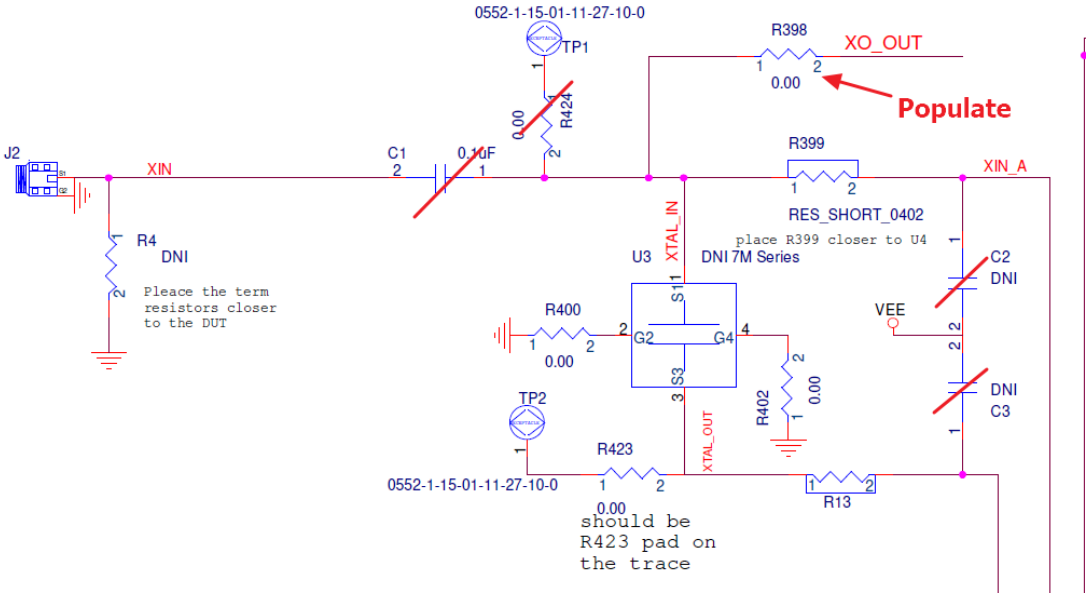

Figure 11. XO Path Connection Schematic

3. Populate R428 if pin 5 of the XO is being used as output.
4. Ensure that the XO output is below ~1.3V amplitude signal in order to support proper XIN pin characteristics.
   a. R416 can be populated with a low value resistor (33Ω) to reduce the XO output amplitude. Otherwise, R416 can be populated with 0 Ohms.

5. R405 and R406 can be populated to adjust the common mode voltage of the XO output.

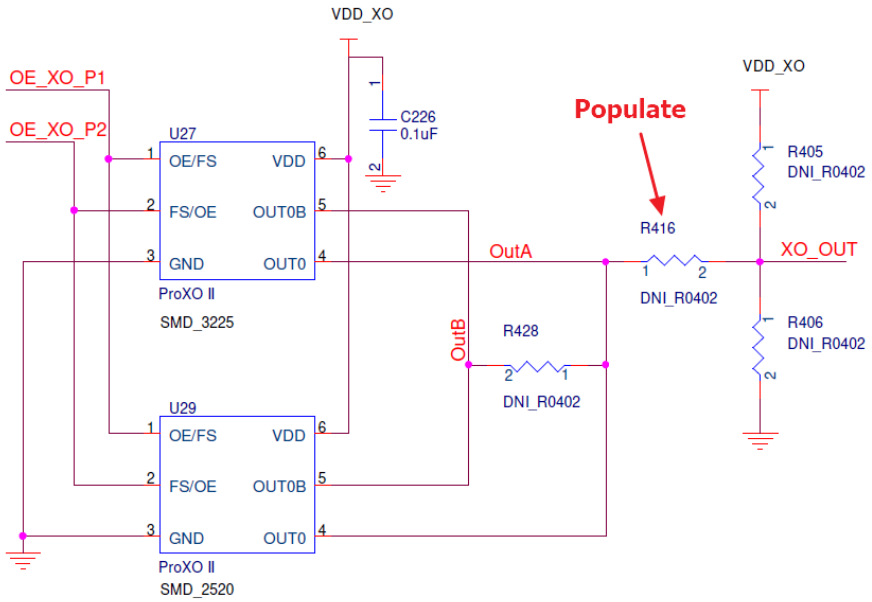

Figure 12. XO Schematic

6. Use jumper on J253 – J256 to pull the XO output enable pin high or low depending on the XO datasheet.

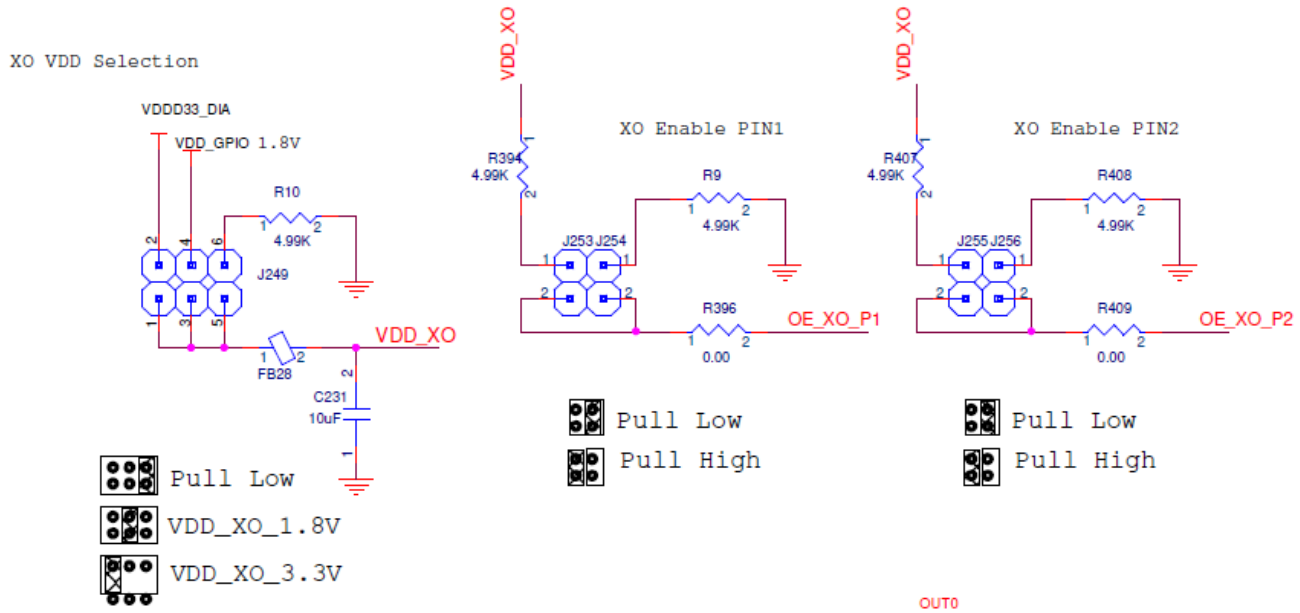

Figure 13. XO OE Pin Header Schematic

1.2.5. Clock Inputs

The RC32312A can accept four differential clock inputs to be used as a jitter attenuator source. To enable proper connection, make sure the input termination resistor setup corresponds to the input signal that is connected. The evaluation board default termination setup has 50Ω to GND at each leg.

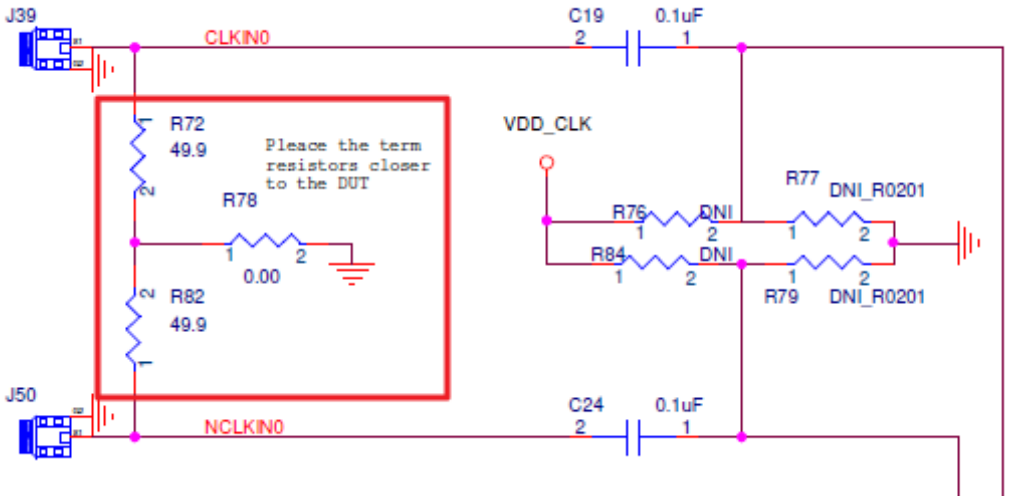

Figure 14. Input Clock Termination Schematic

The RC32312A contains internal AC-coupling for LVDS, HCSL, LVCMOS signals. Supported frequency ranges of the clock inputs are 1kHz to 1GHz in differential mode, and 1kHz to 250MHz in single-ended mode.

Pull-up and pull-down resistors apart of the CLKIN path can be used for common mode voltage adjustments.

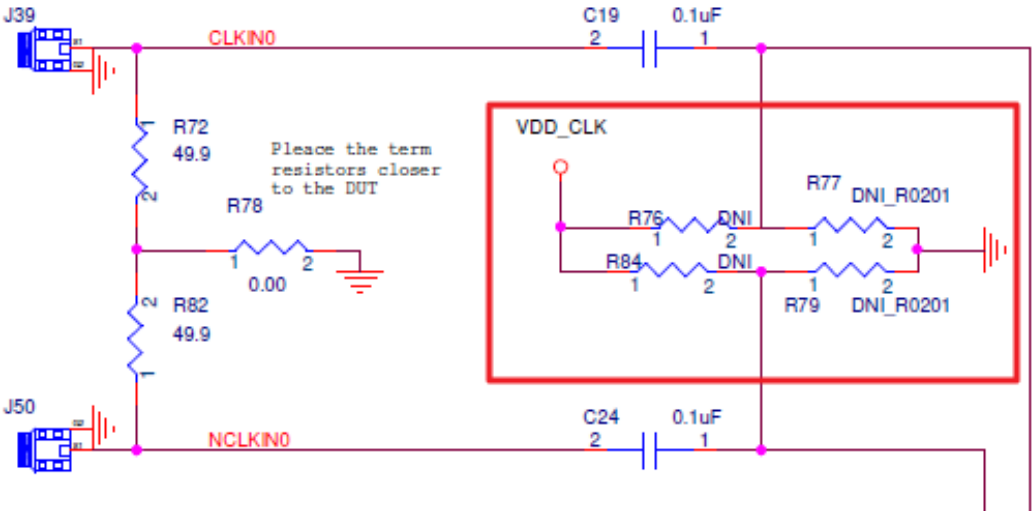

Figure 15. Input Clock Pull-up/down Schematic

Note: Clock inputs are only used with **RC32312A** devices.

1.2.6. Clock Outputs

Each of the 12 differential output pairs can be programmed to LVDS, HCSL or CMOS logic type.

- The HCSL mode supports HCSL by default and can be modified to support other modes by changing the amplitude and enabling/disabling the internal termination.
- For CMOS output type, output phase of each pin can be programmed to be 180 degrees out-of-phase, in-phase, or single pin output.
- LVDS outputs can be configured to 350mV or 400mV swing up to 1V common mode voltage.
- Each output can also be tri-stated when not being used.

Output terminations on the evaluation board can be populated to support the different output types.

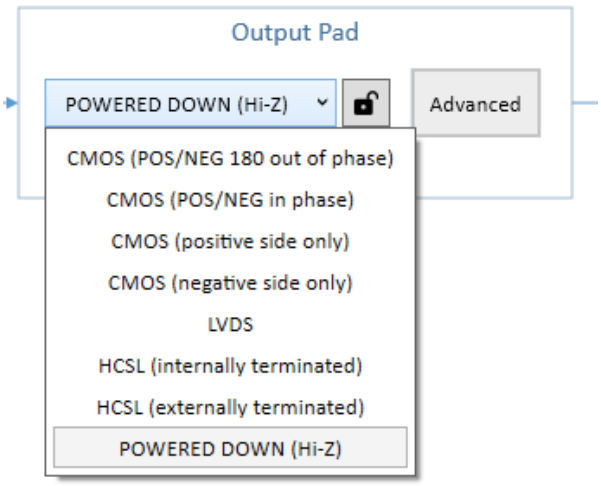

Figure 16. Output Type Options

Place 50Ω across each leg, for a total 100Ω across, to terminate for LVDS.

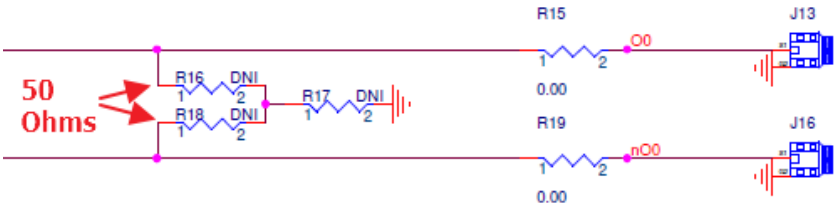

Figure 17. LVDS Input Clock Termination

Place 50Ω to GND at each leg for HCSL terminations.

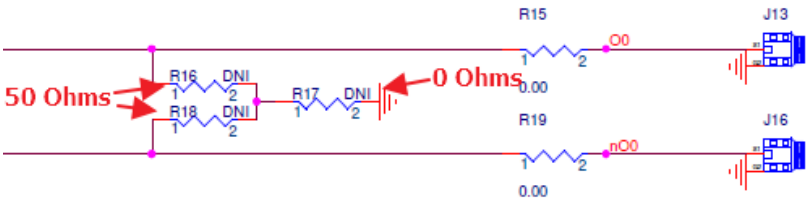

Figure 18. HCSL Input Clock Termination

1.2.7. Serial Connection

The EVB can be connected to a computer via a USB3.0 to USB-C connector. The on-board USB-to-MPSSE Bridge (FTDI FT232HQ) can handle the data communication. The +5V from the USB-C powers the on-board regulators (see section 1.2.1.1).

The Bus Source connector J119 is used to select the source of the communication bus. The bus will be I²C for most communication but can also be SPI for specific tests. Pins 1 and 2 in J119 are SDA and SCL from the FTDI chip. Pins 3 and 4 pass the SDA and SCL to the I²C level shifter. To use the on-board FTDI chip, install jumpers on pins 1–3 and 2–4. The board will be shipped with these jumpers installed. Theoretically, any I²C adapter can be connected to pins 3 and 4 for SDA and SCL. Pin 6 can be used as the ground connection for the I²C connection. Pins 3, 4, 5 and 6 are arranged such that a Total Phase I²C Host Adapter (part number: TP240141) can be plugged onto pins 3, 4, 5 and 6 only (see Figure 19).

For default I²C operation, jumpers are installed on pins 1–3 and 2–4 (see jumper J119 in Table 2).

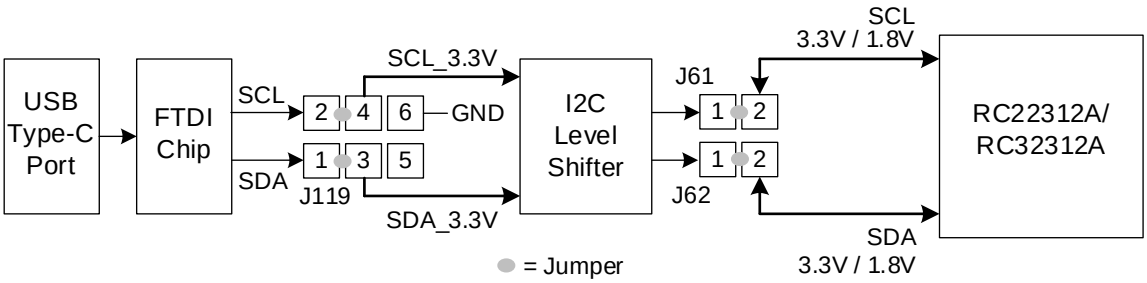

Figure 19. Communication Setup for I²C Mode

Note: For SPI operation instructions, contact Renesas support.

1.2.8. On-board EEPROM

The EVB also supports an external EEPROM IC for loading of an RC22312A/RC32312A configuration programmed into the EEPROM as an option. To load the configurations from EEPROM, the EEPROM load enable bit must be set in device OTP. If the enable bit is not set, the EEPROM load will be skipped.

The EVB provides a socket of 8-lead DIP8 SOIC-8 socket (Figure 20) so other EEPROM devices of different memory size can be tested.

Figure 20. EEPROM in Socket

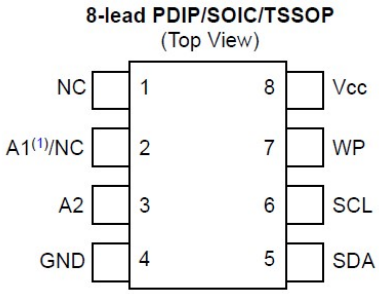

Figure 21. EEPROM Pin Description

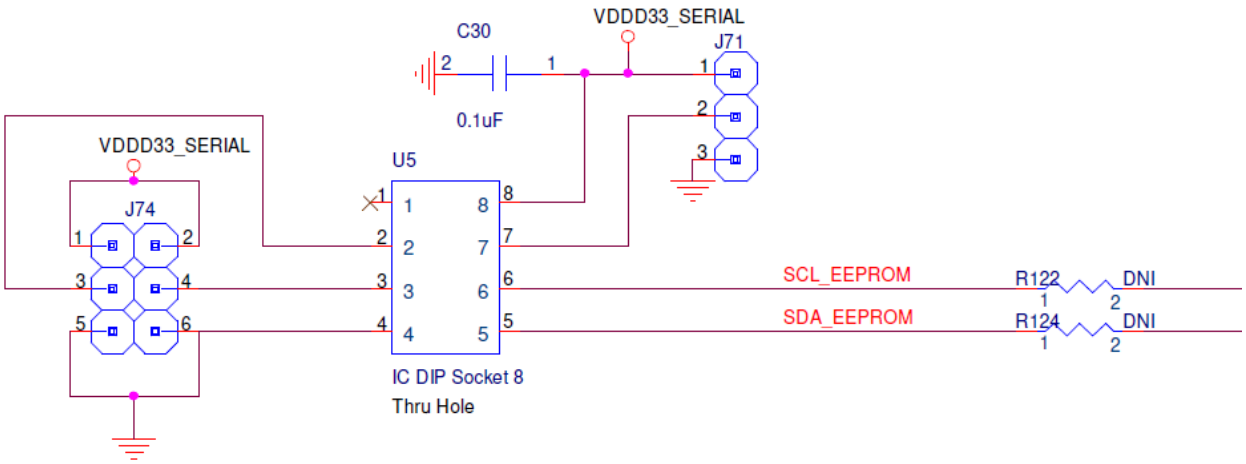

Figure 22. EEPROM Schematic

The A1 and A2 pins are the EEPROM address inputs that can be pull either high or low using jumpers at J74 to define the device address. By default, jumpers can be removed so that A1 and A2 are left floating as they are internally pulled down to GND in most EEPROM devices.

The WP pin is the write-protect input. When the WP pin is pulled down to GND (Low), the EEPROM can have normal write operations. When it is pulled up directly to V_{CC} (High), all write operations are inhibited. The WP pin can be controlled with a jumper at J71.

To establish a connection to the EEPROM, the SDA and SCL traces must be connected to the FTDI communication path. Populate R122 and R124 with 0 Ohms to make the connection. This will allow software features like RICBox to communicate with the EEPROM device.

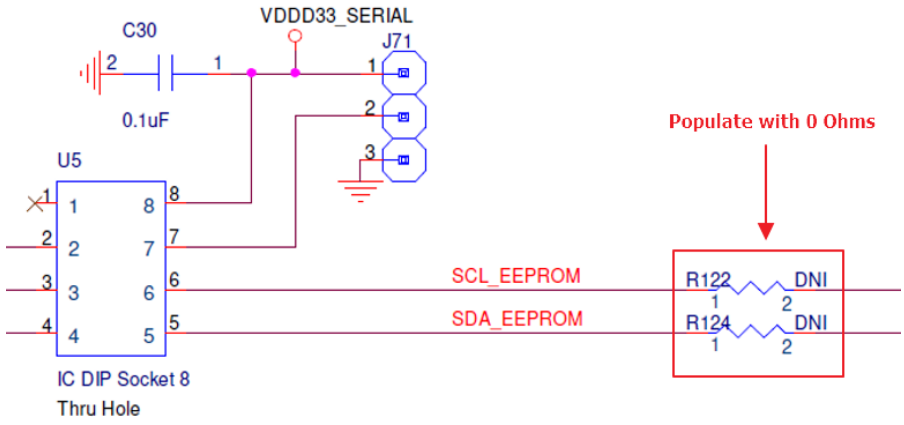

Figure 23. EEPROM Connection Resistors

When the device attempts to load an EEPROM configuration during start-up, the FTDI I²C controller can cause interference. The FTDI device can be removed from the I²C trace path by removing jumpers J61 and J62. This will also disconnect RICBox from communicating with the RC22312A/RC32312A device.

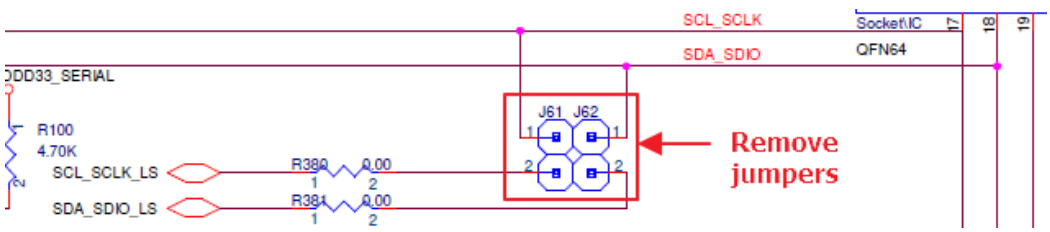

Figure 24. FTDI to I²C Communication Jumpers

1.2.9. GPIO DIP Switch Selectors

The EVB has one DIP switch set (SW1) to support GPIO pins on RC22312A/RC32312A device. GPIOs 0–6 can support a two-level input (low/high). The middle position of the DIP switches leaves the pin open so GPIOs can be controlled with internal pull-up and pull-down resistors. Move to the '+' side to pull the pin high and move to the '-' side to pull the pin low. LEDs correspond to each GPIO to show the pin state.

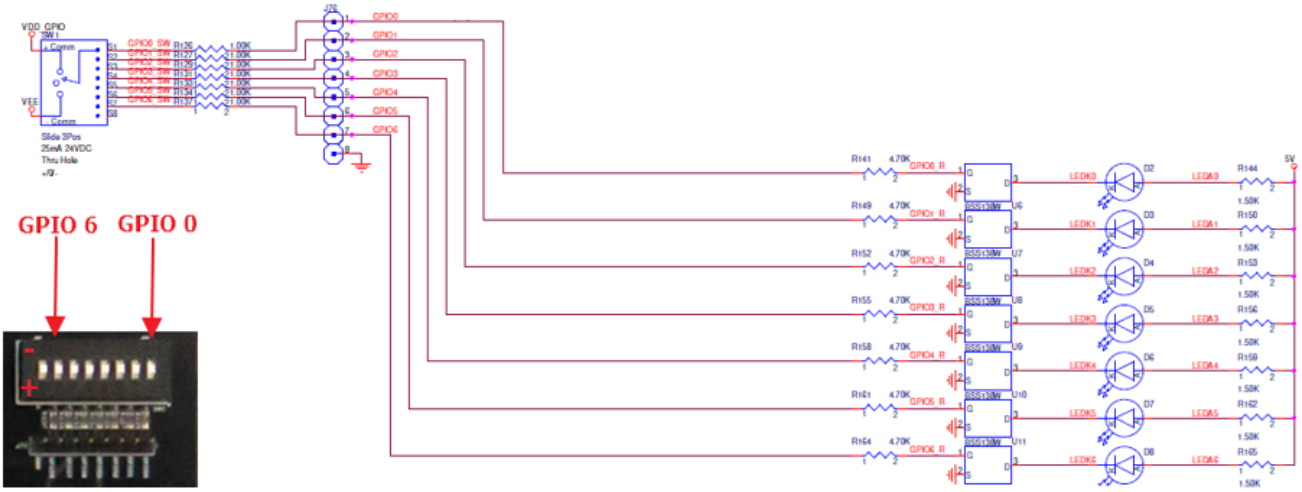

Figure 25. GPIO Schematic and EVB DIP Switches

1.3 Software Setup and Configuration

1.3.1. Prepare the Software

For software installation instructions, see the Renesas IC Toolbox Software Manual, sections 1 and 11.

1.3.2. Launch the GUI

After successfully installing the Renesas IC Toolbox software, launch the software from the Windows <start> menu at the bottom-left corner of the screen.

1. Click Start > RICBox to open the initial RICBox window.
2. Click *Create new project*.

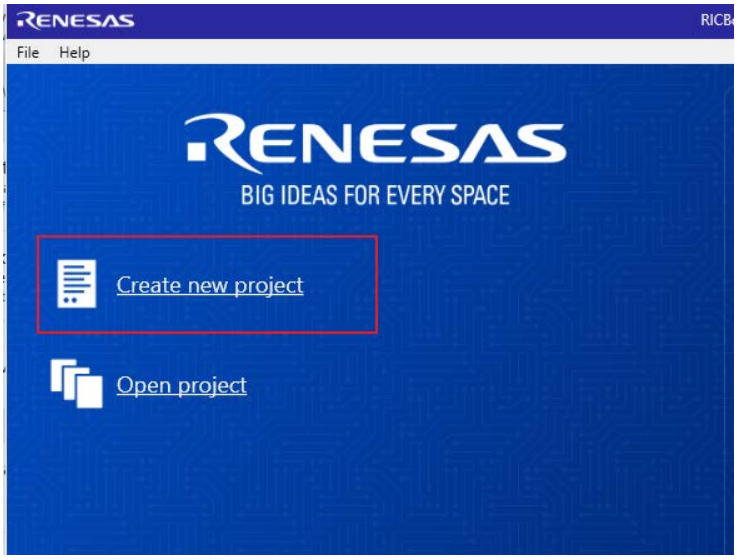

Figure 26. Create New Project in RICBox

3. Select *FemtoClock3* from the “Select a Product Family” list.
4. Select the product variant to evaluate, then click *OK*. In this example, the RC32312A is selected.

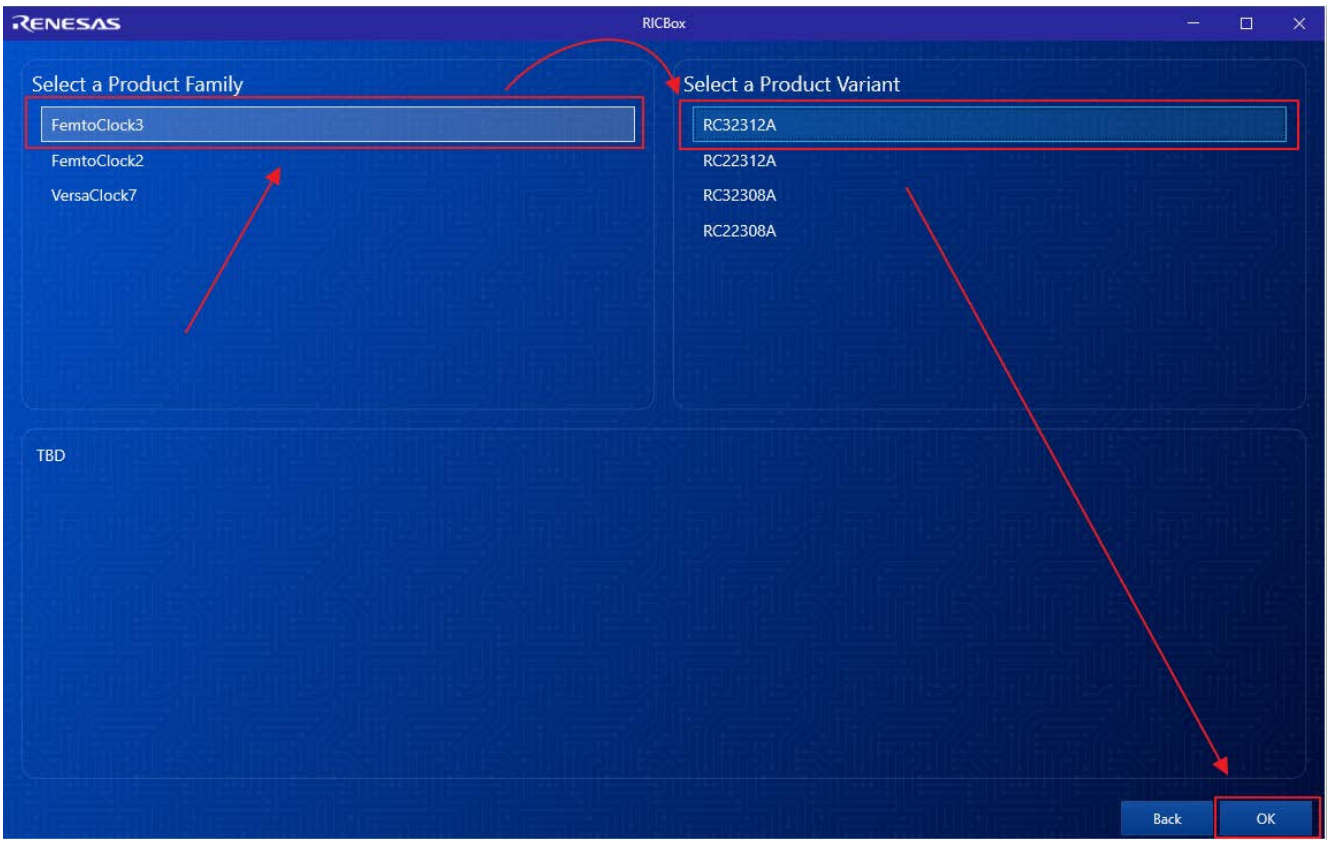

Figure 27. Selecting RC32312A Device GUI in RICBox

5. Follow the on-screen wizard (see Figure 28) to configure the device for general evaluation starting from “Inputs”, then “DPLL”, and finally ”Outputs”.

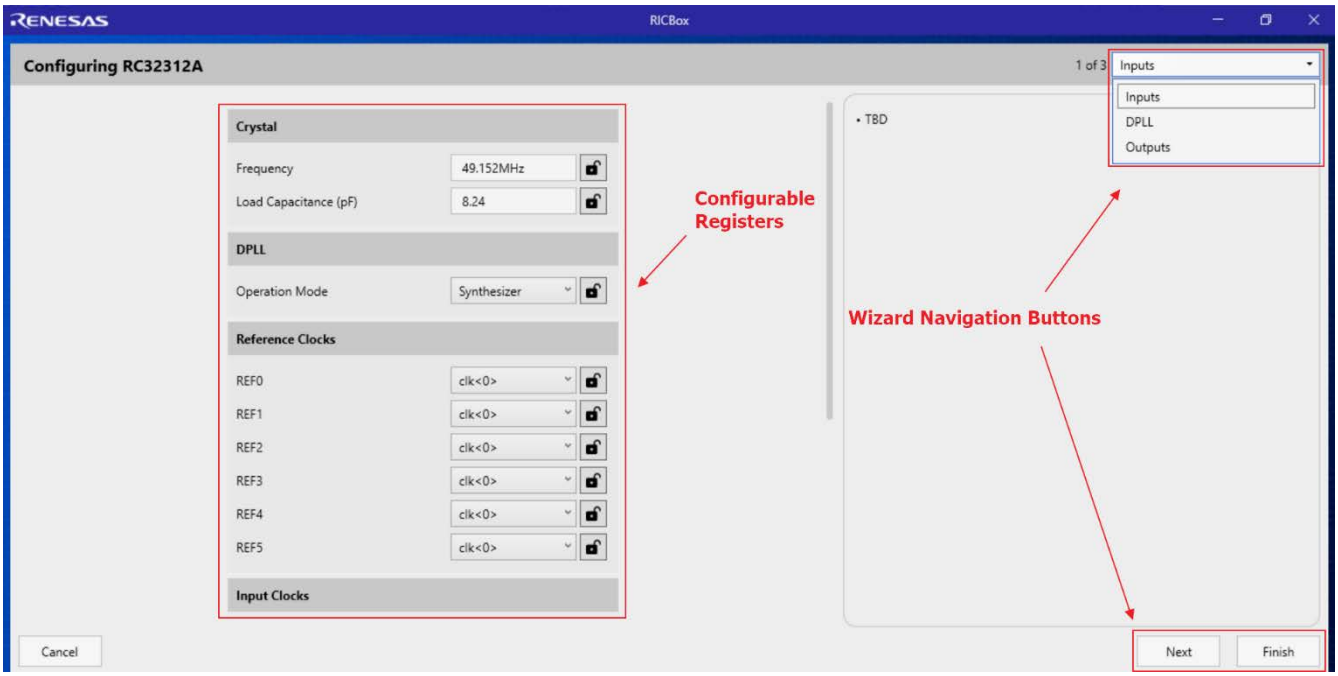

Figure 28. RICBox Wizard Navigation

6. Click on the *Finish* button after the settings are decided and to review the control panel page.
7. Use the side panel menu buttons (see Figure 29) to navigate through the GUI for all five separate pages.

Figure 29. RICBox GUI Menu Buttons

1.3.3. Configure the Evaluation Board

1. To establish communication between the EVB and the GUI, click the *Not Connected* button in the lower right corner, then click *Connect*.

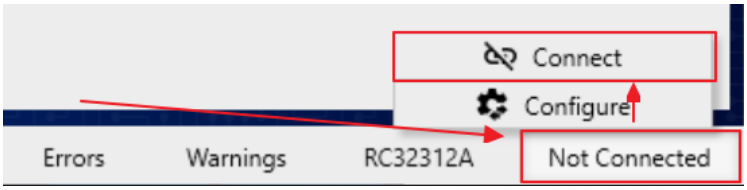

Figure 30. Connect to the Device in RICBox

2. Once the RICBox connection is established to the EVB, the “Not Connected” button will change to “Connected”.

Figure 31. Connected Button

3. Click the *Program* button to write all the changed registers from the GUI to the on-board device. Any register changes made after clicking the “Program” button will occur in real-time and the device will update.

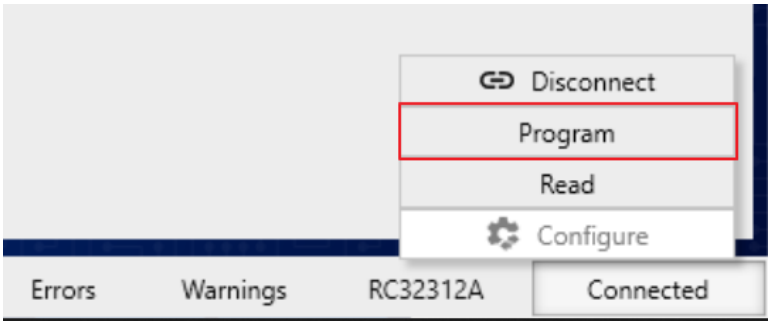

Figure 32. Program Button

2. Board Design

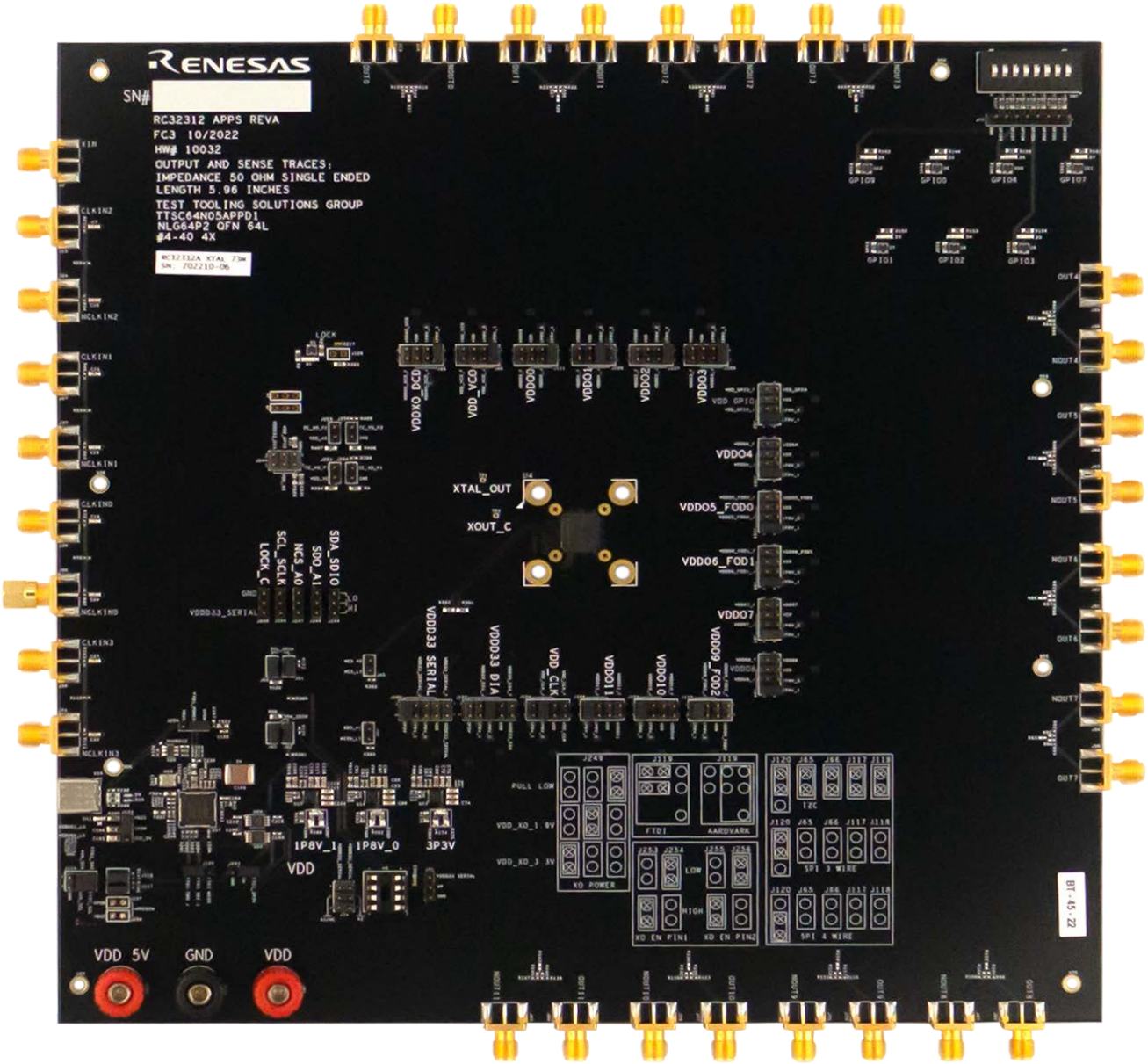

Figure 33. RC22312A/RC32312A Evaluation Board (Top)

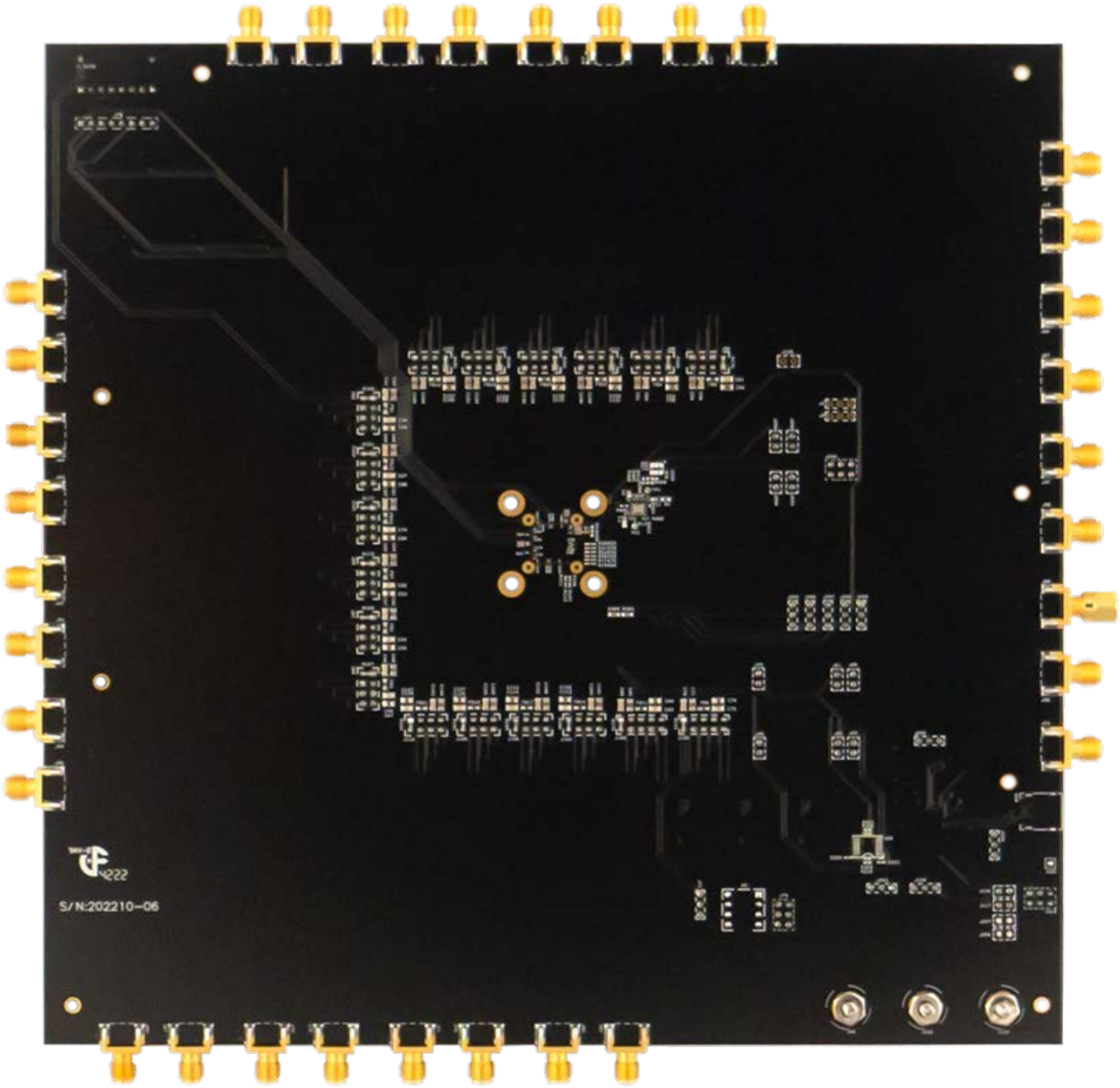

Figure 34. RC22312A/RC32312A Evaluation Board (Bottom)

2.1 Bill of Materials (BOM)

Item	Qty	Reference	Part	Manufacturer Part Number
1	9	C1,C7,C10,C13,C18,C19,C24,C27,C33	0.1µF	C0603C104K5R
2	7	C30,C71,C72,C96,C97,C117,C119	0.1µF	GCM188R71E104KA57D
3	36	C38,C41,C46,C49,C50,C53,C54,C57,C58, C61,C62,C65,C75,C78,C79,C82,C83,C86, C87,C90,C100,C103,C104,C107,C112,C114, C120,C123,C125,C128,C129,C132,C145, C148,C149,C152	0.1µF	GCM21BR71H104K
4	1	C39	10µF	GRM21BC71E106KE11L
5	37	C40,C47,C48,C51,C52,C55,C56,C59,C60, C63,C64,C76,C77,C80,C81,C84,C85,C88, C89,C101,C102,C105,C106,C108,C113, C121,C122,C126,C127,C130,C131,C146, C147,C150,C151,C196,C229	10µF	GRM21BC71E106K
6	7	C66,C68,C91,C93,C109,C115,C231	10µF	GRM188D70J106MA73D
7	7	C67,C69,C92,C94,C110,C116,C228	0.1µF	GCM155R71E104KE02D
8	6	C70,C73,C95,C98,C111,C118	22µF	GRM188R60J226M
9	3	C74,C99,C124	1µF	GCM188R71E105KA64D
10	18	C154,C156,C158,C160,C162,C164,C166, C168,C170,C172,C174,C176,C178,C180, C182,C184,C186,C188	0.1µF	GRM033C81E104M
11	17	C189,C190,C193,C194,C198,C200,C202, C204,C206,C207,C208,C209,C210,C218, C219,C220,C221	0.1µF	GRM155R61H104K
12	2	C191,C192	27pF	GRM1555C1E270J
13	1	C195	0.1µF	GRM21BR71E104K
14	2	C197,C230	0.010µF	GRM155R71E103J
15	1	C199	10µF	CGA9N3X7S2A106M230KE
16	3	C201,C203,C205	4.7µF	ZRB15XR61A475ME01
17	8	C211,C212,C213,C214,C215,C216,C217, C227	1000pF	GRM033R71E102J
18	1	C226	0.1µF	GRM155R71C104KA88D
19	9	D1,D2,D3,D4,D5,D6,D7,D8,D11	LED White	19-117Z/T1D-CN1P2B3X/3T
20	2	D9,D10	PGB1010603NR	PGB1010603NR
21	1	D12	1N4448HLP	1N4448HLP
22	22	FB1,FB3,FB4,FB5,FB6,FB7,FB8,FB9,FB10, FB11,FB12,FB13,FB14,FB15,FB16,FB17, FB18,FB19,FB20,FB21,FB22,FB28	220	BLM18BB221SN1D
23	4	FB23,FB24,FB25,FB26	600	BLM18AG601SN1D

Item	Qty	Reference	Part	Manufacturer Part Number
24	33	J2,J13,J15,J16,J18,J22,J23,J24,J26,J27,J28, J33,J35,J37,J38,J39,J40,J43,J47,J50,J51, J54,J58,J59,J60,J67,J70,J73,J75,J77,J79, J80,J83	Cinch_142_0701_801	142-0701-801
25	12	J45,J46,J61,J62,J65,J66,J117,J118,J253, J254,J255,J256	Headerstrip 1X2	22-28-4023
26	10	J71,J120,J124,J243,J244,J245,J246,J247, J248,J259	Headerstrip 1X3	22-28-4033
27	2	J74,J119	Headerstrip 2X3	10-89-7062
28	1	J76	Headerstrip 1X8	0022284083
29	2	J90,J123	Banana Post Red	7006
30	16	J92,J94,J96,J97,J98,J99,J101,J103,J104, J105,J106,J107,J108,J109,J110,J111	Headerstrip 2X4	10-89-7080
31	2	J100,J102	Headerstrip 2X5	10-89-7100
32	1	J121	Headerstrip 1X1	68000-401HLF
33	1	J125	Banana Post Black	7007
34	1	J249	Headerstrip 2X3	0010897062
35	10	R2,R99,R100,R141,R149,R152,R155,R158, R161,R164	4.70K	CRCW06034K70FK
36	9	R3,R144,R150,R153,R156,R159,R162,R165, R200	1.50K	CRCW06031K50FK
37	5	R9,R10,R394,R407,R408	4.99K	RC0603FR-074K99L
38	28	R15,R19,R23,R29,R33,R38,R43,R45,R52, R55,R60,R66,R68,R74,R78,R81,R88,R91, R95,R98,R106,R110,R116,R121,R123,R136, R139,R147	0.00	ERJ-2GE0R00X
39	8	R21,R34,R46,R57,R72,R82,R103,R112	49.9	ERA-2AEB49R9X
40	7	R126,R127,R129,R131,R133,R134,R137	1.00K	CRCW06031K00FKTA
41	3	R171,R178,R186	10.0K	RC0402JR-0710KL
42	3	R176,R183,R191	0.00	CRCW06030000Z0
43	2	R196,R197	4.70K	RC0402JR-074K7L
44	2	R198,R199	5.10K	CRCW04025K10FK
45	4	R201,R202,R203,R204	10.0	RC0402FR-0710RL
46	4	R211,R212,R213,R214	10.0K	ERJ-2RKF1002
47	1	R215	12.0K	CRCW040212K0FK
48	1	R216	2.00K	CRCW04022K00FKED
49	5	R375,R385,R386,R387,R388	20.0K	CPF-A-0603B20KE
50	9	R380,R381,R382,R383,R396,R398,R400, R402,R409	0.00	ERJ-2GE0R00

Item	Qty	Reference	Part	Manufacturer Part Number
51	1	R384	7.5K	TNPU06037K50BZEN00
52	5	R389,R390,R391,R392,R393	10.0K	RC0603JR-0710KL
53	2	R423,R424	0.00	ERJ-1GN0R00C
54	8	SO1,SO2,SO3,SO4,SO5,SO6,SO7,SO8	Standoff 25mm	25506
55	1	SW1	Slide 3Pos	KAT1108E
56	2	TP1,TP2	0552-1-15-01-11-27-10-0	0552-1-15-01-11-27-10-0
57	8	U1,U6,U7,U8,U9,U10,U11,U12	BSS138W	BSS138W
58	1	U4	RC22312A/RC32312A	RC22312A/RC32312A
59	1	U5	IC DIP Socket 8	A 08-LC-TT
60	3	U13,U14,U15	RAA214020	RAA214020
61	1	U16	USB Type C	12401598E4#2A
62	1	U17	FT232HQ	FT232HQ-REEL
63	1	U19	ABM8W-12.0000MHZ-6-B1U-T3	ABM8W-12.0000MHZ-6-B1U-T3
64	1	U20	93LC56BT-I/OT	93LC56BT-I/OT
65	2	U24,U25	PCA9517	PCA9517

3. Typical Performance Graphs

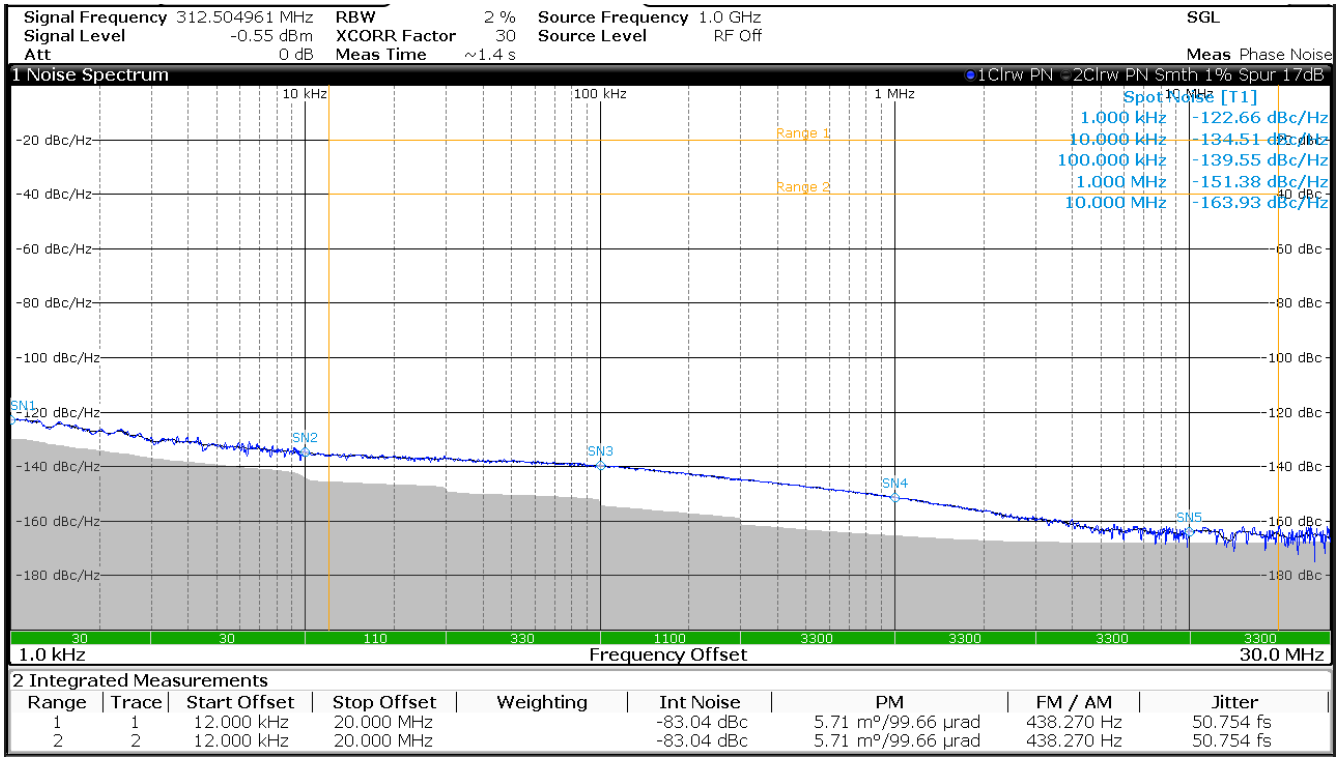

Figure 35. Phase Noise 312.5MHz Output Synthesizer Mode

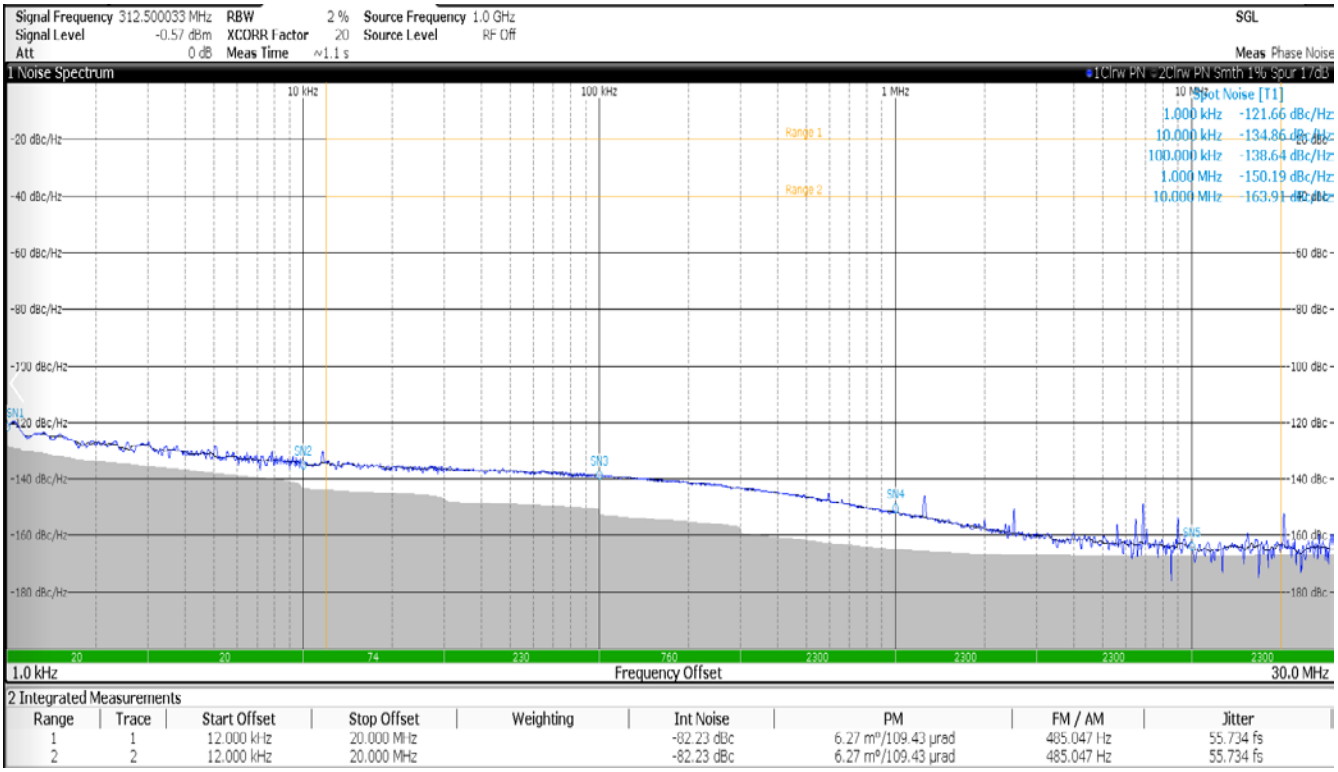

Figure 36. Phase Noise 312.5MHz Output Jitter Attenuation Mode

4. Ordering Information

Part Number	Description
RC32312A-EVK	RC21312A/RC32312A Evaluation Board

5. Revision History

Revision	Date	Description
1.00	Mar 28, 2023	Initial release.

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