RL78 FAMILY
HARDWARE MANUAL GUIDE
- ELECTRICAL CHARACTERISTICS EDITION

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RENESAS ELECTRONICS CORPORATION

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ABSOLUTE MAXIMUM RATINGS ①

This is the range of power supply voltage that will not damage the microcontroller.

This is the input voltage range for the REGC pin that will not damage the microcontroller.

These are the input voltage ranges for each pin that will not damage the microcontroller.

This is supplementary information regarding electrical characteristics. In order to use it correctly, it is necessary to confirm these conditions as well.

Item	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	EV_{DD0} = EV_{DD1}	-0.5 to +6.5	V
	EV_{SS0}, EV_{SS1}	EV_{SS0} = EV_{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.1 and -0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV_{DD0} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V_{DD} + 0.3 Note 2	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). The listed value is the absolute maximum rating of the REGC pin. Only use the capacitor connection. Do not apply a specific voltage to this pin.

Note 2. This voltage must be no higher than 6.5 V.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.**

That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

ABSOLUTE MAXIMUM RATINGS ②

This is the output voltage range for each pin that will not damage the microcontroller.

This is the input voltage range for the analog pin that will not damage the microcontroller.

This is supplementary information regarding electrical characteristics.
In order to use it correctly, it is necessary to confirm these conditions as well.

Item	Symbols	Conditions	Ratings	Unit
Output voltage	V_{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV_{DD0} + 0.3 and -0.3 to V_{DD} + 0.3 **Note 2**	V
	V_{O2}	P20 to P27, P121, P122, P150 to P156	-0.3 to V_{DD} + 0.3 **Note 2**	V
Analog input voltage	V_{AI1}	ANI16 to ANI26	-0.3 to EV_{DD0} + 0.3 and -0.3 to AV_{REFP} + 0.3 **Notes 2, 3**	V
	V_{AI2}	ANI0 to ANI14	-0.3 to V_{DD} + 0.3 and -0.3 to AV_{REFP} + 0.3 **Notes 2, 3**	V

Note 2. This voltage must be no higher than 6.5 V.

Note 3. The voltage on a pin in use for A/D conversion must not exceed AV_{REFP} + 0.3.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.**

That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

: Guaranteed values of characteristics and values that users should adhere to

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ABSOLUTE MAXIMUM RATINGS ③

This is the upper limit of the current that can flow during the high-level output of each pin to prevent damage to the microcontroller.

This is the upper limit of the current that can flow during the low-level output of each pin to prevent damage to the microcontroller.

This is supplementary information regarding electrical characteristics.
In order to use it correctly, it is necessary to confirm these conditions as well.

Item	Symbols	Conditions		Ratings	Unit
High-level output current	I_{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	-100	mA
	I_{OH2}	Per pin	P20 to P27, P121, P122, P150 to P156	-5	mA
		Total of all pins		-20	mA
Low-level output current	I_{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40 Note	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P121, P122, P150 to P156	10	mA
		Total of all pins		20	mA

Note The rating for the following port pins is 80 mA when I_{OL1} = 40.0 mA is specified by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P110 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin package products

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

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ABSOLUTE MAXIMUM RATINGS ④

Item	Symbols	Conditions		Ratings	Unit
Ambient operating temperature	T_A	In normal operation mode	3C: Industrial applications	-40 to +105	°C
			2D: Consumer applications	-40 to +85	
		In flash memory programming mode	3C: Industrial applications	-40 to +105	
			2D: Consumer applications	-40 to +85	
Storage temperature	T_{stg}			-65 to +150	°C

This is the temperature range for storage without operating the microcontroller.

This is supplementary information regarding electrical characteristics.
In order to use it correctly, it is necessary to confirm these conditions as well.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

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CHARACTERISTICS OF THE OSCILLATORS

CHARACTERISTICS OF X1 AND XT1 OSCILLATORS

37.2.1 Characteristics of the X1 oscillator

These are the assumptions for the specifications. Please make sure to confirm them.

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time Note	Ceramic resonator/ crystal resonator		0.05		1	μs

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

For the X1 oscillator circuit, you can use a ceramic oscillator or crystal oscillator with a nominal frequency ranging from 1MHz to 20MHz. There is no need to consider frequency tolerance deviation.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.**

37.2.2 Characteristics of the XT1 oscillator

Products with 30 to 36 pins have different power supply voltage conditions.

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V for the 30- to 36-pin products, 1.6 V ≤ VDD ≤ 5.5 V for the 40- to 128-pin products, VSS = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
XT1 clock oscillation frequency (fXT) Note	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

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CHARACTERISTICS OF THE OSCILLATORS

CHARACTERISTICS OF THE ON-CHIP OSCILLATORS

37.2.3 Characteristics of the On-chip Oscillators

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f_{IH}				1		32	MHz
High-speed on-chip oscillator clock frequency accuracy Note 1		HIPREC = 1	+85 to +105°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-2.0		+2.0	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-6.0		+6.0	%
			-20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-5.0		+5.0	%
			-40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-5.5		+5.5	%
		HIPREC = 0 Note 4			-15		0	%
High-speed on-chip oscillator clock correction resolution						0.05		%

This is the accuracy range of the clock frequency for the high-speed on-chip oscillator. The operation of the CPU and peripheral functions depends on the accuracy of the selected operating clock.

By adjusting the High-Speed On-Chip Oscillator Trimming Register (HIOTRM), fIH can be corrected. It indicates the frequency accuracy that changes when the setting value of HIOTRM is varied by 1.

Note 1. The accuracy values were obtained in testing of this product.

Note 2. The listed values only indicate the characteristics of the oscillators. Refer to AC Characteristics for instruction execution time.

Note 3. Guaranteed by characterization results.

Note 4. The listed condition applies when the setting of the FRQSEL3 bit is 1.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

PIN CHARACTERISTICS ①

This is the upper limit of the current that can flow during the high-level output of each pin. Please limit the current with external circuitry to not exceed this value.

This is the upper limit of the current that can flow per pin.

This is the total upper limit of the current that can flow through the relevant pins. "Duty ≤ 70%" indicates the percentage of time during which the current can flow.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable high-level output current Note 1	I_{OH1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV_{DD0} ≤ 5.5 V			-10.0 Note 2	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (when duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-55.0 Note 4	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-10.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			-5.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (when duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-80.0 Note 5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-19.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			-10.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			-5.0	mA
		Total of all pins (when duty ≤ 70% Note 3)	1.6 V ≤ EV_{DD0} ≤ 5.5 V			-135.0 Note 6	mA

(Notes, Caution, and Remark continue on the next page.)

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

PIN CHARACTERISTICS ②

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable high-level output current Note 1	I_{OH2}	Per pin for P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V			-3.0 Note 2	mA
			2.7 V ≤ V_{DD} < 4.0 V			-1.0 Note 2	mA
			1.8 V ≤ V_{DD} < 2.7 V			-1.0 Note 2	mA
			1.6 V ≤ V_{DD} < 1.8 V			-0.5 Note 2	mA
		Total of all pins (when duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			-5.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			-5.0	mA

The current value that can flow depends on the conditions of VDD.

When using with a duty > 70% condition, the current value that can flow becomes smaller. The average current that can flow remains unchanged.

The current value is different when products for industrial applications are used in the temperature range of -40°C to 105°C.

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the EV_{DD0}, EV_{DD1}, or V_{DD} pin to an output pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = (I_{OH} × 0.7)/(n × 0.01)

  Example when n = 80% and I_{OH} = -10.0 mA

  Total output current from the listed pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is -30 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of 85°C to 105°C.

Note 5. The maximum value is -50 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of 85°C to 105°C.

Note 6. The maximum values are respectively -100 mA and -60 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of -40°C to 85°C and of 85°C to 105°C.

Caution **The following pins are not capable of the output of high-level signals in the N-ch open-drain mode.**
P00, P02 to P04, P10 to P15, P17, P34, P42 to P45, P50, P52 to P55, P71, P72, P74, P80 to P83, P96, P120, and P142 to P144

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

PIN CHARACTERISTICS ③

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (2/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable low-level output current Note 1	IOL1	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				20.0 Notes 2, 3	mA
		Per pin for P60 to P63				15.0 Note 2	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (when duty ≤ 70% Note 4)	4.0 V ≤ EVDD0 ≤ 5.5 V			70.0 Note 5	mA
			2.7 V ≤ EVDD0 < 4.0 V			15.0	mA
			1.8 V ≤ EVDD0 < 2.7 V			9.0	mA
			1.6 V ≤ EVDD0 < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (when duty ≤ 70% Note 4)	4.0 V ≤ EVDD0 ≤ 5.5 V			80.0 Note 5	mA
			2.7 V ≤ EVDD0 < 4.0 V			35.0	mA
			1.8 V ≤ EVDD0 < 2.7 V			20.0	mA
			1.6 V ≤ EVDD0 < 1.8 V			10.0	mA
		Total of all pins (when duty ≤ 70% Note 4)				150.0 Note 6	mA

This is the upper limit of the current that can flow during the low-level output of each pin. Please limit the current with external circuitry to meet this specification.

This is the upper limit of the current that can flow per pin.

This is the total upper limit of the current that can flow through the relevant pins. "Duty ≤ 70%" indicates the percentage of time during which the current can flow.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

(Notes and Remark continue on the next page.)

DC CHARACTERISTICS

PIN CHARACTERISTICS ④

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (2/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable low-level output current Note 1	IOL2	Per pin for P20 to P27, P121, P122, P150 to P156	4.0 V ≤ VDD ≤ 5.5 V			8.5 Note 2	mA
			2.7 V ≤ VDD < 4.0 V			1.5 Note 2	mA
			1.8 V ≤ VDD < 2.7 V			0.6 Note 2	mA
			1.6 V ≤ VDD < 1.8 V			0.4 Note 2	mA
		Total of all pins (when duty ≤ 70% Note 4)	4.0 V ≤ VDD ≤ 5.5 V			20	mA
			2.7 V ≤ VDD < 4.0 V			20	mA
			1.8 V ≤ VDD < 2.7 V			15	mA
			1.6 V ≤ VDD < 1.8 V			10	mA

The current value that can flow depends on the conditions of VDD.

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the EVSS0, EVSS1, or VSS pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

This is the characteristic when used as a 40mA port output.

Note 3. The maximum rating for the following port pins is 40 mA when IOL1 = 40.0 mA is specified by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P101 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin package products

When using with a duty > 70% condition, the current value that can flow becomes smaller. The average current that can flow remains unchanged.

Note 4. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = $(I_{OL} \times 0.7)/(n \times 0.01)$
  Example when n = 80% and I_{OL} = 10.0 mA
  Total output current from the listed pins = $(10.0 \times 0.7)/(80 \times 0.01) \approx 8.7$ mA
  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

The current value is different when products for industrial applications are used in the temperature range of -40°C to 105°C.

Note 5. The maximum value is 40 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of 85°C to 105°C.

Note 6. The maximum value is 80 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of 85°C to 105°C.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

: Guaranteed values of characteristics and values that users should adhere to

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: Explanation subject

DC CHARACTERISTICS

PIN CHARACTERISTICS ⑤

This is the voltage range in which the read value of the port register reliably becomes "1".

The characteristics change when set as a TTL input buffer.

P60-P63 are pins with a voltage withstand capability of 6V.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8 EV_{DD0}		EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV_{DD0} ≤ 5.5 V	2.2		EV_{DD0}	V
			TTL input buffer 3.3 V ≤ EV_{DD0} < 4.0 V	2.0		EV_{DD0}	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	1.5		EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P156		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63		0.7 EV_{DD0}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P34, P42 to P45, P50, P52 to P55, P71, P72, P74, P80 to P83, P96, P120, and P142 to P144 is EV_{DD0}, even in the N-ch open-drain mode.

: Guaranteed values of characteristics and values that users should adhere to

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DC CHARACTERISTICS

PIN CHARACTERISTICS ⑥

This is the voltage range in which the read value of the port register reliably becomes “0".

The characteristics change when set as a TTL input buffer.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2 EV_{DD0}	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV_{DD0} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27, P150 to P156		0		0.3 V_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 EV_{DD0}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

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: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

PIN CHARACTERISTICS ⑦

This is the voltage value output from the pin during high-level output. The voltage value varies depending on the conditions of IOH.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (4/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output voltage, high	V_{OH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -10.0 mA	EV_{DD0} - 1.5			V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -3.0 mA	EV_{DD0} - 0.7			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -2.0 mA	EV_{DD0} - 0.6			V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -1.5 mA	EV_{DD0} - 0.5			V
			1.6 V ≤ EV_{DD0} < 5.5 V, I_{OH1} = -1.0 mA	EV_{DD0} - 0.5			V
	V_{OH2}	P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = -3.0 mA	V_{DD} - 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH2} = -1.0 mA	V_{DD} - 0.5			V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH2} = -1.0 mA	V_{DD} - 0.5			V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OH2} = -0.5 mA	V_{DD} - 0.5			V

Caution **P00, P02 to P04, P10 to P15, P17, P34, P42 to P45, P50, P52 to P55, P71, P72, P74, P80 to P83, P96, P120, and P142 to P144 do not output high-level signals in the N-ch open-drain mode.**

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

PIN CHARACTERISTICS ⑧

This is the voltage value output from the pin during low-level output. The voltage value varies depending on the conditions of IOL.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (5/7)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Output voltage, low	V_{OL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 20.0 mA			1.3	V
				I_{OL1} = 40.0 mA Note			1.3	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 8.5 mA			0.7	V
				I_{OL1} = 17.0 mA Note			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 3.0 mA			0.6	V
				I_{OL1} = 6.0 mA Note			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 1.5 mA			0.4	V
				I_{OL1} = 3.0 mA Note			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 0.6 mA			0.4	V
				I_{OL1} = 1.2 mA Note			0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 0.3 mA			0.4	V
				I_{OL1} = 0.6 mA Note			0.4	V
	V_{OL2}	P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 8.5 mA				0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL2} = 1.5 mA				0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL2} = 0.6 mA				0.4	V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OL2} = 0.4 mA				0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 15.0 mA				2.0	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 5.0 mA				0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 3.0 mA				0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 2.0 mA				0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 1.0 mA				0.4	V

Note The listed value applies when I_{OL1} = 40.0 mA is specified for the following port pins by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P101 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin products

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

PIN CHARACTERISTICS ⑨

This is the value of the current that can flow when the output current control function is enabled.
If an external resistance is connected, the current is limited by the limiting resistor.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (6/7)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Output current[Note]	$CCDI_{OL}$	P16, P17, P50, P51 P60 to P63	CCSm = 01H	4.0 V ≤ EV_{DD0} ≤ 5.5 V	1.0	1.8	2.6	mA
				2.7 V ≤ EV_{DD0} < 4.0 V	0.8	1.5	2.3	mA
			CCSm = 02H	4.0 V ≤ EV_{DD0} ≤ 5.5 V	3.0	4.9	6.5	mA
				3.0 V ≤ EV_{DD0} < 4.0 V	2.7	4.3	5.9	mA
			CCSm = 03H	4.0 V ≤ EV_{DD0} ≤ 5.5 V	6.6	10.0	13.2	mA
				3.3 V ≤ EV_{DD0} < 4.0 V	6.0	9.1	12.1	mA
		P60 to P63	CCSm = 04H	4.0 V ≤ EV_{DD0} ≤ 5.5 V	10.2	15.0	19.8	mA
				3.3 V ≤ EV_{DD0} < 4.0 V	9.4	13.8	18.2	mA

Note The listed currents apply when the output current control function is enabled.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

PIN CHARACTERISTICS ⑩

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (7/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leakage current, high	ILIH1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	VI = EVDD0			0.5	μA
	ILIH2	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	VI = VDD			0.5	μA
	ILIH3	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	VI = VDD			0.5	μA
Input leakage current, low	ILIL1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	VI = EVSS0			-0.5	μA
	ILIL2	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	VI = VSS			-0.5	μA
	ILIL3	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	VI = VSS			-0.5	μA
On-chip pll-up resistance	RU	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120 to P122, P125 to P127, P140 to P147	VI = EVSS0, In input port	10	20	100	kΩ

This is the current that flows through the transistor on the VSS/EVSS0 side when the input pin is allowed to have the same voltage level as VDD/EVDD0.

This is the current that flows through the transistor on the VDD/EVDD0 side when the input pin is allowed to have the same voltage level as VSS/EVSS0.

It is the resistance value of the pull-up resistor set by the pull-up resistor option register (PUxx).

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

SUPPLY CURRENT CHARACTERISTICS ①

This is the total current flowing through VDD and EVDD.

The operating mode indicates the CPU's operating state.

The value of the current flowing through the CPU varies depending on its processing.

The current value flowing through depends on the flash operating mode.

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.3	—	mA
						V_{DD} = 1.8 V		1.3	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
			LS (low-speed main) mode	f_{IH} = 24 MHz Note 2	Normal operation	V_{DD} = 5.0 V		2.3	3.8	mA
						V_{DD} = 1.8 V		2.3	3.8	
				f_{IH} = 16 MHz Note 2	Normal operation	V_{DD} = 5.0 V		1.7	2.7	mA
						V_{DD} = 1.8 V		1.7	2.7	
				f_{IM} = 4 MHz Note 3	Normal operation	V_{DD} = 5.0 V		0.4	0.7	mA
						V_{DD} = 1.6 V		0.4	0.7	
			LP (low-power main) mode	f_{IM} = 2 MHz Note 3	Normal operation	V_{DD} = 5.0 V		200	325	μA
						V_{DD} = 1.6 V		200	325	
				f_{IM} = 1 MHz Note 3	Normal operation	V_{DD} = 5.0 V		112	178	μA
						V_{DD} = 1.6 V		111	176	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		1.9	3.2	mA
						V_{DD} = 1.8 V		1.9	3.2	

(Remarks are listed on the next page.)

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

SUPPLY CURRENT CHARACTERISTICS ②

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	LS (low-speed main) mode	fMX = 20 MHz Note 4, Square wave input	Normal operation	VDD = 5.0 V		1.8	3.0	mA
						VDD = 1.8 V		1.7	3.0	
				fMX = 20 MHz Note 4, Resonator connection	Normal operation	VDD = 5.0 V		1.9	3.2	mA
						VDD = 1.8 V		1.9	3.2	
				fMX = 10 MHz Note 4, Square wave input	Normal operation	VDD = 5.0 V		0.9	1.6	mA
						VDD = 1.8 V		0.9	1.6	
				fMX = 10 MHz Note 4, Resonator connection	Normal operation	VDD = 5.0 V		1.0	1.7	mA
						VDD = 1.8 V		1.0	1.7	
				fMX = 8 MHz Note 4, Square wave input	Normal operation	VDD = 5.0 V		0.8	1.3	mA
						VDD = 1.8 V		0.7	1.3	
				fMX = 8 MHz Note 4, Resonator connection	Normal operation	VDD = 5.0 V		0.9	1.4	mA
						VDD = 1.8 V		0.8	1.4	

The value of the current flowing varies depending on the CPU clock used.

These are the specified conditions for the power supply current.

Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

SUPPLY CURRENT CHARACTERISTICS ③

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 2, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.2	5.5	μA
						T_A = +25°C		3.5	5.8	
						T_A = +50°C		3.8	8.5	
						T_A = +70°C		4.4	13.8	
						T_A = +85°C		5.3	22.1	
						T_A = +105°C		7.7	40.9	
				f_{SUB} = 32.768 kHz Note 3, Square wave input	Normal operation	T_A = -40°C		3.2	5.6	μA
						T_A = +25°C		3.4	5.7	
						T_A = +50°C		3.7	8.5	
						T_A = +70°C		4.3	13.7	
						T_A = +85°C		5.2	21.4	
						T_A = +105°C		7.6	39.0	
				f_{SUB} = 32.768 kHz Note 3, Resonator connection	Normal operation	T_A = -40°C		3.2	5.2	μA
						T_A = +25°C		3.4	5.4	
						T_A = +50°C		3.7	7.7	
						T_A = +70°C		4.3	13.4	
						T_A = +85°C		5.2	20.9	
						T_A = +105°C		7.7	38.5	

If the value varies significantly depending on the ambient temperature, the ambient temperature will be included as a specified condition.

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

SUPPLY CURRENT CHARACTERISTICS ④

This is the current flowing into VDD when the peripheral functions are operational.

The watchdog timer operating current includes the low-speed on-chip oscillator clock operating current.

This is the current flowing into the AVREFP pin.

This is the current flowing when selecting the internal reference voltage as the + side reference voltage of the A/D converter or when selecting the internal reference voltage as the A/D conversion target.

This is the current flowing when selecting the temperature sensor output voltage as the A/D conversion target.

4. Peripheral Functions (Common to all products)

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FIH} Note 1				380		μA
Middle-speed on-chip oscillator operating current	I_{FIM} Note 1				20		μA
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.3		μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{RTCCLK} = 32.768 kHz			0.005		μA
		f_{RTCCLK} = 128 Hz			0.002		μA
32-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.04		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 32.768 kHz (typ.)			0.32		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		0.95	1.6	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.75	mA
AV_{REFP} current	I_{ADREF} Note 7	AV_{REFP} = 5.0 V			52		μA
A/D converter internal reference voltage current	I_{ADREF} Note 1				114		μA
Temperature sensor operating current	I_{TMPS} Note 1				110		μA

(Notes and Remarks continue on the next page.)

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DC CHARACTERISTICS

SUPPLY CURRENT CHARACTERISTICS ⑤

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (1/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
D/A converter operating current	IDAC **Notes 1, 8**	Per channel			150		μA
Comparator operating current	ICMP **Notes 1, 9**				6		μA
LVD operating current	ILVD0 **Notes 1, 10**				0.02		μA
	ILVD1 **Notes 1, 10**				0.02		μA
Self-programming operating current	IFSP **Notes 1, 11**				2.5	12.2	mA
Data flash rewrite operating current	IBGO **Notes 1, 12**				2.5	12.2	mA
SNOOZE mode sequencer operating current	ISMS **Notes 1, 13**	fIH = 32 MHz	30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.1		mA
			30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.1		
			44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products		1.4		
		fIL = 32.768 kHz	30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.2		μA
			30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.2		
			44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products		1.6		

The TYP. value represents the average current. The MAX. value represents the maximum current that flows momentarily.

These values do not include the current flowing through IDD1, IDD2, and IDD3.

It is the average current when executing various sequencer processing commands.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

(Notes and Remarks continue on the next page.)

AC CHARACTERISTICS ①

37.4 AC Characteristics

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (fMAIN) operation	HS (high-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ VDD ≤ 1.8 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ VDD ≤ 1.8 V	0.25		1	μs
			LP (low-power main) mode	1.6 V ≤ VDD ≤ 5.5 V	0.5		1	μs
		Subsystem clock (fSUB) operation		1.6 V ≤ VDD ≤ 5.5 V	26.041	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ VDD ≤ 1.8 V	0.5		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ VDD ≤ 1.8 V	0.5		1	μs
External system clock frequency	fEX	1.8 V ≤ VDD ≤ 5.5 V			1.0		20.0	MHz
		1.6 V ≤ VDD < 1.8 V			1.0		4.0	MHz
	fEXS				32		38.4	kHz
External system clock input high-level width, low-level width	tEXH, tEXL	1.8 V ≤ VDD ≤ 5.5 V			15			ns
		1.6 V ≤ VDD < 1.8 V			120			ns

The MIN. and MAX. values of the instruction cycle vary depending on the conditions.

Note: Operating frequency = 1 / (instruction cycle)

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

(Note and Remark are listed on the next page.)

AC CHARACTERISTICS ②

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	tTIH, tTIL			1/fMCK + 10			nsNote
TO00 to TO07, TO10 to TO17 output frequency	fTO	HS (high-speed main) mode LS (low-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz
			1.8 V ≤ EVDD0 < 2.7 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LP (low-power main) mode	1.6 V ≤ EVDD0 ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	fPCL	HS (high-speed main) mode LS (low-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz
			1.8 V ≤ EVDD0 < 2.7 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LP (low-power main) mode	1.6 V ≤ EVDD0 < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	fINTH, fINTL	INTP0	1.6 V ≤ VDD ≤ 5.5 V	1			µs
		INTP1 to INTP11	1.6 V ≤ EVDD0 ≤ 5.5 V	1			µs
Key interrupt input low-level width	fKRH, fKRL	KR0 to KR7	1.8 V ≤ EVDD0 ≤ 5.5 V	250			ns
			1.6 V ≤ EVDD0 < 1.8 V	1			µs
$\overline{\text{RESET}}$ low-level width	fRSL			10			µs

The MIN. and MAX. values of the output frequency vary depending on the power supply voltage.

The MIN. and MAX. values of the output frequency vary depending on the power supply voltage.

The MIN. value indicates the reliably detectable range. MIN. There is a possibility of detecting signals even below the MIN. value.

Note The following conditions are required for low voltage interface when EVDD0 < VDD.
1.8 V ≤ EVDD0 < 2.7 V: 125 ns min.
1.6 V ≤ EVDD0 < 1.8 V: 250 ns min.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

37.5.1 Serial array unit

1. In UART communications with devices operating at same voltage levels

(T_A = −40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate **Note 1**		1.6 V ≤ EV_{DD0} ≤ 5.5 V		f_{MCK}/6 **Note 2**		f_{MCK}/6 **Note 2**		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} **Note 3**		5.3		4		0.33	Mbps

Note 1. The transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

Note 2. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V: 2.6 Mbps max.
1.8 V ≤ EV_{DD0} < 2.4 V: 1.3 Mbps max.
1.6 V ≤ EV_{DD0} < 1.8 V: 0.6 Mbps max.

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are as follows.
HS (high-speed main) mode : 32 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode : 24 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)
LP (low-power main) mode : 2 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution **Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

When the high-level voltage applied to the RxDq pin is at the same potential as EVDD, this electrical characteristic is applicable.

These are the specified conditions for the peripheral function characteristics.

: Guaranteed values of characteristics and values that users should adhere to
: Guaranteed value of characteristics
: Explanation subject

CHARACTERISTICS OF THE PERIPHERAL FUNCTIONS

SERIAL ARRAY UNIT ②

When the high-level voltage applied to the SIp pin is at the same potential as EVDD, this electrical characteristic is applicable. CSI00 allows for a faster transfer rate compared to other channels. However, different conditions for the power supply voltage apply.

2. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock (the ratings below are only applicable to CSI00)

(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V	62.5		83.3		1000		ns
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	83.3		125		1000		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 7		t_{KCY1}/2 - 10		t_{KCY1}/2 - 50		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 10		t_{KCY1}/2 - 15		t_{KCY1}/2 - 50		ns
SIp setup time (to SCKp↑)Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		23		33		110		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		33		50		110		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp outputNote 2	t_{KSO1}	C = 20 pFNote 3			10		10		10	ns

These are the specified conditions for the peripheral function characteristics.

Note 1. The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the SIp setup time becomes "to SCKp↓" and that for the SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).**

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

CHARACTERISTICS OF THE PERIPHERAL FUNCTIONS

SERIAL ARRAY UNIT ③

5. In simplified I^2C communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		1000 Note 1		400 Note 1	kHz
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
Hold time when SCLr is low	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns
Hold time when SCLr is high	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

5. In simplified I²C communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 **Note 2**		1/f_{MCK} + 85 **Note 2**		1/f_{MCK} + 145 **Note 2**		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 **Note 2**		1/f_{MCK} + 145 **Note 2**		1/f_{MCK} + 145 **Note 2**		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 **Note 2**		1/f_{MCK} + 230 **Note 2**		1/f_{MCK} + 230 **Note 2**		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 290 **Note 2**		1/f_{MCK} + 290 **Note 2**		1/f_{MCK} + 290 **Note 2**		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns

Note 1. The listed times must be no greater than f_{MCK}/4.

Note 2. Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

Caution **Select the normal input buffer and the N-ch open drain output (withstand voltage of V_{DD} (when 30- to 52-pin products)/withstand voltage of EV_{DD} (when 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

37.5.2 Serial interface UARTA

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate			200	0	153600	bps

Caution **Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

1. I^2C standard mode

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	0		100	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7			μs
Hold time[Note 1]	$t_{HD:STA}$		4.0			μs
Hold time when SCLA0 is low	t_{LOW}		4.7			μs
Hold time when SCLA0 is high	t_{HIGH}		4.0			μs
Data setup time (reception)	$t_{SU:DAT}$		250			ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0		3.45	μs
Setup time of stop condition	$t_{SU:STO}$		4.0			μs
Bus-free time	t_{BUF}		4.7			μs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution **The listed frequency and times apply even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.**

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

ANALOG CHARACTERISTICS

A/D CONVERTER CHARACTERISTICS ①

37.6.1 A/D converter characteristics

1. Normal modes 1 and 2

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f_{AD}			1		32	MHz
Overall error Notes 1, 3, 4, 5	AINL	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±7.5	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
Conversion time Note 6	t_{CONV}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
Zero-scale error Notes 1, 2, 3, 4, 5	E_{ZS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Full-scale error Notes 1, 2, 3, 4, 5	E_{FS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR

The total error (LSB) at 10-bit resolution is obtained by dividing it by 4 (= 2^ (12-10)) .

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

(Note and Remark are listed on the next page.)

ANALOG CHARACTERISTICS

A/D CONVERTER CHARACTERISTICS ②

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Integral linearity error Notes 1, 4, 5	ILE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
Differential linearity error Note 1	DLE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

The characteristics vary depending on factors such as the selected analog input channel and other conditions.

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.
Overall error: Add ±3 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Note 4. When reference voltage (+) = V_{DD} and reference voltage (-) = V_{SS}, the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.
Integral linearity error: Add ±4 LSB to the maximum value.

Note 5. When AV_{REFP} < V_{DD}, the maximum values are as follows.
Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.
Integral linearity error: Add (±0.2 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use standard mode 2 with the longer sampling time.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

37.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.42	1.48	1.54	V
Temperature coefficient	F_{VTMPS}	Temperature dependency of the temperature sensor voltage		-3.3		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

These are the characteristics of the temperature sensor output voltage that can be specified as the A/D conversion target.

These are the characteristics of the + side reference voltage of the A/D converter or the internal reference voltage that can be specified as the A/D conversion target.

37.6.3 D/A converter characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES					8	Bit
Overall error	AINL	Rload = 8 MΩ	1.8 V ≤ V_{DD} ≤ 5.5 V			± 2.5	LSB
		Rload = 4 MΩ	1.8 V ≤ V_{DD} ≤ 5.5 V			± 2.5	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V ≤ V_{DD} ≤ 5.5 V			3	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V			6	μs

This is the time it takes for the set voltage to be output.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

ANALOG CHARACTERISTICS
COMPARATOR CHARACTERISTICS

37.6.4 Comparator characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage range	I_{VREF}	Input to the IVREF0 and IVREF1 pins C0LVL = 0, C1LVL = 0		0		V_{DD} - 1.4 and EV_{DD0}	V
		Input to the IVREF0 and IVREF1 pins C0LVL = 1, C1LVL = 1		1.4		EV_{DD0}	V
	I_{VCMP}	Input to the IVCMP0 and IVCMP1 pins		-0.3		EV_{DD0} + 0.3	V
Output delay	td	V_{DD} = 3.0 V, Input slew rate > 1 V/μs	High-speed mode			1.5	μs
			Low-speed mode		3.0		μs
Offset voltage	—	High-speed mode				50	mV
		Low-speed mode				40	mV
Operation stabilization wait time	t_{CMP}			30			μs
Internal reference voltage	V_{BGR2}			1.4		1.6	V

These are the characteristics of the internal reference voltage that can be selected as the reference voltage for Comparator 0.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

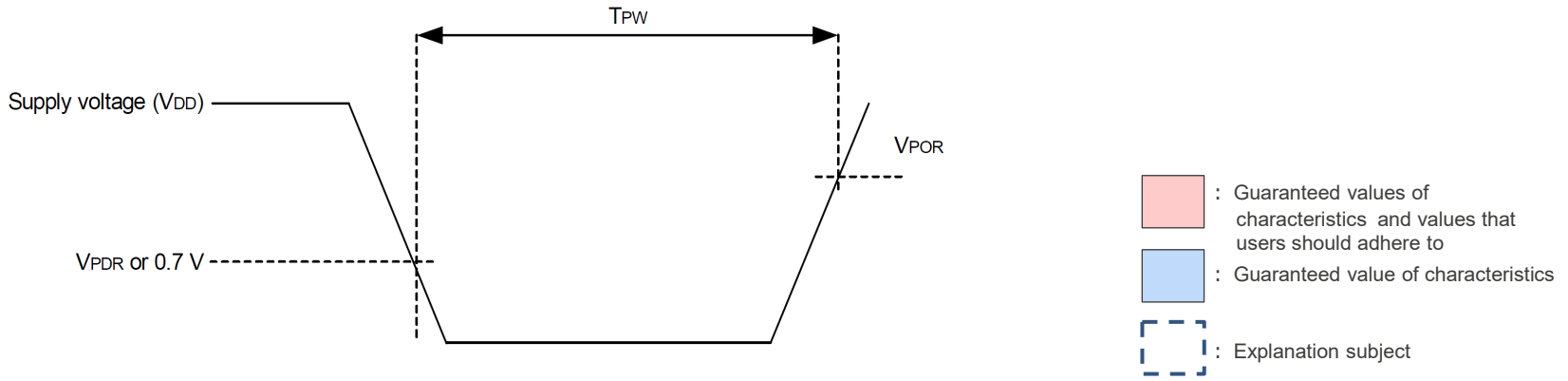
37.6.5 POR circuit characteristics

(TA = -40 to +105°C, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	VPOR, VPDR		1.43	1.50	1.57	V
Minimum pulse width[Note]	TPW		300			μs

Voltage fluctuations of less than 300us may not result in a reset occurring.

Note This width is the minimum time required for a POR reset when VDD falls below VPDR. This width is also the minimum time required for a POR reset from when VDD falls below 0.7 V to when VDD exceeds VPOR in the STOP mode or while the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



ANALOG CHARACTERISTICS
LVD CIRCUIT CHARACTERISTICS

37.6.6 LVD circuit characteristics

1. LVD0 Detection Voltage in the Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	V_{LVD00}	The power supply voltage is rising.	3.84	3.96	4.08	V
			The power supply voltage is falling.	3.76	3.88	4.00	V
		V_{LVD01}	The power supply voltage is rising.	2.88	2.97	3.06	V
			The power supply voltage is falling.	2.82	2.91	3.00	V
		V_{LVD02}	The power supply voltage is rising.	2.59	2.67	2.75	V
			The power supply voltage is falling.	2.54	2.62	2.70	V
		V_{LVD03}	The power supply voltage is rising.	2.31	2.38	2.45	V
			The power supply voltage is falling.	2.26	2.33	2.40	V
		V_{LVD04}	The power supply voltage is rising.	1.84	1.90	1.95	V
			The power supply voltage is falling.	1.80	1.86	1.91	V
		V_{LVD05}	The power supply voltage is rising.	1.64	1.69	1.74	V
			The power supply voltage is falling.	1.60	1.65	1.70	V
Minimum pulse width		t_{LW}		500			µs
Detection delay time						500	µs

This is the time required to detect the state of VDD≧VLVD0 or VDD＜VLVD0. Voltage fluctuations of less than 500us may not result in LVD reset or interrupt requests being generated.

This is the time from the state of VDD≧VLVD0 or VDD＜VLVD0 until an LVD reset or interrupt request is generated.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

ANALOG CHARACTERISTICS

POWER SUPPLY VOLTAGE RISING SLOPE CHARACTERISTICS

37.6.7 Power supply voltage rising slope characteristics

(TA = -40 to +105°C, VSS = 0 V)

This is the specification for when power is turned on. It is not a specification for ripple voltage.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD0 circuit or an external reset until VDD reaches the operating voltage range shown in AC characteristics.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

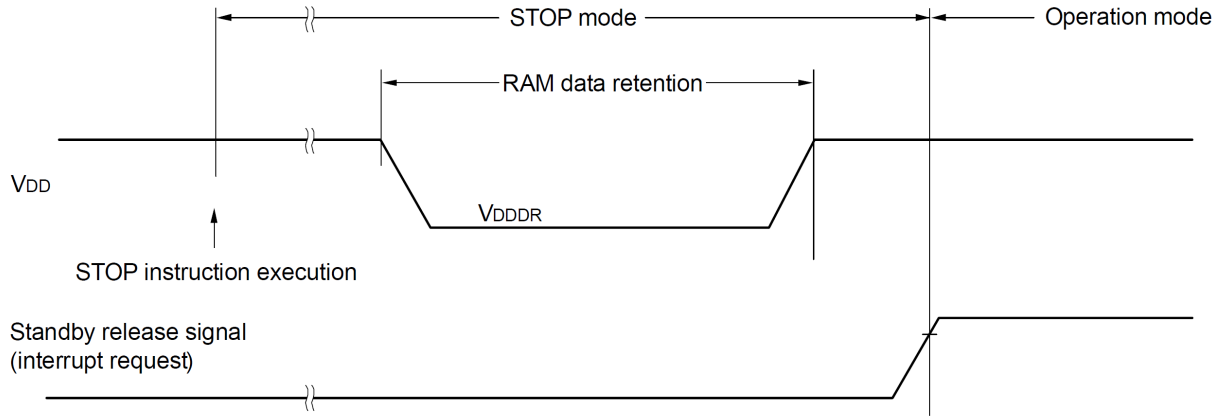
RAM DATA RETENTION CHARACTERISTICS

37.7 RAM Data Retention Characteristics

(T_A = -40 to +105°C, V_{SS} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}		1.43[Note]		5.5	V

Note This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

FLASH MEMORY PROGRAMMING CHARACTERISTICS ①

37.8 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}		1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
		Retained for 20 years T_A = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. The listed numbers of times apply when using flash memory programmer and Renesas Electronics self programming library.

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

FLASH MEMORY PROGRAMMING CHARACTERISTICS ②

This is the characteristic of code flash memory during self-programming for rewriting.

1. Code flash memory

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbol	f_{CLK} = 1 MHz			f_{CLK} = 2 MHz, 3 MHz			4 MHz ≤ f_{CLK} < 8 MHz			8 MHz ≤ f_{CLK} < 32 MHz			f_{CLK} = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	2 Kbytes	t_{E2K}	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	ms
Blank checking time	4 bytes	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	2 Kbytes	t_{BC2K}	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Security setting time		t_{AWSSAS}	—	18.2	526.2	—	14.4	469.2	—	12.5	441.1	—	11.6	427.1	—	11.3	422.6	ms
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs

Caution **The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.**

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

FLASH MEMORY PROGRAMMING CHARACTERISTICS ③

This is the characteristic of data flash memory during self-programming for rewriting.

2. Data flash memory

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbol	f_{CLK} = 1 MHz			f_{CLK} = 2 MHz, 3 MHz			4 MHz ≤ f_{CLK} < 8 MHz			8 MHz ≤ f_{CLK} < 32 MHz			f_{CLK} = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	256 bytes	t_{E2K}	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	ms
Blank checking time	1 byte	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	256 bytes	t_{BC2K}	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs
Time until reading starts following setting DFLEN to 1		—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	µs

Caution **The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.**

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

DEDICATED FLASH MEMORY PROGRAMMER COMMUNICATION (UART)

This is the transfer rate when using the dedicated flash memory programmer (PG-FP6).

37.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

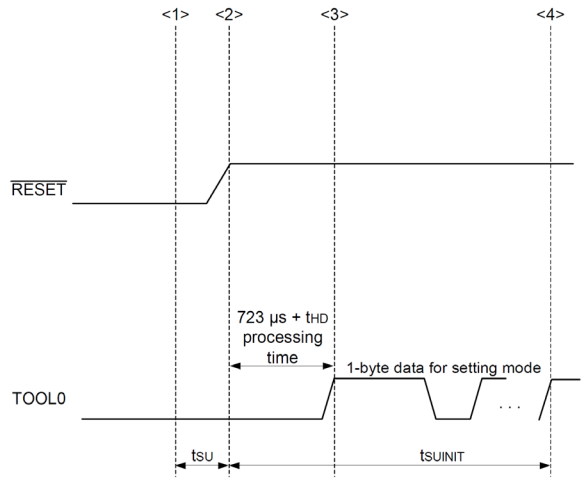
: Explanation subject

TIMING OF ENTRY TO FLASH MEMORY PROGRAMMING MODES

37.10 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (the processing time of the firmware to control the flash memory is not included)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset is released. Note that the POR and LVD reset must be released before the external reset is released.
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

: Guaranteed values of characteristics and values that users should adhere to

: Guaranteed value of characteristics

: Explanation subject

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