User's Manual

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RZ/N1D Group, RZ/N1S Group, RZ/N1L Group

User's Manual: System Introduction, Multiplexing, Electrical and Mechanical Information

RZ Family
RZ/N Series

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Objective and Target Users

This manual was written to explain the hardware functions and electrical characteristics of this LSI to the target users, i.e. those who will be using this LSI in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logic circuits, and microcomputers.

This manual is organized in the following items: an overview of the product, descriptions of the CPU, system control functions, and peripheral functions, electrical characteristics of the device, and usage notes.

When designing an application system that includes this LSI, take all points to note into account.
Points to note are given in their contexts and at the final part of each section, and in the section giving usage notes.

The list of revisions is a summary of major points of revision or addition for earlier versions. It does not cover all revised items. For details on the revised points, see the actual locations in the manual.

The following documents have been prepared for reference.

■ Documents related to RZ/N1

Document Name	Document Number
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group DATASHEET	R01DS0323EJ****
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: System Introduction, Multiplexing, Electrical and Mechanical Information	R01UH0750EJ**** (this manual)
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: System Control and Peripheral	R01UH0751EJ****
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: Peripherals	R01UH0752EJ****
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: R-IN Engine and Ethernet Peripherals	R01UH0753EJ****
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: PWMTimer	R01UH0913EJ****

2. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

X.X.X [Register Name]

(2)

Address: XXXX XXXXh

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	[Bit Field]					—	—	[Bit Field]		—	[Bit]	[Bit]	[Bit]
Value after reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0

Table X.X [Register Name] Register Contents

Bit Position	Bit Name	Function	R/W
b12 to b8	[Bit Field]	[Description]	R/W
b5 to b4	[Bit Field]	[Description] 2'b00: Hi-Z 2'b01: L Output Others: Prohibited (3)	R/W
b2	[Bit]	[Description] 1'b0: H-Z 1'b1: Output (defult)	R/W
b1	[Bit]	[Description] 1'b0: H-Z 1'b1: Output (defult)	R/W
b0	[Bit]	[Description] 1'b0: H-Z 1'b1: Output	R/W (1)

(1) R/W: The bit or field is readable and writable.

R/(W): The bit or field is readable and writable. However, writing to this bit or field has some limitations. For details on the limitations, see the description or notes of respective registers.

R: The bit or field is readable. Writing to this bit or field has no effect.

W: The bit or field is writable. Reading to this bit or field is not guaranteed.

(2) Reserved. Make sure to use the specified value when writing to this bit or field; otherwise, the correct operation is not guaranteed.

(3) Setting prohibited. The correct operation is not guaranteed if such a setting is performed.

3. List of Abbreviations and Acronyms

Abbreviation	Full Form
AHB	Arm Advanced High-performance Bus
APB	Arm Advanced Peripheral Bus
AXI	Arm Advanced eXtensible Interface
bps	bits per second
CA7	Arm Cortex-A7 module
CM3	Arm Cortex-M3 module
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
Hi-Z	High Impedance
HSR	High-availability Seamless Redundancy
HW-RTOS	Hard Ware Real Time OS
I/O	Input/Output
INTC	Interrupt Controller
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
NoC	Network-on-Chip
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
UART	Universal Asynchronous Receiver/Transmitter
OTP	One Time Programmable
PTP	Precision Time Protocol
PRP	Parallel Redundancy Protocol
SoC	System On Chip

4. Description of the Access Size

Access size:

8 bits = Byte

16 bits = Halfword

32 bits = Word

CAN(Controller Area Network): An automotive network specification developed by Robert Bosch GmbH of Germany.

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Table of Contents

Section 1 General Architecture

1.1 Device Overview

■ On-Chip 32-bit Arm® Cortex®-A7 MPCore

- Up to 500 MHz
- Single or Dual core
- FPU, VFPv4-D16
- MMU
- L1 cache: 16 KB (instruction)/16 KB (data) per core
- L2 cache: up to 256 KB

■ On-Chip 32-bit Arm® Cortex®-M3 Processor

- Up to 125 MHz
- Memory Protection Unit (MPU) supported

■ Low Power Features

- Clock gating management
- Clock frequency scaling

■ On-Chip Extended SRAM

- Up to 6 MB with ECC

■ Data Transfer

- 2 × DMAC with 8 channels each

■ Memory Interfaces

- Up to 2 × Quad SPI/XIP
- NAND Flash with advanced ECC management
- 16-bit DDR interface (DDR2-500/DDR3-1000)
- Up to 2 × SD/SDIO/eMMC

■ IO Multiplexing Controller

- Locations of I/Os for peripherals are selectable from multiple pins

■ Clock Oscillator

- External clock/oscillator input frequency: 40 MHz
- RTC with 32 kHz oscillator

■ Security functions (option)

- Secure Boot/JTAG Lock/64bit Chip-ID

■ Peripherals

- CPU resources
  - Mailbox
  - 2 × Timer block (16bit × 6ch, 32bit × 2ch)
  - 1 × PWMTimer (16bit × 16ch)
  - 1 × Watchdog per CPU
  - Semaphore
- General Connectivity
  - 1 × USB2.0 Host
  - 1 × USB2.0 Host & Function
  - 8 × UART
  - 6 × SPI (4 masters/2 slaves)
  - 2 × I^2C
  - 2 × CAN
  - Up to 2 × 12-bit ADC (up to 1 MSPS)
  - MSEBI (Parallel Bus Interface)
- Other features
  - LCD controller
  - GPIO pins (up to 170)

■ R-IN Engine

- Arm® Cortex®-M3 CPU
- Hardware RTOS accelerator (HW-RTOS)
- Hardware Ethernet accelerator

■ Advanced real-time Ethernet features

- Sercos®*1III Slave Controller
- EtherCAT®*2 3 ports slave controller
- Advanced 5 (4 + 1) Port Switch (A5PSW)
  - Switch 5 ports with QoS and IEEE1588
    ➢ Up to 5 Gbit ports
  - PRP compliant to IEC62439-3 Ed2.0- 2012 (option)
- HSR compliant to IEC62439-3 Ed2.0-2012 (option)
- Up to 2 independent GMAC, IEEE1588
- Up to 5 external ports with MII/RMII/RGMII

Note 1. Sercos is a registered trademark of Sercos International e.V.

Note 2. EtherCAT is registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.

1.2 Outline of Specifications

Table 1.1 Outline of Specifications (1/8)

Classification	Module/Function	Description
CPU	Arm Cortex-A7	• Arm 32-bit CPU Cortex-A7 (Revision r0p5) • Dual core or single core • Maximum operating frequency: 500 MHz • Clock frequency scaling • L1 cache: 16 KB (instruction)/16 KB (data) per core • L2 cache: up to 256 KB • FPU, VFPv4-D16 • MMU • Hardware coherent caches • Little endian
	Arm Cortex-M3	• Arm 32-bit CPU Cortex-M3 (Revision r2p1) • Maximum operating frequency: 125 MHz • Memory Protection Unit (MPU) • Little endian
Memory	On-chip 2MB SRAM	• Capacity: 2 MB (1MB + 1MB) • Separated access ports per 512 KB unit • SEC-DED (Single Error Correction, Double Error Detection)
	On-chip 4MB SRAM	• Capacity: 4 MB • Separated access ports per 1 MB unit • SEC-DED (Single Error Correction, Double Error Detection)
Watchdog		• Free running 12-bit decrementing counters with reload register • Output can be used to activate a system reset or as an interrupt • Stop of watchdog effect while CPU is being stopped by debugger (e.g. by breakpoint execution)
Operating Modes		• Three boot modes (CA7) – NAND Flash – QSPI Flash – USB DFU
Clock	Clock Generation Circuit	• Input 40 MHz clock selectable from an oscillator or crystal • System clock up to 125 MHz • Cortex-A7 clock x1/x2/x4 with system clock • DDR memory clock 250 MHz/500 MHz
RTC		• Time-of-day clock in 24-hour mode • Calendar • Alarm capability • XTAL 32 kHz • Separate and isolated power supply for RTC backup mode
Reset		• Master Reset input • Internal System Reset (Software, watchdog)

Table 1.1 Outline of Specifications (2/8)

Classification	Module/Function	Description
Data Transfer	Direct Memory Access Controller (DMAC)	• 2 units: – 8 channels, 16 request sources for DMAC1 – 8 channels, 16 request sources for DMAC2 • Memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers • Transfer width: – 8, 16, 32, 64 bits • Programmable DMA burst size
Mailbox		• 3x programmable mailboxes – 7× 32-bit data registers per mailbox
Semaphore		• Hardware lock mechanism of internal shared resources
Parallel Bus Interface	Medium Speed External Bus Interface (MSEBI)	• Master and slave modes – Data bus width selectable from 8, 16 and 32 bits • Address/data/control-data are multiplexed on data bus • Burst mode • DMA Support – Master mode: Coupling with 4 DMA channels (external request reception capability) – Slave Mode: External request transmission capability • Up to 4 chip selects • Programmable address capability from 2B to 4GB • Programmable setup and hold time • External wait request
I/O Ports	IO Multiplexing	• Locations of IOs for peripherals are selectable • Output drive strength selectable • On-chip Pull-up/Pull-down select
Memory Interfaces	DDR2/3 Controller	• DDR2-500/DDR3-1000 • Programmable memory data path size: 16 bits, 8 bits, 8+ECC bits • Up to 2 chip selects and 2 ODT • Up to 2 GB address capability • ECC SEC/DED software configurable (enable/disable) • Programmable on die termination • Configurable impedance drive and slew rate • DDR2/DDR3 low power control management (by software) • Port Address Protection Check – Up to 16 address protection regions per port
	NAND Flash Controller	• NAND interface with 8-bit bus width • Support for asynchronous mode • 4 chip selects • Write protection • Programmable address cycle (0/1/2/3/4/5) • Integrated DMA • Support for 256 B, 512 B, 2 KB, 1 KB, 4 KB, 8 KB, 16 KB pages • BCH ECC (Error detection and data correction) – ECC data block size: 256 B, 512 B, 1024 B – ECC correction capability: 2, 4, 8, 16, 24, 32 bits errors • Bad Block Management (BBM)

Table 1.1 Outline of Specifications (3/8)

Classification	Module/Function	Description
Memory Interfaces	Quad SPI (QSPI)	• Up to 2 units • Single, dual or quad I/O instructions supported • Supported read performance enhanced mode (NoCMD mode) • Remap address direct access • Programmable device sizes • Up to 4 chip selects • Support for 1/2/3/4 byte addressing • Support for programmable page size (default 256 bytes) • Support for programmable number of bytes per device block • Programmable write protected regions • Transmit and receive FIFOs are 16 bytes • Legacy mode allowing software direct access to low level transmit and receive FIFOs • Set of control registers to perform any FLASH command • Support for write burst in direct access
	SD/SDIO/eMMC	• Up to 2 units • SD/SDIO Card interface – Transfers data in 1 bit or 4 bits mode – Transfers data in Default or High Speed mode • eMMC interface – Transfers data in 1 bit, 4 bits, or 8 bits mode • Speeds – Default mode up to 25 MHz – High Speed mode up to 50 MHz • Support for PIO/SDMA/ADMA2 transfer
Networking Elements	R-IN Engine	• ITRON-like system calls – 30 system calls for elements such as events, semaphores, and mailboxes • Task Scheduler – Hardware ISR: Maximum 32 selectable from 128 interrupts – Number of context elements: 64 – Number of semaphore identifiers: 128 – Number of event identifiers: 64 – Number of mailbox identifiers: 64 – Number of mailbox elements: 192 – Number of context priority levels: 16 • Hardware function manager • Internal DMA controller • Buffer allocator • Header EnDec • Dedicated Gigabit Ethernet MAC (with built-in MACDMAC)

Table 1.1 Outline of Specifications (4/8)

Classification	Module/Function	Description
Networking Elements	Advanced 5 Port Switch	• Operation modes: – 10 Mbps half- and full-duplex – 100 Mbps half- and full-duplex – 1000 Mbps full-duplex only • MAC based RMON statistics counters/per port • Port statistics on per port basis (no aggregation) • Look-up table up to 8192 MAC addresses (static and learned) • Packet buffer size: 1 Mbit • 4 queues with individual QoS levels, supporting frame priority classification for the flexible handling of output queues – Optional arbitration management through weighted fair queuing • Support for Ethernet multicast and broadcast frames with flooding control to avoid unnecessary duplication of frames • Programmable multicast destination port mask to restrict frame duplication for individual multicast addresses • IEEE 1588-2008 compatible – Support for 1 step Peer-to-Peer (P2P) (Layer 2 only) – Support for 1 step End-to-End (E2E) (Layer 2 only) • Multicast and broadcast resolution with VLAN domain filtering providing a strict separation of up to 32 VLANs • Support for reception and transmission of VLAN frames • Programmable addition, removal and manipulation of ingress and egress VLAN tags, supporting single and double-tagged VLAN frames on each port • Support for standard frame size (1536 bytes), extended frame sizes up to 1700 bytes and jumbo frames up to 10 Kbytes • Port mirroring programmable per port • RSTP port states (3 for RSTP/ 5 for STP) – RSTP Port states learning, discarding, forwarding configurable per port – BPDU frame supported – MSTP BPDU frame supported (software) • Start in Managed mode • Frame snooping engine • Standalone Energy-Efficient-Ethernet (EEE) management • Programmable egress rate limit per port • Ingress Configurable Broadcast storm protection per port • Ingress Configurable Multicast storm protection per port • 802.1X source address authentication supported • 802.1X guest VLAN supported • PRP functionality (IEC 62439-3 edition 2.0- 2012) • DLR module • Cut-through • TDMA (Time Division Multiple Access) 4 time slots • Pattern Matchers 8 channels • Remote monitoring via SNMP and the (RMON/MIB) • Hub function

Table 1.1 Outline of Specifications (5/8)

Classification	Module/Function	Description
Networking Elements	HSR Switch	• HSR functionality (IEC 62439-3 edition 2.0- 2012) – DANH – Redundancy Box (Red Box) – Generation of redundant transmit frames – Filtering of duplicated received frames – Redundancy header generation and detection – Table to keep track of received frames • 100 Mbps full-duplex Ethernet • Dynamic frame buffer allocation (page manager) • 128 proxy nodes (VDANs) supported • Support for link-local protocols • Duplicate detection memory • MAC address filtering • 1× VLAN tag supported • Port statistics on per port basis (no aggregation) • 144 KB frame buffer • IEEE 1588-2008 • Support for Ethernet multicast frames with flooding control • Extended frame size: up to 2000 bytes (Jumbo frames not supported) • Support for a minimum of 16 nodes in an HSR loop • Configurable duplicate detection residence time
	EtherCAT Slave Controller	• Up to 3 ports • Automatic TX Shift • Enhanced Link Detection • 8 FMMU (Fieldbus Memory Management Unit) • 8 SyncManagers • 64-bit Distributed Clocks • Mapping to global IRQ • Read/Write Offset • Write Protection • AL Status Code Register • Extended Watchdog • AL Event Mask Register • Watchdog Counter • SyncManager Event Times • EPU Error Counter • Lost Link Counter • I2C interface for external EEPROM
	SercosIII Slave Controller	• 2 ports • The serial interface operates with 100 Mbaud • Telegram processing for automatic transmission, and monitoring of synchronization telegrams and data telegrams • Switch over function between Sercos protocol and standard Ethernet protocol via multiplexer • Monitors the received data stream to detect the frame type and starts operation when SercosIII frame type is detected • Handling of the data transfers to and from SRAM based on telegram type (MST/MDT or AT)

Table 1.1 Outline of Specifications (6/8)

Classification	Module/Function	Description
Networking Elements	Independent GMAC	• 2× MAC instances (GMAC1, GMAC2) • Compliance with the following standards: – IEEE 1588-2008 v2 standard for precision networked clock synchronization – IEEE 1588-2008 v2 is compliant with Power IEEE C37.238 profile – IEEE 802.3-az-2010 for Energy Efficient Ethernet (EEE) • Support for 10/100/1000 Mbps data transfer rates • Support for both half-duplex and full-duplex operation • Programmable frame length to support both standard and “jumbo” Ethernet frames with size up to 16 Kbytes (16KB-1) • 17 MAC address registers for the address filter block • Variety of flexible addresses filtering modes are supported • Native DMA with simple-independent channels for transmit and receive engines • Advanced IEEE 1588-2002 & 2008 Ethernet frame time-stamping supported • Provides the flexibility to control the Pulse-Per-Second (PPS) output signal (GMAC1 only) • Programmable CRC generation and checking • Support for RMON statistics (L2 layer only) • Station Management Block, MDIO interface
Subsystem Elements	USB2.0 HOST	• 1 dedicated port + 1 configurable port (Host or Function) • Supports: – High speed (HS): 480 Mbps (USB 2.0) – Full speed (FS): 12 Mbps (USB 1.1) – Low speed (LS): 1.5 Mbps (USB 1.1) • USB Plug Detect (UPD) • Output port power switch management • Overcurrent indication from application • Integrated DMA • Transmit and receive FIFOs
	USB2.0 Function	• 1 configurable port (Host or Function) • Supports: – High speed (HS): 480 Mbps (USB 2.0) – Full speed (FS): 12 Mbps (USB 1.1) • USB Plug Detect (UPD) which detects the connection of a host via VBUS • 16 physical endpoints • Integrated DMA • Endpoint buffer
	UART 1, 2, 3	• Compliant with 16550 UART • Separate 16×8 (16 location depth × 8-bit width) transmit and 16×8 receive FIFOs • RS485 & MODBUS® enhanced features • Baud rate generation up to 5.2 Mbaud • Generation and detection of line breaks • Programmable hardware flow control • Auto Flow Control mode as specified in the 16750 standard • Supports TXD, RXD, CTS_N, RTS_N, DTR_N, DSR_N, DCD_N, RI_N
	UART 4, 5, 6, 7, 8	• In addition to UART 1, 2, 3, the following function is available: – DMA coupling with burst-mode management

Table 1.1 Outline of Specifications (7/8)

Classification	Module/Function	Description
Subsystem Elements	SPI 1, 2, 3, 4 (Master)	• Transmit and receive FIFOs (16×16) • Programmable RXD sampling logic • Programmable data-size for frames (from 4 to 16 bits) • 4 chip selects • DMA controller interface
	SPI 5, 6 (Slave)	• Transmit and receive FIFOs (16×16) • Programmable data-size for frames (from 4 to 16 bits) • DMA controller interface
	I^2C 1, 2	• Two speeds: – Standard mode (0 to 100 Kbps) – Fast mode (≤ 400 Kbps) • Separated 8×8 transmit and 8×8 receive FIFOs • Master or slave I2C operation • 7- or 10-bit addressing • 7- or 10-bit combined format transfers • Bulk transmit mode • Programmable SDA hold time ($t_{HD;\,DAT}$)
	CAN 1, 2	• Supports both 11-bit and 29-bit identifiers • Supports bit rates from 125 Kbps to 1 Mbps • Acceptance filtering • Software-driven bit-rate detection (offering hot plug-in support) • Single-shot transmission option, listen-only mode, reception of ‘own’ messages • Arbitration lost interrupt with data of bit position • Read/write error counters • Last error register • Programmable error limit warning • Transmit periodic “Sync frame” • Programmable time base
	General Purpose Timers(Timer)	• 2 units, each supporting: – 6 programmable 16-bit timers – 2 programmable 32-bit timers • Prescaler selectable between 2 time bases • Auto-reload mode or single-shot mode • DMA coupling (only for the 32-bit timers)
	PWMTimer	• 6 inputs for capture and clock: – Bounce filter – 40 external inputs • 16 outputs for compare match: – 20 external outputs • 16 basic 16-bit counters: – Capture and compare functions – 32-bit cascaded counter – Two clock prescalers 10 bit – Synchronized with other counters

Table 1.1 Outline of Specifications (8/8)

Classification	Module/Function	Description
ADC	ADC	• Up to 2units • Resolution 12 bits • Sampling rate from 0.0625 MSPS to 1 MSPS • Analog inputs – 8 channels: (5ch + 3ch S/H) • Individual trigger per channel • DNL, ± 1.0 LSB (Max.) [at VAIN = 0.0 V to AVDD, f_{CLK} = 20 MHz] • INL, ± 4.0 LSB (Max.) [at VAIN = 0.0 V to AVDD, f_{CLK} = 20 MHz] • Power-down mode • Two level of priority • Round-robin management of simultaneous conversion requests with the same level of priority • DMA coupling • Virtual channel capability
Multimedia	LCD Controller	• Programmable LCD Panel resolutions • Interface for 1 Port TFT LCD Panel: – 18-bit digital (6 bits/color) – 24-bit digital (8 bits/color) • Programmable frame buffer bits per pixel (bpp) – 1, 2, 4, 8 bpp mapped through Color Palette to 18-bit LCD pixel – 16, 18, bpp directly drive 18-bit LCD pixel – 24 bpp directly drive 24-bit LCD pixel • Hardware blink supported • Pulse Width Modulation module for LCD panel LED backlight brightness control • Power up and down sequencing supported • Integrated DMA
Security		• Checks the signature of the Secure Boot program • Disable the JTAG I/F debugging function • 64bit Chip-ID which can be read by Cortex-A7
Debugging Interface		• ETM coupled with JTAG debugger • Single Embedded Trace Buffer (32 KB) shared by Cortex-A7 and Cortex-M3 cores • Arm JTAG • Arm SWD
Power Supply Voltage		• Core Voltage: 1.15 V ± 0.05 V • IO voltage: 3.3 V ± 0.3 V • DDR IO voltage: 1.8 V ± 0.1 V; 1.5 V ± 0.075 V
Operating Temperature		Junction temperature: −40°C to +110°C
Packages		• RZ/N1D: – 400LFBGA, 17×17 mm, 0.8 mm pitch – 324LFBGA, 15×15 mm, 0.8 mm pitch • RZ/N1S – 324LFBGA, 15×15 mm, 0.8 mm pitch – 196LFBGA, 12×12 mm, 0.8 mm pitch • RZ/N1L – 196LFBGA, 12×12 mm, 0.8 mm pitch

1.3 Function Comparison per Device Family and Package

Table 1.2 Renesas CPU Subsystem Part Description

Hardware Features		RZ/N1D		RZ/N1S		RZ/N1L
	Package Type:	400BGA	324BGA	324BGA	196BGA	196BGA
Processor Unit	Arm Cortex-A7	Dual		Single		—
	Arm Cortex-M3	Available				
Memory Unit	2 MB with ECC	Available				
	4 MB with ECC	—		Available		
	DDR Memory Controller	Available*1		—		
	Quad SPI	1ch		2ch	1ch*2	
	SDIO/SD/eMMC	2ch				
	NAND Flash	Available				
Networking elements	R-IN Engine & HWRTOS	Available*5				
	Ethernet Port	5 ports	3 ports*3	5 ports	3 ports*3	
	Independent GMAC	Up to 2	N/A*4	Up to 2	Up to 1*4	
	EtherCAT Slave Controller	Available*6 *7				
	SercosIII Slave Controller	Available*6 *7				
	Advanced 5port Switch	5 ports (4 + 1)	4 ports (3 + 1)	5 ports (4 + 1)	3 ports (2 + 1)*7	
	PRP	Optional	—	Available	—	
	HSR Switch*5 *6	Optional	—			
Peripheral Group	ADC	2unit	1unit			
	RTC	Available				N/A
	DMAC	2ch				
	UART	8ch				
	I^2C	2ch				
	Parallel bus Master & Slave*8	Available				Slave only
	USB Host & Function	Available				
	Mailbox	Available				N/A
	Watchdog for CA7	Available, 2		Available, 1		N/A
	Watchdog for CM3	Available				
	SPI Master	4ch				
	SPI Slave	2ch				
	CAN	2ch				
	LCDC	Available			N/A	
	Semaphore	Available				
	Timer block	2unit				
	PWMTimer	Available				
GPIO pin*9		170	132	160	95	95
Security functions*10		Optional				—

Note 1. RZ/N1D-324 has 1 Chip Select and 1 ODT.

Note 2. RZ/N1S-196 and RZ/N1L have up to 2 chip selects.

Note 3. Please refer to Restriction of Ethernet Interface Modes chapter for more details about N/A port numbers.

Note 4. GMAC2 is available via A5PSW in RZ/N1D-324, RZ/N1S-196 and RZ/N1L.

Note 5. HW-RTOS and HSR are not available simultaneously.

Note 6. SERCOSIII, ETHERCAT and HSR function are not available simultaneously.

Note 7. A5PSW, SERCOSIII and ETHERCAT function are not available simultaneously in RZ/N1S-196 and RZ/N1L.

Note 8. RZ/N1D-324 is not able to use 32-bit mode. RZ/N1S-196 and RZ/N1L are only able to use 8-bit mode and 2 external wait requests. RZ/N1S-196 is only able to use ALE serial mode in Master.

Note 9. Shared with peripheral signals.

Note 10. Please contact our sales office for information regarding the optional security functions.

1.4 List of Products

Table 1.3 List of Products

Name	P/N	Package(s)	Main CPU	PRP/HSR	Security
RZ/N1D	R9A06G032VGBG	400BGA	Dual Cortex-A7	—	—
	R9A06G032EGBG				Available
	R9A06G032VGBA	324BGA			—
	R9A06G032EGBA				Available
	R9A06G032NGBG	400BGA		PRP/HSR	—
	R9A06G032PGBG				Available
RZ/N1S	R9A06G033VGBA	196BGA	Single Cortex-A7	—	—
	R9A06G033EGBA				Available
	R9A06G033NGBG	324BGA		PRP	—
	R9A06G033PGBG				Available
RZ/N1L	R9A06G034VGBA	196BGA	Cortex-M3	—	—

1.5 Block Diagram

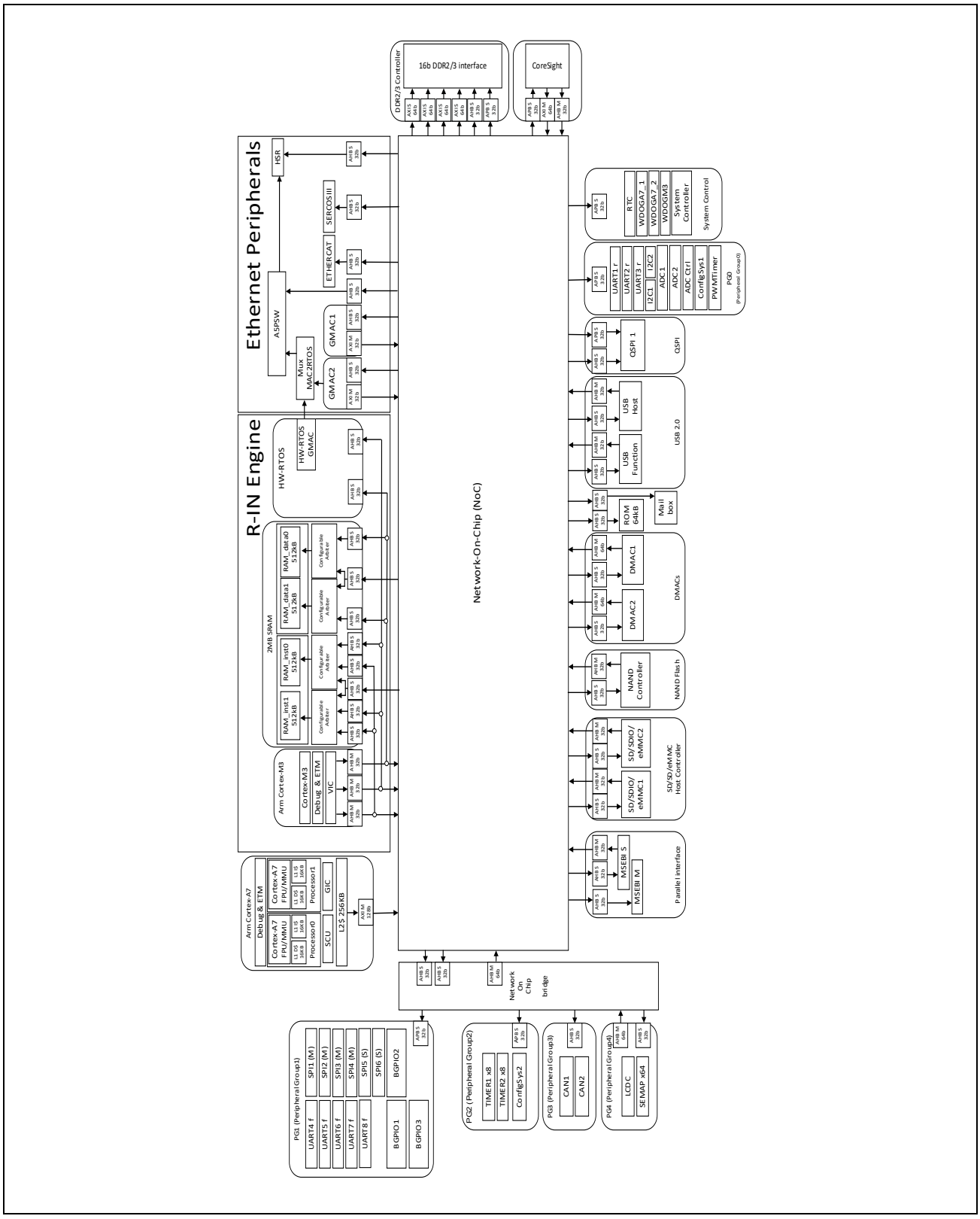


Figure 1.1 RZ/N1D Dual Cortex-A7 & Cortex-M3

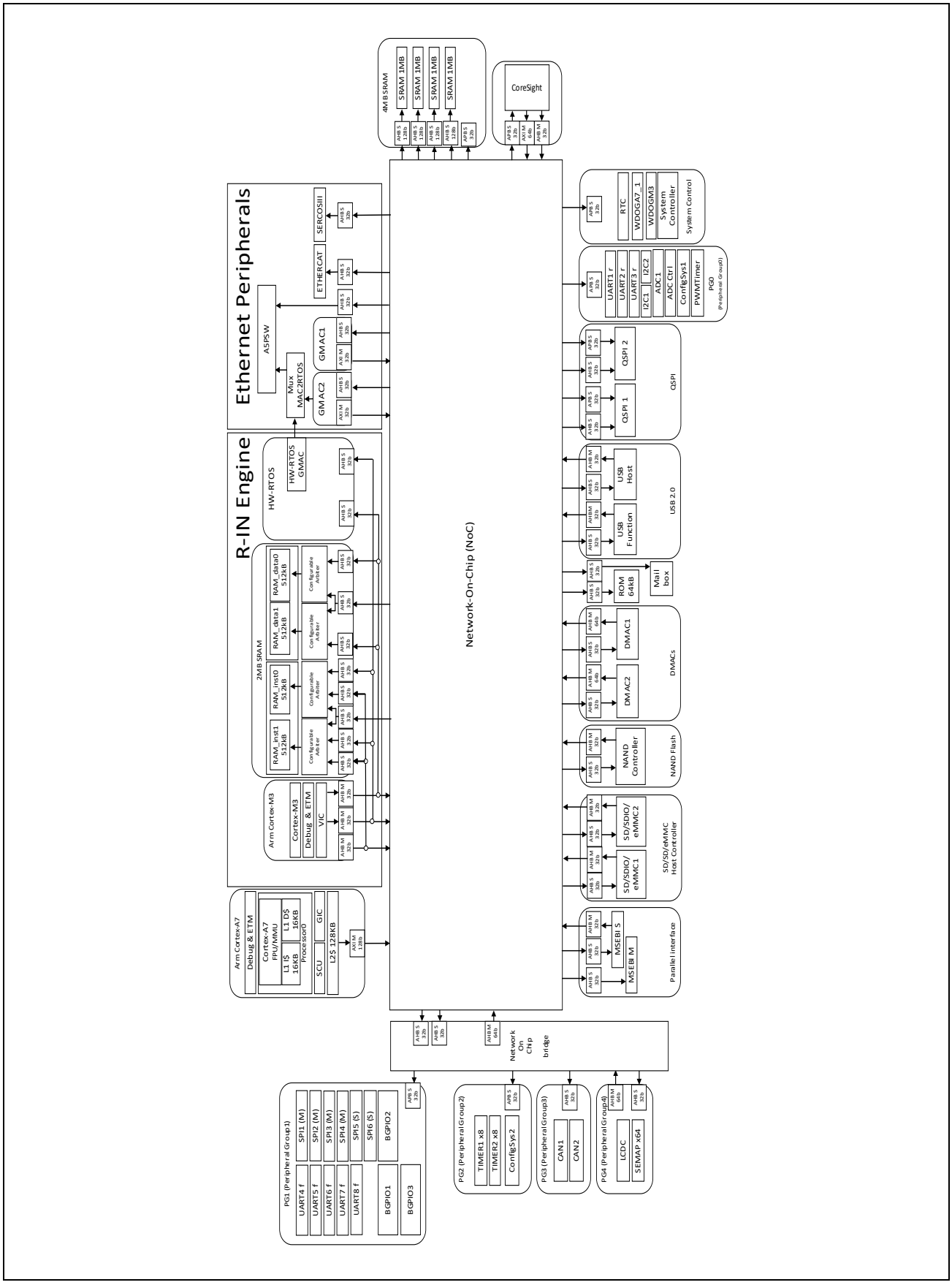


Figure 1.2 RZ/N1S Single Cortex-A7 & Cortex-M3

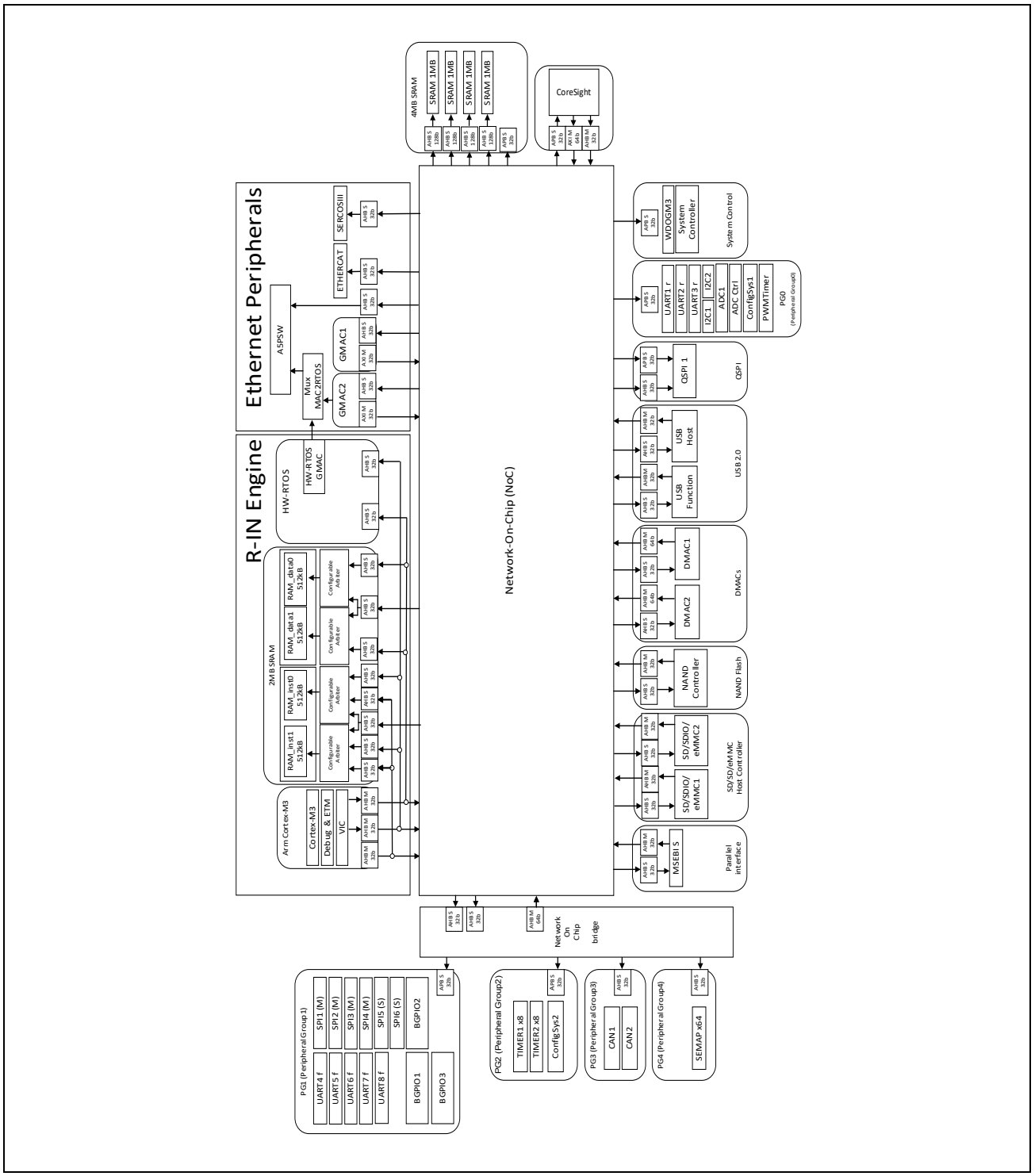


Figure 1.3 RZ/N1L Cortex-M3

Section 2 Address Space

2.1 Memory Map

2.1.1 RZ/N1D

The figure below provides an overview of the memory map as seen by Arm Cortex-A7.

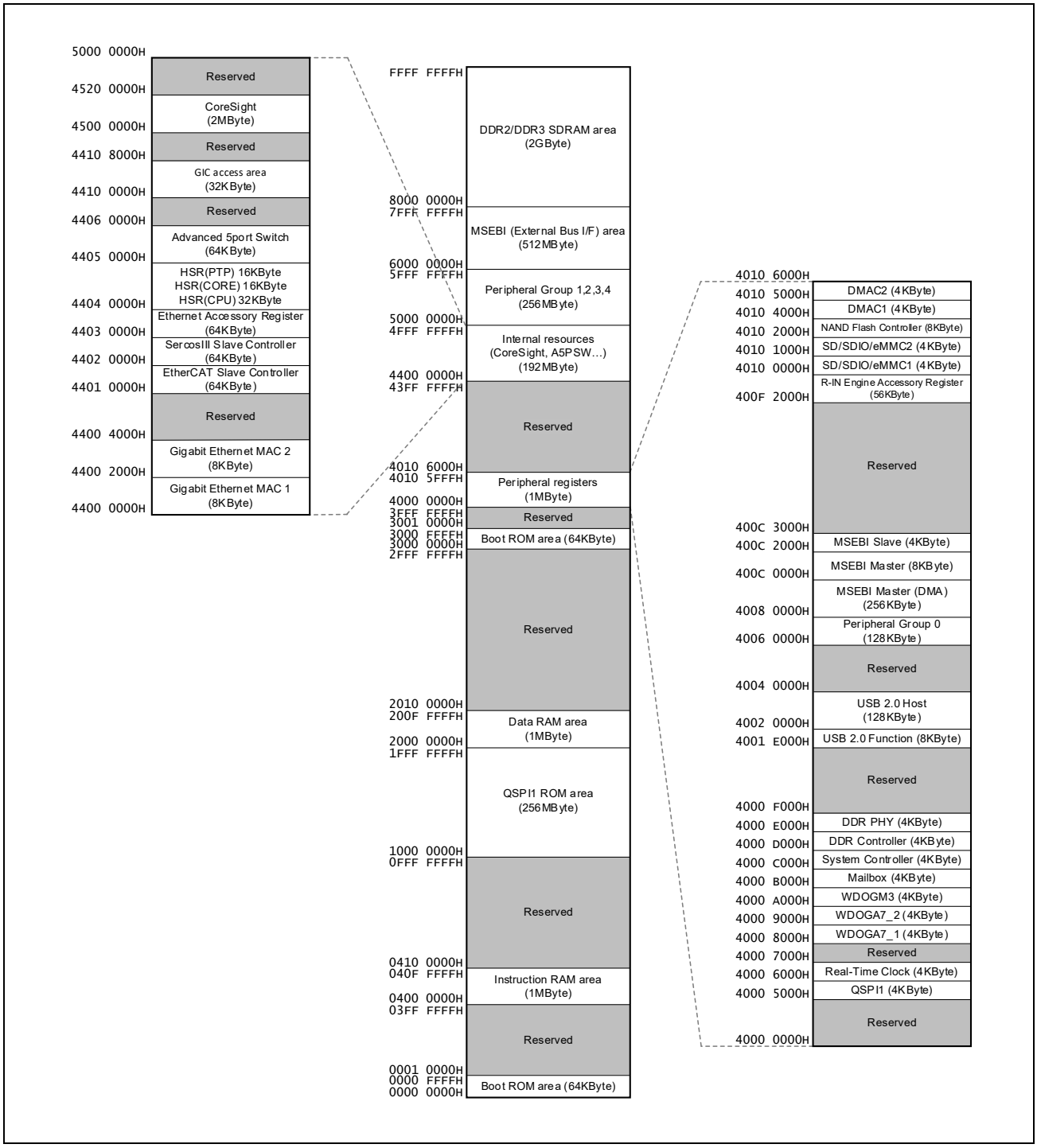


Figure 2.1 Memory Map of RZ/N1D (Cortex-A7)

The figure below provides an overview of the memory map as seen by Arm Cortex-M3.

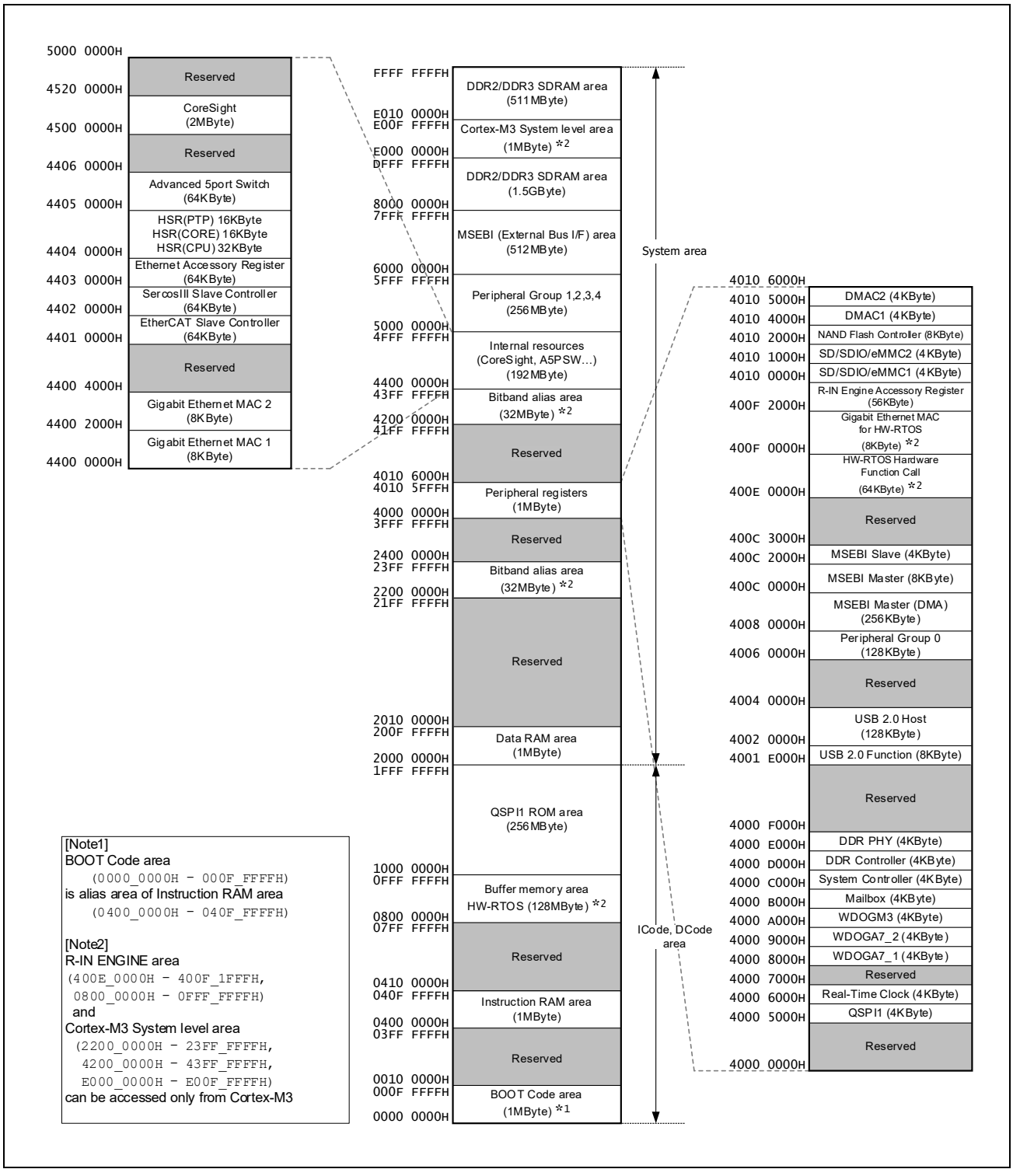


Figure 2.2 Memory Map of RZ/N1D (Cortex-M3)

2.1.2 RZ/N1S

The figure below provides an overview of the memory map as seen by Arm Cortex-A7.

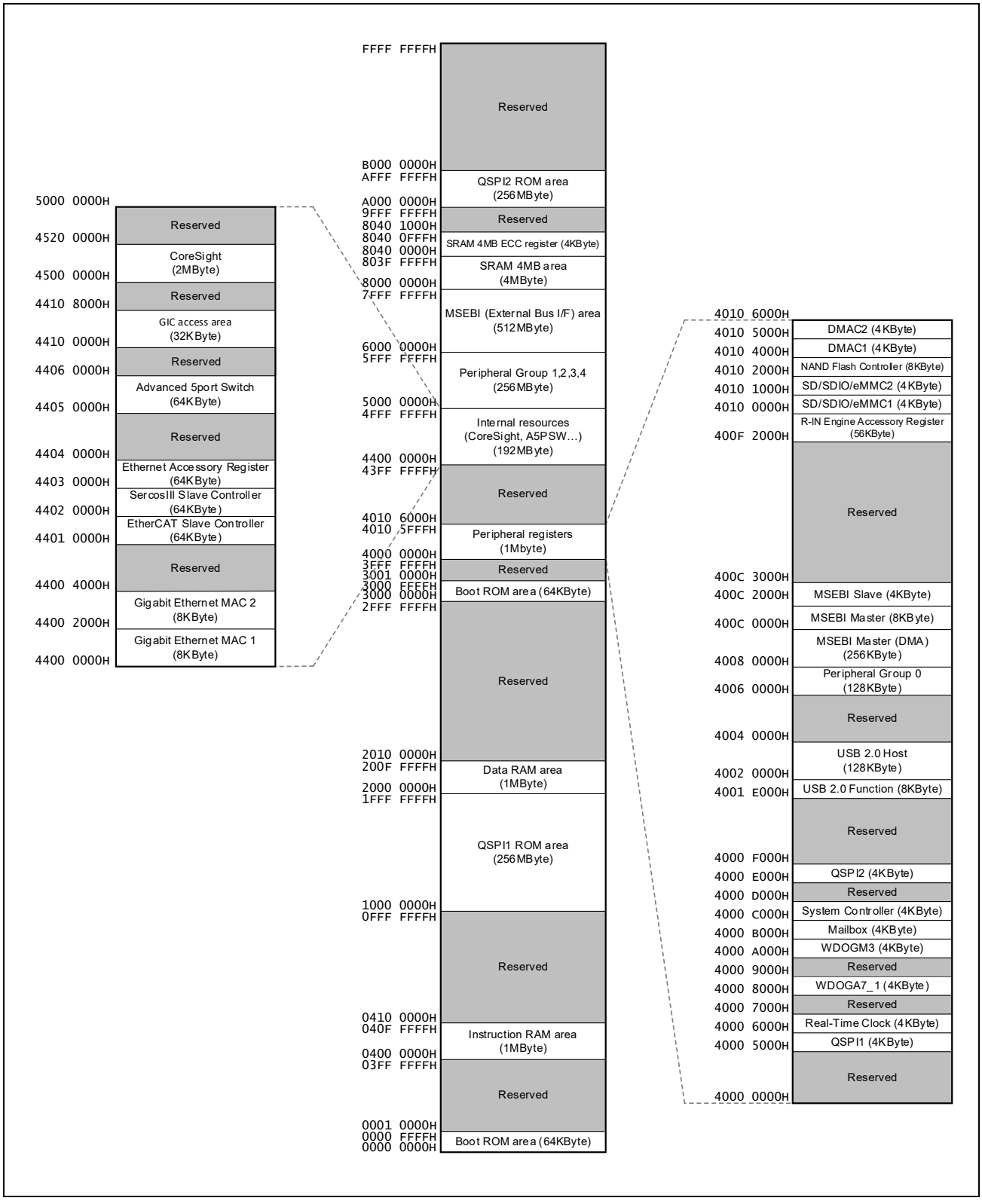


Figure 2.3 Memory Map of RZ/N1S (Cortex-A7)

The figure below provides an overview of the memory map as seen by Arm Cortex-M3.

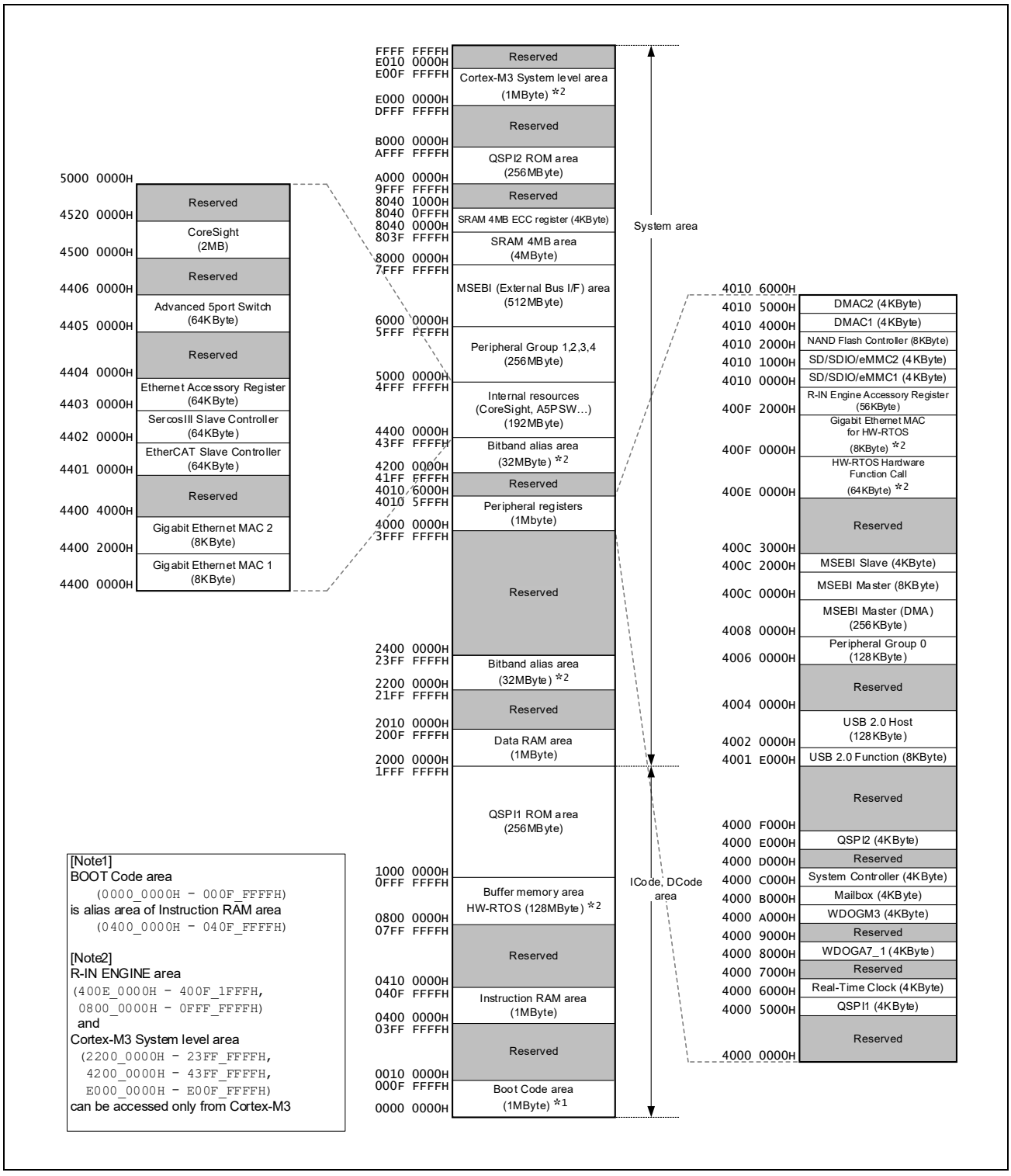


Figure 2.4 Memory Map of RZ/N1S (Cortex-M3)

2.1.3 RZ/N1L

The figure below provides an overview of the memory map as seen by Arm Cortex-M3.

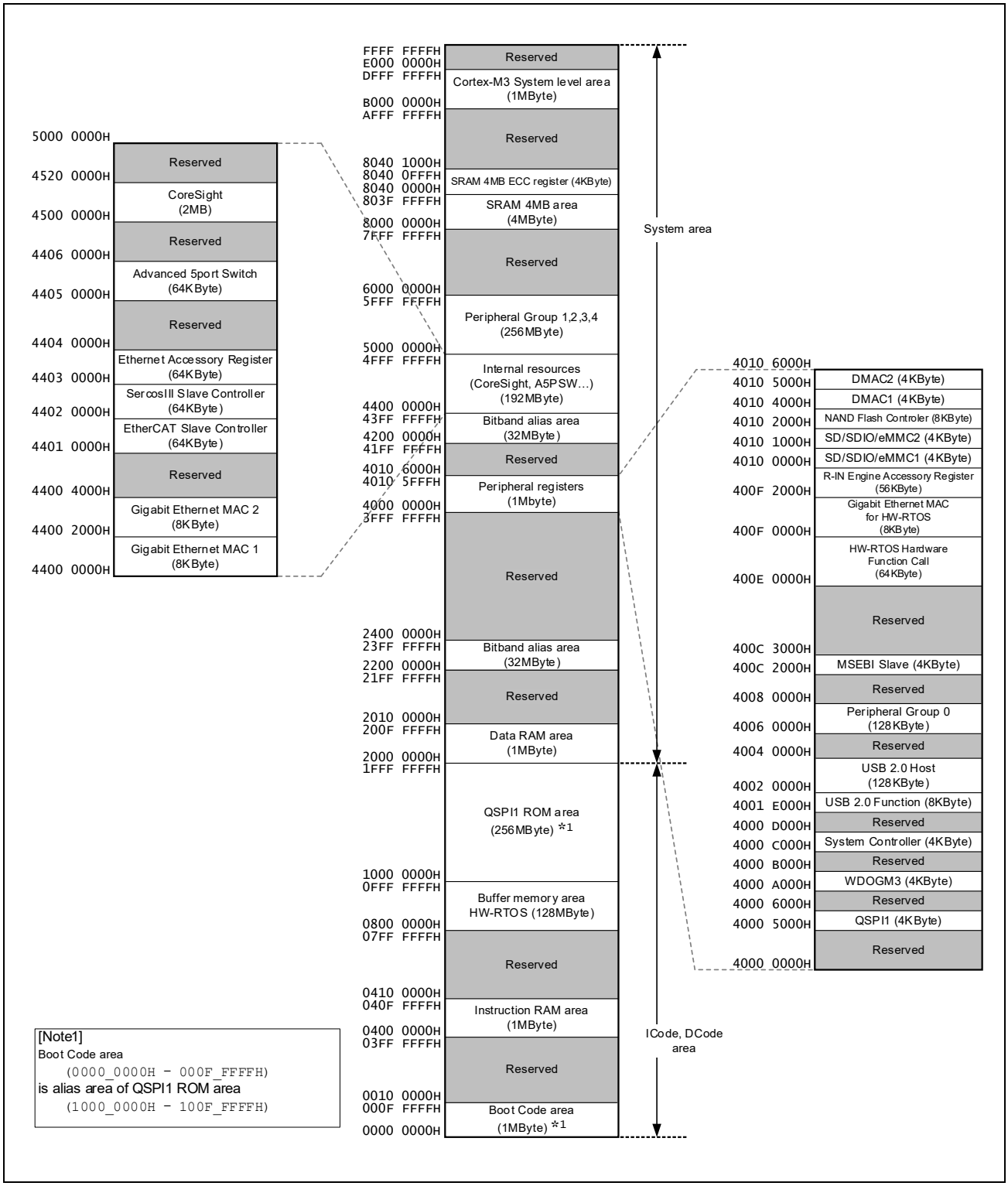


Figure 2.5 Memory Map of RZ/N1L

2.2 Register Map Summary

Following Register map covers base address of peripheral module in all RZ/N1 groups. The unchecked modules should not be accessed.

Table 2.1 Register Map (1/2)

Start Address	Peripheral Module	RZ/N1D-400	RZ/N1D-324	RZ/N1S-324	RZ/N1S-196	RZ/N1L
4000_5000	Quad SPI Controller1 (QSPI1)	✓	✓	✓	✓	✓
4000_6000	Real-Time Clock (RTC)	✓	✓	✓	✓	N/A
4000_8000	Watchdog for CA7 processor0 (WDOGA7_1)	✓	✓	✓	✓	N/A
4000_9000	Watchdog for CA7 processor1 (WDOGA7_2)	✓	✓	N/A	N/A	N/A
4000_A000	Watchdog for CM3 (WDOGCM3)	✓	✓	✓	✓	✓
4000_B000	Mailbox (IPCM)	✓	✓	✓	✓	N/A
4000_C000	System Controller	✓	✓	✓	✓	✓
4000_D000	DDR2/3 Controller	✓	✓	—	—	—
4000_E000	DDR2/3 PHY	✓	✓	—	—	—
	Quad SPI Controller2 (QSPI2)	—	—	✓	N/A	N/A
4001_E000	USB 2.0 HS Function Controller (USBf) / EPC	✓	✓	✓	✓	✓
4001_F000	USB 2.0 HS Function Controller (USBf) / AHB-EPC Bridge	✓	✓	✓	✓	✓
4002_0000	USB 2.0 HS Host Controller (USBh) / OHCI Operation	✓	✓	✓	✓	✓
4002_1000	USB 2.0 HS Host Controller (USBh) / EHCI Operation	✓	✓	✓	✓	✓
4003_0000	USB 2.0 HS Host Controller (USBh) / AHB PCI Bridge (PCI Config. Space)	✓	✓	✓	✓	✓
4003_0000	USB 2.0 HS Host Controller (USBh) / OHCI (PCI Config. Space)	✓	✓	✓	✓	✓
4003_0100	USB 2.0 HS Host Controller (USBh) / EHCI (PCI Config. Space)	✓	✓	✓	✓	✓
4003_0800	USB 2.0 HS Host Controller (USBh) / AHB PCI Bridge (PCI Com. Space)	✓	✓	✓	✓	✓
4006_0000	UART1	✓	✓	✓	✓	✓
4006_1000	UART2	✓	✓	✓	✓	✓
4006_2000	UART3	✓	✓	✓	✓	✓
4006_3000	I2C1	✓	✓	✓	✓	✓
4006_4000	I2C2	✓	✓	✓	✓	✓
4006_5000	ADC Controller / 12bit A/D Converters	✓	✓	✓	✓	✓
4006_7000	ConfigSys1	✓	✓	✓	✓	✓
4006_8000	PWMTimer	✓	✓	✓	✓	✓
4008_0000	Medium Speed External Bus Interface / Master (MSEBIM) From DMA	✓	✓	✓	✓	N/A
400C_0000	Medium Speed External Bus Interface / Master (MSEBIM) From CPU	✓	✓	✓	✓	N/A
400C_1000	Medium Speed External Bus Interface / Slave (MSEBIS) From MSEBI	✓	✓	✓	✓	✓
400C_2000	Medium Speed External Bus Interface / Slave (MSEBIS) From CPU	✓	✓	✓	✓	✓
400E_0000	HW-RTOS Hardware Function Call	✓	✓	✓	✓	✓
400F_0000	Gigabit Ethernet MAC for HW-RTOS (HW-RTOS GMAC)	✓	✓	✓	✓	✓
400F_2000	R-IN Engine Accessory Register	✓	✓	✓	✓	✓
4010_0000	SD/SDIO/eMMC Controller1 (SDIO1)	✓	✓	✓	✓	✓
4010_1000	SD/SDIO/eMMC Controller2 (SDIO2)	✓	✓	✓	✓	✓
4010_2000	NAND Flash Controller	✓	✓	✓	✓	✓
4010_4000	DMAC1	✓	✓	✓	✓	✓
4010_5000	DMAC2	✓	✓	✓	✓	✓

Table 2.1 Register Map (2/2)

Start Address	Peripheral Module	RZ/N1D-400	RZ/N1D-324	RZ/N1S-324	RZ/N1S-196	RZ/N1L
4400_0000	Gigabit Ethernet MAC1 (GMAC1)	✓	N/A	✓	✓	✓
4400_2000	Gigabit Ethernet MAC2 (GMAC2)	✓	✓	✓	✓	✓
4401_0000	EtherCAT Slave Controller (ETHERCAT)	✓	✓	✓	✓	✓
4402_0000	SercosIII Slave Controller (SERCOSIII)	✓	✓	✓	✓	✓
4403_0000	Ethernet Accessory Register	✓	✓	✓	✓	✓
4404_0000	HSR Switch / CPU	*1	—	—	—	—
4404_8000	HSR Switch / CORE	*1	—	—	—	—
4404_C000	HSR Switch / PTP	*1	—	—	—	—
4405_0000	Advanced 5port Switch (A5PSW)	✓	✓	✓	✓	✓
5000_0000	UART4	✓	✓	✓	✓	✓
5000_1000	UART5	✓	✓	✓	✓	✓
5000_2000	UART6	✓	✓	✓	✓	✓
5000_3000	UART7	✓	✓	✓	✓	✓
5000_4000	UART8	✓	✓	✓	✓	✓
5000_5000	SPI1 (Master)	✓	✓	✓	✓	✓
5000_6000	SPI2 (Master)	✓	✓	✓	✓	✓
5000_7000	SPI3 (Master)	✓	✓	✓	✓	✓
5000_8000	SPI4 (Master)	✓	✓	✓	✓	✓
5000_9000	SPI5 (Slave)	✓	✓	✓	✓	✓
5000_A000	SPI6 (Slave)	✓	✓	✓	✓	✓
5000_B000	BGPIO1	✓	✓	✓	✓	✓
5000_C000	BGPIO2	✓	✓	✓	✓	✓
5000_D000	BGPIO3	✓	✓	✓	N/A	N/A
5100_0000	ConfigSys2	✓	✓	✓	✓	✓
5100_1000	Timer Block1 (TIMER1)	✓	✓	✓	✓	✓
5100_2000	Timer Block2 (TIMER2)	✓	✓	✓	✓	✓
5210_4000	CAN1	✓	✓	✓	✓	✓
5210_5000	CAN2	✓	✓	✓	✓	✓
5300_0000	Semaphore (SEMAP)	✓	✓	✓	✓	✓
5300_4000	LCD Controller (LCDC)	✓	✓	✓	N/A	N/A

Note 1. HSR is optional.

Section 3 Clock Generation

3.1 Overview

RZ/N1 has 3 clock sources, 1 reference clock inputs for RGMII, and 2 reference clock outputs for RMII/MII.

System controller includes registers for RZ/N1 Clock Controller. This allows the power management software to have fully flexible control over the implemented clock gating, clock multiplexing and clock division features.

Table 3.1 Specification of Clock Generation

Item	Specifications
Main clock oscillator	Resonator frequency: 40 MHz
	External clock input frequency: 40 MHz
	Main clock source for this system. External clock input mode is also available.
RTC clock oscillator	Resonator frequency: 32.768 kHz
	RTC clock source. It belongs to RTC dedicated power domain.
External clock input for JTAG (JTAG_TCK)	Input frequency: 10 MHz (max) for JTAG
	Clock for CoreSight® and JTAG controller.
PLL	Input clock source: Main clock oscillator
	Output clock frequency: 1000 MHz
	Main PLL for this system
USBPLL	Input clock source: Main clock oscillator
	Output clock frequency: 480 MHz
	PLL for USBPHY. 48 MHz, 1/10 of 480 MHz, is provided to system. Default in power down mode.
External clock input for RGMII (RGMII_REFCLK)	Input frequency: 125 MHz
	Clock for RGMII output signals. Internally generated 125 MHz is also available for RGMII
External clock output for RMII (RMII_REFCLK)	Output frequency: 50 MHz
	Clock supply for external RMII interface
External clock output for MII (MII_REFCLK)	Output frequency: 25 MHz
	Clock supply for external MII interface

A Figure in next page shows abstract clock system of RZ/N1.

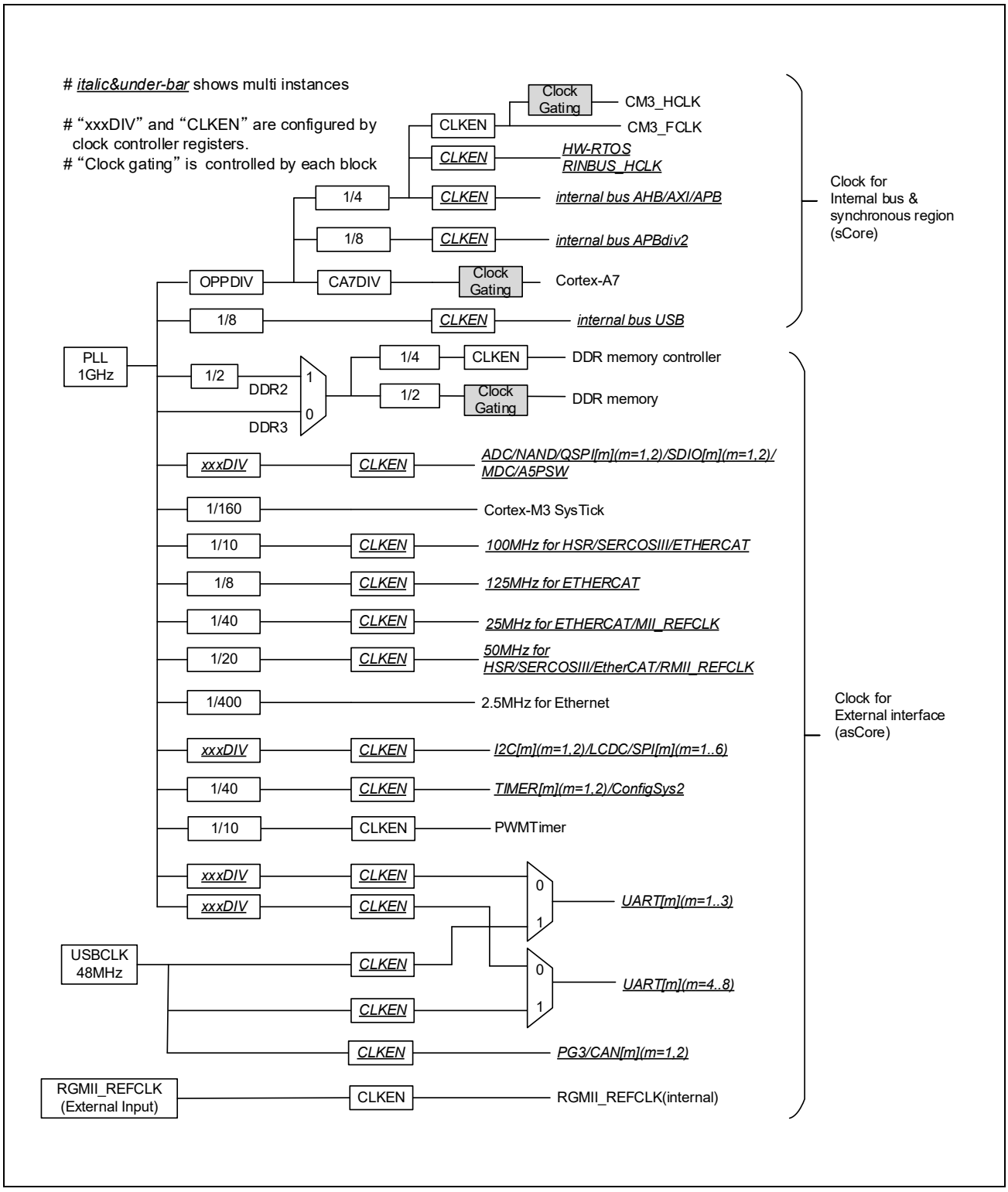


Figure 3.1 Block Diagram of Clock Generation

3.2 Clock Gating

"PWRCTRL_*" registers contain clock gate control bits, "CLKEN_*". There is no special logic in place for the clock gate control signals, all signals are directly feed through the Core block and driven by register bits.

Clock gating of a functioning module may result in system hang up or unpredictable behavior. It is the power management software's responsibility to ensure that no clocks are gated before the corresponding peripheral is disconnected from interconnect.

CAUTION

- RZ/N1 uses the clock provided by USBPLL. The software shall ensure that prior to any access towards USB clocked domain the USBPLL shall be locked. Otherwise the system may hang.
- The software shall not apply clock gating or software reset to any module unless all corresponding ports of the module are disconnected (SCON = 1'b0) and in idle (MISTAT = 1'b1).

3.3 Clock Multiplexing

RZ/N1 Clock Controller has programmable clock multiplexers for each UART. Those multiplexers can be configured by PWRCTRL_PG0_0 and PWRCTRL_PG1_PR2 registers in System Controller Registers.

CAUTION

RZ/N1 uses the clock provided by USBPLL. The software shall ensure that prior to any access towards USB clocked domain the USBPLL shall be locked. Otherwise the system may hang.

3.4 Clock Division

RZ/N1 clock controller has programmable clock dividers. Software may or may not gate the corresponding clocks prior to reprogramming of the dividers. The clock dividers implement a full hardware handshake between System Controller and the clock divider.

CAUTION

The software shall not initiate writes to the control registers of programmable dividers unless the busy flag in the corresponding register is de-asserted.

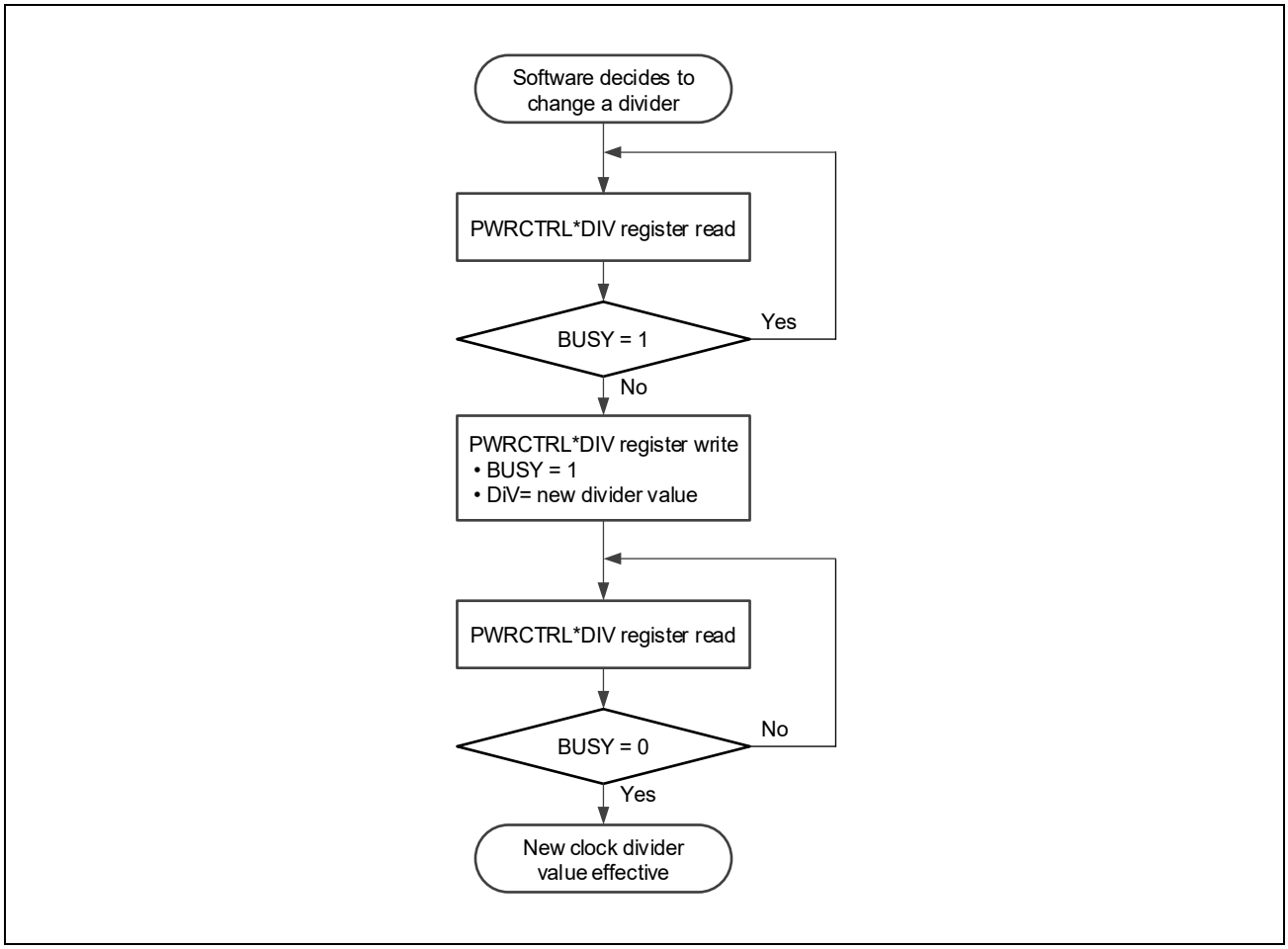


Figure 3.1 Programming Sequence for Programmable Dividers

3.5 Clock Frequency Scaling

RZ/N1 Clock Controller provides two dedicated clock dividers to enable low power operation. One divider is to scale the Cortex-A7 CPU clock by PWRCTRL_CA7DIV register, the other divider is to scale the main NoC interconnect frequency by PWRCTRL_OPPDIV register. The power management software has full control over these dividers and it is in charge of making any decision based on the actual circumstances to scale the clock frequency.

CAUTION

Scaling the frequency of the interconnect scales the frequency of the Watchdog timers.

Following the table shows available clock frequency scaling and use cases. The circuit of each module is classified depending on whether the clock is synchronized with NoC. For each clock, please refer to "**Figure 3.1, Block Diagram of Clock Generation**" and "**Appendix C, Clock Tree Structure**".

- sCore: Circuit which is synchronous to NoC (Clock for AXI/AHB/APB)
- asCore: Circuit which is asynchronous to NoC

Table 3.2 Frequency Mode (1/3)

Function List		125 MHz Mode (Default)	62.5 MHz Mode	31.25 MHz Mode	15.625 MHz Mode
General System – synchronous to NoC					
Network-on-Chip		125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
DMAC		125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
System Control block (RTC, Watchdog, …)		62.5 MHz	31.25 MHz	15.625 MHz	7.8125 MHz
CPU & R-IN Engine – synchronous to NoC					
Cortex-A7	sCore	500 MHz (4×) 250 MHz (2×) (Default) 125 MHz (1×)	250 MHz (4×) 125 MHz (2×) 62.5 MHz (1×)	125 MHz (4×) 62.5 MHz (2×) 31.25 MHz (1×)	62.5 MHz (4×) 31.25 MHz (2×) 15.625 MHz (1×)
Cortex-M3	sCore	125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
HW-RTOS	sCore	125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
Memory Unit					
DDR3-1000	asCore	250 MHz	250 MHz	250 MHz	250 MHz
	Memory Clk	500 MHz	500 MHz	500 MHz	500 MHz
DDR2-500	asCore	125 MHz	125 MHz	125 MHz	125 MHz
	Memory Clk	250 MHz	250 MHz	250 MHz	250 MHz
SRAM 2MB & 4MB	sCore	125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
NAND Flash Controller	sCore	125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
	asCore	Up to 83.33 MHz	←	←	←
QSPI	sCore	125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
	asCore	Up to 250 MHz*1	←	←	←
SD/SDIO/eMMC	sCore	125 MHz	62.5 MHz	31.25 MHz	Not available
	asCore	Up to 50 MHz	←	←	
Networking element & USB					
USB Host & Function	asCore	125 MHz	125 MHz	125 MHz	Not available
	USBCLK out	48 MHz	←	←	

Table 3.2 Frequency Mode (2/3)

Function List		125 MHz Mode (Default)	62.5 MHz Mode	31.25 MHz Mode	15.625 MHz Mode
GMAC	sCore	125 MHz	62.5 MHz	31.25 MHz	Not available
	PTP	125 MHz or 25 MHz	←	←	
	Ether mode*3	GMII/RMII/MII	RMII/MII	RMII/MII	
Advanced 5 Port Switch/PRP	sCore	125 MHz	62.5 MHz	31.25 MHz	Not available
	asCore	200 MHz	←	←	
	Ether mode*3	GMII/RMII/MII 5ports	RMII/MII 5ports	RMII/MII 3ports	
SERCOSIII	asCore	100 MHz	100 MHz	100 MHz	Not available
	Ether mode*3	MII/RMII	MII/RMII	MII/RMII	
ETHERCAT	asCore	125 MHz	125 MHz	125 MHz	Not available
	Ether mode*3	MII/RMII	MII/RMII	MII/RMII	
HSR	asCore	100 MHz	100 MHz	Not available	Not available
RGMII/RMII Converter	Ether mode*3	RGMII/RMII/MII	RMII/MII	RMII/MII	RMII/MII
Peripheral					
	2 clock sources are available for UARTs 1) PLL via divider, up to 83.33 MHz 2) USBPLL, fixed to 48 MHz				
UART 1..3	sCore	62.5 MHz	31.25 MHz	15.625 MHz	7.8125 MHz
	asCore	Up to 83.33 MHz or 48 MHz	←	←	←
UART 4..8	sCore	125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
	asCore	Up to 83.33 MHz or 48 MHz	←	←	←
SPI config1	sCore	125 MHz	Not available	Not available	Not available
	asCore	Up to 125 MHz			
SPI config2	sCore	125 MHz	62.5 MHz	Not available	Not available
	asCore	Up to 62.5 MHz	←		
SPI config3	sCore	125 MHz	62.5 MHz	31.25 MHz	Not available
	asCore	Up to 31.25 MHz	←	←	
SPI config4	sCore	125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
	asCore	Up to 15.625 MHz	←	←	←
I^2C	sCore	62.5 MHz	31.25 MHz	15.625 MHz	7.8125 MHz
	asCore	Up to 83.33 MHz*2	←	←	←
MSEBI	sCore	125 MHz	62.5 MHz	31.25 MHz	Not available
CAN	asCore	48 MHz	←	←	←
BGPIO	sCore	125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
ADC	sCore	62.5 MHz	31.25 MHz	15.625 MHz	7.8125 MHz
	asCore	Up to 20 MHz	←	←	←
TIMER	asCore	25 MHz	←	←	←
PWMTimer	asCore	100 MHz	←	←	Not available
Semaphore	sCore	125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
Mailbox	sCore	125 MHz	62.5 MHz	31.25 MHz	15.625 MHz
LCDC (Config1)	sCore	125 MHz	Not available	Not available	Not available
	asCore	Up to 83.33 MHz			
LCDC (Config2)	sCore	125 MHz	62.5 MHz	Not available	Not available
	asCore	Up to 62.5 MHz	Less than 62.5 MHz		

Table 3.2 Frequency Mode (3/3)

Function List		125 MHz Mode (Default)	62.5 MHz Mode	31.25 MHz Mode	15.625 MHz Mode
LCDC (Config3)	sCore	125 MHz	62.5 MHz	31.25 MHz	Not available
	asCore	Up to 31.25 MHz	←	Less than 31.25 MHz	

Note 1. QSPI asCore must be faster than sCore.

Note 2. I2C asCore must be faster than or equal to sCore.

Note 3. Available RGMII/RMII converter mode

3.6 Clock Oscillator Connection

3.6.1 Main Clock Oscillator

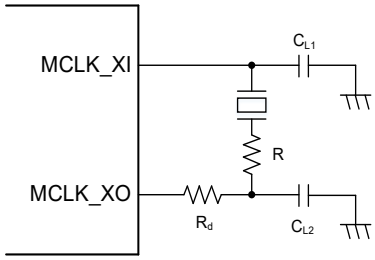
There are two ways of supplying the clock signal to the main clock oscillator: connecting an oscillator or the input of an external clock signal. The clock input mode is set based on the status of the THMODE pin.

Table 3.3 Clock Input Mode Selected for THMODE

THMODE	Clock Input Mode
Low	Oscillator Mode
High	External clock Mode

3.6.1.1 Connected a Crystal Resonator

The following figure shows an example of connecting a crystal resonator.



Note: The values for C_{L1}, C_{L2}, R and R_d should be determined after consultation with the crystal resonator manufacturer.

Figure 3.2 Example of Crystal Resonator Connection (Main Clock)

3.6.1.2 External Clock Input

The following figure shows an example of connection of external clock input. The MCLK_XI pin is tied-down to ground.

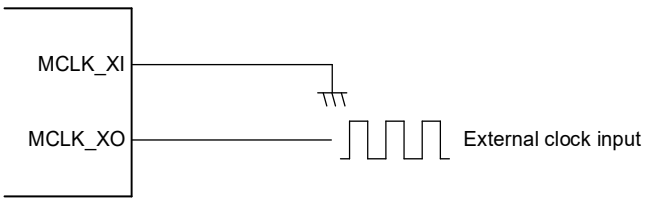


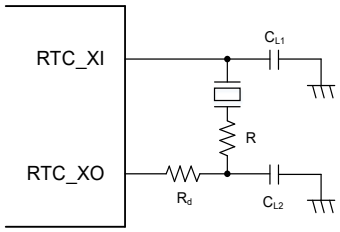
Figure 3.3 Example of External Clock Connection

3.6.2 RTC Clock Oscillator

RTC clock supports oscillator mode only.

3.6.2.1 Connected a Crystal Resonator

The following figure shows an example of connecting a crystal resonator.



Note: The values for C_{L1}, C_{L2}, R and R_d should be determined after consultation with the crystal resonator manufacturer.

Figure 3.4 Example of Crystal Resonator Connection (RTC)

3.6.2.2 Unused RTC on the System

The following figure shows the clock pin connection if RTC is not used on your system. RZ/N1 requires that RTC_XI pin is tied-down to ground and RTC_XO is left opened on the board.

As additional requirements related with RTC, 3.3V power supply is required to RTC_VDD33 and 3.3V input is required to RTC_PWRGOOD input pin.

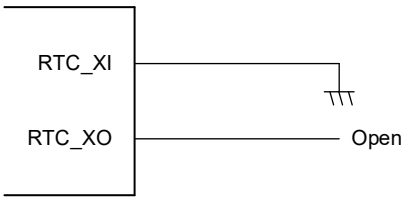


Figure 3.5 Connection of RTC Clock Pins when RTC is Unused

Section 4 Reset

4.1 Overview

RZ/N1 has 2 types of reset, chip-level reset and function module level reset.

Those are shown in below table.

Table 4.1 Category of Reset

	Related External Pin	Description
Master Reset	MRESET_N MRESET_OUT	Reset for entire RZ/N1 LSI. All hardware resource in LSI is in reset during MRESET_N = 0, but only RTC backup domain is exception. MRESET_OUT is 1 during MRESET_N = 0.
System Reset	MRESET_OUT	Reset by internal generated event like watchdog, software trigger. Most part of RZ/N1 is reset by this reset. Software can distinguish source of the last reset, Master reset or System Reset, by RSTSTAT register. When the System reset becomes active, MRESET_OUT outputs 1 with a pulse width of 0.5 µs.
RTC Reset	—	Reset by low voltage detection circuit in RTC domain. The reset is active when supplied voltage for RTC domain becomes below defined level.
JTAG Reset	JTAG_TRST_N	Reset for CoreSight and JTAG TAP controller. Those circuits are reset during JTAG_TRST_N = 0
Module Reset	—	Reset for each function module in RZ/N1. It is controlled by “RSTN_* bit in PWRCTRL_*” registers.

Table 4.2 Reset Domain Definition

	Reset Type				
Reset Target	Master Reset	System Reset	RTC Reset	JTAG Reset	Module Reset
Main Oscillator	—	—	—	—	—
RTC domain	—	—	✓	—	—
PLL	✓	—	—	—	—
USBPLL	✓	✓	—	—	—
RSTSTAT register	✓	—	—	—	—
Main CPU*1	✓	✓	—	—	—
NoC	✓	✓	—	—	—
Function module	✓	✓	—	—	✓ (each module)
CoreSight JTAG TAP controller	✓	—	—	✓	—

Note 1. Cortex-A7 in RZ/N1D, RZ/N1S.
Cortex-M3 in RZ/N1L.

4.2 Chip-level Reset

4.2.1 Master Reset

MRESET_N external pin reset entire RZ/N1 LSI except RTC backup domain. Main oscillator and RTC oscillator are still working during MRESET_N = 0.

CAUTION

RTC backup domain is reset by voltage detection circuit in the domain. The RTC can still count by keep supplying a power for the domain. Therefore, the domain is reset only during entire system power up or low voltage of the power supply.

4.2.2 System Reset

RZ/N1 system controller includes the following registers for system reset control. The reset sources are either the software triggered, watchdog timer, or etc. Each reset source can be enabled or disabled individually and this feature can be enabled or disabled.

Table 4.3 RZ/N1 System Reset Control Register

Address	Register Symbol	Note
4000 C0A8h	RSTSTAT	Reset Status Register It shows the source of the last reset.
4000 C120h	RSTEN	Reset Enable Register. This Register can enable or disable each system reset source. Enabling an active system reset request (in RSTCTRL) will result in immediate reset of the system.
4000 C198h	RSTCTRL	Reset Control Register. Software can use this register to initiate system reset or identify if any of the current hardware system reset sources are requesting a system reset.

CAUTION

- USBPLL is power down mode by system reset and it is the software's responsibility to start it again if needed.
- All programmable dividers return to their power on reset value.
- Before enabling the reset sources in RSTEN register, the software shall make sure that the corresponding reset triggers are cleared in RSTCTRL register otherwise an immediate system reset will occur.

4.2.3 JTAG Reset

JTAG_TRST_N external pin reset CoreSight subsystem and JTAG TAP controller. JTAG TAP controller includes boundary scan circuit. JTAG_TRST_N shall be 0 if CPU debug or JTAG TAP is not used.

4.3 Module Reset

The system controller is capable of providing software reset request to certain modules in the system. The registers that contain the software module reset control bits are named “PWRCTRL_*”, the bit fields are named as “RSTN_*”.

CAUTION

Module reset must be performed with the clock supplied.

Section 5 IO Multiplexing

Signals for System/Peripheral function are multiplexed with External GPIO pins. Timing sensitive signals are routed in Level1 multiplex block, and others are routed in Level2 multiplex blocks. Those are managed by IO multiplex configuration register.

5.1 Overview

Each GPIO[n] pins can be configured individually on following features:

- RGMII interface:
  - Power supply 3.3V for GPIO[n] with n = 0..59
- Standard interface:
  - Power supply 3.3V for GPIO[n] with n = 60..169
- Drive strength capability
- Pull up, pull down or none

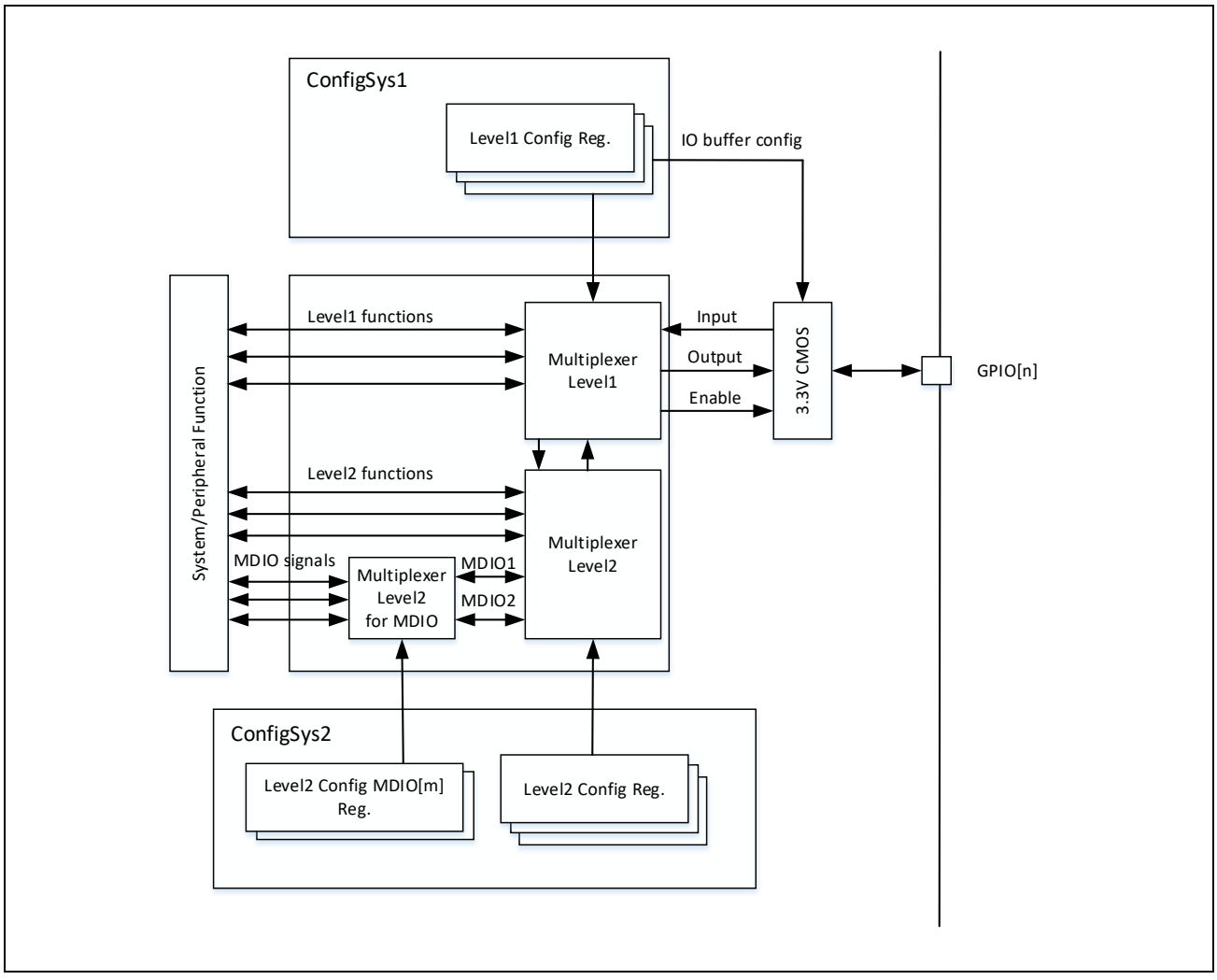


Figure 5.1 IO Multiplex Configuration Level1, Level2

Available Level1 configurations are defined as below.

Table 5.1 IO Multiplex Configuration Level1 List

Function Number	Level1 Function
0	No function (default value)
1	Drive level logic 0
2	RGMII/RMII/MII & Ethernet reference clock
3	NAND Flash & Ethernet reference clock
4	QSPI1,2
5	SDIO1,2
6	LCDC
8	External Bus Interface Master (MSEBIM)
9	External Bus Interface Slave (MSEBIS)
15	IO Multiplex are controlled by Level2

Available Level2 configurations are defined as below.

Table 5.2 IO Multiplex Configuration Level2 List

Function Number	Level2 Function
0	No function (default value)
1	ETHERCAT & Cortex-M3 NMI
2	SERCOSIII
3	Extended SDIO
4	MDIO
6	Extended USB
7	Extended MSEBIM (master)
8	Extended MSEBIS (slave)
12	UART1 Inverted
13	Extended UART1 Inverted
14	UART2 Inverted
15	Extended UART2 Inverted
16	UART3 Inverted
17	Extended UART3 Inverted
18	UART1
19	Extended UART1
20	UART2
21	Extended UART2
22	UART3
23	Extended UART3
24	UART4
25	Extended UART4
26	UART5
27	Extended UART5
28	UART6
29	Extended UART6
30	UART7
31	Extended UART7
32	UART8
33	Extended UART8
34	SPI1 (Master)
36	SPI2 (Master)
38	SPI3 (Master)
40	SPI4 (Master)
42	SPI5 (Slave)
44	SPI6 (Slave)
48	BGPIO
49	CAN
50	I^2C
52 to 56	PWMTimer
61	Extended A5PSW & GMAC

5.2 Register Map

Table 5.3 IO Multiplexing Register Map

Address	Register Symbol	Register Name
4006 7000h + 4h × n	rGPIOs_Level1_ConfigA_[n] (n = 0..59)	GPIO[n] RGMII Multiplexing Level1 Configuration Register
4006 7000h + 4h × n	rGPIOs_Level1_ConfigB_[n] (n = 60..169)	GPIO[n] Standard Multiplexing Level1 Configuration Register
4006 7400h	rGPIOs_Level1_StatusProtect	GPIO Multiplexing Level1 Status and Protect Register
5100 0000h + 4h × n	rGPIOs_Level2_Config_[n] (n = 0..169)	GPIO[n] Multiplexing Level2 Configuration Register
5100 0400h	rGPIOs_Level2_StatusProtect	GPIO Multiplexing Level2 Status and Protect Register
5100 0404h	rGPIOs_Level2_Config_MDIO1	MDIO1 Interface Configuration Register
5100 0408h	rGPIOs_Level2_Config_MDIO2	MDIO2 Interface Configuration Register
5100 0480h+ 4h × n	rGPIOs_Level2_GPIO_Int_[n] (n = 0..7)	GPIO_Int[n] Interrupt Configuration Register

5.3 Register Description

5.3.1 rGPIOs_Level1_ConfigA_[n] — GPIO[n] RGMII Multiplexing Level1 Configuration Register (n = 0..59)

Address: 4006 7000h + 4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	bGPIOs_Level1_DriveStrength		bGPIOs_Level1_PulUp_PullDown		—	—	—	—	bGPIOs_Level1_IOFunction			
Value after reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0

Table 5.4 rGPIOs_Level1_ConfigA_[n] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b12	Reserved	Read as 0.	R
b11, b10	bGPIOs_Level1_DriveStrength	Select drive strength capability used on GPIO. 2'b00: 4 mA 2'b01: 6 mA 2'b10: 8 mA (default value) 2'b11: 12 mA	R/W
b9, b8	bGPIOs_Level1_PulUp_PullDown	Select a pull-up, pull-down resistor used on GPIO. 2'b00: None 2'b01: Pull up (default value) 2'b10: None 2'b11: Pull down	R/W
b7 to b4	Reserved	Read as 0.	R
b3 to b0	bGPIOs_Level1_IOFunction	Select the Level1 function used on GPIO: See **Table 5.1, IO Multiplex Configuration Level1 List**.	R/W

CAUTION

- A write access is protected by bGPIOs_Level1_Config_StatusProtect bit.
- For total output current, see Note 1 of "**Table 11.3, Current**" in "**Section 11.3.1, Current**".

5.3.2 rGPIOs_Level1_ConfigB_[n] — GPIO[n] Standard Multiplexing Level1 Configuration Register (n = 60..169 (max))

Address: 4006 7000h + 4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	bGPIOs_Level1_Standard_DriveStrength		bGPIOs_Level1_Standard_PulUp_PullDown		—	—	—	—	bGPIOs_Level1_Standard_IOFunction			
Value after reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0

Table 5.5 rGPIOs_Level1_ConfigB_[n] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b12	Reserved	Read as 0.	R
b11, b10	bGPIOs_Level1_Standard_DriveStrength	Select drive strength capability used on GPIO. 2'b00: 4 mA 2'b01: 6 mA 2'b10: 8 mA (default value) 2'b11: 12 mA	R/W
b9, b8	bGPIOs_Level1_Standard_PulUp_PullDown	Select a pull-up, pull-down resistor used on GPIO.*1 2'b00: None 2'b01: Pull up (default value) 2'b10: None 2'b11: Pull down	R/W
b7 to b4	Reserved	Read as 0.	R
b3 to b0	bGPIOs_Level1_Standard_IOFunction	Select the Level1 function used on GPIO.*2 See **Table 5.1, IO Multiplex Configuration Level1 List**.	R/W

Note 1. GPIO[73:62] and GPIO[145:127] are configured according to GPIO[79] level at rising of MRESET_N
1: Pull up on GPIO[73:62] and GPIO[145:127]
0: Pull down on GPIO[73:62] and GPIO[145:127]

Note 2. GPIO[79:74] are directly configured on QSPI interface in RZ/N1L.
GPIO[103] is configured on UART1_TXD by boot ROM.

CAUTION

- A write access is protected by bGPIOs_Level1_Config_StatusProtect bit.
- For total output current, see Note 1 of "**Table 11.3, Current**" in "**Section 11.3.1, Current**".

5.3.3 rGPIOs_Level1_StatusProtect — GPIO Multiplexing Level1 Status and Protect Register

Address: 4006 7400h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	bGPIOs_Level1_BadSequence	—	—	—	bGPIOs_Level1_Config_StatusProtect
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.6 rGPIOs_Level1_StatusProtect Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b5	Reserved	Read as 0.	R
b4	bGPIOs_Level1_BadSequence	Bad sequence detection Set “1” when it happens a bad write sequence in the rGPIOs_Level1_StatusProtect register Clear “0” when it happens – Reset – By a specific write sequence (write 4006_7402h to this register)	R/W
b3 to b1	Reserved	Read as 0.	R
b0	bGPIOs_Level1_Config_StatusProtect	Write protection of following registers • rGPIOs_Level1_ConfigA_[n] • rGPIOs_Level1_ConfigB_[n] 0: All the registers are protected in write, read only 1: All the registers are not protected, write and read are enable Clear “0” when it happens – Reset – A bad write sequence in register Set or cleared bGPIOs_Level1_Config_StatusProtect bit by a specific write sequence [Set] Write 4006_7400h to this register [Clear] Write 4006_7401h to this register See Protected access of GPIOs Level1 Configuration Register.	R/W

5.3.4 rGPIOs_Level2_Config_[n] — GPIO[n] Multiplexing Level2 Configuration Register (n = 0..169 (max))

Address: 5100 0000h + 4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	bGPIOs_Level2_IOFunction					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.7 rGPIOs_Level2_Config_[n] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b6	Reserved	Read as 0.	R
b5 to b0	bGPIOs_Level2_IOFunction	Select the Level2 function used on GPIO. See **Table 5.2, IO Multiplex Configuration Level2 List**.	R/W

CAUTION

A write access is protected by bGPIOs_Level2_Config_StatusProtect bit.

5.3.5 rGPIOs_Level2_StatusProtect — GPIO Multiplexing Level2 Status and Protect Register

Address: 5100 0400h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	bGPIOs_Level2_BadSequence	—	—	—	bGPIOs_Level2_Config_StatusProtect
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.8 rGPIOs_Level2_StatusProtect Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b5	Reserved	Read as 0.	R
b4	bGPIOs_Level2_BadSequence	Bad sequence detection Set “1” when it happens a bad write sequence in the rGPIOs_Level2_StatusProtect register Clear “0” when it happens – Reset – By a specific write sequence (write 5100_0420h to this register) Write {Upper 29 bits of rGPIOs_Level2_StatusProtect address, 3’b010} to rGPIOs_Level2_StatusProtect register	R/W
b3 to b1	Reserved	Read as 0.	R
b0	bGPIOs_Level2_Config_StatusProtect	Write protection of following registers • rGPIOs_Level2_Config_[n] • rGPIOs_Level2_Config_MDIO1 • rGPIOs_Level2_Config_MDIO2 0: All the registers are protected in write, read only 1: All the registers are not protected, write and read are enable Clear “0” when it happens – Reset – A bad write sequence in register Set or cleared bGPIOs_Level2_Config_StatusProtect bit by a specific write sequence [Set] Write 5100_0400h to this register [Clear] Write 5100_0401h to this register See Protected access of GPIO Level2 Configuration Register	R/W

5.3.6 rGPIOs_Level2_Config_MDIO1 — MDIO1 Interface Configuration Register

Address: 5100 0404h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	bGPIOs_Level2_Config_MDIO1		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.9 rGPIOs_Level2_Config_MDIO1 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved	Read as 0.	R
b2 to b0	bGPIOs_Level2_Config_MDIO1	MDIO1 interface configuration. 3’b000: Floating 3’b001: GMAC1 3’b010: GMAC2 3’b011: ETHERCAT 3’b100: SERCOSIII MDIO1 3’b101: SERCOSIII MDIO2 3’b110: HW-RTOS GMAC 3’b111: Advanced 5port Switch	R/W

CAUTION

A write access is protected by bGPIOs_Level2_Config_StatusProtect bit.

5.3.7 rGPIOs_Level2_Config_MDIO2 — MDIO2 Interface Configuration Register

Address: 5100 0408h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	bGPIOs_Level2_Config_MDIO2		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.10 rGPIOs_Level2_Config_MDIO2 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved	Read as 0.	R
b2 to b0	bGPIOs_Level2_Config_MDIO2	MDIO2 interface configuration. Same as rGPIOs_Level2_Config_MDIO1	R/W

CAUTION

A write access is protected by bGPIOs_Level2_Config_StatusProtect bit.

5.3.8 rGPIOs_Level2_GPIO_Int_[n] — GPIO_Int[n] Interrupt Configuration Register (n = 0..7)

GPIO_Int[n] (IRQ103 to IRQ110) interrupt line configuration with n = 0..7.

Address: 5100 0480h + 4h × n

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	bGPIOs_Level2_GPIO_Int						
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.11 rGPIOs_Level2_GPIO_Int_[n] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b7	Reserved	Read as 0.	R
b6 to b0	bGPIOs_Level2_GPIO_Int	For each interrupt GPIO_Int[n] Selects an interrupt source from 3x32 possible interrupt sources BGPIO1_Int[31:0] or BGPIO2_Int[31:0] or BGPIO3_Int[31:0] Select function used on multiplexing level2: • Interrupt sources routed from BGPIO1: 7'b00_00000: BGPIO1_Int[0] .... 7'b00_11111: BGPIO1_Int[31] • Interrupt sources routed from BGPIO2: 7'b01_00000: BGPIO2_Int[0] .... 7'b01_11111: BGPIO2_Int[31] • Interrupt sources routed from BGPIO3: 7'b10_00000: BGPIO3_Int[0] .... 7'b10_11111: BGPIO3_Int[31] • Others 7'b11_xxxxx: Reserved	R/W

5.4 Operation

5.4.1 Protected Access of GPIOs Level1 Configuration Register

Lock register to protect registers from unexpected behavior, a specific sequence must be written to change protect status. Set or cleared a protect bit dedicated bGPIOs_Level1_Config_StatusProtect, allowing write of following registers:

- rGPIOs_Level1_ConfigA_[n]
- rGPIOs_Level1_ConfigB_[n]

- Unprotect (writable) — Set bGPIOs_Level1_Config_StatusProtect

  Write {Upper 29 bits of rGPIOs_Level1_StatusProtect address, 3'b000} to rGPIOs_Level1_StatusProtect register
  i.e. *(4006 7400h) = 4006 7400h

- Protect — Clear bGPIOs_Level1_Config_StatusProtect

  Write {Upper 29 bits of rGPIOs_Level1_StatusProtect address, 3'b001} to rGPIOs_Level1_StatusProtect register
  i.e. *(4006 7400h) = 4006 7401h

- Clear BadSequence Bit

  If incorrect data is written to rGPIOs_Level1_StatusProtect Register,
  bGPIOs_Level1_BadSequence is set
  bGPIOs_Level1_Config_StatusProtect is cleared.

  The bit is cleared by
  Write {Upper 29 bits of rGPIOs_Level1_StatusProtect address, 3'b010} to rGPIOs_Level1_StatusProtect register
  i.e. *(4006 7400h) = 4006 7402h

5.4.2 Protected Access of GPIOs Level2 Configuration Register

Lock register to protect registers from unexpected behavior, a specific sequence must be written to change protect status. Set or cleared a protect bit dedicated bGPIOs_Level2_Config_StatusProtect, allowing write of following registers:

- rGPIOs_Level2_Config_[n]
- rGPIOs_Level2_Config_MDIO1
- rGPIOs_Level2_Config_MDIO2

- Unprotect (writable) — Set bGPIOs_Level2_Config_StatusProtect

  Write {Upper 29 bits of rGPIOs_Level2_StatusProtect address, 3'b000} to rGPIOs_Level2_StatusProtect register
  i.e. *(5100 0400h) = 5100 0400h

- Protect — Clear bGPIOs_Level2_Config_StatusProtect

  Write {Upper 29 bits of rGPIOs_Level2_StatusProtect address, 3'b001} to rGPIOs_Level2_StatusProtect register
  i.e. *(5100 0400h) = 5100 0401h

- Clear BadSequence Bit

  If incorrect data is written to rGPIOs_Level2_StatusProtect Register,
  bGPIOs_Level2_BadSequence is set
  bGPIOs_Level2_Config_StatusProtect is cleared.

  The bit is cleared by
  Write {Upper 29 bits of rGPIOs_Level2_StatusProtect address, 3'b010} to rGPIOs_Level2_StatusProtect register
  i.e. *(5100 0400h) = 5100 0402h

5.4.3 Configuration of GPIO Interrupt Line

Interrupt line to CPUs, GPIO_Int[n], are configured by rGPIOs_Level2_GPIO_Int_[n]. GPIO_Int[n] are selected from 32bits × 3 interrupts output of BGPIO modules.

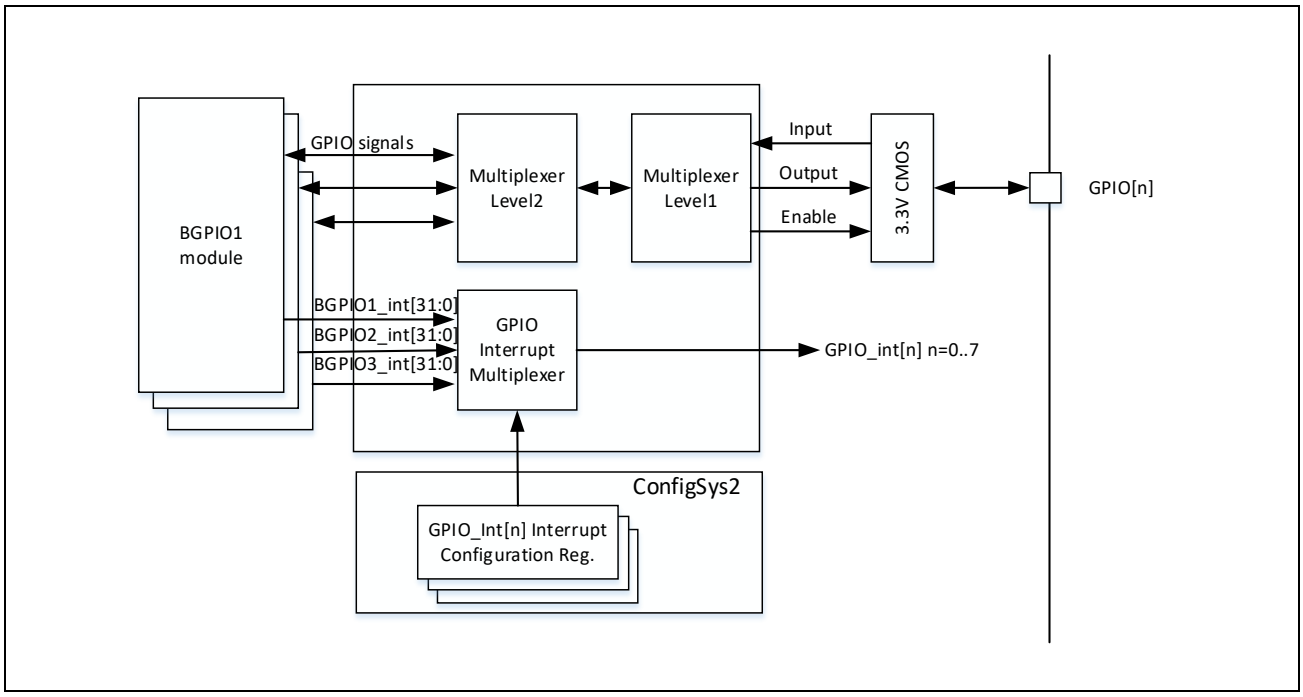


Figure 5.2 GPIO_Int[n] Configuration

Section 6 System Control

6.1 Overview

The RZ/N1 system controller includes registers for setting clock, reset, NoC (Network-on-Chip) management and chip-level LSI configuration. Please refer to Clock Generation, Reset, Operating Mode chapter for more detail.

6.2 Register Map

Table 6.1 Clock Control Registers (1/2)

Address	Register Symbol	Register Name
4000 C00Ch	PWRCTRL_SDIO1	Power Management Control for SDIO1
4000 C010h	PWRSTAT_SDIO1	Power Management Status for SDIO1
4000 C01Ch	PWRCTRL_USB	Power Management Control for USB2.0
4000 C020h	PWRSTAT_USB	Power Management Status for USB2.0
4000 C02Ch	PWRCTRL_MSEBI	Power Management Control for MSEBI
4000 C030h	PWRSTAT_MSEBI	Power Management Status for MSEBI
4000 C034h	PWRCTRL_PG0_0	Power Management Control #0 for PG0
4000 C038h	PWRSTAT_PG0	Power Management Status for PG0
4000 C03Ch	PWRCTRL_PG0_1	Power Management Control #1 for PG0
4000 C040h	PWRCTRL_PG1_1	Power Management Control #1 for PG1
4000 C044h	PWRCTRL_PG1_2	Power Management Control #2 for PG1
4000 C04Ch	PWRCTRL_DMA	Power Management Control for DMAC1 & DMAC2
4000 C050h	PWRCTRL_NFLASH	Power Management Control for NAND FLASH Controller
4000 C054h	PWRCTRL_QSPI1	Power Management Control for QSPI1
4000 C058h	PWRSTAT_DMA	Power Management Status for DMAC1 & DMAC2
4000 C05Ch	PWRSTAT_NFLASH	Power Management Status for NAND FLASH Controller
4000 C060h	PWRSTAT_QSPI1	Power Management Status for QSPI1
4000 C064h	(RZ/N1D) PWRCTRL_DDRC	Power Management Control for DDR Memory Controller
	(RZ/N1S) PWRCTRL_QSPI2DIV	Clock Divider Control for QSPI2
	(RZ/N1L) Reserved	
4000 C068h	PWRCTRL_EETH	Power Management Control for External Ethernet Clock
4000 C06Ch	PWRCTRL_MAC1	Power Management Control for GMAC1
4000 C070h	PWRCTRL_MAC2	Power Management Control for GMAC2
4000 C074h	(RZ/N1D) PWRSTAT_DDRC	Power Management Status for DDR Memory Controller
	(RZ/N1S, RZ/N1L) Reserved	
4000 C078h	PWRSTAT_MAC1	Power Management Status for GMAC1
4000 C07Ch	PWRSTAT_MAC2	Power Management Status for GMAC2
4000 C080h	PWRCTRL_ECAT	Power Management Control for ETHERCAT
4000 C084h	PWRCTRL_SERCOS	Power Management Control for SERCOSIII
4000 C088h	PWRSTAT_ECAT	Power Management Status for ETHERCAT
4000 C08Ch	PWRSTAT_SERCOS	Power Management Status for SERCOSIII
4000 C090h	(RZ/N1D) PWRCTRL_HSR	Power Management Control for HSR
	(RZ/N1S) PWRCTRL_QSPI2	Power Management Control for QSPI2
	(RZ/N1L) Reserved	
4000 C094h	PWRCTRL_SWITCHDIV	Clock Divider Control for A5PSW

Table 6.1 Clock Control Registers (2/2)

Address	Register Symbol	Register Name
4000 C098h	(RZ/N1D) PWRSTAT_HSR	Power Management Status for HSR
	(RZ/N1S) PWRSTAT_QSPI2	Power Management Status for QSPI2
	(RZ/N1L) Reserved	
4000 C09Ch	PWRSTAT_SWITCH	Power Management Status for A5PSW
4000 C0C8h	PWRCTRL_SDIO2	Power Management Control for SDIO2
4000 C0CCh	PWRSTAT_SDIO2	Power Management Status for SDIO2
4000 C0E0h	PWRCTRL_OPPDIV	Clock Divider Control for OPP Modes
4000 C0E4h	PWRCTRL_CA7DIV	Clock Divider Control for CA7
4000 C0E8h	PWRCTRL_PG2_25MHZ	Power Management Control for PG2 25MHz
4000 C0ECh	PWRCTRL_PG1_PR2	Power Management Control for PG1 Program2
4000 C0F0h	PWRCTRL_PG3_48MHZ	Power Management Control for PG3 48MHz
4000 C0F4h	PWRCTRL_PG4	Power Management Control for PG4
4000 C0F8h	PWRCTRL_PG1_PR2DIV	Clock Divider Control for PG1 Program2
4000 C0FCh	PWRCTRL_PG1_PR3	Power Management Control for PG1 Program3
4000 C100h	PWRCTRL_PG1_PR3DIV	Clock Divider Control for PG1 Program3
4000 C104h	PWRCTRL_PG1_PR4	Power Management Control for PG1 Program4
4000 C108h	PWRCTRL_PG1_PR4DIV	Clock Divider Control for PG1 Program4
4000 C10Ch	PWRCTRL_PG4_PR1	Power Management Control for PG4 Program1
4000 C110h	PWRCTRL_PG4_PR1DIV	Clock Divider Control for PG4 Program1
4000 C124h	PWRCTRL_QSPI1DIV	Clock Divider Control for QSPI1
4000 C128h	PWRCTRL_SDIO1DIV	Clock Divider Control for SDIO1
4000 C12Ch	PWRCTRL_SDIO2DIV	Clock Divider Control for SDIO2
4000 C130h	PWRCTRL_SWITCH	Power Management Control for A5PSW
4000 C134h	PWRCTRL_PG0_ADCDIV	Clock Divider Control for PG0 ADC
4000 C138h	PWRCTRL_PG0_I2CDIV	Clock Divider Control for PG0 I2C
4000 C13Ch	PWRCTRL_PG0_UARTDIV	Clock Divider Control for PG0 UART
4000 C140h	PWRCTRL_RTC	Power Management Control for RTC
4000 C144h	PWRSTAT_RTC	Power Management Status for RTC
4000 C148h	PWRCTRL_NFLASHDIV	Clock Divider Control for NAND FLASH Controller
4000 C154h	(RZ/N1D, RZ/N1S) PWRCTRL_ROM	Power Management Control for ROM
	(RZ/N1L) Reserved	
4000 C158h	PWRSTAT_PG1	Power Management Status for PG1
4000 C15Ch	PWRSTAT_PG2_25MHZ	Power Management Status for PG2 25MHz
4000 C160h	PWRSTAT_PG3_48MHZ	Power Management Status for PG3 48MHz
4000 C164h	PWRSTAT_PG4	Power Management Status for PG4
4000 C170h	(RZ/N1D, RZ/N1S) PWRSTAT_ROM	Power Management Status for ROM
	(RZ/N1L) Reserved	
4000 C174h	PWRCTRL_CM3	Power Management Control for CM3
4000 C178h	PWRSTAT_CM3	Power Management Status for CM3
4000 C17Ch	PWRSTAT_RINCTRL	Power Management Status for R-IN Engine Accessory Register
4000 C180h	PWRSTAT_SWITCHCTRL	Power Management Status for Ethernet Accessory Register
4000 C184h	PWRCTRL_RINCTRL	Power Management Control for R-IN Engine Accessory Register
4000 C188h	PWRCTRL_SWITCHCTRL	Power Management Control for Ethernet Accessory Register
4000 C18Ch	PWRCTRL_HWRTOS	Power Management Control for HW-RTOS
4000 C190h	PWRCTRL_HWRTOS_MDCDIV	Clock Divider Control for HW-RTOS GMAC MDC Clock

Table 6.2 Register Map of Reset Control (1/2)

Address	Register Symbol	Register Name
4000 C00Ch	PWRCTRL_SDIO1	Power Management Control for SDIO1
4000 C010h	PWRSTAT_SDIO1	Power Management Status for SDIO1
4000 C018h	SYSSTAT	System Status Flags Register
4000 C01Ch	PWRCTRL_USB	Power Management Control for USB2.0
4000 C020h	PWRSTAT_USB	Power Management Status for USB2.0
4000 C02Ch	PWRCTRL_MSEBI	Power Management Control for MSEBI
4000 C030h	PWRSTAT_MSEBI	Power Management Status for MSEBI
4000 C034h	PWRCTRL_PG0_0	Power Management Control #0 for PG0
4000 C038h	PWRSTAT_PG0	Power Management Status for PG0
4000 C03Ch	PWRCTRL_PG0_1	Power Management Control #1 for PG0
4000 C040h	PWRCTRL_PG1_1	Power Management Control #1 for PG1
4000 C044h	PWRCTRL_PG1_2	Power Management Control #2 for PG1
4000 C04Ch	PWRCTRL_DMA	Power Management Control for DMAC1 & DMAC2
4000 C050h	PWRCTRL_NFLASH	Power Management Control for NAND FLASH Controller
4000 C054h	PWRCTRL_QSPI1	Power Management Control for QSPI1
4000 C058h	PWRSTAT_DMA	Power Management Status for DMAC1 & DMAC2
4000 C05Ch	PWRSTAT_NFLASH	Power Management Status for NAND FLASH Controller
4000 C060h	PWRSTAT_QSPI1	Power Management Status for QSPI1
4000 C064h	(RZ/N1D) PWRCTRL_DDRC	Power Management Control for DDR memory controller
	(RZ/N1S) PWRCTRL_QSPI2DIV	Clock divider Control for QSPI2
	(RZ/N1L) Reserved	
4000 C068h	PWRCTRL_EETH	Power Management Control for External Ethernet Clock
4000 C06Ch	PWRCTRL_MAC1	Power Management Control for GMAC1
4000 C070h	PWRCTRL_MAC2	Power Management Control for GMAC2
4000 C074h	(RZ/N1D) PWRSTAT_DDRC	Power Management Status for DDR memory controller
	(RZ/N1S, RZ/N1L) Reserved	
4000 C078h	PWRSTAT_MAC1	Power Management Status for GMAC1
4000 C07Ch	PWRSTAT_MAC2	Power Management Status for GMAC2
4000 C080h	PWRCTRL_ECAT	Power Management Control for ETHERCAT
4000 C084h	PWRCTRL_SERCOS	Power Management Control for SERCOSIII
4000 C088h	PWRSTAT_ECAT	Power Management Status for ETHERCAT
4000 C08Ch	PWRSTAT_SERCOS	Power Management Status for SERCOSIII
4000 C090h	(RZ/N1D) PWRCTRL_HSR	Power Management Control for HSR
	(RZ/N1S) PWRCTRL_QSPI2	Power Management Control for QSPI2
	(RZ/N1L) Reserved	
4000 C098h	(RZ/N1D) PWRSTAT_HSR	Power Management Status for HSR
	(RZ/N1S) PWRSTAT_QSPI2	Power Management Status for QSPI2
	(RZ/N1L) Reserved	
4000 C09Ch	PWRSTAT_SWITCH	Power Management Status for A5PSW
4000 C0A8h	RSTSTAT	Reset Status Register
4000 C0C0h	USBSTAT	Status information for USBPLL
4000 C0C8h	PWRCTRL_SDIO2	Power Management Control for SDIO2
4000 C0CCh	PWRSTAT_SDIO2	Power Management Status for SDIO2
4000 C0E8h	PWRCTRL_PG2_25MHZ	Power Management Control for PG2 25MHz
4000 C0ECh	PWRCTRL_PG1_PR2	Power Management Control for PG1 Program2

Table 6.2 Register Map of Reset Control (2/2)

Address	Register Symbol	Register Name
4000 C0F0h	PWRCTRL_PG3_48MHZ	Power Management Control for PG3 48MHz
4000 C0F4h	PWRCTRL_PG4	Power Management Control for PG4
4000 C0FCh	PWRCTRL_PG1_PR3	Power Management Control for PG1 Program3
4000 C104h	PWRCTRL_PG1_PR4	Power Management Control for PG1 Program4
4000 C10Ch	PWRCTRL_PG4_PR1	Power Management Control for PG4 Program1
4000 C120h	RSTEN	Reset Enable Register
4000 C130h	PWRCTRL_SWITCH	Power Management Control for A5PSW
4000 C140h	PWRCTRL_RTC	Power Management Control for RTC
4000 C144h	PWRSTAT_RTC	Power Management Status for RTC
4000 C154h	(RZ/N1D, RZ/N1S) PWRCTRL_ROM	Power Management Control for ROM
	(RZ/N1L) Reserved	
4000 C158h	PWRSTAT_PG1	Power Management Status for PG1
4000 C15Ch	PWRSTAT_PG2_25MHZ	Power Management Status for PG2 25MHz
4000 C160h	PWRSTAT_PG3_48MHZ	Power Management Status for PG3 48MHz
4000 C164h	PWRSTAT_PG4	Power Management Status for PG4
4000 C170h	(RZ/N1D, RZ/N1S) PWRSTAT_ROM	Power Management Status for ROM
	(RZ/N1L) Reserved	
4000 C174h	PWRCTRL_CM3	Power Management Control for CM3
4000 C178h	PWRSTAT_CM3	Power Management Status for CM3
4000 C17Ch	PWRSTAT_RINCTRL	Power Management Status for R-IN Engine Accessory Register
4000 C180h	PWRSTAT_SWITCHCTRL	Power Management Status for Ethernet Accessory Register
4000 C184h	PWRCTRL_RINCTRL	Power Management Control for R-IN Engine Accessory Register
4000 C188h	PWRCTRL_SWITCHCTRL	Power Management Control for Ethernet Accessory Register
4000 C18Ch	PWRCTRL_HWRTOS	Power Management Control for HW-RTOS
4000 C198h	RSTCTRL	Reset Control Register

Table 6.3 Register Map of System Configuration

Address	Register Symbol	Register Name
4000 C000h	CFG_USB	USB Mode Configuration Register
4000 C004h	OPMODE	System and Boot Configuration Register
4000 C008h	CFG_SDIO1	SDIO1 Configuration Register
4000 C014h	DBGCON	Debug Control Register
4000 C0A0h	CFG_DMAMUX	DMAC1 & DMAC2 Multiplexer Register
4000 C0A4h	CFG_GPIOT_PTEN_1A	GPIO Trigger Enable Register 1A
4000 C0B0h	CFG_GPIOT_PTEN_1B	GPIO Trigger Enable Register 1B
4000 C0B4h	CFG_GPIOT_PTEN_2A	GPIO Trigger Enable Register 2A
4000 C0B8h	CFG_GPIOT_PTEN_2B	GPIO Trigger Enable Register 2B
4000 C0BCh	CFG_GPIOT_TSRC	GPIO Trigger Source Select Register
4000 C0C4h	CFG_SDIO2	SDIO2 Configuration Register
4000 C0D8h	CFG_GPIOT_PTEN_3A	GPIO Trigger Enable Register 3A
4000 C0DCh	CFG_GPIOT_PTEN_3B	GPIO Trigger Enable Register 3B
4000 C19Ch	VERSION	Product Version Register
4000 C204h	BOOTADDR	Cortex-A7 processor1 Boot Address Configuration Register

6.3 Register Description

6.3.1 PWRCTRL_SWITCHDIV — Clock Divider Control for A5PSW

Address: 4000 C094h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	DIV						
Value after reset	X	X	X	X	X	X	X	X	X	0	0	0	0	1	0	1

Table 6.4 PWRCTRL_SWITCHDIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b7	Reserved		R
b6 to b0	DIV	Clock Divider for A5PSW clock (A5PSW_SXCLK) Valid range: 5	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.2 PWRCTRL_OPPDIV — Clock Divider Control for OPP Modes

This register scales the reference frequency of the system. This value has direct effect on interconnect clocks and Cortex-A7 clock.

Address: 4000 C0E0h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DIV				
Value after reset	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	0

Table 6.5 PWRCTRL_OPPDIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b5	Reserved		R
b4 to b0	DIV	Clock Divider for the NoC clock Valid values are: [2,4,8,16]	R/W

NOTE

- This register values should be changed to initial value in case of entering RTC backup mode.
- Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.
- Changing the frequency of the main interconnect effects the reference clock frequency of the Watchdog timers.

6.3.3 PWRCTRL_CA7DIV — Clock Divider Control for CA7

Address: 4000 C0E4h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DIV		
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0

Table 6.6 PWRCTRL_CA7DIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b3	Reserved		R
b2 to b0	DIV	Clock Divider for the Cortex-A7 processor clock Valid values are: [1,2,4]	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.4 PWRCTRL_PG1_PR2DIV — Clock Divider Control for PG1 Program2

Address: 4000 C0F8h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DIV							
Value after reset	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0	0

Table 6.7 PWRCTRL_PG1_PR2DIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b8	Reserved		R
b7 to b0	DIV	PG1 Program2 Clock Divider for UART[m]_SCLK (m = 4..8) Valid range: 12 to 128	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.5 PWRCTRL_PG1_PR3DIV — Clock Divider Control for PG1 Program3

Address: 4000 C100h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DIV							
Value after reset	X	X	X	X	X	X	X	X	0	0	0	0	1	0	0	0

Table 6.8 PWRCTRL_PG1_PR3DIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b8	Reserved		R
b7 to b0	DIV	PG1 Program3 Clock Divider for SPI[m]_SCLK (m = 1..4) Valid range (also depend on frequency mode): 8–128 ***Note*)** SPI[m]_SCLK must be less than or equal to the frequency of NoC clock.	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.6 PWRCTRL_PG1_PR4DIV — Clock Divider Control for PG1 Program4

Address: 4000 C108h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DIV							
Value after reset	X	X	X	X	X	X	X	X	0	0	0	0	1	0	0	0

Table 6.9 PWRCTRL_PG1_PR4DIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b8	Reserved		R
b7 to b0	DIV	PG1 Program4 Clock Divider for SPI[m]_SCLK (m = 5, 6) Valid range (also depend on frequency mode): 8–128 ***Note*)** SPI[m]_SCLK must be less than or equal to the frequency of NoC clock.	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.7 PWRCTRL_PG4_PR1DIV — Clock Divider Control for PG4 Program1

Address: 4000 C110h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DIV							
Value after reset	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0	0

Table 6.10 PWRCTRL_PG4_PR1DIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b8	Reserved		R
b7 to b0	DIV	PG4 Program1 Clock Divider for LCD_ECLK Valid range (also depend on frequency mode): 12–200 ***Note*)** LCD_ECLK must be slower than LCD_HCLK.	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.8 PWRCTRL_QSPI1DIV — Clock Divider Control for QSPI1

Address: 4000 C124h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	DIV						
Value after reset	X	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0

Table 6.11 PWRCTRL_QSPI1DIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b7	Reserved		R
b6 to b0	DIV	Clock Divider for QSPI1_REFCLK Valid range: 4–64 ***Note*)** QSPI1_REFCLK must be faster than NoC clock.	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.9 PWRCTRL_SDIO1DIV — Clock Divider Control for SDIO1

Address: 4000 C128h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DIV							
Value after reset	X	X	X	X	X	X	X	X	0	0	0	1	0	1	0	0

Table 6.12 PWRCTRL_SDIO1DIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b8	Reserved		R
b7 to b0	DIV	Clock Divider for SDIO1_ECLK Valid range: 20–100	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.10 PWRCTRL_SDIO2DIV — Clock Divider Control for SDIO2

Address: 4000 C12Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DIV							
Value after reset	X	X	X	X	X	X	X	X	0	0	0	1	0	1	0	0

Table 6.13 PWRCTRL_SDIO2DIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b8	Reserved		R
b7 to b0	DIV	Clock Divider for SDIO2_ECLK Valid range: 20–100	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.11 PWRCTRL_PG0_ADCDIV — Clock Divider Control for PG0 ADC

Address: 4000 C134h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DIV									
Value after reset	X	X	X	X	X	X	0	0	0	0	1	1	0	0	1	0

Table 6.14 PWRCTRL_PG0_ADCDIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b10	Reserved		R
b9 to b0	DIV	Clock Divider for ADC_CLK Valid range: 50–250	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.12 PWRCTRL_PG0_I2CDIV — Clock Divider Control for PG0 I2C

Address: 4000 C138h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	DIV						
Value after reset	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	0

Table 6.15 PWRCTRL_PG0_I2CDIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b7	Reserved		R
b6 to b0	DIV	Clock Divider for I2C[m]_SCLK (m = 1, 2) Valid range (also depend on frequency mode): 12–64 ***Note*)** I2C[m]_SCLK must be faster than or equal to the frequency of I2C[m]_PCLK.	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.13 PWRCTRL_PG0_UARTDIV — Clock Divider Control for PG0 UART

Address: 4000 C13Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DIV							
Value after reset	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0	0

Table 6.16 PWRCTRL_PG0_UARTDIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b8	Reserved		R
b7 to b0	DIV	Clock Divider for UART[m]_SCLK (m = 1..3) Valid range: 12–128	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.14 PWRCTRL_NFLASHDIV — Clock Divider Control for NAND FLASH Controller

Address: 4000 C148h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	DIV						
Value after reset	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	0

Table 6.17 PWRCTRL_NFLASHDIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b7	Reserved		R
b6 to b0	DIV	Clock Divider for NAND_ECLK Valid range: 12–64 ***Note*)** If PWRCTRL_OPPDIV.DIV = 2 then the maximum value is 32.	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.15 PWRCTRL_HWRTOS_MDCDIV — Clock Divider Control for HW-RTOS GMAC MDC Clock

Address: 4000 C190h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DIV									
Value after reset	X	X	X	X	X	X	0	0	0	1	0	1	0	0	0	0

Table 6.18 PWRCTRL_HWRTOS_MDCDIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b10	Reserved		R
b9 to b0	DIV	Clock Divider for HWRTOS_MDCCLK Valid values are: [80,160,320,640]	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.16 PWRCTRL_QSPI2DIV — Clock Divider Control for QSPI2

Address: 4000 C064h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BUSY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	DIV						
Value after reset	X	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0

Table 6.19 PWRCTRL_QSPI2DIV Register Contents

Bit Position	Bit Name	Function	R/W
b31	BUSY	Register Write (BUSY = 1) triggers the divider value change. Register Read Shows the status of the Programmable divider. 1: Divider setting is being changed, changing DIV value is forbidden and results in non-deterministic behavior. 0: Clock setting has been applied, new setting may be written to DIV.	R/W
b30 to b7	Reserved		R
b6 to b0	DIV	Clock Divider for QSPI2_REFCLK Valid range: 4–64 ***Note*)** QSPI2_REFCLK must be faster than NoC clock.	R/W

NOTE

Writing to this register is forbidden and results in a bus error response when BUSY field is asserted.

6.3.17 PWRCTRL_SDIO1 — Power Management Control for SDIO1

Address: 4000 C00Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CLKEN_B	MIREQ_A	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	1	1	0	1	1

Table 6.20 PWRCTRL_SDIO1 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b5	Reserved		R
b4	CLKEN_B	Clock Enable for SDIO1_ECLK (external interface) 0: Disable 1: Enable	R/W
b3	MIREQ_A	AHBM Idle Request to the NoC interconnect for SDIO1 0: Active 1: Idle	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the AHBS is ready for SDIO1 access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for SDIO1_HCLK domain. If set to 0, reset the NoC interconnect for SDIO1.	R/W
b0	CLKEN_A	Clock Enable for SDIO1_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.18 PWRSTAT_SDIO1 — Power Management Status for SDIO1

Address: 4000 C010h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0

Table 6.21 PWRSTAT_SDIO1 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	MISTAT_A	AHBM Idle Status of the NoC interconnect for SDIO1 0: Active 1: Idle	R
b1	MIRACK_A	AHBM Idle Request Acknowledge for SDIO1 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b0	SCON_A	AHBS NoC Interconnection Status for SDIO1 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.19 SYSSTAT — System Status Flags Register

Address: 4000 C018h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	PKGMODE	—	CA7_STANDBYWFIL2	CA7_STANDBYWFI		CA7_STANDBYWFE	
Value after reset	X	X	X	X	X	X	X	X	X	0	1	0	0	0	0	0

Table 6.22 SYSSTAT Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b7	Reserved		R
b6	PKGMODE	Package type (RZ/N1D) 0: 400 pin package 1: 324 pin package (RZ/N1S) 0: 324 pin package 1: 196 pin package (RZ/N1L) 1: 196 pin package	R
b5	Reserved		R
b4	CA7_STANDBYWFIL2	Indicates if the L2 memory system is in WFI state: When in the WFI state, all Cortex-A7 processors are in the WFI state. 0: L2 memory system not in WFI state 1: L2 memory system in WFI state	R
b3, b2	CA7_STANDBYWFI	Indicates if a Cortex-A7 processor is in WFI state: 0: Processor not in WFI state 1: Processor in WFI state Bit3 (RZ/N1D) represents processor 1. (RZ/N1S) Reserved. Bit2 represents processor 0.	R
b1, b0	CA7_STANDBYWFE	Indicates if a Cortex-A7 processor is in WFE state: 0: Processor not in WFE state 1: Processor in WFE state Bit1 (RZ/N1D) represents processor 1. (RZ/N1S) Reserved. Bit0 represents processor 0.	R

NOTE

Bit 5 to 0 are reserved bits for RZ/N1L.

6.3.20 PWRCTRL_USB — Power Management Control for USB2.0

Address: 4000 C01Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RSTN_F	CLKEN_E	CLKEN_C	MIREQ_B	CLKEN_B	MIREQ_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1

Table 6.23 PWRCTRL_USB Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b8	Reserved		R
b7	RSTN_F	Active low Reset for 48 MHz clock domain. If set to 0, reset the complete 48 MHz clock domain.	R/W
b6	CLKEN_E	Clock Enable for USB_PCICLK 0: Disable 1: Enable	R/W
b5	CLKEN_C	Clock Enable for USB_HCLKPM (internal bus—Power Management) 0: Disable 1: Enable	R/W
b4	MIREQ_B	Idle Request to the NoC interconnect for USB Function 0: Active 1: Idle	R/W
b3	CLKEN_B	Clock Enable for USB_HCLKF (Internal bus—USB Function) 0: Disable 1: Enable	R/W
b2	MIREQ_A	Idle Request to the NoC interconnect for USB Host 0: Active 1: Idle	R/W
b1	RSTN_A	Active low Reset for USB_HCLKH domain. If set to 0, reset the NoC interconnect for USB.	R/W
b0	CLKEN_A	Clock Enable for USB_HCLKH (internal bus—USB Host) 0: Disable 1: Enable	R/W

6.3.21 PWRSTAT_USB — Power Management Status for USB2.0

Address: 4000 C020h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_B	MIRACK_B	MISTAT_A	MIRACK_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0

Table 6.24 PWRSTAT_USB Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b4	Reserved		R
b3	MISTAT_B	Idle Status of the NoC interconnect for USB Function 0: Active 1: Idle	R
b2	MIRACK_B	Idle Request Acknowledge for USB Function 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b1	MISTAT_A	Idle Status of the NoC interconnect for USB Host 0: Active 1: Idle	R
b0	MIRACK_A	Idle Request Acknowledge for USB Host 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.22 PWRCTRL_MSEBI — Power Management Control for MSEBI

Address: 4000 C02Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	SLVRDY_B	RSTN_B	CLKEN_B	MIREQ_A	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	0	1	1	1	0	1	1

Table 6.25 PWRCTRL_MSEBI Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b7	Reserved		R
b6	SLVRDY_B	Indicates to the NoC interconnect that the AHBS is ready for MSEBI master access 0: Not Ready 1: Ready	R/W
b5	RSTN_B	Active low Reset for MSEBIM_HCLK domain	R/W
b4	CLKEN_B	Clock Enable for MSEBIM_HCLK 0: Disable 1: Enable	R/W
b3	MIREQ_A	AHBM Idle Request to the NoC interconnect for MSEBI slave 0: Active 1: Idle	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the AHBS is ready for MSEBI slave access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for MSEBIS_HCLK domain	R/W
b0	CLKEN_A	Clock Enable for MSEBIS_HCLK 0: Disable 1: Enable	R/W

6.3.23 PWRSTAT_MSEBI — Power Management Status for MSEBI

Address: 4000 C030h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	SCON_B	MISTAT_A	MIRACK_A	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0

Table 6.26 PWRSTAT_MSEBI Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b4	Reserved		R
b3	SCON_B	NoC Interconnection Status for MSEBI master 0: Disconnected 1: Connected	R
b2	MISTAT_A	AHBM Idle Status of the NoC interconnect for MSEBI slave 0: Active 1: Idle	R
b1	MIRACK_A	AHBM Idle Request Acknowledge for MSEBI slave 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b0	SCON_A	AHBS NoC Interconnection Status for MSEBI slave 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.24 PWRCTRL_PG0_0 — Power Management Control #0 for PG0

Address: 4000 C034h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	UARTCLKSEL	RSTN_J2	CLKEN_J2	RSTN_J1	CLKEN_J1	RSTN_I2	CLKEN_I2	RSTN_I1	CLKEN_I1	RSTN_H2	CLKEN_H2	RSTN_H1	CLKEN_H1	SLVRDY_F	RSTN_F
Value after reset	X	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CLKEN_F	SLVRDY_E	RSTN_E	CLKEN_E	SLVRDY_D	RSTN_D	CLKEN_D	SLVRDY_C	RSTN_C	CLKEN_C	SLVRDY_B	RSTN_B	CLKEN_B	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1

Table 6.27 PWRCTRL_PG0_0 Register Contents (1/2)

Bit Position	Bit Name	Function	R/W
b31	Reserved		R
b30	UARTCLKSEL	Select source of all PG0 UART[m]_SCLK (m = 1..3)*1 0: MAIN PLL (output of the divider controlled by PWRCTRL_PG0_UARTDIV) 1: USB_DCLK48 (48 MHz clock from USBPLL) clock	R/W
b29	RSTN_J2	Active low Reset for UART3_SCLK domain (when USB_DCLK48 is selected).*2	R/W
b28	CLKEN_J2	Clock Enable for UART3_SCLK (when USB_DCLK48 is selected).*2 0: Disable 1: Enable	R/W
b27	RSTN_J1	Active low Reset for UART3_SCLK domain (when MAIN PLL is selected).	R/W
b26	CLKEN_J1	Clock Enable for UART3_SCLK (when MAIN PLL is selected). 0: Disable 1: Enable	R/W
b25	RSTN_I2	Active low Reset for UART2_SCLK domain (when USB_DCLK48 is selected).*2	R/W
b24	CLKEN_I2	Clock Enable for UART2_SCLK (when USB_DCLK48 is selected).*2 0: Disable 1: Enable	R/W
b23	RSTN_I1	Active low Reset for UART2_SCLK domain (when MAIN PLL is selected).	R/W
b22	CLKEN_I1	Clock Enable for UART2_SCLK (when MAIN PLL is selected). 0: Disable 1: Enable	R/W
b21	RSTN_H2	Active low Reset for UART1_SCLK domain (when USB_DCLK48 is selected).*2	R/W
b20	CLKEN_H2	Clock Enable for UART1_SCLK (when USB_DCLK48 is selected).*2 0: Disable 1: Enable	R/W
b19	RSTN_H1	Active low Reset for UART1_SCLK domain (when MAIN PLL is selected).	R/W
b18	CLKEN_H1	Clock Enable for UART1_SCLK (when MAIN PLL is selected). 0: Disable 1: Enable	R/W
b17	SLVRDY_F	Indicates to the NoC interconnect that the ADC is ready for access 0: Not Ready 1: Ready	R/W
b16	RSTN_F	Active low Reset for ADC_PCLK domain	R/W
b15	CLKEN_F	Clock Enable for ADC_PCLK (internal bus) 0: Disable 1: Enable	R/W

Table 6.27 PWRCTRL_PG0_0 Register Contents (2/2)

Bit Position	Bit Name	Function	R/W
b14	SLVRDY_E	Indicates to the NoC interconnect that the I2C2 is ready for access 0: Not Ready 1: Ready	R/W
b13	RSTN_E	Active low Reset for I2C2_PCLK domain	R/W
b12	CLKEN_E	Clock Enable for I2C2_PCLK (internal bus) 0: Disable 1: Enable	R/W
b11	SLVRDY_D	Indicates to the NoC interconnect that the I2C1 is ready for access 0: Not Ready 1: Ready	R/W
b10	RSTN_D	Active low Reset for I2C1_PCLK domain	R/W
b9	CLKEN_D	Clock Enable for I2C1_PCLK (internal bus) 0: Disable 1: Enable	R/W
b8	SLVRDY_C	Indicates to the NoC interconnect that the UART3 is ready for access 0: Not Ready 1: Ready	R/W
b7	RSTN_C	Active low Reset for UART3_PCLK domain	R/W
b6	CLKEN_C	Clock Enable for UART3_PCLK (internal bus) 0: Disable 1: Enable	R/W
b5	SLVRDY_B	Indicates to the NoC interconnect that the UART2 is ready for access 0: Not Ready 1: Ready	R/W
b4	RSTN_B	Active low Reset for UART2_PCLK domain	R/W
b3	CLKEN_B	Clock Enable for UART2_PCLK (internal bus) 0: Disable 1: Enable	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the UART1 is ready for access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for UART1_PCLK domain	R/W
b0	CLKEN_A	Clock Enable for UART1_PCLK (internal bus) 0: Disable 1: Enable	R/W

Note 1. Prior to changing the Clock Multiplexer, the Software shall return both clocks to SW reset values and make sure that the USBPLL is LOCKED.

Note 2. For the proper operation this functionality, the USBPLL shall be locked.

6.3.25 PWRSTAT_PG0 — Power Management Status for PG0

Address: 4000 C038h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SCON_P	—	—	SCON_F	SCON_E	SCON_D	SCON_C	SCON_B	SCON_A
Value after reset	X	X	X	X	X	X	X	0	X	X	0	0	0	0	0	0

Table 6.28 PWRSTAT_PG0 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b9	Reserved		R
b8	SCON_P	NoC Interconnection Status for PWMTimer 0: Disconnected 1: Connected	R
b7 to b6	Reserved		R
b5	SCON_F	NoC Interconnection Status for ADC 0: Disconnected 1: Connected	R
b4	SCON_E	NoC Interconnection Status for I2C2 0: Disconnected 1: Connected	R
b3	SCON_D	NoC Interconnection Status for I2C1 0: Disconnected 1: Connected	R
b2	SCON_C	NoC Interconnection Status for UART3 0: Disconnected 1: Connected	R
b1	SCON_B	NoC Interconnection Status for UART2 0: Disconnected 1: Connected	R
b0	SCON_A	NoC Interconnection Status for UART1 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.26 PWRCTRL_PG0_1 — Power Management Control #1 for PG0

Address: 4000 C03Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	SLVRDY_P	RSTN_P	CLKEN_P	RSTN_M	CLKEN_M	RSTN_L	CLKEN_L	RSTN_K	CLKEN_K	—	—	—	—	—	—
Value after reset	X	0	1	1	1	1	1	1	1	1	X	X	X	X	X	X

Table 6.29 PWRCTRL_PG0_1 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b15	Reserved		R
b14	SLVRDY_P	Indicates to the NoC interconnect that the PWMTimer is ready for access 0: Not Ready 1: Ready	R/W
b13	RSTN_P	Active low Reset for PWM_PCLK domain	R/W
b12	CLKEN_P	Clock Enable for PWM_PCLK (internal bus) 0: Disable 1: Enable	R/W
b11	RSTN_M	Active low Reset for ADC_CLK domain	R/W
b10	CLKEN_M	Clock Enable for ADC_CLK 0: Disable 1: Enable	R/W
b9	RSTN_L	Active low Reset for I2C2_SCLK domain	R/W
b8	CLKEN_L	Clock Enable for I2C2_SCLK 0: Disable 1: Enable	R/W
b7	RSTN_K	Active low Reset for I2C1_SCLK domain	R/W
b6	CLKEN_K	Clock Enable for I2C1_SCLK 0: Disable 1: Enable	R/W
b5 to b0	Reserved		R

6.3.27 PWRCTRL_PG1_1 — Power Management Control #1 for PG1

Address: 4000 C040h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	SLVRDY_J	RSTN_J	CLKEN_J	SLVRDY_I	RSTN_I	CLKEN_I	SLVRDY_H	RSTN_H	CLKEN_H	SLVRDY_G	RSTN_G	CLKEN_G	SLVRDY_F	RSTN_F
Value after reset	X	X	0	1	1	0	1	1	0	1	1	0	1	1	0	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CLKEN_F	SLVRDY_E	RSTN_E	CLKEN_E	SLVRDY_D	RSTN_D	CLKEN_D	SLVRDY_C	RSTN_C	CLKEN_C	SLVRDY_B	RSTN_B	CLKEN_B	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1

Table 6.30 PWRCTRL_PG1_1 Register Contents (1/2)

Bit Position	Bit Name	Function	R/W
b31, b30	Reserved		R
b29	SLVRDY_J	Indicates to the NoC interconnect that the UART5 is ready for access 0: Not Ready 1: Ready	R/W
b28	RSTN_J	Active low Reset for UART5_PCLK domain	R/W
b27	CLKEN_J	Clock Enable for UART5_PCLK (internal bus) 0: Disable 1: Enable	R/W
b26	SLVRDY_I	Indicates to the NoC interconnect that the UART4 is ready for access 0: Not Ready 1: Ready	R/W
b25	RSTN_I	Active low Reset for UART4_PCLK domain	R/W
b24	CLKEN_I	Clock Enable for UART4_PCLK (internal bus) 0: Disable 1: Enable	R/W
b23	SLVRDY_H	Indicates to the NoC interconnect that the BGPIO2 is ready for access 0: Not Ready 1: Ready	R/W
b22	RSTN_H	Active low Reset for BGPIO2_PCLK domain	R/W
b21	CLKEN_H	Clock Enable for BGPIO2_PCLK (internal bus) 0: Disable 1: Enable	R/W
b20	SLVRDY_G	Indicates to the NoC interconnect that the BGPIO1 is ready for access 0: Not Ready 1: Ready	R/W
b19	RSTN_G	Active low Reset for BGPIO1_PCLK domain	R/W
b18	CLKEN_G	Clock Enable for BGPIO1_PCLK (internal bus) 0: Disable 1: Enable	R/W
b17	SLVRDY_F	Indicates to the NoC interconnect that the SPI6 is ready for access 0: Not Ready 1: Ready	R/W
b16	RSTN_F	Active low Reset for SPI6_PCLK domain	R/W
b15	CLKEN_F	Clock Enable for SPI6_PCLK (internal bus) 0: Disable 1: Enable	R/W

Table 6.30 PWRCTRL_PG1_1 Register Contents (2/2)

Bit Position	Bit Name	Function	R/W
b14	SLVRDY_E	Indicates to the NoC interconnect that the SPI5 is ready for access 0: Not Ready 1: Ready	R/W
b13	RSTN_E	Active low Reset for SPI5_PCLK domain	R/W
b12	CLKEN_E	Clock Enable for SPI5_PCLK (internal bus) 0: Disable 1: Enable	R/W
b11	SLVRDY_D	Indicates to the interconnect that the SPI4 is ready for access 0: Not Ready 1: Ready	R/W
b10	RSTN_D	Active low Reset for SPI4_PCLK domain	R/W
b9	CLKEN_D	Clock Enable for SPI4_PCLK (internal bus) 0: Disable 1: Enable	R/W
b8	SLVRDY_C	Indicates to the NoC interconnect that the SPI3 is ready for access 0: Not Ready 1: Ready	R/W
b7	RSTN_C	Active low Reset for SPI3_PCLK domain	R/W
b6	CLKEN_C	Clock Enable for SPI3_PCLK (internal bus) 0: Disable 1: Enable	R/W
b5	SLVRDY_B	Indicates to the NoC interconnect that the SPI2 is ready for access 0: Not Ready 1: Ready	R/W
b4	RSTN_B	Active low Reset for SPI2_PCLK domain	R/W
b3	CLKEN_B	Clock Enable for SPI2_PCLK (internal bus) 0: Disable 1: Enable	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the SPI1 is ready for access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for SPI1_PCLK domain	R/W
b0	CLKEN_A	Clock Enable for SPI1_PCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.28 PWRCTRL_PG1_2 — Power Management Control #2 for PG1

Address: 4000 C044h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SLVRDY_N	RSTN_N	CLKEN_N	SLVRDY_M	RSTN_M	CLKEN_M	SLVRDY_L	RSTN_L	CLKEN_L	SLVRDY_K	RSTN_K	CLKEN_K
Value after reset	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1

Table 6.31 PWRCTRL_PG1_2 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b18	Reserved		R
b17 to b12	Reserved	Keep initial value	R/W
b11	SLVRDY_N	Indicates to the NoC interconnect that the BGPIO3 is ready for access 0: Not Ready 1: Ready	R/W
b10	RSTN_N	Active low Reset for BGPIO3_PCLK domain	R/W
b9	CLKEN_N	Clock Enable for BGPIO3_PCLK (internal bus) 0: Disable 1: Enable	R/W
b8	SLVRDY_M	Indicates to the NoC interconnect that the UART8 is ready for access 0: Not Ready 1: Ready	R/W
b7	RSTN_M	Active low Reset for UART8_PCLK domain	R/W
b6	CLKEN_M	Clock Enable for UART8_PCLK (internal bus) 0: Disable 1: Enable	R/W
b5	SLVRDY_L	Indicates to the NoC interconnect that the UART7 is ready for access 0: Not Ready 1: Ready	R/W
b4	RSTN_L	Active low Reset for UART7_PCLK domain	R/W
b3	CLKEN_L	Clock Enable for UART7_PCLK (internal bus) 0: Disable 1: Enable	R/W
b2	SLVRDY_K	Indicates to the NoC interconnect that the UART6 is ready for access 0: Not Ready 1: Ready	R/W
b1	RSTN_K	Active low Reset for UART6_PCLK domain	R/W
b0	CLKEN_K	Clock Enable for UART6_PCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.29 PWRCTRL_DMA — Power Management Control for DMAC1 & DMAC2

Address: 4000 C04Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	MIREQ_B	SLVRDY_B	RSTN_B	CLKEN_B	MIREQ_A	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	1	0	1	1	1	0	1	1

Table 6.32 PWRCTRL_DMA Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b8	Reserved		R
b7	MIREQ_B	AHBM Idle Request to the NoC interconnect for DMAC2 0: Active 1: Idle	R/W
b6	SLVRDY_B	Indicates to the NoC interconnect that the AHBS is ready for DMAC2 access 0: Not Ready 1: Ready	R/W
b5	RSTN_B	Active low Reset for DMA2_HCLK domain	R/W
b4	CLKEN_B	Clock Enable for DMA2_HCLK (internal bus) 0: Disable 1: Enable	R/W
b3	MIREQ_A	AHBM Idle Request to the NoC interconnect for DMAC1 0: Active 1: Idle	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the AHBS is ready for DMAC1 access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for DMA1_HCLK domain	R/W
b0	CLKEN_A	Clock Enable for DMA1_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.30 PWRCTRL_NFLASH — Power Management Control for NAND FLASH Controller

Address: 4000 C050h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	RSTN_B	CLKEN_B	MIREQ_A	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	1	1	1	0	1	1

Table 6.33 PWRCTRL_NFLASH Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b6	Reserved		R
b5	RSTN_B	Active low Reset for NAND_ECLK domain	R/W
b4	CLKEN_B	Clock Enable for NAND_ECLK (external interface) 0: Disable 1: Enable	R/W
b3	MIREQ_A	AHBM Idle Request to the NoC interconnect for NAND Flash Controller 0: Active 1: Idle	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the AHBS is ready for NAND Flash Controller access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for NAND_HCLK domain	R/W
b0	CLKEN_A	Clock Enable for NAND_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.31 PWRCTRL_QSPI1 — Power Management Control for QSPI1

Address: 4000 C054h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	RSTN_B	CLKEN_B	MIREQ_A	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	1	1	1	0	1	1

Table 6.34 PWRCTRL_QSPI1 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b6	Reserved		R
b5	RSTN_B	Active low Reset for QSPI1_REFCLK domain	R/W
b4	CLKEN_B	Clock Enable for QSPI1_REFCLK (external interface) 0: Disable 1: Enable	R/W
b3	MIREQ_A	AHBS Idle Request to the NoC interconnect for QuadSPI1 0: Active 1: Idle	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the APBS is ready for QuadSPI1 access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for QSPI1_HCLK/QSPI1_PCLK domain	R/W
b0	CLKEN_A	Clock Enable for QSPI1_HCLK, QSPI1_PCLK (internal bus) 0: Disable 1: Enable	R/W

NOTE

Reset shall be initiated during QSPI1 module is in process. In case of RZ/N1L, this register initial value is 0x37.

6.3.32 PWRSTAT_DMA — Power Management Status for DMAC1 & DMAC2

Address: 4000 C058h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	MISTAT_B	MIRACK_B	SCON_B	MISTAT_A	MIRACK_A	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0

Table 6.35 PWRSTAT_DMA Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b6	Reserved		R
b5	MISTAT_B	AHBM Idle Status of the NoC interconnect for DMAC2 0: Active 1: Idle	R
b4	MIRACK_B	AHBM Idle Request Acknowledge for DMAC2 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b3	SCON_B	AHBS NoC Interconnection Status for DMAC2 0: Disconnected 1: Connected	R
b2	MISTAT_A	AHBM Idle Status of the NoC interconnect for DMAC1 0: Active 1: Idle	R
b1	MIRACK_A	AHBM Idle Request Acknowledge for DMAC1 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b0	SCON_A	AHBS NoC Interconnection Status for DMAC1 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.33 PWRSTAT_NFLASH — Power Management Status for NAND FLASH Controller

Address: 4000 C05Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0

Table 6.36 PWRSTAT_NFLASH Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	MISTAT_A	AHBM Idle Status of the NoC interconnect for NAND Flash Controller 0: Active 1: Idle	R
b1	MIRACK_A	AHBM Idle Request Acknowledge for NAND Flash Controller 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b0	SCON_A	AHBS NoC Interconnection Status for NAND Flash Controller 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.34 PWRSTAT_QSPI1 — Power Management Status for QSPI1

Address: 4000 C060h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0

Table 6.37 PWRSTAT_QSPI1 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	MISTAT_A	AHBS Idle Status of the NoC interconnect for QSPI1 0: Active 1: Idle	R
b1	MIRACK_A	AHBS Idle Request Acknowledge for QSPI1 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b0	SCON_A	APBS NoC Interconnection Status for QSPI1 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.35 PWRCTRL_DDRC — Power Management Control for DDR Memory Controller

Address: 4000 C064h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	RSTN_B	CLKEN_B	RSTN_A	MIREQ_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1	1

Table 6.38 PWRCTRL_DDRC Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b5	Reserved		R
b4	RSTN_B	Active low Reset for DDR_DFICLK domain.	R/W
b3	CLKEN_B	Clock Enable for DDR_DFICLK 0: Disable 1: Enable	R/W
b2	RSTN_A	Active low Reset for DDR_XCLK domain	R/W
b1	MIREQ_A	Idle Request to the NoC interconnect for DDR memory controller 0: Active 1: Idle	R/W
b0	CLKEN_A	Clock Enable for DDR_XCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.36 PWRCTRL_EETH — Power Management Control for External Ethernet Clock

Address: 4000 C068h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKEN_C	CLKEN_B	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1

Table 6.39 PWRCTRL_EETH Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	CLKEN_C	Clock Enable for MII_REFCLK (External output) 0: Disable 1: Enable	R/W
b1	CLKEN_B	Clock Enable for RMII_REFCLK (External output) 0: Disable 1: Enable	R/W
b0	CLKEN_A	Clock Enable for RGMII_REFCLK (External input) 0: Disable 1: Enable	R/W

6.3.37 PWRCTRL_MAC1 — Power Management Control for GMAC1

Address: 4000 C06Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	MIREQ_A	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	1

Table 6.40 PWRCTRL_MAC1 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b4	Reserved		R
b3	MIREQ_A	AXIM Idle Request to the NoC interconnect for GMAC1 0: Active 1: Idle	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the AHBS is ready for GMAC1 access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for GMAC1_XCLK/GMAC1_HCLK domain	R/W
b0	CLKEN_A	Clock Enable for GMAC1_XCLK, GMAC1_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.38 PWRCTRL_MAC2 — Power Management Control for GMAC2

Address: 4000 C070h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	MIREQ_A	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	1

Table 6.41 PWRCTRL_MAC2 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b4	Reserved		R
b3	MIREQ_A	AXIM Idle Request to the NoC interconnect for GMAC2 0: Active 1: Idle	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the AHBS is ready for GMAC2 access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for GMAC2_XCLK/GMAC2_HCLK domain	R/W
b0	CLKEN_A	Clock Enable for GMAC2_XCLK, GMAC2_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.39 PWRSTAT_DDRC — Power Management Status for DDR Memory Controller

Address: 4000 C074h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0

Table 6.42 PWRSTAT_DDRC Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b2	Reserved		R
b1	MISTAT_A	Idle Status of the NoC interconnect for DDR memory controller 0: Active 1: Idle	R
b0	MIRACK_A	Idle Request Acknowledge for DDR memory controller 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.40 PWRSTAT_MAC1 — Power Management Status for GMAC1

Address: 4000 C078h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0

Table 6.43 PWRSTAT_MAC1 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	MISTAT_A	AXIM Idle Status of the NoC interconnect for GMAC1 0: Active 1: Idle	R
b1	MIRACK_A	AXIM Idle Request Acknowledge for GMAC1 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b0	SCON_A	AHBS NoC Interconnection Status for GMAC1 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.41 PWRSTAT_MAC2 — Power Management Status for GMAC2

Address: 4000 C07Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0

Table 6.44 PWRSTAT_MAC2 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	MISTAT_A	AXIM Idle Status of the NoC interconnect for GMAC2 0: Active 1: Idle	R
b1	MIRACK_A	AXIM Idle Request Acknowledge for GMAC2 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b0	SCON_A	AHBS NoC Interconnection Status for GMAC2 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.42 PWRCTRL_ECAT — Power Management Control for ETHERCAT

Address: 4000 C080h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	CLKEN_C	RSTN_B	CLKEN_B	MIREQ_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	1	0	1	1	0	1

Table 6.45 PWRCTRL_ECAT Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b6	Reserved		R
b5	CLKEN_C	Clock Enable for ECAT_CLK100 0: Disable 1: Enable	R/W
b4	RSTN_B	Active low Reset for ECAT_CLK25 domain	R/W
b3	CLKEN_B	Clock Enable for ECAT_CLK25 0: Disable 1: Enable	R/W
b2	MIREQ_A	Idle Request to the NoC interconnect for ETHERCAT 0: Active 1: Idle	R/W
b1	RSTN_A	Active low Reset for ECAT_HCLK domain	R/W
b0	CLKEN_A	Clock Enable for ECAT_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.43 PWRCTRL_SERCOS — Power Management Control for SERCOSIII

Address: 4000 C084h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	CLKEN_C	CLKEN_B	RSTN_B	RSTN_A	MIREQ_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	1	1	0	0	1	1

Table 6.46 PWRCTRL_SERCOS Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b6	Reserved		R
b5	CLKEN_C	Clock Enable for SERCOS_CLK100 0: Disable 1: Enable	R/W
b4	CLKEN_B	Clock Enable for SERCOS_CLK50 0: Disable 1: Enable	R/W
b3	RSTN_B	Active low Reset for SERCOS_CLK50 domain	R/W
b2	RSTN_A	Active low Reset for SERCOS_HCLK domain	R/W
b1	MIREQ_A	Idle Request to the NoC interconnect for SERCOSIII 0: Active 1: Idle	R/W
b0	CLKEN_A	Clock Enable for SERCOS_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.44 PWRSTAT_ECAT — Power Management Status for ETHERCAT

Address: 4000 C088h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0

Table 6.47 PWRSTAT_ECAT Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b2	Reserved		R
b1	MISTAT_A	Idle Status of the NoC interconnect for ETHERCAT 0: Active 1: Idle	R
b0	MIRACK_A	Idle Request Acknowledge for ETHERCAT 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.45 PWRSTAT_SERCOS — Power Management Status for SERCOSIII

Address: 4000 C08Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0

Table 6.48 PWRSTAT_SERCOS Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b2	Reserved		R
b1	MISTAT_A	Idle Status of the NoC interconnect for SERCOSIII 0: Active 1: Idle	R
b0	MIRACK_A	Idle Request Acknowledge for SERCOSIII 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.46 PWRCTRL_HSR — Power Management Control for HSR

Address: 4000 C090h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	RSTN_C	CLKEN_C	CLKEN_B	RSTN_A	MIREQ_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	0	1	1	0	1	1

Table 6.49 PWRCTRL_HSR Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b6	Reserved		R
b5	RSTN_C	Active low Reset for HSR_CLK50 domain	R/W
b4	CLKEN_C	Clock Enable for HSR_CLK50 0: Disable 1: Enable	R/W
b3	CLKEN_B	Clock Enable for HSR_CLK100 0: Disable 1: Enable	R/W
b2	RSTN_A	Active low Reset for HSR_HCLK domain	R/W
b1	MIREQ_A	Idle Request to the NoC interconnect for HSR 0: Active 1: Idle	R/W
b0	CLKEN_A	Clock Enable for HSR_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.47 PWRCTRL_QSPI2 — Power Management Control for QSPI2

Address: 4000 C090h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	RSTN_B	CLKEN_B	MIREQ_A	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	1	1	1	0	1	1

Table 6.50 PWRCTRL_QSPI2 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b6	Reserved		R
b5	RSTN_B	Active low Reset for QSPI2_REFCLK	R/W
b4	CLKEN_B	Clock Enable for QSPI2_REFCLK (external interface) 0: Disable 1: Enable	R/W
b3	MIREQ_A	AHBS Idle Request to the NoC interconnect for QuadSPI2 0: Active 1: Idle	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the APBS is ready for QuadSPI2 access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for QSPI2_HCLK/QSPI2_PCLK domain	R/W
b0	CLKEN_A	Clock Enable for QSPI2_HCLK, QSPI2_PCLK (internal bus) 0: Disable 1: Enable	R/W

NOTE

Reset shall be initiated during QSPI2 module is in process.

6.3.48 PWRSTAT_HSR — Power Management Status for HSR

Address: 4000 C098h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0

Table 6.51 PWRSTAT_HSR Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b2	Reserved		R
b1	MISTAT_A	Idle Status of the NoC interconnect for HSR 0: Active 1: Idle	R
b0	MIRACK_A	Idle Request Acknowledge for HSR 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.49 PWRSTAT_QSPI2 — Power Management Status for QSPI2

Address: 4000 C098h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0

Table 6.52 PWRSTAT_QSPI2 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	MISTAT_A	AHBS Idle Status of the NoC interconnect for QSPI2 0: Active 1: Idle	R
b1	MIRACK_A	AHBS Idle Request Acknowledge for QSPI2 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b0	SCON_A	APBS NoC Interconnection Status for QSPI2 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.50 PWRSTAT_SWITCH — Power Management Status for A5PSW

Address: 4000 C09Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0

Table 6.53 PWRSTAT_SWITCH Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b1	Reserved		R
b0	SCON_A	NoC Interconnection Status for A5PSW 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.51 RSTSTAT — Reset Status Register

Address: 4000 C0A8h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PORRST_ST	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	SWRST_ST	CM3SYSRESET_ST	CM3LOCKUPRST_ST	WDM3RST_ST	WDA7RST_ST		—
Value after reset	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	X

Table 6.54 RSTSTAT Register Contents

Bit Position	Bit Name	Function	R/W
b31	PORRST_ST	Status bit whether or not external (power-on) reset has been performed 0: External (power-on) reset has not been performed. 1: External (power-on) reset is performed.	R/W
b30 to b7	Reserved		R
b6	SWRST_ST	Status bit of Software reset 0: Software triggered reset has not been performed. 1: Software triggered reset is performed.	R/W
b5	CM3SYSRESET_ST	Status bit of Cortex-M3 initiated system reset 0: Cortex-M3 triggered system reset has not been performed. 1: Cortex-M3 triggered system reset is performed.	R/W
b4	CM3LOCKUPRST_ST	Status bit of Cortex-M3 Core Lockup initiated system reset 0: Cortex-M3 Lockup triggered system reset has not been performed. 1: Cortex-M3 Lockup triggered system reset is performed.	R/W
b3	WDM3RST_ST	Status bit of Cortex-M3 watchdog initiated system reset; If a software failure prevents the Watchdog Counter Register from being refreshed, the Watchdog Counter Register reaches zero, the Watchdog reset status flag is set and the associated reset request is asserted. 0: Device has not performed any watchdog triggered system reset. 1: Device has performed a watchdog triggered system reset.	R/W
b2, b1	WDA7RST_ST	Status bit of Cortex-A7 watchdog initiated system reset 0: Watchdog triggered system reset has not been performed. 1: Watchdog triggered system reset is performed. Bit2 (RZ/N1D) Cortex-A7 processor1 watchdog reset (RZ/N1S, RZ/N1L) Reserved Bit1 (RZ/N1D, RZ/N1S) Cortex-A7 processor0 watchdog reset (RZ/N1L) Reserved	R/W
b0	Reserved		R

NOTE

These status bits are cleared by write 1.

6.3.52 USBSTAT — Status information for USBPLL

Address: 4000 C0C0h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PLL_LOCK
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0

Table 6.55 USBSTAT Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b1	Reserved		R
b0	PLL_LOCK	Status of USBPLL 0: UNLOCKED 1: LOCKED	R

NOTE

Software shall make sure that the USBPLL is locked prior to initiating any access to peripherals running on USBPLL clock. Otherwise the system may hang-up.

CAUTION

USBPLL is unlocked by specific register access (e.g. PLL_RST) to USB module or resetting the USB module.

6.3.53 PWRCTRL_SDIO2 — Power Management Control for SDIO2

Address: 4000 C0C8h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CLKEN_B	MIREQ_A	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	1	1	0	1	1

Table 6.56 PWRCTRL_SDIO2 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b5	Reserved		R
b4	CLKEN_B	Clock Enable for SDIO2_ECLK (external interface) 0: Disable 1: Enable	R/W
b3	MIREQ_A	AHBM Idle Request to the NoC interconnect for SDIO2 0: Active 1: Idle	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the AHBS is ready for SDIO2 access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for SDIO2_HCLK domain	R/W
b0	CLKEN_A	Clock Enable for SDIO2_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.54 PWRSTAT_SDIO2 — Power Management Status for SDIO2

Address: 4000 C0CCh

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0

Table 6.57 PWRSTAT_SDIO2 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	MISTAT_A	AHBM Idle Status of the NoC interconnect for SDIO2 0: Active 1: Idle	R
b1	MIRACK_A	AHBM Idle Request Acknowledge for SDIO2 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b0	SCON_A	AHBS NoC Interconnection Status for SDIO2 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.55 PWRCTRL_PG2_25MHZ — Power Management Control for PG2 25MHz

Address: 4000 C0E8h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	0	1	1	0	1	1	0	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SLVRDY_S	RSTN_S	CLKEN_S	SLVRDY_R	RSTN_R	CLKEN_R	SLVRDY_Q	RSTN_Q	CLKEN_Q
Value after reset	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1

Table 6.58 PWRCTRL_PG2_25MHZ Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b24	Reserved		R
b23 to b9	Reserved	Keep initial value	R/W
b8	SLVRDY_S	Indicates to the NoC interconnect that the TIMER2 is ready for access 0: Not Ready 1: Ready	R/W
b7	RSTN_S	Active low Reset for TIMER2_PCLK domain	R/W
b6	CLKEN_S	Clock Enable for TIMER2_PCLK (internal bus) 0: Disable 1: Enable	R/W
b5	SLVRDY_R	Indicates to the NoC interconnect that the TIMER1 is ready for access 0: Not Ready 1: Ready	R/W
b4	RSTN_R	Active low Reset for TIMER1_PCLK domain	R/W
b3	CLKEN_R	Clock Enable for TIMER1_PCLK (internal bus) 0: Disable 1: Enable	R/W
b2	SLVRDY_Q	Indicates to the NoC interconnect that the ConfigSys2 is ready for access 0: Not Ready 1: Ready	R/W
b1	RSTN_Q	Active low Reset for PG2_PCLK domain	R/W
b0	CLKEN_Q	Clock Enable for PG2_PCLK (internal bus of ConfigSys2) 0: Disable 1: Enable	R/W

6.3.56 PWRCTRL_PG1_PR2 — Power Management Control for PG1 Program2

Address: 4000 C0ECh

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	UARTCLKSEL	—	—	—	—	RSTN_AK2	CLKEN_AK2	RSTN_AK1	CLKEN_AK1
Value after reset	X	X	X	X	X	X	X	0	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RSTN_AJ2	CLKEN_AJ2	RSTN_AJ1	CLKEN_AJ1	RSTN_AI2	CLKEN_AI2	RSTN_AI1	CLKEN_AI1	RSTN_AH2	CLKEN_AH2	RSTN_AH1	CLKEN_AH1	RSTN_AG2	CLKEN_AG2	RSTN_AG1	CLKEN_AG1
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 6.59 PWRCTRL_PG1_PR2 Register Contents (1/2)

Bit Position	Bit Name	Function	R/W
b31 to b25	Reserved		R
b24	UARTCLKSEL	Select source of all PG1 UART[m]_SCLK (m = 4..8)*1 0: MAIN PLL (output of the divider controlled by PWRCTRL_PG1_PR2DIV) 1: USB_DCLK48 (48 MHz clock from USBPLL) clock.	R/W
b23 to b20	Reserved	Keep initial value.	R/W
b19	RSTN_AK2	Active low Reset for UART8_SCLK domain (when USB_DCLK48 is selected).*2	R/W
b18	CLKEN_AK2	Clock Enable for UART8_SCLK (when USB_DCLK48 is selected).*2 0: Disable 1: Enable	R/W
b17	RSTN_AK1	Active low Reset for UART8_SCLK domain (when MAIN PLL is selected).	R/W
b16	CLKEN_AK1	Clock Enable for UART8_SCLK (when MAIN PLL is selected). 0: Disable 1: Enable	R/W
b15	RSTN_AJ2	Active low Reset for UART7_SCLK domain (when USB_DCLK48 is selected).*2	R/W
b14	CLKEN_AJ2	Clock Enable for UART7_SCLK (when USB_DCLK48 is selected).*2 0: Disable 1: Enable	R/W
b13	RSTN_AJ1	Active low Reset for UART7_SCLK domain (when MAIN PLL is selected).	R/W
b12	CLKEN_AJ1	Clock Enable for UART7_SCLK (when MAIN PLL is selected). 0: Disable 1: Enable	R/W
b11	RSTN_AI2	Active low Reset for UART6_SCLK domain (when USB_DCLK48 is selected).*2	R/W
b10	CLKEN_AI2	Clock Enable for UART6_SCLK (when USB_DCLK48 is selected).*2 0: Disable 1: Enable	R/W
b9	RSTN_AI1	Active low Reset for UART6_SCLK domain (when MAIN PLL is selected).	R/W
b8	CLKEN_AI1	Clock Enable for UART6_SCLK (when MAIN PLL is selected). 0: Disable 1: Enable	R/W

Table 6.59 PWRCTRL_PG1_PR2 Register Contents (2/2)

Bit Position	Bit Name	Function	R/W
b7	RSTN_AH2	Active low Reset for UART5_SCLK domain (when USB_DCLK48 is selected).*2	R/W
b6	CLKEN_AH2	Clock Enable for UART5_SCLK (when USB_DCLK48 is selected).*2 0: Disable 1: Enable	R/W
b5	RSTN_AH1	Active low Reset for UART5_SCLK domain (when MAIN PLL is selected).	R/W
b4	CLKEN_AH1	Clock Enable for UART5_SCLK (when MAIN PLL is selected). 0: Disable 1: Enable	R/W
b3	RSTN_AG2	Active low Reset for UART4_SCLK domain (when USB_DCLK48 is selected).*2	R/W
b2	CLKEN_AG2	Clock Enable for UART4_SCLK (when USB_DCLK48 is selected).*2 0: Disable 1: Enable	R/W
b1	RSTN_AG1	Active low Reset for UART4_SCLK domain (when MAIN PLL is selected).	R/W
b0	CLKEN_AG1	Clock Enable for UART4_SCLK (when MAIN PLL is selected). 0: Disable 1: Enable	R/W

Note 1. Prior to changing the Clock Multiplexer, the Software shall return both clocks to SW reset values and make sure that the USBPLL is LOCKED.

Note 2. For the proper operation of this function, the USBPLL shall be locked.

6.3.57 PWRCTRL_PG3_48MHZ — Power Management Control for PG3 48MHz

CAUTION

The USBPLL shall be locked prior to making any access to Peripheral Group 3. Otherwise the system may hang-up.

Address: 4000 C0F0h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIREQ_UF	RSTN_UF	CLKEN_UF	—	—	—	SLVRDY_AA	RSTN_AA	CLKEN_AA	SLVRDY_Z	RSTN_Z	CLKEN_Z	—	—	—
Value after reset	X	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1

Table 6.60 PWRCTRL_PG3_48MHZ Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b15	Reserved		R
b14	MIREQ_UF	Idle Request to the NoC interconnect for Peripheral Group 3 0: Active 1: Idle	R/W
b13	RSTN_UF	Active low Reset for Peripheral Group 3	R/W
b12	CLKEN_UF	Clock Enable for Peripheral Group 3 0: Disable 1: Enable	R/W
b11 to b9	Reserved	Keep initial value.	R/W
b8	SLVRDY_AA	Indicates to the NoC interconnect that the CAN2 is ready for access 0: Not Ready 1: Ready	R/W
b7	RSTN_AA	Active low Reset for CAN2_HCLK domain	R/W
b6	CLKEN_AA	Clock Enable for CAN2_HCLK (internal bus) 0: Disable 1: Enable	R/W
b5	SLVRDY_Z	Indicates to the NoC interconnect that the CAN1 is ready for access 0: Not Ready 1: Ready	R/W
b4	RSTN_Z	Active low Reset for CAN1_HCLK domain	R/W
b3	CLKEN_Z	Clock Enable for CAN1_HCLK (internal bus) 0: Disable 1: Enable	R/W
b2 to b0	Reserved	Keep initial value	R/W

6.3.58 PWRCTRL_PG4 — Power Management Control for PG4

Address: 4000 C0F4h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIREQ_UI	RSTN_UI	CLKEN_UI	—	—	—	—	—	—	SLVRDY_AD	RSTN_AD	CLKEN_AD	SLVRDY_AC	RSTN_AC	CLKEN_AC
Value after reset	X	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1

Table 6.61 PWRCTRL_PG4 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b15	Reserved		R
b14	MIREQ_UI	Idle Request to the NoC interconnect for Peripheral Group 4 0: Active 1: Idle	R/W
b13	RSTN_UI	Active low Reset for Peripheral Group 4	R/W
b12	CLKEN_UI	Clock Enable for Peripheral Group 4 0: Disable 1: Enable	R/W
b11 to b6	Reserved	Keep initial value	R/W
b5	SLVRDY_AD	Indicates to the NoC interconnect that the Semaphore is ready for access 0: Not Ready 1: Ready	R/W
b4	RSTN_AD	Active low Reset for SEMAP_HCLK domain	R/W
b3	CLKEN_AD	Clock Enable for SEMAP_HCLK (internal bus) 0: Disable 1: Enable	R/W
b2	SLVRDY_AC	Indicates to the NoC interconnect that the LCDC is ready for access 0: Not Ready 1: Ready	R/W
b1	RSTN_AC	Active low Reset for LCD_HCLK domain	R/W
b0	CLKEN_AC	Clock Enable for LCD_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.59 PWRCTRL_PG1_PR3 — Power Management Control for PG1 Program3

Address: 4000 C0FCh

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RSTN_AP	CLKEN_AP	RSTN_AO	CLKEN_AO	RSTN_AN	CLKEN_AN	RSTN_AM	CLKEN_AM
Value after reset	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1

Table 6.62 PWRCTRL_PG1_PR3 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b8	Reserved		R
b7	RSTN_AP	Active low Reset for SPI4_SCLK domain	R/W
b6	CLKEN_AP	Clock Enable for SPI4_SCLK (external interface) 0: Disable 1: Enable	R/W
b5	RSTN_AO	Active low Reset for SPI3_SCLK domain	R/W
b4	CLKEN_AO	Clock Enable for SPI3_SCLK (external interface) 0: Disable 1: Enable	R/W
b3	RSTN_AN	Active low Reset for SPI2_SCLK domain	R/W
b2	CLKEN_AN	Clock Enable for SPI2_SCLK (external interface) 0: Disable 1: Enable	R/W
b1	RSTN_AM	Active low Reset for SPI1_SCLK domain	R/W
b0	CLKEN_AM	Clock Enable for SPI1_SCLK (external interface) 0: Disable 1: Enable	R/W

6.3.60 PWRCTRL_PG1_PR4 — Power Management Control for PG1 Program4

Address: 4000 C104h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	RSTN_AR	CLKEN_AR	RSTN_AQ	CLKEN_AQ
Value after reset	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1

Table 6.63 PWRCTRL_PG1_PR4 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b8	Reserved		R
b7 to b4	Reserved	Keep initial value	R/W
b3	RSTN_AR	Active low Reset for SPI6_SCLK domain	R/W
b2	CLKEN_AR	Clock Enable for SPI6_SCLK (external interface) 0: Disable 1: Enable	R/W
b1	RSTN_AQ	Active low Reset for SPI5_SCLK domain	R/W
b0	CLKEN_AQ	Clock Enable for SPI5_SCLK (external interface) 0: Disable 1: Enable	R/W

6.3.61 PWRCTRL_PG4_PR1 — Power Management Control for PG4 Program1

Address: 4000 C10Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RSTN_AU	CLKEN_AU
Value after reset	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1

Table 6.64 PWRCTRL_PG4_PR1 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b8	Reserved		R
b7 to b2	Reserved	Keep initial value	R/W
b1	RSTN_AU	Active low Reset for LCD_ECLK domain	R/W
b0	CLKEN_AU	Clock Enable for LCD_ECLK (external interface) 0: Disable 1: Enable	R/W

6.3.62 RSTEN — Reset Enable Register

This Register can enable or disable each system reset source. Enabling an active system reset request (in RSTCTRL) will result in immediate reset of the system.

Address: 4000 C120h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	SWRST_EN	CM3SYSRESET_EN	CM3LOCKUPRST_EN	WDM3RST_EN	WDA7RST_EN		MRESET_EN
Value after reset	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0

Table 6.65 RSTEN Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b7	Reserved		R
b6	SWRST_EN	Enable bit of Software triggered system reset request (SWRST_REQ bit of RSTCTRL register) 0: Disable 1: Enable	R/W
b5	CM3SYSRESET_EN	Enable Cortex-M3 SYSRESETREQ initiated reset 0: Disable 1: Enable	R/W
b4	CM3LOCKUPRST_EN	Enable bit of Cortex-M3 Core Lockup reset 0: Disable 1: Enable	R/W
b3	WDM3RST_EN	Enable bit of Cortex-M3 Core watchdog reset 0: Disable 1: Enable	R/W
b2, b1	WDA7RST_EN	Enable bit of Cortex-A7 watchdog reset 0: Disable 1: Enable Bit2 (RZ/N1D) Cortex-A7 processor1 watchdog reset request (RZ/N1S, RZ/N1L) Reserved. Bit1 (RZ/N1D, RZ/N1S) Cortex-A7 processor0 watchdog reset request (RZ/N1L) Reserved.	R/W
b0	MRESET_EN	Enable bit of system reset Bit6..1 are activated if this bit is set to 1.	R/W

6.3.63 PWRCTRL_SWITCH — Power Management Control for A5PSW

Address: 4000 C130h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	RSTN_B	CLKEN_B	SLVRDY_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	1

Table 6.66 PWRCTRL_SWITCH Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b4	Reserved		R
b3	RSTN_B	Active low Reset for A5PSW_SXCLK domain	R/W
b2	CLKEN_B	Clock Enable for A5PSW_SXCLK (core clock) 0: Disable 1: Enable	R/W
b1	SLVRDY_A	Indicates to the NoC interconnect that the A5PSW is ready for access 0: Not Ready 1: Ready	R/W
b0	CLKEN_A	Clock Enable for A5PSW_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.64 PWRCTRL_RTC — Power Management Control for RTC

Use below order to enable RTC for software access:

1. Release RST_RTC
2. Enable RTC_PCLK
3. Release RSTN_FW_RTC
4. Release IDLE_REQ

Address: 4000 C140h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	RSTN_FW_RTC	IDLE_REQ	RST_RTC	CLKEN_RTC
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	0

Table 6.67 PWRCTRL_RTC Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b4	Reserved		R
b3	RSTN_FW_RTC	Software reset to the NoC interconnect for RTC 0: Reset 1: Reset release	R/W
b2	IDLE_REQ	Idle Request to the NoC interconnect for RTC 1: IDLE-status request 0: Active status	R/W
b1	RST_RTC	Active high Reset for RTC_PCLK domain 1: Reset 0: Reset release	R/W
b0	CLKEN_RTC	Clock Enable for RTC_PCLK (internal bus) 1: CLK for RTC APB and NoC interconnect on 0: CLK off	R/W

6.3.65 PWRSTAT_RTC — Power Management Status for RTC

Address: 4000 C144h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	PWR_GOOD	RTC_IDLE	RTC_IACK
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0

Table 6.68 PWRSTAT_RTC Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	PWR_GOOD	Indicate status of RTC_PWRGOOD signal	R
b1	RTC_IDLE	Idle Status of the NoC interconnect for RTC 0: Active 1: Idle	R
b0	RTC_IACK	Idle Request Acknowledge for RTC 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R

NOTE

The software shall not apply clock gating or software reset unless idle (RTC_IDLE = 1).

6.3.66 PWRCTRL_ROM — Power Management Control for ROM

Address: 4000 C154h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1

Table 6.69 PWRCTRL_ROM Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	SLVRDY_A	Indicates to the NoC interconnect that the ROM is ready for access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for ROM_HCLK domain	R/W
b0	CLKEN_A	Clock Enable for ROM_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.67 PWRSTAT_PG1 — Power Management Status for PG1

Address: 4000 C158h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SCON_N	SCON_M	SCON_L	SCON_K	SCON_J	SCON_I	SCON_H	SCON_G	SCON_F	SCON_E	SCON_D	SCON_C	SCON_B	SCON_A
Value after reset	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6.70 PWRSTAT_PG1 Register Contents (1/2)

Bit Position	Bit Name	Function	R/W
b31 to b14	Reserved		R
b13	SCON_N	NoC Interconnection Status for BGPIO3 0: Disconnected 1: Connected	R
b12	SCON_M	NoC Interconnection Status for UART8 0: Disconnected 1: Connected	R
b11	SCON_L	NoC Interconnection Status for UART7 0: Disconnected 1: Connected	R
b10	SCON_K	NoC Interconnection Status for UART6 0: Disconnected 1: Connected	R
b9	SCON_J	NoC Interconnection Status for UART5 0: Disconnected 1: Connected	R
b8	SCON_I	NoC Interconnection Status for UART4 0: Disconnected 1: Connected	R
b7	SCON_H	NoC Interconnection Status for BGPIO2 0: Disconnected 1: Connected	R
b6	SCON_G	NoC Interconnection Status for BGPIO1 0: Disconnected 1: Connected	R
b5	SCON_F	NoC Interconnection Status for SPI6 0: Disconnected 1: Connected	R
b4	SCON_E	NoC Interconnection Status for SPI5 0: Disconnected 1: Connected	R
b3	SCON_D	NoC Interconnection Status for SPI4 0: Disconnected 1: Connected	R
b2	SCON_C	NoC Interconnection Status for SPI3 0: Disconnected 1: Connected	R

Table 6.70 PWRSTAT_PG1 Register Contents (2/2)

Bit Position	Bit Name	Function	R/W
b1	SCON_B	NoC Interconnection Status for SPI2 0: Disconnected 1: Connected	R
b0	SCON_A	NoC Interconnection Status for SPI1 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.68 PWRSTAT_PG2_25MHZ — Power Management Status for PG2 25MHz

Address: 4000 C15Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	SCON_S	SCON_R	SCON_Q
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0

Table 6.71 PWRSTAT_PG2_25MHZ Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	SCON_S	NoC Interconnection Status for TIMER2 0: Disconnected 1: Connected	R
b1	SCON_R	NoC Interconnection Status for TIMER1 0: Disconnected 1: Connected	R
b0	SCON_Q	NoC Interconnection Status for ConfigSys2 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.69 PWRSTAT_PG3_48MHZ — Power Management Status for PG3 48MHz

Address: 4000 C160h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	MISTAT_UF	MIRACK_UF	—	SCON_AA	SCON_Z	—
Value after reset	X	X	X	X	X	X	X	X	X	X	0	0	X	0	0	X

Table 6.72 PWRSTAT_PG3_48MHZ Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b6	Reserved		R
b5	MISTAT_UF	Idle Status of the NoC interconnect for Peripheral Group 3 0: Active 1: Idle	R
b4	MIRACK_UF	Idle Request Acknowledge for Peripheral Group 3 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b3	Reserved		R
b2	SCON_AA	NoC Interconnection Status for CAN2 0: Disconnected 1: Connected	R
b1	SCON_Z	NoC Interconnection Status for CAN1 0: Disconnected 1: Connected	R
b0	Reserved		R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.70 PWRSTAT_PG4 — Power Management Status for PG4

Address: 4000 C164h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	MISTAT_UI	MIRACK_UI	—	—	SCON_AD	SCON_AC
Value after reset	X	X	X	X	X	X	X	X	X	X	0	0	X	X	0	0

Table 6.73 PWRSTAT_PG4 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b6	Reserved		R
b5	MISTAT_UI	Idle Status of the NoC interconnect for Peripheral Group 4 0: Active 1: Idle	R
b4	MIRACK_UI	Idle Request Acknowledge for Peripheral Group 4 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R
b3, b2	Reserved		R
b1	SCON_AD	NoC Interconnection Status for Semaphore 0: Disconnected 1: Connected	R
b0	SCON_AC	NoC Interconnection Status for LCDC 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.71 PWRSTAT_ROM — Power Management Status for ROM

Address: 4000 C170h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0

Table 6.74 PWRSTAT_ROM Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b1	Reserved		R
b0	SCON_A	NoC Interconnection Status for ROM 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.72 PWRCTRL_CM3 — Power Management Control for CM3

Address: 4000 C174h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MIREQ_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	1

Table 6.75 PWRCTRL_CM3 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	MIREQ_A	Idle Request to the NoC interconnect for Cortex-M3 0: Active 1: Idle Note that the clock and reset domain of CM3 belongs to RIN BUS sub system. Therefore, clock and reset in PWRCTRL_RINCTRL should be controlled accordingly.	R/W
b1	RSTN_A	Active low Reset for CM3_HCLK/CM3_FCLK domain	R/W
b0	CLKEN_A	Clock Enable for CM3_HCLK, CM3_FCLK 0: Disable 1: Enable	R/W

NOTE

Software shall request reset of Cortex-M3 only if there are no pending transactions on the NoC interconnect. e.g. The Cortex-M3 is in WFE state. Interruption of Cortex-M3 bus operation results in hang-up of the NoC interconnect. In case of RZ/N1L, this register initial value is 0x3.

6.3.73 PWRSTAT_CM3 — Power Management Status for CM3

Address: 4000 C178h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MISTAT_A	MIRACK_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0

Table 6.76 PWRSTAT_CM3 Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b2	Reserved		R
b1	MISTAT_A	Idle Status of the NoC interconnect for Cortex-M3 0: Active 1: Idle	R
b0	MIRACK_A	Idle Request Acknowledge for Cortex-M3 0: Not acknowledged Idle Request 1: Acknowledged Idle Request	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.74 PWRSTAT_RINCTRL — Power Management Status for R-IN Engine Accessory Register

Gating of the RINBUS_HCLK may result in non-deterministic behavior of the 2MB SRAM clocked by RINBUS_HCLK in R-IN Engine Accessory Register block.

Address: 4000 C17Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0

Table 6.77 PWRSTAT_RINCTRL Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b1	Reserved		R
b0	SCON_A	NoC Interconnection Status for R-IN Engine Accessory Register 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.75 PWRSTAT_SWITCHCTRL — Power Management Status for Ethernet Accessory Register

Address: 4000 C180h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCON_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0

Table 6.78 PWRSTAT_SWITCHCTRL Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b1	Reserved		R
b0	SCON_A	NoC Interconnection Status for Ethernet Accessory Register 0: Disconnected 1: Connected	R

NOTE

The software shall not apply clock gating or software reset to any module unless all corresponding NoC interconnect of the module are disconnected (SCON = 0) and in idle (MISTAT = 1).

6.3.76 PWRCTRL_RINCTRL — Power Management Control for R-IN Engine Accessory Register

Gating of the RINBUS_HCLK may result in non-deterministic behavior of the 2MB SRAM clocked by RINBUS_HCLK in R-IN Engine Accessory Register block.

During Cortex-M3 operation, gating the RINBUS_HCLK results in hang-up of the Cortex-M3 accesses since RIN BUS sub system used in Cortex-M3 accesses is stopped.

Address: 4000 C184h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1

Table 6.79 PWRCTRL_RINCTRL Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	SLVRDY_A	Indicates to the NoC interconnect that the R-IN Engine Accessory Register is ready for access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for RINBUS_HCLK domain	R/W
b0	CLKEN_A	Clock Enable for RINBUS_HCLK (internal bus) 0: Disable 1: Enable	R/W

6.3.77 PWRCTRL_SWITCHCTRL — Power Management Control for Ethernet Accessory Register

Address: 4000 C188h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	RSTN_ETH	RSTN_CLK25	SLVRDY_A	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1

Table 6.80 PWRCTRL_SWITCHCTRL Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b5	Reserved		R
b4	RSTN_ETH	Active low Reset for RGMII/RMII Converter (50 MHz).	R/W
b3	RSTN_CLK25	Active low Reset for Timestamp signal selection logic	R/W
b2	SLVRDY_A	Indicates to the NoC interconnect that the Ethernet Accessory Register is ready for access 0: Not Ready 1: Ready	R/W
b1	RSTN_A	Active low Reset for RINEG_HCLK domain	R/W
b0	CLKEN_A	Clock Enable for RINEG_HCLK (internal bus—Ethernet Accessory Register) 0: Disable 1: Enable	R/W

6.3.78 PWRCTRL_HWRTOS — Power Management Control for HW-RTOS

Address: 4000 C18Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKEN_B	RSTN_A	CLKEN_A
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1

Table 6.81 PWRCTRL_HWRTOS Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	CLKEN_B	Clock Enable for HWRTOS_MDCCLK 0: Disable 1: Enable	R/W
b1	RSTN_A	Active low Reset for HWRTOS_CLK domain	R/W
b0	CLKEN_A	Clock Enable for HWRTOS_CLK 0: Disable 1: Enable	R/W

6.3.79 RSTCTRL — Reset Control Register

Software can use this register to initiate system reset or identify if any of the current hardware system reset sources are requesting a system reset.

Address: 4000 C198h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	SWRST_REQ	CM3SYSRESET_REQ	CM3LOCKUPRST_REQ	WDM3RST_REQ	WDA7RST_REQ		—
Value after reset	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	X

Table 6.82 RSTCTRL Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b7	Reserved		R
b6	SWRST_REQ	Software triggered system reset request 0: No system reset request 1: Software requests a system reset to be performed.	R/W
b5	CM3SYSRESET_REQ	Cortex-M3 SYSRESETREQ initiated system reset 0: No system reset request 1: Pending system reset request*1	R/W
b4	CM3LOCKUPRST_REQ	Cortex-M3 Core Lockup reset request 0: No system reset request 1: Pending system reset request*1	R/W
b3	WDM3RST_REQ	Cortex-M3 Core watchdog reset request 0: No system reset request 1: Pending system reset request*1	R/W
b2, b1	WDA7RST_REQ	Cortex-A7 watchdog reset request 0: No system reset request 1: Pending system reset request*1 Bit2 (RZ/N1D) Cortex-A7 processor1 watchdog reset request (RZ/N1S, RZ/N1L) Reserved. Bit1 (RZ/N1D, RZ/N1S) Cortex-A7 processor0 watchdog reset request (RZ/N1L) Reserved.	R/W
b0	Reserved		R

Note 1. Cleared by write 1

6.3.80 CFG_USB — USB Mode Configuration Register

Changing the USB Host/Function controller configuration may affect the USBPLL operation. The interruption of USBPLL operation may lead to a system hang-up. The software shall make sure that prior to applying any change to USB configuration, disconnect all module operated by USBPLL clock from the NoC interconnect in order to avoid bus hang-up.

Address: 4000 C000h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	FRCLK 48MOD	H2MOD E	DIRPD
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	1

Table 6.83 CFG_USB Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b3	Reserved		R
b2	FRCLK48MOD	0: USBPLL stops during USB suspend 1: USBPLL operates regardless of USB state i.e. It can be used to clock other modules	R/W
b1	H2MODE	USB interface Port setting signal 0: Port1 Function, Port2 Host 1: Port1 Host, Port2 Host In the USB reset sequence, set this bit before canceling the host reset.	R/W
b0	DIRPD	Direct power down control 0: USBPLL Powered 1: USBPLL Powered down This bit is direct power down signal to USB module. Please refer to USB 2.0 HS Host/Function Controller section in UM of System Control and Peripheral for more details about Direct power down feature.	R/W

6.3.81 OPMODE — System and Boot Configuration Register

Boot mode configurations are read from external configuration pins after Power on Reset. System reset has no effect on these values.

Address: 4000 C004h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	LCD1PU	—	CM3BOOTSEL	CA7BOOTSRC		—	DDRMOD
Value after reset	X	X	X	X	X	X	X	X	X	X*1	X	X*1	X*1	X*1	X	X*1

Table 6.84 OPMODE Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b7	Reserved		R
b6	LCD1PU	LCD interface (assignment to GPIO pins) default pull configuration (RZ/N1D and RZ/N1S) 0: Pull-down on GPIO[73:62] and GPIO[145:127] 1: Pull-up on GPIO[73:62] and GPIO[145:127]	R
b5	Reserved		R
b4	CM3BOOTSEL	Cortex-M3 Boot mode configuration 0: CA7 boot from CA7BOOTSRC 1: CM3 boot from QSPI (RZ/N1L)	R
b3, b2	CA7BOOTSRC	Boot mode configuration 2’b00: Boot on QuadSPI1 2’b01: Boot on NAND Flash 2’b10: Boot on USB function 2’b11: Reserved	R
b1	Reserved		R
b0	DDRMOD	DDR Controller Configuration (RZ/N1D) 0: DDR3 1: DDR2	R

Note 1. The value is reflected after power-on reset.

6.3.82 CFG_SDIO[m] — SDIO[m] Configuration Register (m = 1 or 2)

Address: CFG_SDIO1: 4000 C008h
CFG_SDIO2: 4000 C0C4h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	SLOTTYPE		BASECLKFREQ							
Value after reset	X	X	X	X	X	X	0	0	0	0	0	0	0	0	0	1

Table 6.85 CFG_SDIO[m] Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b10	Reserved		R
b9, b8	SLOTTYPE	Slot Type—Should be set based on the product usage 2'b00: Removable Card Slot 2'b01: Embedded Slot Other: Reserved This slot type is reflected to the SDIO Capabilities register. This field should be set to an appropriate value since it is also used to determine the Card Detection time.	R/W
b7 to b0	BASECLKFREQ	Base Clock Frequency (MHz) setting for SDIO[m]_ECLK Clock This field must be set to the below value: SDIO[m]_ECLK frequency = roundup (1000 / PWRCTRL_SDIO[m]DIV.DIV)	R/W

6.3.83 DBGCON — Debug Control Register

Address: 4000 C014h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	CA7WD1_DBG_EN	CA7WD0_DBG_EN	CM3WD_DBG_EN	PR_DBG_EN
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1

Table 6.86 DBGCON Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b4	Reserved		R
b3	CA7WD1_DBG_EN	(RZ/N1D) Control the watchdog function while Cortex-A7 processor1 is HALTED 0: Enable Cortex-A7 processor1 watchdog on HALT 1: Stop Cortex-A7 processor1 watchdog on HALT (RZ/N1S, RZ/N1L) Reserved	R/W
b2	CA7WD0_DBG_EN	(RZ/N1D, RZ/N1S) Control the watchdog function while Cortex-A7 processor0 is HALTED 0: Enable Cortex-A7 processor0 watchdog on HALT 1: Stop Cortex-A7 processor0 watchdog on HALT (RZ/N1L) Reserved	R/W
b1	CM3WD_DBG_EN	Control the watchdog function while Cortex-M3 Core is HALTED 0: Enable Cortex-M3 Core watchdog on HALT 1: Stop Cortex-M3 Core watchdog on HALT	R/W
b0	PR_DBG_EN	Control Emulation function 0: Disable emulation function 1: Enable emulation function—Stop HW-RTOS timers on Halt PR_DBG_EN bit is control enable, disable of emulation function. Initial setting is enable of emulation function. During PR_DBG_EN is enable and CPU is halted by debug (e.g. Stop CPU by ICE), HW-RTOS timer is stopped. This function prevents HW-RTOS OS timer inconsistence	R/W

6.3.84 CFG_GPIOT_PTEN_xx — GPIO Trigger Enable Register

Address: CFG_GPIOT_PTEN_1A: 4000 C0A4h
CFG_GPIOT_PTEN_1B: 4000 C0B0h
CFG_GPIOT_PTEN_2A: 4000 C0B4h
CFG_GPIOT_PTEN_2B: 4000 C0B8h
CFG_GPIOT_PTEN_3A: 4000 C0D8h
CFG_GPIOT_PTEN_3B: 4000 C0DCh

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PORTEN															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PORTEN															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6.87 CFG_GPIOT_PTEN_xx Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b0	PORTEN	GPIO port trigger enable (per bit) 0: Port trigger disable (Enable original BGPIO function) 1: Port trigger enable	R/W

NOTE

Bit 31 to 10 are reserved bits for CFG_GPIOT_PTEN_3B.

6.3.85 CFG_GPIOT_TSRC — GPIO Trigger Source Select Register

Trigger Source Select Control for BGPIO1/2/3 Port A/B.

Address: 4000 C0BCh

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	TRIG3					—	—	—	TRIG2				
Value after reset	X	X	X	0	0	0	0	0	X	X	X	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TRIG1					—	—	—	TRIG0				
Value after reset	X	X	X	0	0	0	0	0	X	X	X	0	0	0	0	0

Table 6.88 CFG_GPIOT_TSRC Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b29	Reserved		R
b28 to b24	TRIG3	GPIO Trigger Source Select for GPIO_TRIGGER[3] (to BGPIO) from interrupt sources. TRIG3[4:0] interrupt source 5'h00: GPIO_TRIGGER[0] selected by Ethernet Accessary Register 5'h01: GPIO_TRIGGER[1] selected by Ethernet Accessary Register 5'h02: GPIO_TRIGGER[2] selected by Ethernet Accessary Register 5'h03: GPIO_TRIGGER[3] selected by Ethernet Accessary Register Others: Not used	R/W
b23 to b21	Reserved		R
b20 to b16	TRIG2	GPIO Trigger Source Select for GPIO_TRIGGER[2] (to BGPIO) from interrupt sources. The interrupt sources are same as TRIG3.	R/W
b15 to b13	Reserved		R
b12 to b8	TRIG1	GPIO Trigger Source Select for GPIO_TRIGGER[1] (to BGPIO) from interrupt sources. The interrupt sources are same as TRIG3.	R/W
b7 to b5	Reserved		R
b4 to b0	TRIG0	GPIO Trigger Source Select for GPIO_TRIGGER[0] (to BGPIO) from interrupt sources. The interrupt sources are same as TRIG3.	R/W

6.3.86 CFG_DMAMUX — DMAC1 & DMAC2 Multiplexer Register

Ethernet DMA sources can be assigned to 4 DMA channels. However, the same DMA source must not be assigned to multiple channels.

Address: 4000 C0A0h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	D2MX15	D2MX14	D2MX13	D2MX12	D2MX11	D2MX10	D2MX9	D2MX8	D2MX7	D2MX6	D2MX5	D2MX4	D2MX3	D2MX2	D2MX1	D2MX0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	D1MX15	D1MX14	D1MX13	D1MX12	D1MX11	D1MX10	D1MX9	D1MX8	D1MX7	D1MX6	D1MX5	D1MX4	D1MX3	D1MX2	D1MX1	D1MX0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6.89 CFG_DMAMUX Register Contents (1/3)

Bit Position	Bit Name	Function	R/W
b31	D2MX15	DMAC2 Request interface15 Multiplexer 0: TIMER2_SubTimer7 1: ADC ch1	R/W
b30	D2MX14	DMAC2 Request interface14 Multiplexer 0: S3_DIVCLK*1 1: ADC ch0	R/W
b29	D2MX13	DMAC2 Request interface13 Multiplexer 0: S3_CONCLK*1 1: MSEBIM3 (TX on CS1_N)	R/W
b28	D2MX12	DMAC2 Request interface12 Multiplexer 0: MAC_TRIG[1]*1 1: MSEBIM2 (RX on CS1_N)	R/W
b27	D2MX11	DMAC2 Request interface11 Multiplexer 0: MAC_PPS[1]*1 1: MSEBIM1 (TX on CS0_N)	R/W
b26	D2MX10	DMAC2 Request interface10 Multiplexer 0: MAC_PPS[0]*1 1: MSEBIM0 (RX on CS0_N)	R/W
b25	D2MX9	DMAC2 Request interface9 Multiplexer 0: CAT_SYNC1 or SERCOS3_Int[1]*1 1: Reserved	R/W
b24	D2MX8	DMAC2 Request interface8 Multiplexer 0: CAT_SYNC0 or SERCOS3_Int[0]*1 1: Reserved	R/W
b23	D2MX7	DMAC2 Request interface7 Multiplexer 0: TIMER2_SubTimer6 1: Reserved	R/W
b22	D2MX6	DMAC2 Request interface6 Multiplexer 0: S3_DIVCLK*1 1: Reserved	R/W
b21	D2MX5	DMAC2 Request interface5 Multiplexer 0: S3_CONCLK*1 1: UART8 TX	R/W

Table 6.89 CFG_DMAMUX Register Contents (2/3)

Bit Position	Bit Name	Function	R/W
b20	D2MX4	DMAC2 Request interface4 Multiplexer 0: MAC_TRIG[1]*1 1: UART8 RX	R/W
b19	D2MX3	DMAC2 Request interface3 Multiplexer 0: MAC_PPS[1]*1 1: SPI6 TX	R/W
b18	D2MX2	DMAC2 Request interface2 Multiplexer 0: MAC_PPS[0]*1 1: SPI6 RX	R/W
b17	D2MX1	DMAC2 Request interface1 Multiplexer 0: CAT_SYNC1 or SERCOS3_Int[1]*1 1: SPI5 TX	R/W
b16	D2MX0	DMAC2 Request interface0 Multiplexer 0: CAT_SYNC0 or SERCOS3_Int[0]*1 1: SPI5 RX	R/W
b15	D1MX15	DMAC1 Request interface15 Multiplexer 0: TIMER1_SubTimer7 1: SPI4 TX	R/W
b14	D1MX14	DMAC1 Request interface14 Multiplexer 0: S3_DIVCLK*1 1: SPI4 RX	R/W
b13	D1MX13	DMAC1 Request interface13 Multiplexer 0: S3_CONCLK*1 1: SPI3 TX	R/W
b12	D1MX12	DMAC1 Request interface12 Multiplexer 0: MAC_TRIG[1]*1 1: SPI3 RX	R/W
b11	D1MX11	DMAC1 Request interface11 Multiplexer 0: MAC_PPS[1]*1 1: SPI2 TX	R/W
b10	D1MX10	DMAC1 Request interface10 Multiplexer 0: MAC_PPS[0]*1 1: SPI2 RX	R/W
b9	D1MX9	DMAC1 Request interface9 Multiplexer 0: CAT_SYNC1 or SERCOS3_Int[1]*1 1: SPI1 TX	R/W
b8	D1MX8	DMAC1 Request interface8 Multiplexer 0: CAT_SYNC0 or SERCOS3_Int[0]*1 1: SPI1 RX	R/W
b7	D1MX7	DMAC1 Request interface7 Multiplexer 0: TIMER1_SubTimer6 1: UART7 TX	R/W
b6	D1MX6	DMAC1 Request interface6 Multiplexer 0: S3_DIVCLK*1 1: UART7 RX	R/W
b5	D1MX5	DMAC1 Request interface5 Multiplexer 0: S3_CONCLK*1 1: UART6 TX	R/W
b4	D1MX4	DMAC1 Request interface4 Multiplexer 0: MAC_TRIG[1]*1 1: UART6 RX	R/W

Table 6.89 CFG_DMAMUX Register Contents (3/3)

Bit Position	Bit Name	Function	R/W
b3	D1MX3	DMAC1 Request interface3 Multiplexer 0: MAC_PPS[1]*1 1: UART5 TX	R/W
b2	D1MX2	DMAC1 Request interface2 Multiplexer 0: MAC_PPS[0]*1 1: UART5 RX	R/W
b1	D1MX1	DMAC1 Request interface1 Multiplexer 0: CAT_SYNC1 or SERCOS3_Int[1]*1 1: UART4 TX	R/W
b0	D1MX0	DMAC1 Request interface0 Multiplexer 0: CAT_SYNC0 or SERCOS3_Int[0]*1 1: UART4 RX	R/W

Note 1. CAT_SYNC0 or SERCOS3_Int[0] is selected by DMACTRL in Ethernet Accessory registers.
CAT_SYNC1 or SERCOS3_Int[1] is selected by DMACTRL in Ethernet Accessory registers.
7 DMA requests from Ethernet Peripherals are assigned to the request interface 4 times, only one request should be used at the same time.

6.3.87 VERSION — Product Version Register

Address: 4000 C19Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PROD	VERSION							
Value after reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 6.90 VERSION Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b9	Reserved		R
b8	PROD	0: RZ/N1D 1: RZ/N1S, RZ/N1L	R
b7 to b0	VERSION	HW version*1 RZ/N1D: 0x13 RZ/N1S, RZ/N1L: 0x11	R

Note 1. If the version shows RZ/N1D: 0x11 or RZ/N1S, RZ/N1L: 0x10, A5PSW register write access issue might happen. Please refer to *Technical Update* with regard to the workaround.

6.3.88 BOOTADDR — Cortex-A7 processor1 Boot Address Configuration Register

Cortex-A7 processor1 is in standby mode during processor0 ROM boot process. 2nd boot loader should set this register in order to define the processor1 boot address. Once the processor1 reset is released, it executes a code in ROM at first, and gets jump address from this register.

This register is only used in RZ/N1D and is available from Cortex-A7.

Address: 4000 C204h

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BOOTADDR															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BOOTADDR															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6.91 BOOTADDR Register Contents

Bit Position	Bit Name	Function	R/W
b31 to b0	BOOTADDR	2nd boot address of the Cortex-A7 processor1	R/W

Section 7 Operating Modes

7.1 Overview

In RZ/N1D and RZ/N1S, Cortex-A7 boots at first, then executes the bootloader in embedded ROM. 3 boot sources, QSPI or NAND Flash or USB are available. The bootloader initializes the RZ/N1 for 1st boot, after that loads and executes a second bootloader from the boot sources.

In RZ/N1L, Cortex-M3 boots (Cortex-A7 is not available). Cortex-M3 executes a code in QSPI directly.

System Controller manages reset, clock and configuration based on external pins or registers. Boot mode and sequence are also handled in the System Controller.

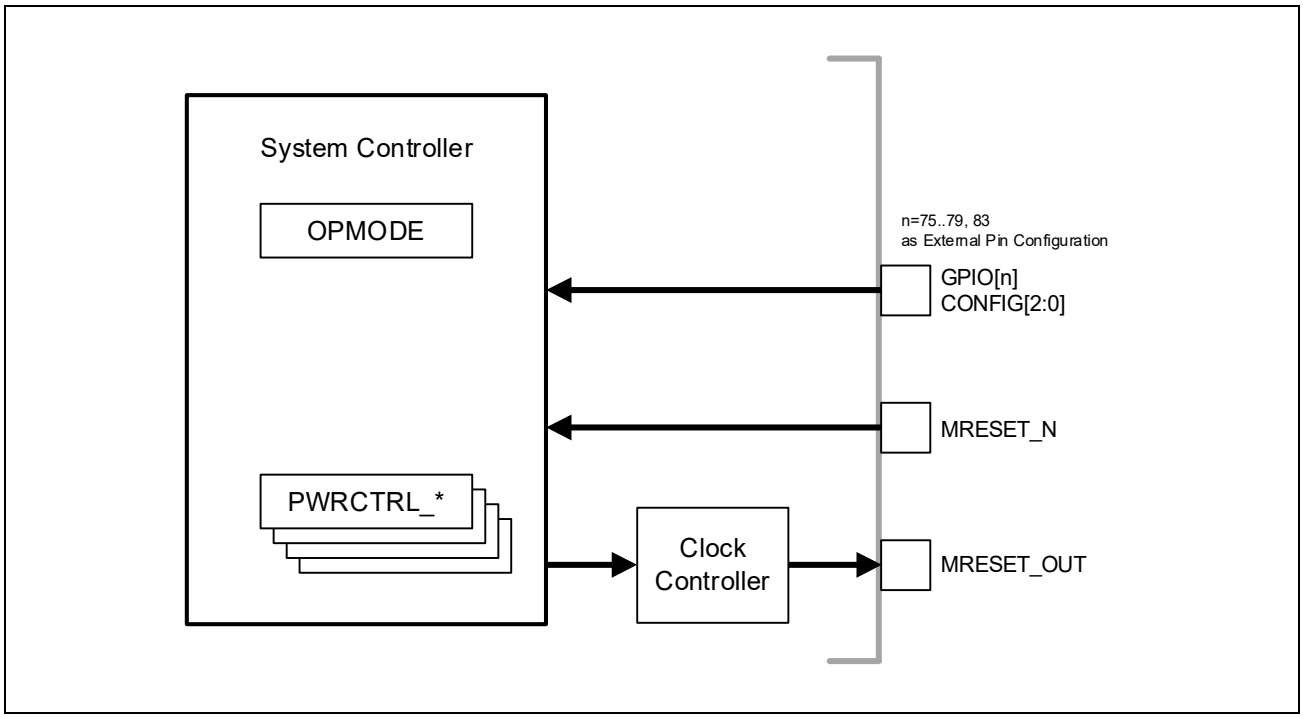


Figure 7.1 System Controller

7.2 Boot Mode Specification (for RZ/N1D and RZ/N1S)

7.2.1 Common Feature

- Cortex-A7 Clock Speed
  - Cortex-A7: 250 MHz
  - The BootROM uses the default divider setting (/2).
- RAM requirements
  - 64 kB, 0x200F_0000 – 0x200F_FFFF, is used by for BootROM
- UART1 outputs boot messages.
  - 115200Baud
  - UART TXD pin (GPIO[103]) is used for UART interface
  - Boot progress and error messages
- 2nd Stage Boot Image
  - Maximum Size 1 MByte
  - Minimum Size 4 Bytes
  - 2nd Stage Image must execute from internal SRAM (2MB SRAM) in continuous region.
    In other words, address region from either 0x0400_0000 – 0x040F_FFFF or 0x2000_0000 – 0x200E_FFFF.

7.2.2 QSPI Boot Feature

- The bootloader in embedded ROM initializes QSPI module and configures following GPIO pins as Level1/Func4 (QSPI1) in QSPI boot mode. QUAD1_CS_N[3:1] (GPIO73, GPIO149 and 150) are configured as CS output pins. Please take into account the I/O mode if those pins are used for other function on a board design.

GPIO pins	Pull mode	QSPI1 pin name	Pin I/O mode	Note
GPIO74	without Pullup/Pulldown	QUAD1_CS_N[0]	Output	Always used in QSPI boot
GPIO75		QUAD1_IO[3]	Input/Output	Refer to "**Section 7.3.2, External Pin Configuration**".
GPIO76		QUAD1_IO[2]	Input/Output	
GPIO77		QUAD1_IO[1]	Input/Output	
GPIO78		QUAD1_IO[0]	Input/Output	
GPIO79		QUAD1_CLK	Output	
GPIO73		QUAD1_CS_N[1]	Output	These pins could be used for other function by user configuration. but please be aware of pin state set by the ROM.
GPIO149		QUAD1_CS_N[2]	Output	
GPIO150		QUAD1_CS_N[3]	Output	

- Supported Serial Flash

  (1) Quad IO SPI Flash
  (2) Single IO SPI Flash

  The bootloader accesses the device connected to QUAD1_CS_N[0] in standard SPI mode.
- CLK frequency for Flash: 5.2 MHz
- Address: 3 bytes

7.2.3 NAND Boot Feature

- The bootloader in embedded ROM initializes NAND module and configures following GPIO pins as Level1/Func3 (NAND) in NAND boot mode.

GPIO pins	Pull mode	QSPI1 pin name	Pin I/O mode	Note
GPIO80	without Pullup/Pulldown	FNAND_ALE	Output	
GPIO81		FNAND_CLE	Output	
GPIO82		FNAND_WE_N	Output	
GPIO83		FNAND_RE_N	Output	Refer to "**Section 7.3.2, External Pin Configuration**".
GPIO91..84		FNAND_IO[7:0]	Input/Output	
GPIO92		FNAND_CE_N[0]	Output	
GPIO93		FNAND_WP_N[0]	Output	
GPIO94	with pullup	FNAND_RY/BY_N[0]	Input	

- Supported NAND Flash

  (1) ONFI 1.0 / asynchronous NAND Flash

  - IO bus size: 8-bit
  - Density: 1 to 8-Gbit
  - Mode 0 is used through boot. Devices must support Mode0.

  The bootloader identifies the device before triggering the boot sequence (either "Read ID" command or Read ONFI parameters) and set timings & ECC accordingly.
  If "READ ID" is not supported on the device, it cannot be booted.

  (2) ONFI 2.0 synchronous NAND Flash

  Only in ONFI 1.0 backwards compatibility mode, compliant to the NAND Flash Controller limitations

- NAND_ECLK frequency: 83.3MHz
  - FNAND_RE_N/FNAND_WE_N is asserted for 5 NAND_ECLK cycles and held high for 3 NAND_ECLK cycles.

7.2.4 USB Boot Feature

- The bootloader in embedded ROM configures the RZ/N1 USB Port1 as a USB Function mode and DFU Device
- USB Speed
  - Full speed and High speed
- USB DFU Function interface
  - Standard DFU interface for uploading 2nd stage image
- PC / Host DFU Software
  - Generic DFU host software may be used

    e.g. “dfu_util” from Sourceforge, and a generic DFU driver “libUSBk”
    http://dfu-util.sourceforge.net/releases/dfu-util-0.8-binaries/win32-mingw32/
    https://sourceforge.net/projects/libusbk/

The Boot from USB downloads an SPKG format image at first. An SPKG image will be downloaded to the internal SRAM from a USB DFU Host e.g. a PC running USB Function Firmware Upgrade application.

The PC utility only provides a mechanism for downloading an SPKG. The host PC is not able to directly reprogram the FLASH.

After USB boot, this application (possibly uBoot or similar) is able to update the FLASH with a new image from the PC.

7.3 Standard Boot Sequence

7.3.1 Overview

RZ/N1 System Controller captures initial system setting from certain external pins at rising of MRESET_N pin. Then, primary CPU execute 1st bootloader. In RZ/N1D and RZ/N1S, primary CPU is Cortex-A7 and 1st bootloader is placed in embedded ROM. In RZ/N1L, primary CPU is Cortex-M3 and 1st boot loader should be placed in QSPI Flash.

7.3.2 External Pin Configuration

The following external pins are used to system configuration and boot sequence.

- GPIO[75] (QUAD1_IO[3])
- GPIO[76] (QUAD1_IO[2])
- GPIO[77] (QUAD1_IO[1])
- GPIO[78] (QUAD1_IO[0])
- GPIO[79] (QUAD1_CLK)
- GPIO[83] (FNAND_RE_N)

These pins come up as input without integrated pull-up/-down.

Please select suitable mode by external pull-up/-down resister on a PCB board.

Table 7.1 External Pin Configuration

Control Signal	Function Configured	Comment
GPIO[75]	0: DDR3 1: DDR2	DDR Memory controller configuration for RZ/N1D. In other models, should be pulled up or down.
GPIO[76]	Should be 1	
GPIO[78:77]	2'b00: CA7 Boot on QuadSPI 2'b01: CA7 Boot on NAND Flash 2'b10: CA7 Boot on USB Function 2'b11: Reserved	Boot mode configuration for RZ/N1D and RZ/N1S. In RZ/N1L, pulled up or down.
GPIO[79]	1: Pull-up on GPIO[73:62] and GPIO[145:127] 0: Pull-down on GPIO[73:62] and GPIO[145:127]	LCD interface default pull configuration for RZ/N1D and RZ/N1S. In RZ/N1L, should be 1.
GPIO[83]	Should be 1	
Boot Debug signal	**Function configured**	**Comment**
GPIO[103]	UART1 TXD	UART debugging for boot (for RZ/N1D and RZ/N1S)

7.3.3 CPU Booting

The system controller carries out the initial setup of the interconnect and releases the reset of the primary CPU based on the system configuration. A series of actions precedes the reset de-assertion of the primary CPU. These initial setup actions are carried out in system controller. During this phase, all CPUs are held in reset. Once all steps accomplished, the primary CPU is released from reset.

During the system initialization after external reset triggered by “MRESET_N”, the system controller samples and stores the external pin configuration defined by external pull resistors.

The sampling sequence is as follows:

- On the first oscillator clock edge after “MRESET_N” de-assertion: The external pin configurations are sampled, the LCD pull up/down control bit is directly taken from the GPIO[79].
- On the second “clock” edge after “MRESET_N” de-assertion: The boot configuration is sampled to FF, the LCD pull up/down control bit switches to be driven from FF value.
- On the third “clock” edge after “MRESET_N” de-assertion: The “BOOTMODE_LATCHED” signal is asserted for the de-assertion of “MRESET_OUT” in clock controller

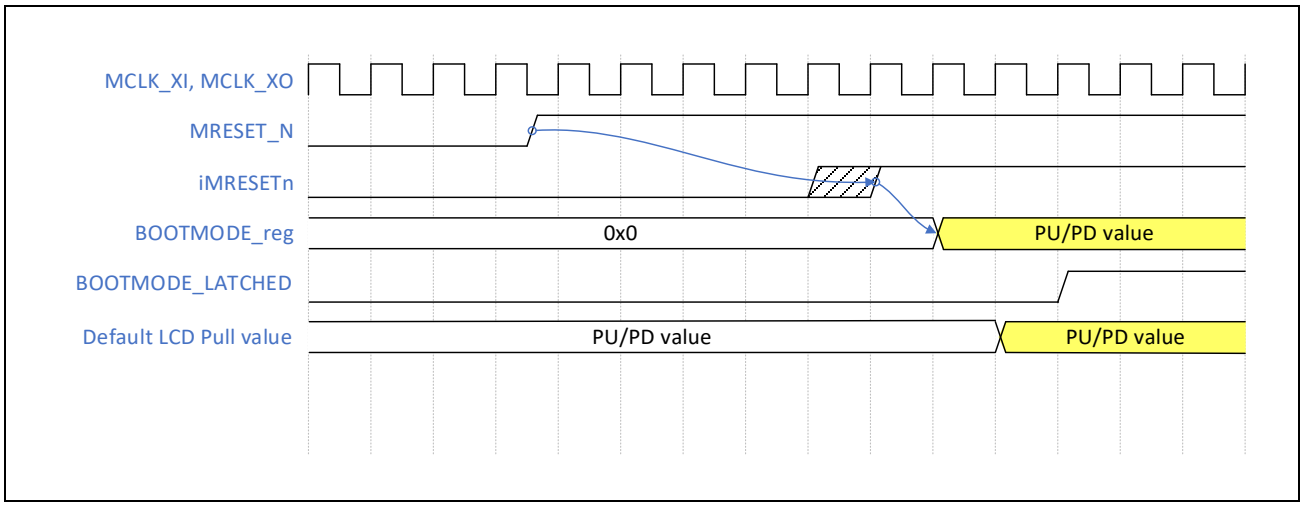


Figure 7.2 Boot Configuration Sampling Sequence

CAUTION

External pull values must be kept that the appropriate value is captured in the External Pin Configuration while the “MRESET_OUT” signal is being asserted.

7.3.4 RZ/N1D and RZ/N1S Boot

In a system with Cortex-A7 processor(s) and Cortex-M3 processor, Cortex-A7 processor0 will be the Primary or Boot processor.

After the system is powered up, both Cortex-A7 processors, Cortex-A7 processor0 and processor1, will come out of reset and execute the code in embedded ROM at address 0x00000000. An initial core ID check puts Cortex-A7 processor1 to WFE.

Only Cortex-A7 processor0 will be permitted to execute the remainder of the boot code. Then the 2nd stage bootloader is executed. The Reset vector address for the Cortex-A7 processor1 and the Cortex-M3 processor may be configured to any locations. BOOTADDR register defines the boot address for Cortex-A7 processor1.

- For debug purpose, the bootloader configures the GPIO[103] in Level 1 function 15 and Level 2 function 12 (UART1_TXD), this IO Multiplexing configuration is kept after the end of bootloader.

7.3.5 RZ/N1L Boot

In RZ/N1L, Cortex-M3 will be the Primary processor.

The Cortex-M3 will not run the Bootloader in embedded ROM. It boots directly at 5.2 MHz from QSPI Flash mapped to 0x00000000.

GPIO[74:79] is configured to QSPI1 by System Controller with the following settings:

GPIO pins	Pull mode	QSPI1 pin name	Pin I/O mode	Note
GPIO74	with Pullup	QUAD1_CS_N[0]	Output	
GPIO75	without Pullup/Pulldown	QUAD1_IO[3]	Input/Output	Refer to “**Section 7.3.2, External Pin Configuration**”.
GPIO76		QUAD1_IO[2]	Input/Output	
GPIO77		QUAD1_IO[1]	Input/Output	
GPIO78		QUAD1_IO[0]	Input/Output	
GPIO79		QUAD1_CLK	Output	

7.4 SPKG Format (for RZ/N1D and RZ/N1S)

7.4.1 Overview

Data loaded from boot source (QSPI, NAND FLASH, USB) is subject to the possibility of the corrupt image by bit errors. SPKG format is used to check the contents.

7.4.2 Implementation Specifics

The Bootloader loads a valid SPKG from the chosen boot source (QSPI, NAND FLASH or USB).

The SPKG contains:

- A block consisting of 8 headers (with a header CRC)
- A Payload (Immediately following the block of headers):
  - The 2nd stage bootloader image
  - A payload CRC value

The SPKG data fields are defined in the following table.

Table 7.2 SPKG Fields

SPKG Field	Bits	Length	Field	Description
Header*1				Total 24 bytes
	31:0	32 bits	Marker	“R”, “Z”, “N”, “1” to mark the Header start
	35:32	4 bits	version	SPKG header type version
	39:36	4 bits	spare bits	Set to “0”
	40	1 bit	padding	Set to “0”
	42:41	2 bits	NAND ECC block size (codeword size)	Value is configured to ECC_BLOCK_SIZE in CONTROL register of NAND Flash Controller 2’b00 – 256 bytes 2’b01 – 512 bytes 2’b10 – 1024 bytes 2’b11 – INVALID
	44:43	2 bits	padding	Set to “0”
	45	1 bit	Hardware ECC Support enable	Value is configured to ECC_EN in CONTROL register of NAND Flash Controller 0 – ECC disabled 1 – ECC enabled
	47:46	2 bits	padding	Set to “0”
	50:48	3 bits	NAND ECC scheme	Value is configured to ECC_CAP in ECC_CTRL register of NAND Flash Controller 3’b000 – BCH2 3’b001 – BCH4 3’b010 – BCH8 3’b011 – BCH16 3’b100 – BCH24 3’b101, 3’b110, 3’b111 – BCH32
	55:51	5 bits	padding	Set to “0”
	63:56	8 bits	NAND ECC bytes per block	Number (8-bit value) of NAND Flash ECC Bytes per NAND ECC block e.g. for BCH8 and NAND ECC block size = 512, this value will be typically 14 (0x0E)
	71:64	8 bits	spare byte	Set to “0”
	95:72	24 bits	payload length	Payload length consisting of BLp_header, image and Payload CRC
	127:96	32 bits	load addr	Address of internal memory to where the 2nd stage bootloader image should be written.
	159:128	32 bits	execution offset*2	Offset from the start of the 2nd stage bootloader image in internal memory to where the code should execute from.
	191:160	32 bits	Header CRC	
Payload				variable length
		264 Bytes	BLp_header	Header for Security option. Set to “0” if not to use the security function.
		variable	2nd stage bootloader image	
		32 bits	Payload CRC	

Note 1. When downloading from NAND Flash, the Header will not have ECC but will check by CRC. The Payload will be ECC-protected using the scheme as specified in bits 41-63. The Header will be repeated 8 times since no ECC. i.e. the SPKG will consist of 8 Headers followed by 1 Payload.

Note 2. Bit 0 of execution offset is used to select Thumb® or Arm instruction for the 2nd Stage Bootloader (0 = Arm instruction, 1 = Thumb instruction).

The integrity of the boot image data from three sources (QSPI, NAND FLASH, USB) is taken account as following.

- NAND – Data stored in NAND FLASH will be verified integrity by CRC feature and is also able to use option to be safeguarded by the BCH ECC feature in the hardware. The ECC data is stored in the spare area of the NAND FLASH.
  - The bootloader accesses the data of header block in the NAND without ECC. The header block is read and verified using the header CRC value. Since the header is not subject to ECC, eight copies of the header are used to mitigate for errors.
  - Once a header is validated, the ECC parameter of the payload is configured.
  - The ECC parameter is user defined. The parameter used when writing the image to NAND FLASH should be reflected to SPKG header. The user should be free to decide on the level of ECC within what supported by the NAND Flash controller.
  - An SPKG should be located at the start of a page. The bootloader searches an SPKG from the first page in order.
- QuadSPI – This is less likely to contain errors, but will also be CRC checked to verify its integrity as part of the standard SPKG processing.
  - An SPKG should be located at the start of a page. The bootloader searches an SPKG from the first page in order.
- USB –The bootloader will also CRC check for the SPKG received via USB DFU. SPKG downloaded over USB is only one.

The SPKG verification is as follows:

- The header is located in the first of SPKG, and verified using header CRC value. When fail, the next header is used, if all 8 headers fail, the next SPKG is used. Then the process repeats until no errors. Failures in the CRC check will be reported as UART message. The bootloader process is halted if all SPKGs are invalid.
- The payload is verified by CRC check
- If an error is detected in SPKG, this will be reported as UART message.

In a multi Logical Unit (multi-LUN) Flash device, the Bootloader will use the images stored in the first LUN detected – LUN0.

7.5 RZ/N1 Initialize Sequence

7.5.1 Standard Initialize Sequence

1) Set programmable clock divider value by DIV of PWRCTRL_*DIV register.
2) Enable target clock by CLKEN_* bit of PWRCTRL_* register
3) De-assert reset for target function module by RSTN_* bit of PWRCTRL_* register.
4) Connect NoC interconnect by PWRCTRL_* and PWRSTAT_* registers.
   Refer to “Generic Programming Sequence for NoC” part
5) IO multiplexing configuration by rGPIOs_Level1_Config* and rGPIOs_Level2_Config* registers.
   Refer to “IO Multiplexing” chapter
6) Module initialize

7.5.2 USBPLL Setting

USBPLL can provide 48MHz clock for some modules besides USB. If the clock is necessary, following sequence is required.

1) Enable USB_HCLKH, USB_HCLKF, USB_HCLKPM and USB_PCICLK by CLKEN_* bit of PWRCTRL_USB register.
2) De-assert reset of USB by RSTN_* bit of PWRCTRL_USB register.
3) Connect NoC interconnect by PWRCTRL_USB and PWRSTAT_USB registers.
4) Enable FRCLK48MOD bit of CFG_USB register.
5) Disable DIRPD bit of CFG_USB register.
6) Wait 1ms.
7) De-assert PLL_RST bit of EPCTR register in USB Function.
8) Wait until PLL_LOCK bit of EPCTR register in USB Function is asserted.

7.5.3 Activating Cortex-M3

In case of RZ/N1D and RZ/N1S, Cortex-M3 reset is enabled after Cortex-A7 bootup.

Cortex-A7 needs to execute following sequence in order to activate Cortex-M3.

1) Enable RINBUS_HCLK by CLKEN_A of PWRCTRL_RINCTRL register.
2) Enable CM3_HCLK by CLKEN_A of PWRCTRL_CM3 register.
3) Release reset of Cortex-M3 by RSTN_A of PWRCTRL_CM3 register.
4) Connect NoC interconnect by PWRCTRL_CM3 and PWRSTAT_CM3 registers.

Then, Cortex-M3 boots up by the code placed at 0x0400_0000.

(In RZ/N1D and RZ/N1S, 0x0400_0000 – is mirrored to 0x0 by R-IN Engine internal structure)

7.5.4 Generic Programming Sequence for NoC

The following figure shows the programming sequence of the clock, reset and NoC connect/disconnect flow.

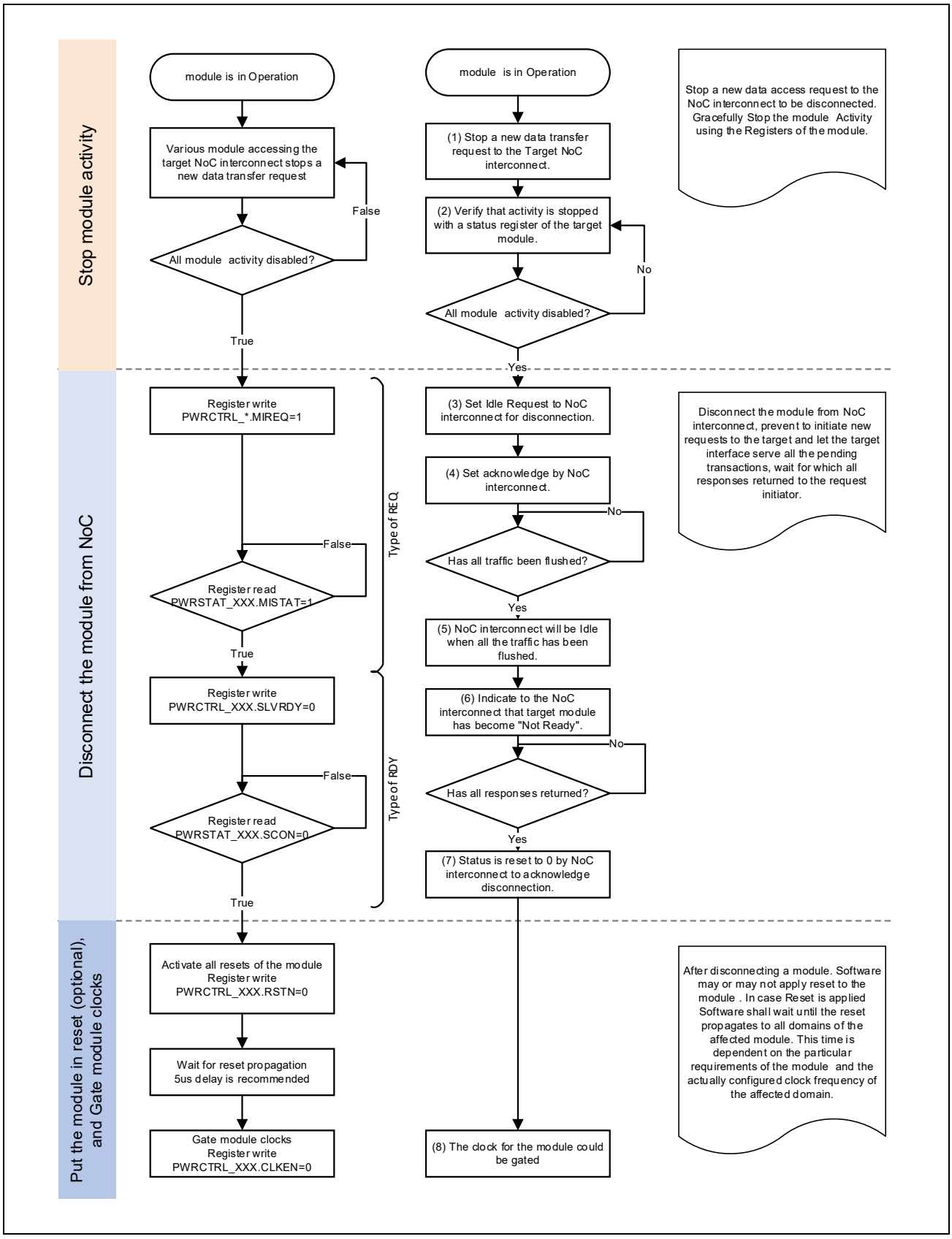


Figure 7.3 Generic Programming Sequence for NoC – Disconnect

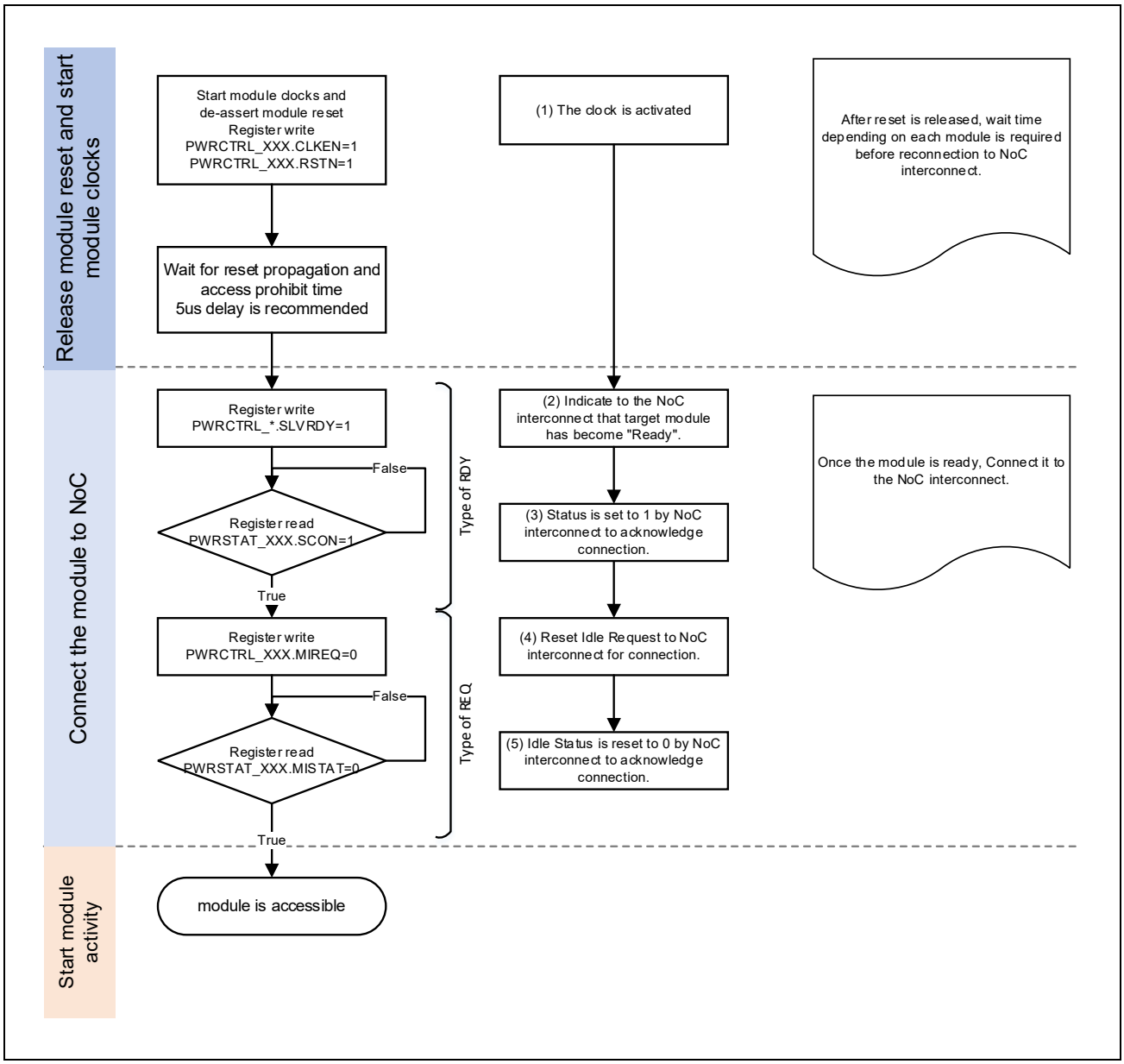


Figure 7.4 Generic Programming Sequence for NoC – Connect

The following table shows related PWRCTRL and PWRSTAT registers to make each module available.

There is no need to control PWRCTRL & PWRSTAT registers to access Watchdog for CA7/CM3, System Controller, ConfigSys1, 4MB SRAM with ECC Controller, CoreSight, Mailbox.

PWRCTRL_RINCTRL should be enabled before accessing registers since ECC registers of 2MB SRAM is running on a clock controlled by PWRCTRL_RINCTRL.

Table 7.3 Related Registers for Connect/Disconnect of Each module (1/2)

	PWRCTRL_XXX Register for NoC Connect (Type of REQ)		PWRCTRL_XXX Register for NoC Connect (Type of RDY)		PWRCTRL_XXX Register for module Interface
	MIREQ/MISTAT	CLKEN/RSTN	SLVRDY/SCON	CLKEN/RSTN	CLKEN/RSTN
MSEBIM			MSEBI	MSEBI	
ROM			ROM	ROM	
R-IN Engine Accessory Register			RINCTRL	RINCTRL	
Ethernet Accessory Register			SWITCHCTRL	SWITCHCTRL	SWITCHCTRL*1
A5PSW			SWITCH	SWITCH	SWITCH
QSPI1	QSPI1	QSPI1*2	QSPI1	QSPI1*2	QSPI1
QSPI2	QSPI2	QSPI2*2	QSPI2	QSPI2*2	QSPI2
I2C 1/2			PG0_0	PG0_0	PG0_1
UART 1/2/3*3			PG0_0	PG0_0	PG0_0
ADC 1/2			PG0_0	PG0_0	PG0_1
PWMTimer			PG0_1		PG0_1
UART 4/5*3			PG1_1	PG1_1	PG1_PR2
UART 6/7/8*3			PG1_2	PG1_2	PG1_PR2
SPI 1/2/3/4			PG1_1	PG1_1	PG1_PR3
SPI 5/6			PG1_1	PG1_1	PG1_PR4
CAN 1/2			PG3_48MHZ		PG3_48MHZ
ConfigSys2			PG2_25MHZ		PG2_25MHZ
TIMER 1/2			PG2_25MHZ		PG2_25MHZ
Semaphore			PG4	PG4	
BGPIO 1/2			PG1_1	PG1_1	
BGPIO 3			PG1_2	PG1_2	
LCDC	PG4	PG4	PG4	PG4	PG4_PR1
ETHERCAT	ECAT	ECAT			ECAT*4
SERCOSIII	SERCOS	SERCOS			SERCOS*4
HSR	HSR	HSR			HSR*4
DDR 2/3 Controller	DDRC	DDRC			DDRC
USB	USB*5	USB*5			USB
Cortex-M3*6	CM3	CM3			
MSEBIS	MSEBI	MSEBI*2	MSEBI	MSEBI*2	
DMAC 1/2	DMA	DMA*2	DMA	DMA*2	
GMAC1	MAC1	MAC1*2	MAC1	MAC1*2	
GMAC2	MAC2	MAC2*2	MAC2	MAC2*2	

Table 7.3 Related Registers for Connect/Disconnect of Each module (2/2)

	PWRCTRL_XXX Register for NoC Connect (Type of REQ)		PWRCTRL_XXX Register for NoC Connect (Type of RDY)		PWRCTRL_XXX Register for module Interface
	MIREQ/MISTAT	CLKEN/RSTN	SLVRDY/SCON	CLKEN/RSTN	CLKEN/RSTN
SDIO1	SDIO1	SDIO1*2	SDIO1	SDIO1*2	SDIO1
SDIO2	SDIO2	SDIO2*2	SDIO2	SDIO2*2	SDIO2
NAND Flash Controller	NFLASH	NFLASH*2	NFLASH	NFLASH*2	NFLASH
RTC*7	RTC	RTC			RTC
External Ethernet Clock					EETH*8
HW-RTOS					HWRTOS*9

Note 1. 2xRSTNs (RSTN_ETH, RSTN_CLK25)

Note 2. CLKEN/RSTN are common for both type

Note 3. Main PLL or USBPLL are selectable for clock source

Note 4. 2xCLKENs, 1xRSTN

Note 5. 2xMIREQs, 3xCLKENs, 1xRSTN

Note 6. PWRCTRL_RINCTRL should be enabled before PWRCTRL_CM3

Note 7. Special sequence is required for RTC
Release RST_RTC → Enable RTC_PCLK → Release RSTN_FW_RTC → Release IDLE_REQ
CLKEN_RTC should be enabled during RTC access only

Note 8. CLKEN for MII REFCLK (External output), RMII REFCLK (External output) and RGMII REFCLK (External input)

Note 9. CLKEN/RST for HW-RTOS and CLKEN for HW-RTOS GMAC MDC

Section 8 Ethernet Interface Modes

8.1 Overview

Several modules for Ethernet protocols, GMII/MII Multiplexing logic and RGMII/RMII Converters are in Ethernet Peripherals part. This chapter provides the information about available Ethernet Peripherals part configuration.

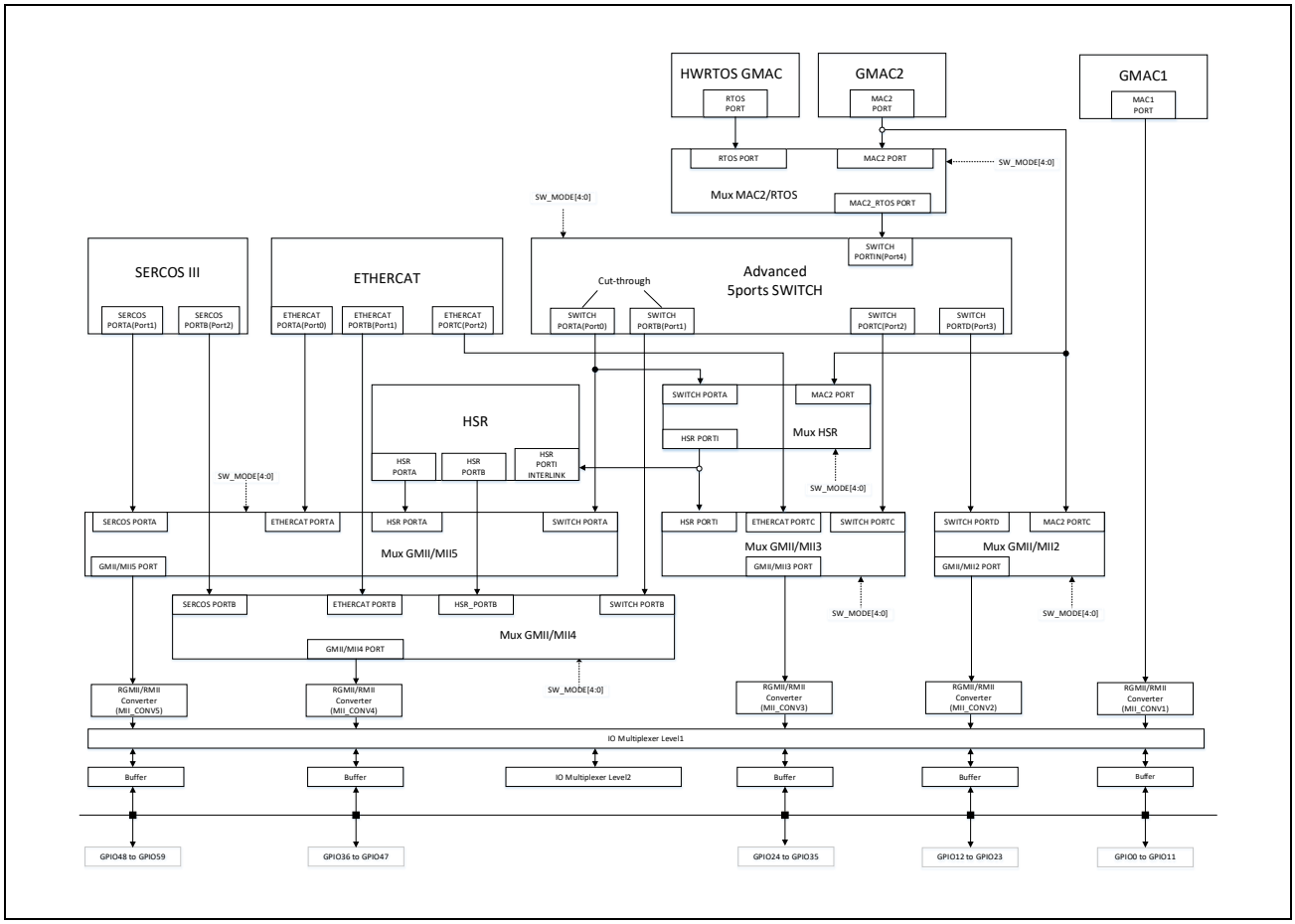


Figure 8.1 Ethernet Peripherals Part Structure

Table 8.1 Supported Ethernet Port

	RZ/N1D		RZ/N1S		RZ/N1L
Ethernet Port	BGA-400	BGA-324	BGA-324	BGA-196	BGA-196
Port 1	✓	N/A	✓	✓	✓
Port 2	✓	N/A	✓	N/A	N/A
Port 3	✓	✓	✓	N/A	N/A
Port 4	✓	✓	✓	✓	✓
Port 5	✓	✓	✓	✓	✓

Note: Please refer to **Section 8.2.1, Internal Connection of Ethernet Ports** about SW_MODE[4:0] in the above figure. However, the available setting is different for each product.

The following registers are used for configuring RGMII/RMII Converter and multiplex of Ethernet Peripherals part.

Please refer to UM for R-IN Engine and Ethernet Peripherals.

Table 8.2 Operation Mode Control Registers

Address	Register Symbol	Register Name
4403 0008h	MODCTRL	Mode Control register
4403 000Ch	PTPMCTRL	PTP Mode Control register
4403 0100h	CONVCTRL1	RGMII/RMII Converter1 Control register
4403 0104h	CONVCTRL2	RGMII/RMII Converter2 Control register
4403 0108h	CONVCTRL3	RGMII/RMII Converter3 Control register
4403 010Ch	CONVCTRL4	RGMII/RMII Converter4 Control register
4403 0110h	CONVCTRL5	RGMII/RMII Converter5 Control register

8.2 Support Modes

Table 8.3 Support Modes of Ethernet I/F

Ethernet I/F Mode		After Conversion	Before Conversion	Communication Mode		Register Value			
						RGMII/RMII Converter			RGMII Clock Selector
No.	Mode Name	MII /RMII /RGMII	MII /GMII	Speed [bps]	Full Duplex /Half Duplex	CONVCTRL[m]. CONV_MODE (m = 1 to 5)	CONVCTRL[m]. FULLD (m = 1 to 5)	CONVCTRL[m]. RMII_CRS_MODE (m = 1 to 5)	PTPMCTRL. RGMII_CLKSEL
1	MII_10M_HALF	MII	MII	10 M	Half	5'b00000	1'b0	1'b1	1'b0
2	MII_10M_FULL	MII	MII	10 M	Full	5'b00000	1'b1	1'b1	1'b0
3	MII_100M_HALF	MII	MII	100 M	Half	5'b00000	1'b0	1'b1	1'b0
4	MII_100M_FULL	MII	MII	100 M	Full	5'b00000	1'b1	1'b1	1'b0
5	RMII_10M_HALF_RI	RMII	MII	10 M	Half	5'b00100	1'b0	1'b1	1'b0
6	RMII_10M_FULL_RI	RMII	MII	10 M	Full	5'b00100	1'b1	1'b1	1'b0
7	RMII_100M_HALF_RI	RMII	MII	100 M	Half	5'b00101	1'b0	1'b1	1'b0
8	RMII_100M_FULL_RI	RMII	MII	100 M	Full	5'b00101	1'b1	1'b1	1'b0
9	RMII_10M_HALF_RO	RMII	MII	10 M	Half	5'b10100	1'b0	1'b1	1'b0
10	RMII_10M_FULL_RO	RMII	MII	10 M	Full	5'b10100	1'b1	1'b1	1'b0
11	RMII_100M_HALF_RO	RMII	MII	100 M	Half	5'b10101	1'b0	1'b1	1'b0
12	RMII_100M_FULL_RO	RMII	MII	100 M	Full	5'b10101	1'b1	1'b1	1'b0
13	RGMII_10M_HALF_RI	RGMII	MII	10 M	Half	5'b01000	1'b0	1'b1	1'b1
14	RGMII_10M_FULL_RI	RGMII	MII	10 M	Full	5'b01000	1'b1	1'b1	1'b1
15	RGMII_100M_HALF_RI	RGMII	MII	100 M	Half	5'b01001	1'b0	1'b1	1'b1
16	RGMII_100M_FULL_RI	RGMII	MII	100 M	Full	5'b01001	1'b1	1'b1	1'b1
17	RGMII_1G_HALF_RI	RGMII	GMII	1 G	Half	5'b01010	1'b0	1'b1	1'b1
18	RGMII_1G_FULL_RI	RGMII	GMII	1 G	Full	5'b01010	1'b1	1'b1	1'b1
19	RGMII_10M_HALF	RGMII	MII	10 M	Half	5'b01000	1'b0	1'b1	1'b0
20	RGMII_10M_FULL	RGMII	MII	10 M	Full	5'b01000	1'b1	1'b1	1'b0
21	RGMII_100M_HALF	RGMII	MII	100 M	Half	5'b01001	1'b0	1'b1	1'b0
22	RGMII_100M_FULL	RGMII	MII	100 M	Full	5'b01001	1'b1	1'b1	1'b0
23	RGMII_1G_HALF	RGMII	GMII	1 G	Half	5'b01010	1'b0	1'b1	1'b0
24	RGMII_1G_FULL	RGMII	GMII	1 G	Full	5'b01010	1'b1	1'b1	1'b0

Table 8.4 Clock I/F for Ethernet PHY (Part 1)

Clocks \ No. & Mode Name		1	2	3	4
		MII_10M_HALF	MII_10M_FULL	MII_100M_HALF	MII_100M_FULL
Reference Clock	Direction	output to PHY			
	Clock Signal Name	MII_REFCLK			
	Frequency [MHz]	25			
Transmit Clock	Direction	Input from PHY			
	Clock Signal Name	GMII[m]_TXCLK (m = 1..5)			
	Frequency [MHz]	2.5		25	
Receive Clock	Direction	Input from PHY			
	Clock Signal Name	GMII[m]_RXCLK (m = 1..5)			
	Frequency [MHz]	2.5		25	

Table 8.5 Clock I/F for Ethernet PHY (Part 2)

Clocks \ No. & Mode Name		5	6	7	8
		RMII_10M_HALF_RI	RMII_10M_FULL_RI	RMII_100M_HALF_RI	RMII_100M_FULL_RI
Reference Clock	Direction	Input from PHY			
	Clock Signal Name	GMII[m]_RXCLK (m = 1..5)			
	Frequency [MHz]	50			
Transmit Clock	Direction	Reference Clock is used			
	Clock Signal Name				
	Frequency [MHz]				
Receive Clock	Direction	Reference Clock is used			
	Clock Signal Name				
	Frequency [MHz]				

Table 8.6 Clock I/F for Ethernet PHY (Part 3)

Clocks \ No. & Mode Name		9	10	11	12
		RMII_10M_HALF_RO	RMII_10M_FULL_RO	RMII_100M_HALF_RO	RMII_100M_FULL_RO
Reference Clock	Direction	Output to PHY			
	Clock Signal Name	RMII_REFCLK			
	Frequency [MHz]	50			
Transmit Clock	Direction	Reference Clock is used			
	Clock Signal Name				
	Frequency [MHz]				
Receive Clock	Direction	Reference Clock is used			
	Clock Signal Name				
	Frequency [MHz]				

Table 8.7 Clock I/F for Ethernet PHY (Part 4)

Clocks \ No. & Mode Name		13	14	15	16
		RGMII_10M_HALF_RI	RGMII_10M_FULL_RI	RGMII_100M_HALF_RI	RGMII_100M_FULL_RI
Reference Clock	Direction	Input from external oscillator			
	Clock Signal Name	RGMII_REFCLK			
	Frequency [MHz]	125			
Transmit Clock	Direction	Output to PHY			
	Clock Signal Name	GMII[m]_TXCLK (m = 1..5)			
	Frequency [MHz]	2.5		25	
Receive Clock	Direction	Input from PHY			
	Clock Signal Name	GMII[m]_RXCLK (m = 1..5)			
	Frequency [MHz]	2.5		25	

Table 8.8 Clock I/F for Ethernet PHY (Part 5)

Clocks \ No. & Mode Name		17	18
		RGMII_1G_HALF_RI	RGMII_1G_FULL_RI
Reference Clock	Direction	Input from external oscillator	
	Clock Signal Name	RGMII_REFCLK	
	Frequency [MHz]	125	
Transmit Clock	Direction	Output to PHY	
	Clock Signal Name	GMII[m]_TXCLK (m = 1..5)	
	Frequency [MHz]	125	
Receive Clock	Direction	Input from PHY	
	Clock Signal Name	GMII[m]_RXCLK (m = 1..5)	
	Frequency [MHz]	125	

Table 8.9 Clock I/F for Ethernet PHY (Part 6)

Clocks \ No. & Mode Name		19	20	21	22
		RGMII_10M_HALF	RGMII_10M_FULL	RGMII_100M_HALF	RGMII_100M_FULL
Reference Clock	Direction	—			
	Clock Signal Name	—			
	Frequency [MHz]	—			
Transmit Clock	Direction	Output to PHY			
	Clock Signal Name	GMII[m]_TXCLK (m = 1..5)			
	Frequency [MHz]	2.5		25	
Receive Clock	Direction	Input from PHY			
	Clock Signal Name	GMII[m]_RXCLK (m = 1..5)			
	Frequency [MHz]	2.5		25	

Table 8.10 Clock I/F for Ethernet PHY (Part 7)

Clocks \ No. & Mode Name		23	24
		RGMII_1G_HALF	RGMII_1G_FULL
Reference Clock	Direction	—	
	Clock Signal Name	—	
	Frequency [MHz]	—	
Transmit Clock	Direction	Output to PHY	
	Clock Signal Name	GMII[m]_TXCLK (m = 1..5)	
	Frequency [MHz]	125	
Receive Clock	Direction	Input from PHY	
	Clock Signal Name	GMII[m]_RXCLK (m = 1..5)	
	Frequency [MHz]	125	

Table 8.11 Support Modes for Each Module

Ethernet I/F Mode		Support Modes for Each Module					
			A5PSW Port A/B/C/D				
No.	Mode Name	GMAC1/2	Store and Forward/ Cut Through	HUB Mode	ETHERCAT Port A/B/C	SERCOSIII Port A/B	HSR Port A/B InterLink*1
1	MII_10M_HALF	Yes	Yes	No	No	No	No
2	MII_10M_FULL	Yes	Yes	No	No	No	No
3	MII_100M_HALF	Yes	Yes	No	No	No	No
4	MII_100M_FULL	Yes	Yes	No	Yes*2	Yes	Yes
5	RMII_10M_HALF_RI	Yes	Yes	No	No	No	No
6	RMII_10M_FULL_RI	Yes	Yes	No	No	No	No
7	RMII_100M_HALF_RI	Yes	Yes	No	No	No	No
8	RMII_100M_FULL_RI	Yes	Yes	No	Yes*3	Yes	Yes
9	RMII_10M_HALF_RO	Yes	Yes	No	No	No	No
10	RMII_10M_FULL_RO	Yes	Yes	No	No	No	No
11	RMII_100M_HALF_RO	Yes	Yes	Yes	No	No	No
12	RMII_100M_FULL_RO	Yes	Yes	No	Yes	Yes	Yes
13	RGMII_10M_HALF_RI	Yes	Yes	No	No	No	No
14	RGMII_10M_FULL_RI	Yes	Yes	No	No	No	No
15	RGMII_100M_HALF_RI	Yes	Yes	No	No	No	No
16	RGMII_100M_FULL_RI	Yes	Yes	No	No	No	No
17	RGMII_1G_HALF_RI	Yes	No	No	No	No	No
18	RGMII_1G_FULL_RI	Yes	Yes	No	No	No	No
19	RGMII_10M_HALF	Yes	Yes	No	No	No	No
20	RGMII_10M_FULL	Yes	Yes	No	No	No	No
21	RGMII_100M_HALF	Yes	Yes	No	No	No	No
22	RGMII_100M_FULL	Yes	Yes	No	No	No	No
23	RGMII_1G_HALF	Yes	No	No	No	No	No
24	RGMII_1G_FULL	Yes	Yes	No	No	No	No

Note 1. Port InterLink is only supported when connected to external port (MODCTRL.SW_MODE[4:0] = 5'b11110).

Note 2. Reference Clock of input GMII[m]_TXCLK (m = 3..5) must be synchronized to output clock of MII_REFCLK when ETHERCAT is used.

Note 3. Reference Clock of input GMII[m]_RXCLK (m = 3..5) must be synchronized to output clock of RMII_REFCLK when ETHERCAT is used.

8.2.1 Internal Connection of Ethernet Ports

Internal connection of Ethernet ports are controlled by Mode Control register (MODCTRL) of Ethernet Accessory Register as follows.

Table 8.12 Internal Connection of Ethernet Ports

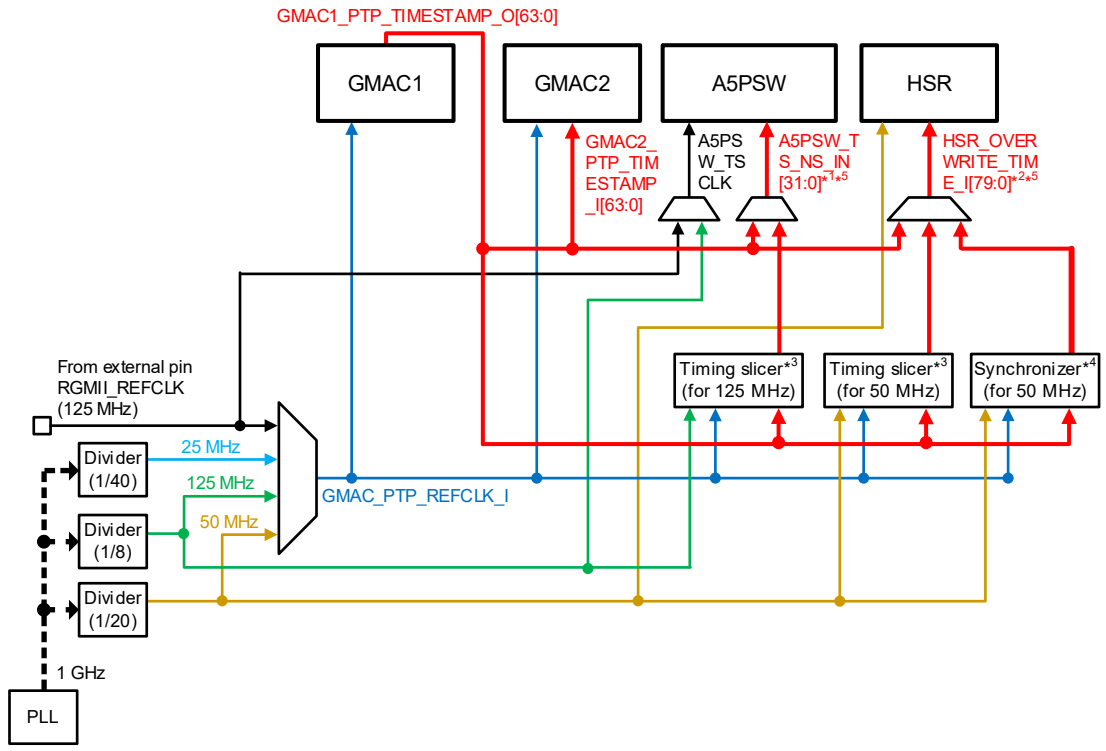
Mode Control Register		Internal Connection of Ethernet Ports						
MODCTRL. SW_MODE[4:0]								
decimal	binary	HSR PORTI INTERLINK	SWITCH PORTIN (A5PSW Management Port)	MII_CONV1	MII_CONV2	MII_CONV3	MII_CONV4	MII_CONV5
0	5'b00000	—	RTOS PORT	MAC1 PORT	SWITCH PORTD	SWITCH PORTC	SERCOS PORTB	SERCOS PORTA
1	5'b00001	—	RTOS PORT	MAC1 PORT	SWITCH PORTD	SWITCH PORTC	ETHERCAT PORTB	ETHERCAT PORTA
2	5'b00010	—	RTOS PORT	MAC1 PORT	SWITCH PORTD	ETHERCAT PORTC	ETHERCAT PORTB	ETHERCAT PORTA
3	5'b00011	—	RTOS PORT	MAC1 PORT	SWITCH PORTD	SWITCH PORTC	SWITCH PORTB	SWITCH PORTA
4 to 7	5'b00100 to 5'b00111	Reserved (Do not use)						
8	5'b01000	—	RTOS PORT	MAC1 PORT	MAC2 PORT	SWITCH PORTC	SERCOS PORTB	SERCOS PORTA
9	5'b01001	—	RTOS PORT	MAC1 PORT	MAC2 PORT	SWITCH PORTC	ETHERCAT PORTB	ETHERCAT PORTA
10	5'b01010	—	RTOS PORT	MAC1 PORT	MAC2 PORT	ETHERCAT PORTC	ETHERCAT PORTB	ETHERCAT PORTA
11	5'b01011	—	RTOS PORT	MAC1 PORT	MAC2 PORT	SWITCH PORTC	SWITCH PORTB	SWITCH PORTA
12 to 15	5'b01100 to 5'b01111	Reserved (Do not use)						
16	5'b10000	—	MAC2 PORT	MAC1 PORT	SWITCH PORTD	SWITCH PORTC	SERCOS PORTB	SERCOS PORTA
17	5'b10001	—	MAC2 PORT	MAC1 PORT	SWITCH PORTD	SWITCH PORTC	ETHERCAT PORTB	ETHERCAT PORTA
18	5'b10010	—	MAC2 PORT	MAC1 PORT	SWITCH PORTD	ETHERCAT PORTC	ETHERCAT PORTB	ETHERCAT PORTA
19	5'b10011	—	MAC2 PORT	MAC1 PORT	SWITCH PORTD	SWITCH PORTC	SWITCH PORTB	SWITCH PORTA
20 to 27	5'b10100 to 5'b11011	Reserved (Do not use)						
28	5'b11100	—	MAC2 PORT	MAC1 PORT	SWITCH PORTD	SWITCH PORTC	HSR PORTB	HSR PORTA
29	5'b11101	SWITCH PORTA	MAC2 PORT	MAC1 PORT	SWITCH PORTD	SWITCH PORTC	HSR PORTB	HSR PORTA
30	5'b11110	MII_CONV3	MAC2 PORT	MAC1 PORT	SWITCH PORTD	HSR PORTI INTERLINK	HSR PORTB	HSR PORTA
31	5'b11111	MAC2 PORT	—	MAC1 PORT	—	—	HSR PORTB	HSR PORTA

8.2.2 Selection of clocks for PTP

Clocks for PTP are selected by PTP Mode Control register (PTPMCTRL) of Ethernet Accessory Register.

"**Table 8.13, Selection of Clocks for PTP**" shows clock setting for each PTP and "**Table 8.14, Recommended Setting of PTP_MODE**" shows the recommended value for MODCTRL.SW_MODE bits.

For the PTP function of each module, please refer to "Programming Guidelines for IEEE 1588 Timestamping" and "Timestamping Functions (TSM)" in UM for R-IN Engine and Ethernet Peripherals.



Note 1. Bit map for Advanced 5 port Switch is below.
A5PSW_TS_NS_IN[31:30] = 00b
A5PSW_TS_NS_IN[29:0] = GMAC1_PTP_TIMESTAMP_O[29:0]

Note 2. Bit map for HSR is below.
HSR_OVERWRITE_TIME_I[79:64] = 0000h
HSR_OVERWRITE_TIME_I[63:32] = GMAC1_PTP_TIMESTAMP_O[63:32]
HSR_OVERWRITE_TIME_I[31:30] = 00b
HSR_OVERWRITE_TIME_I[29:0] = GMAC1_PTP_TIMESTAMP_O[29:0]

Note 3. Timing slicer is a synchronous bridge to convert clock frequency.

Note 4. Synchronizer is an asynchronous bridge to convert clock frequency.

Note 5. In order to validate, release the reset by RSTN_CLK25 in PWRCTRL_SWITCHCTRL register.

Figure 8.2 Selection of Clocks for PTP by PTPMCTRL Register

Table 8.13 Selection of Clocks for PTP

	GMAC1	GMAC2	A5PSW		HSR		
PTPMCTRL.PTP_MODE[3:0]	GMAC_PTP_REFCLK_I	GMAC_PTP_REFCLK_I	Clock for PTP (A5PSW_TSCLK)	Timing Slicer	Clock for PTP	Synchronizer	Timing Slicer
O 4'b0000	Stop	Stop	Stop	Disable	Disable	Disable	Disable
A 4'b0001	RGMII_REFCLK (125 MHz from external pin)	RGMII_REFCLK (125 MHz from external pin)	RGMII_REFCLK (125 MHz from external pin)	Disable	50 MHz (from PLL source)	Enable	Disable
B 4'b0010	125 MHz (from PLL source)	125 MHz (from PLL source)	125 MHz (from PLL source)	Disable	50 MHz (from PLL source)	Disable	Enable
C 4'b0011	50 MHz (from PLL source)	50 MHz (from PLL source)	125 MHz (from PLL source)	Enable	50 MHz (from PLL source)	Disable	Disable
D 4'b0100	25 MHz (from PLL source)	25 MHz (from PLL source)	125 MHz (from PLL source)	Enable	50 MHz (from PLL source)	Disable	Enable

Table 8.14 Recommended Setting of PTP_MODE

Mode Control Register		PTP Mode Control Register			
		Recommended Value of PTPMCTRL.PTP_MODE[3:0]			
		When High-Accuracy is required for PTP-Timer		When Low-Power is required for PTP-Timer	When No PTP-Timer is used
MODCTRL.SW_MODE[4:0]		When RGMII_REFCLK is used (PTPMCTRL.RGMII_CLKSEL = 1)	when No RGMII_REFCLK is used (PTPMCTRL.RGMII_CLKSEL = 0)		
decimal	binary	Symbol	Symbol	Symbol	Symbol
0	5'b00000	A	B	D	O
1	5'b00001	A	B	D	O
2	5'b00010	A	B	D	O
3	5'b00011	A	B	D	O
4 to 7	5'b00100 to 5'b00111	Reserved (Do not set)			
8	5'b01000	A	B	D	O
9	5'b01001	A	B	D	O
10	5'b01010	A	B	D	O
11	5'b01011	A	B	D	O
12 to 15	5'b01100 to 5'b01111	Reserved (Do not set)			
16	5'b10000	A	B	D	O
17	5'b10001	A	B	D	O
18	5'b10010	A	B	D	O
19	5'b10011	A	B	D	O
20 to 27	5'b10100 to 5'b11011	Reserved (Do not set)			
28	5'b11100	B	B	C	O
29	5'b11101	B	B	C	O
30	5'b11110	B	B	C	O
31	5'b11111	B	B	C	O

The timestamp processing and configuration example in PTP are shown as below.

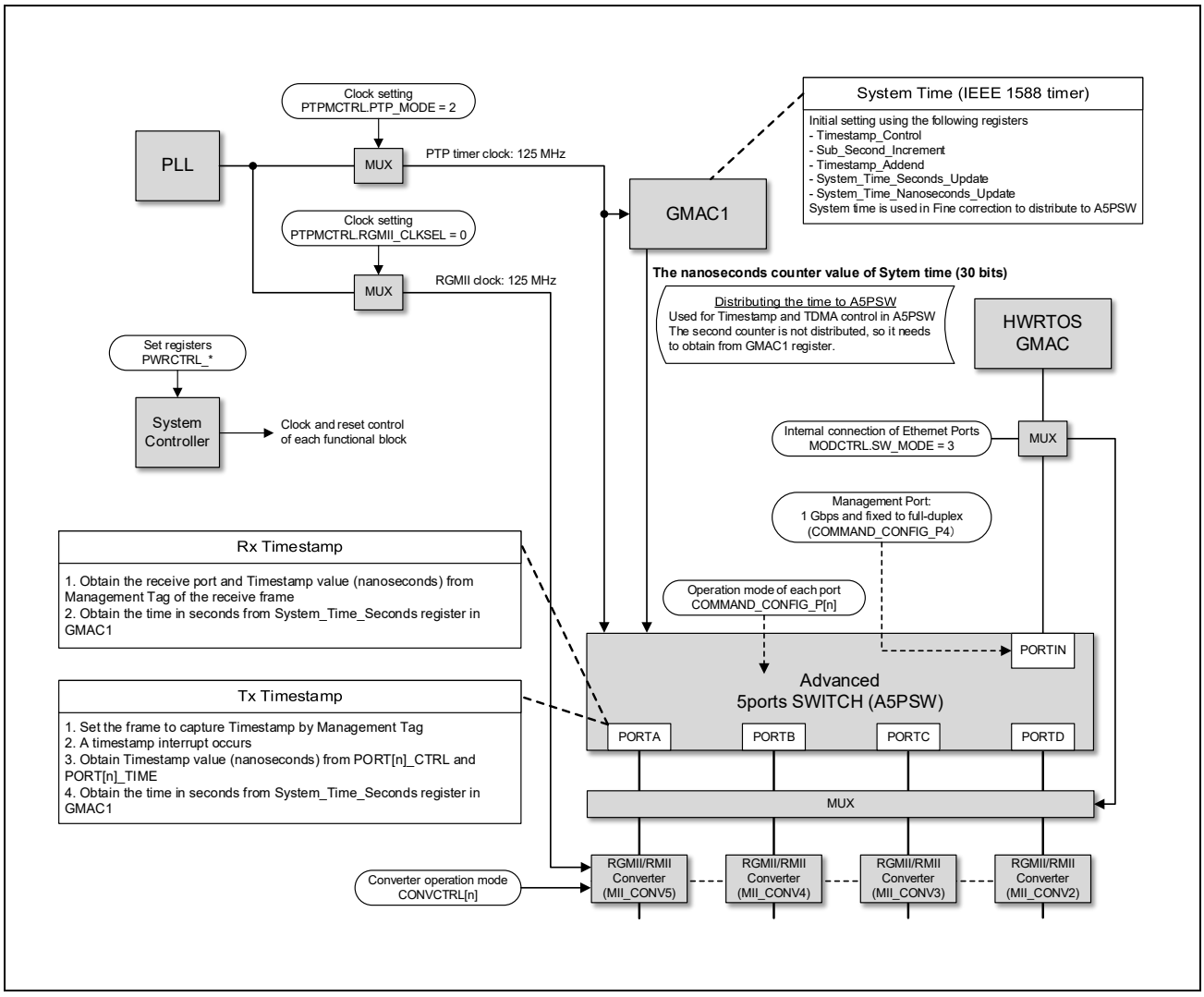


Figure 8.3 Configuration example in PTP

8.3 Operation

8.3.1 Initializing

Example sequence for using Ethernet is shown as below.

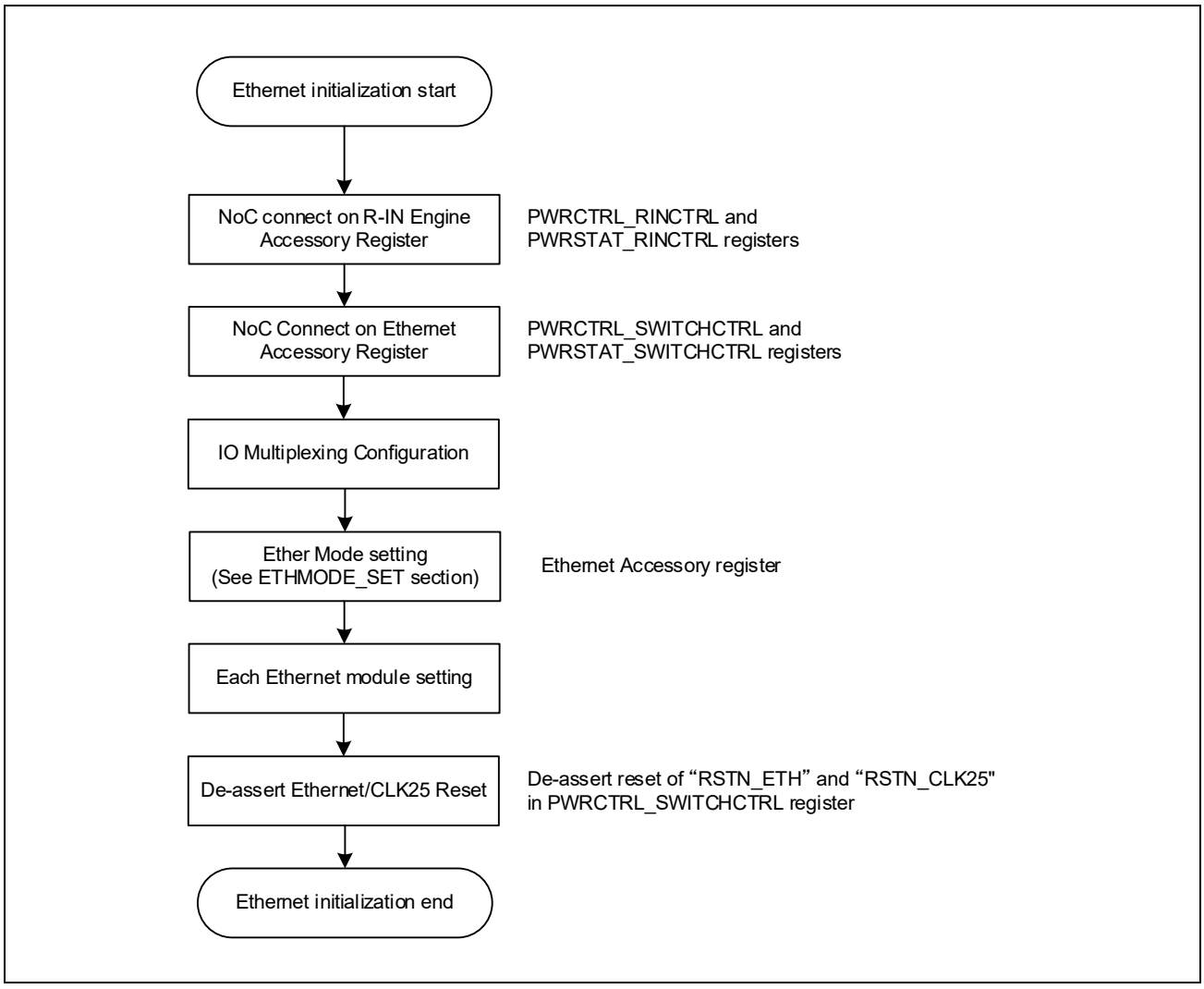
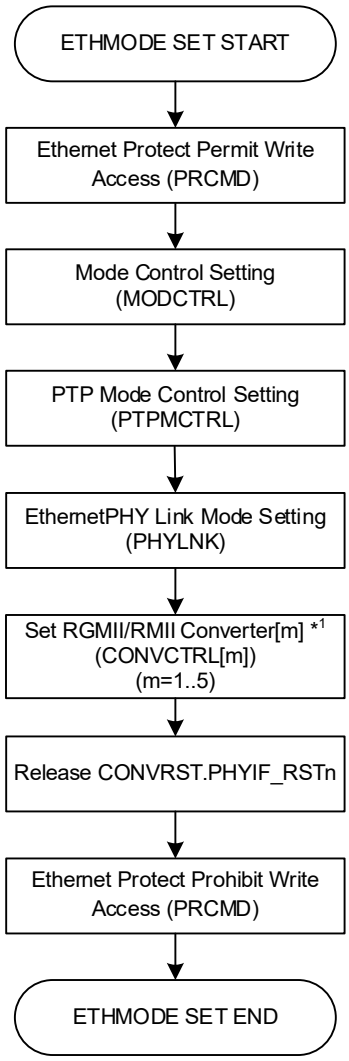


Figure 8.4 Initializing of Ethernet Flowchart

8.3.2 ETHMODE_SET

For ETHMODE_SET operation, complete the following flowchart:



Note: See Register Description in Ethernet Accessory Register.

Note 1. If ethernet port1 is not used, set RGMII/RMII Converter1 = 0000_0115h. Without this setting, PTP circuit doesn't work. For example, RZ/N1D-324 doesn't have the port1, therefore this setting is essential.

Figure 8.5 ETHMODE_SET Flowchart

8.4 Usage Notes

8.4.1 Restriction

- SERCOSIII, ETHERCAT and HSR function are not available simultaneously.
- HW-RTOS GMAC and HSR are not available simultaneously.
- HSR is available only in RZ/N1D.
- RZ/N1D-324 can only use port3, port4, and port5.
- RZ/N1S-196 and RZ/N1L can only use port1, port4, and port5.

8.4.1.1 Supported Ethernet Signals

Table 8.15 Ethernet Signals for Each PHY Mode

Signal Name	MII Mode	RMII Mode	RGMII Mode	Remark
GMII[m]_TXCLK	TX_CLK	Not use	TXC	
GMII[m]_TXD0	TXD0	TXD0	TXD0	
GMII[m]_TXD1	TXD1	TXD1	TXD1	
GMII[m]_TXD2	TXD2	Not use	TXD2	
GMII[m]_TXD3	TXD3	Not use	TXD3	
GMII[m]_TXEN	TX_EN	TX_EN	TX_CTL	
GMII[m]_TXER	TX_ER	Not use	Not use	Port1 of RZ/N1S-196 and RZ/N1L doesn't have it.
GMII[m]_RXCLK	RX_CLK	REF_CLK	RXC	
GMII[m]_RXD0	RXD0	RXD0	RXD0	
GMII[m]_RXD1	RXD1	RXD1	RXD1	
GMII[m]_RXD2	RXD2	Not use	RXD2	
GMII[m]_RXD3	RXD3	Not use	RXD3	
GMII[m]_RXDV	RX_DV	CRS_DV	RX_CTL	
GMII[m]_RXER	RX_ER	RX_ER (option)	Not use	Port1 of RZ/N1S-196 and RZ/N1L doesn't have it.
GMII[m]_CRS	CRS	Not use	Not use	Port1 of RZ/N1S-196 and RZ/N1L doesn't have it.
GMII[m]_COL	COL	Not use	Not use	Port1 of RZ/N1S-196 and RZ/N1L doesn't have it.

Note: m = 1..5.

Section 9 Interrupts

9.1 Overview

RZ/N1 has Cortex-A7 GICv2 and Cortex-M3 NVIC as an interrupt controller.

9.1.1 Cortex-A7 GICv2

The GIC collates and arbitrates from a large number of interrupt sources. It provides:

- Masking of interrupts
- Prioritization of interrupts
- Distribution of the interrupts to the target processors nIRQ and nFIQ
- Tracking the status of interrupts
- Generation of interrupts by software
- Support for Security Extensions
- Support for Virtualization Extensions
- Support for 160 standard interrupt sources
- The GIC is compliant with the version 2.0 of the Arm Generic Interrupt Controller (GIC) Architecture Specification

Please refer to "*CoreLink™ GIC-400 Generic Interrupt Controller Technical Reference Manual*" on Arm website.

9.1.2 Cortex-M3 NVIC

The NVIC main features are listed below:

- Masking of interrupts
- Prioritization of interrupts
- Generation of interrupts by software
- Facilitates low latency interrupt (The NVIC and the processor core interface are closely coupled). The NVIC maintains knowledge of the stacked (nested) interrupts to enable multiple interrupts
- Controls power management
- Support for 240 standard interrupt sources with up to 256 levels of priority
- NMI Interrupt controlled from external IO

Please refer to "*Cortex-M3 Technical Reference Manual*" on Arm website.

9.2 Operation

9.2.1 IRQ Synchronization

RZ/N1 System Controller receives all the IRQ signals from all sources and it delivers to Cortex-A7 GIC, Cortex-M3 NVIC and to HW-RTOS. The following IRQ handling categories are differentiated.

- Cortex-A7 GIC has synchronization logic.
- RZ/N1 System Controller has a synchronization logic for Cortex-M3 and HW-RTOS on all interrupt. Therefore, Cortex-M3 and HW-RTOS receives synchronized interrupt signals.
- Ethernet peripherals share certain interrupt (IRQ 49..52) the combination of these IRQs

9.2.2 Non Maskable Interrupt

The Cortex-M3 CPU has a non-maskable interrupt input. This interrupt is able to be assigned to external pin by the IO multiplexing.

9.2.3 Interrupt Management on Cortex-A7 and Cortex-M3

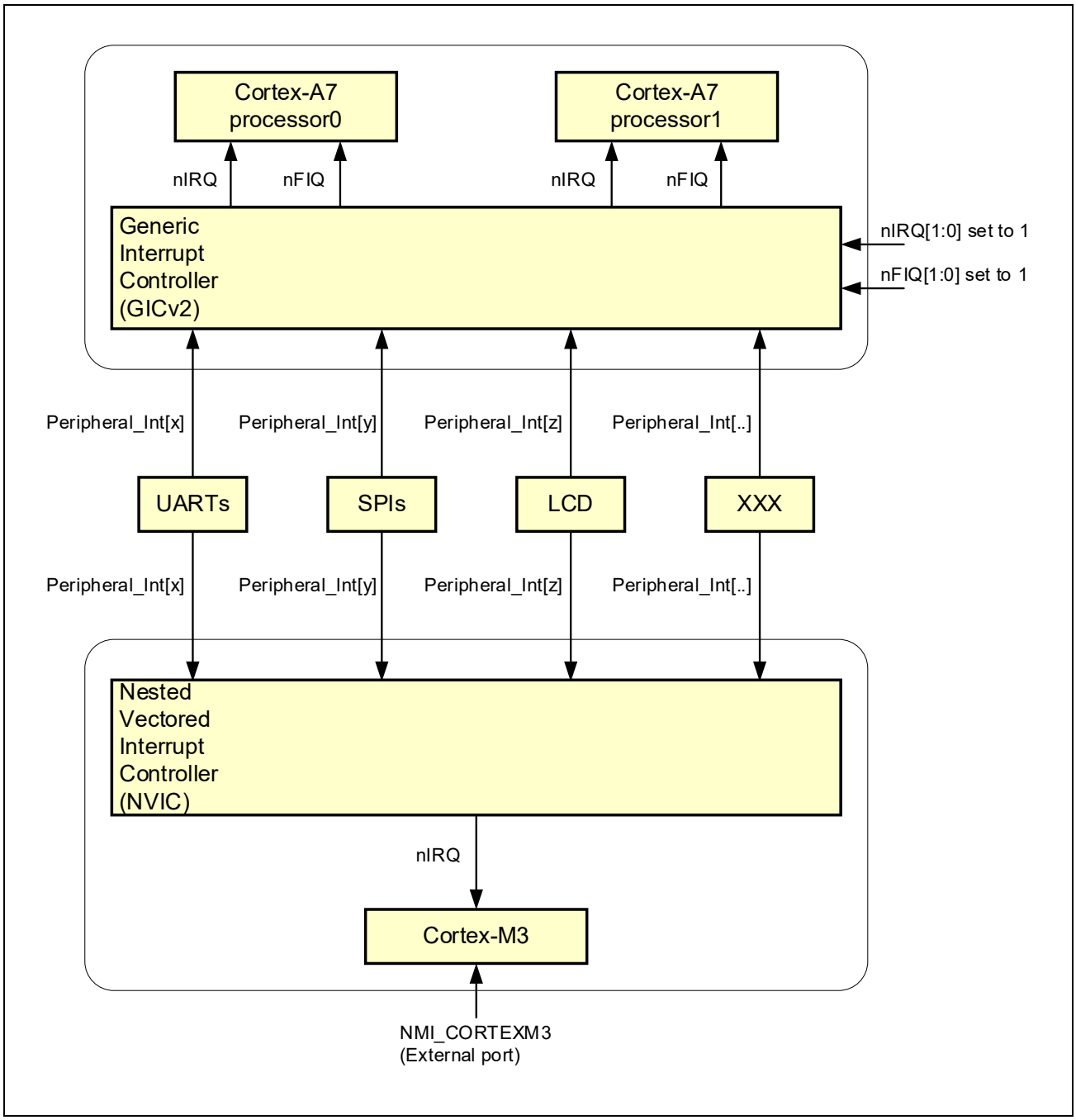


Figure 9.1 Interrupt Management on Cortex-A7 and Cortex-M3

9.2.4 Interrupts Allocation and Vector Number

Table 9.1 Interrupts Allocation and Vector Number (1/4)

IRQ [Index]	IRQ	N1D		N1S		N1L	Description
		CA7	CM3	CA7	CM3	CM3	
0	ADC_Int	✓	✓	✓	✓	✓	ADC interrupt
1	I2C1_Int	✓	✓	✓	✓	✓	I2C1 interrupt
2	I2C2_Int	✓	✓	✓	✓	✓	I2C2 interrupt
3	Reserved	—	—	—	—	—	Reserved
4	Reserved	—	—	—	—	—	Reserved
5	Reserved	—	—	—	—	—	Reserved
6	UART1_Int	✓	✓	✓	✓	✓	UART1 interrupt
7	UART2_Int	✓	✓	✓	✓	✓	UART2 interrupt
8	UART3_Int	✓	✓	✓	✓	✓	UART3 interrupt
9	Reserved	—	—	—	—	—	Reserved
10	PWM_Int	✓	✓	✓	✓	✓	PWMTimer interrupt
11	ECC_4MB_Int	—	—	✓	✓	✓	ECC error detected and not corrected on 4MB SRAM
12	ECC_2MB_Int	✓	✓	✓	✓	✓	ECC error detected and not corrected on 2MB SRAM
13	CM3_LOCKUP_Int	✓	—	✓	—	—	Cortex-M3 lockup
14	CM3_TRING_Int[0]	✓	✓	✓	✓	—	Trigger Interrupt0 (Cross Trigger Interface for Cortex-M3)
15	CM3_TRING_Int[1]	✓	✓	✓	✓	—	Trigger Interrupt1 (Cross Trigger Interface for Cortex-M3)
16	HWRTOS_BRAMERR_Int	—	✓	—	✓	✓	HW-RTOS GMAC Buffer RAM area access error
17	HWRTOS_BUFDMA_Int	—	✓	—	✓	✓	HW-RTOS GMAC InterBuffer DMA transfer completion
18	HWRTOS_BUFDMAERR_Int	—	✓	—	✓	✓	HW-RTOS GMAC InterBuffer DMA error
19	HWRTOS_ETHMMAI_Int	—	✓	—	✓	✓	HW-RTOS GMAC MII management access completion interrupt
20	HWRTOS_ETHPPIT_Int	—	✓	—	✓	✓	HW-RTOS GMAC pause packet transmission completion
21	HWRTOS_ETHDRIE_Int	—	✓	—	✓	✓	HW-RTOS GMAC MACDMA reception error
22	HWRTOS_ETHDMAIR_Int	—	✓	—	✓	✓	HW-RTOS GMAC MACDMA reception completion
23	HWRTOS_ETHRFE_Int	—	✓	—	✓	✓	HW-RTOS GMAC MACDMA error frame reception completion
24	HWRTOS_ETHRFIV_Int	—	✓	—	✓	✓	HW-RTOS GMAC RX FIFO overflow
25	HWRTOS_ETHIT_Int	—	✓	—	✓	✓	HW-RTOS GMAC transmission completion interrupt
26	HWRTOS_ETHDTIE_Int	—	✓	—	✓	✓	HW-RTOS GMAC MACDMA transmission error
27	HWRTOS_ETHDMAIT_Int	—	✓	—	✓	✓	HW-RTOS GMAC MACDMA transmission completion
28	HWRTOS_ETHTFIU_Int	—	✓	—	✓	✓	HW-RTOS GMAC TX FIFO underflow
29	HWRTOS_ETHTFIE_Int	—	✓	—	✓	✓	HW-RTOS GMAC TX FIFO error interrupt
30	HWRTOS_Int	—	✓	—	✓	✓	HW-RTOS interrupt
31	HWRTOS_ETHRFI_Int	—	✓	—	✓	✓	HW-RTOS GMAC MACDMA valid frame reception completion
32	Reserved	—	—	—	—	—	Reserved
33	Reserved	—	—	—	—	—	Reserved
34	GMAC1_SBD_Int	✓	✓	✓	✓	✓	GMAC1 general
35	GMAC1_LPI_Int	✓	✓	✓	✓	✓	GMAC1 energy efficient
36	GMAC1_PMT_Int	✓	✓	✓	✓	✓	GMAC1 power management
37	GMAC2_SBD_Int	✓	✓	✓	✓	✓	GMAC2 general
38	GMAC2_LPI_Int	✓	✓	✓	✓	✓	GMAC2 energy efficient
39	GMAC2_PMT_Int	✓	✓	✓	✓	✓	GMAC2 power management

Table 9.1 Interrupts Allocation and Vector Number (2/4)

IRQ [Index]	IRQ	N1D		N1S		N1L	Description
		CA7	CM3	CA7	CM3	CM3	
40	A5PSW_DLR_Int	✓	✓	✓	✓	✓	A5PSW – DLR interrupt
41	Reserved	—	—	—	—	—	Reserved
42	A5PSW_Int	✓	✓	✓	✓	✓	A5PSW
43	A5PSW_PRP_Int	✓	✓	✓	✓	—	A5PSW – PRP interrupt
44	A5PSW_HUB_Int	✓	✓	✓	✓	✓	A5PSW – integrated Hub module
45	A5PSW_PTRN_Int	✓	✓	✓	✓	✓	A5PSW – RX Pattern Matcher
46	ETHCAT_RST_Int	✓	✓	✓	✓	✓	ETHERCAT Reset interrupt
47	ETHCAT_SYNC_Int[0]	✓	✓	✓	✓	✓	ETHERCAT Sync0 interrupt
48	ETHCAT_SYNC_Int[1]	✓	✓	✓	✓	✓	ETHERCAT Sync1 interrupt
49	ETHCAT_WDT_Int SERCOS3_DIVCLK_Int	✓	✓	✓	✓	✓	OR'ed between ETHERCAT, SERCOSIII IRQs (Only 1 module is used exclusively) ETHERCAT: WDT interrupt SERCOSIII: Divided communication clock out
50	ETHCAT_EOF_Int SERCOS3_CONCLK_Int HSR_PTP_I_IRQ	✓	✓	✓	✓	✓	OR'ed between ETHERCAT, SERCOSIII and HSR IRQs (Only 1 module is used exclusively) ETHERCAT: EOF interrupt SERCOSIII: Communication synchronized control clock output HSR: PTP interface interrupt
51	ETHCAT_SOF_Int SERCOS3_Int[0] HSR_CPU_I_IRQ	✓	✓	✓	✓	✓	OR'ed between ETHERCAT, SERCOSIII and HSR IRQs (Only 1 module is used exclusively) ETHERCAT: SOF interrupt SERCOSIII: Port1 interrupt HSR: CPU interface interrupt
52	ETHCAT_Int SERCOS3_Int[1]	✓	✓	✓	✓	✓	Multiplexing between ETHERCAT, SERCOSIII IRQs (depending on active module) ETHERCAT interrupt SERCOSIII: Port2 interrupt
53	Reserved	—	—	—	—	—	Reserved
54	Reserved	—	—	—	—	—	Reserved
55	Reserved	—	—	—	—	—	Reserved
56	DMA1_Int	✓	✓	✓	✓	✓	DMAC1 interrupt
57	DMA2_Int	✓	✓	✓	✓	✓	DMAC2 interrupt
58	NAND_Int	✓	✓	✓	✓	✓	NAND Flash Controller interrupt
59	IPCM_Int[0]	✓	✓	✓	✓	—	Mailbox interrupt0
60	IPCM_Int[1]	✓	✓	✓	✓	—	Mailbox interrupt1
61	IPCM_Int[2]	✓	✓	✓	✓	—	Mailbox interrupt2
62	Reserved	—	—	—	—	—	Reserved
63	MSEBIS_Int	✓	✓	✓	✓	✓	MSEBI Slave bus interrupt
64	QSPI1_Int	✓	✓	✓	✓	✓	QuadSPI1 interrupt
65	QSPI2_Int	—	—	✓	✓	—	QuadSPI2 interrupt
66	RTCATINTAL_Int	✓	—	✓	—	—	RTC (Alarm interrupt)
67	RTCATINTR_Int	✓	—	✓	—	—	RTC (Fixed period interrupt)
68	RTCATINT1S_Int	✓	—	✓	—	—	RTC (1 second interrupt)
69	SDIF1_Int	✓	✓	✓	✓	✓	SDIO/SD/eMMC 1 interrupt
70	SDIF1_wkup_Int	✓	✓	✓	✓	✓	SDIO/SD/eMMC 1 wakeup
71	SDIF2_Int	✓	✓	✓	✓	✓	SDIO/SD/eMMC 2 interrupt

Table 9.1 Interrupts Allocation and Vector Number (3/4)

IRQ [Index]	IRQ	N1D		N1S		N1L	Description
		CA7	CM3	CA7	CM3	CM3	
72	SDIF2_wkup_Int	✓	✓	✓	✓	✓	SDIO/SD/eMMC 2 wakeup
73	WDT_CA7_p0_reset_Int	✓	✓	✓	✓	—	Watchdog timer for CA7 processor0
74	WDT_CA7_p1_reset_Int	✓	✓	—	—	—	Watchdog timer for CA7 processor1
75	WDT_CM3_reset_Int	✓	✓	✓	✓	✓	Watchdog timer for CM3
76	DDRC_Int	✓	✓	—	—	—	DDR Controller
77	USB2F_EPC_Int	✓	✓	✓	✓	✓	USB Function
78	USB2F_Int	✓	✓	✓	✓	✓	USB Function
79	USB2H_BIND_Int	✓	✓	✓	✓	✓	USB Host
80	SPI1_Int	✓	✓	✓	✓	✓	SPI1 Master interrupt
81	SPI2_Int	✓	✓	✓	✓	✓	SPI2 Master interrupt
82	SPI3_Int	✓	✓	✓	✓	✓	SPI3 Master interrupt
83	SPI4_Int	✓	✓	✓	✓	✓	SPI4 Master interrupt
84	SPI5_Int	✓	✓	✓	✓	✓	SPI5 Slave interrupt
85	SPI6_Int	✓	✓	✓	✓	✓	SPI6 Slave interrupt
86	UART4_Int	✓	✓	✓	✓	✓	UART4 interrupt
87	UART5_Int	✓	✓	✓	✓	✓	UART5 interrupt
88	UART6_Int	✓	✓	✓	✓	✓	UART6 interrupt
89	UART7_Int	✓	✓	✓	✓	✓	UART7 interrupt
90	UART8_Int	✓	✓	✓	✓	✓	UART8 interrupt
91	Reserved	—	—	—	—	—	Reserved
92	Reserved	—	—	—	—	—	Reserved
93	Reserved	—	—	—	—	—	Reserved
94	Reserved	—	—	—	—	—	Reserved
95	CAN1_Int	✓	✓	✓	✓	✓	CAN1
96	CAN2_Int	✓	✓	✓	✓	✓	CAN2
97	LCDC_Int	✓	✓	✓	✓	—	LCD Controller interrupt
98	Reserved	—	—	—	—	—	Reserved
99	Reserved	—	—	—	—	—	Reserved
100	Reserved	—	—	—	—	—	Reserved
101	Reserved	—	—	—	—	—	Reserved
102	Reserved	—	—	—	—	—	Reserved
103	GPIO_Int[0]	✓	✓	✓	✓	✓	Multiplexed from 32*3 interrupt sources (BGPIO1,2,3)*1
104	GPIO_Int[1]	✓	✓	✓	✓	✓	Multiplexed from 32*3 interrupt sources (BGPIO1,2,3)*1
105	GPIO_Int[2]	✓	✓	✓	✓	✓	Multiplexed from 32*3 interrupt sources (BGPIO1,2,3)*1
106	GPIO_Int[3]	✓	✓	✓	✓	✓	Multiplexed from 32*3 interrupt sources (BGPIO1,2,3)*1
107	GPIO_Int[4]	✓	✓	✓	✓	✓	Multiplexed from 32*3 interrupt sources (BGPIO1,2,3)*1
108	GPIO_Int[5]	✓	✓	✓	✓	✓	Multiplexed from 32*3 interrupt sources (BGPIO1,2,3)*1
109	GPIO_Int[6]	✓	✓	✓	✓	✓	Multiplexed from 32*3 interrupt sources (BGPIO1,2,3)*1
110	GPIO_Int[7]	✓	✓	✓	✓	✓	Multiplexed from 32*3 interrupt sources (BGPIO1,2,3)*1
111	Reserved	—	—	—	—	—	Reserved
112	TIMER1_Int[0]	✓	✓	✓	✓	✓	TIMER1, Sub Timer0 interrupt
113	TIMER1_Int[1]	✓	✓	✓	✓	✓	TIMER1, Sub Timer1 interrupt
114	TIMER1_Int[2]	✓	✓	✓	✓	✓	TIMER1, Sub Timer2 interrupt
115	TIMER1_Int[3]	✓	✓	✓	✓	✓	TIMER1, Sub Timer3 interrupt

Table 9.1 Interrupts Allocation and Vector Number (4/4)

IRQ [Index]	IRQ	N1D		N1S		N1L	Description
		CA7	CM3	CA7	CM3	CM3	
116	TIMER1_Int[4]	✓	✓	✓	✓	✓	TIMER1, Sub Timer4 interrupt
117	TIMER1_Int[5]	✓	✓	✓	✓	✓	TIMER1, Sub Timer5 interrupt
118	TIMER1_Int[6]	✓	✓	✓	✓	✓	TIMER1, Sub Timer6 interrupt
119	TIMER1_Int[7]	✓	✓	✓	✓	✓	TIMER1, Sub Timer7 interrupt
120	TIMER2_Int[0]	✓	✓	✓	✓	✓	TIMER2, Sub Timer0 interrupt
121	TIMER2_Int[1]	✓	✓	✓	✓	✓	TIMER2, Sub Timer1 interrupt
122	TIMER2_Int[2]	✓	✓	✓	✓	✓	TIMER2, Sub Timer2 interrupt
123	TIMER2_Int[3]	✓	✓	✓	✓	✓	TIMER2, Sub Timer3 interrupt
124	TIMER2_Int[4]	✓	✓	✓	✓	✓	TIMER2, Sub Timer4 interrupt
125	TIMER2_Int[5]	✓	✓	✓	✓	✓	TIMER2, Sub Timer5 interrupt
126	TIMER2_Int[6]	✓	✓	✓	✓	✓	TIMER2, Sub Timer6 interrupt
127	TIMER2_Int[7]	✓	✓	✓	✓	✓	TIMER2, Sub Timer7 interrupt
128 … 154	Reserved	—	—	—	—	—	Reserved
155	AXIERR_IRQ	✓	—	✓	—	—	External memory errors on cacheable writes Interrupt
156-239	Reserved	n/a	—	n/a	—	—	Reserved

Note 1. Select from the interrupt source of BGPIO [m] _Int [31: 0] (m = 1, 2, 3) by rGPIOs_Level 2 _Gpio_Int_ [n] (n = 0..7)

Section 10 IOs

10.1 Pinout Description

Table 10.1 PKG Power Supply Pin Name

Classification	PKG Pin Name	Power	Description
Power supply	VDD11	(V_{DD11})	Power supply pin for Internal logic
	VDD11_CA7		
	GND	—	Ground pin
	VDD33	(V_{DD33})	Power supply pin for I/O pin other than GPIO59 to GPIO0
	RGMII1_VDDQ	(V_{RGMII})	Power supply pin for GPIO11 to GPIO0
	RGMII2_VDDQ		Power supply pin for GPIO23 to GPIO12
	RGMII3_VDDQ		Power supply pin for GPIO35 to GPIO24
	RGMII4_VDDQ		Power supply pin for GPIO47 to GPIO36
	RGMII5_VDDQ		Power supply pin for GPIO59 to GPIO48
PLL Power supply	PLL_AVDD	(V_{PLL})	Power supply pin for PLL
	PLL_AGND	—	Ground pin for PLL
USB Power supply	USB_VD33	(V_{USB})	Power supply pin for USB PHY
	USB_GND	—	Ground pin for USB PHY
	USB_AVDD	(V_{USB})	Analog power supply pin for USB PHY
	USB_AVSS	—	Analog ground pin for USB PHY
RTC Power supply	RTC_VDD33	(V_{RTC})	Power supply pin for RTC
ADC Power supply	ADC1_AVDD	(V_{ADC})	Power supply pin for ADC1
	ADC1_AGND	—	Ground pin for ADC1
	ADC2_AVDD	(V_{ADC})	Power supply pin for ADC2
	ADC2_AGND	—	Ground pin for ADC2
OTP Power supply	ANF_VDD_PRG	(V_{ANFPRG})	OTP memory programming voltage input pin
DDR PHY Power supply	DVDD	(V_{DVDD})	Power supply pin for DDR PHY Core and PLL
	DVDDQ	(V_{DVDDQ})	Power supply pin for DDR PHY I/O
	DVSS	—	Ground pin for DDR PHY

Table 10.2 PKG Pin Name (1/2)

Classification	PKG Pin Name	IO	Active	Power	Description
Clock	MCLK_XO	I/O	—	VDD33	Connected to a crystal resonator. And external clock signal may also be input to the MCLK_XO pin.
	MCLK_XI	Input	—		
	RTC_XO	Output	—		Connected to a crystal resonator
	RTC_XI	Input	—		
Operating mode control	CONFIG[1:0]	Input	—		Debugging interface mode control pins 2'b00: Arm-JTAG/SWD (CoreSight) 2'b10: Boundary Scan (JTAG-TAP Controller) Others: Reserved These pins have internal pull-down resistor (R_{PUUD}).
	CONFIG2	Input	—		Reserved configuration pin. Should be 1.
	TMC[2:1]	Input	—		Production test pins. Should be 2'b00.
	CTRSTBYB	Input	High		IO Buffer enable pin, Schmitt input 0: IO Buffer Disable (Output: Hi-Z) 1: IO Buffer Enable Please refer to "Power-up/down Sequence" This pin has internal pull-up resistor (R_{PUUD}).
System control	MRESET_N	Input	Low		Master reset signal input pin, Schmitt input
	MRESET_OUT	Output	High		Master reset signal output pin. Output 1 during MRESET_N=0 or System Reset.
	THMODE	Input	—		Main clock input mode select pin. This pin has internal pull-down resistor (R_{PUUD}).
Debugging interface	JTAG_TRST_N	Input	Low		CoreSight or boundary scan pins. These pins have internal pull-up/down resistor (R_{PUUD}): JTAG_TRST_N, JTAG_TMS, JTAG_TDI, and JTAG_TDO: pull-up JTAG_TCK: pull-down
	JTAG_TMS	I/O	—		
	JTAG_TDI	Input	—		
	JTAG_TDO	Output	—		
	JTAG_TCK	Input	—		
DDR2/3 interface	DDR_CLKP	Output	—	DVDDQ	Differential clock output pins CLKP – CK for DDR, CLKN -- /CK for DDR
	DDR_CLKN	Output	—		
	DDR_CLKEN	Output	High		Clock enable signal
	DDR_RESET_N	Output	Low		Reset signal for DDR3-SDRAM
	DDR_ADDR[15:0]	Output	—		Address bus
	DDR_BA[2:0]	Output	—		Bank address
	DDR_DQ[15:0]	I/O	—		Data bus
	DDR_DM1 DDR_DM0	Output	High		Data mask signal
	DDR_DQS1 DDR_DQS0	I/O	—		Differential bidirectional data strobe DQS[n] -- DQS for DDR DQS_N[n] -- /DQS for DDR
	DDR_DQS_N1 DDR_DQS_N0	I/O	—		
	DDR_WE	Output	Low		/WE for DDR
	DDR_RAS	Output	Low		/RAS for DDR
	DDR_CAS	Output	Low		/CAS for DDR
	DDR_CS1 DDR_CS0	Output	Low		Chip Select
	DDR_ODT1 DDR_ODT0	Output	High		ODT Control

Table 10.2 PKG Pin Name (2/2)

Classification	PKG Pin Name	IO	Active	Power	Description
DDR2/3 interface	DDR_MZQ	I/O	—	—	External Reference resistance connection pin for the output impedance control DDR2: should be connected to GND via 150Ω ±1% DDR3: should be connected to GND via 120Ω ±1%
	DDR_VREF	Input	—	($V_{DDR\ REF}$)	Reference voltage input pin
USB interface	USB_RREF	Input	—	—	Reference current generation pin RZ/N1D: should be connected to GND via 1.6kΩ ±1% RZ/N1S, N1L: should be connected to GND via 2.2kΩ ±1%
	USB_VBUS	Input	—	USB_VD33	Port power detection pin for USB Function, Schmitt input
	USB_DP1	I/O	—		USB High Speed D ±signal (Port1)
	USB_DM1	I/O	—		
	USB_DP2	I/O	—		USB High Speed D ±signal (Port2)
	USB_DM2	I/O	—		
AD Converter	ADC1_VREFP	Input	—	($V_{ADC\ REFP}$)	Reference voltage input pins
	ADC1_VREFN	Input	—	($V_{ADC\ REFM}$)	
	ADC1_IN[n]	Input	—	ADC1_AVDD	Analog input pins for ADC1 n = 0..4, 6..8
	ADC2_VREFP	Input	—	($V_{ADC\ REFP}$)	Reference voltage input pins
	ADC2_VREFN	Input	—	($V_{ADC\ REFM}$)	
	ADC2_IN[n]	Input	—	ADC2_AVDD	Analog input pins for ADC2 n = 0..4, 6..8
Real Time Clock (RTC)	RTC_PWRGOOD	Input	—	RTC_VDD33	RTC backup mode control pin 0: Backup 1: Normal
GPIO	GPIO[n]	I/O	—	RGMII1_VDDQ	n = 0..11
				RGMII2_VDDQ	n = 12..23
				RGMII3_VDDQ	n = 24..35
				RGMII4_VDDQ	n = 36..47
				RGMII5_VDDQ	n = 48..59
				VDD33	n = 60..169 (max) GPIO75..79, 83 are also used in External Pin Configuration. Detail of this function is described in **Section 7.3.2, External Pin Configuration**.

Table 10.3 GPIO Multiplexed Pin Name (1/3)

Classification	IOMuxed Signal Name	IO	Active Level	Description
Ethernet RGMII/RMII/MII	GMII[m]_TXCLK	I/O	—	TX clock m = 1..5
	GMII[m]_TXD[3:0]	Output	—	TX data m = 1..5
	GMII[m]_TXEN	Output	High	TX data enable m = 1..5
	GMII[m]_TXER	Output	High	TX data error m = 1..5
	GMII[m]_RXCLK	Input	—	RX clock m = 1..5
	GMII[m]_RXD[3:0]	Output	—	RX data m = 1..5
	GMII[m]_RXDV	Input	High	RX data enable m = 1..5
	GMII[m]_RXER	Input	High	RX data error m = 1..5
	GMII[m]_CRS	Input	High	Carrier detection m = 1..5
	GMII[m]_COL	Input	High	Collision detection m = 1..5
	RGMII_REFCLK	Input	—	125 MHz input for RGMII
	RMII_REFCLK	Output	—	50 MHz output for RMII
	MII_REFCLK_[5:0]	Output	—	25 MHz output for MII
NAND Flash	FNAND_CE_N[3:0]	Output	Low	Chip Enable
	FNAND_IO[7:0]	I/O	—	Data
	FNAND_CLE	Output	High	Command Latch Enable
	FNAND_ALE	Output	High	Address Latch Enable
	FNAND_RE_N	Output	Low	Read Enable
	FNAND_WE_N	Output	Low	Write Enable
	FNAND_WP_N[3:0]	Output	Low	Write Protect/Reset
	FNAND_RY/BY_N[3:0]	Input	—	Ready/Busy
QSPI	QUAD[m]_CLK	Output	—	Clock m = 1..2
	QUAD[m]_IO[3:0]	I/O	—	Data m = 1..2
	QUAD[m]_CS_N[3:0]	Output	Low	Slave selection m = 1..2
SD/MMC/SDIO	SDIO[m]_CLK	Output	—	Clock m = 1..2
	SDIO[m]_CMD	I/O	—	Command/response m = 1..2
	SDIO[m]_IO[7:0]	I/O	—	Data m = 1..2
	SDIO[m]_CD_N	Input	Low	Card Detection m = 1..2
	SDIO[m]_WP	Input	High	SD Card Write Protect m = 1..2
	SDIO[m]_LEDCTRL	Output	High	LED control m = 1..2
LCD	LCD_PCLK	Output	—	Pixel Clock
	LCD_HSYNC	Output	Selectable	Horizontal Sync Pulse
	LCD_VSYNC	Output	Selectable	Vertical Sync Pulse
	LCD_DE	Output	Selectable	Data Enable
	LCD_PE	Output	High	Power Enable
	LCD_PWM[n]	Output	—	LCD LED Pulse Width Modulation n = 0..1
	LCD_R[7:0]	Output	—	Red Data
	LCD_G[7:0]	Output	—	Green Data
	LCD_B[7:0]	Output	—	Blue Data

Table 10.3 GPIO Multiplexed Pin Name (2/3)

Classification	IOMuxed Signal Name	IO	Active Level	Description
MSEBI Master	MSEBIM_ACD[31:0]	I/O	—	Address, Control and Data multiplexed
	MSEBIM_ALE	Output	High	Address Latch Enable
	MSEBIM_ALE1	Output	High	Address Latch Enable for parallel mode
	MSEBIM_ALE2	Output	High	Address Latch Enable for parallel mode
	MSEBIM_ALE3	Output	High	Address Latch Enable for parallel mode
	MSEBIM_CLE	Output	High	Address and Control Latch Enable
	MSEBIM_DLE	Output	High	Data Latch Enable
	MSEBIM_WR_N	Output	Low	Write enable
	MSEBIM_RD_N	Output	Low	Read enable
	MSEBIM_CLK	Output	—	Clock
	MSEBIM_WAIT_N[3:0]	Input	Low	Wait Request input
	MSEBIM_DMA_RD_N[1:0]	Input	Low	DMA Read Request
	MSEBIM_DMA_WR_N[1:0]	Input	Low	DMA Write Request
MSEBI Slave	MSEBIS_ACD[31:0]	I/O	—	Address, Control and Data multiplexed
	MSEBIS_ALE	Input	High	Address Latch Enable
	MSEBIS_CLE	Input	High	Address and Control Latch Enable
	MSEBIS_DLE	Input	High	Data Latch Enable
	MSEBIS_CLK	Input	—	Clock
	MSEBIS_WAIT_N[3:0]	Output	Low	Wait Request output
	MSEBIS_DMA_RD_N[1:0]	Output	Low	DMA Read Request
	MSEBIS_DMA_WR_N[1:0]	Output	Low	DMA Write Request
Cortex-M3	NMI_CORTEXM3	Input	High	Non-maskable Interrupt for Cortex-M3
ETHERCAT	CAT_LEDRUN	Output	High	RUN LED
	CAT_LEDSTER	Output	High	Dual-color State LED
	CAT_LEDERR	Output	High	Error LED
	CAT_LINKACT[n]	Output	High	link / Activity LED n = 0..2
	CAT_SYNC[n]	Output	High	SYNC n = 0..1
	CAT_LATCH[n]	Input	Both edge	LATCH n = 0..1
	CAT_MII_LINK[n]	Input	Selectable	Link status from PHY n = 0..2
	CAT_RESETOUT_N	Output	Low	RESET OUT
	CAT_I2CCLK	Output	—	EEPROM I2C clock
	CAT_I2CDATA	I/O	—	EEPROM I2C data
SERCOSIII	S3_LED_GN	Output	High	LED (green)
	S3_LED_RD	Output	High	LED (red)
	S3_ACTLEDP[m]	Output	High	activity LED m = 1..2
	S3_LINKLEDP[m]	Output	High	link LED m = 1..2
	S3_CONCLK	Output	—	Communication synchronized control clock output
	S3_DIVCLK	Output	—	Divided communication clock out
	S3_MII_LINKP[m]	Input	Selectable	Link status from PHY m = 1..2
	S3_PHY_RESET_N	Output	Low	PHY RESET
	S3_TESTPIN[m]	Output	—	test signal output by DBGOCR m = 1..2
GMAC/A5PSW	MAC_PPS[n]	Output	High	GMAC1 Pulse Per Second output n = 0..1
	MAC_TRIG[m]	Input	Rise Edge	GMAC[m] Auxiliary Timestamp Trigger Input m = 1..2
	SWITCH_MII_LINK[m]	Input	Selectable	A5PSW Link status from PHY m = 2..5

Table 10.3 GPIO Multiplexed Pin Name (3/3)

Classification	IOMuxed Signal Name	IO	Active Level	Description
MDIO	MDC[m]	Output	—	Management data clock m = 1..2
	MDIO[m]	I/O	—	Management data I/O m = 1..2
USB	USB_OC[m]	Input	Low	Overcurrent status for USB Host m = 1..2
	USB_PPON[m]	Output	High	Port Power control for USB Host m = 1..2
UART	UART[m]_RXD	Input	—	Receive data m = 1..8
	UART[m]_TXD	Output	—	Transmit data m = 1..8
	UART[m]_CTS_N	Input	Low	Clear To Send Modem Status m = 1..8
	UART[m]_DSR_N	Input	Low	Data Set Ready Modem Status m = 1..8
	UART[m]_DCD_N	Input	Low	Data Carrier Detect Modem Status m = 1..8
	UART[m]_RI_N	Input	Low	Ring Indicator Modem Status m = 1..8
	UART[m]_DTR_N	Output	Low	Modem Control Data Terminal Ready m = 1..8
	UART[m]_RTS_N	Output	Low	Modem Control Request To Send m = 1..8
SPI Master	SPI[m]_CLK	Output	—	Clock m = 1..4
	SPI[m]_MOSI	Output	—	Master transmit data m = 1..4
	SPI[m]_MISO	Input	—	Slave transmit data m = 1..4
	SPI[m]_SS_N[n]	Output	Low	Slave selection m = 1..4, n = 0..3
SPI Slave	SPI[m]_CLK	Input	—	Clock m = 5..6
	SPI[m]_MOSI	Input	—	Master transmit data m = 5..6
	SPI[m]_MISO	Output	—	Slave transmit data m = 5..6
	SPI[m]_SS_N	Input	Low	Slave selection m = 5..6
BGPIO	BGPIO[m]A[n]	I/O	—	Basic GPIO[m] port A m = 1..3, n = 0..31
	BGPIO[m]B[n]	I/O	—	Basic GPIO[m] port B m = 1..3, n = 0..31
CAN	CAN[m]_RXD	Input	—	Receive data m = 1..2
	CAN[m]_TXD	Output	—	Transmit data m = 1..2
I2C	I2C[m]_SCL	I/O	—	Serial clock m = 1..2
	I2C[m]_SDA	I/O	—	Serial data m = 1..2
PWMTimer	PWM_IN[n]	Input	—	Input pins n = 0..39
	PWM_OUT[n]	Output	—	Output pins n = 0..19

10.2 Handling of Unused Pins

Table 10.4 Handling of Unused Pins

Pin Name	Handling
USB_VD33	Connect this pin to VDD33
USB_GND	GND
USB_AVDD	Connect this pin to VDD33
USB_AVSS	GND
RTC_VDD33	Connect this pin to VDD33
ADC1_AVDD	Connect this pin to VDD33
ADC1_AGND	GND
ADC2_AVDD	Connect this pin to VDD33
ADC2_AGND	GND
MCLK_XI	GND
RTC_XO	Open
RTC_XI	GND
MRESET_OUT	Open
JTAG_TRST_N	Open or 4.7kΩ pull-down
JTAG_TMS	Open or 4.7kΩ pull-up
JTAG_TDI	Open or 4.7kΩ pull-up
JTAG_TDO	Open
JTAG_TCK	Open or 4.7kΩ pull-up or pull-down
USB_RREF	Same as used case. Refer to NOTES 2.
USB_VBUS	10kΩ pull-down
USB_DP1	10kΩ pull-down
USB_DM1	
USB_DP2	10kΩ pull-down
USB_DM2	
ADC1_VREFP	Open
ADC1_VREFN	
ADC1_IN[n]	Open
ADC2_VREFP	Open
ADC2_VREFN	
ADC2_IN[n]	Open
RTC_PWRGOOD	Connect this pin to VDD33
ANF_VDD_PRG	GND
GPIO[n] n = 0..169 (max)	[Mode Config] Level1 function: floating (default) and pull-up (default) / down

NOTES

1. ADC should be set to power down mode when ADC is not used.
2. USB_RREF needs reference resister as normal use case, it is necessary for USBPLL operation.

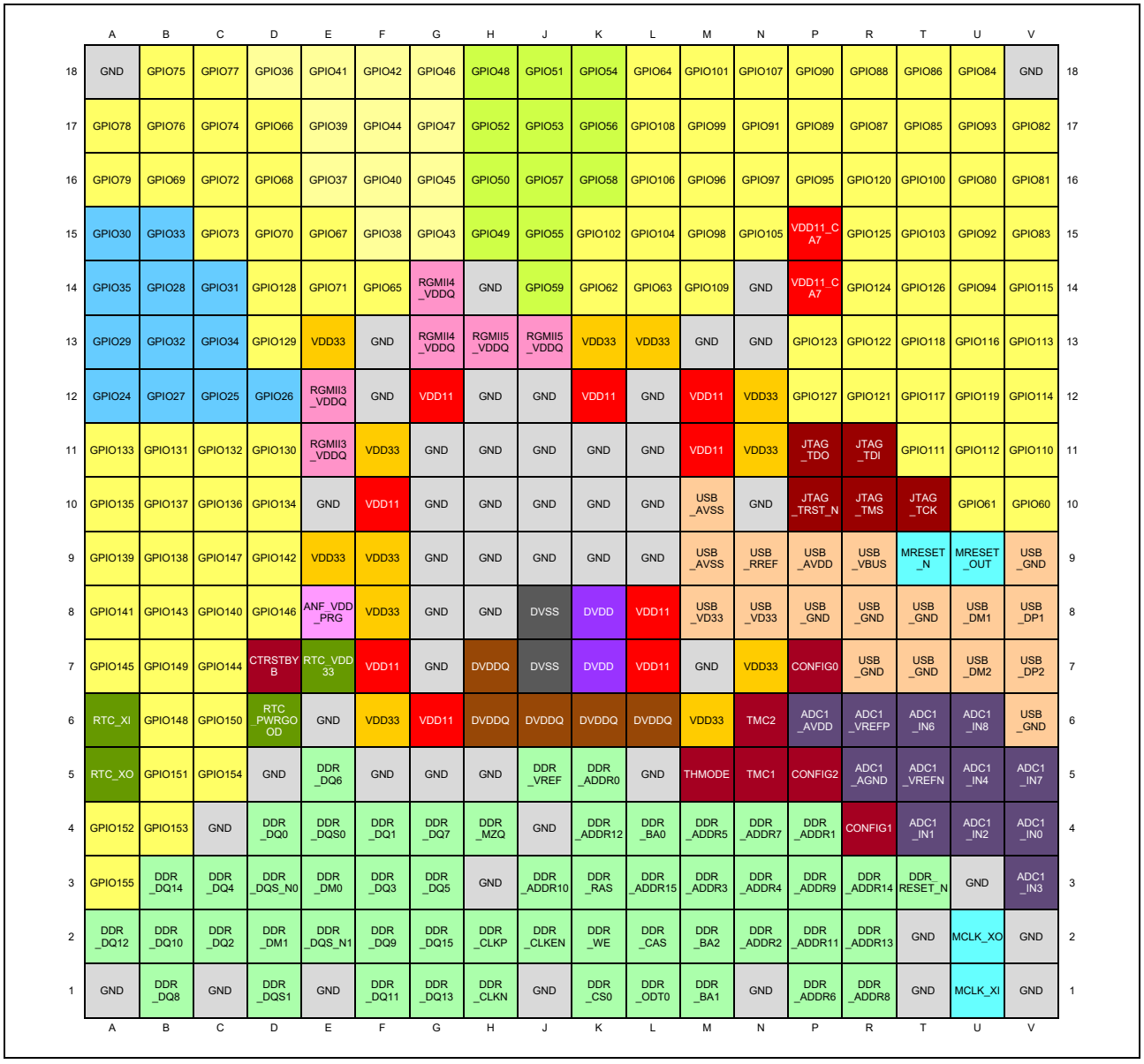
10.3 Pinout

10.3.1 RZ/N1D BGA-400 Package

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
20	GND	GPIO75	GPIO77	GPIO36	GPIO37	GPIO42	GPIO48	GPIO53	GPIO54	GPIO59	GPIO12	GPIO18	GPIO20	GPIO62	GPIO63	GPIO90	GPIO88	GPIO86	GPIO84	GND	20
19	GPIO78	GPIO76	GPIO74	GPIO68	GPIO38	GPIO41	GPIO45	GPIO51	GPIO56	GPIO58	GPIO13	GPIO17	GPIO64	GPIO106	GPIO91	GPIO89	GPIO87	GPIO85	GPIO93	GPIO82	19
18	GPIO30	GPIO79	GPIO73	GPIO71	GPIO66	GPIO39	GPIO44	GPIO47	GPIO52	GPIO55	GPIO19	GPIO15	GPIO22	GPIO102	GPIO107	GPIO96	GPIO95	GPIO100	GPIO80	GPIO81	18
17	GPIO27	GPIO32	GPIO34	GPIO69	GPIO70	GPIO67	GPIO40	GPIO46	GPIO49	GPIO57	GPIO16	GPIO21	GPIO104	GPIO99	GPIO98	GPIO97	GPIO105	GPIO103	GPIO92	GPIO83	17
16	GPIO24	GPIO28	GPIO29	GPIO129	GPIO128	GPIO72	GPIO65	GPIO43	GPIO50	GND	GPIO14	GPIO23	GPIO108	GPIO101	VDD11_CA7	GPIO120	GPIO109	GPIO118	GPIO94	GPIO117	16
15	GPIO6	GPIO8	GPIO31	GPIO33	GPIO35	GND	GND	GND	RGMII5_VDDQ	RGMII5_VDDQ	GND	GND	VDD33	GND	VDD11_CA7	GPIO125	GPIO126	GPIO121	GPIO116	GPIO119	15
14	GPIO5	GPIO9	GPIO10	GPIO26	RGMII3_VDDQ	RGMII3_VDDQ	VDD33	RGMII4_VDDQ	RGMII4_VDDQ	GND	RGMII2_VDDQ	RGMII2_VDDQ	VDD33	GND	GPIO124	GPIO123	GPIO122	GPIO111	GPIO115	GPIO113	14
13	GPIO2	GPIO4	GPIO3	GPIO11	GPIO25	GND	VDD11	GND	VDD11	VDD11	GND	VDD11	GND	VDD33	GPIO127	JTAG_TDO	JTAG_TCK	GPIO114	GPIO112	GPIO110	13
12	GPIO0	GPIO131	GPIO1	GPIO7	RGMII1_VDDQ	GND	VDD11	GND	GND	GND	GND	GND	VDD11	VDD33	GND	JTAG_TRST_N	JTAG_TDI	JTAG_TMS	GPIO61	GPIO60	12
11	GPIO137	GPIO135	GPIO133	GPIO132	GPIO130	RGMII1_VDDQ	GND	GND	GND	GND	GND	GND	GND	USB_AVSS	USB_RREF	USB_AVDD	USB_VBUS	MRESET_N	MRESET_OUT	USB_GND	11
10	GPIO139	GPIO136	GPIO138	GPIO140	GPIO134	GND	VDD33	GND	GND	GND	GND	GND	VDD11	USB_AVSS	USB_GND	USB_GND	USB_GND	USB_GND	USB_DM1	USB_DP1	10
9	GPIO141	GPIO143	GPIO147	GPIO144	CTRSTBYB	VDD33	VDD33	VDD11	GND	GND	GND	GND	VDD11	GND	USB_VD33	USB_VD33	USB_GND	USB_GND	USB_DM2	USB_DP2	9
8	GPIO145	GPIO149	GPIO142	GPIO148	ANF_VDD_PRG	RTC_VDD33	GND	VDD11	VDD11	DVSS	DVDD	VDD11	GND	VDD33	ADC2_AGND	ADC2_AVDD	ADC2_IN6	ADC2_IN7	ADC2_IN8	USB_GND	8
7	RTC_XI	GPIO146	RTC_PWRGOOD	GPIO152	GPIO150	GND	VDD33	DVDDQ	GND	DVSS	DVDD	DVDDQ	VDD33	TMC2	THMODE	ADC2_VREFN	ADC2_VREFP	ADC2_IN3	ADC2_IN2	ADC2_IN4	7
6	RTC_XO	GPIO151	GPIO153	GPIO154	GPIO158	GND	VDD33	GND	DVDDQ	DVDDQ	DVDDQ	DVDDQ	GND	CONFIG1	CONFIG0	ADC1_AVDD	ADC1_VREFP	ADC1_IN8	ADC2_IN1	ADC2_IN0	6
5	GPIO155	GPIO157	GPIO159	GPIO163	GPIO162	DDR_DQ6	GND	GND	GND	DDR_VREF	GND	DDR_ADDR0	GND	DDR_ADDR5	CONFIG2	ADC1_AGND	ADC1_VREFN	ADC1_IN4	ADC1_IN6	ADC1_IN7	5
4	GPIO160	GPIO156	GPIO167	GPIO165	GND	DDR_DQ0	DDR_DQS_N0	DDR_DQ7	DDR_DQ5	DDR_MZQ	DDR_CS1	DDR_ADDR12	DDR_ADDR15	DDR_BA0	DDR_ADDR7	DDR_ADDR1	TMC1	ADC1_IN3	ADC1_IN0	ADC1_IN2	4
3	GPIO161	GPIO169	GPIO166	GND	DDR_DQ4	DDR_DQS0	DDR_DM0	DDR_DQ1	DDR_DQ3	GND	DDR_ADDR10	DDR_RAS	DDR_CAS	DDR_ADDR3	DDR_ADDR4	DDR_ADDR9	DDR_ADDR14	DDR_RESET_N	GND	ADC1_IN1	3
2	GPIO164	GPIO168	DDR_DQ14	DDR_DQ8	DDR_DQ2	DDR_DM1	DDR_DQS_N1	DDR_DQ9	DDR_DQ15	DDR_CLKP	DDR_CLKEN	DDR_WE	DDR_ODT0	DDR_BA2	DDR_ADDR2	DDR_ADDR11	DDR_ADDR13	GND	MCLK_XO	GND	2
1	GND	GND	DDR_DQ12	DDR_DQ10	GND	DDR_DQS1	GND	DDR_DQ11	DDR_DQ13	DDR_CLKN	GND	DDR_CS0	DDR_ODT1	DDR_BA1	GND	DDR_ADDR6	DDR_ADDR8	GND	MCLK_XI	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Figure 10.1 RZ/N1D Pinout BGA-400 (Top View)

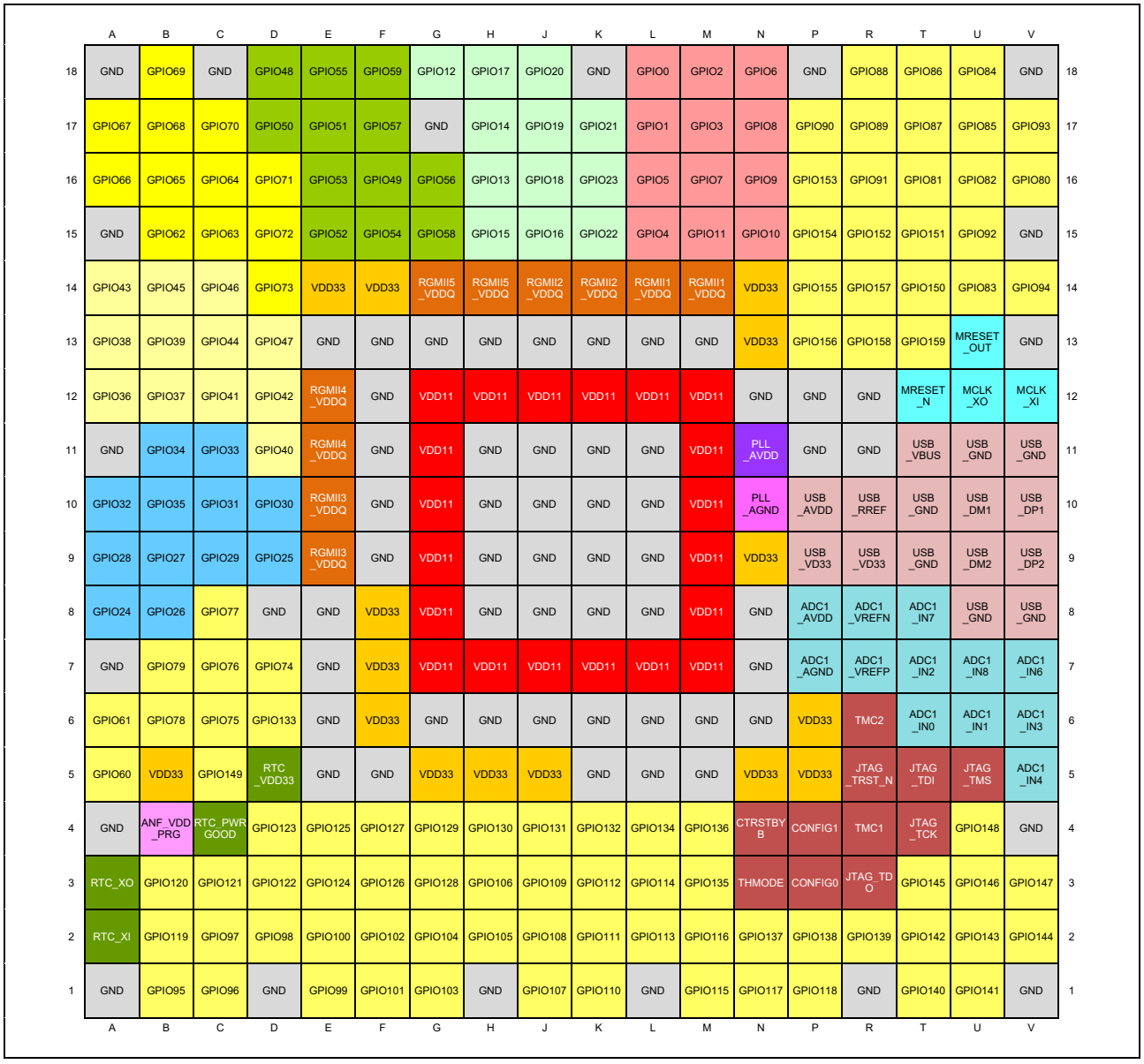
10.3.2 RZ/N1D BGA-324 Package



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	
18	GND	GPIO75	GPIO77	GPIO36	GPIO41	GPIO42	GPIO46	GPIO48	GPIO51	GPIO54	GPIO64	GPIO101	GPIO107	GPIO90	GPIO88	GPIO86	GPIO84	GND	18
17	GPIO78	GPIO76	GPIO74	GPIO66	GPIO39	GPIO44	GPIO47	GPIO52	GPIO53	GPIO56	GPIO108	GPIO99	GPIO91	GPIO89	GPIO87	GPIO85	GPIO93	GPIO82	17
16	GPIO79	GPIO69	GPIO72	GPIO68	GPIO37	GPIO40	GPIO45	GPIO50	GPIO57	GPIO58	GPIO106	GPIO96	GPIO97	GPIO95	GPIO120	GPIO100	GPIO80	GPIO81	16
15	GPIO30	GPIO33	GPIO73	GPIO70	GPIO67	GPIO38	GPIO43	GPIO49	GPIO55	GPIO102	GPIO104	GPIO98	GPIO105	VDD11_CA7	GPIO125	GPIO103	GPIO92	GPIO83	15
14	GPIO35	GPIO28	GPIO31	GPIO128	GPIO71	GPIO65	RGMII4_VDDQ	GND	GPIO59	GPIO62	GPIO63	GPIO109	GND	VDD11_CA7	GPIO124	GPIO126	GPIO94	GPIO115	14
13	GPIO29	GPIO32	GPIO34	GPIO129	VDD33	GND	RGMII4_VDDQ	RGMII5_VDDQ	RGMII5_VDDQ	VDD33	VDD33	GND	GND	GPIO123	GPIO122	GPIO118	GPIO116	GPIO113	13
12	GPIO24	GPIO27	GPIO25	GPIO26	RGMII3_VDDQ	GND	VDD11	GND	GND	VDD11	GND	VDD11	VDD33	GPIO127	GPIO121	GPIO117	GPIO119	GPIO114	12
11	GPIO133	GPIO131	GPIO132	GPIO130	RGMII3_VDDQ	VDD33	GND	GND	GND	GND	GND	VDD11	VDD33	JTAG_TDO	JTAG_TDI	GPIO111	GPIO112	GPIO110	11
10	GPIO135	GPIO137	GPIO136	GPIO134	GND	VDD11	GND	GND	GND	GND	GND	USB_AVSS	GND	JTAG_TRST_N	JTAG_TMS	JTAG_TCK	GPIO61	GPIO60	10
9	GPIO139	GPIO138	GPIO147	GPIO142	VDD33	VDD33	GND	GND	GND	GND	GND	USB_AVSS	USB_RREF	USB_AVDD	USB_VBUS	MRESET_N	MRESET_OUT	USB_GND	9
8	GPIO141	GPIO143	GPIO140	GPIO146	ANF_VDD_PRG	VDD33	GND	GND	DVSS	DVDD	VDD11	USB_VD33	USB_VD33	USB_GND	USB_GND	USB_GND	USB_DM1	USB_DP1	8
7	GPIO145	GPIO149	GPIO144	CTRSTBYB	RTC_VDD33	VDD11	GND	DVDDQ	DVSS	DVDD	VDD11	GND	VDD33	CONFIG0	USB_GND	USB_GND	USB_DM2	USB_DP2	7
6	RTC_XI	GPIO148	GPIO150	RTC_PWRGOOD	GND	VDD33	VDD11	DVDDQ	DVDDQ	DVDDQ	DVDDQ	VDD33	TMC2	ADC1_AVDD	ADC1_VREFP	ADC1_IN6	ADC1_IN8	USB_GND	6
5	RTC_XO	GPIO151	GPIO154	GND	DDR_DQ6	GND	GND	GND	DDR_VREF	DDR_ADDR0	GND	THMODE	TMC1	CONFIG2	ADC1_AGND	ADC1_VREFN	ADC1_IN4	ADC1_IN7	5
4	GPIO152	GPIO153	GND	DDR_DQ0	DDR_DQS0	DDR_DQ1	DDR_DQ7	DDR_MZQ	GND	DDR_ADDR12	DDR_BA0	DDR_ADDR5	DDR_ADDR7	DDR_ADDR1	CONFIG1	ADC1_IN1	ADC1_IN2	ADC1_IN0	4
3	GPIO155	DDR_DQ14	DDR_DQ4	DDR_DQS_N0	DDR_DM0	DDR_DQ3	DDR_DQ5	GND	DDR_ADDR10	DDR_RAS	DDR_ADDR15	DDR_ADDR3	DDR_ADDR4	DDR_ADDR9	DDR_ADDR14	DDR_RESET_N	GND	ADC1_IN3	3
2	DDR_DQ12	DDR_DQ10	DDR_DQ2	DDR_DM1	DDR_DQS_N1	DDR_DQ9	DDR_DQ15	DDR_CLKP	DDR_CLKEN	DDR_WE	DDR_CAS	DDR_BA2	DDR_ADDR2	DDR_ADDR11	DDR_ADDR13	GND	MCLK_XO	GND	2
1	GND	DDR_DQ8	GND	DDR_DQS1	GND	DDR_DQ11	DDR_DQ13	DDR_CLKN	GND	DDR_CS0	DDR_ODT0	DDR_BA1	GND	DDR_ADDR6	DDR_ADDR8	GND	MCLK_XI	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	

Figure 10.2 RZ/N1D Pinout BGA-324 (Top View)

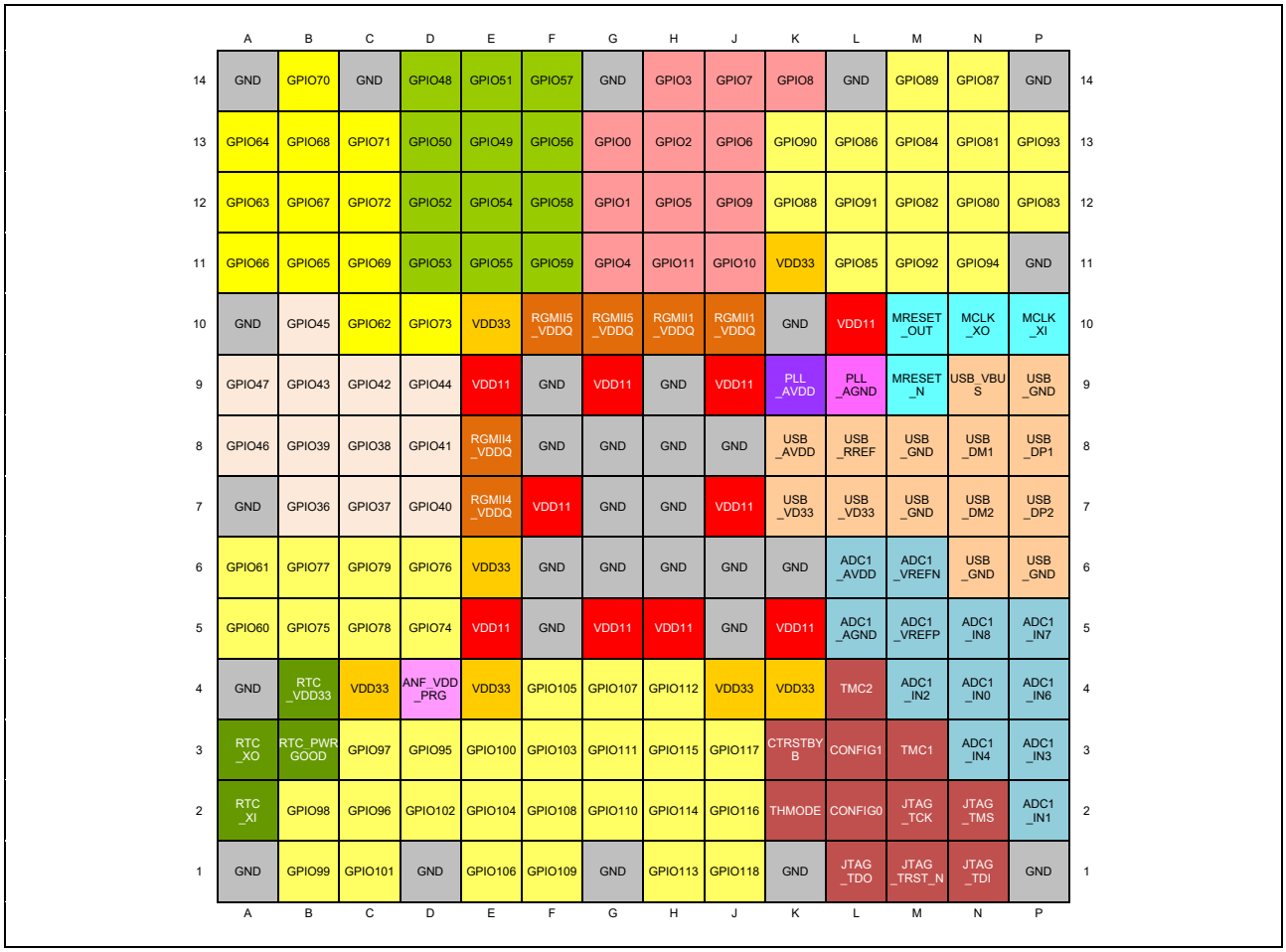
10.3.3 RZ/N1S BGA-324 Package



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	
18	GND	GPIO69	GND	GPIO48	GPIO55	GPIO59	GPIO12	GPIO17	GPIO20	GND	GPIO0	GPIO2	GPIO6	GND	GPIO88	GPIO86	GPIO84	GND	18
17	GPIO67	GPIO68	GPIO70	GPIO50	GPIO51	GPIO57	GND	GPIO14	GPIO19	GPIO21	GPIO1	GPIO3	GPIO8	GPIO90	GPIO89	GPIO87	GPIO85	GPIO93	17
16	GPIO66	GPIO65	GPIO64	GPIO71	GPIO53	GPIO49	GPIO56	GPIO13	GPIO18	GPIO23	GPIO5	GPIO7	GPIO9	GPIO153	GPIO91	GPIO81	GPIO82	GPIO80	16
15	GND	GPIO62	GPIO63	GPIO72	GPIO52	GPIO54	GPIO58	GPIO15	GPIO16	GPIO22	GPIO4	GPIO11	GPIO10	GPIO154	GPIO152	GPIO151	GPIO92	GND	15
14	GPIO43	GPIO45	GPIO46	GPIO73	VDD33	VDD33	RGMII5_VDDQ	RGMII5_VDDQ	RGMII2_VDDQ	RGMII2_VDDQ	RGMII1_VDDQ	RGMII1_VDDQ	VDD33	GPIO155	GPIO157	GPIO150	GPIO83	GPIO94	14
13	GPIO38	GPIO39	GPIO44	GPIO47	GND	GND	GND	GND	GND	GND	GND	GND	VDD33	GPIO156	GPIO158	GPIO159	MRESET_OUT	GND	13
12	GPIO36	GPIO37	GPIO41	GPIO42	RGMII4_VDDQ	GND	VDD11	VDD11	VDD11	VDD11	VDD11	VDD11	GND	GND	GND	MRESET_N	MCLK_XO	MCLK_XI	12
11	GND	GPIO34	GPIO33	GPIO40	RGMII4_VDDQ	GND	VDD11	GND	GND	GND	GND	VDD11	PLL_AVDD	GND	GND	USB_VBUS	USB_GND	USB_GND	11
10	GPIO32	GPIO35	GPIO31	GPIO30	RGMII3_VDDQ	GND	VDD11	GND	GND	GND	GND	VDD11	PLL_AGND	USB_AVDD	USB_RREF	USB_GND	USB_DM1	USB_DP1	10
9	GPIO28	GPIO27	GPIO29	GPIO25	RGMII3_VDDQ	GND	VDD11	GND	GND	GND	GND	VDD11	VDD33	USB_VD33	USB_VD33	USB_GND	USB_DM2	USB_DP2	9
8	GPIO24	GPIO26	GPIO77	GND	GND	VDD33	VDD11	GND	GND	GND	GND	VDD11	GND	ADC1_AVDD	ADC1_VREFN	ADC1_IN7	USB_GND	USB_GND	8
7	GND	GPIO79	GPIO76	GPIO74	GND	VDD33	VDD11	VDD11	VDD11	VDD11	VDD11	VDD11	GND	ADC1_AGND	ADC1_VREFP	ADC1_IN2	ADC1_IN8	ADC1_IN6	7
6	GPIO61	GPIO78	GPIO75	GPIO133	GND	VDD33	GND	GND	GND	GND	GND	GND	GND	VDD33	TMC2	ADC1_IN0	ADC1_IN1	ADC1_IN3	6
5	GPIO60	VDD33	GPIO149	RTC_VDD33	GND	GND	VDD33	VDD33	VDD33	GND	GND	GND	VDD33	VDD33	JTAG_TRST_N	JTAG_TDI	JTAG_TMS	ADC1_IN4	5
4	GND	ANF_VDD_PRG	RTC_PWR GOOD	GPIO123	GPIO125	GPIO127	GPIO129	GPIO130	GPIO131	GPIO132	GPIO134	GPIO136	CTRSTBYB	CONFIG1	TMC1	JTAG_TCK	GPIO148	GND	4
3	RTC_XO	GPIO120	GPIO121	GPIO122	GPIO124	GPIO126	GPIO128	GPIO106	GPIO109	GPIO112	GPIO114	GPIO135	THMODE	CONFIG0	JTAG_TDO	GPIO145	GPIO146	GPIO147	3
2	RTC_XI	GPIO119	GPIO97	GPIO98	GPIO100	GPIO102	GPIO104	GPIO105	GPIO108	GPIO111	GPIO113	GPIO116	GPIO137	GPIO138	GPIO139	GPIO142	GPIO143	GPIO144	2
1	GND	GPIO95	GPIO96	GND	GPIO99	GPIO101	GPIO103	GND	GPIO107	GPIO110	GND	GPIO115	GPIO117	GPIO118	GND	GPIO140	GPIO141	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	

Figure 10.3 RZ/N1S Pinout BGA-324 (Top View)

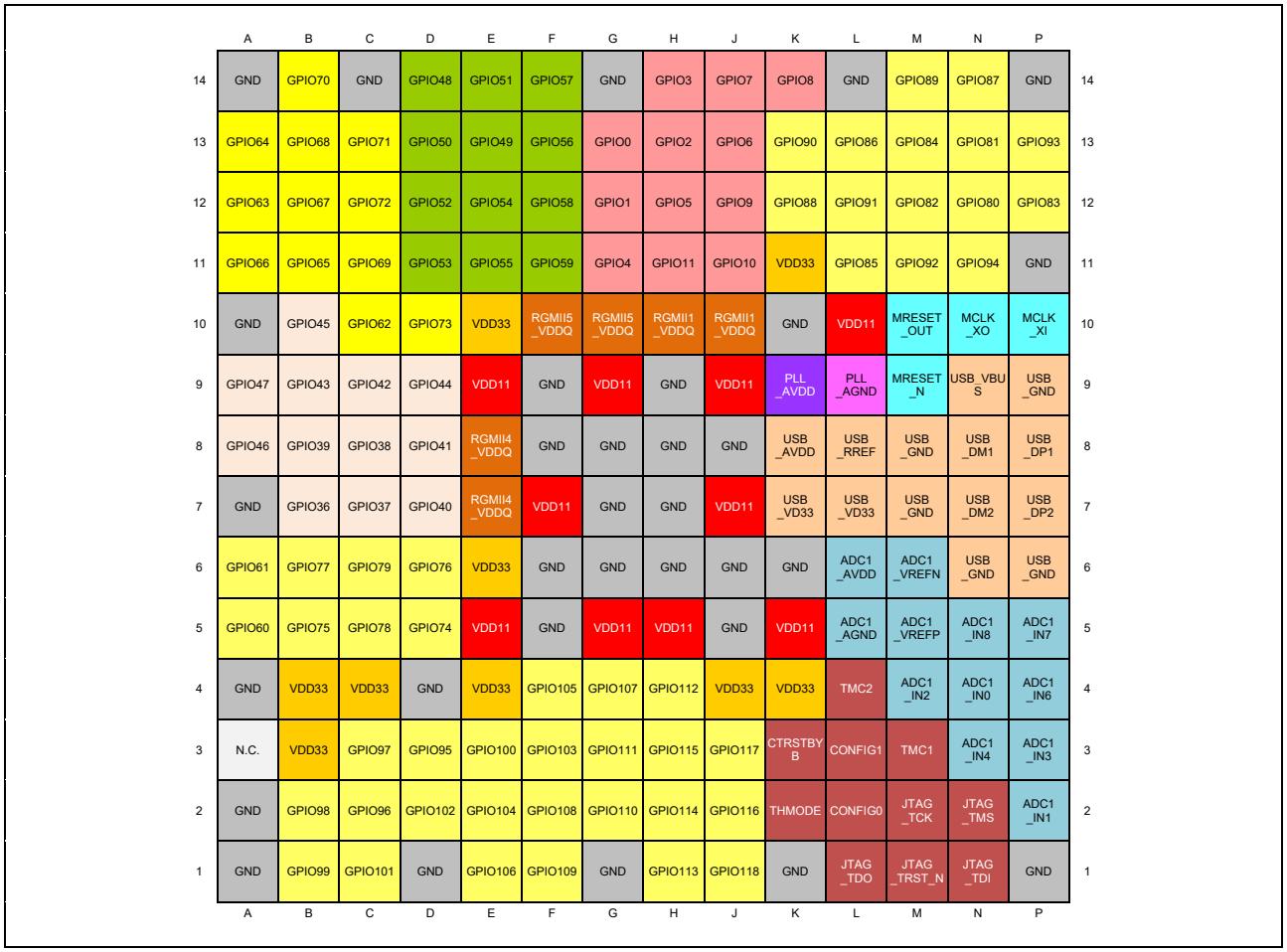
10.3.4 RZ/N1S BGA-196 Package



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	GND	GPIO70	GND	GPIO48	GPIO51	GPIO57	GND	GPIO3	GPIO7	GPIO8	GND	GPIO89	GPIO87	GND	14
13	GPIO64	GPIO68	GPIO71	GPIO50	GPIO49	GPIO56	GPIO0	GPIO2	GPIO6	GPIO90	GPIO86	GPIO84	GPIO81	GPIO93	13
12	GPIO63	GPIO67	GPIO72	GPIO52	GPIO54	GPIO58	GPIO1	GPIO5	GPIO9	GPIO88	GPIO91	GPIO82	GPIO80	GPIO83	12
11	GPIO66	GPIO65	GPIO69	GPIO53	GPIO55	GPIO59	GPIO4	GPIO11	GPIO10	VDD33	GPIO85	GPIO92	GPIO94	GND	11
10	GND	GPIO45	GPIO62	GPIO73	VDD33	RGMII5_VDDQ	RGMII5_VDDQ	RGMII1_VDDQ	RGMII1_VDDQ	GND	VDD11	MRESET_OUT	MCLK_XO	MCLK_XI	10
9	GPIO47	GPIO43	GPIO42	GPIO44	VDD11	GND	VDD11	GND	VDD11	PLL_AVDD	PLL_AGND	MRESET_N	USB_VBUS	USB_GND	9
8	GPIO46	GPIO39	GPIO38	GPIO41	RGMII4_VDDQ	GND	GND	GND	GND	USB_AVDD	USB_RREF	USB_GND	USB_DM1	USB_DP1	8
7	GND	GPIO36	GPIO37	GPIO40	RGMII4_VDDQ	VDD11	GND	GND	VDD11	USB_VD33	USB_VD33	USB_GND	USB_DM2	USB_DP2	7
6	GPIO61	GPIO77	GPIO79	GPIO76	VDD33	GND	GND	GND	GND	GND	ADC1_AVDD	ADC1_VREFN	USB_GND	USB_GND	6
5	GPIO60	GPIO75	GPIO78	GPIO74	VDD11	GND	VDD11	VDD11	GND	VDD11	ADC1_AGND	ADC1_VREFP	ADC1_IN8	ADC1_IN7	5
4	GND	RTC_VDD33	VDD33	ANF_VDD_PRG	VDD33	GPIO105	GPIO107	GPIO112	VDD33	VDD33	TMC2	ADC1_IN2	ADC1_IN0	ADC1_IN6	4
3	RTC_XO	RTC_PWRGOOD	GPIO97	GPIO95	GPIO100	GPIO103	GPIO111	GPIO115	GPIO117	CTRSTBYB	CONFIG1	TMC1	ADC1_IN4	ADC1_IN3	3
2	RTC_XI	GPIO98	GPIO96	GPIO102	GPIO104	GPIO108	GPIO110	GPIO114	GPIO116	THMODE	CONFIG0	JTAG_TCK	JTAG_TMS	ADC1_IN1	2
1	GND	GPIO99	GPIO101	GND	GPIO106	GPIO109	GND	GPIO113	GPIO118	GND	JTAG_TDO	JTAG_TRST_N	JTAG_TDI	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 10.4 RZ/N1S Pinout BGA-196 (Top View)

10.3.5 RZ/N1L BGA-196 Package



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	GND	GPIO70	GND	GPIO48	GPIO51	GPIO57	GND	GPIO3	GPIO7	GPIO8	GND	GPIO89	GPIO87	GND	14
13	GPIO64	GPIO68	GPIO71	GPIO50	GPIO49	GPIO56	GPIO0	GPIO2	GPIO6	GPIO90	GPIO86	GPIO84	GPIO81	GPIO93	13
12	GPIO63	GPIO67	GPIO72	GPIO52	GPIO54	GPIO58	GPIO1	GPIO5	GPIO9	GPIO88	GPIO91	GPIO82	GPIO80	GPIO83	12
11	GPIO66	GPIO65	GPIO69	GPIO53	GPIO55	GPIO59	GPIO4	GPIO11	GPIO10	VDD33	GPIO85	GPIO92	GPIO94	GND	11
10	GND	GPIO45	GPIO62	GPIO73	VDD33	RGMII5_VDDQ	RGMII5_VDDQ	RGMII1_VDDQ	RGMII1_VDDQ	GND	VDD11	MRESET_OUT	MCLK_XO	MCLK_XI	10
9	GPIO47	GPIO43	GPIO42	GPIO44	VDD11	GND	VDD11	GND	VDD11	PLL_AVDD	PLL_AGND	MRESET_N	USB_VBUS	USB_GND	9
8	GPIO46	GPIO39	GPIO38	GPIO41	RGMII4_VDDQ	GND	GND	GND	GND	USB_AVDD	USB_RREF	USB_GND	USB_DM1	USB_DP1	8
7	GND	GPIO36	GPIO37	GPIO40	RGMII4_VDDQ	VDD11	GND	GND	VDD11	USB_VD33	USB_VD33	USB_GND	USB_DM2	USB_DP2	7
6	GPIO61	GPIO77	GPIO79	GPIO76	VDD33	GND	GND	GND	GND	GND	ADC1_AVDD	ADC1_VREFN	USB_GND	USB_GND	6
5	GPIO60	GPIO75	GPIO78	GPIO74	VDD11	GND	VDD11	VDD11	GND	VDD11	ADC1_AGND	ADC1_VREFP	ADC1_IN8	ADC1_IN7	5
4	GND	VDD33	VDD33	GND	VDD33	GPIO105	GPIO107	GPIO112	VDD33	VDD33	TMC2	ADC1_IN2	ADC1_IN0	ADC1_IN6	4
3	N.C.	VDD33	GPIO97	GPIO95	GPIO100	GPIO103	GPIO111	GPIO115	GPIO117	CTRSTBYB	CONFIG1	TMC1	ADC1_IN4	ADC1_IN3	3
2	GND	GPIO98	GPIO96	GPIO102	GPIO104	GPIO108	GPIO110	GPIO114	GPIO116	THMODE	CONFIG0	JTAG_TCK	JTAG_TMS	ADC1_IN1	2
1	GND	GPIO99	GPIO101	GND	GPIO106	GPIO109	GND	GPIO113	GPIO118	GND	JTAG_TDO	JTAG_TRST_N	JTAG_TDI	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 10.5 RZ/N1L Pinout BGA-196 (Top View)

Section 11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 11.1 Absolute Maximum Ratings

Parameter		Symbol	Conditions	Value	Unit
Power supply voltage	Logic core	V_{DD11}	—	−0.45 to +1.6	V
	I/O	V_{DD33}	—	−0.5 to +4.6	V
	I/O for RGMII	V_{RGMII}	—	−0.5 to +4.6	V
	PLL	V_{PLL}	—	−0.45 to +1.6	V
	USB	V_{USB}	—	−0.5 to +4.6	V
	ADC	V_{ADC}	—	−0.5 to +4.6	V
	RTC	V_{RTC}	—	−0.5 to +4.6	V
	DDRPHY I/O	V_{DVDDQ}	—	−0.5 to +2.5	V
	DDRPHY core	V_{DVDD}	—	−0.45 to +1.6	V
	DDRPHY reference	$V_{DDR\ REF}$	—	−0.5 to +2.5	V
	OTP memory programming	V_{ANFPRG}	—	−0.5 to +7.5	V
Input/output voltage		V_I / V_O	V_I / V_O < V_{DD33} + 0.5 V	−0.5 to +4.6	V
Storage temperature		T_{stg}	—	−55 to +125	°C

CAUTION

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding the absolute maximum ratings can cause permanent damage. The parameters apply independently. The device should be operated within the limits specified by the DC and AC characteristics.

11.2 Recommended Operating Conditions

Table 11.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply voltage	V_{DD11}		1.10	1.15	1.20	V
	V_{DD33}		3.0	3.3	3.6	V
	V_{RGMII}	RGMII mode	3.14	3.3	3.46	V
	V_{PLL}		1.10	1.15	1.20	V
	V_{USB}		3.0	3.3	3.6	V
	V_{ADC}		3.0	3.3	3.6	V
	$V_{ADC\ REFP}$		V_{ADC}			V
	$V_{ADC\ REFM}$		0			V
	V_{RTC}	Normal mode $\lvert V_{DD33} - V_{RTC} \rvert \leq 0.3$	3.0	3.3	3.6	V
		Backup mode	1.8	—	3.6	V
	V_{DVDDQ}	DDR3	1.425	1.5	1.575	V
		DDR2	1.7	1.8	1.9	V
	V_{DVDD}		1.10	1.15	1.20	V
	$V_{DDR\ REF}$		V_{DVDDQ} × 0.49	V_{DVDDQ} × 0.50	V_{DVDDQ} × 0.51	V
	V_{ANFPRG}	OTP memory programming	6.8	6.9	7.0	V
		Normal	—	0	—	V
Clock input frequency	f_{OSC}	±50 ppm*1	—	40.0	—	MHz
Junction temperature	T_j		−40	—	110	°C

Note 1. ±25 ppm for EtherCAT

11.3 DC Characteristics

11.3.1 Current

Table 11.3 Current

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Current drain	I_{DD11}	RZ/N1D		—	—	1450	mA
		RZ/N1S, RZ/N1L		—	—	1300	mA
	I_{DD33}			—	—	250	mA
	I_{RGMII}	RGMII 1 ch		—	—	50	mA
	I_{PLL}	RZ/N1S, RZ/N1L only		—	—	15	mA
	I_{USB}	2 ports used		—	—	125	mA
	I_{ADC}	ADC 1 unit		—	—	12	mA
	$I_{ADC\ REF}$	ADC 1 unit		—	—	300	µA
	I_{RTC_NM}	Normal mode RTC_PCLK is supplied		—	—	1.5	mA
	I_{RTC_BU}	Backup mode T_j = 0 to 40°C, V_{RTC} = 3.0 V		—	2.0	4.0	µA
	I_{DVDDQ}	DDR3		—	—	210	mA
	I_{DVDD}	DDR3		—	—	140	mA
	I_{ANFPRG}	OTP memory programming		—	—	30	mA
Input leakage current	I_{LI}	V_I = V_{DD33} or GND		—	—	±5	µA
		V_I = GND with internal pull-up		−36		−96	µA
		V_I = V_{DD33} with internal pull-down		37		96	µA
Output current high	$-I_{OH}$*1	V_{OH} = 2.4 V	4 mA	4	—	—	mA
			6 mA	6	—	—	mA
			8 mA	7.8	—	—	mA
			12 mA	9.5	—	—	mA
Output current low	I_{OL}*1	V_{OL} = 0.4 V	4 mA	4	—	—	mA
			6 mA	6	—	—	mA
			8 mA	7.8	—	—	mA
			12 mA	9.5	—	—	mA

Note 1. Total output current values are strongly recommended to be within the values I_{DD33} and I_{RGMII} to ensure the reliability of this LSI.
I_{DD33}: Total output current values of I/O pins from GPIO60 to GPIO169
I_{RGMII}: Total output current values of each channel I/O pins (GPIO11 to GPIO0, GPIO23 to GPIO12, GPIO35 to GPIO24, GPIO47 to GPIO36, GPIO59 to GPIO48)

11.3.2 Digital IO

Table 11.4 Digital IO

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	3.3 V input	2.0	—	V_{DD33} + 0.3	V
Low-level input voltage	V_{IL}	3.3 V input	−0.3	—	0.8	V
Positive trigger voltage	V_P	Schmitt input	0.9	—	2.1	V
Negative trigger voltage	V_N	Schmitt input	0.7	—	1.9	V
Hysteresis of Schmitt trigger	V_{H1}	Schmitt input	0.2	—	1.4	V
High-level output voltage	V_{OH}	I_{OH}	2.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL}	0	—	0.4	V
Input rise/fall time data	t_{rid} / t_{fid}	—	0	—	200	ns
Input rise/fall time clock	t_{ric} / t_{fic}	—	0	—	4	ns
Input rise/fall time Schmitt	t_{ris} / t_{fis}	—	0	—	1	ms
Pull up/down resistor	R_{PUUD}	—	37	50	82	kΩ
Input capacitance	Cin	—	—	—	6.0	pF

11.3.3 DDR3/DDR2 SDRAM Interface

Table 11.5 DDR3/DDR2 SDRAM Interface

Parameter	Symbol	Min	Typ	Max	Unit	Note
Reference voltage input	$V_{DDR\ REF}$	V_{DVDDQ} × 0.49	V_{DVDDQ} × 0.50	V_{DVDDQ} × 0.51	V	
DC input logic high	V_{DDRIH} (dc)	$V_{DDR\ REF}$ + 0.1	—	V_{DVDDQ}	V	*1
DC input logic low	V_{DDRIL} (dc)	0	—	$V_{DDR\ REF}$ − 0.1	V	*1
DC differential input high	$V_{DDRIHdiff}$ (dc)	0.400	—	—	V	*2
DC differential input low	$V_{DDRILdiff}$ (dc)	—	—	−0.400	V	*2
AC input logic high	V_{DDRIH} (ac)	$V_{DDR\ REF}$ + 0.150	—	V_{DVDDQ} + 0.5	V	*3
AC input logic low	V_{DDRIL} (ac)	−0.5	—	$V_{DDR\ REF}$ − 0.150	V	*3
AC differential input high	$V_{DDRIHdiff}$ (ac)	0.500	—	—	V	*2
AC differential input low	$V_{DDRILdiff}$ (ac)	—	—	−0.500	V	*2
AC differential cross point voltage (input)	V_{DDRIX} (ac)	0.5 × V_{DVDDQ} − 0.150	—	0.5 × V_{DVDDQ} + 0.150	V	*2
AC differential cross point voltage (output)	V_{DDROX} (ac)	0.5 × V_{DVDDQ} − 0.050	—	0.5 × V_{DVDDQ} + 0.050	V	*4

Note 1. DDR_DQ, DDR_DQS, DDR_DQS_N

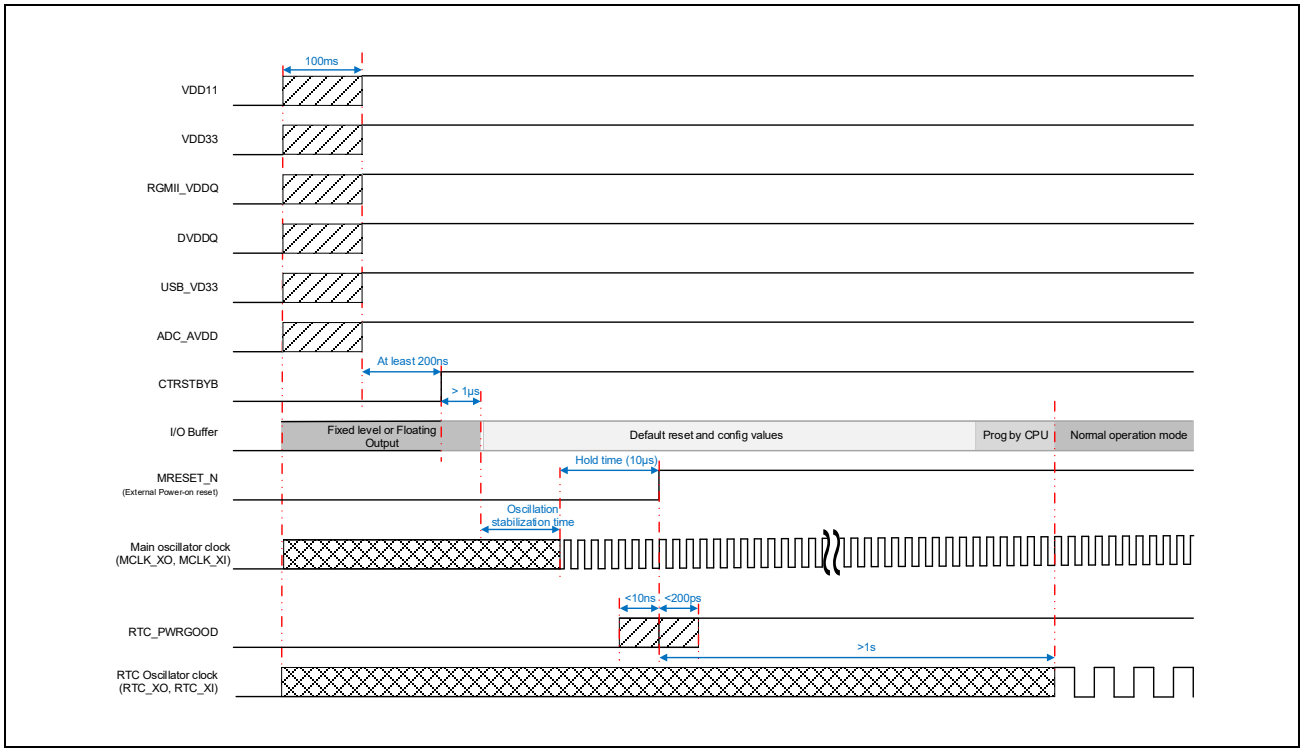
Note 2. DDR_DQS, DDR_DQS_N

Note 3. DDR_DQ

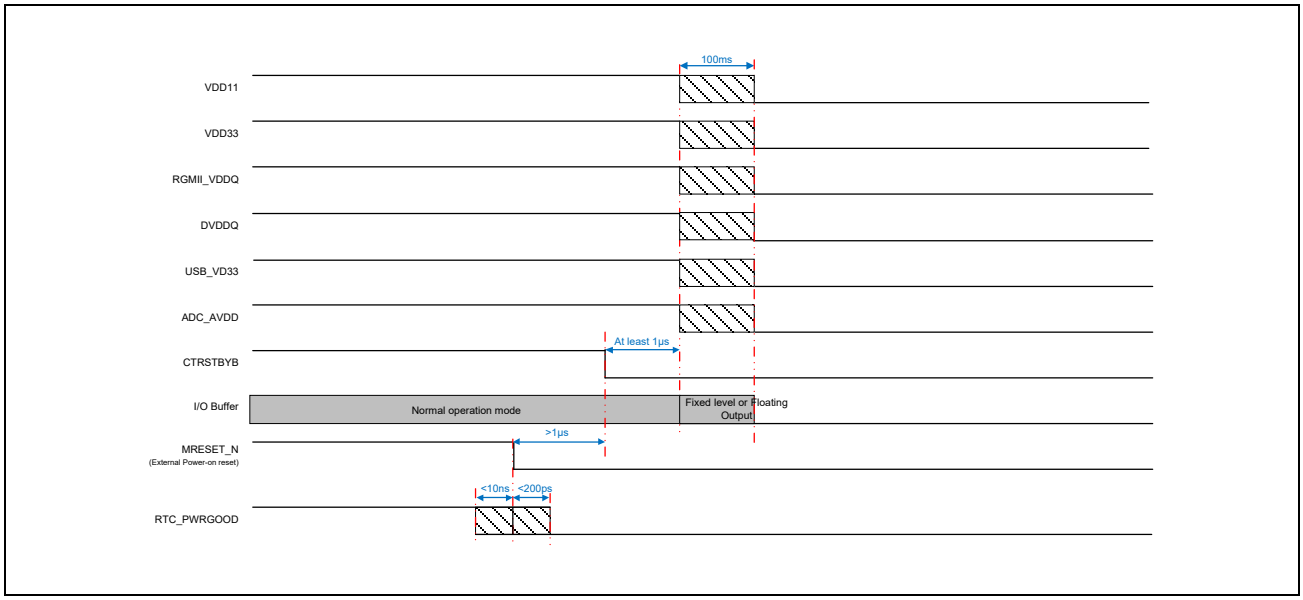
Note 4. DDR_CLKP, DDR_CLKN, DDR_DQS, DDR_DQS_N

11.4 Power-up/down Sequence

11.4.1 Power-up



11.4.2 Power-down



CAUTION

Release the reset after the oscillation stabilization time of the main oscillator clock.

If RTC is not used, the startup time (t_{START}) of the RTC Oscillator clock is not necessary. The timing control is required for RTC_PWRGOOD when RTC backup mode.

11.5 AC Timing Characteristics

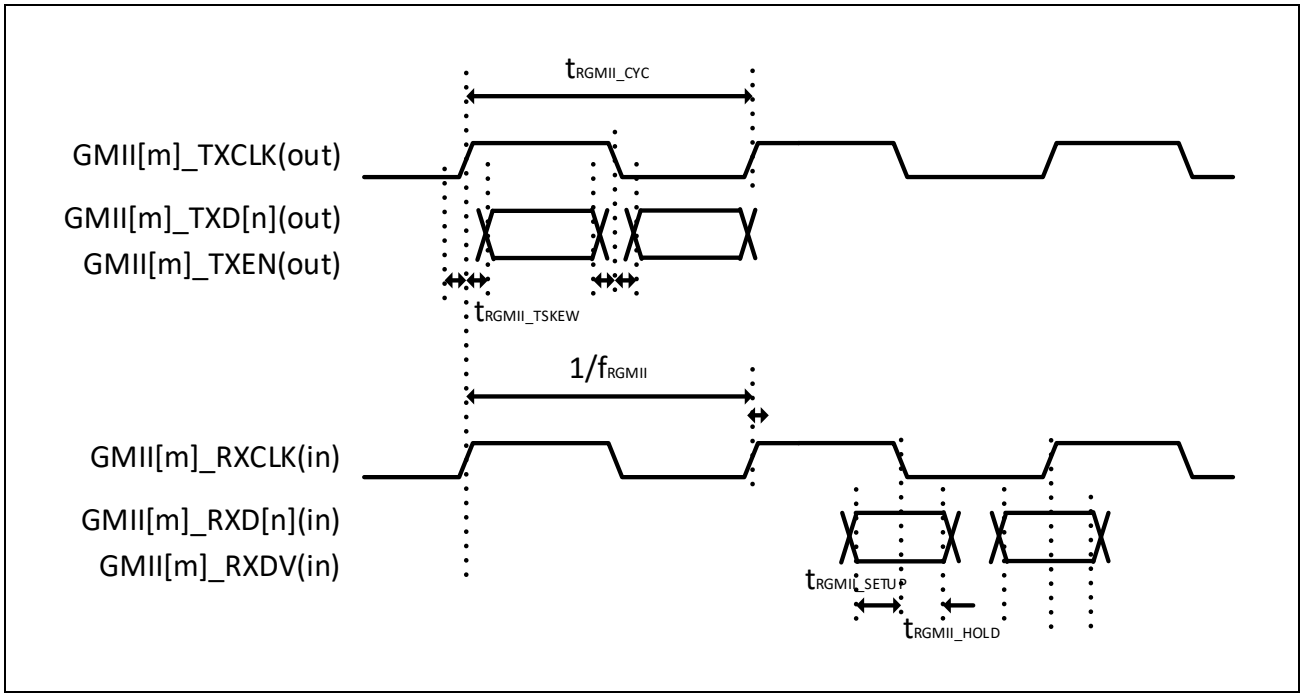
11.5.1 Ethernet MAC Interface Timing

11.5.1.1 RGMII

Table 11.6 RGMII

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GMII[m]_TXCLK/RXCLK frequency	f_{RGMII}	±50 ppm	—	125	—	MHz
GMII[m]_TXCLK/RXCLK clock cycle duration	t_{RGMII_CYC}	—	7.2	8	8.8	ns
Rise/fall time of signals	$t_{RGMII\_RISEFALL}$	20%–80%			0.75	ns
GMII[m]_TXCLK/RXCLK duty cycle	$t_{RGMII\_CLK\_DUTY}$	—	45	50	55	%
GMII[m]_TXD[n] GMII[m]_TXEN (TX_CTL) to GMII[m]_TXCLK skew	t_{RGMII_TSKEW}	GMII[m]_TXCLK Rise/fall	−0.5	—	0.5	ns
GMII[m]_RXD[n] GMII[m]_RXDV (RX_CTL) setup time	t_{RGMII_SETUP}	GMII[m]_RXCLK Rise/fall	1	—	—	ns
GMII[m]_RXD[n] GMII[m]_RXDV (RX_CTL) hold time	t_{RGMII_HOLD}		1	—	—	ns

Note: m = 1..5, n = 0..3, load capacitance $C_{L(max)}$ = 15 pF, drive strength 8 mA
Voltage condition should be compliant with V_{RGMII}.



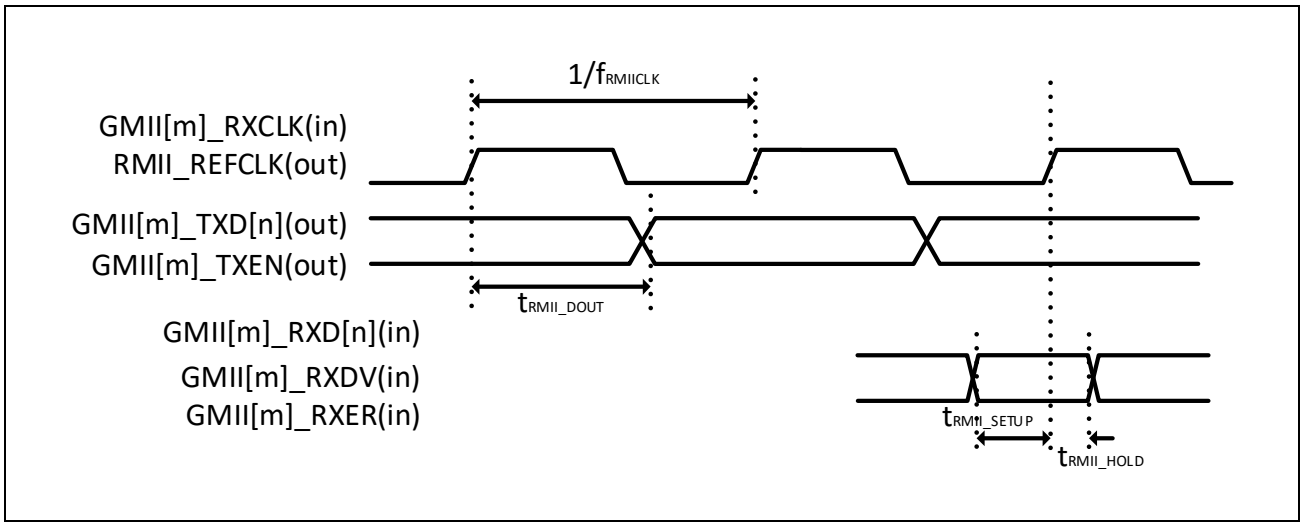
11.5.1.2 RMII

Table 11.7 RMII

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GMII[m]_RXCLK/RMII_REFCLK frequency*1	$f_{RMIICLK}$	±50 ppm	—	50	—	MHz
GMII[m]_RXCLK/RMII_REFCLK duty cycle*1	$t_{RMII\_CLK\_DUTY}$	—	35		65	%
GMII[m]_TXD[n]/TXEN enable delay time	t_{RMII_DOUT}	GMII[m]_RXCLK/RMII_REFCLK rise*1	2	—	10	ns
GMII[m]_RXD[n]/RXDV/RXER setup time	t_{RMII_SETUP}		4	—	—	ns
GMII[m]_RXD[n]/RXDV/RXER hold time	t_{RMII_HOLD}		2	—	—	ns

Note: m = 1..5, n = 0..1, load capacitance $C_{L(max)}$ = 25 pF, drive strength 8 mA

Note 1. Reference Clock Input: GMII[m]_RXCLK, Reference Clock Output: RMII_REFCLK

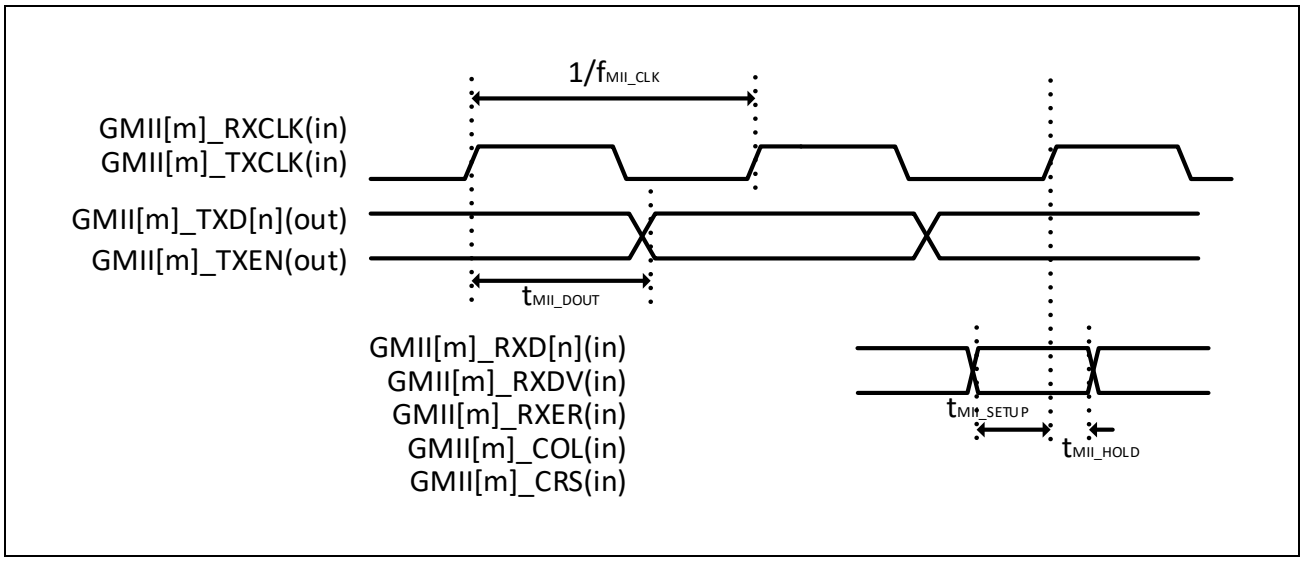


11.5.1.3 MII

Table 11.8 MII

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GMII[m]_TXCLK/RXCLK frequency	f_{MII_CLK}	±50 ppm	—	25	—	MHz
GMII[m]_TXD[n]/TXEN enable delay time	t_{MII_DOUT}	GMII[m]_RXCLK rise	0	—	25	ns
GMII[m]_RXD[n] /RXDV/RXER/COL/CRS setup time	t_{MII_SETUP}		10	—	—	ns
GMII[m]_RXD[n] /RXDV/RXER/COL/CRS hold time	t_{MII_HOLD}		10	—	—	ns

Note: m = 1..5, n = 0..3, load capacitance $C_{L(max)}$ = 30 pF, drive strength 8 mA



11.5.1.4 MDIO

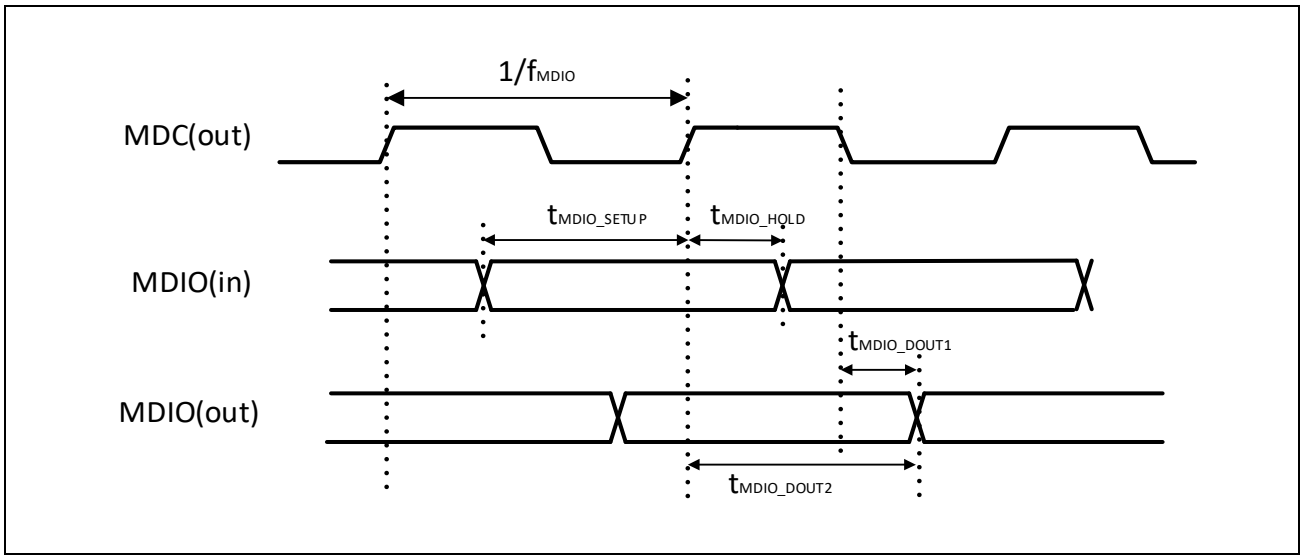
Table 11.9 MDIO

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MDC[m] Frequency*1	f_{MDIO}		—	—	12.5	MHz
MDIO[m] Output delay*2	t_{MDIO_DOUT1}	MDC fall	−20	—	20	ns
	t_{MDIO_DOUT2}	MDC rise	reg_delay ×T_{A5PSW_HCLK} −20	—	reg_delay ×T_{A5PSW_HCLK} +20	ns
MDIO[m] Input setup time	t_{MDIO_SETUP}	MDC rise	20	—	—	ns
MDIO[m] Input hold time	t_{MDIO_HOLD}		0	—	—	ns

Note: m = 1..2, load capacitance $C_{L(max)}$ = 30 pF, drive strength 8 mA

Note 1. The frequency from EtherCAT is 2.5 MHz.

Note 2. Other than A5PSW: t_{MDIO_DOUT1}, A5PSW: t_{MDIO_DOUT2}
The output timing from A5PSW is based on the rising edge of MDC, and the output delay can be set in the register.
T_{A5PSW_HCLK}: AHB clock period of A5PSW, reg_delay: Number of delay cycles for register setting



11.5.2 Memory Interface Timing

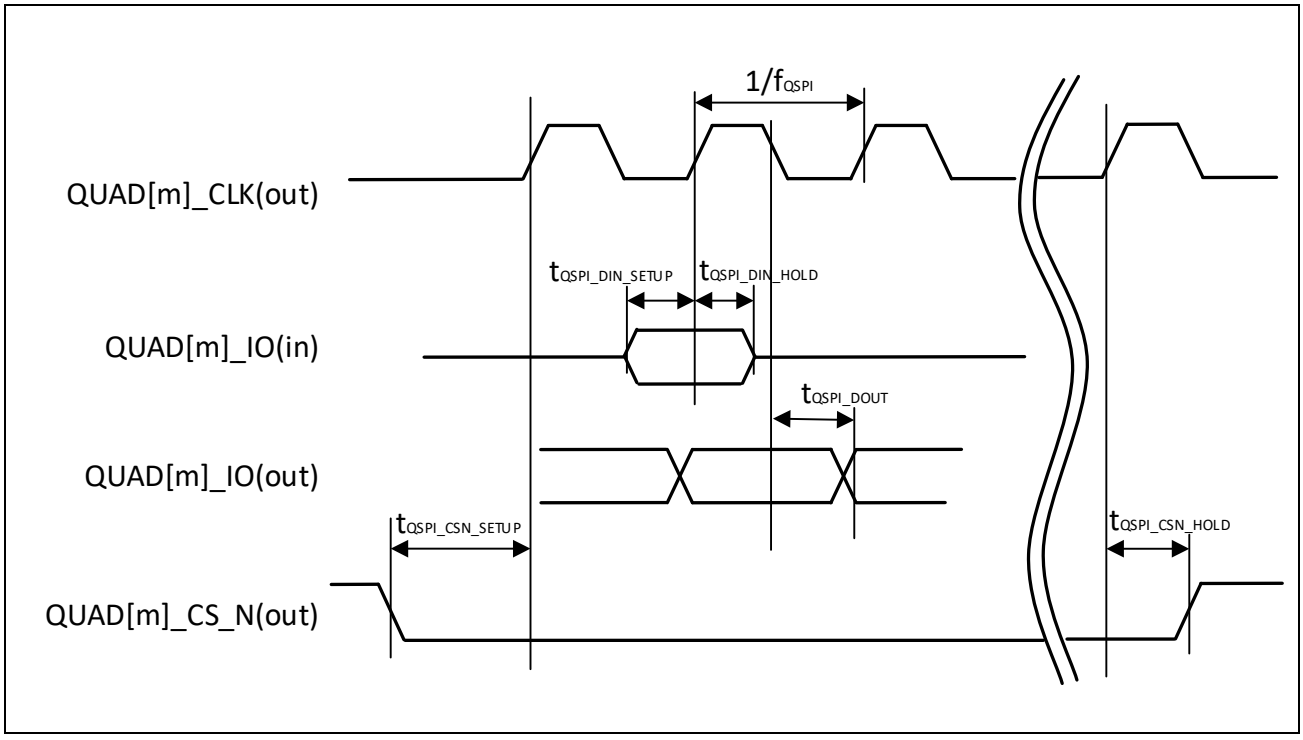
11.5.2.1 QSPI Flash Interface

Table 11.10 QSPI Flash Interface

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
QUAD[m]_CLK frequency*1	f_{QSPI}	—	—	—	62.5	MHz
QUAD[m]_IO input setup time	$t_{QSPI\_DIN\_SETUP}$	QUAD[m]_CLK rise	10 − T_{REF} × D_{RD}	—	—	ns
QUAD[m]_IO input hold time	$t_{QSPI\_DIN\_HOLD}$		T_{REF} × D_{RD} − 3	—	—	ns
QUAD[m]_IO delay time	t_{QSPI_DOUT}	QUAD[m]_CLK fall	−3	—	4	ns
QUAD[m]_CS_N setup time	$t_{QSPI\_CSN\_SETUP}$	QUAD[m]_CLK rise	0.5T − 3	—	—	ns
QUAD[m]_CS_N hold time	$t_{QSPI\_CSN\_HOLD}$		0.5T − 3	—	—	ns

Note: m = 1..2, load capacitance $C_{L(max)}$ = 30 pF, drive strength 8 mA
T= QUAD[m]_CLK period, T_{REF} = QSPI[m]_REFCLK period, D_{RD} = Read Delay setting of QSPI Read Data Capture Register

Note 1. QSPI Interface is able to shift internal capture edge by register setting.



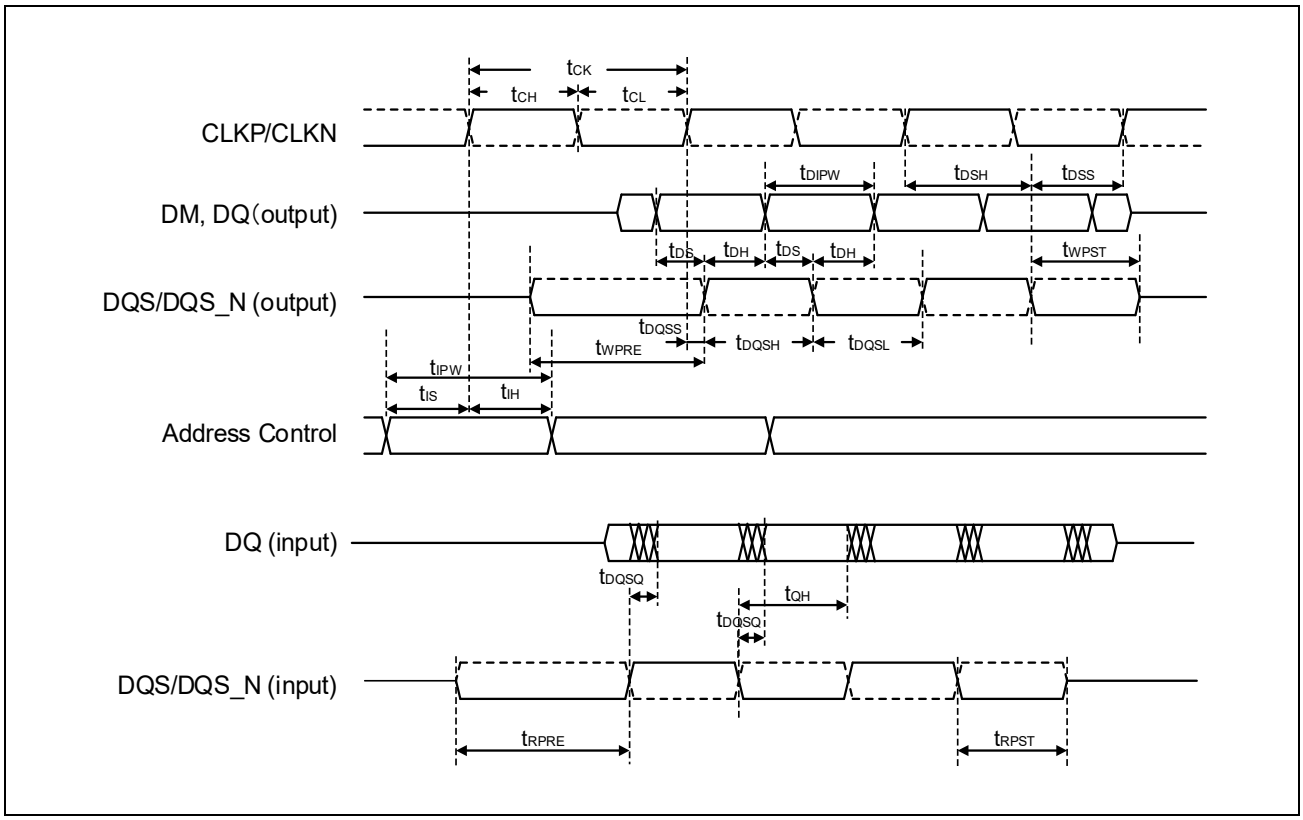
11.5.2.2 DDR3/DDR2 Interface

Table 11.11 DDR3-1000

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
CLK cycle time	t_{CK}	2000	—	—	ps	Average
CLKP/CLKN high level width	t_{CH}	0.47 × t_{CK} + 10 ps	—	0.53 × t_{CK} − 10 ps	t_{CK}	Average
CLKP/CLKN low level width	t_{CL}	0.47 × t_{CK} + 10 ps	—	0.53 × t_{CK} − 10 ps	t_{CK}	Average
DQ, DM setup time	t_{DS}	320	—	—	ps	DQ: 1.0 V/ns, DQS: 2.0 V/ns converted
DQ, DM hold time	t_{DH}	290	—	—	ps	DQ: 1.0 V/ns, DQS: 2.0 V/ns converted
Control & Address pulse width for each signal	t_{IPW}	1600	—	—	ps	—
DQ, DM pulse width for each signal	t_{DIPW}	800	—	—	ps	—
DQ, DM skew for DQS and associated DQ signals	t_{DQSQ}	—	—	245	ps	—
DQ hold time from DQS	t_{QH}	675	—	—	ps	—
Write command to first DQS latching transition	t_{DQSS}	−250	—	+250	ps	—
DQS/DQS_N high pulse width	t_{DQSH}	0.45 × t_{CK} + 10 ps	—	0.55 × t_{CK} − 10 ps	t_{CK}	—
DQS/DQS_N low pulse width	t_{DQSL}	0.45 × t_{CK} + 10 ps	—	0.55 × t_{CK} − 10 ps	t_{CK}	—
DQS/DQS_N falling edge to CLKP/CLKN setup time	t_{DSS}	0.325	—	—	t_{CK}	—
DQS/DQS_N falling edge hold time from CLKP/CLKN	t_{DSH}	0.325	—	—	t_{CK}	—
Write preamble	t_{WPRE}	0.91	—	—	t_{CK}	—
Write postamble	t_{WPST}	0.31	—	—	t_{CK}	—
Read preamble	t_{RPRE}	0.89	—	—	t_{CK}	—
Read postamble	t_{RPST}	0.25	—	—	t_{CK}	—
Address and control signal setup time	t_{IS}	670	—	—	ps	CMD, ADD: 1.0 V/ns CLK: 2.0 V/ns converted
Address and control signal hold time	t_{IH}	670	—	—	ps	CMD, ADD: 1.0 V/ns CLK: 2.0 V/ns converted

Table 11.12 DDR2-500

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
CLK cycle time	t_{CK}	4000	—	—	ps	Average
CLKP/CLKN high level width	t_{CH}	0.48 × t_{CK} + 10 ps	—	0.52 × t_{CK} − 10 ps	t_{CK}	Average
CLKP/CLKN low level width	t_{CL}	0.48 × t_{CK} + 10 ps	—	0.52 × t_{CK} − 10 ps	t_{CK}	Average
DQ, DM setup time	t_{DS}	500	—	—	ps	DQ: 1.0 V/ns, DQS: 2.0 V/ns converted
DQ, DM hold time	t_{DH}	500	—	—	ps	DQ: 1.0 V/ns, DQS: 2.0 V/ns converted
Control & Address pulse width for each signal	t_{IPW}	0.8	—	—	t_{CK}	—
DQ, DM pulse width for each signal	t_{DIPW}	0.4	—	—	t_{CK}	—
DQ, DM skew for DQS and associated DQ signals	t_{DQSQ}	—	—	450	ps	—
DQ hold time from DQS	t_{QH}	1100	—	—	ps	—
Write command to first DQS latching transition	t_{DQSS}	−0.125	—	+0.125	t_{CK}	—
DQS/DQS_N high pulse width	t_{DQSH}	0.41 × t_{CK} + 10 ps	—	—	t_{CK}	—
DQS/DQS_N low pulse width	t_{DQSL}	0.41 × t_{CK} + 10 ps	—	—	t_{CK}	—
DQS/DQS_N falling edge to CLKP/CLKN setup time	t_{DSS}	0.325	—	—	t_{CK}	—
DQS/DQS_N falling edge hold time from CLKP/CLKN	t_{DSH}	0.325	—	—	t_{CK}	—
Write preamble	t_{WPRE}	0.26	—	—	t_{CK}	—
Write postamble	t_{WPST}	0.41	—	—	t_{CK}	—
Read preamble	t_{RPRE}	0.89	—	—	t_{CK}	—
Read postamble	t_{RPST}	0.35	—	—	t_{CK}	—
Address and control signal setup time	t_{IS}	1400	—	—	ps	CMD, ADD: 1.0 V/ns CLK: 2.0 V/ns converted
Address and control signal hold time	t_{IH}	1400	—	—	ps	CMD, ADD: 1.0 V/ns CLK: 2.0 V/ns converted

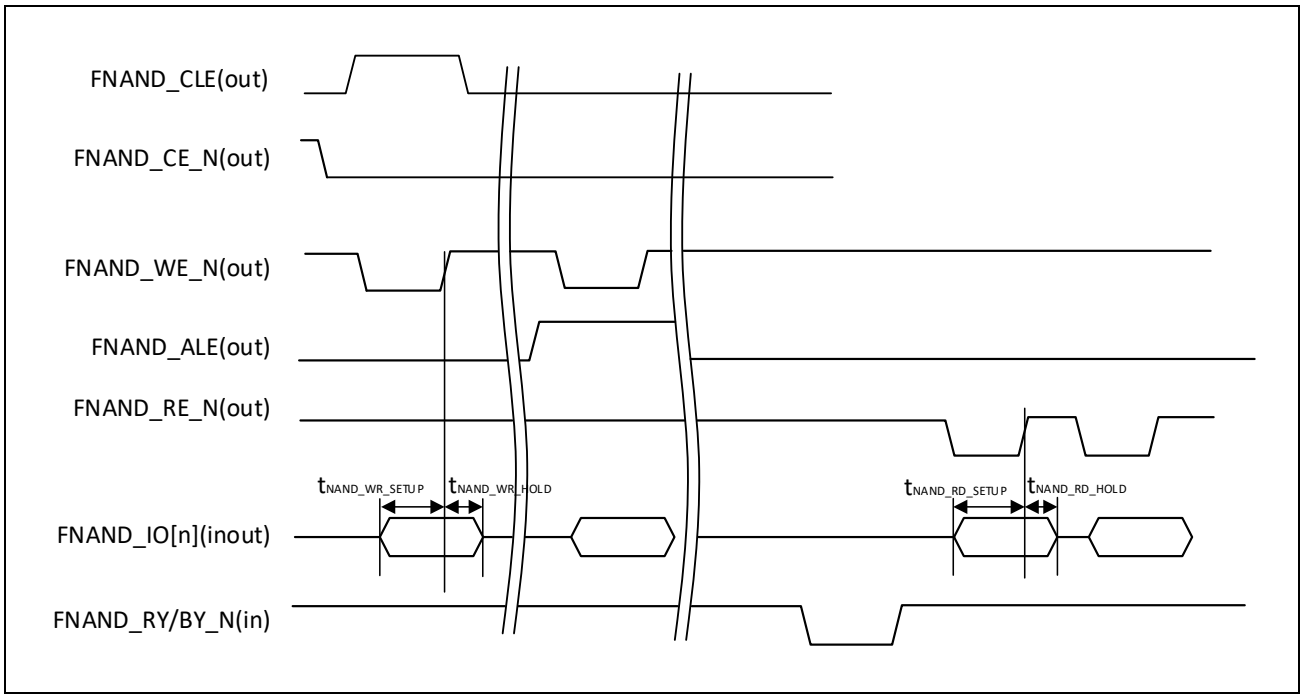

tCK
tCH
tCL
CLKP/CLKN
tDIPW
tDSH
tDSS
DM, DQ(output)
tDS
tDH
tDS
tDH
tWPST
DQS/DQS_N (output)
tDQSS
tWPRE
tDQSH
tDQSL
tIPW
tIS
tIH
Address Control
DQ (input)
tDQSQ
tQH
tDQSQ
DQS/DQS_N (input)
tRPRE
tRPST

11.5.2.3 NAND Flash Interface

Table 11.13 NAND Flash Interface

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Write data setup time	$t_{NAND\_WR\_SETUP}$	FNAND_WE_N rise	$n_1 \times T - 6$	—	—	ns
Write data hold time	$t_{NAND\_WR\_HOLD}$		$n_2 \times T - 6$	—	—	ns
Read data setup time	$t_{NAND\_RD\_SETUP}$	FNAND_RE_N rise	10	—	—	ns
Read data hold time	$t_{NAND\_RD\_HOLD}$		0	—	—	ns

Note: load capacitance $C_{L(max)}$ = 25 pF, drive strength 8 mA
T = NAND_ECLK period, n_1 and n_2 are register setting.



11.5.2.4 SD/eMMC/SDIO Interface

Table 11.14 SD Bus Timing (Default Mode)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SDIO_CLK frequency (Data transfer mode)	f_{SD}	—	—	—	25	MHz
SDIO_CLK clock low width	t_{SD_CKLO}	—	16	—	—	ns
SDIO_CLK clock high width	t_{SD_CKHI}	—	16	—	—	ns
SDIO_CLK clock rise time	t_{SD_CKRISE}	V_{OL} to V_{OH}	—	—	2	ns
SDIO_CLK clock fall time	t_{SD_CKFALL}	V_{OH} to V_{OL}	—	—	2	ns
Input CMD, IO setup time	t_{SD_SETUP}	SDIO_CLK rise	4	—	—	ns
Input CMD, IO hold time	t_{SD_HOLD}		2	—	—	ns
Output CMD, IO delay time during data transfer mode	t_{SD_DOUT}	SDIO_CLK fall	−2	—	11	ns

Note: load capacitance $C_{L(max)}$ = 30 pF, drive strength 8 mA

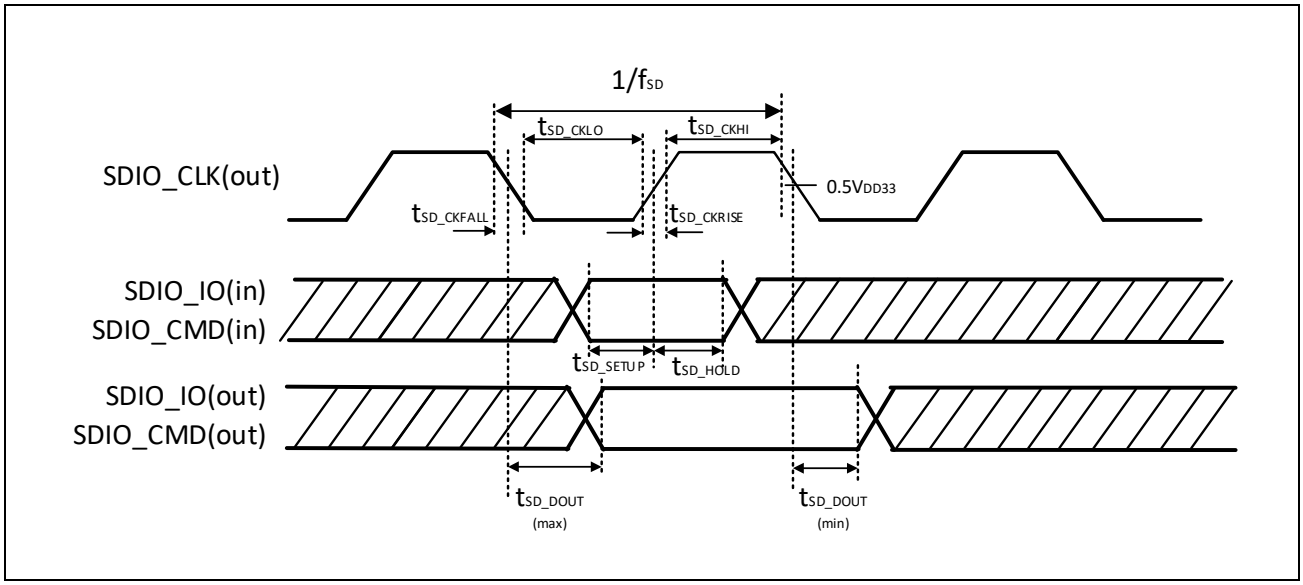
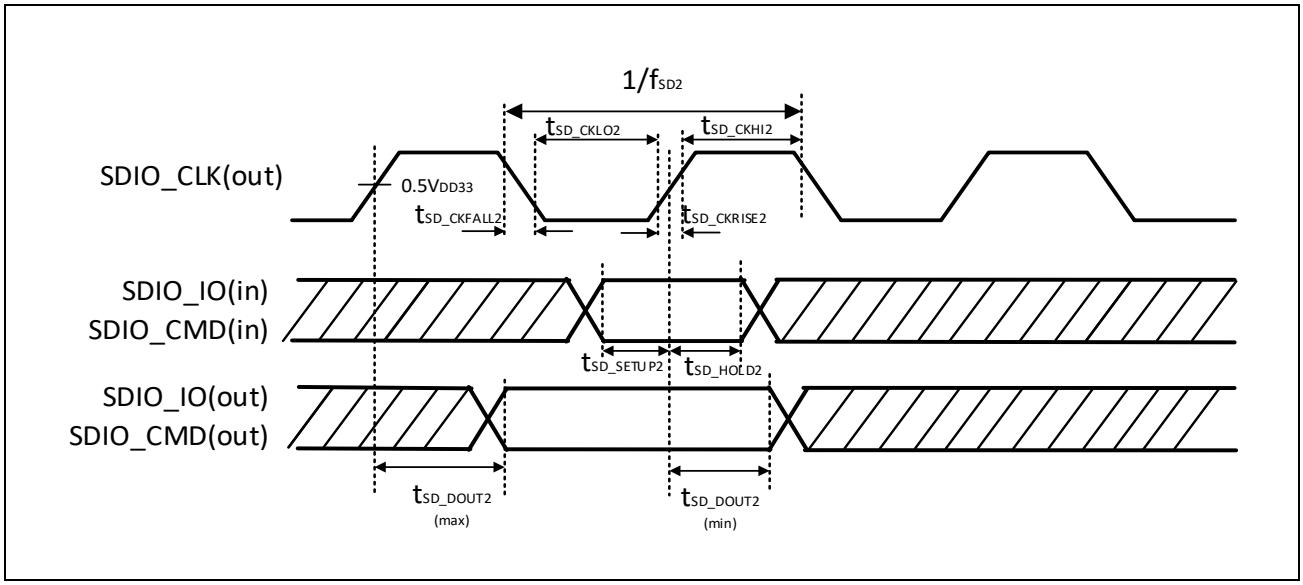


Table 11.15 SD Bus Timing (High Speed Mode)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SDIO_CLK frequency (Data transfer mode)	f_{SD2}	—	—	—	50	MHz
SDIO_CLK clock low width	t_{SD_CKLO2}	—	8	—	—	ns
SDIO_CLK clock high width	t_{SD_CKHI2}	—	8	—	—	ns
SDIO_CLK clock rise time	$t_{SD\_CKRISE2}$	V_{OL} to V_{OH}	—	—	1	ns
SDIO_CLK clock fall time	$t_{SD\_CKFALL2}$	V_{OH} to V_{OL}	—	—	1	ns
Input CMD, IO setup time	t_{SD_SETUP2}	SDIO_CLK rise	4	—	—	ns
Input CMD, IO hold time	t_{SD_HOLD2}		2	—	—	ns
Output CMD, IO delay time during data transfer mode	t_{SD_DOUT2}	SDIO_CLK rise	3	—	13	ns

Note: load capacitance $C_{L(max)}$ = 25 pF, drive strength 8 mA



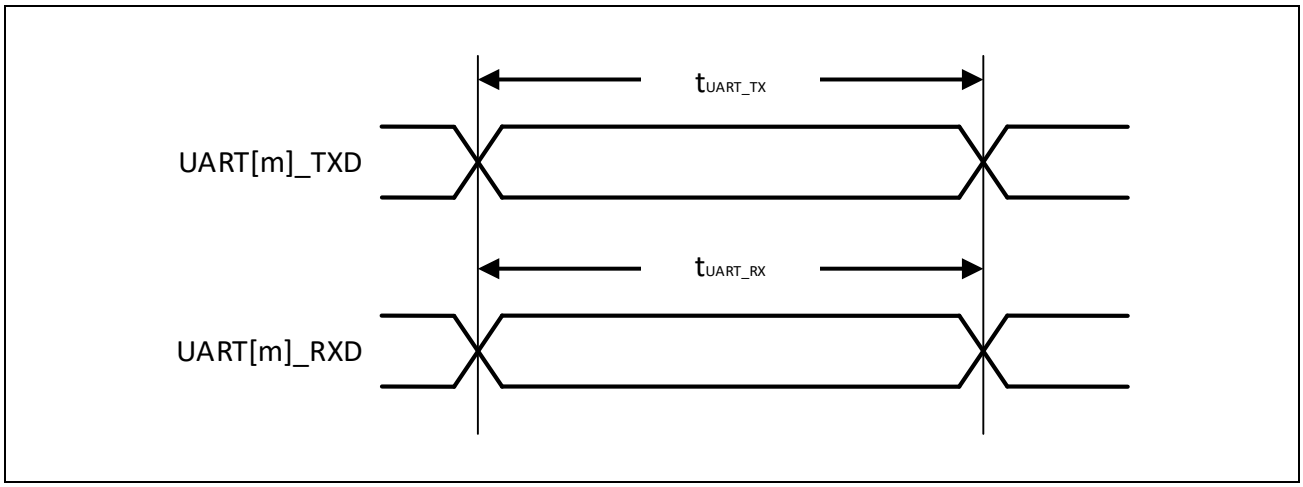
11.5.3 Serial Interface Timing

11.5.3.1 UART

Table 11.16 UART

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
UART[m]_TXD pulse width	t_{UART_TX}	—	192	—	—	ns
UART[m]_RXD pulse width	t_{UART_RX}	—	192	—	—	ns

Note: m = 1..8



11.5.3.2 SPI Master

Table 11.17 SPI Master

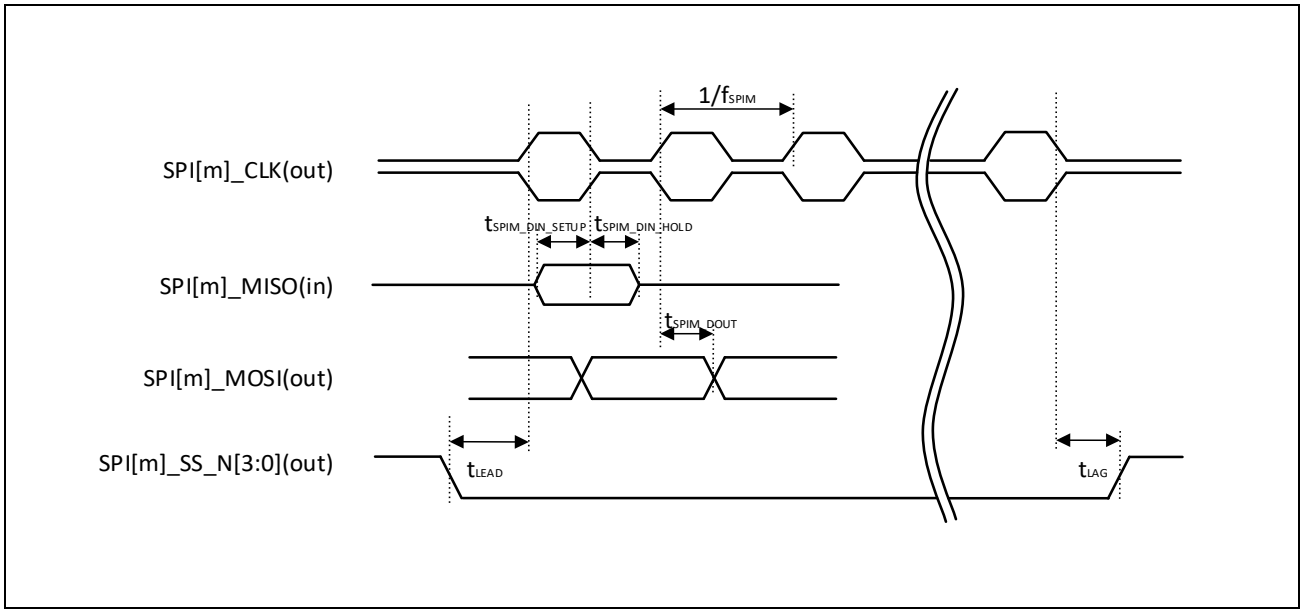
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SPI[m]_CLK frequency*1	f_{SPIM}	—	—	—	25	MHz
SPI[m]_MISO data input setup time	$t_{SPIM\_DIN\_SETUP}$	—	20	—	—	ns
SPI[m]_MISO data input hold time	$t_{SPIM\_DIN\_HOLD}$	—	0	—	—	ns
SPI[m]_MOSI delay time	t_{SPIM_DOUT}	—	−6	—	6	ns
SPI[m]_SS_N[3:0] output setup time	t_{LEAD}	—	$(N - 1) \times T_{REF} - 8$*2	—	—	ns
SPI[m]_SS_N[3:0] output hold time	t_{LAG}	—	$(N/2 + 1) \times T_{REF} - 6$*3	—	—	ns

Note: m = 1..4, load capacitance $C_{L(max)}$ = 25 pF, drive strength 8 mA
T_{REF} = Reference clock (SPI[m]_SCLK) period, N = SPI Clock Divider setting of Baud Rate Select Register

Note 1. The polarity of the SPI[m]_CLK can be changed by setting the register. In the default settings, the data output starts at the falling edge of the SPI[m]_CLK and the data capture starts at the rising edge. Default (bSpi_SCPOL = 1: inactive state of the serial clock is high, bSpi_SCPH = 1: the first serial clock toggles at start of the data bit)

Note 2. When Motorola SPI (bSpi_SCPH = 0): $[(N/2 - 1) \times T_{REF} - 8]$

Note 3. When Texas Instruments Synchronous Serial Protocol: $[T_{REF} - 6]$



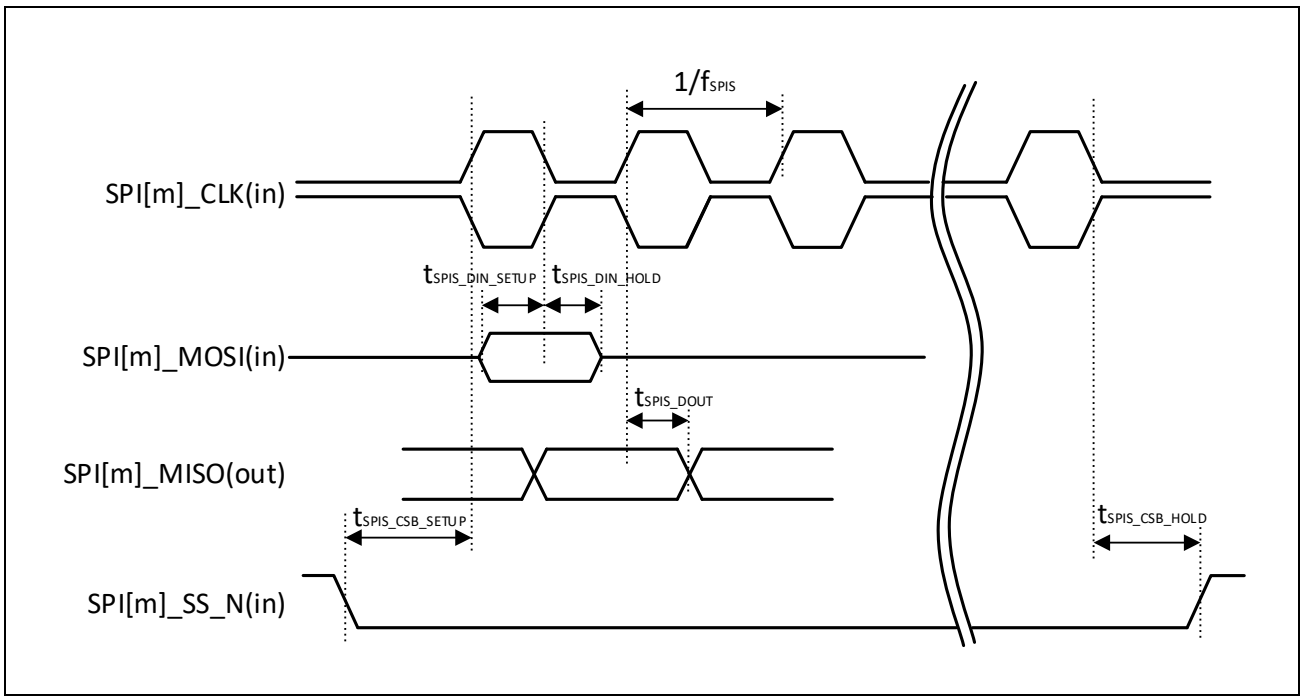
11.5.3.3 SPI Slave

Table 11.18 SPI Slave

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SPI[m]_CLK input frequency*1	f_{SPIS}	—	—	—	12.5	MHz
SPI[m]_MOSI data input setup time	$t_{SPIS\_DIN\_SETUP}$	—	0	—	—	ns
SPI[m]_MOSI data input hold time	$t_{SPIS\_DIN\_HOLD}$	—	$3T_{REF}$ + 4	—	—	ns
SPI[m]_MISO delay time	t_{SPIS_DOUT}	—	—	—	$3T_{REF}$ + 12	ns
SPI[m]_SS_N input setup time	$t_{SPIS\_CSB\_SETUP}$	—	$3T_{REF}$	—	—	ns
SPI[m]_SS_N input hold time	$t_{SPIS\_CSB\_HOLD}$	—	$3T_{REF}$	—	—	ns

Note: m = 5..6, load capacitance $C_{L(max)}$ = 25 pF, drive strength 8 mA
T_{REF} = Reference clock (SPI[m]_SCLK) period

Note 1. The polarity of the SPI[m]_CLK can be changed by setting the register. In the default settings, the data output starts at the falling edge of the SPI[m]_CLK and the data capture starts at the rising edge. Default (bSpi_SCPOL = 1: inactive state of the serial clock is high, bSpi_SCPH = 1: the first serial clock toggles at start of the data bit)

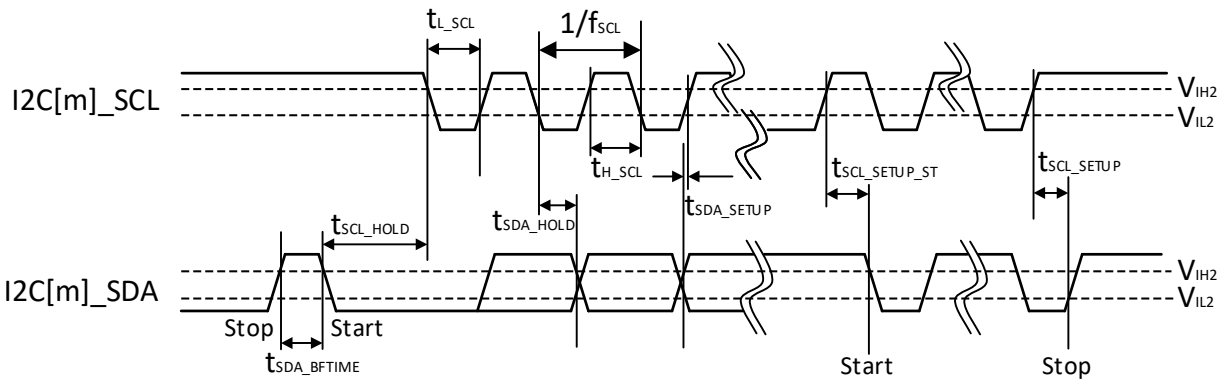


11.5.3.4 I2C

Table 11.19 I2C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I2C[m]_SCL clock frequency	f_{SCL}	Standard mode	—	—	100	kHz
		Fast mode	—	—	400	kHz
Bus free time (Stop and start)	t_{SDA_BFTIME}	Standard mode	4.7	—	—	µs
		Fast mode	1.3	—	—	µs
I2C[m]_SCL hold time (On start)	t_{SCL_HOLD}	Standard mode	4.0	—	—	µs
		Fast mode	0.6	—	—	µs
I2C[m]_SCL low width	t_{L_SCL}	Standard mode	4.7	—	—	µs
		Fast mode	1.3	—	—	µs
I2C[m]_SCL high width	t_{H_SCL}	Standard mode	4.0	—	—	µs
		Fast mode	0.6	—	—	µs
I2C[m]_SCL setup time (On start)	$t_{SCL\_SETUP\_ST}$	Standard mode	4.7	—	—	µs
		Fast mode	0.6	—	—	µs
I2C[m]_SDA hold time	t_{SDA_HOLD}	Standard mode	0	—	—	µs
		Fast mode	0	—	—	µs
I2C[m]_SDA setup time	t_{SDA_SETUP}	Standard mode	250	—	—	ns
		Fast mode	100	—	—	µs
I2C[m]_SCL setup time	t_{SCL_SETUP}	Standard mode	4.0	—	—	µs
		Fast mode	0.6	—	—	µs

Note: m = 1..2



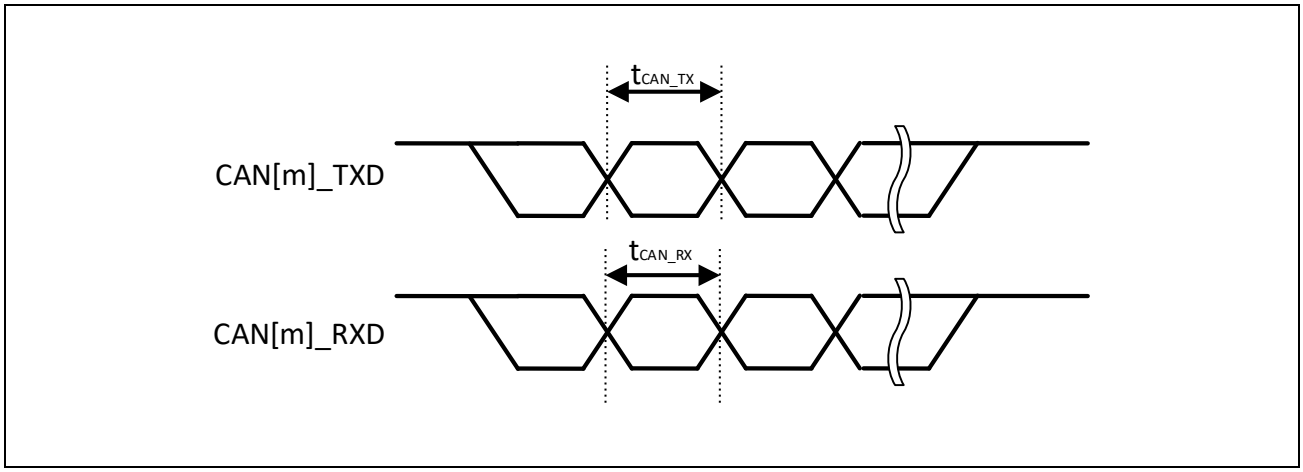
Note: V_{IH2}/V_{IL2} is V_{IH}/V_{IL} of I2C Bus Specification.

11.5.3.5 CAN

Table 11.20 CAN

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CAN baud rate	f_{CAN}	—	—	—	1	Mbaud
CAN[m]_TXD Pulse Width	t_{CAN_TX}	—	$1/f_{CAN} - 5$	—	$1/f_{CAN} + 5$	ns
CAN[m]_RXD Pulse Width	t_{CAN_RX}	—	$1/f_{CAN} - 5$	—	$1/f_{CAN} + 5$	ns

Note: m = 1..2



11.5.3.6 JTAG/SWD

Table 11.21 JTAG

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
JTAG_TCK input frequency	f_{JTAG}	—	—	—	10	MHz
JTAG_TCK low period	t_{JTAG_CL}	—	40	—	—	ns
JTAG_TCK high period	t_{JTAG_CH}	—	40	—	—	ns
JTAG_TMS/TDI setup time	t_{JTAG_SETUP}	JTAG_TCK rise	6	—	—	ns
JTAG_TMS/TDI hold time	t_{JTAG_HOLD}	JTAG_TCK rise	6	—	—	ns
JTAG_TDO output delay	t_{JTAG_DOUT}	JTAG_TCK fall	0	—	15	ns

Note: load capacitance $C_{L(max)}$ = 25 pF, drive strength 8 mA (fixed)

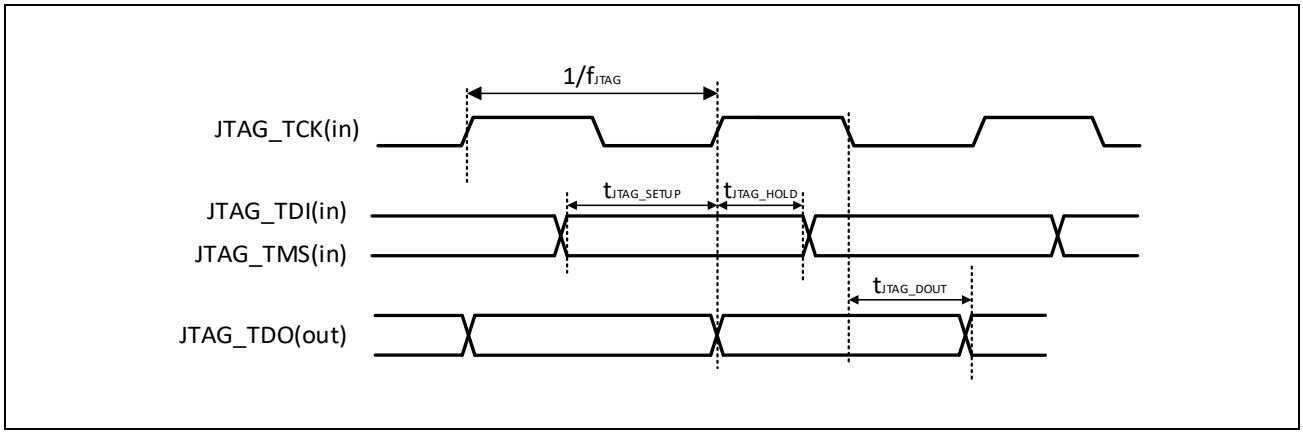
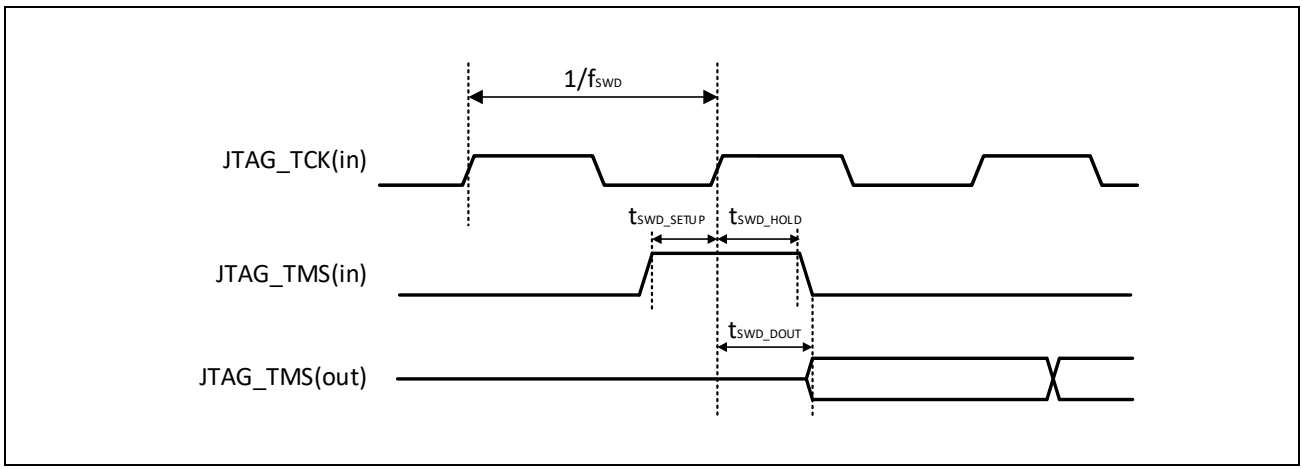


Table 11.22 Serial Wire Debug (SWD)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
JTAG_TCK (SWDCLK) input frequency	f_{SWD}	—	—	—	40	MHz
JTAG_TCK (SWDCLK) low period	t_{SWD_CL}	—	10	—	—	ns
JTAG_TCK (SWDCLK) high period	t_{SWD_CH}	—	10	—	—	ns
JTAG_TMS (SWDIO) setup time	t_{SWD_SETUP}	JTAG_TCK rise	4	—	—	ns
JTAG_TMS (SWDIO) hold time	t_{SWD_HOLD}	JTAG_TCK rise	4	—	—	ns
JTAG_TMS (SWDIO) output delay	t_{SWD_DOUT}	JTAG_TCK rise	2	—	15	ns

Note: load capacitance $C_{L(max)}$ = 25 pF, drive strength 8 mA (fixed)

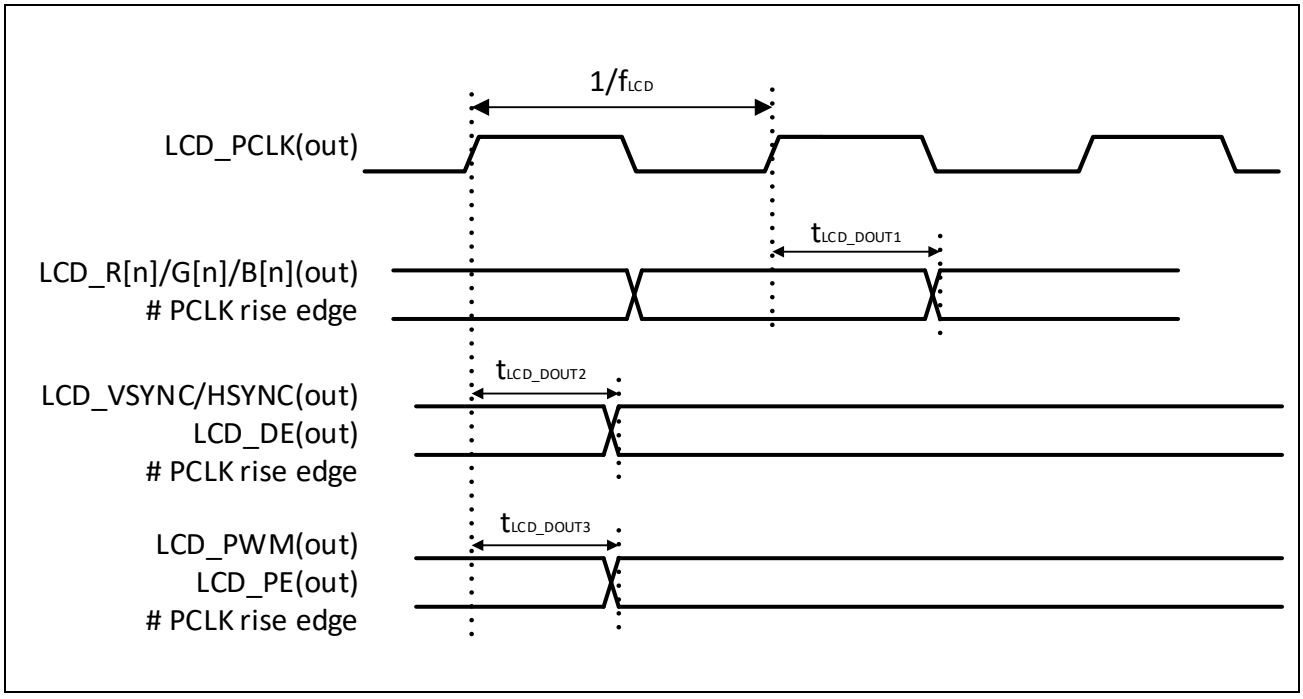


11.5.4 LCD Interface Timing

Table 11.23 LCD Interface Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LCD_PCLK frequency	f_{LCD}	—	—	—	83.3	MHz
LCD_R[n]/G[n]/B[n] output delay	t_{LCD_DOUT1}	LCD_PCLK rise or fall	1.5	—	8.5	ns
LCD_HSYNC/VSYNC LCD_DE output delay	t_{LCD_DOUT2}	LCD_PCLK rise or fall	1.5	—	8.5	ns
LCD_PE LCD_PWM output delay	t_{LCD_DOUT3}	LCD_PCLK rise or fall	0	—	20	ns

Note: n = 0..7, load capacitance $C_{L(max)}$ = 25 pF, drive strength 6 mA



11.5.5 MSEBI Interface Timing

Table 11.24 MSEBI master

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
MSEBIM_CLK frequency*1		f_{MSEBIM}	—	—	—	62.5	MHz
MSEBIM_WAIT_N[3:0] MSEBIM_ACD[31:0] Input	setup time	t_{MSEBIM_SETUP}	MSEBIM_CLK rise	14	—	—	ns
	hold time	t_{MSEBIM_HOLD}	MSEBIM_CLK rise	0	—	—	ns
MSEBIM_ACD[31:0] MSEBIM_ALE, MSEBIM_ALE1, MSEBIM_ALE2, MSEBIM_ALE3 MSEBIM_DLE MSEBIM_CLE MSEBIM_WR_N MSEBIM_RD_N output delay		t_{MSEBIM_DOUT}	MSEBIM_CLK rise	0	—	10	ns

Note: load capacitance $C_{L(max)}$ = 15 pF, drive strength 8 mA

Note 1. Maximum burst speed is 31.25 MHz.

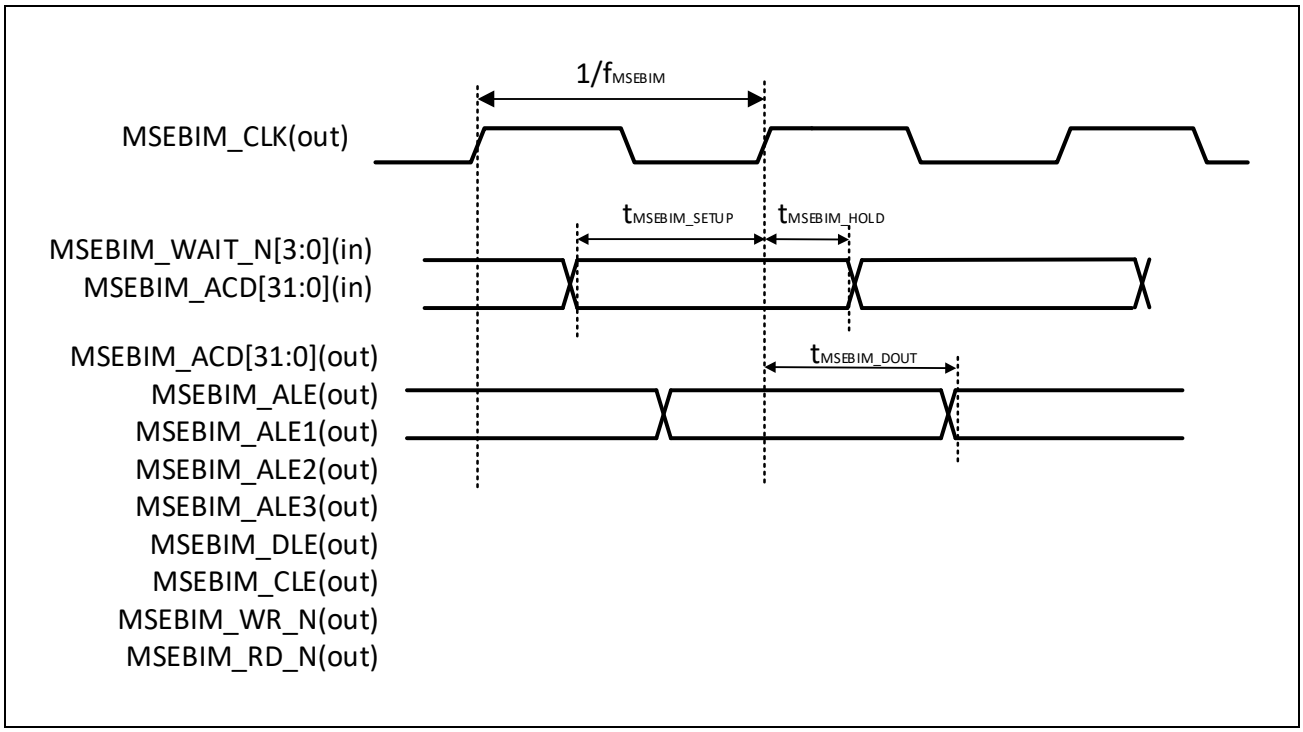
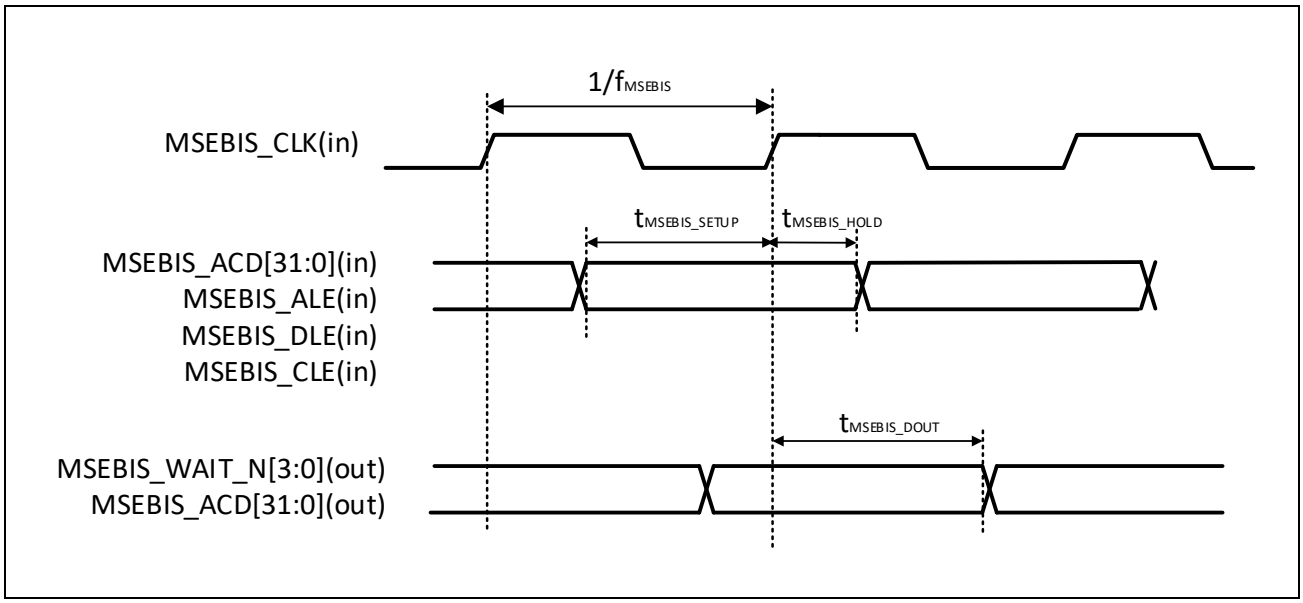


Table 11.25 MSEBI slave

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
MSEBIS_CLK frequency		f_{MSEBIS}	—	—	—	31.25	MHz
MSEBIS_WAIT_N[3:0] MSEBIS_ACD[31:0] output delay		t_{MSEBIS_DOUT}	MSEBIS_CLK rise	4	—	16	ns
MSEBIS_ACD[31:0] MSEBIS_ALE MSEBIS_DLE MSEBIS_CLE input	setup time	t_{MSEBIS_SETUP}	MSEBIS_CLK rise	14	—	—	ns
	hold time	t_{MSEBIS_HOLD}	MSEBIS_CLK rise	0	—	—	ns

Note: load capacitance $C_{L(max)}$ = 15 pF, drive strength 8 mA



11.6 ADC Characteristics

Condition: V_{ADC} = $V_{ADC\ REFP}$ = 3.3 ±0.3 V, $V_{ADC\ REFM}$ = 0 V, V_{DD11} = 1.15 ±0.05 V, Rs (source impedance) ≤ 300 Ω, T_A = +25°C

Table 11.26 ADC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution	RES	—	—	12	—	bit
Integral non linearity	INL	—	—	±1.0	±4.0	LSB
Differential non linearity	DNL	—	—	±0.3	±1.0	LSB
Zero scale error	ZSE	—	—	±2.0	±6.0	LSB
Full scale error	FSE	—	—	±0.5	±1.5	LSB
ADC input equivalent capacitance	C_{Ain}	—	—	—	8.0	pF
ADC sample/hold input equivalent capacitance	C_{ASHin}	—	—	—	6.0	pF

These errors don't include sampling error by external circuit. Furthermore, when $V_{ADC\ REFP} < V_{ADC}$ and $V_{ADC\ REFM} >$ 0.0 V, they become bigger.

11.7 RTC Oscillator Characteristics

Table 11.27 RTC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Oscillation frequency	$F_{OSC\ RTC}$	Load capacitance C_L = 7 pF	—	32.768	—	kHz
Output clock duty	$Duty_{RTC}$	Load capacitance C_L = 7 pF	40	—	60	%
Low voltage detect voltage*1	$L2H_{RTC}$	RTC_VDD33 Slew rate < 1 V/1msec	2.0	2.2	2.4	V
	$H2L_{RTC}$		1.8	2.0	2.2	V
Startup time	t_{START}	RTC_PWRGOOD = 1	—	1	—	sec

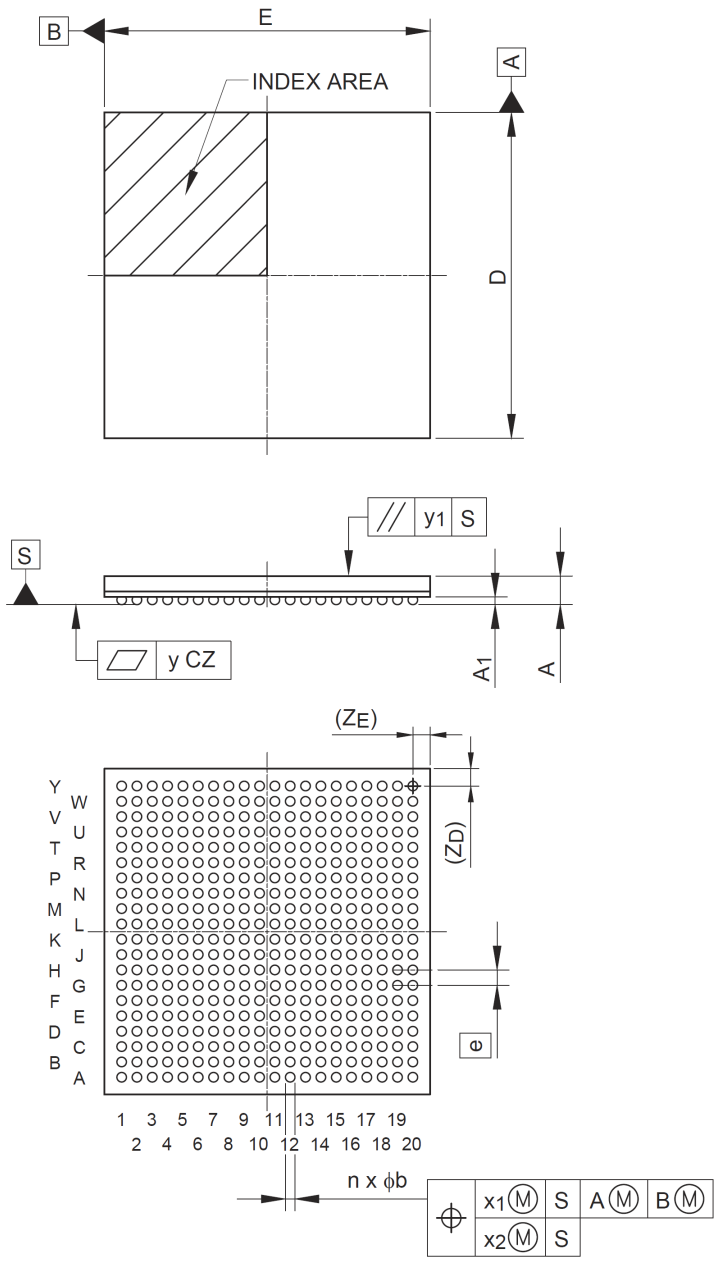
Note 1. Low Voltage Reset signal is asserted when RTC_VDD33 becomes $H2L_{RTC}$ and RTC circuit is reset.

Section 12 Mechanical Characteristics

12.1 Package Information

12.1.1 BGA-400 Package

JEITA Package Code	RENESAS Code	MASS (Typ) [g]
P-LFBGA400-17x17-0.80	PLBG0400GB-A	0.88

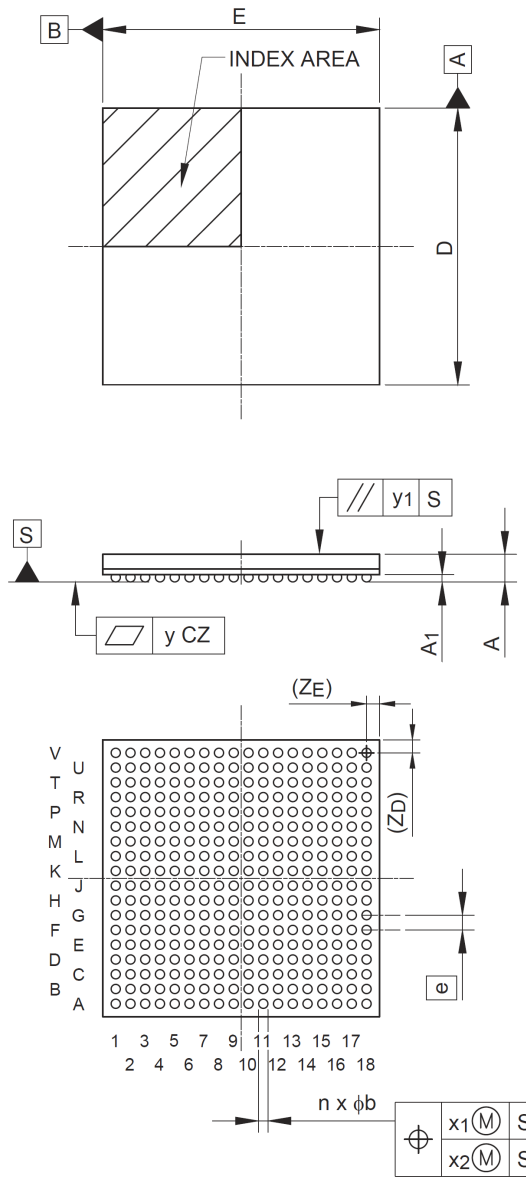


Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	16.90	17.00	17.10
E	16.90	17.00	17.10
A	—	—	1.70
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x_1	—	—	0.15
x_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
n	—	400	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure 12.1 BGA-400 Package Dimensions

12.1.2 BGA-324 Package

JEITA Package Code	RENESAS Code	MASS (Typ) [g]
P-LFBGA324-15x15-0.80	PLBG0324GA-A	0.70

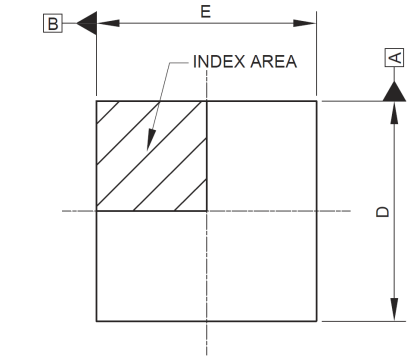


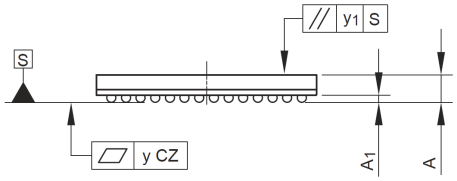
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	14.90	15.00	15.10
E	14.90	15.00	15.10
A	—	—	1.70
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x_1	—	—	0.15
x_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
n	—	324	—
Z_D	—	0.70	—
Z_E	—	0.70	—

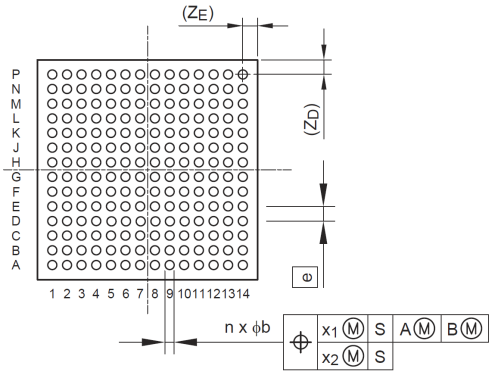
Figure 12.2 BGA-324 Package Dimensions

12.1.3 BGA-196 Package

JEITA Package Code	RENESAS Code	MASS (Typ) [g]
P-LFBGA196-12x12-0.80	PLBG0196GA-A	0.43







Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.92	12.0	12.08
E	11.92	12.0	12.08
A	—	—	1.70
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x_1	—	—	0.15
x_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
n	—	196	—
Z_D	—	0.80	—
Z_E	—	0.80	—

Figure 12.3 BGA-196 Package Dimensions

Appendix A Pin Assignment

Table A.1 Pin Assignment (1/7)

Classification	PKG Pin Name	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196
DDR2/3 interface	DDR_ADDR0	M5	K5	—	—	—
	DDR_ADDR1	T4	P4	—	—	—
	DDR_ADDR2	R2	N2	—	—	—
	DDR_ADDR3	P3	M3	—	—	—
	DDR_ADDR4	R3	N3	—	—	—
	DDR_ADDR5	P5	M4	—	—	—
	DDR_ADDR6	T1	P1	—	—	—
	DDR_ADDR7	R4	N4	—	—	—
	DDR_ADDR8	U1	R1	—	—	—
	DDR_ADDR9	T3	P3	—	—	—
	DDR_ADDR10	L3	J3	—	—	—
	DDR_ADDR11	T2	P2	—	—	—
	DDR_ADDR12	M4	K4	—	—	—
	DDR_ADDR13	U2	R2	—	—	—
	DDR_ADDR14	U3	R3	—	—	—
	DDR_ADDR15	N4	L3	—	—	—
	DDR_RAS	M3	K3	—	—	—
	DDR_CAS	N3	L2	—	—	—
	DDR_WE	M2	K2	—	—	—
	DDR_CS0	M1	K1	—	—	—
	DDR_CS1	L4	—	—	—	—
	DDR_BA0	P4	L4	—	—	—
	DDR_BA1	P1	M1	—	—	—
	DDR_BA2	P2	M2	—	—	—
	DDR_CLKEN	L2	J2	—	—	—
	DDR_ODT0	N2	L1	—	—	—
	DDR_ODT1	N1	—	—	—	—
	DDR_DM0	G3	E3	—	—	—
	DDR_DM1	F2	D2	—	—	—
	DDR_DQS0	F3	E4	—	—	—
	DDR_DQS_N0	G4	D3	—	—	—
	DDR_DQS1	F1	D1	—	—	—
	DDR_DQS_N1	G2	E2	—	—	—
	DDR_DQ0	F4	D4	—	—	—
	DDR_DQ1	H3	F4	—	—	—
	DDR_DQ2	E2	C2	—	—	—
	DDR_DQ3	J3	F3	—	—	—
	DDR_DQ4	E3	C3	—	—	—
	DDR_DQ5	J4	G3	—	—	—
	DDR_DQ6	F5	E5	—	—	—
	DDR_DQ7	H4	G4	—	—	—
	DDR_DQ8	D2	B1	—	—	—

Table A.1 Pin Assignment (2/7)

Classification	PKG Pin Name	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196
DDR2/3 interface	DDR_DQ9	H2	F2	—	—	—
	DDR_DQ10	D1	B2	—	—	—
	DDR_DQ11	H1	F1	—	—	—
	DDR_DQ12	C1	A2	—	—	—
	DDR_DQ13	J1	G1	—	—	—
	DDR_DQ14	C2	B3	—	—	—
	DDR_DQ15	J2	G2	—	—	—
	DDR_CLKN	K1	H1	—	—	—
	DDR_CLKP	K2	H2	—	—	—
	DDR_RESET_N	V3	T3	—	—	—
	DDR_VREF	K5	J5	—	—	—
	DDR_MZQ	K4	H4	—	—	—
USB interface	USB_DP1	Y10	V8	V10	P8	P8
	USB_DM1	W10	U8	U10	N8	N8
	USB_DP2	Y9	V7	V9	P7	P7
	USB_DM2	W9	U7	U9	N7	N7
	USB_RREF	R11	N9	R10	L8	L8
	USB_VBUS	U11	R9	T11	N9	N9
RTC	RTC_XO	A6	A5	A3	A3	—
	RTC_XI	A7	A6	A2	A2	—
	RTC_PWRGOOD	C7	D6	C4	B3	—
ADC	ADC1_VREFP	U6	R6	R7	M5	M5
	ADC1_VREFN	U5	T5	R8	M6	M6
	ADC1_IN0	W4	V4	T6	N4	N4
	ADC1_IN1	Y3	T4	U6	P2	P2
	ADC1_IN2	Y4	U4	T7	M4	M4
	ADC1_IN3	V4	V3	V6	P3	P3
	ADC1_IN4	V5	U5	V5	N3	N3
	ADC1_IN6	W5	T6	V7	P4	P4
	ADC1_IN7	Y5	V5	T8	P5	P5
	ADC1_IN8	V6	U6	U7	N5	N5
	ADC2_VREFP	U7	—	—	—	—
	ADC2_VREFN	T7	—	—	—	—
	ADC2_IN0	Y6	—	—	—	—
	ADC2_IN1	W6	—	—	—	—
	ADC2_IN2	W7	—	—	—	—
	ADC2_IN3	V7	—	—	—	—
	ADC2_IN4	Y7	—	—	—	—
	ADC2_IN6	U8	—	—	—	—
	ADC2_IN7	V8	—	—	—	—
	ADC2_IN8	W8	—	—	—	—
Clock	MCLK_XO	W2	U2	U12	N10	N10
	MCLK_XI	W1	U1	V12	P10	P10

Table A.1 Pin Assignment (3/7)

Classification	PKG Pin Name	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196
System control	MRESET_N	V11	T9	T12	M9	M9
	MRESET_OUT	W11	U9	U13	M10	M10
	THMODE	R7	M5	N3	K2	K2
OTP	ANF_VDD_PRG	E8	E8	B4	D4	—
Debugging interface	JTAG_TRST_N	T12	P10	R5	M1	M1
	JTAG_TCK	U13	T10	T4	M2	M2
	JTAG_TMS	V12	R10	U5	N2	N2
	JTAG_TDI	U12	R11	T5	N1	N1
	JTAG_TDO	T13	P11	R3	L1	L1
Operating mode control	CONFIG0	R6	P7	P3	L2	L2
	CONFIG1	P6	R4	P4	L3	L3
	CONFIG2	R5	P5	—	—	—
	TMC1	U4	N5	R4	M3	M3
	TMC2	P7	N6	R6	L4	L4
	CTRSTBYB	E9	D7	N4	K3	K3
GPIO	GPIO0	A12	—	L18	G13	G13
	GPIO1	C12	—	L17	G12	G12
	GPIO2	A13	—	M18	H13	H13
	GPIO3	C13	—	M17	H14	H14
	GPIO4	B13	—	L15	G11	G11
	GPIO5	A14	—	L16	H12	H12
	GPIO6	A15	—	N18	J13	J13
	GPIO7	D12	—	M16	J14	J14
	GPIO8	B15	—	N17	K14	K14
	GPIO9	B14	—	N16	J12	J12
	GPIO10	C14	—	N15	J11	J11
	GPIO11	D13	—	M15	H11	H11
	GPIO12	L20	—	G18	—	—
	GPIO13	L19	—	H16	—	—
	GPIO14	L16	—	H17	—	—
	GPIO15	M18	—	H15	—	—
	GPIO16	L17	—	J15	—	—
	GPIO17	M19	—	H18	—	—
	GPIO18	M20	—	J16	—	—
	GPIO19	L18	—	J17	—	—
	GPIO20	N20	—	J18	—	—
	GPIO21	M17	—	K17	—	—
	GPIO22	N18	—	K15	—	—
	GPIO23	M16	—	K16	—	—
	GPIO24	A16	A12	A8	—	—
	GPIO25	E13	C12	D9	—	—
	GPIO26	D14	D12	B8	—	—
	GPIO27	A17	B12	B9	—	—
	GPIO28	B16	B14	A9	—	—

Table A.1 Pin Assignment (4/7)

Classification	PKG Pin Name	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196
GPIO	GPIO29	C16	A13	C9	—	—
	GPIO30	A18	A15	D10	—	—
	GPIO31	C15	C14	C10	—	—
	GPIO32	B17	B13	A10	—	—
	GPIO33	D15	B15	C11	—	—
	GPIO34	C17	C13	B11	—	—
	GPIO35	E15	A14	B10	—	—
	GPIO36	D20	D18	A12	B7	B7
	GPIO37	E20	E16	B12	C7	C7
	GPIO38	E19	F15	A13	C8	C8
	GPIO39	F18	E17	B13	B8	B8
	GPIO40	G17	F16	D11	D7	D7
	GPIO41	F19	E18	C12	D8	D8
	GPIO42	F20	F18	D12	C9	C9
	GPIO43	H16	G15	A14	B9	B9
	GPIO44	G18	F17	C13	D9	D9
	GPIO45	G19	G16	B14	B10	B10
	GPIO46	H17	G18	C14	A8	A8
	GPIO47	H18	G17	D13	A9	A9
	GPIO48	G20	H18	D18	D14	D14
	GPIO49	J17	H15	F16	E13	E13
	GPIO50	J16	H16	D17	D13	D13
	GPIO51	H19	J18	E17	E14	E14
	GPIO52	J18	H17	E15	D12	D12
	GPIO53	H20	J17	E16	D11	D11
	GPIO54	J20	K18	F15	E12	E12
	GPIO55	K18	J15	E18	E11	E11
	GPIO56	J19	K17	G16	F13	F13
	GPIO57	K17	J16	F17	F14	F14
	GPIO58	K19	K16	G15	F12	F12
	GPIO59	K20	J14	F18	F11	F11
	GPIO60	Y12	V10	A5	A5	A5
	GPIO61	W12	U10	A6	A6	A6
	GPIO62	P20	K14	B15	C10	C10
	GPIO63	R20	L14	C15	A12	A12
	GPIO64	N19	L18	C16	A13	A13
	GPIO65	G16	F14	B16	B11	B11
	GPIO66	E18	D17	A16	A11	A11
	GPIO67	F17	E15	A17	B12	B12
	GPIO68	D19	D16	B17	B13	B13
	GPIO69	D17	B16	B18	C11	C11
	GPIO70	E17	D15	C17	B14	B14
	GPIO71	D18	E14	D16	C13	C13
	GPIO72	F16	C16	D15	C12	C12
	GPIO73	C18	C15	D14	D10	D10

Table A.1 Pin Assignment (5/7)

Classification	PKG Pin Name	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196
GPIO	GPIO74	C19	C17	D7	D5	D5
	GPIO75	B20	B18	C6	B5	B5
	GPIO76	B19	B17	C7	D6	D6
	GPIO77	C20	C18	C8	B6	B6
	GPIO78	A19	A17	B6	C5	C5
	GPIO79	B18	A16	B7	C6	C6
	GPIO80	W18	U16	V16	N12	N12
	GPIO81	Y18	V16	T16	N13	N13
	GPIO82	Y19	V17	U16	M12	M12
	GPIO83	Y17	V15	U14	P12	P12
	GPIO84	W20	U18	U18	M13	M13
	GPIO85	V19	T17	U17	L11	L11
	GPIO86	V20	T18	T18	L13	L13
	GPIO87	U19	R17	T17	N14	N14
	GPIO88	U20	R18	R18	K12	K12
	GPIO89	T19	P17	R17	M14	M14
	GPIO90	T20	P18	P17	K13	K13
	GPIO91	R19	N17	R16	L12	L12
	GPIO92	W17	U15	U15	M11	M11
	GPIO93	W19	U17	V17	P13	P13
	GPIO94	W16	U14	V14	N11	N11
	GPIO95	U18	P16	B1	D3	D3
	GPIO96	T18	M16	C1	C2	C2
	GPIO97	T17	N16	C2	C3	C3
	GPIO98	R17	M15	D2	B2	B2
	GPIO99	P17	M17	E1	B1	B1
	GPIO100	V18	T16	E2	E3	E3
	GPIO101	P16	M18	F1	C1	C1
	GPIO102	P18	K15	F2	D2	D2
	GPIO103	V17	T15	G1	F3	F3
	GPIO104	N17	L15	G2	E2	E2
	GPIO105	U17	N15	H2	F4	F4
	GPIO106	P19	L16	H3	E1	E1
	GPIO107	R18	N18	J1	G4	G4
	GPIO108	N16	L17	J2	F2	F2
	GPIO109	U16	M14	J3	F1	F1
	GPIO110	Y13	V11	K1	G2	G2
	GPIO111	V14	T11	K2	G3	G3
	GPIO112	W13	U11	K3	H4	H4
	GPIO113	Y14	V13	L2	H1	H1
	GPIO114	V13	V12	L3	H2	H2
	GPIO115	W14	V14	M1	H3	H3
	GPIO116	W15	U13	M2	J2	J2
	GPIO117	Y16	T12	N1	J3	J3
	GPIO118	V16	T13	P1	J1	J1

Table A.1 Pin Assignment (6/7)

Classification	PKG Pin Name	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196
GPIO	GPIO119	Y15	U12	B2	—	—
	GPIO120	T16	R16	B3	—	—
	GPIO121	V15	R12	C3	—	—
	GPIO122	U14	R13	D3	—	—
	GPIO123	T14	P13	D4	—	—
	GPIO124	R14	R14	E3	—	—
	GPIO125	T15	R15	E4	—	—
	GPIO126	U15	T14	F3	—	—
	GPIO127	R13	P12	F4	—	—
	GPIO128	E16	D14	G3	—	—
	GPIO129	D16	D13	G4	—	—
	GPIO130	E11	D11	H4	—	—
	GPIO131	B12	B11	J4	—	—
	GPIO132	D11	C11	K4	—	—
	GPIO133	C11	A11	D6	—	—
	GPIO134	E10	D10	L4	—	—
	GPIO135	B11	A10	M3	—	—
	GPIO136	B10	C10	M4	—	—
	GPIO137	A11	B10	N2	—	—
	GPIO138	C10	B9	P2	—	—
	GPIO139	A10	A9	R2	—	—
	GPIO140	D10	C8	T1	—	—
	GPIO141	A9	A8	U1	—	—
	GPIO142	C8	D9	T2	—	—
	GPIO143	B9	B8	U2	—	—
	GPIO144	D9	C7	V2	—	—
	GPIO145	A8	A7	T3	—	—
	GPIO146	B7	D8	U3	—	—
	GPIO147	C9	C9	V3	—	—
	GPIO148	D8	B6	U4	—	—
	GPIO149	B8	B7	C5	—	—
	GPIO150	E7	C6	T14	—	—
	GPIO151	B6	B5	T15	—	—
	GPIO152	D7	A4	R15	—	—
	GPIO153	C6	B4	P16	—	—
	GPIO154	D6	C5	P15	—	—
	GPIO155	A5	A3	P14	—	—
	GPIO156	B4	—	P13	—	—
	GPIO157	B5	—	R14	—	—
	GPIO158	E6	—	R13	—	—
	GPIO159	C5	—	T13	—	—
	GPIO160	A4	—	—	—	—
	GPIO161	A3	—	—	—	—
	GPIO162	E5	—	—	—	—
	GPIO163	D5	—	—	—	—

Table A.1 Pin Assignment (7/7)

Classification	PKG Pin Name	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196
GPIO	GPIO164	A2	—	—	—	—
	GPIO165	D4	—	—	—	—
	GPIO166	C3	—	—	—	—
	GPIO167	C4	—	—	—	—
	GPIO168	B2	—	—	—	—
	GPIO169	B3	—	—	—	—

Table A.2 Pin Assignment (Power Supply) (1/2)

Classification	PKG Pin Name	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196
Power supply	VDD11	G13, J13, K13, M13, G12, N12, N10, H9, N9, H8, J8, M8	G12, K12, M12, M11, F10, L8, F7, L7, G6	G12, H12, J12, K12, L12, M12, G11, M11, G10, M10, G9, M9, G8, M8, G7, H7, J7, K7, L7, M7	L10, E9, G9, J9, F7, J7, E5, G5, H5, K5	L10, E9, G9, J9, F7, J7, E5, G5, H5, K5
	VDD11_CA7	R16, R15	P15, P14	—	—	—
	GND	A20, Y20, K16, F15, G15, H15, L15, M15, P15, K14, P14, F13, H13, L13, N13, F12, H12, J12, K12, L12, M12, R12, G11, H11, J11, K11, L11, M11, N11, F10, H10, J10, K10, L10, M10, J9, K9, L9, M9, P9, G8, N8, F7, J7, F6, H6, N6, G5, H5, J5, L5, N5, E4, D3, K3, W3, V2, Y2, A1, B1, E1, G1, L1, R1, V1, Y1	A18, V18, H14, N14, F13, M13, N13, F12, H12, J12, L12, G11, H11, J11, K11, L11, E10, G10, H10, J10, K10, L10, N10, G9, H9, J9, K9, L9, G8, H8, G7, M7, E6, D5, F5, G5, H5, L5, C4, J4, H3, U3, T2, V2, A1, C1, E1, J1, N1, T1, V1	A18, C18, K18, P18, V18, G17, A15, V15, E13, F13, G13, H13, J13, K13, L13, M13, V13, F12, N12, P12, R12, A11, F11, H11, J11, K11, L11, P11, R11, F10, H10, J10, K10, L10, F9, H9, J9, K9, L9, D8, E8, H8, J8, K8, L8, N8, A7, E7, N7, E6, G6, H6, J6, K6, L6, M6, N6, E5, F5, K5, L5, M5, A4, V4, A1, D1, H1, L1, R1, V1	A14, C14, G14, L14, P14, P11, A10, K10, F9, H9, F8, G8, H8, J8, A7, G7, H7, F6, G6, H6, J6, K6, F5, J5, A4, A1, D1, G1, K1, P1	A14, C14, G14, L14, P14, P11, A10, K10, F9, H9, F8, G8, H8, J8, A7, G7, H7, F6, G6, H6, J6, K6, F5, J5, A4, A1, D1, G1, K1, P1, A2, D4
	VDD33	N15, G14, N14, P13, P12, G10, G9, P8, G7, N7, G6, F9	E13, K13, L13, N12, F11, N11, F9, F8, N7, F6, M6, E9	E14, F14, N14, N13, N9, F8, F7, F6, P6, G5, H5, J5, N5, P5, B5	K11, E10, E6, E4, J4, K4, C4	K11, E10, E6, E4, J4, K4, B3, B4, C4
	RGMII1_VDDQ	E12, F11	—	L14, M14	H10, J10	H10, J10
	RGMII2_VDDQ	L14, M14	—	J14, K14	—	—
	RGMII3_VDDQ	E14, F14	E12, E11	E10, E9	—	—
	RGMII4_VDDQ	H14, J14	G14, G13	E12, E11	E8, E7	E8, E7
	RGMII5_VDDQ	J15, K15	H13, J13	G14, H14	F10, G10	F10, G10
PLL Power supply	PLL_AVDD	—	—	N11	K9	K9
	PLL_AGND	—	—	N10	L9	L9
USB Power supply	USB_VD33	R9, T9	M8, N8	P9, R9	K7, L7	K7, L7
	USB_GND	Y11, R10, T10, U10, V10, U9, V9, Y8	V9, P8, R8, T8, R7, T7, V6	U11, V11, T10, T9, U8, V8	P9, M8, M7, N6, P6	P9, M8, M7, N6, P6
	USB_AVDD	T11	P9	P10	K8	K8
	USB_AVSS	P11, P10	M10, M9	—	—	—
RTC Power supply	RTC_VDD33	F8	E7	D5	B4	—

Table A.2 Pin Assignment (Power Supply) (2/2)

Classification	PKG Pin Name	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196
ADC Power supply	ADC1_AVDD	T6	P6	P8	L6	L6
	ADC1_AGND	T5	R5	P7	L5	L5
	ADC2_AVDD	T8	—	—	—	—
	ADC2_AGND	R8	—	—	—	—
DDR PHY Power supply	DVDD	L8, L7	K8, K7	—	—	—
	DVDDQ	H7, M7, J6, K6, L6, M6	H7, H6, J6, K6, L6	—	—	—
	DVSS	K8, K7	J8, J7	—	—	—

Appendix B IO Multiplexing Assignment

The following table shows some of the IO Multiplexing assignment. Please check with the dedicated assignment software for function not listed.

Table B.1 IO Multiplexing Assignment (1/4)

	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196	Level1 Func2	Level1 Func3	Level1 Func4	Level1 Func5	Level1 Func6	Level1 Func8	Level1 Func9	Level2 Func48
GPIO0	✓	—	✓	✓	✓	GMII1_TXCLK							BGPIO1A[0]
GPIO1	✓	—	✓	✓	✓	GMII1_TXD0							BGPIO1B[0]
GPIO2	✓	—	✓	✓	✓	GMII1_TXD1							BGPIO1B[1]
GPIO3	✓	—	✓	✓	✓	GMII1_TXD2							BGPIO1A[1]
GPIO4	✓	—	✓	✓	✓	GMII1_TXD3							BGPIO1A[2]
GPIO5	✓	—	✓	✓	✓	GMII1_TXEN							BGPIO1B[2]
GPIO6	✓	—	✓	✓	✓	GMII1_RXCLK							BGPIO1B[3]
GPIO7	✓	—	✓	✓	✓	GMII1_RXD0							BGPIO1B[4]
GPIO8	✓	—	✓	✓	✓	GMII1_RXD1							BGPIO1B[5]
GPIO9	✓	—	✓	✓	✓	GMII1_RXD2							BGPIO1A[3]
GPIO10	✓	—	✓	✓	✓	GMII1_RXD3							BGPIO1A[4]
GPIO11	✓	—	✓	✓	✓	GMII1_RXDV							BGPIO1B[6]
GPIO12	✓	—	✓	—	—	GMII2_TXCLK							BGPIO1A[5]
GPIO13	✓	—	✓	—	—	GMII2_TXD0							BGPIO1B[7]
GPIO14	✓	—	✓	—	—	GMII2_TXD1							BGPIO1B[8]
GPIO15	✓	—	✓	—	—	GMII2_TXD2							BGPIO1A[6]
GPIO16	✓	—	✓	—	—	GMII2_TXD3							BGPIO1A[7]
GPIO17	✓	—	✓	—	—	GMII2_TXEN							BGPIO1B[9]
GPIO18	✓	—	✓	—	—	GMII2_RXCLK							BGPIO1B[10]
GPIO19	✓	—	✓	—	—	GMII2_RXD0							BGPIO1B[11]
GPIO20	✓	—	✓	—	—	GMII2_RXD1							BGPIO1B[12]
GPIO21	✓	—	✓	—	—	GMII2_RXD2							BGPIO1A[8]
GPIO22	✓	—	✓	—	—	GMII2_RXD3							BGPIO1A[9]
GPIO23	✓	—	✓	—	—	GMII2_RXDV							BGPIO1B[13]
GPIO24	✓	✓	✓	—	—	GMII3_TXCLK							BGPIO1A[10]
GPIO25	✓	✓	✓	—	—	GMII3_TXD0							BGPIO1B[14]
GPIO26	✓	✓	✓	—	—	GMII3_TXD1							BGPIO1B[15]
GPIO27	✓	✓	✓	—	—	GMII3_TXD2							BGPIO1A[11]
GPIO28	✓	✓	✓	—	—	GMII3_TXD3							BGPIO1A[12]
GPIO29	✓	✓	✓	—	—	GMII3_TXEN							BGPIO1B[16]
GPIO30	✓	✓	✓	—	—	GMII3_RXCLK							BGPIO1B[17]
GPIO31	✓	✓	✓	—	—	GMII3_RXD0							BGPIO1B[18]
GPIO32	✓	✓	✓	—	—	GMII3_RXD1							BGPIO1B[19]
GPIO33	✓	✓	✓	—	—	GMII3_RXD2							BGPIO1A[13]
GPIO34	✓	✓	✓	—	—	GMII3_RXD3							BGPIO1A[14]
GPIO35	✓	✓	✓	—	—	GMII3_RXDV							BGPIO1B[20]
GPIO36	✓	✓	✓	✓	✓	GMII4_TXCLK							BGPIO1A[15]
GPIO37	✓	✓	✓	✓	✓	GMII4_TXD0							BGPIO1B[21]
GPIO38	✓	✓	✓	✓	✓	GMII4_TXD1							BGPIO1B[22]
GPIO39	✓	✓	✓	✓	✓	GMII4_TXD2							BGPIO1A[16]
GPIO40	✓	✓	✓	✓	✓	GMII4_TXD3							BGPIO1A[17]
GPIO41	✓	✓	✓	✓	✓	GMII4_TXEN							BGPIO1B[23]
GPIO42	✓	✓	✓	✓	✓	GMII4_RXCLK							BGPIO1B[24]
GPIO43	✓	✓	✓	✓	✓	GMII4_RXD0							BGPIO1B[25]
GPIO44	✓	✓	✓	✓	✓	GMII4_RXD1							BGPIO1B[26]
GPIO45	✓	✓	✓	✓	✓	GMII4_RXD2							BGPIO1A[18]

Table B.1 IO Multiplexing Assignment (2/4)

	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196	Level1 Func2	Level1 Func3	Level1 Func4	Level1 Func5	Level1 Func6	Level1 Func8	Level1 Func9	Level2 Func48
GPIO46	✓	✓	✓	✓	✓	GMII4_RXD3							BGPIO1A[19]
GPIO47	✓	✓	✓	✓	✓	GMII4_RXDV							BGPIO1B[27]
GPIO48	✓	✓	✓	✓	✓	GMII5_TXCLK							BGPIO1A[20]
GPIO49	✓	✓	✓	✓	✓	GMII5_TXD0							BGPIO1B[28]
GPIO50	✓	✓	✓	✓	✓	GMII5_TXD1							BGPIO1B[29]
GPIO51	✓	✓	✓	✓	✓	GMII5_TXD2							BGPIO1A[21]
GPIO52	✓	✓	✓	✓	✓	GMII5_TXD3							BGPIO1A[22]
GPIO53	✓	✓	✓	✓	✓	GMII5_TXEN							BGPIO1B[30]
GPIO54	✓	✓	✓	✓	✓	GMII5_RXCLK							BGPIO1B[31]
GPIO55	✓	✓	✓	✓	✓	GMII5_RXD0							BGPIO2B[0]
GPIO56	✓	✓	✓	✓	✓	GMII5_RXD1							BGPIO2B[1]
GPIO57	✓	✓	✓	✓	✓	GMII5_RXD2							BGPIO1A[23]
GPIO58	✓	✓	✓	✓	✓	GMII5_RXD3							BGPIO1A[24]
GPIO59	✓	✓	✓	✓	✓	GMII5_RXDV							BGPIO2B[2]
GPIO60	✓	✓	✓	✓	✓	RGMII_REFCLK	MII_REFCLK_0						BGPIO2B[3]
GPIO61	✓	✓	✓	✓	✓	RMII_REFCLK	MII_REFCLK_1						BGPIO2B[4]
GPIO62	✓	✓	✓	✓	✓	GMII3_TXER	FNAND_CE_N2			LCD_R1			BGPIO1A[25]
GPIO63	✓	✓	✓	✓	✓	GMII3_RXER	FNAND_WP_N2			LCD_G1			BGPIO1A[26]
GPIO64	✓	✓	✓	✓	✓	GMII3_CRS	FNAND_RY/BY_N2			LCD_B1			BGPIO1A[27]
GPIO65	✓	✓	✓	✓	✓	GMII3_COL	FNAND_CE_N3			LCD_R2			BGPIO1A[28]
GPIO66	✓	✓	✓	✓	✓	GMII4_TXER	FNAND_WP_N3			LCD_G2			BGPIO1A[29]
GPIO67	✓	✓	✓	✓	✓	GMII4_RXER	FNAND_RY/BY_N3			LCD_B2			BGPIO1A[30]
GPIO68	✓	✓	✓	✓	✓	GMII4_CRS				LCD_R3			BGPIO1A[31]
GPIO69	✓	✓	✓	✓	✓	GMII4_COL	FNAND_CE_N1			LCD_G3			BGPIO2A[0]
GPIO70	✓	✓	✓	✓	✓	GMII5_TXER	FNAND_WP_N1			LCD_B3			BGPIO2A[1]
GPIO71	✓	✓	✓	✓	✓	GMII5_RXER	FNAND_RY/BY_N1			LCD_R4			BGPIO2A[2]
GPIO72	✓	✓	✓	✓	✓	GMII5_CRS				LCD_G4			BGPIO2A[3]
GPIO73	✓	✓	✓	✓	✓	GMII5_COL		QUAD1_CS_N1		LCD_B4			BGPIO2A[4]
GPIO74	✓	✓	✓	✓	✓			QUAD1_CS_N0					BGPIO2B[5]
GPIO75	✓	✓	✓	✓	✓			QUAD1_IO3					BGPIO2B[6]
GPIO76	✓	✓	✓	✓	✓			QUAD1_IO2					BGPIO2B[7]
GPIO77	✓	✓	✓	✓	✓			QUAD1_IO1					BGPIO2B[8]
GPIO78	✓	✓	✓	✓	✓			QUAD1_IO0					BGPIO2B[9]
GPIO79	✓	✓	✓	✓	✓			QUAD1_CLK					BGPIO2B[10]
GPIO80	✓	✓	✓	✓	✓		FNAND_ALE						BGPIO2B[11]
GPIO81	✓	✓	✓	✓	✓		FNAND_CLE						BGPIO2B[12]
GPIO82	✓	✓	✓	✓	✓		FNAND_WE_N						BGPIO2B[13]
GPIO83	✓	✓	✓	✓	✓		FNAND_RE_N						BGPIO2B[14]
GPIO84	✓	✓	✓	✓	✓		FNAND_IO0						BGPIO2B[15]
GPIO85	✓	✓	✓	✓	✓		FNAND_IO1						BGPIO2B[16]
GPIO86	✓	✓	✓	✓	✓		FNAND_IO2						BGPIO2B[17]
GPIO87	✓	✓	✓	✓	✓		FNAND_IO3						BGPIO2B[18]
GPIO88	✓	✓	✓	✓	✓		FNAND_IO4						BGPIO2B[19]
GPIO89	✓	✓	✓	✓	✓		FNAND_IO5						BGPIO2B[20]
GPIO90	✓	✓	✓	✓	✓		FNAND_IO6						BGPIO2B[21]
GPIO91	✓	✓	✓	✓	✓		FNAND_IO7						BGPIO2B[22]
GPIO92	✓	✓	✓	✓	✓		FNAND_CE_N0						BGPIO2B[23]
GPIO93	✓	✓	✓	✓	✓		FNAND_WP_N0						BGPIO2B[24]
GPIO94	✓	✓	✓	✓	✓		FNAND_RY/BY_N0						BGPIO2B[25]
GPIO95	✓	✓	✓	✓	✓				SDIO1_CMD				BGPIO2A[5]
GPIO96	✓	✓	✓	✓	✓				SDIO1_CLK				BGPIO2A[6]

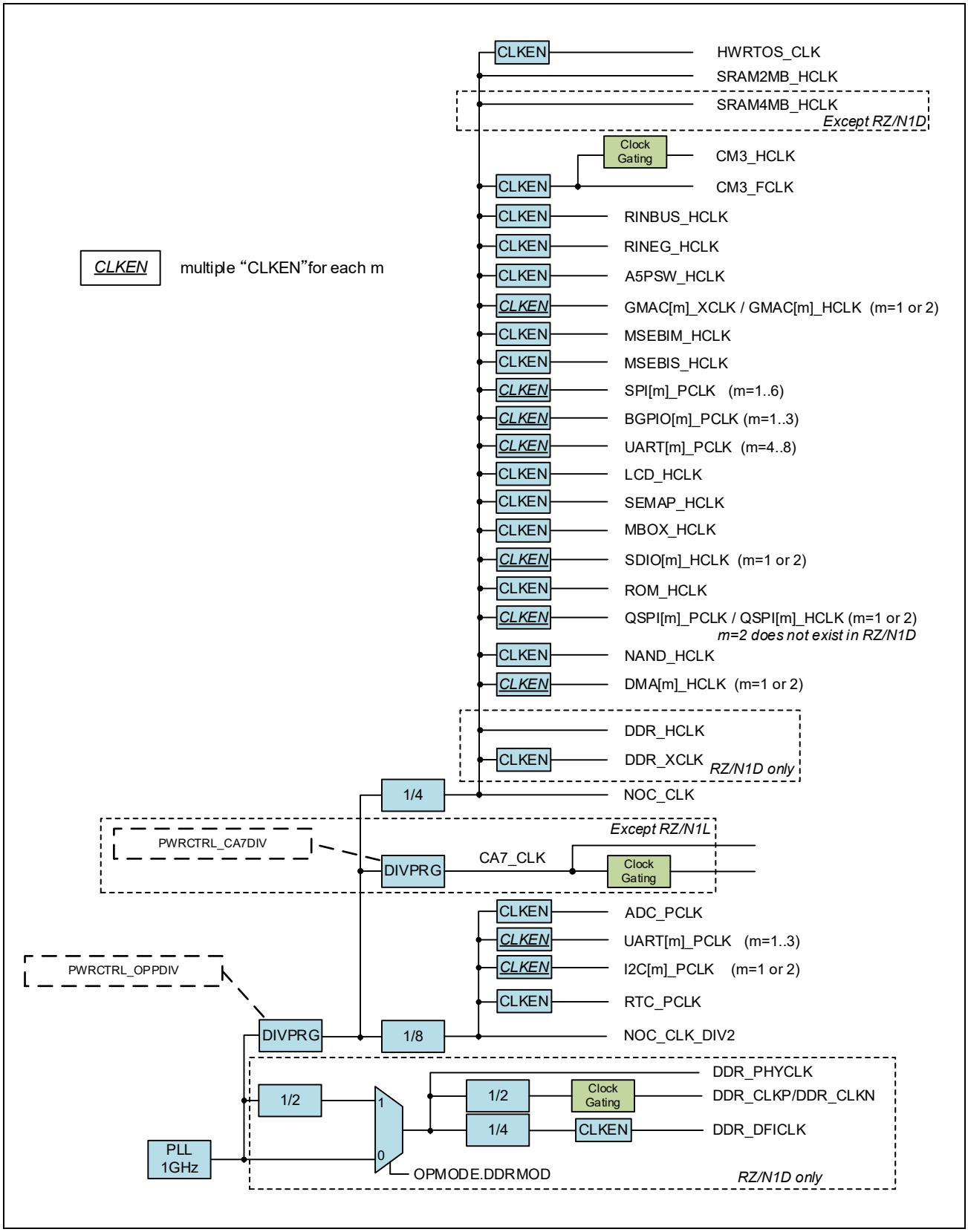
Table B.1 IO Multiplexing Assignment (3/4)

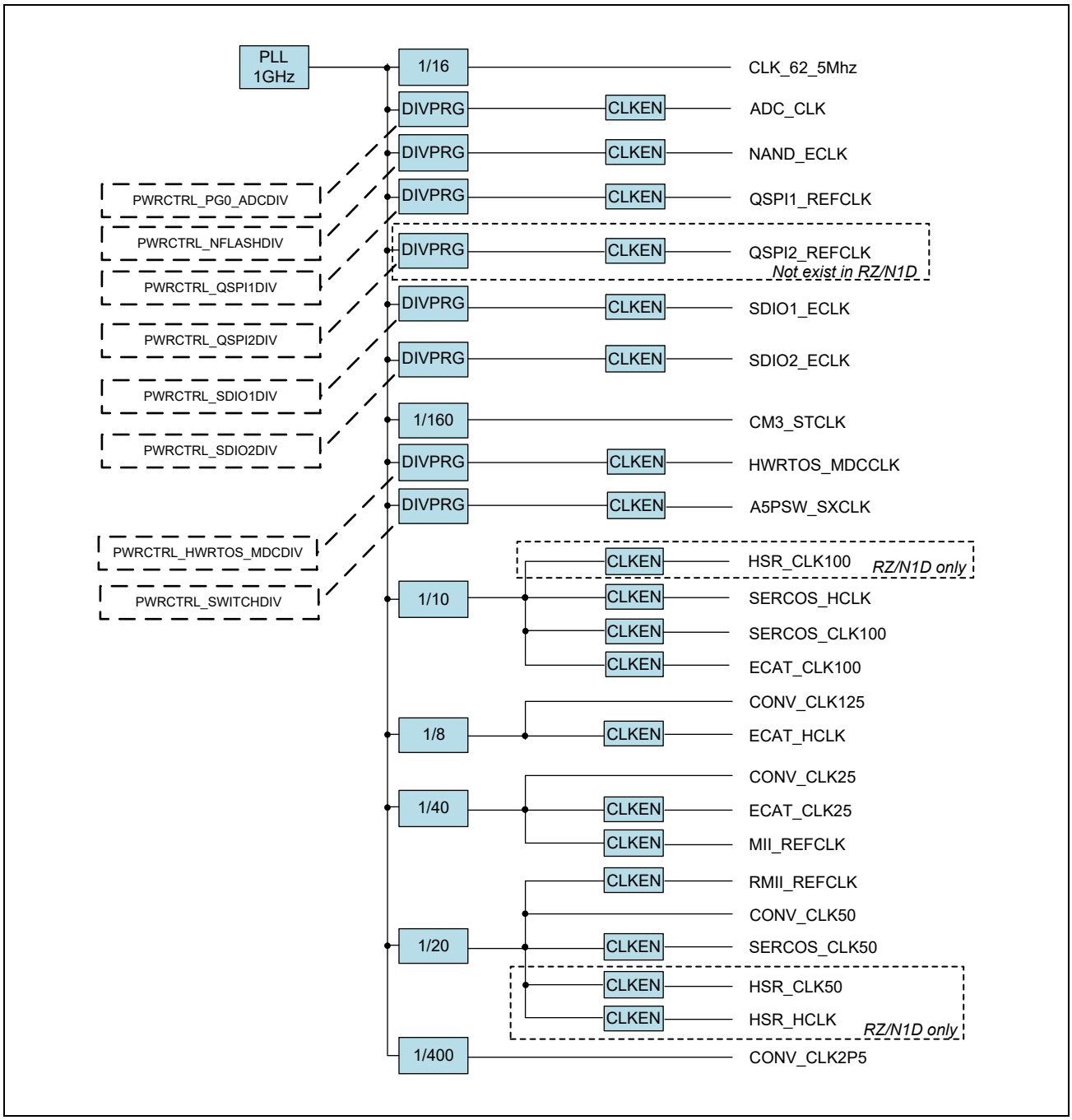
	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196	Level1 Func2	Level1 Func3	Level1 Func4	Level1 Func5	Level1 Func6	Level1 Func8	Level1 Func9	Level2 Func48
GPIO97	✓	✓	✓	✓	✓				SDIO1_IO0				BGPIO2A[7]
GPIO98	✓	✓	✓	✓	✓				SDIO1_IO1				BGPIO2A[8]
GPIO99	✓	✓	✓	✓	✓				SDIO1_IO2				BGPIO2A[9]
GPIO100	✓	✓	✓	✓	✓				SDIO1_IO3				BGPIO2A[10]
GPIO101	✓	✓	✓	✓	✓				SDIO1_IO4		MSEBIM_ALE2		BGPIO2A[11]
GPIO102	✓	✓	✓	✓	✓				SDIO1_IO5		MSEBIM_ALE3		BGPIO2A[12]
GPIO103	✓	✓	✓	✓	✓				SDIO1_IO6				BGPIO2A[13]
GPIO104	✓	✓	✓	✓	✓				SDIO1_IO7				BGPIO2A[14]
GPIO105	✓	✓	✓	✓	✓				SDIO2_CMD		MSEBIM_ACD0	MSEBIS_ACD0	BGPIO2A[15]
GPIO106	✓	✓	✓	✓	✓				SDIO2_CLK		MSEBIM_ACD1	MSEBIS_ACD1	BGPIO2A[16]
GPIO107	✓	✓	✓	✓	✓				SDIO2_IO0		MSEBIM_ACD2	MSEBIS_ACD2	BGPIO2A[17]
GPIO108	✓	✓	✓	✓	✓				SDIO2_IO1		MSEBIM_ACD3	MSEBIS_ACD3	BGPIO2A[18]
GPIO109	✓	✓	✓	✓	✓				SDIO2_IO2		MSEBIM_ALE	MSEBIS_ACD4	BGPIO2A[19]
GPIO110	✓	✓	✓	✓	✓				SDIO2_IO3		MSEBIM_CLK	MSEBIS_ACD5	BGPIO2A[20]
GPIO111	✓	✓	✓	✓	✓				SDIO2_IO4		MSEBIM_CLE	MSEBIS_ACD6	BGPIO2A[21]
GPIO112	✓	✓	✓	✓	✓	MII_REFCLK_2			SDIO2_IO5		MSEBIM_DLE	MSEBIS_ACD7	BGPIO2A[22]
GPIO113	✓	✓	✓	✓	✓				SDIO2_IO6		MSEBIM_ACD4	MSEBIS_ALE	BGPIO2A[23]
GPIO114	✓	✓	✓	✓	✓				SDIO2_IO7		MSEBIM_ACD5	MSEBIS_CLK	BGPIO2A[24]
GPIO115	✓	✓	✓	✓	✓						MSEBIM_ACD6	MSEBIS_CLE	BGPIO2A[25]
GPIO116	✓	✓	✓	✓	✓						MSEBIM_ACD7	MSEBIS_DLE	BGPIO2A[26]
GPIO117	✓	✓	✓	✓	✓						MSEBIM_WAIT_N0	MSEBIS_WAIT_N0	BGPIO2A[27]
GPIO118	✓	✓	✓	✓	✓						MSEBIM_WAIT_N1	MSEBIS_WAIT_N1	BGPIO2A[28]
GPIO119	✓	✓	✓	—	—								BGPIO2A[29]
GPIO120	✓	✓	✓	—	—								BGPIO2A[30]
GPIO121	✓	✓	✓	—	—								BGPIO2A[31]
GPIO122	✓	✓	✓	—	—								BGPIO3A[0]
GPIO123	✓	✓	✓	—	—								BGPIO3A[1]
GPIO124	✓	✓	✓	—	—								BGPIO3A[2]
GPIO125	✓	✓	✓	—	—								BGPIO3A[3]
GPIO126	✓	✓	✓	—	—	MII_REFCLK_3							BGPIO3A[4]
GPIO127	✓	✓	✓	—	—					LCD_PWM0			BGPIO3A[5]
GPIO128	✓	✓	✓	—	—					LCD_PCLK			BGPIO3A[6]
GPIO129	✓	✓	✓	—	—					LCD_HSYNC			BGPIO3A[7]
GPIO130	✓	✓	✓	—	—					LCD_VSYNC			BGPIO3A[8]
GPIO131	✓	✓	✓	—	—					LCD_DE			BGPIO3A[9]
GPIO132	✓	✓	✓	—	—					LCD_PE			BGPIO3A[10]
GPIO133	✓	✓	✓	—	—					LCD_PWM1	MSEBIM_ALE1		BGPIO3A[11]
GPIO134	✓	✓	✓	—	—	MII_REFCLK_4				LCD_R5	MSEBIM_WAIT_N2	MSEBIS_WAIT_N2	BGPIO3A[12]
GPIO135	✓	✓	✓	—	—					LCD_R0	MSEBIM_WAIT_N3	MSEBIS_WAIT_N3	BGPIO3A[13]
GPIO136	✓	✓	✓	—	—					LCD_G0	MSEBIM_ACD8	MSEBIS_ACD8	BGPIO3A[14]
GPIO137	✓	✓	✓	—	—					LCD_B0	MSEBIM_ACD9	MSEBIS_ACD9	BGPIO3A[15]
GPIO138	✓	✓	✓	—	—					LCD_R6	MSEBIM_ACD10	MSEBIS_ACD10	BGPIO3A[16]
GPIO139	✓	✓	✓	—	—					LCD_G6	MSEBIM_ACD11	MSEBIS_ACD11	BGPIO3A[17]
GPIO140	✓	✓	✓	—	—					LCD_B6	MSEBIM_ACD12	MSEBIS_ACD12	BGPIO3A[18]
GPIO141	✓	✓	✓	—	—					LCD_R7	MSEBIM_ACD13	MSEBIS_ACD13	BGPIO3A[19]
GPIO142	✓	✓	✓	—	—					LCD_G7	MSEBIM_ACD14	MSEBIS_ACD14	BGPIO3A[20]
GPIO143	✓	✓	✓	—	—					LCD_B7	MSEBIM_ACD15	MSEBIS_ACD15	BGPIO3A[21]
GPIO144	✓	✓	✓	—	—					LCD_G5	MSEBIM_ACD16	MSEBIS_ACD16	BGPIO3A[22]
GPIO145	✓	✓	✓	—	—	MII_REFCLK_5				LCD_B5	MSEBIM_ACD17	MSEBIS_ACD17	BGPIO3A[23]
GPIO146	✓	✓	✓	—	—						MSEBIM_ACD18	MSEBIS_ACD18	BGPIO3A[24]
GPIO147	✓	✓	✓	—	—						MSEBIM_ACD19	MSEBIS_ACD19	BGPIO3A[25]

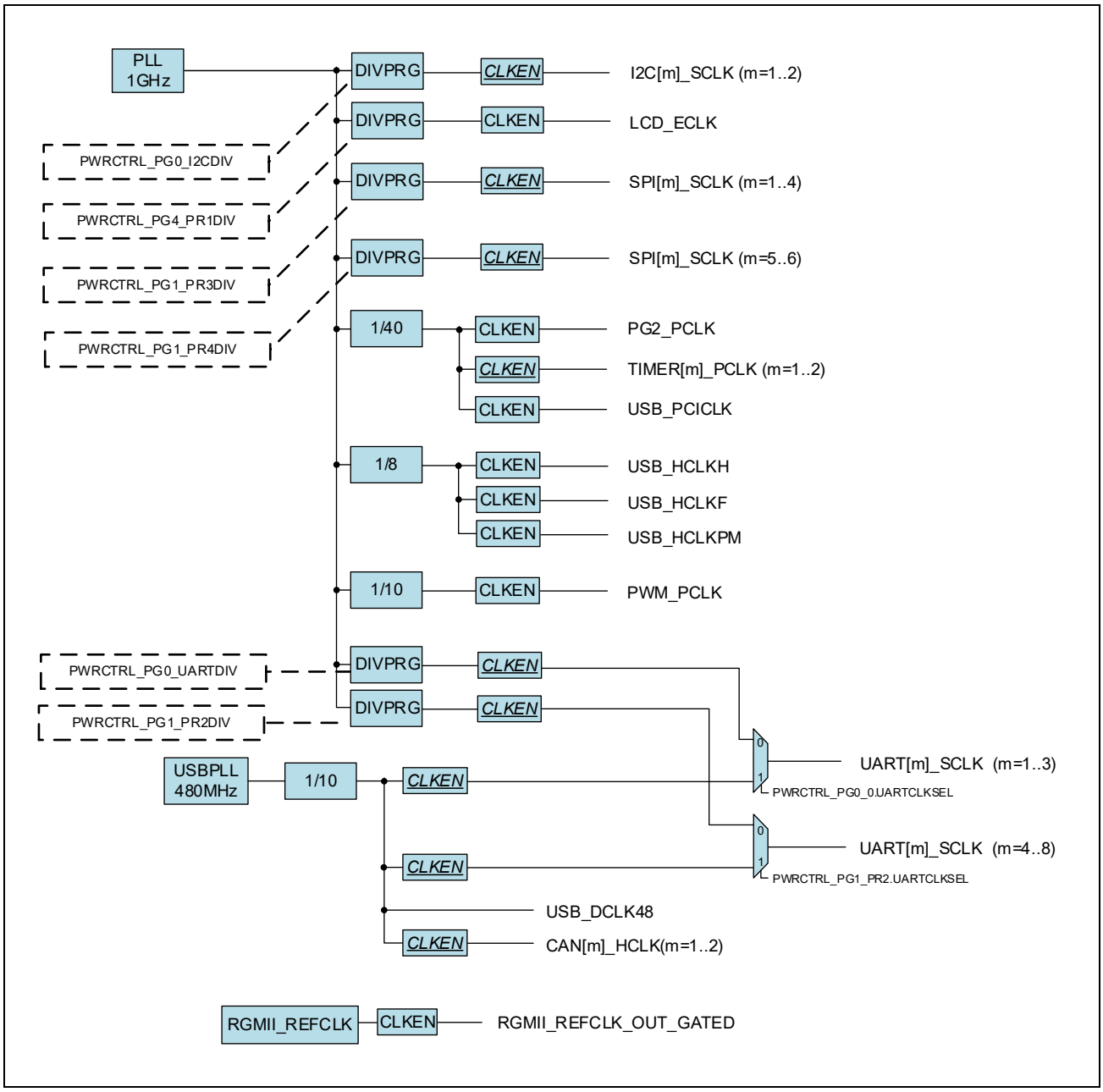
Table B.1 IO Multiplexing Assignment (4/4)

	N1D 400	N1D 324	N1S 324	N1S 196	N1L 196	Level1 Func2	Level1 Func3	Level1 Func4	Level1 Func5	Level1 Func6	Level1 Func8	Level1 Func9	Level2 Func48
GPIO148	✓	✓	✓	—	—						MSEBIM_ACD20	MSEBIS_ACD20	BGPIO3A[26]
GPIO149	✓	✓	✓	—	—			QUAD1_CS_N2			MSEBIM_ACD21	MSEBIS_ACD21	BGPIO3A[27]
GPIO150	✓	✓	✓	—	—			QUAD1_CS_N3			MSEBIM_ACD22	MSEBIS_ACD22	BGPIO2B[26]
GPIO151	✓	✓	✓	—	—			QUAD2_CS_N3			MSEBIM_ACD23	MSEBIS_ACD23	BGPIO2B[27]
GPIO152	✓	✓	✓	—	—	GMII1_TXER		QUAD2_CS_N2			MSEBIM_ACD24	MSEBIS_ACD24	BGPIO2B[28]
GPIO153	✓	✓	✓	—	—	GMII1_RXER		QUAD2_CS_N1			MSEBIM_ACD25	MSEBIS_ACD25	BGPIO2B[29]
GPIO154	✓	✓	✓	—	—	GMII1_CRS		QUAD2_CS_N0			MSEBIM_ACD26	MSEBIS_ACD26	BGPIO2B[30]
GPIO155	✓	✓	✓	—	—	GMII1_COL		QUAD2_IO3			MSEBIM_ACD27	MSEBIS_ACD27	BGPIO2B[31]
GPIO156	✓	—	✓	—	—	GMII2_TXER		QUAD2_IO2			MSEBIM_ACD28	MSEBIS_ACD28	BGPIO3A[28]
GPIO157	✓	—	✓	—	—	GMII2_RXER		QUAD2_IO1			MSEBIM_ACD29	MSEBIS_ACD29	BGPIO3A[29]
GPIO158	✓	—	✓	—	—	GMII2_CRS		QUAD2_IO0			MSEBIM_ACD30	MSEBIS_ACD30	BGPIO3A[30]
GPIO159	✓	—	✓	—	—	GMII2_COL		QUAD2_CLK			MSEBIM_ACD31	MSEBIS_ACD31	BGPIO3A[31]
GPIO160	✓	—	—	—	—								BGPIO3B[0]
GPIO161	✓	—	—	—	—								BGPIO3B[1]
GPIO162	✓	—	—	—	—								BGPIO3B[2]
GPIO163	✓	—	—	—	—								BGPIO3B[3]
GPIO164	✓	—	—	—	—								BGPIO3B[4]
GPIO165	✓	—	—	—	—								BGPIO3B[5]
GPIO166	✓	—	—	—	—								BGPIO3B[6]
GPIO167	✓	—	—	—	—								BGPIO3B[7]
GPIO168	✓	—	—	—	—								BGPIO3B[8]
GPIO169	✓	—	—	—	—								BGPIO3B[9]

Appendix C Clock Tree Structure




PLL
1GHz
1/16
CLK_62_5Mhz
DIVPRG
CLKEN
ADC_CLK
NAND_ECLK
QSPI1_REFCLK
QSPI2_REFCLK
Not exist in RZ/N1D
SDIO1_ECLK
SDIO2_ECLK
1/160
CM3_STCLK
HWRTOS_MDCCLK
A5PSW_SXCLK
HSR_CLK100
RZ/N1D only
1/10
SERCOS_HCLK
SERCOS_CLK100
ECAT_CLK100
CONV_CLK125
1/8
ECAT_HCLK
CONV_CLK25
1/40
ECAT_CLK25
MII_REFCLK
RMII_REFCLK
CONV_CLK50
1/20
SERCOS_CLK50
HSR_CLK50
HSR_HCLK
RZ/N1D only
1/400
CONV_CLK2P5
PWRCTRL_PG0_ADCDIV
PWRCTRL_NFLASHDIV
PWRCTRL_QSPI1DIV
PWRCTRL_QSPI2DIV
PWRCTRL_SDIO1DIV
PWRCTRL_SDIO2DIV
PWRCTRL_HWRTOS_MDCDIV
PWRCTRL_SWITCHDIV


PLL
1GHz
DIVPRG
CLKEN
I2C[m]_SCLK (m=1..2)
DIVPRG
CLKEN
LCD_ECLK
PWRCTRL_PG0_I2CDIV
DIVPRG
CLKEN
SPI[m]_SCLK (m=1..4)
PWRCTRL_PG4_PR1DIV
DIVPRG
CLKEN
SPI[m]_SCLK (m=5..6)
PWRCTRL_PG1_PR3DIV
1/40
CLKEN
PG2_PCLK
PWRCTRL_PG1_PR4DIV
CLKEN
TIMER[m]_PCLK (m=1..2)
CLKEN
USB_PCICLK
1/8
CLKEN
USB_HCLKH
CLKEN
USB_HCLKF
CLKEN
USB_HCLKPM
1/10
CLKEN
PWM_PCLK
PWRCTRL_PG0_UARTDIV
DIVPRG
CLKEN
PWRCTRL_PG1_PR2DIV
DIVPRG
CLKEN
USBPLL
480MHz
1/10
CLKEN
0
1
UART[m]_SCLK (m=1..3)
PWRCTRL_PG0_0.UARTCLKSEL
CLKEN
0
1
UART[m]_SCLK (m=4..8)
PWRCTRL_PG1_PR2.UARTCLKSEL
USB_DCLK48
CLKEN
CAN[m]_HCLK(m=1..2)
RGMII_REFCLK
CLKEN
RGMII_REFCLK_OUT_GATED

REVISION HISTORY	RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: System Introduction, Multiplexing, Electrical and Mechanical Information

Rev.	Date	Description	
		Page	Summary
0.50	Jun 30, 2017	—	First Edition issued
0.80	Oct 31, 2017	13	1.1, revised
		14	1.2, Table 1.1 (1/8), modified
		15	1.2, Table 1.1 (2/8): General Purpose I/O Ports → IO Multiplexing, modified. IO Multiplexing: Locations of IOs for Peripherals are selectable, added. DDR2/3 Controller: Description, modified.
		16	1,2, Table 1.1 (3/8): SD/SDIO/eMMC: Normal mode → Default mode, revised
		20	1.2, Table 1.1 (7/8): SPI Master: ssi_clk → SPI_SCLK, corrected. SPI Slave: DMA Transmit and Receive transfer enabling by external event (rising or falling edge), deleted. CAN: 2× triggers, deleted.
		21	1.2, Table 1.1 (8/8), modified
		22	1.3, corrected and modified
		23, 24	1.4, Figure 1.1 and 1.2, corrected and modified
		23	1.4, Figure 1.1: figure title, modified
		24	1.4, Figure 1.2: figure title, modified
		25	1.4, Figure 1.3, added
		27, 29, 30	2.1, Figure 2.2, 2.4 and 2.5: 4000E000 to 400F1FFF, corrected
		26 to 30	2.1, Figure 2.1 to 2.5: module name, revised
		31, 32	2.2, Table 2.1, modified (product packege column, added. Note, added. module name, revised.)
		34	3.1, Figure 3.1, modified
		37 to 39	3.5, Table 3.2, corrected and modified
		40	3.6.1, Table 3.3, revised
		40	3.6.1.1, Figure 3.3, revised
		41	3.6.2.1, Figure 3.5, revised
		43	4.2, chapter title, modified
		43	4.2.2, description, modified
		43	4.2.3, chapter title, modified. 4.2.3, description, modified.
		45	5, section title, modified
		45	5.1, RGMII Interface, corrected
		47	5.1, Table 5.2: Function Number 48, corrected
		48	5.2, Table 5.3: table title, corrected
		49	5.3.1, Table 5.4: b9, b8 and b3 to b0: description, modified. Note1, deleted
		50	5.3.2, Table 5.5: b11, b10 and b3 to b0: description, modified. Note1: description, modified.
		51	5.3.3, Table 5.6: description, modified
		53	5.3.5, chapter title, corrected. 5.3.5, Table 5.8: description, modified.
		56	5.3.8, Address, corrected (5100 0480h + 4h × [n] → 5100 0480h + 4h × n)
		57, 58	5.4.1 and 5.4.2, description, modified
		59	5.4.3, Figure 5.2: figure title, corrected
		60	6.1, description, revised
		60 to 150	6.2 and 6.3 (including sub-capter), Register Name, corrected
		66	6.3.3, Table 6.6: R/W cell of b32 and b2 to b0, corrected

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		Page	Summary
0.80	Oct 31, 2017	67	6.3.4, Table 6.7: DIV, modified
		68	6.3.5, Table 6.8: DIV, modified
		69	6.3.6, Table 6.9: DIV, modified
		70	6.3.7, Table 6.10: DIV, modified
		81	6.3.18, moved NOTE to under Table 6.21, modified
		82	6.3.19, “Value after reset” of b5, corrected. Bit Name of b5, corrected
		85	6.3.22, Table 6.22: RSTN_A_ZERO, modified. NOTE, modified
		88	6.3.25, Table 6.28: Bit Position, corrected (b31 to b8 → b31 to b4)
		89	6.3.26, Table 6.29: UARTCLKSEL, modified. b29-b18, modified
		98	6.3.33, NOTE, modified
		103	6.3.40, chapter title, corrected
		106	6.3.45, Table 6.48: b5, b4: modified
		110	6.3.49, Table 6.52: Bit Name, corrected
		113	6.3.53, Table 6.56: description of WDM3RST_ST and WDA7RST_ST, modified
		114	6.3.54, Table 6.57: Note of b0, deleted
		118	6.3.58, Table 6.61: moved Caution of b24 to as Note1, modified. UARTCLKSEL, modified. b19-b0, modified. Note2, added.
		125	6.3.66, description, corrected
		130	6.3.70, Table 6.73: SCON_Q, corrected
		134	6.3.74, Table 6.77: CLKEN_A, revised
		134	6.3.74, NOTE, modified
		141	6.3.82, Table 6.85: DIRPD, revised
		142	6.3.83, Table 6.86: LCD1PU, modified
		143	6.3.84, Table 6.87: SLOTTYPE, modified. BASECLKFREQ, revised.
		147 to 149	6.3.88, Table 6.91, corrected
		151	7.1, description, modified
		151	7.1, Figure 7.1, revised
		152	7.2, chapter title, modified
		152	7.2.1, description, modified
		152	7.2.2, description, revised
		153	7.2.3, description, revised
		154	7.2.4, description, revised
		155	7.3.2, Table 7.1: table title, corrected
		155	7.3.2, Table 7.1, modified
		156	7.3.3, Figure 7.2, corrected. 7.3.3, description, modified.
		157	7.3.4, chapter title, corrected
		157	7.3.4, description, modified
		157	7.3.5, chapter title, corrected
		157	7.3.5, description, modified
		158	7.4, chapter titile, modified
		159	7.4.3, Table 7.2, modified
		161	7.5, chapter title, corrected
		165, 166	7.5.4, Table 7.3, revised
		165	7.5.4, description, modified
		167	8.1, description, revised
		172	8.2.1, Table 8.11, revised

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		Page	Summary
0.80	Oct 31, 2017	175	8.3.1, Figure 8.3, corrected
		176	8.3.2, Figure 8.4, revised
		177	8.4.1.1, newly added
		179	9.2.2, chapter title, changed
		181 to 184	9.2.4, Table 9.1, revised and corrected
		185	10.1, Table 10.1, revised and corrected (Table title, modified. Power column, added. IO column, deleted. Description, modified)
		186, 187	10.1, Table 10.2 (1/2) and (2/2), revised and corrected (Table title: Table 10.1 → 10.2, (2/3) → (1/2), (3/3) → (2/2), modified. Power and Active column, added. Description, modified)
		188 to 190	10.1, Table 10.3, revised and corrected (Active Level column, added. CAT_RESETOUT → CAT_RESETOUT_N, modified. S3_TESTPIN[n] → S3_TESTPIN[m], corrected. GPIO[m]a[n] → BGPIO[m]a[n], GPIO[m]b[n] → BGPIO[m]B[n], corrected. Description, modified.)
		191	10.2, Table 10.4, modified
		197	11.1. Table 11.1: Absolute Maximum Ratings, corrected
		198	11.2. Table 11.2: Recommended Operating Conditions, corrected
		199	11.3.1, Table 11.3: Current spec, revised
		200	11.3.2, Table 11.4: Digital IO spec, corrected
		201	11.4.1, Power-up timing figure, revised
		201	11.4.2, Power-down timing figure, revised
		202	11.5.1.1, Table 11.6: Note, revised
		205	11.5.1.4, Table 11.9: MDIO interface spec parameter, revised
		206	11.5.2.1, Table 11.10: QSPI Flash Interface spec, corrected
		206	11.5.2.1, QSPI Flash Interface timing figure, corrected
		207	1.5.2.2, DDR3/DDR2 Interface timing figure, corrected
		211	11.5.2.4, Table 11.14: SD/MMC/SDIO interface spec, revised
		216	11.5.3.4, I2C timing figure, corrected
		218	11.5.3.6, Table 11.21: JTAG spec, revised and corrected
		218	11.5.3.6, Table 11.22: SWD spec, revised and corrected
		218	11.5.3.6, JTAG/SWD timing figures, corrected
		219	11.5.4, Table 11.23: IO strength of Note, corrected
		220	11.5.5, Table 11.24, revised
		221	11.5.5, Table 11.25, revised
		222	11.6, VREFP → VADC REFP, VREFM → VADC REFM, VAREFP → VADC REFP, VAREFM → VADC REFM, corrected
		226, 227	Appendix A, Table A.1: Pin assignment corrected. (DDR pins)
		233, 234	Appendix A, Table A.2: Pin assignment corrected. (RTC_VDD33, ADC1_VDD, ADC_GND)
		235	Appendix B: newly added
		239	Appendix C: newly added
0.90	Dec 28, 2017	all	All sections, corrected English spelling and syntax errors
		13, 19, 33, 157, 177	Section 1, 3, 7 and 9, add trademarks
		13, 14, 21 to 30, 157, 177, 185	Section 1, 2, 7, 9, and 10, ARM → Arm, changed
		13	1.1, Low Power Feature and Advanced real-time Ethernet features, revised
		14	1.2, Description of CPU, revised
		15	1.2, Description of DMAC, revised
		15	1.2, Description of MSEBI, Address/data/control-data are multiplexed on data bus, added

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		Page	Summary
0.90	Dec 28, 2017	15	1.2, Description of DDR2/3 Controller, revised
		16	1.2, Description of QSPI, revised
		16	1.2, Description of SD/SDIO/eMMC, revised
		19	1.2, Description of USB2.0 HOST, revised
		19	1.2, Description of UART 4, 5, 6, 7, 8, revised
		20	1.2, Description of SPI 1, 2, 3, 4 (Master), revised
		20	1.2, Description of I^2C 1, 2, revised
		21	1.2, Description of LCD Controller, revised
		21	1.2, Description of Clock Monitoring, revised
		31	2.2, description, revised
		32	2.2, Table 2.1: Note2, corrected
		36	3.4, CAUTION, revised
		37	3.5, capter title, modified
		37	3.5, description, revised
		37	3.5, Table 3.2, R-IN/RTOS → R-IN Engine, corrected
		43	4.2.2, description, revised
		43	4.2.2, Table 4.3: RSTEN, System Reset Source Control/Mask Register → Reset Enable Register, changed
		43	4.2.2, Table 4.3: RSTEN, description, revised
		43	4.2.2, CAUTION, corrected
		44	4.3, revised
		45	5.1, LVTTL, removed
		51, 53	5.3.3 and 5.3.5, Function, revised
		54	5.3.6, Table 5.9: b2 to b0, HighZ → Floating, corrected
		57, 58	5.4.1 and 5.4.2, description, revised
		60	Section 6, PWRCTRL_CRYPTO and PWRSTAT_CRYPTO registers, deleted
		61, 66	Section 6, Register Name of PWRCTRL_CA7DIV, Clock Divider Control for CA7 CLKIN → Clock Divider Control for CA7, changed
		62, 111	Section 6, Register Name of RSTSTAT, Reset Status Register Showing the Source of the Last Reset → Reset Status Register, changed
		63, 121	Section 6, Register Name of RSTEN, System Reset Source Control/Mask Register → Reset Enable Register, changed
		64 to 77	6.3, Function of PWRCTRL_*DIV registers, revised
		65	6.3.2, description, corrected
		80, 81, 83 to 110, 113 to 120, 122, 123, 125 to 137	6.3, Function of MIREQ_*, SLVRDY_*, RSTN_*, MISTAT_*, MIRACK_* and SCON_* bits, revised
		81	6.3.18, CAUTION, modified
		82	6.3.19, Table 6.22: WFI low-power state → WFI state, WFE low-power state → WFE state, modifed
		82	6.3.19, Table 6.22: CA7_STANDBYWFIL2, description, modified
		84, 86 to 89, 96 to 98, 101 to 103, 105, 106, 109, 110, 114, 127 to 135	6.3.21, 6.3.23 to 6.3.25, 6.3.31 to 6.3.33, 6.3.39 to 6.3.41, 6.3.44, 6.3.45, 6.3.48, 6.3.50, 6.3.54, and 6.3.67 to 6.3.75, NOTE, modified
		88, 116	6.3.24 and 6.3.56, Note 1, revised
		96, 108	6.3.31 and 6.3.47, NOTE, revised

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		Page	Summary
0.90	Dec 28, 2017	111	6.3.51, Table 6.54: Function, revised
		112	6.3.52, NOTE and CAUTION, revised
		121	6.3.62, description, revised. 6.3.62, Table 6.65: Function, modified.
		123	6.3.64, description, modified
		123, 124	6.3.64 and 6.3.65, Function, revised
		138	6.3.79, Table 6.84: CM3SYSRESET_REQ: Function, revised
		139	6.3.80, revised
		141	6.3.82, Table 6.87: SLOTTYPE: Function, modified
		144	6.3.85, Table 6.90: Function, revised
		148	6.3.87, Table 6.92: title, corrected
		148	6.3.88, sleep state → standby mode, modified. 6.3.88, Table 6.93: Function, revised
		149	7.1, description, revised
		150 to 152	7.2, description, revised
		153 to 155	7.3, description, revised
		156 to 158	7.4, Requirement chapter, deleted. 7.4, description, revised
		159	7.5, NoC socket → NoC interconnect, revised
		159	7.5.3, description, revised
		160	7.5.4, CAUTION, modified.
		161, 162	7.5.4, Figure 7.3 and 7.4, revised
		163	7.5.4, description, modified
		163	7.5.4, Table 7.3, table title and header line, modified
		163	7.5.4, Table 7.3: BGPIO 1/2/3 row has been divided into BGPIO1/2 row and BGPIO3 row.
		163	7.5.4, Table 7.3: USB row, add the Note 5 marker to CLKEN/RSTN cell of Type of REQ colum, corrected
		164	7.5.4, Table 7.3: NAND Flash Controller row, add the Note 2 marker to CLKEN/RSTN cell of Type of RDY colum, corrected
		164	7.5.4, Table 7.3: Note 2, 3, 7, revised. 7.5.4, Table 7.3: Note7, modified.
		165, 166	Section 8, moved Supported Ethernet Port table from 8.4.1.1 to 8.1
		165	8.1, Figure 8.1, revised. 8.1, Table8.1: Note, added
		172	8.2.2, Figure 8.2: Note 3 and 4, revised
		176	8.4.1.1, chapter title, modified
		177	9.1, description, modified
		177	9.1.1, integrated GIC → GIC, modified
		177	9.1.2, tail chaining of interrupts → multiple interrupts, modified
		178	9.2.1, chapter title, modified. 9.2.1, description, revised.
		178	9.2.2, description, revised
		179	9.2.3, Figure 9.1, figure title, modified
		180	9.2.4, Table 9.1: IRQ16 to 29 and 31 to 33, IRQ name and Description, changed
		181	9.2.4, Table 9.1: IRQ53, changed to Reserved
		184	10.1, Table 10.1: Description of USB_AVDD and USB_AVSS, revised
		184	10.1, Table 10.1: ANF_VDD_33V, deleted
		185	10.1, Table 10.2: Description of CTRSTBYB, High-Z → Floating
		186	10.1, Table 10.2: Description of USB_DP* and USB_DM*, revised
		187	10.1, Table 10.3: MII_REFCLK → MII_REFCLK_[5:0], changed
		187	10.1, Table 10.3: Description of SDIO[m]_LEDCTRL, revised

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0.90	Dec 28, 2017	188	10.1, Table 10.3: Description of MSEBIM_ACD[31:0] and MSEBIS_ACD[31:0], Command → Control, modified
		188	10.1, Table 10.3: Description of MSEBIM_WAIT_N[3:0] and MSEBIS_WAIT_N[3:0], revised
		188	10.1, Table 10.3: Description of LED signals (S3_LED_GN, S3_LED_RD, S3_ACTLEDP[m], and S3_LINKLEDP[m]), modified
		189	10.1, Table 10.3: Description of Safty signals, revised
		191	10.3.1, Figure 10.1: F9, ANF_VDD_33V → VDD33, modified
		192	10.3.2, Figure 10.2: E9, ANF_VDD_33V → VDD33, modified
		193	10.3.3, Figure 10.3: B5, ANF_VDD_33V → VDD33, modified
		194	10.3.4, Figure 10.4: C4, ANF_VDD_33V → VDD33, modified
		196, 197	11.1 and 11.2, specification of V_{ANF}, deleted
		200	11.4, timing chart figures, modified (High-Z → Floating)
		205	11.5.2.1, interface timing figure, corrected (index symbol, n → m)
		210, 211	11.5.2.4, Table 11.14 and Table 11.15: Input CMD, IO setup time, 6 → 4, corrected
		227	Appendix A, Table A.1: ANF_VDD_33V, deleted
		232	Appendix A, Table A.2: VDD33, added assignment at N1D400 (F9), N1D324 (E9), N1S324 (B5) and N1S196 (C4), modified
		234	Appendix B, description, added
		234 to 237	Appendix B, Table B.1: header line, revised
		235	Appendix B, Table B.1: GPIO60: Level1 Func3, MII_REFCLK → MII_REFCLK_0, changed
		235	Appendix B, Table B.1: GPIO61: Level1 Func3, MII_REFCLK → MII_REFCLK_1, changed
		236	Appendix B, Table B.1: GPIO112: Level Func2, MII_REFCLK_2, added
		236	Appendix B, Table B.1: GPIO126: Level Func2, MII_REFCLK_3, added
		236	Appendix B, Table B.1: GPIO134: Level Func2, MII_REFCLK_4, added
		237	Appendix B, Table B.1: GPIO145: Level Func2, MII_REFCLK_5, added
0.95	Oct 19, 2018	—	All sections, spelling, syntax errors and appearances are corrected, and expressions are modified properly
		—	All sections delete safety function (Clock Monitoring, Watchdog Safe 1/2, Safety Reset, Safety Filtering)
		4	How to Use This Manual, 1. Objective and Target Users, Documents related to RZ/N1 (R18DS0026 → R01DS0323), table modified
		6	How to Use This Manual, 3. List of Abbreviations and Acronyms, INTC, OTP, description modified
		13	1.1 Device Overview, DMA (2 × DMA with 16 channels → 2 × DMA with 8 channels each), description modified
		13	1.1 Device Overview, Timer block (6 × 16 bits + 2 × 32 bits → 16bit × 6ch, 32bit × 2ch), description modified
		13	1.1 Device Overview, ADC (ADC @ 1 MHz → ADC (up to 1 MSPS)), description modified
		13	1.1 Device Overview, MSEBI (Parallel Bus Interface), description added
		13	1.1 Device Overview, Note2 (EtherCAT trademark), expression modified
		14	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (1/8), CPU (16 KB/16 KB → 16 KB (instruction)/16 KB (data)), expression modified
		14	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (1/8), Watchdog, description modified
		15	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (2/8), Semaphore, description added
		15	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (2/8), DDR2/3 Controller, expression modified
		16	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (3/8), Quad SPI (QSPI), description added

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0.95	Oct 19, 2018	16	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (3/8), SD/SDIO/eMMC (eMMC card interface → eMMC interface, ADMA → ADMA2), description modified
		16	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (3/8), R-IN Engine, description modified
		17	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (4/8), Advanced 5 Port Switch, description modified
		18	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (5/8), SercosIII Slave Controller, description modified
		19	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (6/8), Independent GMAC, description modified
		20	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (7/8), CAN 1, 2 (with record of bit → with data of bit), description modified
		20	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (7/8), General Purpose Timers, expression modified
		21	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (8/8), Power Supply Voltage (3.3V → 3.3 V ± 0.3V, 1.8 V; 1.5 V → 1.8 V ± 0.1 V; 1.5 V ± 0.075 V), others, description modified
		22	1.3 List of Products, (Peripherals SoC → Peripheral Group, others), description modified
		23	1.4 Block Diagram, Figure 1.1 RZ/N1D Dual Cortex-A7 & Cortex-M3, figure modified
		24	1.4 Block Diagram, Figure 1.2 RZ/N1S Single Cortex-A7 & Cortex-M3, figure modified
		26	2.1.1 RZ/N1D, Figure 2.1 Memory Map of RZ/N1D (Cortex-A7) (delete: Service area, add: GIC access area), figure modified
		27	2.1.1 RZ/N1D, Figure 2.2 Memory Map of RZ/N1D (Cortex-M3) Same configuration as CA7, figure modified
		28	2.1.2 RZ/N1S, Figure 2.3 Memory Map of RZ/N1S (Cortex-A7) (add: GIC access area), figure modified
		29	2.1.2 RZ/N1S, Figure 2.4 Memory Map of RZ/N1S (Cortex-M3) Same configuration as CA7, figure modified
		30	2.1.3 RZ/N1L, Figure 2.5 Memory Map of RZ/N1L, figure modified
		31	2.2 Register Map Summary, Table 2.1 Register Map (1/2), description modified
		32	2.2 Register Map Summary, Table 2.1 Register Map (2/2), description modified
		34	3.1 Overview, Figure 3.1 Block Diagram of Clock Generation, description modified
		37	3.5 Clock Frequency Scaling, description modified
		37, 38	3.5 Clock Frequency Scaling, Table 3.2 Frequency Mode SD/SDIO/eMMC (50 MHz → Up to 50 MHz), ADC (20 MHz → Up to 20 MHz), BGPIO, others, description modified
		39	3.5 Clock Frequency Scaling, Table 3.2 Frequency Mode, Note1,2 (Relationship between asCore and sCore), description added
		39	3.5 Clock Frequency Scaling, Table 3.2 Frequency Mode, Note3 (Ether mode), description added
		47	5.1 Overview, Table 5.2 IO Multiplex Configuration Level2 List, description modified
		49	5.3.1 rGPIOs_Level1_ConfigA_[n] — GPIO[n] RGMII Multiplexing Level1 Configuration Register (n = 0..59), caution added
		50	5.3.2 rGPIOs_Level1_ConfigB_[n] — GPIO[n] Standard Multiplexing Level1 Configuration Register (n = 60..169 (max)) Bit(level1_xx → level1_Standard_xx), name modified
		50	5.3.2 rGPIOs_Level1_ConfigB_[n] — GPIO[n] Standard Multiplexing Level1 Configuration Register (n = 60..169 (max)), caution added
		51	5.3.3 rGPIOs_Level1_StatusProtect — GPIO Multiplexing Level1 Status and Protect Register, caution deleted
		52	5.3.4 rGPIOs_Level2_Config_[n] — GPIO[n] Multiplexing Level2 Configuration Register (n = 0..169 (max)), caution added
		53	5.3.5 rGPIOs_Level2_StatusProtect — GPIO Multiplexing Level2 Status and Protect Register, caution deleted

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0.95	Oct 19, 2018	56	5.3.8 rGPIOs_Level2_Gpio_Int_[n] — GPIO_Int[n] Interrupt Configuration Register (n = 0..7), bGPIOs_Level2_GPIO_Int (BGPIO3 → BGPIO2), description modified
		64	6.3.1 PWRCTRL_SWITCHDIV — Clock Divider Control for A5PSW, DIV (Valid range: 5-40 → Valid range: 5), description modified
		68 to 70, 75	6.3.5 PWRCTRL_PG1_PR3DIV — Clock Divider Control for PG1 Program3, DIV (clock Mode → frequency mode), term modified 6.3.6..7, 6.3.12, Same as 6.3.5 PWRCTRL_PG1_PR3DIV
		68 to 71, 75, 79	6.3.5 PWRCTRL_PG1_PR3DIV — Clock Divider Control for PG1 Program3, DIV, note added 6.3.6..8, 6.3.12, 6.3.16 Same as 6.3.5 PWRCTRL_PG1_PR3DIV
		80	6.3.17 PWRCTRL_SDIO1 — Power Management Control for SDIO1, Function, expression modified
		82	6.3.19 SYSSTAT — System Status Flags Register, CA7_STANDBYWFIL2 (All processors → All Cortex-A7 processors), description modified
		83	6.3.20 PWRCTRL_USB — Power Management Control for USB2.0, Function, clocks expression modified 6.3.22..78 Same as 6.3.20 PWRCTRL_USB
		87	6.3.24 PWRCTRL_PG0_0 — Power Management Control #0 for PG0, Function (UART clocks → UART[m]_SCLK (m = 1..3)), description modified
		115	6.3.55 PWRCTRL_PG2_25MHZ — Power Management Control for PG2 25 MHz, SLVRDY_Q, CLKEN_Q, description modified
		116	6.3.56 PWRCTRL_PG1_PR2 — Power Management Control for PG1 Program2, Function (UART clocks → UART[m]_SCLK (m = 4..8)), description modified
		121	6.3.62 RSTEN — Reset Enable Register, SWRST_EN, description modified
		123	6.3.64 PWRCTRL_RTC — Power Management Control for RTC, RST_RTC (No Reset → Reset release), expression modified
		128	6.3.68 PWRSTAT_PG2_25MHZ — Power Management Status for PG2 25 MHz, SCON_Q, description modified
		136	6.3.76 PWRCTRL_RINCTRL — Power Management Control for R-IN Engine Accessory Register, description modified
		138	6.3.79 RSTCTRL — Reset Control Register, SWRST_REQ (Software reset request → Software triggered system reset request, Not Reset → No system reset request), description modified
		139	6.3.80 CFG_USB — USB Mode Configuration Register, description modified
		140	6.3.81 OPMODE — System and Boot Configuration Register, Value after reset, note added
		140	6.3.81 OPMODE — System and Boot Configuration Register, LCD1PU, description modified
		145	6.3.86 CFG_DMAMUX — DMA1 & DMA2 Multiplexer Register, description modified
		149	7.1 Overview, description modified
		150	7.2.1 Common Feature, RAM requirements and 2nd Stage Boot Image, description modified
		150	7.2.2 QSPI Boot Feature, description modified
		151	7.2.3 NAND Boot Feature, description modified
		153	7.3.2 External Pin Configuration, Table 7.1 External Pin Configuration, Comment, description modified
		155	7.3.5 RZ/N1L Boot, description modified
		157	7.4.2 Implementation Specifics, Table 7.2 SPKG Fields, description modified
		158	7.4.2 Implementation Specifics, QuadSPI, description modified
		160	7.5.4 Generic Programming Sequence for NoC, caution deleted
		163, 164	7.5.4 Generic Programming Sequence for NoC, Table 7.3 Related Registers for Connect/Disconnect of Each module, description modified
		167	8.2 Support Modes (Support Modes for Each Module → Support Modes), title modified

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0.95	Oct 19, 2018	167	8.2 Support Modes, Table 8.3 Support Modes of Ethernet I/F, description modified
		168, 169	8.2 Support Modes, Table 8.4 Clock I/F for Ethernet PHY (Part 1)..Table 8.10 Clock I/F for Ethernet PHY (Part 7), description modified
		171	8.2.1 Internal connection of Ethernet ports (Switch Mux Modes → Internal connection of Ethernet ports), title and description modified
		171	8.2.1 Internal connection of Ethernet ports, Table 8.12 Internal connection of Ethernet ports (Switch Mux Modes → Internal connection of Ethernet ports), title and description modified
		172	8.2.2 Selection of clocks for PTP (PTP Modes → Selection of clocks for PTP), title and description modified
		172	8.2.2 Selection of clocks for PTP, Figure 8.2 Selection of clocks for PTP by PTPMCTRL register (Connection of ptp_timestamp Signals → Selection of clocks for PTP by PTPMCTRL register), title and figure modified
		173	8.2.2 Selection of clocks for PTP, Table 8.13 Selection of clocks for PTP (PTP_MODE Selection (1/2) → Selection of clocks for PTP), title and description modified
		173	8.2.2 Selection of clocks for PTP, Table 8.14 Recommended setting of PTP_MODE (PTP_MODE Selection (2/2) → Recommended setting of PTP_MODE), title modified
		174	8.3.1 Initializing, Figure 8.3 Initializing of Ethernet Flowchart, figure modified
		175	8.3.2 ETHMODE_SET, Figure 8.4 ETHMODE_SET Flowchart, figure modified
		176	8.4.1 Restriction, description modified
		176	8.4.1.1 Supported Ethernet Signals, Table 8.15 Ethernet Signals for Each PHY Mode, term modified
		179	9.2.3 Interrupt Management on Cortex-A7 and Cortex-M3, Figure 9.1 Interrupt Management on Cortex-A7 and Cortex-M3, figure modified
		180	9.2.4 Interrupts Allocation and Vector Number, Table 9.1 Interrupts Allocation and Vector Number (1/4) (IRQ32,33: HWRTOS_TM_LPI_AST_Int and HWRTOS_TM_LPI_DEAST_Int → Reserved, others), description modified
		181	9.2.4 Interrupts Allocation and Vector Number, Table 9.1 Interrupts Allocation and Vector Number (2/4) (A5PSW_HUB_Int, A5PSW_PTRN_Int), description modified
		182	9.2.4 Interrupts Allocation and Vector Number, Table 9.1 Interrupts Allocation and Vector Number (3/4), description modified
		183	9.2.4 Interrupts Allocation and Vector Number, Table 9.1 Interrupts Allocation and Vector Number, Note1, description added
		184	10.1 Pinout Description, Table 10.1 PKG Power Supply Pin Name, OTP Power supply (OTP → OTP memory), term modified
		185	10.1 Pinout Description, Table 10.2 PKG Pin Name (1/2), CTRSTBYB, description modified
		189	10.1 Pinout Description, Table 10.3 GPIO Multiplexed Pin Name (3/3), description modified
		196	11.1 Absolute Maximum Ratings, Table 11.1 Absolute Maximum Ratings (OTP → OTP memory), term modified
		197	11.2 Recommended Operating Conditions, Table 11.2 Recommended Operating Conditions (OTP → OTP memory), term modified
		198	11.3.1 Current, Table 11.3 Current (OTP → OTP memory), term modified
		198	11.3.1 Current, Table 11.3 Current (I_{OH} → $-I_{OH}$), expression modified
		198	11.3.1 Current, Table 11.3 Current, Note 1, description added
		199	11.3.2 Digital IO, Table 11.4 Digital IO, Input capacitance, description added
		200	11.4.1 Power-up, DVDD, PLL_AVDD, USB_AVDD, figure modified
		200	11.4.2 Power-down, DVDD, PLL_AVDD, USB_AVDD, figure modified
		202	11.5.1.2 RMII, Table 11.7 RMII, title modified
		206	11.5.2.2 DDR3/DDR2 Interface, Table 11.11 DDR3 -1000, (DQ hold skew factor from DQS → DQ hold time from DQS), description modified
		207	11.5.2.2 DDR3/DDR2 Interface, Table 11.12 DDR2-500, (DQ hold skew factor from DQS → DQ hold time from DQS), description modified

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0.95	Oct 19, 2018	210	11.5.2.4 SD/MMC/SDIO Interface, Table 11.14 SD Bus Timing (Default Mode), Conditions, description modified
		211	11.5.2.4 SD/MMC/SDIO Interface, Table 11.15 SD Bus Timing (High Speed Mode), Conditions, description modified
		217	11.5.3.6 JTAG/SWD, Table 11.21 JTAG, title modified
		217	11.5.3.6 JTAG/SWD, Table 11.22 Serial Wire Debug (SWD), title modified
		221	11.6 ADC Characteristics, Table 11.26 ADC Characteristics, input equivalent capacitance, description added
		222	12.1.1 BGA-400 Package, Figure 12.1 BGA-400 Package Dimensions, figure modified
		223	12.1.2 BGA-324 Package, Figure 12.2 BGA-324 Package Dimensions, figure modified
		224	12.1.3 BGA-196 Package, Figure 12.3 BGA-196 Package Dimensions, figure modified
		240	Appendix C Clock Tree Structure (UART4_SCLK → UART[m]_SCLK (m=4..8)), others figure modified
1.00	Mar 29, 2019	—	All sections, spelling, syntax errors and appearances are corrected, and expressions are modified properly
		22	1.3 Function Comparison per Device Family and Package, title modified
		23	1.4 List of Products, Table 1.3 List of Products, table added
		39	3.5 Clock Frequency Scaling, Table 3.2 Frequency Mode (2/3), Mailbox, description added
		48	5.1 Overview, Table 5.2 IO Multiplex Configuration Level2 List, Function Number 1, description modified
		73	6.3.9 PWRCTRL_SDIO1DIV — Clock Divider Control for SDIO1, DIV, value modified
		74	6.3.10 PWRCTRL_SDIO2DIV — Clock Divider Control for SDIO2, DIV, value modified
		82 to 146	6.3.18 PWRSTAT_SDIO1 — Power Management Status for SDIO1, As same, 6.3.21..24, 6.3.26..49, 6.3.53..63, 6.3.65..66, 6.3.69..70, 6.3.72..73, 6.3.76..78, description modified
		83	6.3.19 SYSSTAT — System Status Flags Register, description modified
		100	6.3.34 PWRSTAT_QSPI1 — Power Management Status for QSPI1, note modified
		115	6.3.49 PWRSTAT_QSPI2 — Power Management Status for QSPI2, note modified
		157	6.3.87 VERSION — Product Version Register, VERSION, description modified
		189	9.2.4 Interrupts Allocation and Vector Number, Table 9.1 Interrupts Allocation and Vector Number (1/4), HWRTOS_*, description modified
		194	10.1 Pinout Description, Table 10.2 PKG Pin Name (1/2), CTRSTBYB, DDR_ADDR, description modified
		198	10.1 Pinout Description, Table 10.3 GPIO Multiplexed Pin Name (3/3), SPI[m]_SS_N[n], description modified
		199	10.2 Handling of Unused Pins, Table 10.4 Handling of Unused Pins, GPIO[n], description added
		222	11.5.3.2 SPI Master, Table 11.17 SPI Master, description modified
		223	11.5.3.3 SPI Slave, Table 11.18 SPI Slave, description modified
		228	11.5.5 MSEBI Interface Timing, Table 11.24 MSEBI master, description modified
		247	Appendix C Clock Tree Structure, SRAM2MB_HCLK, SRAM4MB_HCLK, MBOX_HCLK, figure modified
1.10	Jul 29, 2019	—	Sections 6, 8, and 11 spelling, syntax errors and appearances are corrected, and expressions are modified properly
		88	6.3.24 PWRCTRL_PG0_0 — Power Management Control #0 for PG0 (USBPLL → USB_DCLK48), term modified
		122, 123	6.3.56 PWRCTRL_PG1_PR2 — Power Management Control for PG1 Program2 (USBPLL → USB_DCLK48), term modified
		131	6.3.64 PWRCTRL_RTC — Power Management Control for RTC, term unified
		145	6.3.77 PWRCTRL_SWITCHCTRL — Power Management Control for Ethernet, Accessory Register, RSTN_CLK25, CLKEN_A, description modified

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1.10	Jul 29, 2019	151	6.3.83 DBGCON — Debug Control Register, expression modified
		154 to 156	6.3.86 CFG_DMAMUX — DMAC1 & DMAC2 Multiplexer Register, expression unified, (System Control and Peripheral, 11.6.2 DMA Request Allocation)
		157	6.3.87 VERSION — Product Version Register, VERSION, value modified, description added
		176	8.2 Support Modes, Table 8.3 Support Modes of Ethernet I/F, expression modified
		180	8.2.1 Internal Connection of Ethernet Ports, expression modified
		181	8.2.2 Selection of clocks for PTP, Figure 8.2 Selection of Clocks for PTP by PTPMCTRL Register, note added
		—	Overall of Section 11 Electrical Characteristics, pin names and symbols unified
		—	Overall of Section 11 Electrical Characteristics (CL, drive IO strength → load capacitance CL, drive strength), expression unified
		215 to 216	11.5.2.2 DDR3/DDR2 Interface, expression unified
		224	11.5.3.4 I2C, timing chart, note added
		226	11.5.3.6 JTAG/SWD, Table 11.22 Serial Wire Debug (SWD) (t_{SWD_CL} → t_{SWD_CH}), timing chart (t_{SWD_OUT} → t_{SWD_DOUT}), symbol unified
		228	11.5.5 MSEBI Interface Timing, Table 11.24 MSEBI master and timing chart, pin name (MSEBIM_ALE), expression unified
		229	11.5.5 MSEBI Interface Timing, Table 11.25 MSEBI slave and timing chart, pin name (MSEBIS_WR_N, MSEBIS_RD_N), expression deleted
1.20	May 29, 2020	13	1.1 Device Overview, Security functions, description added
		15	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (2/8), Direct Memory Access Controller (DMAC), description modified
		16	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (3/8), Quad SPI (QSPI), description modified
		21	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (8/8), Security, description added
		22 to 23	1.3 Function Comparison per Device Family and Package, Table 1.2 Renesas CPU Subsystem Part Description, Security functions, description added
		23	1.4 List of Products, Table 1.3 List of Products, Security, description added
		35	3.1 Overview, Figure 3.1 Block Diagram of Clock Generation, USBCLK, figure modified
		43	4.1 Overview, Table 4.1 Category of Reset, System Reset, description modified
		166	7.4.2 Implementation Specifics, Table 7.2 SPKG Fields, BLp_header, description modified
		174	8.1 Overview, Note: reference modified
		209	11.4 Power-up/down Sequence, caution added
		209	11.4.1 Power-up, figure modified
		209	11.4.2 Power-down, figure modified
1.30	Sep 30, 2020	13	1.1 Device Overview, Peripherals, PWMTimer, description added
		20	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (7/8), PWMTimer, description added
		22	1.3 Function Comparison per Device Family and Package, Table 1.2 Renesas CPU Subsystem Part Description, PWMTimer, description added
		24	1.5 Block Diagram, Figure 1.1 RZ/N1D Dual Cortex-A7 & Cortex-M3, PWMTimer, figure modified
		25	1.5 Block Diagram, Figure 1.2 RZ/N1S Single Cortex-A7 & Cortex-M3, PWMTimer, figure modified
		26	1.5 Block Diagram, Figure 1.3 RZ/N1L Cortex-M3, PWMTimer, figure modified
		32	2.2 Register Map Summary, Table 2.1 Register Map (1/2), PWMTimer, description added
		35	3.1 Overview, Figure 3.1 Block Diagram of Clock Generation, PWMTimer, figure modified

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1.30	Sep 30, 2020	39	3.5 Clock Frequency Scaling, Table 3.2 Frequency Mode (2/3), PWMTimer, description added
		47	5.1 Overview, Table 5.1 IO Multiplex Configuration Level1 List, Function Number 0, description modified
		48	5.1 Overview, Table 5.2 IO Multiplex Configuration Level2 List, Function Number 0, description modified
		48	5.1 Overview, Table 5.2 IO Multiplex Configuration Level2 List, PWMTimer, description added
		90	6.3.25 PWRSTAT_PG0 — Power Management Status for PG0, SCON_P, description added
		91	6.3.26 PWRCTRL_PG0_1 — Power Management Control #1 for PG0, SLVRDY_P, RSTN_P, CLKEN_P, description added
		172	7.5.4 Generic Programming Sequence for NoC, Table 7.3 Related Registers for Connect/Disconnect of Each module (1/2), PWMTimer, description added
		189	9.2.4 Interrupts Allocation and Vector Number, Table 9.1 Interrupts Allocation and Vector Number (1/4), PWM_Int, description added
		198	10.1 Pinout Description, Table 10.3 GPIO Multiplexed Pin Name (3/3), PWMTimer, description added
		211	11.5.1.2 RMII, RMII_REFCLK, description added
		249	Appendix C Clock Tree Structure, PWM_PCLK, figure modified
1.40	Feb 28, 2021	17	1.2 Outline of Specifications, Table 1.1 Outline of Specifications (4/8), Advanced 5 Port Switch, description modified
1.50	Dec 29, 2021	—	All sections, spelling, syntax errors and appearances are corrected, and expressions are modified properly
		183	8.2.2 Selection of clocks for PTP, Figure 8.3 Configuration example in PTP, figure added
		210	11.4 Power-up/down Sequence, CAUTION, description added
		210	11.4.1 Power-up, figure modified
		214	11.5.1.4 MDIO, Table 11.9 MDIO, note added

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