User's Manual

CN300-SCAPBACKPOCZ

Smart Terminal with Supercap by ISL81401
Rev.1.0
Sep. 21, 2020

Smart Terminal with Supercap by ISL81401

Description

The CN300-SCAPBACKPOCZ Smart Terminal with Suercap by ISL81401 board is the application of supercapacitor as backup power supply. The board allows quick evaluation of the ISL81401 Bi-directional operation. It is a cost-effective solution for the low-power, wide input voltage range point-of-load application where both stepping up and stepping down voltage capabilities are required.

Specifications

The design specifications of the CN300-SCAPBACKPOCZ Smart Terminal with Supercap by ISL81401 are shown in Table 1.

TABLE 1. SPECIFICATIONS

Parameters	Values
Input Voltage (J1 VIN)	12V to 40V
Output Voltage (J4 VOUT)	12V
Reverse output (J3 VIN)	11V
Input current (Iin)	3A
Output current (Iout)	1.5A

Key Features

- Flexible design
- Bi-directional operation
- High light-load efficiency in pulse skipping DEM operation
- OVP, OTP, and UVP protection
- Back biased from output to improve efficiency
- Convenient power connection

Related Literature

ISL81401 Datasheet

ISL88002 Datasheet

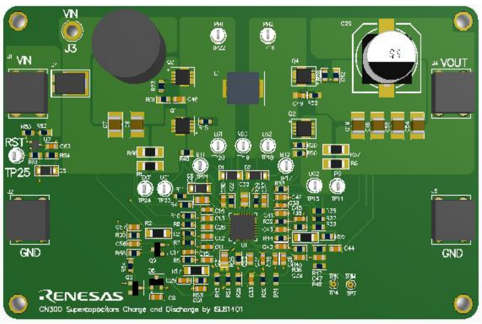

Figure1 Top View

Functional Description

The CN300-SCAPBACKPOCZ board is the same test board used by Renesas application engineers and IC designers to evaluate the performance of the ISL81401 QFN IC. The board provides an easy and complete evaluation of all the IC and board functions.

As shown in Figure 3 on page 3. The DC power is supplied to J1(VIN +) and J2(GND -). The power the load through J3(+) and J2(-). The regulated 12V output on J4 (+) and J5 (-) can supply up to 1.5A to charger the super cap.

As shown in Figure 4 on page 3. After the DC power off, super cap start discharge. The J4(+) and J5(-) is converted to power input. The regulated 11V output on J3(+) and J2(-) can supply up to 3A to load.

Quick Test Setup

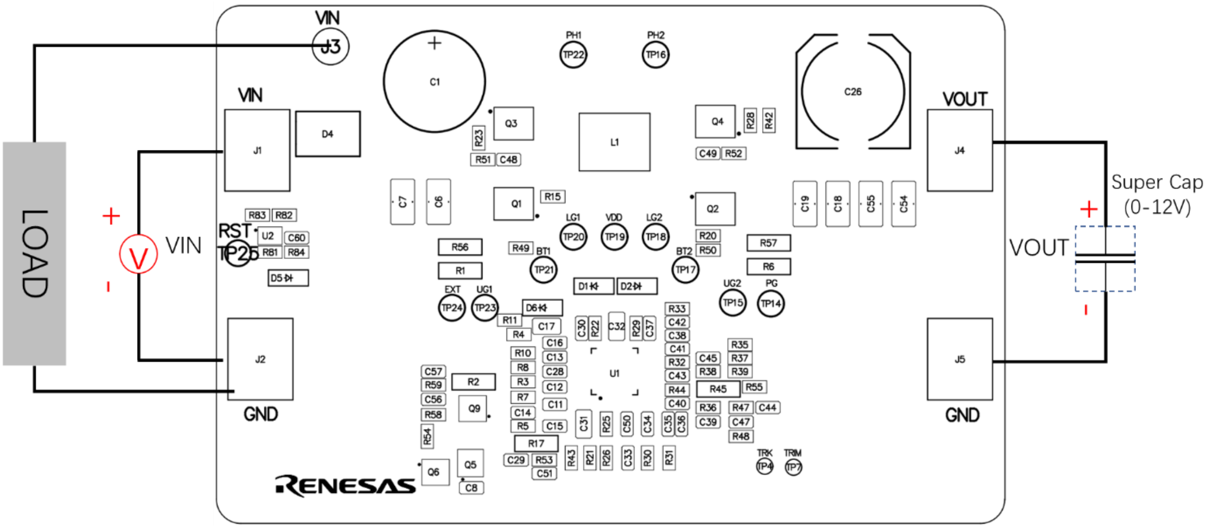

Figure 2 Connection diagram

1, Connect the power supply to the input terminals VIN (J1) and GND (J2). Connect the load terminal to the output VIN (J3) and GND (J2). Connect the super cap to the output VOUT (J4) and GND (J5). Make sure the setup is correct prior to applying any power or load to the board. Refer to Figure2.

2, Adjust the power supply to 12V to 40V and turn it on. The board supplies the load while the super cap is charging. Refer to Figure 3 for the current flow direction.

3, Verify the load voltage and use oscilloscope to monitor the supercapacitor voltage. Refer to Figure 2.

4, When the charging voltage of the super cap reaches the set value, the charging ends. Then turn off the power, the board start discharges. Refer to Figure 4 for the current flow direction.

5, Verify the load voltage and use oscilloscope to monitor the supercapacitor voltage. Refer to Figure 2.

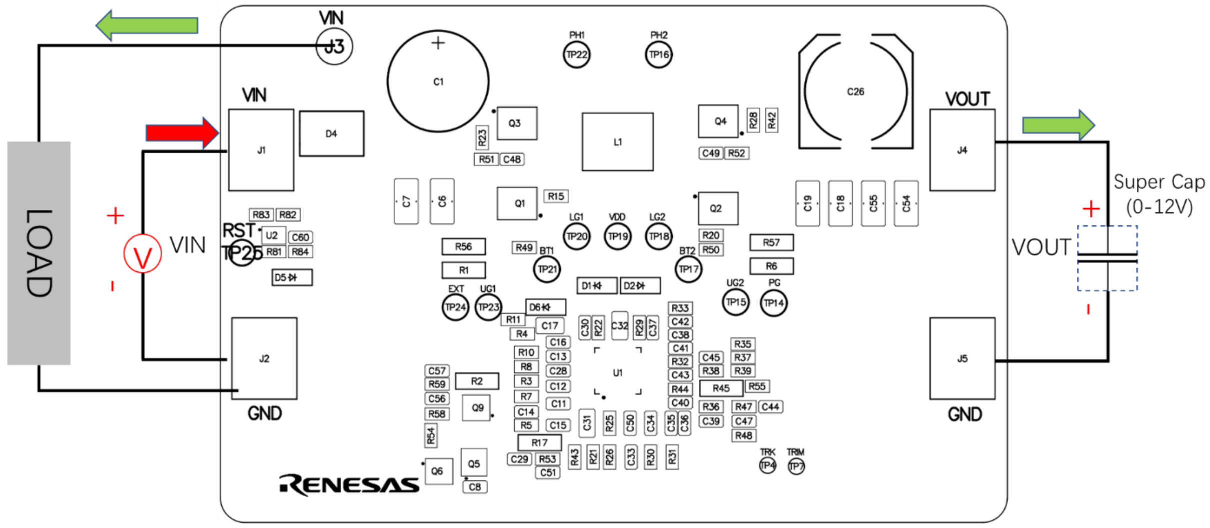

Figure 3 Charging current direction

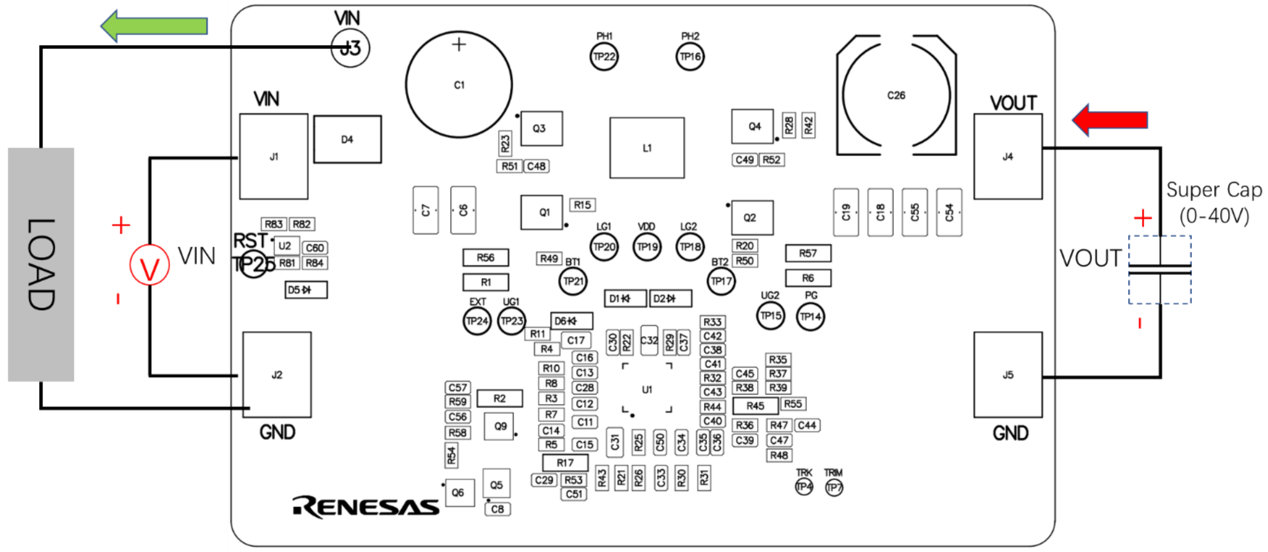

Figure 4 Discharging current direction

Test Environment

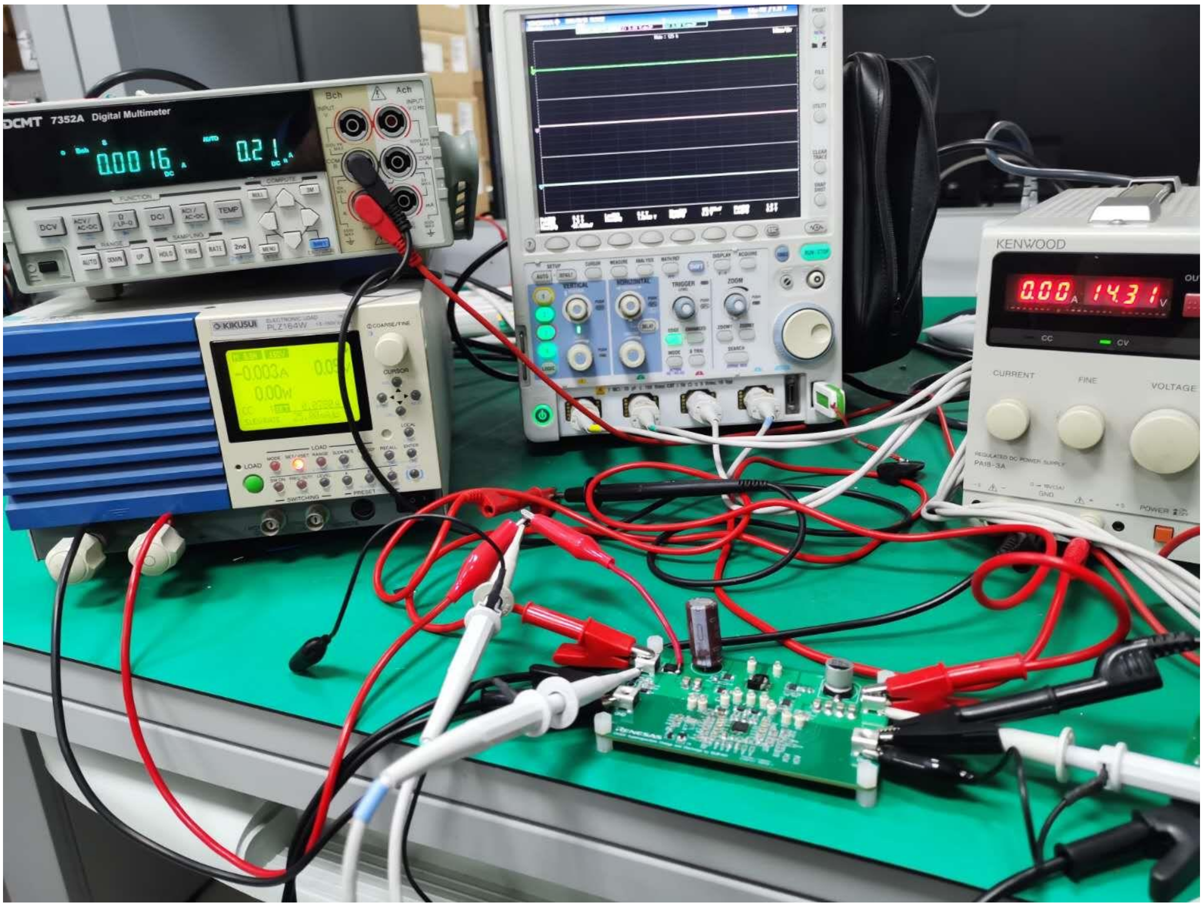

Figure 5 Test Environment

Test Example

- Reverse discharge mode: Electronic load set to CC mode(100mA)
- Disharging voltage: Vout=VCAP=12V, Vin = 11V
- Discharging cut-off:1.2V, discharging time:130.36s, Efficiency: 11*0.2*130.36 / (0.5*2.5*12*12) = 79.66%

$$\mu = \frac{\text{Vout} \times \text{Iout} \times t}{0.5 \times Ccap \times Vcap^2}$$

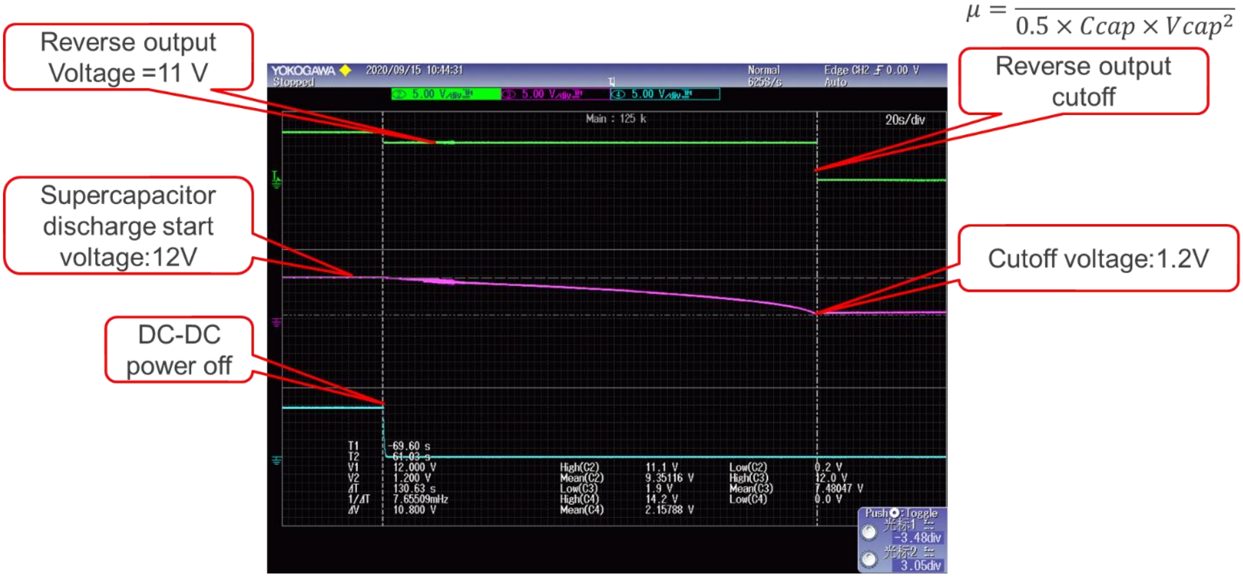

Figure 6 Discharging in CC Mode(100mA)

- Reverse discharge mode: Electronic load set to CC mode(200mA)
- Disharging voltage: Vout=VCAP=12V, Vin = 11V
- Discharging cut-off:2.6V, discharging time:71.19s, Efficiency: 11*0.2*71.19 / (0.5*2.5*12*12)=87.01%

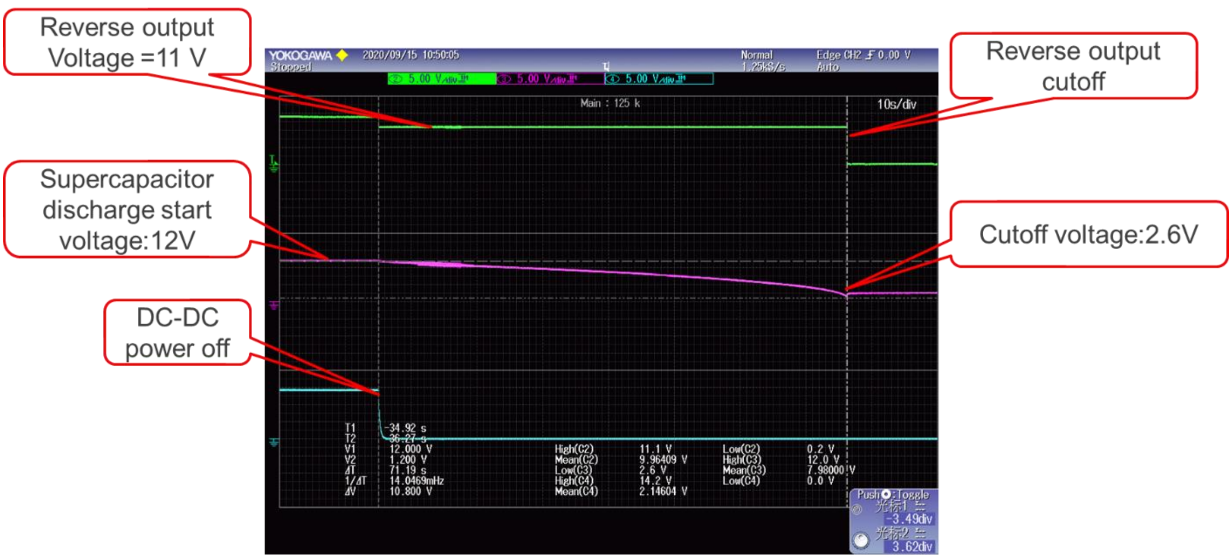

Figure 7 Discharging in CC Mode(200mA)

- Reverse discharge mode: Electronic load set to CC mode(500mA)
- Disharging voltage: Vout=VCAP=12V, Vin = 11V
- Discharging cut-off:3.5V, discharging time:28.197s, Efficiency: 11*0.5*28.197 / (0.5*2.5*12*12) = 86.16%

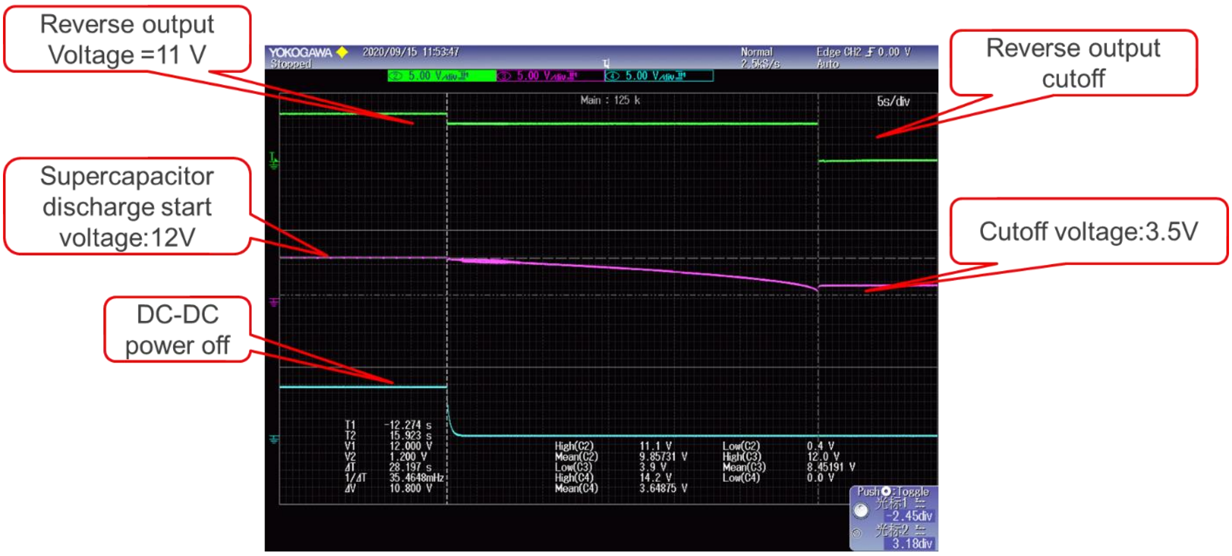

Figure 8 Discharging in CC Mode(500mA)

- Reverse discharge mode: Electronic load set to CC mode(1000mA)
- Disharging voltage: Vout=VCAP=12V, Vin = 11V
- Discharging cut-off:3.5V, discharging time:12.299s, Efficiency: 11*1*12.299 / (0.5*2.5*12*12) = 75.16%

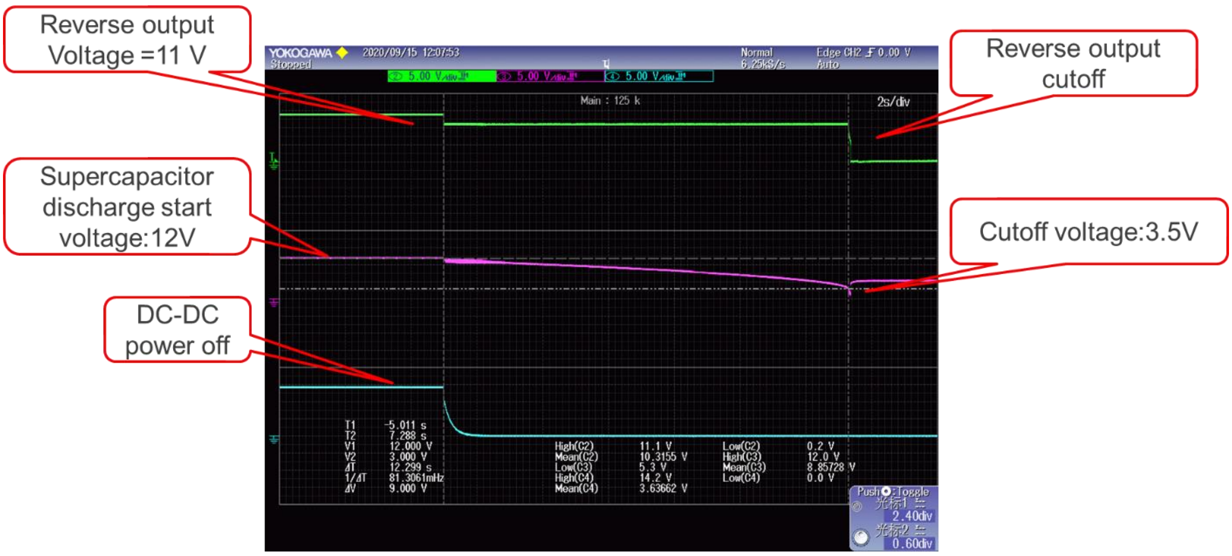

Figure 9 Discharging in CC Mode(1000mA)

- Reverse discharge mode: Electronic load set to CC mode(1500mA)
- Disharging voltage: Vout=VCAP=12V, Vin = 11V
- Discharging cut-off:4.25V, discharging time:6.791s, Efficiency: 11*2*4.038 / (0.5*2.5*12*12) = 49.35%

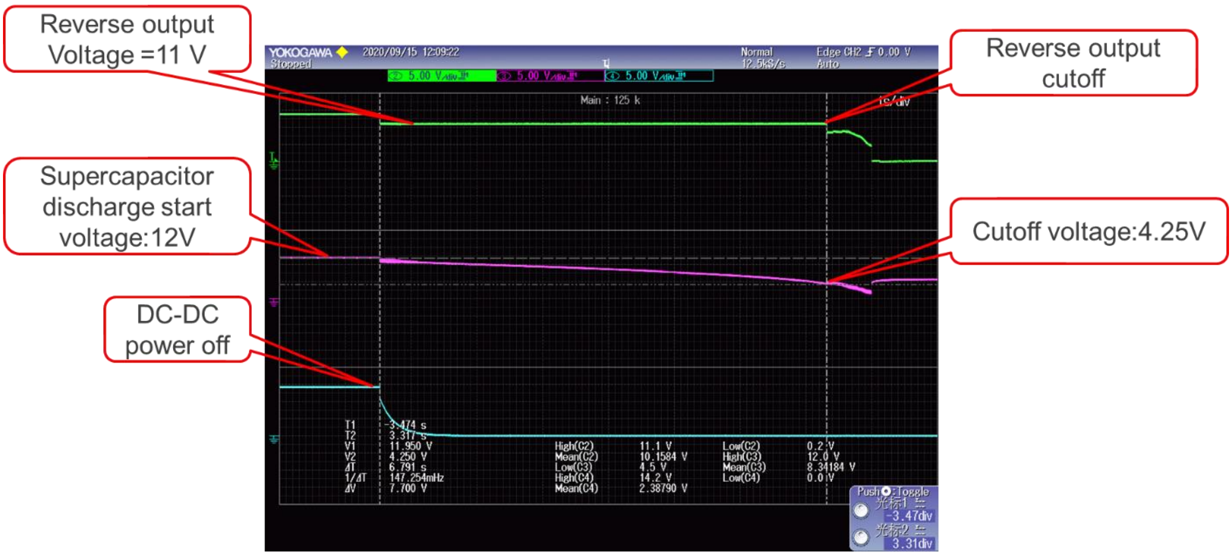

Figure 10 Discharging in CC Mode(1500mA)

- Reverse discharge mode: Electronic load set to CC mode(2000mA)
- Disharging voltage: Vout=VCAP=12V, Vin = 11V
- Discharging cut-off:3.5V, discharging time:6.791s, Efficiency: 11*2*6.791 / (0.5*2.5*12*12) = 62.25%

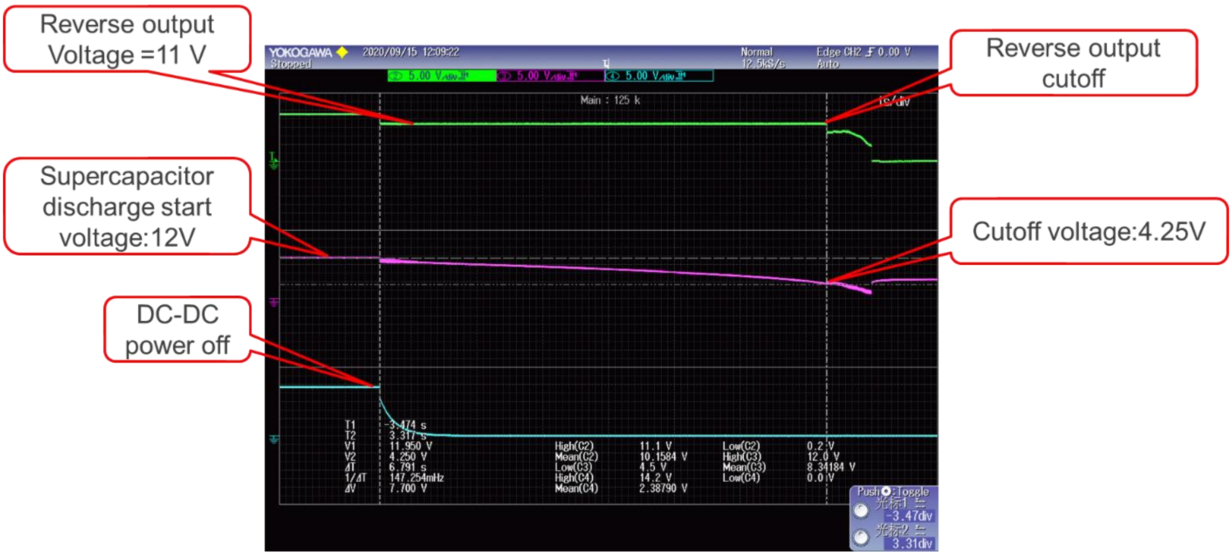

Figure 11 Discharging in CC Mode(2000mA)

CN300-SCAPBACKPOCZ Smart Terminal with Supercap by ISL81401 Circuit Schematic

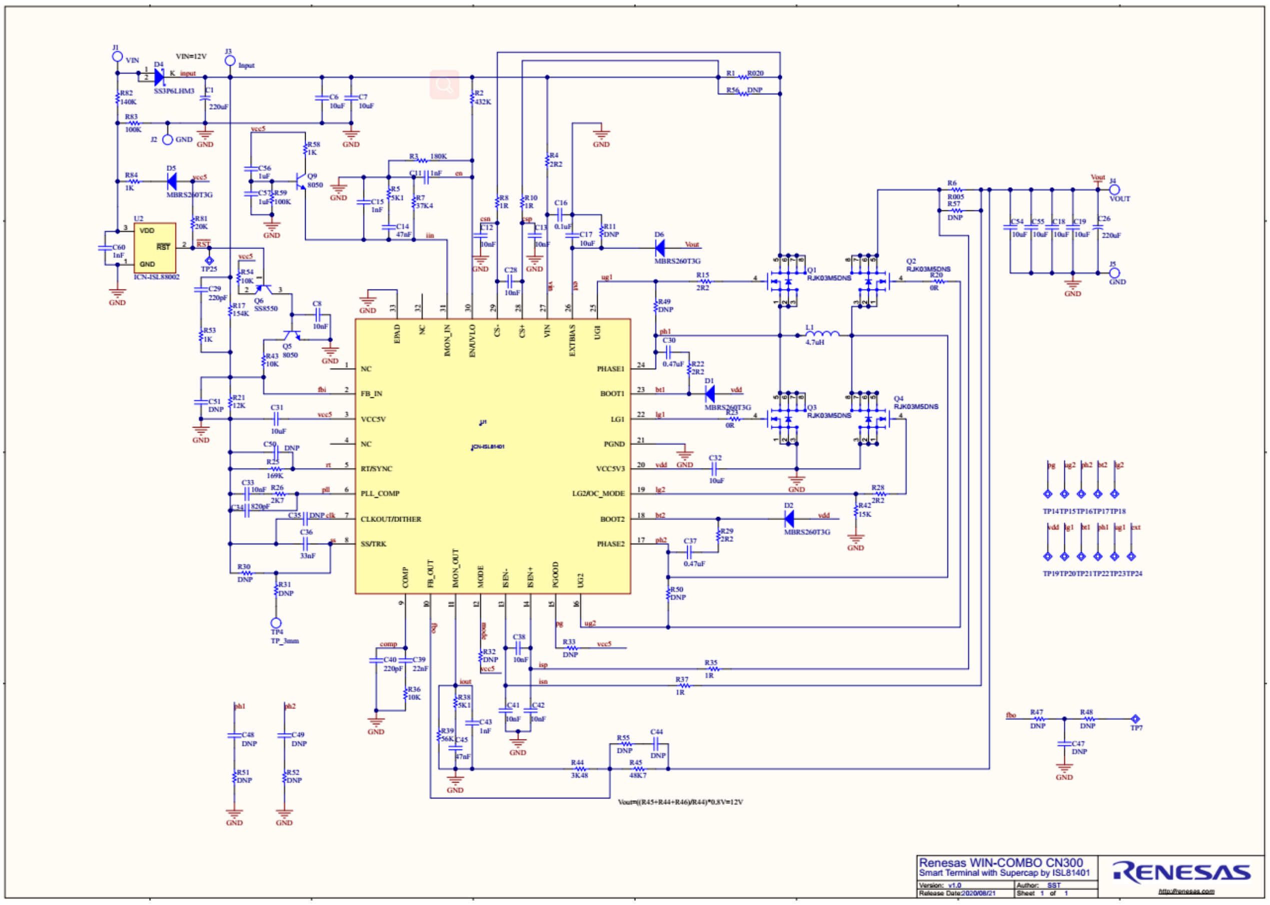

Figure 12 Circuit Schematic

Bill of Materials

TABLE 2. BOM List (1/2)

Designator	Mfg Part Number	Qty	Description	Manufacturer
C1	EKZN101ELL221MK25S	1	CAP ALUM 220UF 20% 100V RADIAL	UCC
C6, C7, C18, C19, C54, C55	GCM32EL8EH106KA07L	6	Ceramic Chip Capacitor 1206 10uF 50V	MURATA
C8, C28, C33, C38, C41, C42	GCM188R72A103KA37J	6	Ceramic Chip Capacitor 0603 10nF 100V	MURATA
C11, C15, C43, C60	GRM1885C1H102JA01D	4	Ceramic Chip Capacitor 0603 1nF 50V	MURATA
C12, C13, C16	GCM188L81H104KA57D	3	Ceramic Chip Capacitor 0603 0.1uF 50V	MURATA
C14	GCJ188R71H473KA12D	1	Ceramic Chip Capacitor 0603 47nF 50V	Murata
C17, C31, C32	GRM21BR61C106KE15L	3	Ceramic Chip Capacitor 0805 10uF 16V	MURATA
C26	EEE-FN1H221V	1	CHIP ALUM CAP 220UF 20% 50V SMD	Panasonic
C35, C44, C47, C48, C49, C50, C51		7	Ceramic Chip Capacitor 0603	
C29, C40	GCM1885C2A221JA16D	2	Ceramic Chip Capacitor 0603 220pF 100V	Murata
C30, C37	GRM188R71E474KA12D	2	Ceramic Chip Capacitor 0603 0.47uF 25V	MURATA
C34	GRM1555C1H821JA01D	1	Ceramic Chip Capacitor 0603 820pF 50V	MURATA
C36	GCM188L81H333KA55D	1	Ceramic Chip Capacitor 0603 33nF 50V	MURATA
C39	GCE188R71H223KA01D	1	Ceramic Chip Capacitor 0603 22nF 50V	MURATA
C45	GCJ188R71H473KA12D	1	Ceramic Chip Capacitor 0603 47nF 50V	MURATA
C56, C57	GRT188R61H105KE13D	2	Ceramic Chip Capacitor 0603 1uF 50V	MURATA
D1, D2, D5, D6	DSK26	4	DIODE SCHOTTKY 60V 2A SOD-123FL	MDD
D4	SS3P6LHM3	1	Schottky DIODE 60V 3A TO-227A	VISHAY
J1	KSE_7795	1	TE KSE_7795	TE
J2, J5	KSE_7795	2	TE KSE_7795	TE
J3		1	High current test terminal Hole 2.5mm	
J4	KSE_7795	1	TE KSE_7795	TE
L1	HCP0703-4R7-R	1	Power Inductor 4.7uH 10A 7*7	COOPER
Q1, Q2, Q3, Q4	RJK03M5DNS	4	MOSFET BEAM2 Series FET, 30V, HWSON3030-8	Renesas
Q5, Q9	MMSS8050	2	TRANS NPN 25V 1.5A SOT-23	MCC
Q6	MMSS8550-H-TP	1	TRANS PNP 25V 1.5A SOT-23	MCC
R1	PE1206FKM470R02Z	1	Chip Resistor Thick Film 1206 R020 1% 1/10W	YAGEO
R2	RC1206FR-07432KL	1	Chip Resistor Thick Film 1206 432K 1% 1/10W	YAGEO
R3	RC0603FR-10180KL	1	Chip Resistor Thick Film 0603 180K 1% 1/10W	YAGEO
R4, R15, R22, R28, R29	RC0603FR-072R2L	5	Chip Resistor Thick Film 0603 2R2 1% 1/10W	YAGEO
R5, R38	RC0603FR-075K1L	2	Chip Resistor Thick Film 0603 5K1 1% 1/10W	YAGEO
R6	PE1206FRM470R005L	1	Chip Resistor Thick Film 1206 R005 1% 1/10W	YAGEO
R7	RC0603FR-0737K4L	1	Chip Resistor Thick Film 0603 37K4 1% 1/10W	YAGEO
R8, R10, R35, R37	RC0603FR-071RL	4	Chip Resistor Thick Film 0603 1R 1% 1/10W	YAGEO
R11, R30, R31, R32, R33, R47, R48, R49, R50, R51, R52, R55, R56, R57	DNP	14	DNP	

TABLE 3. BOM List (2/2)

Designator	Mfg Part Number	Qty	Description	Manufacturer
R17	RC1206FR-07154KL	1	Chip Resistor Thick Film 1206154K 1% 1/10W	YAGEO
R20, R23	RC0603FR-070RL	2	Chip Resistor Thick Film 0603 0R 1% 1/10W	YAGEO
R21	RC0603FR-0712KL	1	Chip Resistor Thick Film 0603 12K 1% 1/10W	YAGEO
R25	RC0603FR-07169KL	1	Chip Resistor Thick Film 0603 169K 1% 1/10W	YAGEO
R26	RC0603FR-132K7L	1	Chip Resistor Thick Film 0603 2K7 1% 1/10W	YAGEO
R59, R83	RC0603FR-07100KL	2	Chip Resistor Thick Film 0603 100K 1% 1/10W	YAGEO
R36, R43, R54	RC0603FR-0710KL	3	Chip Resistor Thick Film 0603 10K 1% 1/10W	YAGEO
R39	RC0603FR-0756KL	1	Chip Resistor Thick Film 0603 56K 1% 1/10W	YAGEO
R42	RC0603FR-0715KL	1	Chip Resistor Thick Film 0603 15K 1% 1/10W	YAGEO
R44	RC0603FR-073K48L	1	Chip Resistor Thick Film 0603 3K48 1% 1/10W	YAGEO
R45	RC1206FR-0748K7L	1	Chip Resistor Thick Film 1206 48K7 1% 1/10W	
R53, R58, R84	RC0603FR-071KL	3	Chip Resistor Thick Film 0603 1K 1% 1/10W	YAGEO
R82,	RC0603FR-07140KL	1	Chip Resistor Thick Film 0603 140K 1% 1/10W	YAGEO
R81	RC0603FR-0720KL	1	Chip Resistor Thick Film 0603 20K 1% 1/10W	YAGEO
TP4	DNP	1	DNP	
TP7	DNP	1	DNP	
TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25	DNP	12	DNP	Keystone
U1	ISL81401FRZ	1	40V Bidirectional 4- Switch Synchronous Buck-Boost Controller	Renesas
U2	ISL88002EI31Z	1	Ultra-Low Power 3 Ld Voltage Supervisors in SC-70 and SOT-23 Packages	Renesas

Board Layout

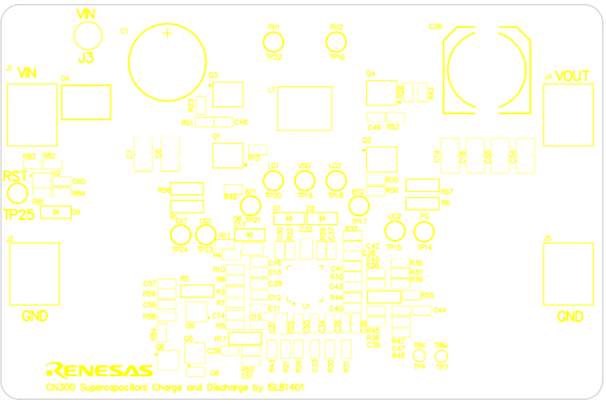

Figure 13 Silkscreen TOP

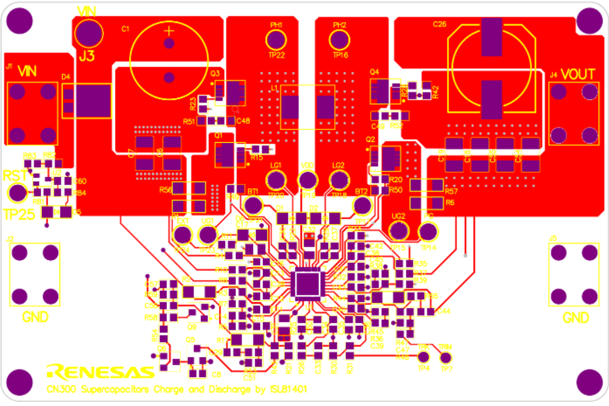

Figure 14 Top Layer

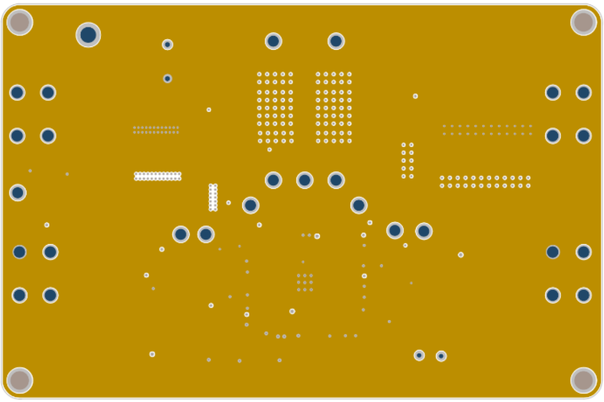

Figure 15 2nd Layer

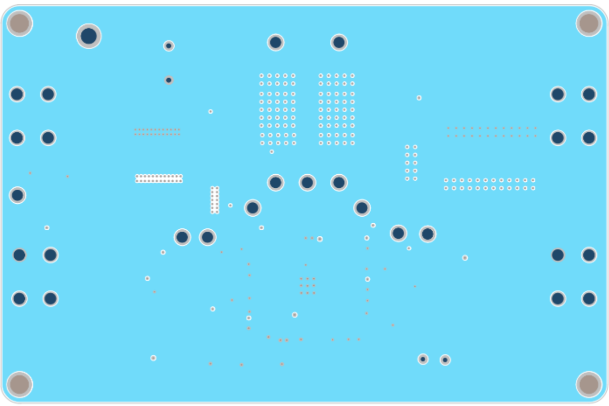

Figure 16 3rd Layer

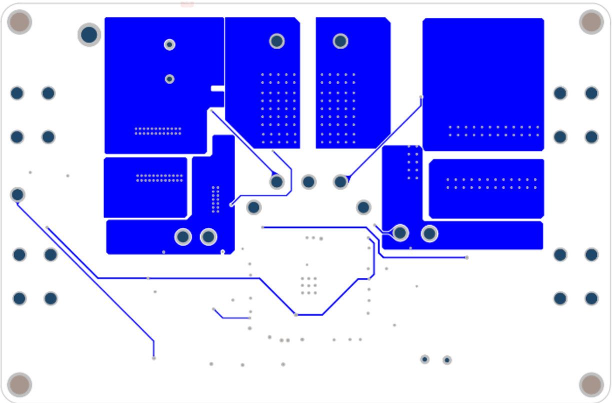

Figure 17 Bottom Layer

Revision History

Rev.	Date	Description	
		Page	Summary
0.1	Sep. 21, 2020	—	First edition issued

General Precautions in the Handling of Micro processing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Micro processing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced near the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a micro processing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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