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Renesas Electronics Corporation

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User's Manual

Renesas Starter Kit LCD Application Board

User's Manual

RENESAS STARTER KIT

Renesas Electronics
www.renesas.com

Rev.2.00 2007.11

Table of Contents

Chapter 1. Preface

Cautions

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Glossary

CPU	Central Processing Unit	RTE	Renesas Technology Europe Ltd.
HEW	High-performance Embedded Workshop	RSO	Renesas Solutions Organisation.
LCD	Liquid Crystal Display	RSK	Renesas Starter Kit
PC	Program Counter	E8A	E8a On-chip debugger module

Chapter 2.Purpose

This RSK Application Board is an evaluation tool for Renesas microcontrollers with an LCD driver interface. It is used in conjunction with the RSK for the microcontroller to be evaluated.

Features include:

- Mounting connections to allow RSK to be added to top of board.
- Interface to standard RSK LCD expansion connector and RSK expansion connections.
- 8 character 14 segment “starburst” LCD.
- Coin cell holder to power mounted RSK for low power operation.

Chapter 3.Board Layout

3.1.Component References

The following diagram shows the component references for the board.

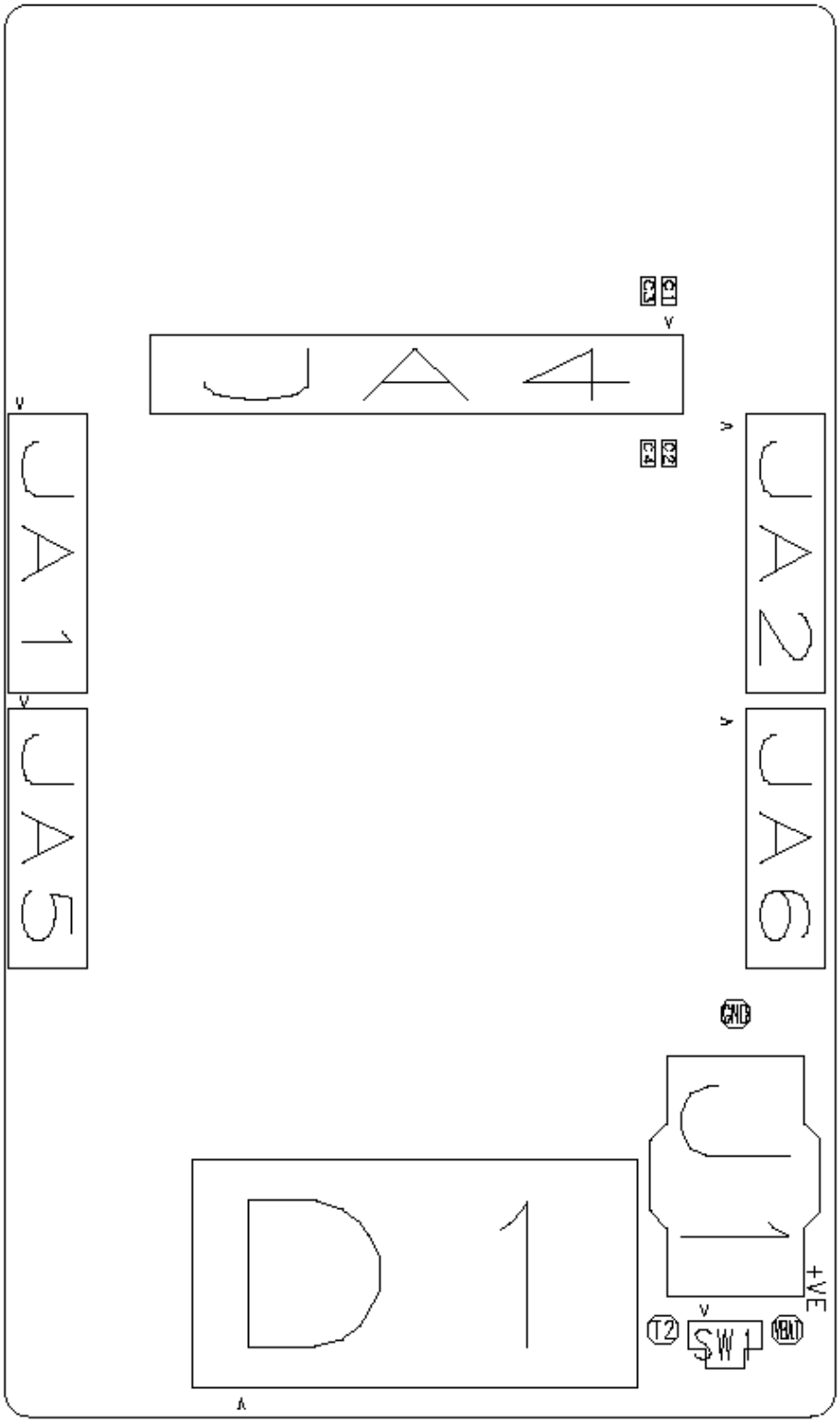

Figure 3-1: Component References

3.2.Board Component functions

The following diagram the shows the functions of the components on the board.

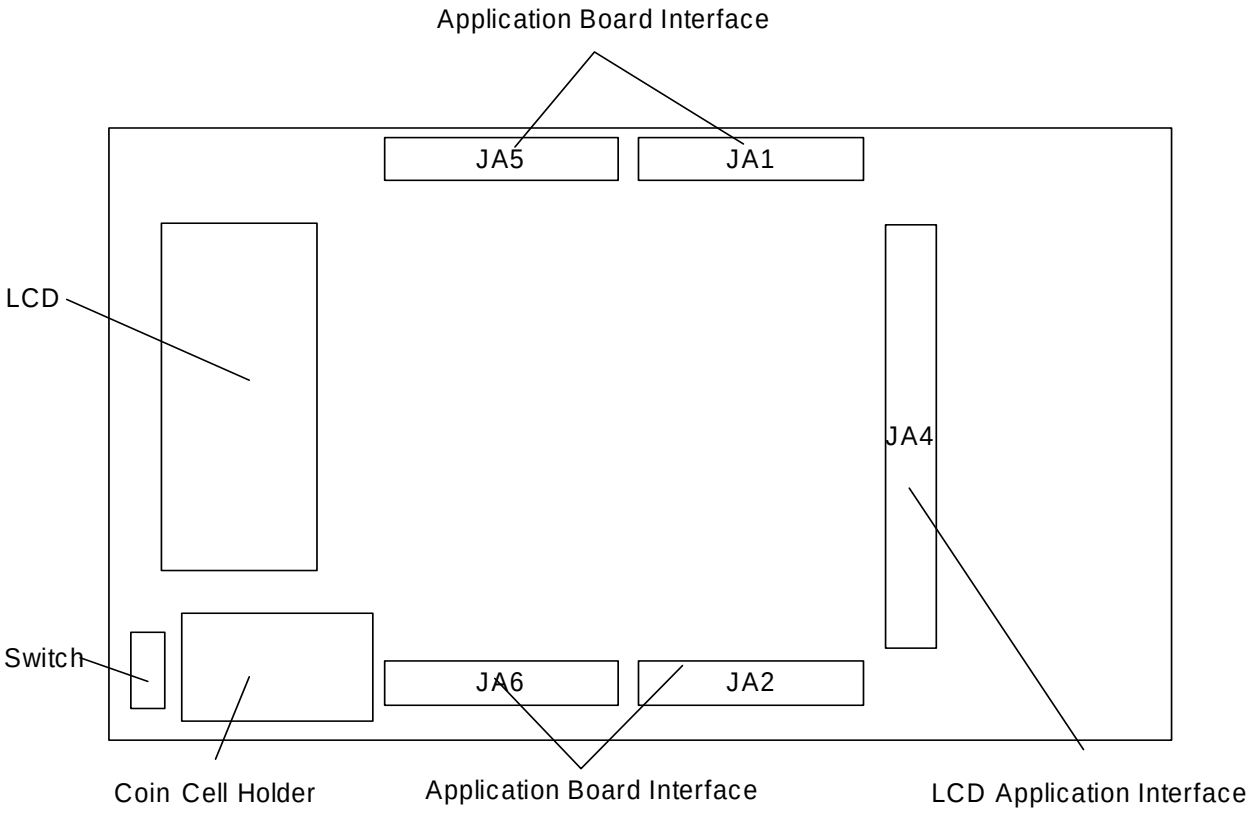

Figure 3-2: Board Layout

Caution: If processor is not in low power mode at start up the battery life will be significantly reduced.

3.3.Board Dimensions

The following diagram gives the board dimensions and connector positions. All through hole connectors are on a common 0.1” grid for easy interfacing.

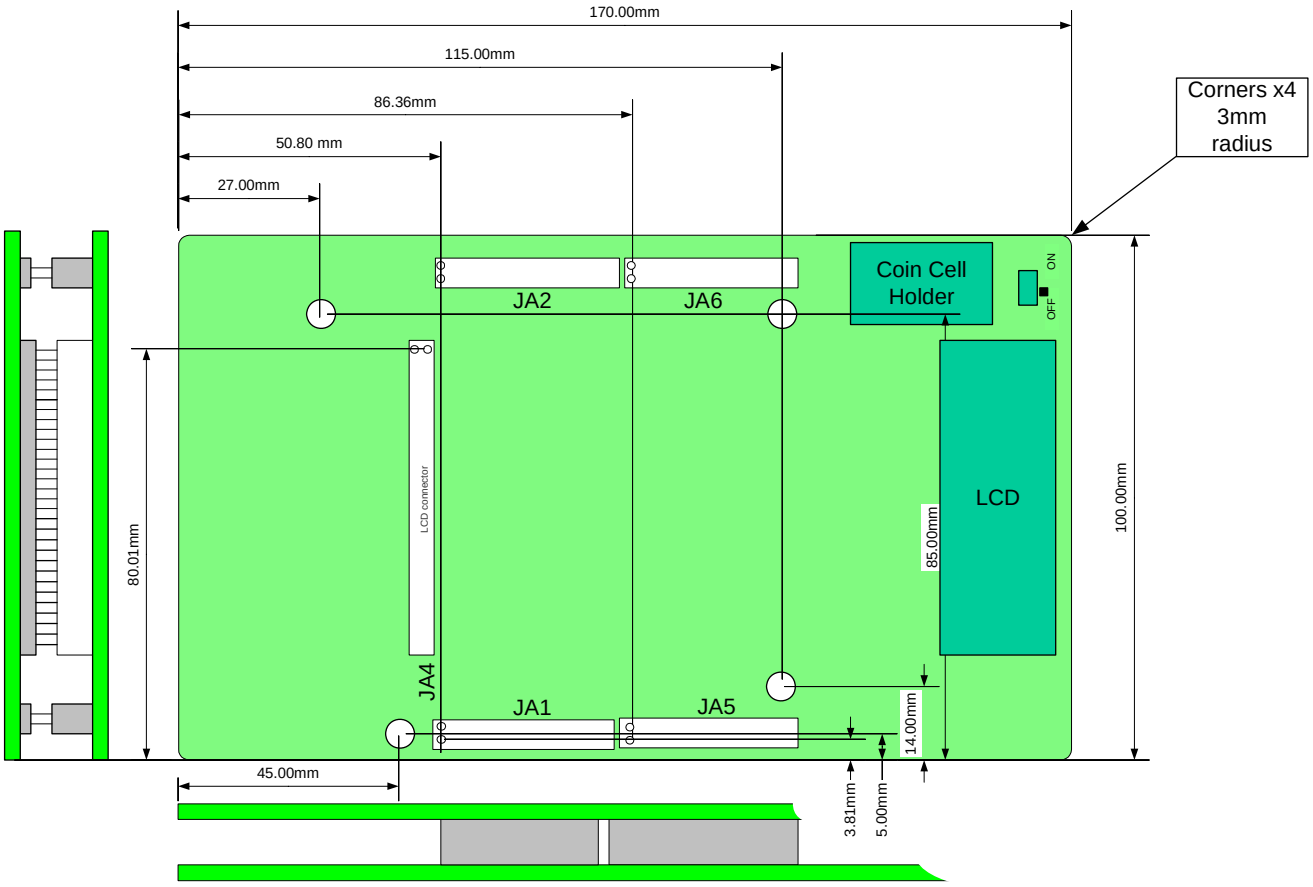

Figure 3-3 : Board Dimensions

Chapter 4.User Circuitry

4.1.Fitting the Target RSK to the RSK LCD application board

The board is supplied with 2x 24 way sockets, 2x 26 way sockets and 1 x 50 way socket.

These should be soldered on the underside of the host RSK in JA1, JA2, JA5, JA6 and JA4 positions.

The RSK should be plugged into the equivalent connectors on the RSK LCD application board.

4.2.LCD Module

The LCD module on the board is connected to the RSK LCD connector JA4.

It uses ¼ duty cycle and has 4 common lines. There are 8x14 segment starburst characters. Refer to Figure 4-1: LCD Segment Names.

Each character uses 4 SEG lines. Each SEG line controls 4 segments on the LCD as it uses ¼ duty cycle.

The LCD controller must be programmed for ¼ duty cycle.

In the case of the H838347, a RAM in the LCD controller has 1 bit per segment. Thus each character is a 16 bit number.

The following Table 4-1: LCD character maps gives the bit mappings for common characters for this controller.

The lowest address (H'F740 in the case of the H838347) represents the rightmost character of the display.

The next word address (H'F742 in the case of the H838347) represents the next character, etc.

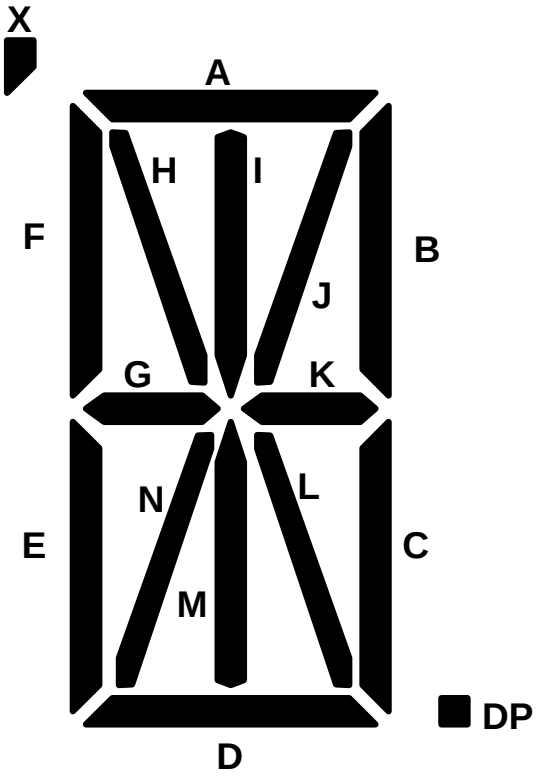

Figure 4-1: LCD Segment Names

Segment	L	K	J	I	DP	C	B	A	D	E	F	X	M	N	G	H	
Bit number	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Hex value for RAM
A	0	1	0	0	0	1	1	1	0	1	1	0	0	0	1	0	4762
B	1	0	1	0	0	0	0	1	1	1	1	0	0	0	1	0	A1E2
C	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	01E0
D	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0065
E	0	1	0	0	0	0	0	1	1	1	1	0	0	0	1	0	41E2
F	0	1	0	0	0	0	0	1	0	1	1	0	0	0	1	0	4162
G	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	81E0
H	0	1	0	0	0	1	1	0	0	1	1	0	0	0	1	0	4662
I	0	0	0	1	0	0	0	1	1	0	0	0	1	0	0	0	1188
J	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0680
K	1	0	1	0	0	0	0	0	0	1	1	0	0	0	1	0	A062
L	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	00E0
M	0	0	1	0	0	1	1	0	0	1	1	0	0	0	0	1	2661
N	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	1	8661
O	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	07E0
P	0	1	0	0	0	0	1	1	0	1	1	0	0	0	1	0	4362
Q	1	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	87E0
R	1	1	0	0	0	0	1	1	0	1	1	0	0	0	1	0	C362
T	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1108
S	0	1	0	0	0	1	0	1	1	0	1	0	0	0	1	0	45A2
U	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	06E0
V	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	8601
W	1	0	0	0	0	1	1	0	0	1	1	0	0	1	0	0	8664
X	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	A005
Y	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	2009
Z	0	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0	2184
0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	07E0
1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1008
2	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	0	43C2
3	0	1	0	0	0	1	1	1	1	0	0	0	0	0	1	0	4782
4	0	1	0	0	0	1	1	0	0	0	1	0	0	0	1	0	4622
5	0	1	0	0	0	1	0	1	1	0	1	0	0	0	1	0	45A2
6	0	1	0	0	0	1	0	1	1	1	1	0	0	0	1	0	45E2
7	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0700
8	0	1	0	0	0	1	1	1	1	1	1	0	0	0	1	0	47E2
9	0	1	0	0	0	1	1	1	1	0	1	0	0	0	1	0	47A2
?	0	1	0	0	0	0	1	1	0	0	1	0	1	0	0	0	4328

Table 4-1: LCD character maps

4.3.Coin Cell and switch.

The board includes a coin cell holder to hold a 2032 3.6V coin cell. To power the attached RSK from this cell the switch must be in the "ON" position.

IT IS IMPORTANT NOT TO POWER THE ATTACHED RSK VIA THE POWER SUPPLY JACK OR VIA THE E8A IF THIS OPTION IS USED.

Caution: If processor is not in low power mode at start up the battery life will be significantly reduced.

4.4.Capacitors

Pads are supplied to allow 0603 capacitors to be placed on the LCD drive voltages V1 – V4.

Chapter 5.Headers

5.1.Application Headers

This information is supplied for reference. Only JA1 pin 3 (battery supply voltage to RSK) and the ground pins are connected on this board.

Table 5-1 and Table 5-2 below show the standard application header connections.

JA1							
Pin	Generic Header Name		CPU board Signal Name	Pin	Header Name		CPU board Signal Name
1	Regulated Supply 1		5V	2	Regulated Supply 1		GROUND
3	Regulated Supply 2		3V3	4	Regulated Supply 2		GROUND
5	Analogue Supply		AVcc	6	Analogue Supply		AVss
7	Analogue Reference		AVref	8	ADTRG		ADTRG
9	ADC0	I0	AD0	10	ADC1	I1	AD1
11	ADC2	I2	AD2	12	ADC3	I3	AD3
13	DAC0		DAC0	14	DAC1		DAC1
15	IOPort		IO_0	16	IOPort		IO_1
17	IOPort		IO_2	18	IOPort		IO_3
19	IOPort		IO_4	20	IOPort		IO_5
21	IOPort		IO_6	22	IOPort		IO_7
23	Open drain	IRQAEC	IRQ3	24	I²C Bus - (3rd pin)		IIC_EX
25	I²C Bus		IIC_SDA	26	I²C Bus		IIC_SCL

Table 5-1: JA1 Standard Generic Header

JA2						
Pin	Generic Header Name		CPU board Signal Name	Pin	Header Name	CPU board Signal Name
1	Open drain		RESn	2	External Clock Input	EXTAL
3	Open drain		NMIn	4	Regulated Supply 1	Vss1
5	Open drain output		WDT_OVF	6	Serial Port	SCIaTX
7	Open drain	WUP	IRQ0	8	Serial Port	SCIaRX
9	Open drain		IRQ1	10	Serial Port	SCIaCK
11	Up/down		MO_UD	12	Serial Port Handshake	CTS/RTS
13	Motor control		MO_Up	14	Motor control	MO_Un
15	Motor control		MO_Vp	16	Motor control	MO_Vn
17	Motor control		MO_Wp	18	Motor control	MO_Wn
19	Output		TMR0	20	Output	TMR1
21	Input		TRIGa	22	Input	TRIGb
23	Open drain		IRQ2	24	Tristate Control	TRSTn
25	SPARE		-	26	SPARE	-

Table 5-2: JA2 Standard Generic Header

Table 5-3 and Table 5-4 below show the optional generic header connections

JA5							
Pin	Generic Header Name		CPU board Signal Name	Pin	Header Name		CPU board Signal Name
1	ADC4	I4	AD4	2	ADC5	I5	AD5
3	ADC6	I6	AD6	4	ADC7	I7	AD7
5	CAN		CAN1TX	6	CAN		CAN1RX
7	CAN		CAN2TX	8	CAN		CAN2RX
9	Reserved			10	Reserved		
11	Reserved			12	Reserved		
13	Reserved			14	Reserved		
15	Reserved			16	Reserved		
17	Reserved			18	Reserved		
19	Reserved			20	Reserved		
21	Reserved			22	Reserved		
23	Reserved			24	Reserved		

Table 5-3: JA5 Optional Generic Header

JA6							
Pin	Generic Header Name		CPU board Signal Name	Pin	Header Name		CPU board Signal Name
1	DMA		DREQ	2	DMA		DACK
3	DMA		TEND	4	Standby (Open drain)		STBYn
5	Host Serial	SCIdTX	RS232TX	6	Host Serial	SCIdRX	RS232RX
7	Serial Port		SCIbRX	8	Serial Port		SCIbTX
9	Serial Port	Synchronous	SCIcTX	10	Serial Port		SCIbCK
11	Serial Port	Synchronous	SCIcCK	12	Serial Port	Synchronous	SCIcRX
13	Reserved			14	Reserved		
15	Reserved			16	Reserved		
17	Reserved			18	Reserved		
19	Reserved			20	Reserved		
21	Reserved			22	Reserved		
23	Reserved			24	Reserved		

Table 5-4: JA6 Optional Generic Header

Table 5-5 below shows the LCD header connections

JA4					
Pin	Generic Header Name	Signal Name	Pin	Header Name	Signal Name
1	V0	V0	2	V1	V1
3	V2	V2	4	V3	V3
5	GROUND	GROUND	6	GROUND	GROUND
7	COM1	COM1	8	COM2	COM2
9	COM3	COM3	10	COM4	COM4
11	SEG1	SEG1	12	SEG2	SEG2
13	SEG3	SEG3	14	SEG4	SEG4
15	SEG5	SEG5	16	SEG6	SEG6
17	SEG7	SEG7	18	SEG8	SEG8
19	SEG9	SEG9	20	SEG10	SEG10
21	SEG11	SEG11	22	SEG12	SEG12
23	SEG13	SEG13	24	SEG14	SEG14
25	SEG15	SEG15	26	SEG16	SEG16
27	SEG17	SEG17	28	SEG18	SEG18
29	SEG19	SEG19	30	SEG20	SEG20
31	SEG21	SEG21	32	SEG22	SEG22
33	SEG23	SEG23	34	SEG24	SEG24
35	SEG25	SEG25	36	SEG26	SEG26
37	SEG27	SEG27	38	SEG28	SEG28
39	SEG29	SEG29	40	SEG30	SEG30
41	SEG31	SEG31	42	SEG32	SEG32
43	SEG33	SEG33	44	SEG34	SEG34
45	SEG35	SEG35	46	SEG36	SEG36
47	SEG37	SEG37	48	SEG38	SEG38
49	SEG39	SEG39	50	SEG40	SEG40

Table 5-5: JA4 LCD Expansion connector

Chapter 6.Code Development

RSKs with appropriate LCD connections will include suitable sample software to drive the LCD on this board. Section 4.2 includes details of bit mapping for the LCD segments.

Chapter 7.Additional Information

For details on how to use High-performance Embedded Workshop (HEW), refer to the HEW manual available on the CD or from the web site.

Online technical support and information is available at: http://www.renesas.com/renesas_starter_kits

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