RTKA226110DE0010BU

Evaluation Board

This user manual discusses the RTKA226110DE0010BU with GS66508B GaN E-HEMT daughter board and GS665MB-EVB evaluation platform. The RTKA226110DE0010BU is a gate drive evaluation board following the GS665XXX-EVBDB daughter board style and uses the RAA226110 device. This evaluation board consists of two GaN Systems 650V GaN Enhancement-mode HEMTs (E-HEMTs) and all necessary circuits including half-bridge gate drivers, isolated power supplies, and an optional heatsink to form a functional half-bridge power stage. It allows you to evaluate the GaN E-HEMT performance in any half-bridge-based topology, either with the universal mother board (GS665MB-EVB) or your own system design. The RTKA226110DE0010BU evaluation board provides a 0V turn-off voltage solution. A 0V turn-off solution is normally used in low power applications. A 0V turn-off solution is easy to implement as there is no need for a negative power supply rail and the reverse conduction voltage drop of GaN is lower. For the E-mode GaN device, the V_{GS} threshold voltage is low (typical 1.7V). A 0V turn-off has the risk of false turn-on when the GaN device is in an off state. Also, the switching-off loss is higher than the negative turn-off voltage. The 0V turn-off solution is normally used in low power applications.

Read the entire user manual and, specifically, the warnings and restrictions notices before handling the product. Persons handling the product(s) must have electronics training and observe good engineering practice standards.

Features

- Serves as a reference design and evaluation tool in addition to a deployment-ready solution for easy in-system evaluation.
- Vertical mount style with the height of 35mm that fits in the majority of 1U designs and allows evaluation of a GaN E-HEMT in traditional through-hole type power supply board.
- Current shunt position for switching characterization testing
- Universal form factor and footprint for all products
- 0V turn off voltage

Related Literature

For a full list of related documents, visit our website:

- RAA226110 device page

Ordering Information

Part Number	Description
RTKA226110DE0010BU	RAA226110 evaluation board

	**DANGER!** This evaluation board is designed for engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY. High voltage is exposed on the board during the test and even brief contact during operation may result in severe injury or death. Never leave the board operating unattended. After it is de-energized, always wait until all capacitors are discharged before touching the board.
	**CAUTION**: This product contains parts that are susceptible to damage by Electrostatic Discharge (ESD). Always follow ESD prevention procedures when handling the product.

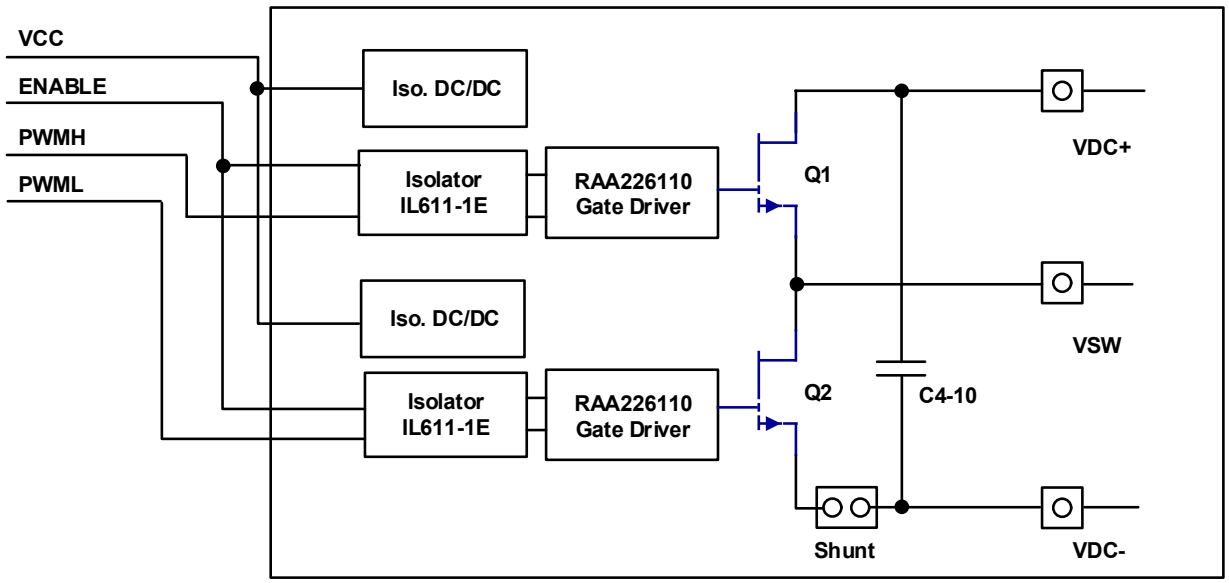


Figure 1. RTKA226110DE0010BU Evaluation Board Block Diagram

1. Functional Description

1.1 Control and Power I/Os:

The daughter board RTKA226110DE0010BU circuit diagram is shown in Figure 1. The control logic inputs on the 2x3 pin header J1 are listed in Table 1.

Table 1. Control Pins

Pin	Description
ENABLE	Enable input. It is internally pulled up to VCC, a low logic disables all the PWM gate drive outputs.
+5V	+5V auxiliary power supply input for logic circuit and gate driver. On the daughter board there are two isolated 5V to 9V DC/DC power supplies for top and bottom switches.
VDRV	Not used. VDRV can be connected to VCC though R43. R43 is DNP by default.
PWMH_IN	High-side PWM logic input for top switch Q1. It is compatible with 3.3V and 5V.
PWML_IN	Low-side PWM logic input for bottom switch Q2. It is compatible with 3.3V and 5V.
0V	Logic inputs and gate drive power supply ground return.

The three power pins are:

- VDC+: Input DC Bus voltage
- VSW: Switching node output
- VDC-: Input DC bus voltage ground return. **Note:** Control ground 0V is isolated from VDC-

1.2 Using RTKA226110DE0010BU with Universal Mother Board GS665MB-EVB

GaN Systems provides a universal 650V mother board (ordering part number: GS665MB-EVB, sold separately) that can be used as the basic evaluation platform for all applicable daughter boards.

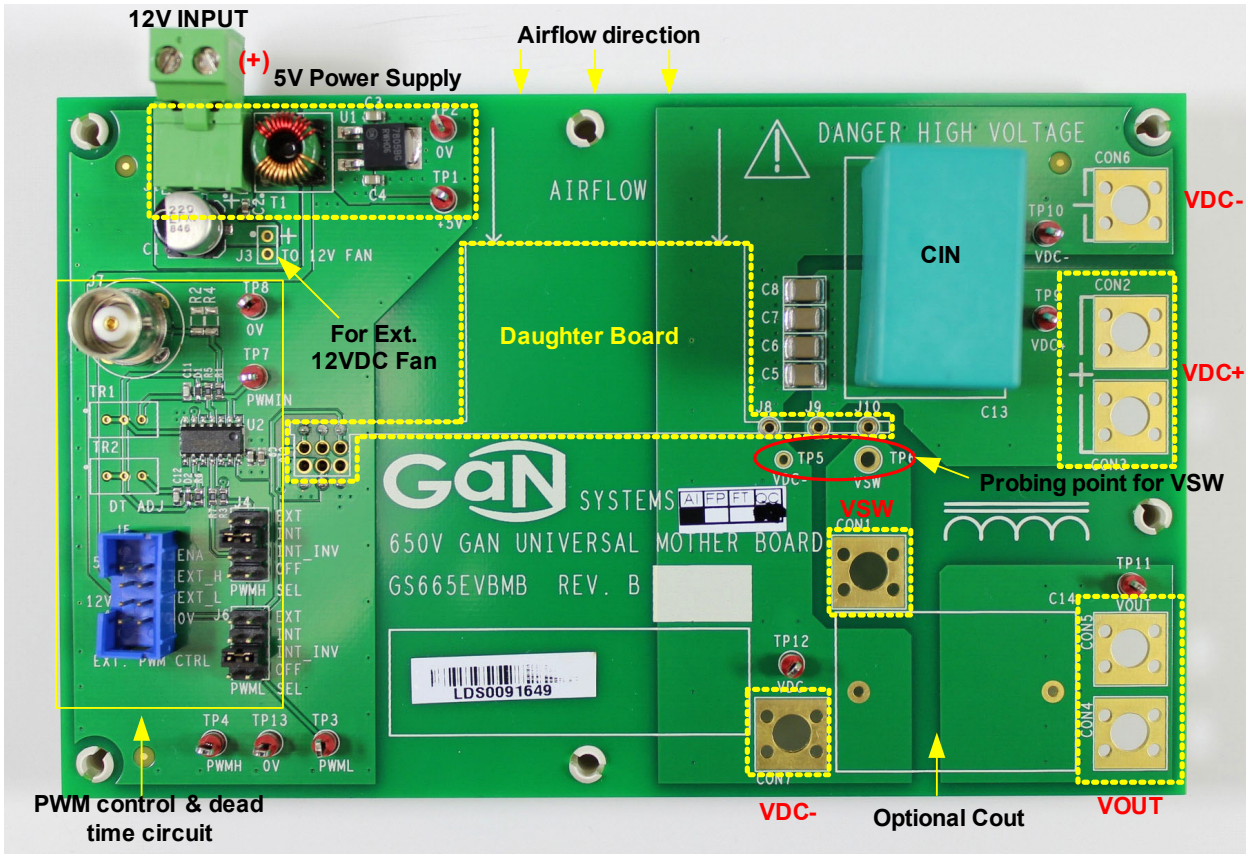


Figure 2. 650V Universal Mother Board GS665MB-EVB

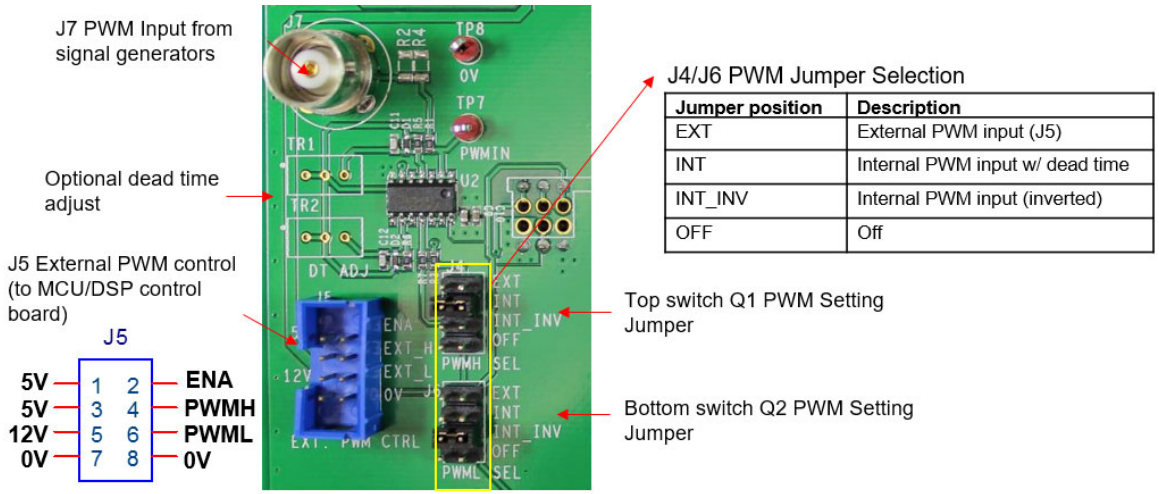
The universal 650V mother board evaluation kit includes the following items:

- Mother board GS665MB-EVB
- $12V_{DC}$ Fan

1.2.1 12V Input

The mother board can be powered by 9V to 12V on J1. The on-board voltage regulator creates 5V for the daughter board and control logic circuits. J3 is used for the external $12V_{DC}$ fan.

1.2.2 PWM Control Circuit



Jumper position	Description
EXT	External PWM input (J5)
INT	Internal PWM input w/ dead time
INT_INV	Internal PWM input (inverted)
OFF	Off

Figure 3. PWM Control Input and Dead Time Circuit

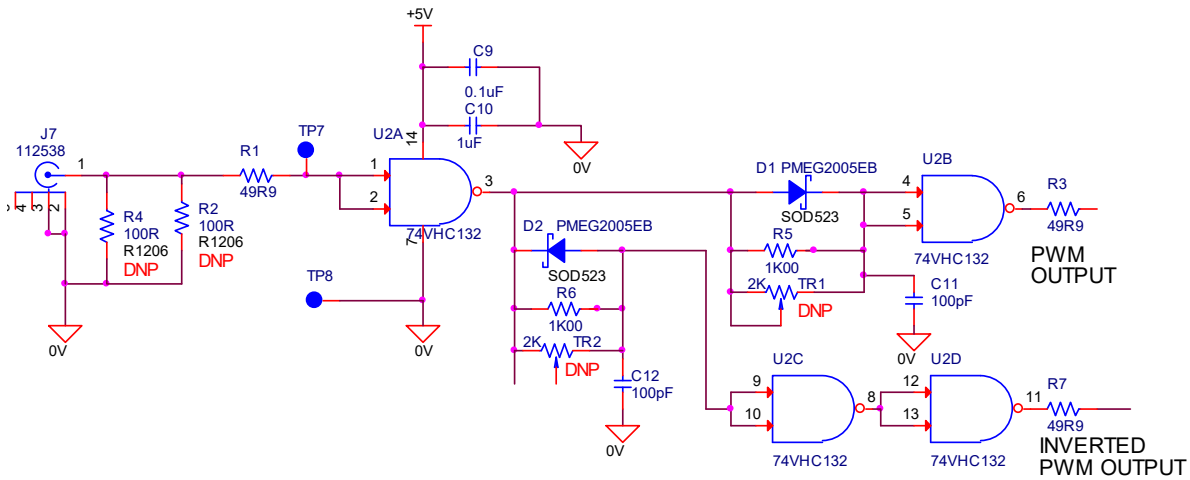


Figure 4. On-Board Dead Time Generation Circuit

The top and bottom switches (PWM inputs) can be individually controlled by two jumpers, J4 and J6. You can choose between a pair of complementary on-board internal PWM signals (non-inverted and inverted, controlled by J7 input) with dead time or an external high-side/low-side drive signals from J5 (your own control board).

An on-board dead time generation circuit is included on the mother board. Dead time is controlled by two RC delay circuits, R6/C12 and R5/C11. The default dead time is set to about 100ns. Additionally, two potentiometer locations are provided (TR1/TR2, not included) to allow fine adjustment of the dead time, if needed.

WARNING!
ALWAYS double check the jumper setting and PWM gate drive signals before applying power. Incorrect PWM inputs or jumper settings may cause device failures

1.2.3 Test Points

Test points are designed in groups/pairs to facilitate probing.

Table 2. Test Points

Test points	Name	Description
TP1/TP2	+5V/0V	5V bias power
TP7/TP8	PWMIN/0V	PWM input signal from J7
TP4/TP3/TP13	PWMH/PWML/0V	High-side/low-side gate signals to daughter board
TP9/TP10	VDC+/VDC-	DC bus voltage
TP11/TP12	VOUT/VDC-	Output voltage
TP6/TP5	VSW/VDC-	Switching node output voltage (for HV oscilloscope probe)

1.2.4 Power Connections

The CON1-CON7 mounting pads are compatible with following mounting terminals:

- #10-32 Screw mount
- Banana Jack PCB mount (Keystone P/N: 575-4)
- PC Mount Screw Terminal (Keystone P/N: 8191)

1.2.5 Output Passives (L and C14)

An external power inductor (not included) can be connected between VSW (CON1) and VOUT (CON4/5) or VDC+ (CON2/3) for double pulse test. You can choose your inductor size to meet the test requirement. Renesas recommends using a power inductor with low inter-winding capacitance to obtain best switching performance. For the double pulse testing, use 2x 60µH/40A inductor (CWS, HF467-600M-40AV) in series. C14 accommodates a film capacitor as an output filter.

1.2.6 Double Pulse Test Mode

The double pulse test allows evaluation of the device switching performance at high voltage/current without the need of actually running at high power. It is also used for the switching loss (Eon/Eoff) measurement and other switching characterization parameter tests.

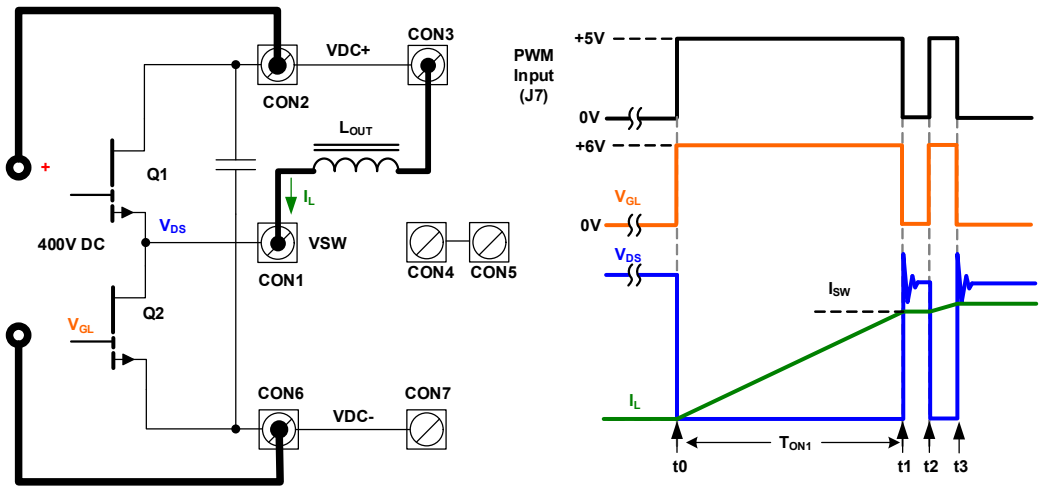


Figure 5. Double Pulse Test Setup

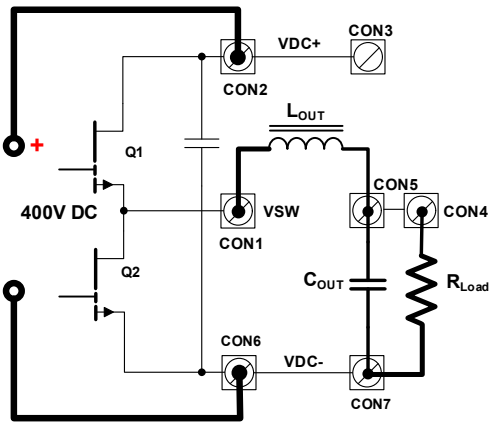
The circuit configuration and operating principle is shown in Figure 5.

- The output inductor is connected to the VDC+.
- At t0 when Q2 is switched on, the inductor current starts to ramp up until t1. The period of first pulse T_{ON1} defines the switching current $I_{SW} = (V_{DS} * T_{ON1}) / L$.
- t1-t2 is the free wheeling period when the inductor current I_L forces Q1 to conduct in reverse.
- t1 (turn-off) and t2 (turn-on) are of interest for this test because they are the hard switching transients for the half-bridge circuit when Q2 is under high switching stress.
- Keep the second pulse t2-t3 short to limit the peak inductor current at t3.

The double pulse signal can be generated using a programmable signal generator or microcontroller/DSP board. Because this test involves high switching stress and high current, Renesas recommends setting the double pulse test gate signal as a single trigger mode or use a long repetition period (for example >50ms-100ms) to avoid excess stress to the switches. Q1 can be kept off during the test or driven synchronously (J4 set to OFF or INT_INV) and Q2 is set to INT (or EXT position if the PWM signal is from J5).

WARNING!
Limit the maximum switching test current to 30A and ensure maximum drain voltage including ringing is below 650V for pulse testing. Exceeding this limit may cause damage to the devices.

1.2.7 Buck/Standard Half-Bridge Mode



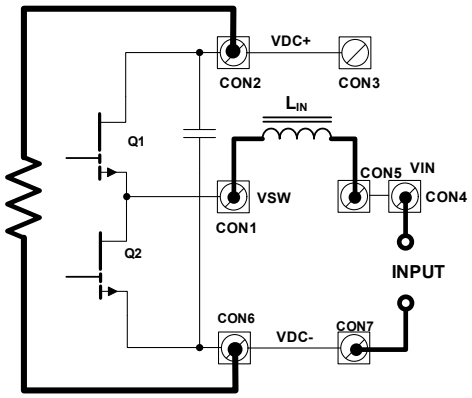
This is a standard half-bridge configuration that can be used in the following circuits:

- Synchronous Buck DC/DC
- Single phase half-bridge inverter
- ZVS half-bridge LLC
- Phase leg for full bridge DC/DC or
- Phase leg for a 3-phase motor drive

Jumper setting:

- J4 (Q1): INT
- J6 (Q2): INT_INV

1.2.8 Boost Mode



When the output becomes the input and the load is attached between VDC+ and VDC-, the board is converted into a boost mode circuit and can be used for the following:

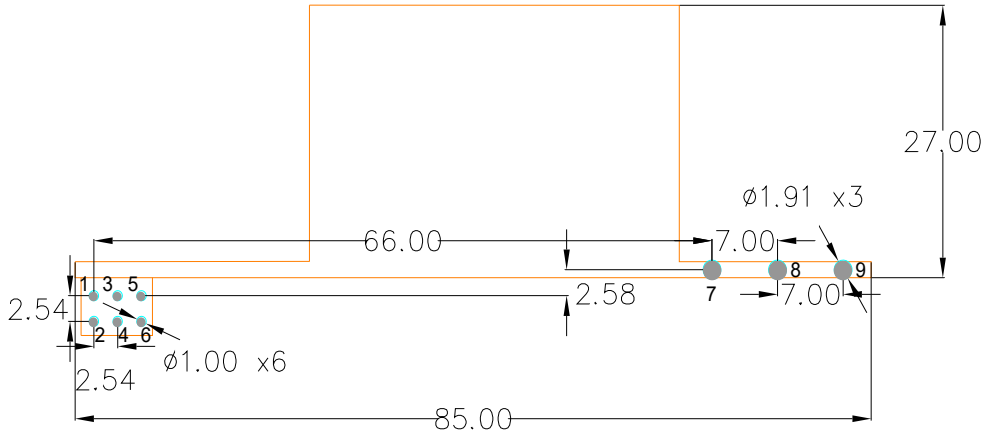
- Synchronous Boost DC/DC
- Totem pole bridgeless PFC

Jumper setting:

- J4 (Q1): INT_INV
- J6 (Q2): INT

1.3 Using RTKA226110DE0010BU in System

The daughter board allows you to evaluate the GaN performance in your own systems. See the footprint drawing of RTKA226110DE0010BU shown in Figure 6.



1. All units are in mm.
2. Pin 1-6: Dia. 1mm
3. Pin 7-9: 1.91mm (75mil) mounting hole for Mill-max Receptacle P/N: 0312-0-15-15-34-27-10-0.

Figure 6. Recommended Footprint Drawing of Daughter Board

1.4 Quick Start Procedure – Pulses Test

The following equipment and components are required:

- Four-channel oscilloscope with 500MHz bandwidth or higher
- High bandwidth (500MHz or higher) passive probe
- High bandwidth (500MHz) high voltage probe (>600V)
- AC/DC current probe for inductor current measurement
- 12V DC power supply
- Signal generator capable of creating testing pulses
- High voltage power supply (0-400VDC) with current limit.
- External power inductor (recommend toroid inductor 50-200µH)

The following are the instructions to quickly get started with your evaluation of the GaN E-HEMT.

1. Check position E (Figure 10) on the RTKA226110DE0010BU daughter board.
2. Install RTKA226110DE0010BU on the mother board. Press all the way down until you feel a click. Connect the probe between TP8 (low-side GaN gate) and TP3 (low-side GaN source) for gate voltage measurement in the daughter board.
3. Set up the mother board
   a. Connect $12V_{DC}$ bias supply to J1.
   b. Connect PWM input gate signal (0-5V) to J7. If it is generated from a signal generator, ensure the output mode is high-Z mode.
   c. Set J4 to OFF position and J7 to INT.
   d. Set the High Voltage (HV) DC supply voltage to 0V and ensure the output is OFF. Connect the HV supply to CON2 and CON6.
   e. Use the HV probe between TP6 and TP5 for V_{DS} measurement.

f. Connect an external inductor between CON1 and CON3. Use the current probe to measure the inductor current (I_L).

4. Set up and check the PWM gate signal
   a. Turn on the $12V_{DC}$ power.
   b. Check the two LEDs on the daughter board. They should be turned on indicating the isolated 9V is present.
   c. Set up the signal generator as shown in Figure 5 to create the waveforms. Use equation $I_{SW} = (V_{DS} * T_{ON1}) / L$ to calculate the pulse width of the first pulse and ensure the I_{SW_MAX} is ≤40A at $400V_{DC}$.
   d. Set the operation mode to either Single Trigger or Burst mode with repetition periods of 100ms.
   e. Turn on the PWM output and check on the oscilloscope to make sure the GaN gate drive voltage waveform is present and matches the PWM input.
5. Power on
   a. Turn on the output of the HV supply. Start with low voltage and slowly ramp the voltage up until it reaches $400V_{DC}$. During the ramping period, closely observe the voltage and current waveforms on the oscilloscope.
6. Power off
   a. After the test is complete, slowly ramp down the HV supply voltage to 0V and turn off the output. Then turn off the 12V bias supply and signal generator output.

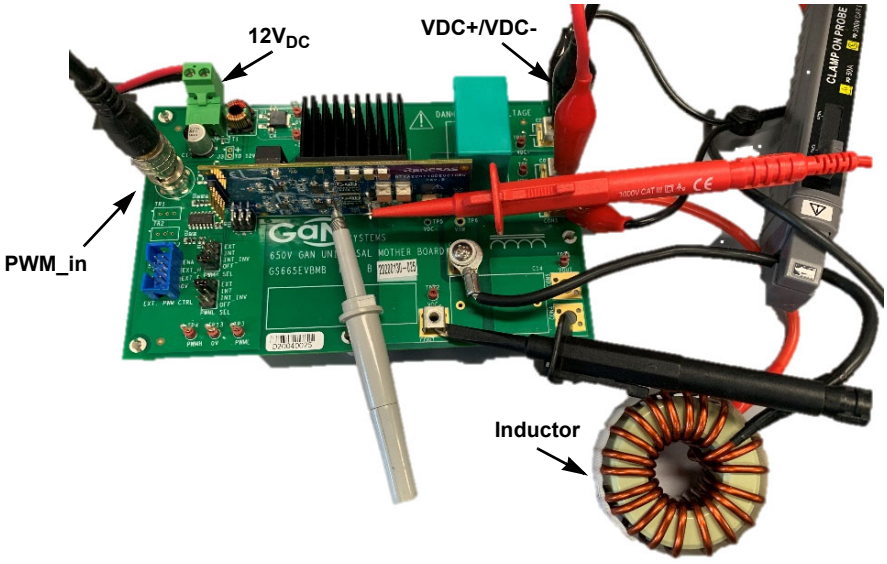


Figure 7. Pulses Test Setup Example

1.5 Test Results

Pulses test (V_{DS} = 400V, IMAX = 33A, Lp = 120µH, $R_{G(ON)}$ = 0Ω, IGSEL is connected to VDRV, Gate driver current is 0.3A, $R_{G(OFF)}$ =1Ω, 8 pulses, period = 4µs, duty = 50%).

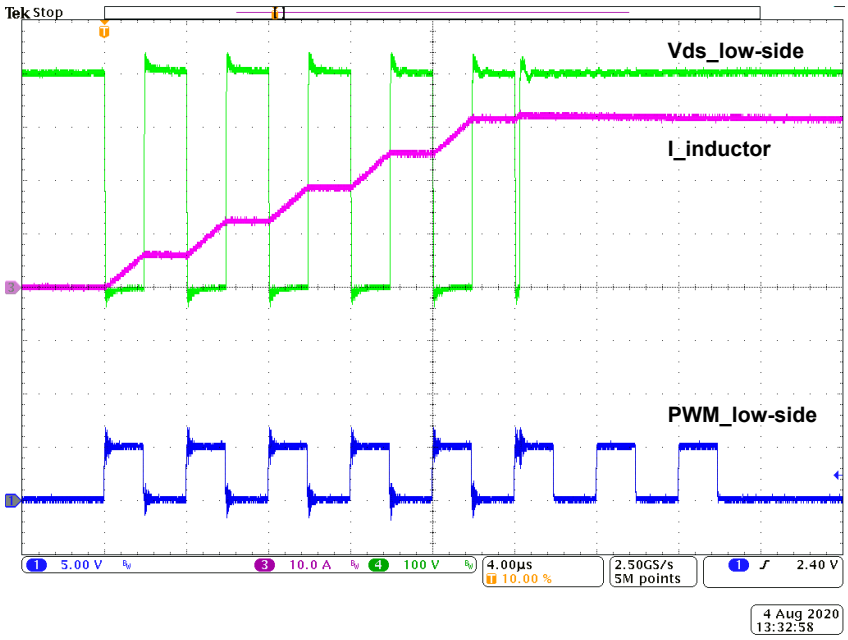


Figure 8. 400V/33A Pulses Test Waveform

Figure 8 shows the hard switching on waveforms at 400V/33A. A V_{DS} dip can be seen because of the rising drain current (di/dt in the power loop ΔV = Lp * di/dt, where Lp is the total power loop inductance). After the drain current reaches the inductor current, the V_{DS} starts to fall. The V_{GS} undershoot spike is caused by the Miller feedback through Cgd under negative dv/dt.

Because of the low gate charge and small $R_{G(OFF)}$, the GaN E-HEMT gate has limited control on the turn-off dv/dt. Instead, the V_{DS} rise time is determined by how fast the turn-off current charges the switching node capacitance (C_{OSS}).

The low C_{OSS} of the GaN E-HEMT and low parasitic inductance of the GaNPX™ package together with optimized PCB layout, enables a fast and clean turn-off V_{DS} waveform with 50V the turn-off V_{DS} overshoot at dv/dt >100V/ns. The measured rise time is 4ns at 400V and 33A hard turn-off.

The OCP setting point is 40A. Because of the ringing on the current sensing signal, the actual OCP trigger point is 33A. After the OCP occurs, the driver is locked with the Gate pulled low regardless the PWM input.

Synchronous Buck Test (L = 120µH, V_{IN} = 400V, V_{OUT} = 80V, D = 20%, f_{SW} = 100kHz, POUT = 300W).

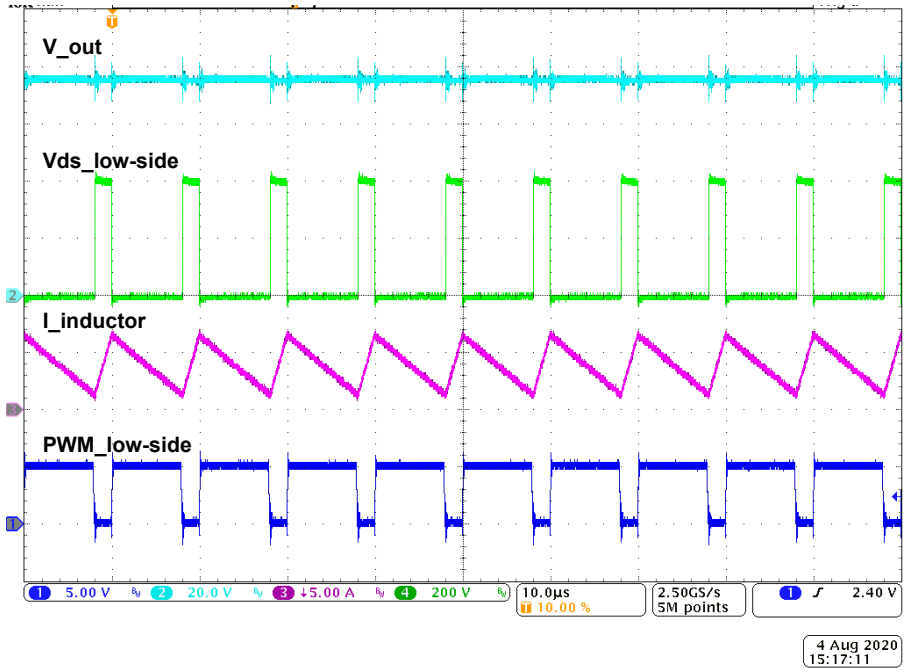


Figure 9. Buck Test Waveform (POUT = 300W)

2. PCB Layout Guidelines

2.1 RTKA226110DE0010BU Evaluation Board (Daughter Board)

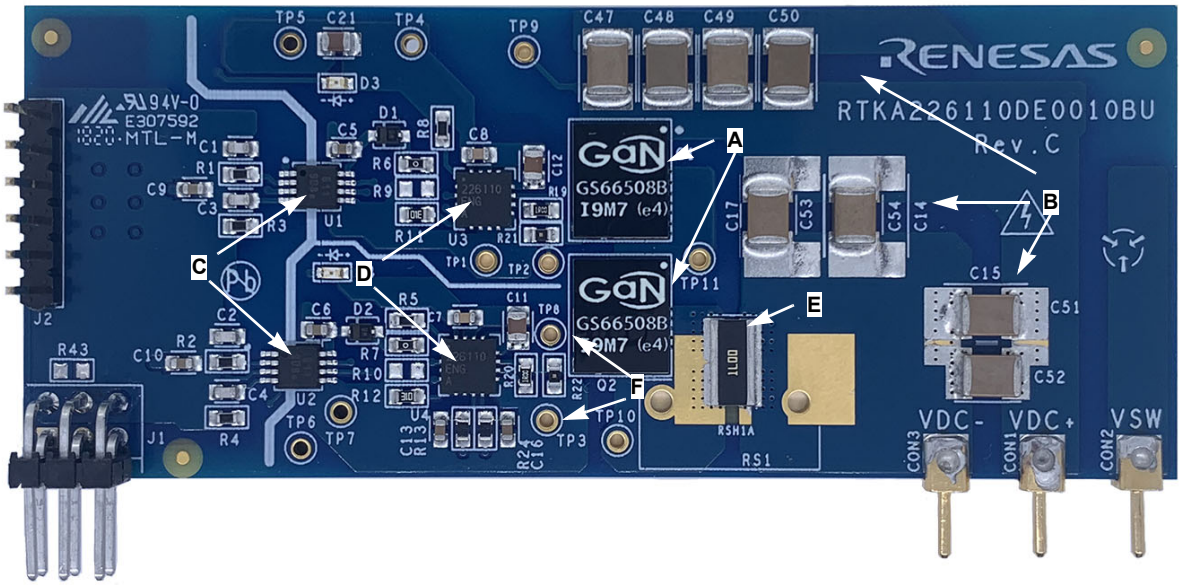


Figure 10. RTKA226110DE0010BU Top Side

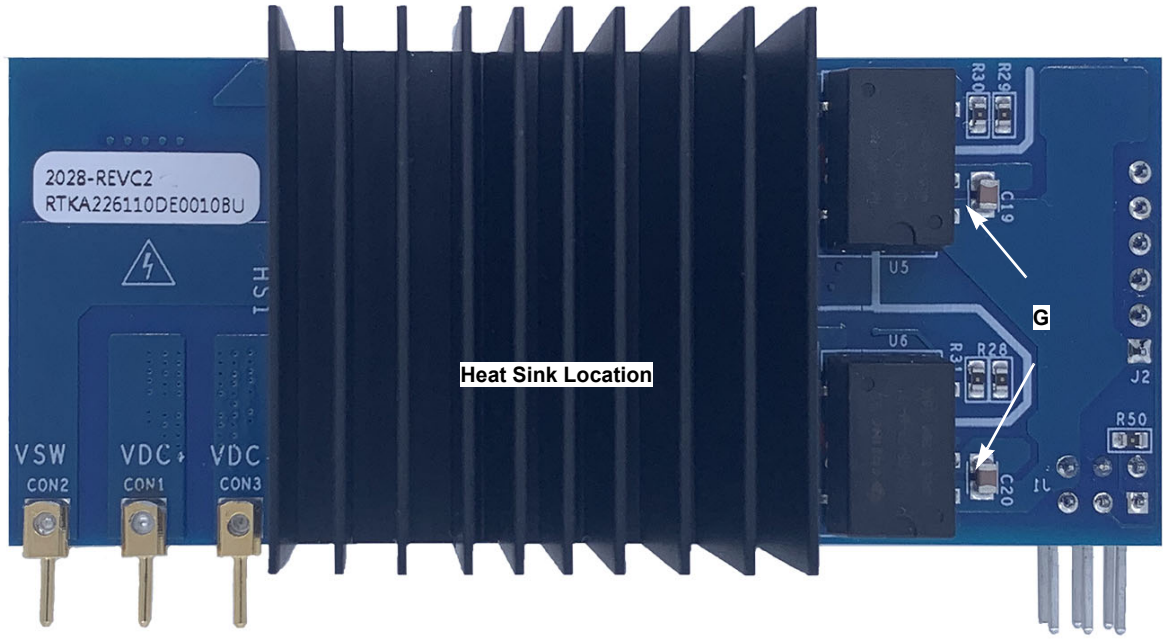


Figure 11. RTKA226110DE0010BU Bottom Side

- A. 2x GaN Systems 650V E-HEMT GS66508B, 30A/50mΩ
- B. Decoupling capacitors C14-C17 and C47-C54
- C. Signal isolator IL611-1E
- D. GaN driver RAA226110
- E. OCP shunt
- F. TP8 (gate) and TP3 (source) test points for bottom Q2 V_{GS}
- G. 5V-9V isolated DC/DC gate drive power supply

2.1.1 GaN E-HEMTs

This daughter board includes two GaN Systems E-HEMT GS66508B (650V/30A, 50mΩ) in a GaNPx™ B type package. The large S pad serves as source connection and thermal pad. Pin 4 is the Kelvin source connection for gate drive return.

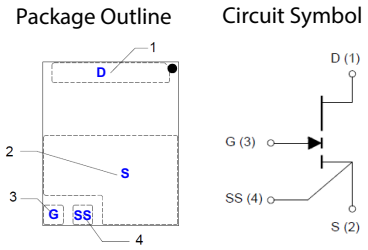


Figure 12. Package Outline of GS66508B

2.1.2 Gate Driver Circuit

The Renesas RAA226110 low-side gate driver is chosen for this design. This driver provides 5.8V gate drive with 3.8V UVLO. It supports the 5.8V turn-on and -3V/0V turn-off. It has separated source and sink drive outputs that eliminates the need for an additional diode. OCP is also integrated in the driver.

RAA226110 provides configurable source current (0.3A/0.75A/2A) to adjust the slew rate of GS66508B without gate resistor to minimize the gate loop. The turn off speed can be directly controlled by the gate resistor $R_{G(OFF)}$ (R19/R20).

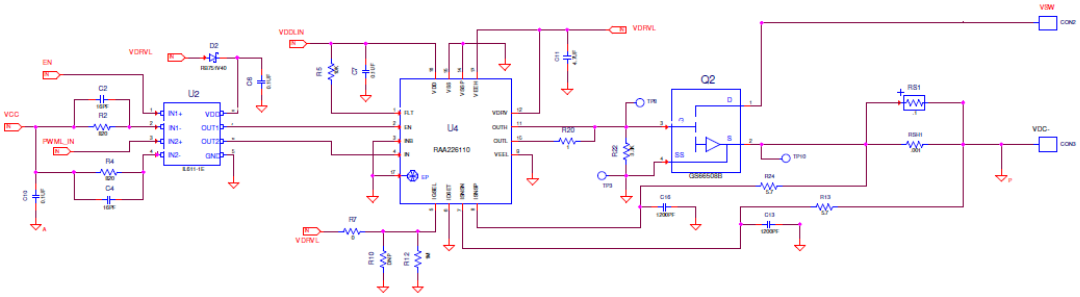


Figure 13. Gate Driver Circuit

2.1.3 Gate Drive Power Supply

5V to 9V isolated DC/DC converters are used for gate drive. The RAA226110 accepts 4.5V to 18V V_{DD} input voltage. DC/DC converter 9V output is directly connected to RAA226110.

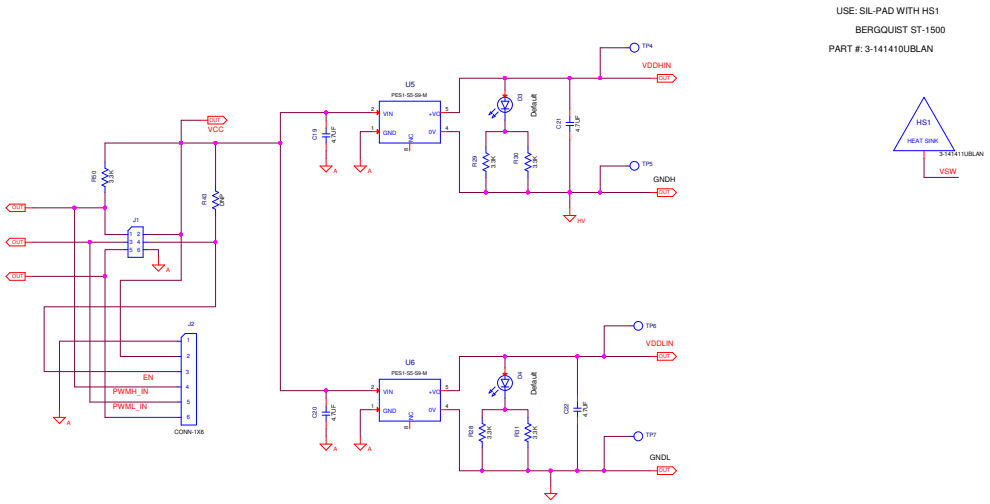


Figure 14. Gate Drive Power Supply

2.1.4 Current Shunt

- The board provides an optional current shunt position E (Figure 10) between the source of Q2 and power ground return, allowing the drain current measurement for switching characterization test such as Eon/Eoff measurement.
- The current shunt also provides the OCP signal for the RAA226110 to trigger OCP. The OCP threshold voltage 40mV/80mV/120mV can be configured through the IDSET pin of RAA226110.
- If current shunt is not used, position E must be shorted.

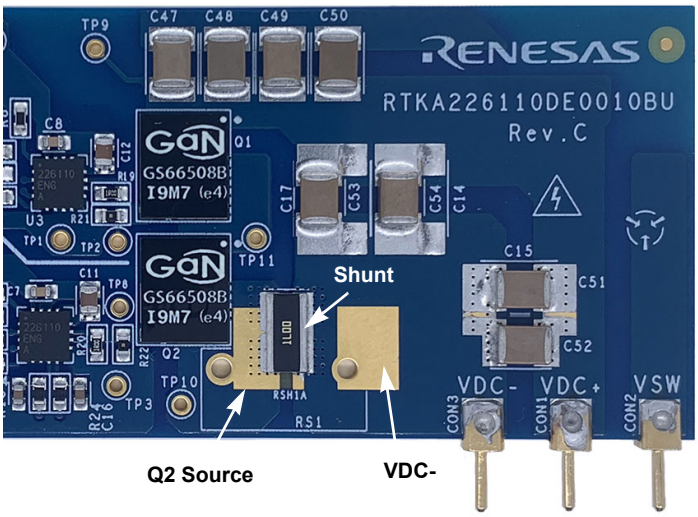


Figure 15. Current Shunt Position E

CAUTION:
Check the shunt position E before the first time use. To complete the circuit position E needs to be either shorted or a current shunt must be inserted before powering up.

2.1.5 Measurement with Current Shunt

- When measuring VSW with current shunt, ensure all channel probe grounds and the current shunt BNC output case are all referenced to the source end of Q2 before the current shunt. The recommended setup of probes is shown in Figure 16.
- The output of coaxial current shunt can be connected to oscilloscope through a 50Ω termination impedance to reduce the ringing.
- The measured current is inverted and can be scaled by using: $I_D = V_{ID} / R_{SHUNT}$.

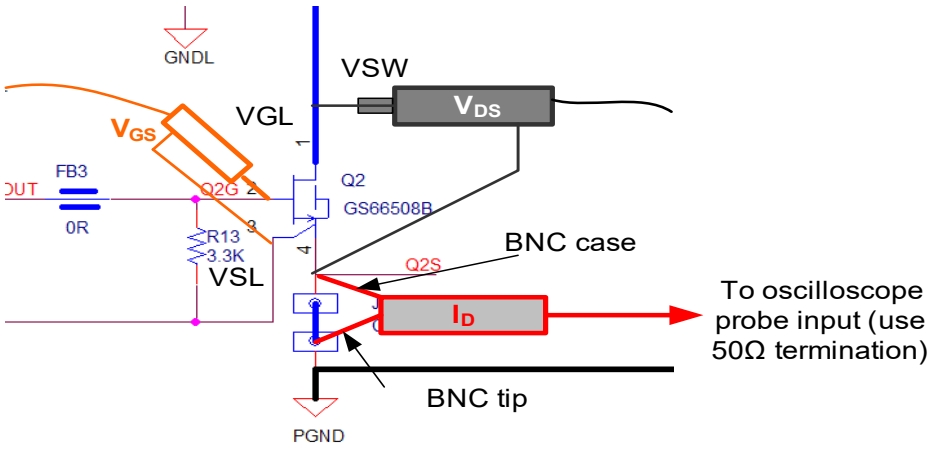


Figure 16. Recommended Probe Connection with Current Shunt

2.1.6 Thermal Design

- GS66508B has a thermal pad on the bottom side for heat dissipation. The heat is transferred to the bottom side of the Printed Circuit Board (PCB) using thermal vias and copper plane.
- A heatsink (35x35mm size) can be attached to the bottom side of the board for optimum cooling. Thermal Interface Material (TIM) is needed to provide electrical insulation and conformance to the PCB surface. The daughter board is shipped with a sample 35x35mm fin heatsink (not installed), although other heatsinks can also be used to fit your system design.
- A thermal tape type TIM (Berguist® Bond-Ply 100) is chosen for its easy assembly. The supplied heatsink has the thermal tape pre-applied so simply peel off the protective film and attach the heatsink to the back of board as marked in Figure 11.
- Two optional mounting holes as shown in Figure 17 are provided for mounting customized heatsink using screws.
- Using the supplied heatsink and TIM, the overall junction to ambient thermal resistance R_{thJ-A} is ~9°C/W with 500LFM airflow.
- Forced air cooling is recommended for power testing.

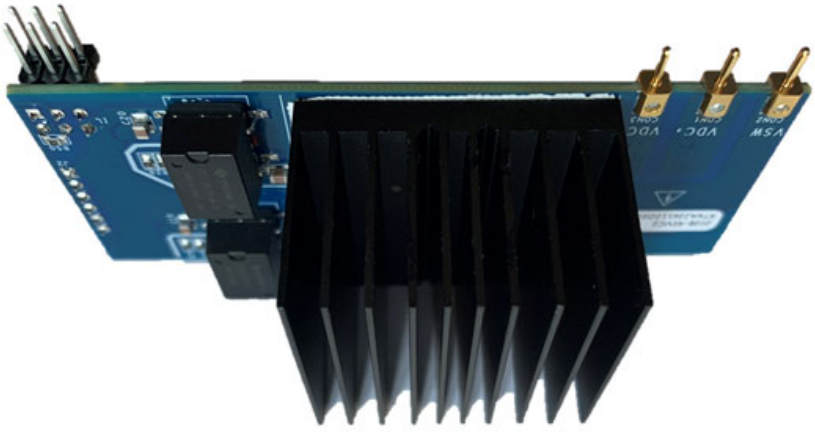


Figure 17. Daughter Board with Heatsink Attached

CAUTION:
There is no on-board over-temperature protection. Device temperature must be closely monitored during the test. Never operate the board with device temperature exceeding T_{J_MAX} (150°C)

2.2 RTKA226110DE0010BU Circuit Schematic

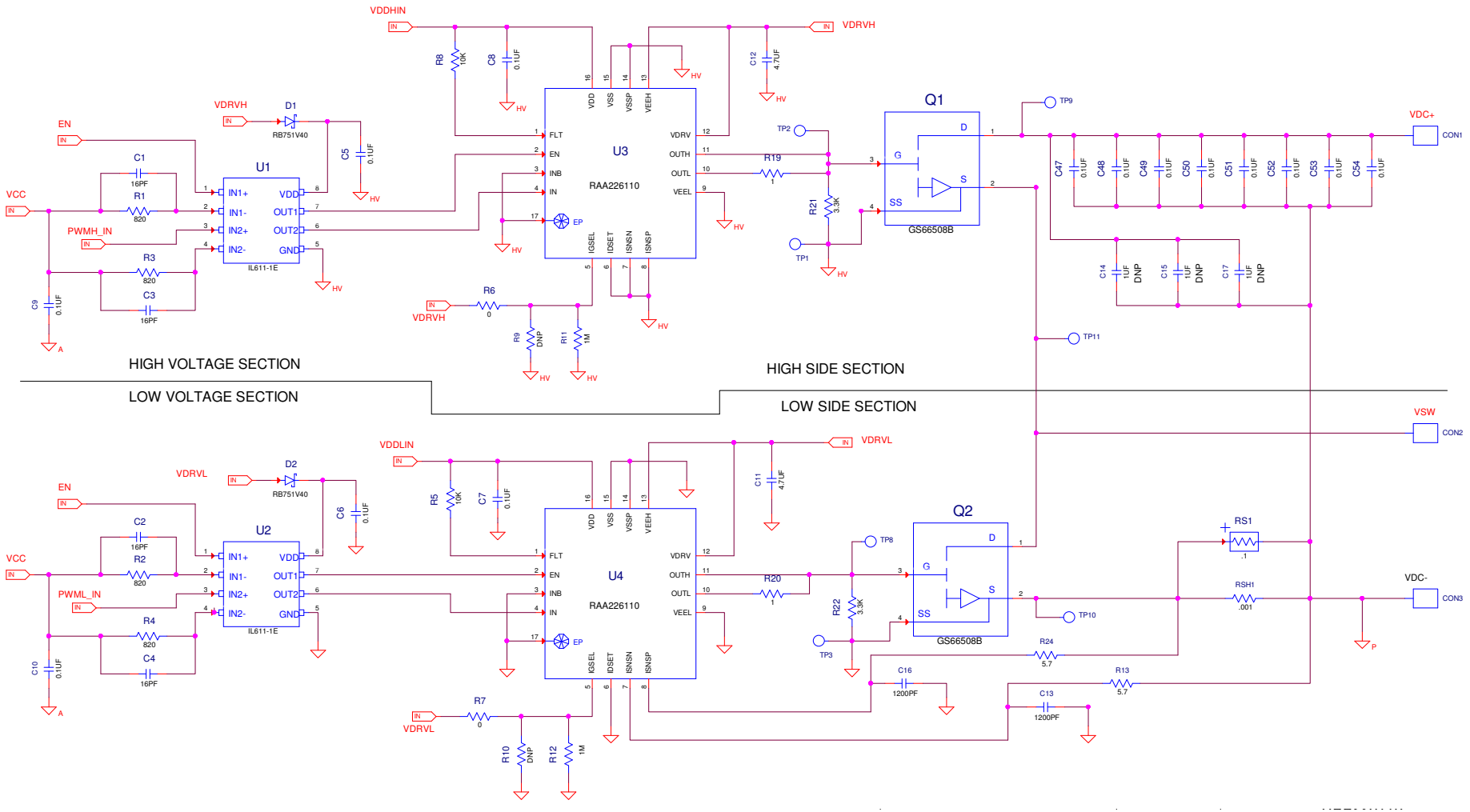


Figure 18. Schematic

2.3 RTKA226110DE0010BU Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB,RTKA226110DE0010BU, REVC, ROHS	Imagineering Inc	RTKA226110DE0010BURVCPCB
6	C11, C12, C19-C22	CAP-AEC-Q200, SMD, 0805, 4.7µF, 25V, 10%, X7R, ROHS	TDK	CGA4J1X7R1E475K125AC
2	C7, C8	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R, ROHS	Yageo	CC0603KRX7R8BB104
4	C5, C6, C9, C10	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	AVX	06035C104KAT2A
2	C13, C16	CAP, SMD, 0603, 1200pF, 50V, 10%, X7R, ROHS	Panasonic	ECJ-1VB1H122K
4	C1, C2, C3, C4	CAP, SMD, 0603, 16pF, 50V, 5%, C0G/NP0, ROHS	Yageo	CC0603JRNPO9BN160
3	CON1, CON2, CON3	CONN-PC PIN, TH, 1.02mmDIA., 9.04mmLENGTH, GOLD, ROHS	Mill-max	3620-2-32-15-00-00-08-0
1	J2	CONN-HEADER,1x6, BRKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
1	J1	CONN-HEADER, 2x3, BRKAWY, 2.54mm, TIN, R/A, ROHS	Samtec	TSW-103-08-T-D-RA
2	D1, D2	DIODE-SCHOTTKY, SMD, SOD-323, 40V, 120mA, ROHS	Nexperia USA, INC	RB751V40,115
2	D3, D4	LED, SMD, 0603, GREEN CLEAR, 2V, 20mA, 574nm, 35mcd, ROHS	LITEON/VISHAY	LTST-C191KGKT
2	U1, U2	IC-DIGITAL ISOLATOR, SMD, 8P, MSOP, 2-CHANNEL, 2500Vrms, ROHS	NVE Corporation	IL611-1E
2	U3, U4	IC Low-Side Gan Driver, 16P, QFN, 4x4, ROHS	Renesas Electronics	RAA2261104GNP#MA0
2	Q1, Q2	TRANSISTOR-MOS, N-CHANNEL, SMD, 8.8x7mm, 650V, 30A, 50mΩ, ROHS	GaN Systems	GS66508B-E01-MR
0	R9, R10, R43	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER		
2	R19, R20	RES, SMD, 0603, 1Ω, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3RQF1R0V
2	R6, R7	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	Venkel	CR0603-10W-000T
2	R5, R8	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
2	R11, R12	RES, SMD, 0603, 1M, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1004V
2	R13, R24	RES, SMD, 0603, 5.76Ω, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-075R76L
4	R1, R2, R3, R4	RES, SMD, 0603, 820Ω, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-8200FT
7	R21, R22, R28, R29, R30, R31, R50	RES-AEC-Q200, SMD, 0603, 3.3k, 1/10W, 1%, TF, ROHS	Rohm	KTR03EZPF3301
1	RSH1A	RES-AEC-Q200, SMD, 2512-WIDE, 0.001Ω, 2W, 5%, ROHS	Rohm	PML100HZPJV1L0
1	HS1 (See Assy Instructions)	HEATSINK-BGA, 35x35x24.50mm, Straight Fin w/Thermal Tape	Advanced Thermal Solutions Inc	ATS-54350W-C1-R0

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	HS1-Cut thermal sheet into 1.378 inch squares and place between heat sink and PCB.	Instructions for assembly.	Renesas Electronics America	Assembly Instructions
1	HS1 (SEE ASSY INSTRUCTIONS)	INSULATION-BOND-PLY, 11mil, 10x10in, 2-SIDE ADHESIVE, ROHS	Bergquist	BP100-0.011-00-1010-NA
8	C47, C48, C49, C50, C51, C52, C53, C54	CAP, SMD, 1812, 0.1µF, 1kV, 10%, X7R, ROHS	Kemet	C1812C104KDRAC7800
0	C14, C15 ,C17 (2220Y6300105KXTWS2)	DO NOT POPULATE OR PURCHASE		
0	RS1	DO NOT POPULATE OR PURCHASE		
0	TP1-TP11	DO NOT POPULATE OR PURCHASE		
2	U5, U6	PWR-SUPPLY, DC/DC CONVERT, SMD, 12.7x8.3, 1W, 5V, 111mA, ROHS	CUI, INC	PES1-S5-S9-M-TR

2.4 RTKA226110DE0010BU Board Layout

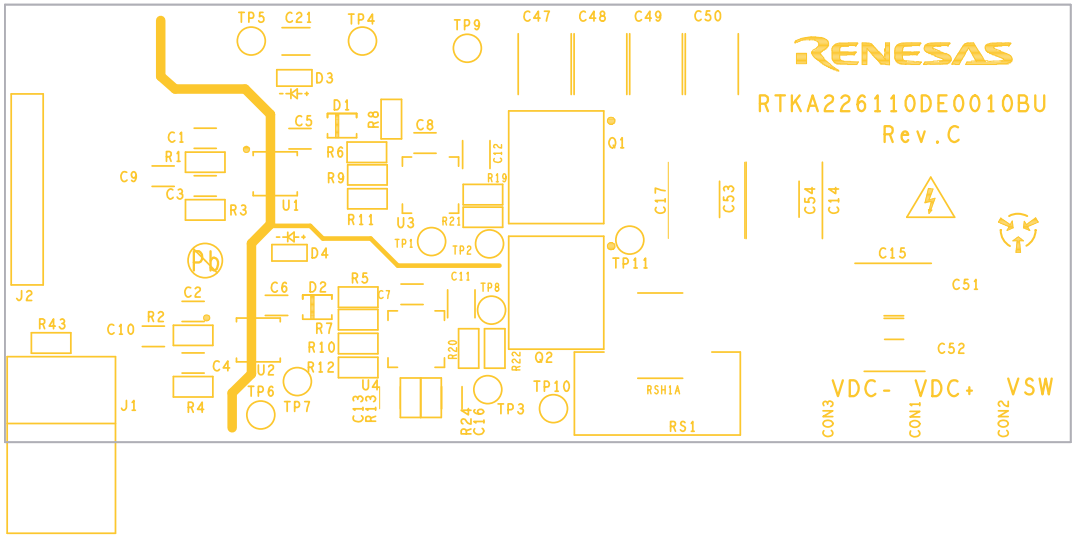


Figure 19. Silkscreen Top

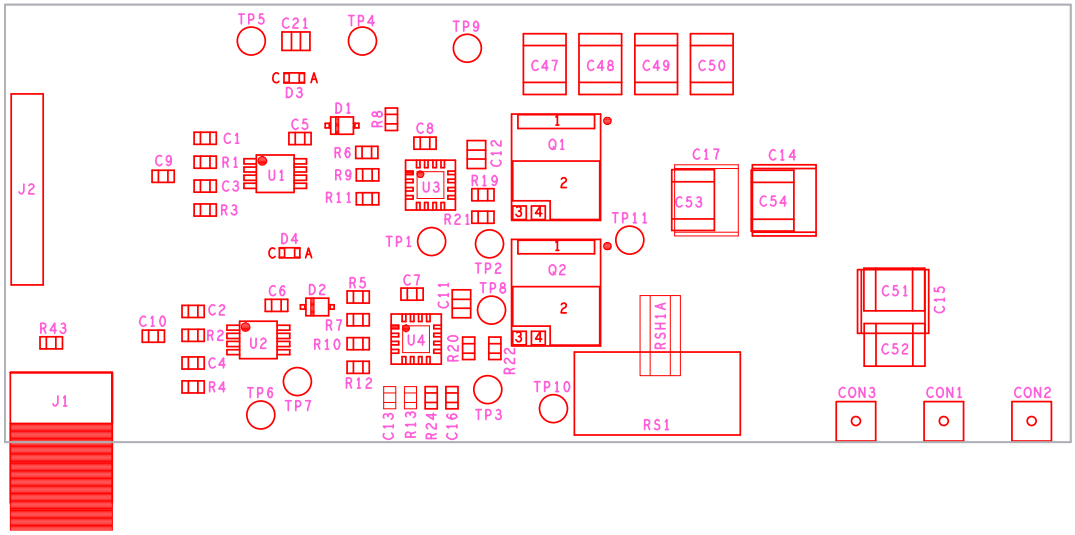


Figure 20. Assembly Top

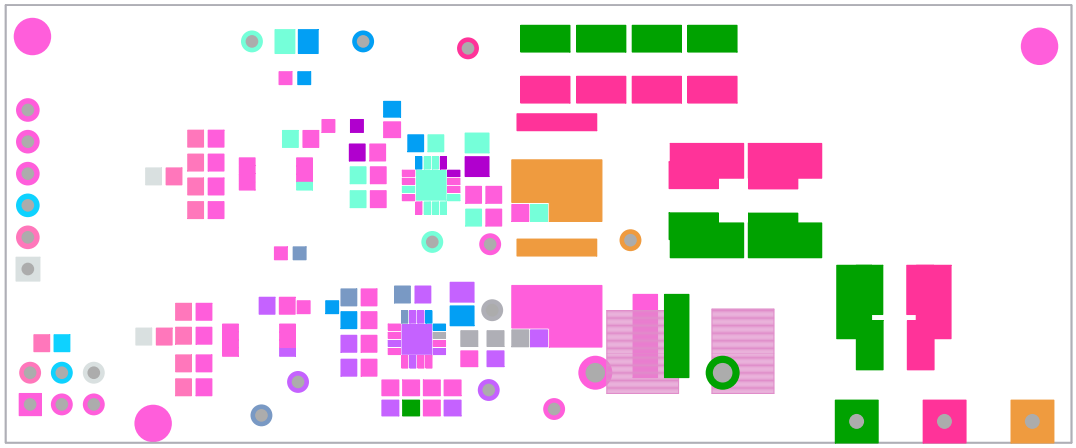


Figure 21. Solder Top

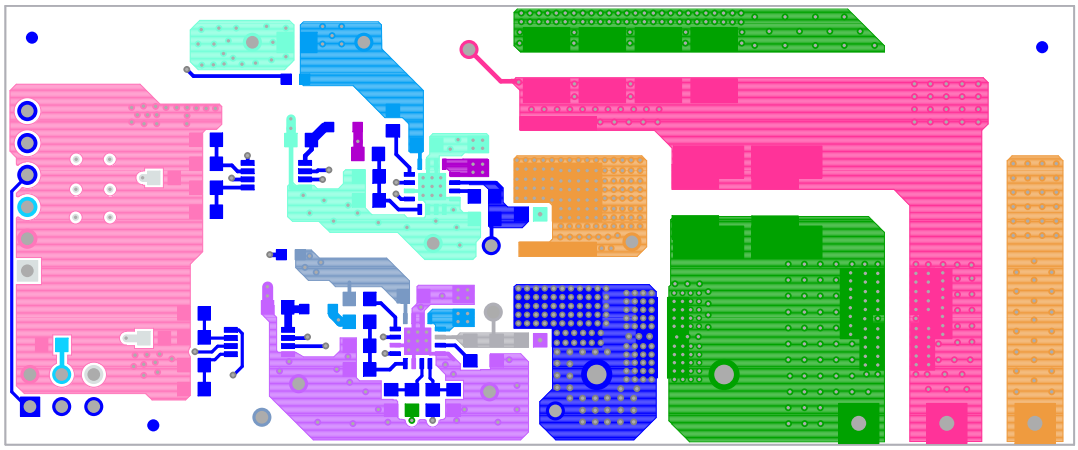


Figure 22. Top Layer

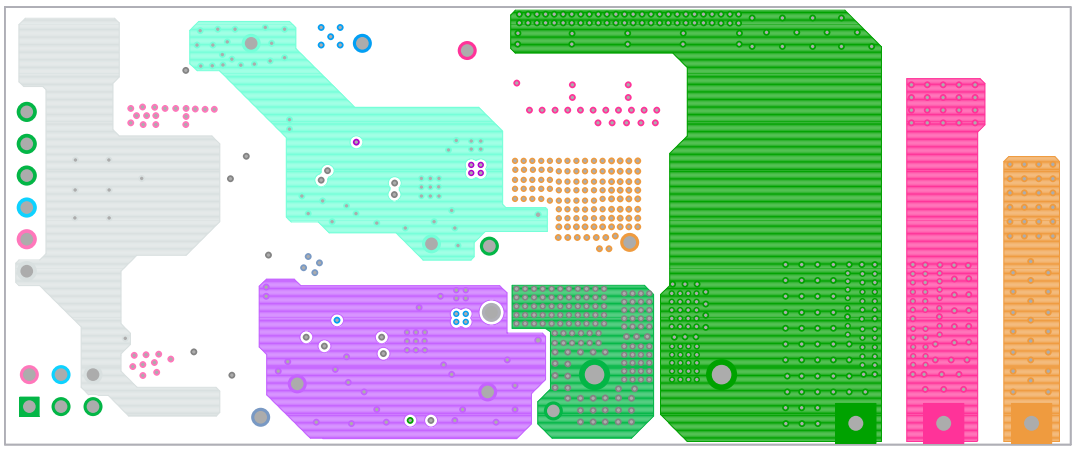


Figure 23. Layer 2

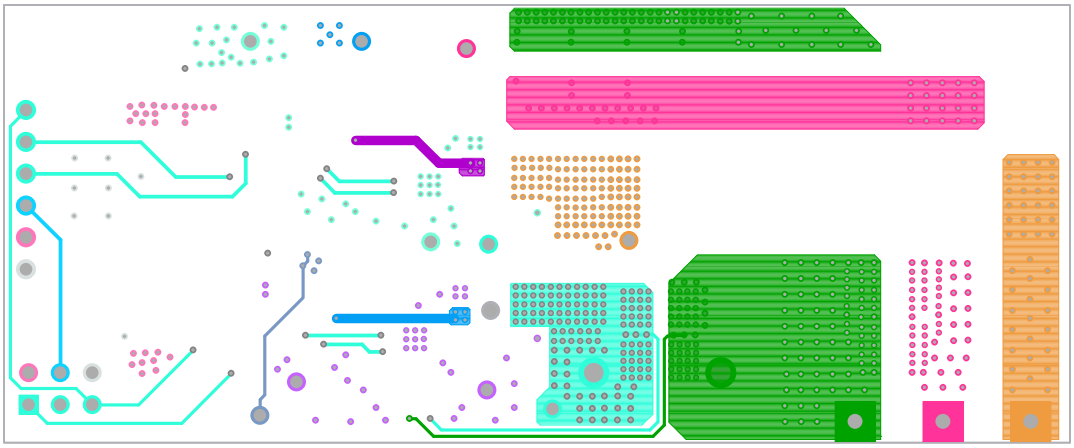


Figure 24. Layer 3

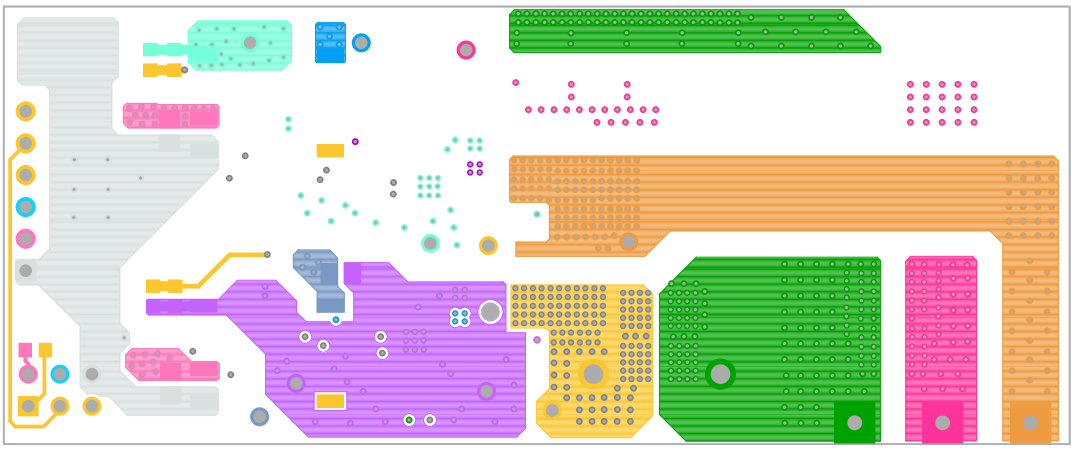


Figure 25. Bottom Layer

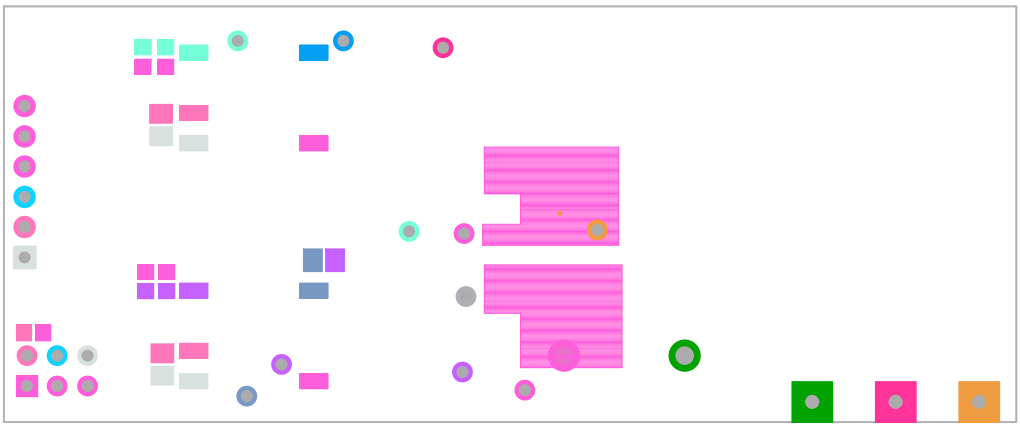
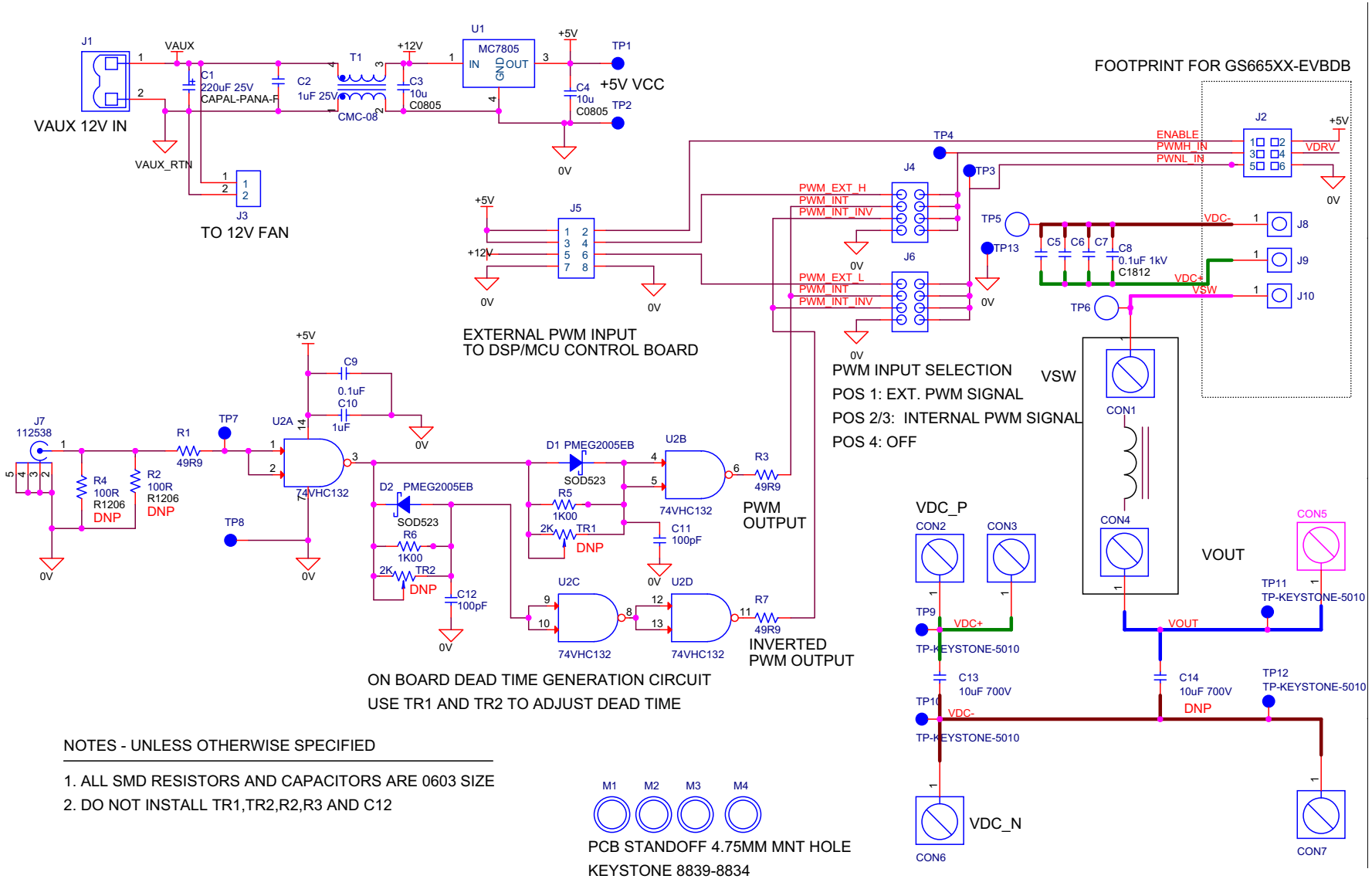


Figure 26. Solder Bottom

3. Appendix A - GS665MB-EVB

To ensure that you have the latest GS665MB-EVB information, visit the GaN systems Inc website.

3.1 GS665MB-EVB Circuit Schematics



NOTES - UNLESS OTHERWISE SPECIFIED

1. ALL SMD RESISTORS AND CAPACITORS ARE 0603 SIZE
2. DO NOT INSTALL TR1,TR2,R2,R3 AND C12

M1 M2 M3 M4

PCB STANDOFF 4.75MM MNT HOLE
KEYSTONE 8839-8834

3.2 GS665MB-EVB Board Layout

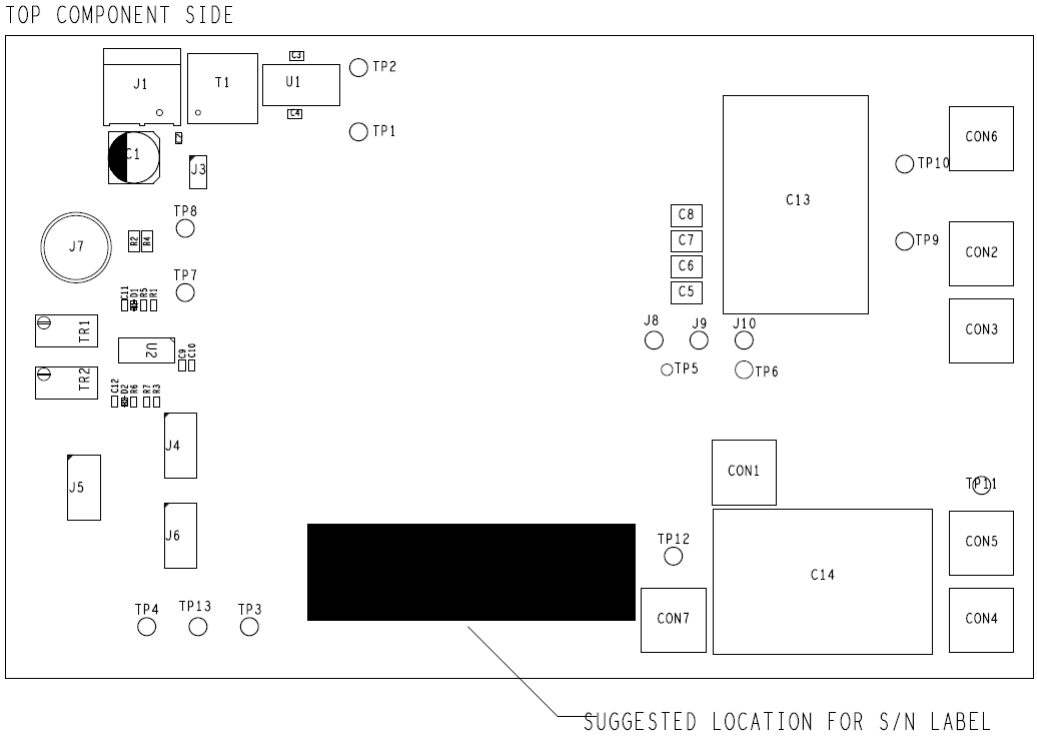


Figure 27. Assembly Top

Figure 28. Assembly Bottom

3.3 GS665MB-EVB Bill of Materials

Quantity	Reference	Description	Value	Manufacturer	Part number	Assembly Note
1	PCB	PCB bare 2-layer 2oz Cu.	Gerber file: GS665EVBMB-GerberNCDrill-RevB-20160628	Shenzhen Sprint PCB	GS665EVBMB-GerberNCDrill-RevB-20160628	
7	**CON1, CON2, CON3, CON4, CON5, CON6, CON7**	**TERMINAL SCREW VERTICAL PC MNT**	**CON-10-32-SCRWMNT**	**Keystone**	**RevB-**	**DO NOT INSTALL ***
1	C1	CAP ALUM 220µF 20% 25V SMD	220µF 25V	Panasonic	20160628	
1	C2,C10	GENERIC 1µF/25V, 10% X7R SMD 0603	1µF	Taiyo Yuden	TMK107B7105KA-T	
2	C3, C4	GENERIC 10µF/25V, 10% SMD 0805	10µF	Taiyo Yuden	TMK212BBJ106KG-T	
4	C5, C6, C7, C8	GENERIC 0.1µF/1000V, SMD 1812	0.1µF 1kV	Kemet	C1812C104KDRAC7800	
1	C9	GENERIC 0.1µF/25V, 10% X7R SMD 0603	0.1µF	Taiyo Yuden	TMJ107BB7104KAHT	
2	C11, C12	GENERIC 100PF/25V 5% NP0 SMD 0603	100pF	Kemet	C0603C101J3GACTU	
1	**C13, ~~C14~~**	**CAP FILM 10µF/600VDC 5%, 27.5MM LEAD SPACING**	**10µF 700V**	**Kemet**	**C4AEHBU5100A11J**	**DO NOT INSTALL C14 ***
2	D1, D2	DIODE SCHOTTKY 20V 500MA SOD523	PMEG2005EB	NXP	PMEG2005EB,115	
1	J1	TERM BLOCK HDR 2POS R/A 5.08MM	CON-TERM-BLK-2POS-RA	TE Connectivity	796638-2	
1	J1-PLUG	TERM BLOCK BLUG 2POS 5.08MM		Te Connectivity	796634-2	
1	J2	CONN RCPT 6POS 0.100 DBL STR PCB	CON-RCPT-2X3-BOT	Harwin	M20-7850342	MOUNT FROM BOTTOM SIDE
1	**J3**		**CON-2POS**			**CONNECTOR FOR 12V FAN, DO NOT INSTALL ***
2	J4, J6	CONN HEADER 8POS DUAL VERT PCB	CON-JMP-4POS	Harwin	M20-9980445	
1	J5	CONN 8-POS, DUAL ROW 2.54MM	CON-HDR-4X2	Amphenol	75869-132LF	
1	J7	CONN BNC JACK STR 50Ω PCB	112538	Amphenol	112538	
3	J8, J9, J10	CONN RECEPT PIN 032 -.046" 0.075"	CON-RCPT-EDGEMNT	Millmax	0312-0-15-15-34-27-10-0	MATING SOCKET FOR MILLMAX EDGE MNT PIN
3	R1, R3, R7	generic 1% SMD 0603	49R9	Vishay Dale	CRCW060349R9FKEA	
2	R2, R4	generic 1% SMD 1206	100R			DO NOT INSTALL *
2	R5, R6	generic 1% SMD 0603	1K00	VISHAY DALE	CRCW06031K00FKEA	

Quantity	Reference	Description	Value	Manufacturer	Part number	Assembly Note
11	TP1, TP2, TP3, TP4, TP7, TP8, TP9, TP10, TP11, TP12, TP13	TEST POINT PCB	TP-KEYSTONE-5010	KEYSTONE	5010	
2	**TR1, TR2**	**TRIM POT CERM 2kΩ 25TRN TOP**	**2k**			**DO NOT INSTALL ***
1	T1	COMM MODE CHOKE 5.2A T/H	CMC-08	RECOM	CMC-08	
1	U1	IC REG LDO 5V 1A DPAK	MC7805	ON SEMI	MC7805BDTRKG	
1	U2	1 IC GATE NAND 4CH 2-INP 14-SOIC	74VHC132	FAIRCHILD	74VHC132MX	
Off the Board Components						
6	M1, M2, M3, M4, M5, M6	BRD SPT SNAP FIT SCREW MNT 1/2"	MECH-STDOFF-KEYSTONE-8833	KEYSTONE	8833	PCB SPACER, INSTALL FROM BOTTOM SIDE
1	FAN	FAN AXIAL 38X20MM 12V_{DC} WIRE		SUNON FANS	PMD1238PKB1-A.(2).GN	SUPPLY LOOSE, DO NOT INSTALL ON THE ASSEMBLY
2	JUMPER	JUMPER SHUNT GENERIC		TE CONNECTIVITY	382811-8	INSTALL ON J4 "INT" POSITION AND J6 "INT_INV" POSITION

4. Revision History

Rev.	Date	Description
1.00	Dec.7.20	Initial release

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