

RAA271005 GUI Software

Introduction

The RAA271005 Graphic User Interface (GUI) is a comprehensive interface that configures and monitors the Buck and LDO regulators. It allows users to adjust voltage and frequency settings, and test different configurations. This manual provides instructions on how to use real-time performance features by the GUI application to communicate with the RAA271005 device to monitor key parameters.

Contents

1.	System Requirements	1
2.	Installation Guide	1
3.	User Interface Overview	2
4.	Configuring and Using the Control Menu	3
5.	Configuring and Using the Register Window	4
6.	Revision History	5

1. System Requirements

The following list shows the minimum system requirements for the RAA271005 GUI software program:

- PC with Intel i5 2.60GHz CPU or better
- Windows 10 or higher
- 82MB of free hard-disk space
- USB port

To communicate between the system and GUI application, a USB to I²C/SPI communication dongle (ISLUSBMINIEVAL1Z) is required. The Renesas GUI supports this tool across all operating systems.

2. Installation Guide



3. User Interface Overview

	4				- Regi	ster Map F	eature	es				Control
Contraction Status - Contra	OTP	ADCMC	INI INI	ILDOREGU EXTLDO	PVIN VOUT	EXT MTE I S	DC Table View	v				RENESA
Devotes a cost devotes according of the second devotes according a	43	3	×	OTP_SOAKCOUNT	0	OTP_READDATA	247	01 110	P_CALCCRCMSB P_CALCCRCMSB	97 ×	Communication Status	Communication USB connection
OP CALCERCISS OP WINTERATA OP WINTERATA OP WINTERATA OP CALCERCISS OP CALCERCISS <td>0x2E</td> <td>x28</td> <td></td> <td>0x0023</td> <td>0x00</td> <td>0x0024</td> <td>0xF7</td> <td>0x0</td> <td>0025</td> <td>0x61</td> <td></td> <td>Raa271005 Device Communica</td>	0x2E	x28		0x0023	0x00	0x0024	0xF7	0x0	0025	0x61		Raa271005 Device Communica
Concept of the concep	247	47	×	OTP_WRITEDATA	0	OTP_RWADDR OTP_CRC_FAULT OTP_BUSY OTP_RW OTP_ADDRMSB	CRC p OTP mac Power off s 0	pass OTI cro is state	P_ADDRLSB P_ADDRLSB	0 ~	RAW I/O	Reconnect to device Raw I/O Bus Interface I2C PROT Slave Address REGU Slave Address Di54
OTP_FILSORD OTP_CRCMSS OTP_CRCMSS OTP_CRCMSS OTP_CRCMSS OTP_FILSORD OTP_FILSORD OTP_CRCMSS OTP_CRCMSS OTP_FILSORD OTP_CRCMSS OTP_CRCMSS OTP_FILSORD OTP_CRCMSS OTP_FILSORD OTP_CRCMSS OTP_CRC	0xF7	xF7		0x0027	0x00	0x0028	0x00	0×0	0029	0x00		Reg. Address 0x000022
Polling - Register Read Back - Salur Friering opp. Truncete Model Log Irent Info	9e0 25 9e2 26 9 26 9 26 9 26	fault record fault record fault record fault record fault record fault record fault record fault record fault record	ded ded ded ded ded ded ded	OTP_CRCMSB	220	OTP_CRCLSB	186	10 × 170 × 1	P_FLT_MASK P_FItMask_DLOAD P_FItMask_INIT_Fail P_FItMask_CRC_Fail. P_FItMask_CRC_Fail. P_FItMask_PGM_N P_FItMask_PGM_W P_FItMask_PGM_W P_FItMask_PGM_Er	not masked not masked not masked not masked not masked not masked		Send Data 0x00 Read Data 0x28 # Aranneck Mode Address Bytes 3 Frequency 400.000 kHz Dev Num 0 CRC Flag 0
	UXPE	wrc		0x0028	URDC	0x002C	UKBA	UX	J126	000	Bolling	Raa271005 Test Mode Off
Seture Seture Teler (vig ropt) Enumerate Mode Log (vet life) Output L og Windowy											Poliing —	Disabled O Poll All Registers Poll Visible
Setter Vergreger											Register Read Back	Read All Registers
Status Status A Mine Status Status S											-	File IO File IO Save Load Format: CM Scripting Mode
Output Log Window) ark	53	ive to file	F	Status itter (reg expr):	-	Enumerate Mode	le	Log level: [i	nto v	Infe infe Bitteld Info Inference Bitteld Inference Inference Bitteld Inference	Chip ID
Current Value 1 Current Value 1 Curent Value 1 Current Value 1 Curent Value 1 Current Value 1 Current Value 1 Current				Output	Log Wi	ndow					ROX 0 Current/Nue 1 Enumented Value: 1 Chipmodd Blocks Chipmodd Blocks	Read Chip ID USB Interface Info Interface: Renesas ISL ISL Version: 00.000 Device: 0

Figure 1. GUI Interface Application

- Register Map Features The GUI is divided into two sections, regulation and protection. The regulation side of the PMIC is responsible for power management functions and delivers stable power to all outputs while the protection side monitors internal signals for faults. The registers are sorted by categorical titles with each register displaying its corresponding register field bit names.
- Communication Status To confirm that the USB dongle and device are properly connected, both status indicators should display green. If either of the status indicators depicts a red state as depicted in Figure 3, this indicates that communication between the USB dongle and device has not been established correctly. In this case, check the configuration and connection to resolve the issue. Ensure that the correct slave address for regulation and protection has been selected according to the OTP settings.

In Figure 2, the indicators depict that no connection has been detected.



Figure 2. No Communication Status Detected

Com	Communication							
	USB connection							
0	Raa271005 Device Communication							
	Reconnect to device							





RAW I/O – The RAW I/O enables users to configure communication protocol settings. The bus interface
includes options for selecting either I²C or SPI protocol, allowing the GUI to adapt accordingly. Individual
register addresses can also be accessed by entering the corresponding slave address, which can be used for
either regulation or protection features. In addition, the advance mode options allow users to customize settings
by adjusting the clock frequency and toggling CRC (Cyclic Redundancy Check).

Note: When using the RAW I/O read or write regulation setting, an offset of 0x10000 must be added to the register address. Not doing so, causes the command to communicate with the protection side setting. The number of address bytes must also be set to 3. Figure 4 shows a setup on how to configure a regulation register address.

Raw I/O						
Bus Interface		I2C	\sim			
PROT Slave Ad	dress	0x59	÷			
REGU Slave Ad	dress	0x58	÷			
Reg. Address		0x010022	÷			
Send Dat	a	0x00	÷			
Read Dat	a	0xE9				
Advanced N	/lode					
Address Bytes	3		÷			
Frequency	400 k	Hz	÷			
Dev Num	0		÷			
CRC Flag	0		÷			

Figure 4. RAW I/O Configuration

- Polling The polling feature enables users to observe register settings in real-time metrics. If selected, registers are continuously read and are displayed in the output window log.
- Register Read Back This option enables all registers to be read and updated. *Note*: If this option is selected, any modifications made to individual registers within the register map revert to the default OTP (One-Time Programmable) settings.
- Output Log Window This section displays the activity within the GUI, providing a log of interactions. It can sort
 and review through register readback history, allowing users to track and analyze register data. The feature
 also offers debug capability, as it helps identify issues within setup and operation.

4. Configuring and Using the Control Menu

The following steps must be taken to ensure proper communication of the RAA271005, which shows the status indicators are green within the GUI application.

Example setup for I²C protocol:

- 1. Supply 5V to VIN.
- 2. Connect dongle to J69 (located at top right corner of board).
- 3. Configure jumpers for SCL (IO1) and SDA (IO2); Jumpers must also be added at J60 and J61 to ensure proper communication with GUI application.





Figure 5. RAA271005 Evaluation Board Setup

5. Configuring and Using the Register Window

The register window provides a full display of the register map, allowing users to manipulate individual bits within a register. The registers of both protection and regulation settings are sorted by categories for convenient navigation. Figure 6 shows the different category tabs with each containing specific registers.

In the example shown in Figure 6, register 0x0022 (IO_MODECTRL_REGU) and 0x0023 (IO_MODECTRL2_REGU) depicts the output states of the regulators. The green status of register field bits represents a high state while gray status depicts low state.



In register 0x0022, only Buck4 is disabled out of the Buck regulators. While LDO1-3 regulators are disabled in register 0x0023. To disable other regulators, click on the regulator status, which updates the register data in real time.

PROTECT	ION REGULATION							
MISC	IO OTP FLT F	G1 BUCK1 BUCK2	2 BUCK3 BUCK4 E	UCK5 LDO1 LDO	SELDIV I			
2	- 10							
						C 11]
	IO_PAGE_REGU	Curtanua Dana 🔤		2.44		GU		254
	IO_PAGE	Customer Page V	IO_CHIPNAME	5 - n.a. 👻	IO_CHIPVERSION	194 - n.a. 👻	IO_DIEID3	254
	0x0000	0x00	0x0001	0x03	0x0002	0xC2	0x0003	OXFE
	IO_DIEID2_REGU		IO_DIEID1_REGU		IO_DIEID0_REGU		IO_MODECTRL_REGU	
	IO_DIEID2	220 👻	IO_DIEID1	186 🗸	IO_DIEID0	152 🔍	IO_BUCK1_EN	Buck1 Enabled
							IO_BUCK2_EN	Buck2 Enabled
							IO_BUCK3_EN	Buck3 Enabled
							IO_BUCK4_EN	Buck4 Disabled
							IO_BUCK5_EN	Buck5 Enabled
							IO_MODECTRL_REGU	LDO1 Disabled
							IO_MODECTRL_REGU	LDO1 Disabled
							IO_REGVALID	OTP read successful
	0x0004	0xDC	0x0005	0xBA	0x0006	0x98	0x0022	0xE9
	IO_MODECTRL2_REG	U	IO_GP2CFGMSB		IO_GP2CFGLSB		IO_GP3CFGMSB	
	IO_MODECTRL2_REG	U LDO6 Enabled	IO_GP2CFGMSB IO_GP2DTEST	DTEST0 V	IO_GP2CFGLSB IO_GP2DIGDIRECTION	Output I/O ac	IO_GP3CFGMSB IO_GP3DTEST	DTEST0 V
	IO_MODECTRL2_REG IO_LDO6_EN IO_LDO5_EN	U LDO6 Enabled LDO5 Enabled	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL	DTEST0 v Test path is disco	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2OPENDRAIN	Output I/O ac A CMOS output b	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL	DTEST0 V Test path is disco
	IO_MODECTRL2_REGI IO_LDO6_EN IO_LDO5_EN IO_LDO4_EN	U LDO6 Enabled LDO5 Enabled LDO4 Enabled	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN	DTESTO V Test path is disco No pull up or pu V	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2OPENDRAIN IO_GP2INVERT	Output I/O ac A CMOS output b Noninverting	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN	DTEST0 V Test path is disco No pull up or pt V
	IO_MODECTRL2_REG IO_LDO6_EN IO_LDO5_EN IO_LDO4_EN IO_LDO3_EN	U LDO6 Enabled LDO5 Enabled LDO4 Enabled LDO3 Disabled	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN IO_GP2DRIVE	DTEST0 Test path is disco No pull up or p. Min (20% of Ma:	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2OPENDRAIN IO_GP2INVERT IO_GP2I2CGLTCHFLTR	Output I/O ac A CMOS output b Noninverting Is not	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN IO_GP3DRIVE	DTEST0 V Test path is disco No pull up or pu V Min (20% of Ma: V
	IO_MODECTRL2_REG IO_LDO6_EN IO_LDO5_EN IO_LDO4_EN IO_LDO3_EN IO_LDO3_EN IO_LDO2_EN	U LDO6 Enabled LDO5 Enabled LDO4 Enabled LDO3 Disabled LDO2 Disabled	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN IO_GP2DRIVE	DTEST0 Test path is disco No pull up or pu Min (20% of Ma v	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2OPENDRAIN IO_GP2INVERT IO_GP2I2CGLTCHFLTR IO_GP2I2CSLEWFLTR	Output I/O ac A CMOS output b Noninverting Is not Filters is not	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN IO_GP3DRIVE	DTESTO V Test path is disco No pull up or pt V Min (20% of Ma: V
	IO_MODECTRL2_REG IO_LDO6_EN IO_LDO5_EN IO_LDO4_EN IO_LDO3_EN IO_LDO2_EN IO_LDO1_EN	U LDO6 Enabled LDO5 Enabled LDO4 Enabled LDO3 Disabled LDO2 Disabled LDO1 Disabled	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN IO_GP2DRIVE	DTESTO V Test path is disco No pull up or pu V Min (20% of Mar V	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2OPENDRAIN IO_GP2INVERT IO_GP2I2CGLTCHFLTR IO_GP2I2CSLEWFLTR IO_GP2DINSUPPLY	Output I/O ac A CMOS output b Noninverting Is not Filters is not Low	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN IO_GP3DRIVE	DTESTO
	IO_MODECTRL2_REG IO_LDO6_EN IO_LDO5_EN IO_LDO4_EN IO_LDO3_EN IO_LDO2_EN IO_LDO1_EN	U LDO6 Enabled LDO5 Enabled LDO4 Enabled LDO3 Disabled LDO2 Disabled LDO1 Disabled (0x38	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN IO_GP2DRIVE	DTESTO V Test path is disco No pull up or pt V Min (20% of Ma: V 0x00	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2DIFDRAIN IO_GP2INVERT IO_GP2I2CGITCHFLTR IO_GP2I2CSLEWFLTR IO_GP2DINSUPPLY 0x004B	Output I/O ac A CMOS output b Noninverting Is not Filters is not Low 0x00	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN IO_GP3DRIVE	DTEST0 V Test path is disco No pull up or pt V Min (20% of Mar V 0x00
	IO_MODECTRL2_REG IO_LDO6_EN IO_LDO5_EN IO_LDO4_EN IO_LDO3_EN IO_LDO2_EN IO_LDO1_EN 0x0023	U LDO6 Enabled LDO5 Enabled LDO4 Enabled LDO3 Disabled LDO2 Disabled LDO1 Disabled Ox38	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN IO_GP2DRIVE 0x004A IO_GP4CFGMSB	DTEST0 Test path is disco No pull up or pL Min (20% of Mar) 0x00	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2DISDIRECTION IO_GP2INVERT IO_GP2I2CGITCHFLTR IO_GP2I2CSLEWFLTR IO_GP2DINSUPPLY 0x004B IO_GP4CFGLSB	Output 1/0 ac A CMOS output b Noninverting Is not Filters is not Low 0x00	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN IO_GP3DRIVE 0x004C IO_GP5CFGMSB	DTEST0 V Test path is disco No pull up or pt V Min (20% of Mar V 0x00
	IO_MODECTRL2_REG IO_LDO6_EN IO_LDO5_EN IO_LDO4_EN IO_LDO3_EN IO_LDO2_EN IO_LDO1_EN 0x0023	U LDO6 Enabled LDO5 Enabled LDO4 Enabled LDO3 Disabled LDO1 Disabled DO2 Disabled DO33	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN IO_GP2DRIVE 0x004A IO_GP4CFGMSB IO_GP4DTEST	DTESTO Vo puth is disco No puth up or pu Min (20% of Mar) 0x00 DTESTO	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2DFENDRAIN IO_GP2INVERT IO_GP2IZCGLTCHFITR IO_GP2DISCUTCHFITR IO_GP2DISUPPLY 0x004B IO_GP4CFGLSB IO_GP4DIGDIRECTION	Output I/O ac A CMOS output b Noninverting Is not Filters is not Low 0x00	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN IO_GP3DRIVE 0x004C IO_GP5CFGMSB IO_GP5CFGMSB IO_GP5DTEST	DTESTO V Test path is disco No pull up or pt V Min (20% of Mar V 0x00 ••
	IO_MODECTRL2_REG IO_LD06_EN IO_LD05_EN IO_LD04_EN IO_LD02_EN IO_LD02_EN IO_LD01_EN 0x0023	U LDO6 Enabled LDO5 Enabled LDO4 Enabled LDO3 Disabled LDO1 Disabled DO2 Disabled (0x38	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN IO_GP2DRIVE 0x004A IO_GP4CFGMSB IO_GP4DTEST IO_GP4TESTSEL	DTESTO Test path is disco No pull up or pu Min (20% of Ma 0x00 Test path is disco	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2DFENDRAIN IO_GP2INVERT IO_GP2IZCGLTCHFITR IO_GP2IZCSLEWFUTR IO_GP2DINSUPPLY 0x004B IO_GP4CFGLSB IO_GP4DIGDIRECTION IO_GP4OPENDRAIN	Output I/O ac A CMOS output b Noninverting Is not Filters is not Low 0x00	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN IO_GP3DRIVE 0x004C IO_GP5CFGMSB IO_GP5CFGMSB IO_GP5DTEST IO_GP5TESTSEL	DTESTO V Test path is disco No pull up or pL Min (20% of Ma 0x00 Test path is disco
	IO_MODECTRL2_REG IO_LD06_EN IO_LD04_EN IO_GP3CFGLSB IO_GP3OFENDRAIN IO_G93INVERT	U LDO6 Enabled LDO3 Enabled LDO4 Enabled LDO3 Disabled LDO2 Disabled DO1 Disabled (0x38 ** Output I/O acts Ii A CMOS output b Noninverting	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN IO_GP2DRIVE 0x004A IO_GP4CFGMSB IO_GP4DTEST IO_GP4TESTSEL IO_GP4PULLUPDOWN	DTESTO Test path is disco No pull up or pL Min (20% of Ma 0x00 Test path is disco No pull up or pL No pull up or pL V	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2OFENDRAIN IO_GP2IXVERT IO_GP2IZCGITCHFITR IO_GP2DISUBVERT IO_GP2DINSUPPLY 0X004B IO_GP4CFGLSB IO_GP4DIGDIRECTION IO_GP4DIGDIRECTION IO_GP4OFENDRAIN IO_GP4OFENDRAIN	Output I/O ac A CMOS output b Noninverting Is not Fitters is not Low 0x00	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN IO_GP3DRIVE 0x004C IO_GP5CFGMSB IO_GP5DTEST IO_GP5TESTSEL IO_GP5FULUPDOWN	DTESTO V Test path is disco No pull up or pu V Min (20% of Ma V 0x00 ••• DTESTO V Test path is disco No pull up or pu V
	IO_MODECTRL2_REG IO_LD06_EN IO_LD05_EN IO_LD04_EN IO_LD03_EN IO_LD02_EN IO_LD01_EN 0x0023	U LDO6 Enabled LDO5 Enabled LDO4 Enabled LDO3 Disabled LDO2 Disabled DO1 Disabled (x38 ************************************	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN IO_GP2DRIVE 0x004A IO_GP4CFGMSB IO_GP4DTEST IO_GP4TESTSEL IO_GP4DRIVE	DTESTO Test path is disco No pull up or pL v Min (20% of Ma v Dx00 Test path is disco No pull up or pL v Min (20% of Ma v	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2DENDRAIN IO_GP2IXVERT IO_GP2IZCGITCHFITR IO_GP2DISUEWFITR IO_GP2DINSUPPLY 0X004B IO_GP4DIGDIRECTION IO_GP4DIGDIRECTION IO_GP4DIGDIRECTION IO_GP4DIGDIRECTION IO_GP4IXCGITCHFITR	Output I/O ac A CMOS output b Noninverting Is not Fitters is not Low 0x00 ** Input Output dev A CMOS output b Noninverting Is not	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN IO_GP3DRIVE 0x004C IO_GP5CFGMSB IO_GP5DTEST IO_GP5TESTSEL IO_GP5ESTSEL IO_GP5EVILUPDOWN IO_GP5DRIVE	DTESTO Test path is disco No pull up or pu Min (20% of Ma Dx00 Test path is disco No pull up or pu Min (20% of Ma Min (20%
	IO_MODECTRL2_REG IO_LDO6_EN IO_LDO5_EN IO_LDO4_EN IO_LDO3_EN IO_LDO1_EN Ox0023	U LDO6 Enabled LDO5 Enabled LDO4 Enabled LDO3 Disabled LDO2 Disabled (DO1 Disabled (DV38) Coutput I/O acts II A CMOS output D Noninverting Is not Fitters is not	IO_GP2CFGMSB IO_GP2DTEST IO_GP2TESTSEL IO_GP2PULLUPDOWN IO_GP2DRIVE 0x004A IO_GP4CFGMSB IO_GP4DTEST IO_GP4DTEST IO_GP4DLUPDOWN IO_GP4DRIVE	DTESTO Test path is disco No pull up or pu Min (20% of Ma DTESTO Test path is disco No pull up or pu Min (20% of Ma	IO_GP2CFGLSB IO_GP2DIGDIRECTION IO_GP2OPENDRAIN IO_GP2I2CGITCHFITR IO_GP2I2CGITCHFITR IO_GP2DINSUPPLY OX004B IO_GP4CFGLSB IO_GP4DIGDIRECTION IO_GP4OPENDRAIN IO_GP4I2CGITCHFITR IO_GP4I2CGITCHFITR IO_GP4I2CSLEWFITR	Output I/O ac A CMOS output b Noninverting Is not Fitters is not Low 0x00 * Input Output dev A CMOS output b Noninverting Is not Fitters is not	IO_GP3CFGMSB IO_GP3DTEST IO_GP3TESTSEL IO_GP3PULLUPDOWN IO_GP3DRIVE 0x004C IO_GP5CFGMSB IO_GP5CFSTSEL IO_GP5TESTSEL IO_GP5ESTSEL IO_GP5DRIVE	DTESTO Vest path is disco No pull up or pu Min (20% of Ma Vest path is disco No pull up or pu Min (20% of Ma Vest path is disco No pull up or pu Min (20% of Ma Vest path is disco

Figure 6. Buck and LDO Regulator Output State

6. Revision History

Revision	Date	Description
1.00	Mar 7, 2025	Initial release.



Notice

- 1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
- Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
- 3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
- 4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
- 5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
- 6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
 - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

- 7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
- 8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
- 9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for systems manufactured by you.
- 10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- 11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
- 12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
- 13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
- 14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
- (Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Disclaimer Rev.5.0-1)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.