

RC2121xA

This document describes programming information for the RC2121xA. Detailed register definitions can be located by following the links in the document.

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1. Overview

The [Programming Description](#) section provides a high-level overview of registers that system software will typically interact with during system operation.

The [Registers](#) section provides detailed descriptions of all user-accessible registers in the device. These registers are loaded from OTP at boot time. OTP images are created using the Renesas [RICBox](#) software.

Note: For device information and electrical characteristics, see the [RC2121xA Datasheet](#).

2. Programming Description

2.1 Paging

The RC2121xA can be configured by OTP for 16 bits or 8 bits of internal I2C addressing. Internally registers are addressed by 16 bits. If 16 bit I2C addresses are used then paging is not used.

If the RC2121xA is configured for 8 bits of I2C addressing then paging must be used as described:

- Address 0xFC is the 32 bit page register, and is accessible independent of page register setting.
 - 0xFC – Write to 0x0.
 - 0xFD – Write page offset, this becomes the upper 8 bits of the internal address.
 - 0xFE – Write to 0x0.
 - 0xFF – Write to 0x0.

2.2 Scratch

S/W may make use of a dedicated scratch pad register.

- SCRATCH0: may be used as scratch pad.

2.3 Output Enables

Output Enables may be configured via OTP configuration to be under S/W register control, or pin control. The following describes the S/W register control. S/W register control takes precedence over pin control.

- Writing OUT_CTRL.out_dis to a “1” will always disable a particular output.
- Writing OUT_CTRL.out_dis to a “0” will enable a particular output if:
 - There is no OE pin associated with the output based on OTP configuration.
 - Or the OE pin is enabling the output.

2.4 GPIO Pins

The GPIO pins may be configured via OTP to have special functions, i.e. OE, or may be general purpose R/W bits. The following describes the S/W register control and status:

- GPO_CTRL: Will determine the output value, when configured as general purpose output.
- GPIO_STS.gpio_sts: Displays the current logic level of the pins.
- STARTUP_STS: Displays the logic level of the pins latched at power on.

2.5 GPI Pins

Note that GPI pins are only available in variants that use a single crystal.

The GPI pins may be configured via OTP to have special functions, i.e. OE, or may be general purpose RO bits. The following describes the S/W register status:

- GPIO_STS.gpi_sts: Displays the current logic level of the pins.

2.6 Event handling

Device Events are captured in the DEVICE_EVENT register. These events indicate that a monitor has detected an issue with the operation of the device. These bits are all RW1C, H/W sets the bit on the event, and S/W can clear individual bits by writing a 0x1 to the desired bit. Some of the events may persist, and H/W will immediately set the associated RW1C bit again. Events may be mapped to an interrupt see [Interrupts](#) or a fault see [Faults](#).

2.7 Interrupts

Events that are configured to an interrupt are programmed via the INT_EN register. When the corresponding bit is set in the DEVICE_EVENT register, and the event is enabled in the INT_EN register (and the device_int_en bit is set) then the INT GPIO pin is asserted, if the INT pin has been configured.

The interrupt handler should read the DEVICE_EVENT and INT_EN register to see what events have occurred and which are mapped to interrupts.

It is also possible to use polling for interrupt status via DEVICE_STS.device_int_sts, rather than the GPIO INT pin.

- DEVICE_EVENT: RW1C status bits for all events.
- INT_EN: RW control bits to select which events cause interrupts via GPIO pin.
- DEVICE_STS.device_int_sts: RO bit for interrupt status.

Once the interrupt source has been determined the associated interrupt should be cleared to prevent further interrupts from the same source. The process for this depends on the particular interrupt, as described in the following sections.

Table 1. DEVICE_EVENT Interrupt Type Mapping

| bit | field | type |
|------|----------------|------------|
| 0 | apll_lol | once |
| 1 | los0_evt | persistent |
| 2 | los1_evt | persistent |
| 3 | xtal_ppm_warn | persistent |
| 4 | xtal_ppm_err | persistent |
| 5 | xtal0_st_er | persistent |
| 6 | xtal1_st_er | persistent |
| 18:7 | freq[11:0]_evt | output |
| 19 | i2c_crc_err | once |
| 20 | dig_bist_fail | once |
| 21 | ana_bist_fail | once |
| 22 | csr_sig_fail | once |
| 23 | csr_sig_reload | once |
| 24 | xtal_switch | once |
| 25 | dual_xtal_fail | once |

Table 1. DEVICE_EVENT Interrupt Type Mapping (Cont.)

| bit | field | type |
|-----|---------------|------|
| 26 | otp_crc_err | once |
| 27 | otp_load_fail | once |

2.7.1 Persistent Type

Persistent type interrupts generally will continue to set the RW1C bit in the DEVICE_EVENT register, and thus clearing the interrupt RW1C bit is generally not effective. These interrupts should be cleared via INT_EN. When the interrupt is disabled it will not longer contribute to INT pin assertion. The RW1C bit in the DEVICE_EVENT register will continue operate.

2.7.2 Once Type

Once type interrupts generally will set the RW1C bit in the DEVICE_EVENT register once, and thus clearing the interrupt RW1C bit is generally effective. These interrupts should be cleared via RW1C bit in the DEVICE_EVENT register. When the interrupt RW1C is cleared it will no longer contribute to INT pin assertion.

2.7.3 Output type

These types refer to interrupts related to the output monitor. The interrupt handler should process these interrupts as follows:

- Write OUT_CTRL.out_dis with 1 to disable affected output, Note that H/W will automatically disable the output. Disabling the output via this register is required to keep it disabled while the interrupt is cleared.
- Write FREQ_CLOCK_SEL.freq_out_sel/freq_outb_sel to 0.
- write DEVICE_EVENT with 1 to clear RW1C bit.

When the interrupt RW1C is cleared it will no longer contribute to INT pin assertion.

2.8 Faults

Events that are configured to an fault are programed via the FAULT_EN register. When the corresponding bit is set in the DEVICE_EVENT register, and the event is enabled in the FAULT_EN register (and the device_fault_en bit is set) then the FAULT GPIO pin is asserted.

When a fault occurs the device goes to the safe state as described in the RC2121xA data sheet.

2.9 Direct Fault Insertion

To aid S/W development a direct fault insertion mechanism is available. The EVENT_GEN register contains bits that when written to a 0x1 trigger the corresponding bit in the DEVICE_EVENT register. This does not affect the operation of the RC2121xA, outputs, etc. continue to operate normally.

- EVENT_GEN: RW control bits to generate events.

2.10 Other Status Registers

The following registers contain status information that may be of interest to system S/W.

- DEVICE_STS.xtal_sel_sts: which crystal is currently used to lock the APLL.
- LOSMON_STS: status information on crystals.
- PPM_MON_STS: current ppm difference between the two crystals.

2.11 Fault Insertion

Fault insertion may also be performed by writing specific registers that cause an output or other circuit to fail. This will mimic the actual event, and outputs will be affected. This is provided to aid S/W development to various fault scenarios in RC2121xA. The registers that are used for fault insertion require that the lock bit be disabled. The lock bit prevents configurations registers, that should not be modified during normal operation, from being modified. The following assumes that the various monitors have been configured and enabled as part of the OTP image.

- REG_LOCK: clear register lock to perform fault insertion.
 - Register locking not implemented for TV, this step can be skipped.
- To set DEVICE_EVENT.apll_lol: read modify write APLL_FB_DIV_INT, by adding 2.
- To set DEVICE_EVENT.los0_evt: write LOSMON_CNFG_0.los_thresh to 0x1.
- To set DEVICE_EVENT.los1_evt: write LOSMON_CNFG_1.los_thresh to 0x1.
- To set DEVICE_EVENT.xtal_ppm_warn write PPM_CNFG.ppm_warn_thresh to 0x1.
- To set DEVICE_EVENT.xtal_ppm_err write PPM_CNFG.ppm_err_thresh to 0x1.
- To set DEVICE_EVENT.xtal0_st_err write ANA_CLK_EN.en_xtal0_hdiv_dig to 0x0.
- To set DEVICE_EVENT.xtal1_st_err write ANA_CLK_EN.en_xtal1_hdiv_dig to 0x0.
- To set DEVICE_EVENT.freq[11:0]_evt write FREQMON_THRESH_[11:0].freq_max_thresh 0x1.
 - Output must be enabled first.
 - Must be configured via OTP to have monitor active.
- To set DEVICE_EVENT.i2c_crc_err create I2C access with incorrect CRC.
- To set DEVICE_EVENT.dig_bist_fail write EVENT_GEN.dig_bist_fail_gen.
- To set DEVICE_EVENT.ana_bist_fail write EVENT_GEN.ana_bist_fail_gen.
- To set DEVICE_EVENT.csr_sig_fail: modify CSR_SIG.csr_sig_exp. Only works in device is configured to not reload registers on error.
- To set DEVICE_EVENT.csr_sig_reload: modify CSR_SIG.csr_sig_exp. Only works in device is configured to reload registers on error.
- To set DEVICE_EVENT.xtal_switch write LOSMON_CNFG_0.los_thresh to 0x1
- To set DEVICE_EVENT.dual_xtal_fail write LOSMON_CNFG_0.los_thresh to 0x1 and write LOSMON_CNFG_1.los_thresh to 0x1.
- To set DEVICE_EVENT.otp_crc_err write EVENT_GEN.otp_crc_err_gen.
- To set DEVICE_EVENT.otp_load_fail write EVENT_GEN.otp_load_fail_gen.

After a fault has been inserted a power on reset should be issued to return the device to normal operation.

3. Registers

Table 2. Registers

| Module Base Address (Hex) | Name | Module Description | Link |
|---------------------------|------------|---|-------------------------|
| 0x0 | GLOBAL | Global control and status registers | GLOBAL |
| 0x40 | SSI | I2C registers | SSI |
| 0x48 | XO[0] | XO control registers | XO |
| 0x4C | XO[1] | Same as XO[0] | XO |
| 0x50 | SYSDIV | System clock registers | SYSDIV |
| 0x58 | XTALMON | Crystal monitoring registers | XTALMON |
| 0x60 | LOSMON[0] | LOS monitor registers | LOSMON |
| 0x64 | LOSMON[1] | Same as LOSMON[0] | LOSMON |
| 0x70 | FREQMON[0] | Bank output frequency monitor registers | FREQMON |
| 0x78 | FREQMON[1] | Same as FREQMON[0] | FREQMON |
| 0x80 | FREQMON[2] | Same as FREQMON[0] | FREQMON |
| 0x88 | FREQMON[3] | Same as FREQMON[0] | FREQMON |
| 0x90 | FREQMON[4] | Same as FREQMON[0] | FREQMON |
| 0x98 | FREQMON[5] | Same as FREQMON[0] | FREQMON |
| 0xA0 | FREQMON[6] | Same as FREQMON[0] | FREQMON |
| 0xB0 | APLL | APLL control registers | APLL |
| 0xF0 | SSC[0] | Spread spectrum registers | SSC |
| 0xF4 | SSC[1] | Same as SSC[0] | SSC |
| 0x100 | IOD[0] | Integer Output Divider registers | IOD |
| 0x108 | IOD[1] | Same as IOD[0] | IOD |
| 0x110 | HPFOD[0] | High Performance Fractional Output Divider registers | HPFOD |
| 0x120 | HPFOD[1] | Same as HPFOD[0] | HPFOD |
| 0x130 | HPFOD[2] | Same as HPFOD[0] | HPFOD |
| 0x140 | DCD[0] | DCD control registers for HPFOD's | DCD |
| 0x150 | DCD[1] | Same as DCD[0] | DCD |
| 0x160 | DCD[2] | Same as DCD[0] | DCD |
| 0x170 | LPFOD[0] | Limited Performance Fractional Output Divider Registers | LPFOD |
| 0x180 | LPFOD[1] | Same as LPFOD[0] | LPFOD |
| 0x190 | OUT[0] | Output control registers | OUT |
| 0x194 | OUT[1] | Same as OUT[0] | OUT |
| 0x198 | OUT[2] | Same as OUT[0] | OUT |
| 0x19C | OUT[3] | Same as OUT[0] | OUT |
| 0x1A0 | OUT[4] | Same as OUT[0] | OUT |
| 0x1A4 | OUT[5] | Same as OUT[0] | OUT |
| 0x1A8 | OUT[6] | Same as OUT[0] | OUT |

Table 2. Registers

| Module Base Address (Hex) | Name | Module Description | Link |
|---------------------------|---------------|-------------------------------|----------------------------|
| 0x1AC | OUT[7] | Same as OUT[0] | OUT |
| 0x1B0 | OUT[8] | Same as OUT[0] | OUT |
| 0x1B4 | OUT[9] | Same as OUT[0] | OUT |
| 0x1B8 | OUT[10] | Same as OUT[0] | OUT |
| 0x1BC | OUT[11] | Same as OUT[0] | OUT |
| 0x1C0 | BANK[0] | Output bank control registers | BANK |
| 0x1C4 | BANK[1] | Same as BANK[0] | BANK |
| 0x1C8 | BANK[2] | Same as BANK[0] | BANK |
| 0x1CC | BANK[3] | Same as BANK[0] | BANK |
| 0x1D0 | BANK[4] | Same as BANK[0] | BANK |
| 0x1D4 | BANK[5] | Same as BANK[0] | BANK |
| 0x1D8 | BANK[6] | Same as BANK[0] | BANK |
| 0x1F0 | GPI[0] | GPI control registers, | GPI |
| 0x1F4 | GPI[1] | Same as GPI[0] | GPI |
| 0x200 | GPIO[0] | GPIO control registers | GPIO |
| 0x204 | GPIO[1] | Same as GPIO[0] | GPIO |
| 0x208 | GPIO[2] | Same as GPIO[0] | GPIO |
| 0x20C | GPIO[3] | Same as GPIO[0] | GPIO |
| 0x210 | GPIO[4] | Same as GPIO[0] | GPIO |
| 0x214 | GPIO[5] | Same as GPIO[0] | GPIO |
| 0x218 | GPIO[6] | Same as GPIO[0] | GPIO |
| 0x220 | INT | Interrupt and fault registers | INT |
| 0x280 | STATUS | Status registers | STATUS |
| 0x2C0 | DCD_STATUS[0] | DCD Status registers | DCD_STATUS |
| 0x2C8 | DCD_STATUS[1] | Same as DCD_STATUS[0] | DCD_STATUS |
| 0x2D0 | DCD_STATUS[2] | Same as DCD_STATUS[0] | DCD_STATUS |
| 0x2E0 | CTRL | Control registers | CTRL |

3.1 GLOBAL

Global control and status registers.

Table 3. GLOBAL Register Index

| Offset (Hex) | Register Module Base Address: 0x0 | |
|--------------|-----------------------------------|--|
| | Register Name | Register Description |
| 0x0 | VENDOR_ID | Vendor ID and Device ID Type |
| 0x2 | DEVICE_ID | Device ID |
| 0x4 | DEVICE_REV | Font ID, Analog Revision, and Digital Revision |
| 0x6 | DEVICE_PGM | Device Dash Code |

Table 3. GLOBAL Register Index

| Offset (Hex) | Register Module Base Address: 0x0 | |
|--------------|-----------------------------------|--|
| | Register Name | Register Description |
| 0x8 | DEVICE_CNFG | Device Configuration Settings |
| 0xC | CNFG_LOCK | OTP Lock Control |
| 0x14 | SW_RESET | Software Reset Bits |
| 0x1C | FREQ_WINDOW_CNFG | Frequency Monitor Window Configuration |
| 0x20 | FREQ_CLOCK_SEL | Output Frequency Monitor Control |
| 0x24 | MISC_CNFG | Configuration Settings |
| 0x2C | DIG_POST_CNFG | Digital POST Disable Controls |
| 0x30 | ANA_POST_CNFG | Analog POST Disable Controls |
| 0x34 | POST_FREQMON_CNFG | POST Output Frequency Monitor Configuration |
| 0x38 | POST_APLL_FB_DIV_LOL | POST APLL LOL Feedback Divider Integer Setting |
| 0x3C | POST_PPM_CNFG | POST Crystal PPM Monitor Configuration |
| 0x3E | POST_LOS_THRESH | POST LDO Bias Fault Detection Settings |

3.1.1 VENDOR_ID

Vendor ID and Device ID Type.

| VENDOR_ID Bit Field Descriptions | | | | |
|----------------------------------|-------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:12 | dev_id_type | RO | 0x1 | Device ID Block Type. A value of 0x1 indicates that this register is followed by a 16-bit Device ID register and an 16-bit Device Revision register, and a 16-bit Device Programming register. |
| 11 | reserved | RO | 0x0 | Reserved |
| 10:0 | vendor_id | RO | 0x33 | Vendor ID. IDT JEDEC ID. |

3.1.2 DEVICE_ID

Device ID.

| DEVICE_ID Bit Field Descriptions | | | | |
|----------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:0 | device_id | RW | 0x0 | Device ID. For default value refer to Product Identification. This field is write-able so it may be configured from OTP. |

3.1.3 DEVICE_REV

Font ID, Analog Revision, and Digital Revision.

| DEVICE_REV Bit Field Descriptions | | | | |
|-----------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:13 | reserved | RO | 0x0 | Reserved |
| 12:8 | font_id | RO | 0x1 | Font ID. Font ID to distinguish die variants. Decode as follows: 0x0 = Font 0 0x1 = Font 1 |
| 7:4 | ana_rev | RO | 0x2 | Hardware analog revision. Analog revision. Decode as follows: 0x1 = Test vehicle 0x2 = Rev A |
| 3:0 | dig_rev | RO | 0x2 | Hardware digital revision. Digital revision. Decode as follows: 0x1 = Test vehicle 0x2 = Rev A |

3.1.4 DEVICE_PGM

Device Dash Code.

| DEVICE_PGM Bit Field Descriptions | | | | |
|-----------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:0 | dash_code | RW | 0x0 | Dash code. Decimal value assigned by IDT to identify the user configuration loaded in OTP at the factory. This field is write-able and is configured from the OTP common configuration programmed at the factory. 0x0 = No user configurations are programmed at the factory |

3.1.5 DEVICE_CNFG

Device Configuration Settings.

| DEVICE_CNFG Bit Field Descriptions | | | | |
|------------------------------------|---------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:29 | reserved | RO | 0x0 | Reserved |
| 28:27 | vco_cal_timer | RW | 0x1 | Timeout timer value during VCO Calibration state. Sets the timeout timer allowed for VCO Calibration before that state times out in the startup process. If this is not set correctly to a value longer than the expected VCO calibration time, vco_timeout error can occur. 0x0 = 4 ms 0x1 = 8 ms 0x2 = 16 ms 0x3 = 32 ms |

| DEVICE_CNFG Bit Field Descriptions | | | | |
|------------------------------------|-------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 26 | float_vddo6 | RW | 0x0 | <p>Float VDDO6 Supply. Active high bit to enable Iref and Ibias to output divider LDO, output bank LDO, output divider IOD0 and output driver OUT11/11B in VDDO6 domain. iod_rst for IOD0 must be set to '1' if this bit is set to '1'. Only set this bit to '1' for configurations that do not use IOD0 or OUT11/11B from any divider.</p> <p>Must be set to 0x1 (disabled) when the VDDO6 pin floats.</p> <p>0x0 = reference currents enabled 0x1 = reference currents disabled</p> |
| 25 | float_vddo5 | RW | 0x0 | <p>Float VDDO5 Supply. Active high bit to disable Iref and Ibias to output divider LDO, output bank LDO, output divider IOD1 and output driver OUT10/10B in VDDO5 domain. iod_rst for IOD1 must be set to '1' if this bit is set to '1'. Only set this bit to '1' for configurations that do not use IOD1 or OUT10/10B from any divider.</p> <p>Must be set to 0x1 (disabled) when the VDDO5 pin floats.</p> <p>0x0 = reference currents enabled 0x1 = reference currents disabled</p> |
| 24 | float_vddo4 | RW | 0x0 | <p>Float VDDO4 Supply. Active high bit to disable Iref and Ibias to output divider LDO, output bank LDO, output divider HPFOD2 and output driver OUT/OUTB 8,9 in VDDO4 domain. hpfod_rst for HPFOD2 must be set to '1' if this bit is set to '1'. Only set this bit to '1' for configurations that do not use HPFOD2 or any of OUT/OUTB 8,9 from any divider.</p> <p>Must be set to 0x1 (disabled) when the VDDO4 pin floats.</p> <p>0x0 = reference currents enabled 0x1 = reference currents disabled</p> |
| 23 | float_vddo3 | RW | 0x0 | <p>Float VDDO3 Supply. Active high bit to disable Iref and Ibias to output divider LDO, output bank LDO, output divider HPFOD1 and output driver OUT/OUTB 4-7 in VDDO3 domain. hpfod_rst for HPFOD1 must be set to '1' if this bit is set to '1'. Only set this bit to '1' for configurations that do not use HPFOD1 or any of OUT/OUTB 4-7 from any divider.</p> <p>Must be set to 0x1 (disabled) when the VDDO3 pin floats.</p> <p>0x0 = reference currents enabled 0x1 = reference currents disabled</p> |
| 22 | float_vddo2 | RW | 0x0 | <p>Float VDDO2 Supply. Active high bit to disable Iref and Ibias to output divider LDO, output bank LDO, output divider HPFOD0 and output driver OUT/OUTB 2,3 in VDDO2 domain. hpfod_rst for HPFOD0 must be set to '1' if this bit is set to '1'. Only set this bit to '1' for configurations that do not use HPFOD0 or any of OUT/OUTB 2,3 from any divider.</p> <p>Must be set to 0x1 (disabled) when the VDDO2 pin floats.</p> <p>0x0 = reference currents enabled 0x1 = reference currents disabled</p> |
| 21 | float_vddo1 | RW | 0x0 | <p>Float VDDO1 Supply. Active high bit to disable Iref and Ibias to output divider LDO, output bank LDO, output divider LPFOD1 and output driver OUT1/1B in VDDO1 domain. lpfod_rst for LPFOD1 must be set to '1' if this bit is set to '1'. Only set this bit to '1' for configurations that do not use LPFOD1 or OUT1/1B from any divider.</p> <p>Must be set to 0x1 (disabled) when the VDDO1 pin floats.</p> <p>0x0 = reference currents enabled 0x1 = reference currents disabled</p> |

| DEVICE_CNFG Bit Field Descriptions | | | | |
|------------------------------------|---------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 20 | float_vddo0 | RW | 0x0 | <p>Float VDDO0 Supply. Active high bit to disable Iref and Ibias to output divider LDO, output bank LDO, output divider LPFOD0 and output driver OUT0/0B in VDDO0 domain. Ipfod_rst for LPFOD0 must be set to '1' if this bit is set to '1'. Only set this bit to '1' for configurations that do not use LPFOD0 or OUT0/0B from any divider.</p> <p>Must be set to 0x1 (disabled) when the VDDO0 pin floats.</p> <p>0x0 = reference currents enabled 0x1 = reference currents disabled</p> |
| 19:16 | sync_dis_wait | RW | 0x2 | <p>Divider Synchronization Output Clock Disable Wait Time. During the divider synchronization procedure, after deasserting the output enable to the affected output drivers, the control logic waits for this period of time before stopping the clocks and synchronizing the dividers. This must be set longer than the period of the slowest output clock, and longer than the SSC modulation interval (if enabled).</p> <p>0x0 = 1us 0x1 = 2us 0x2 = 4us 0x3 = 8us 0x4 = 16us 0x5 = 32us 0x6 = 64us 0x7 = 128us 0x8 = 256us 0x9 = 512us</p> |
| sync_dis_wait (continued) | | | | <p>0xA = 1024us 0xB = 2048us 0xC = 4096us</p> |
| 15 | digldo_cnf | RW | 0x0 | <p>Digital LDO voltage select. Selects the digital LDO voltage level. This setting is intended for test purposes only. This is controlled by scan_control[6] during scan mode.</p> <p>0x0 = 1.25V 0x1 = 1.32V</p> |
| 14:12 | xo_delay | RW | 0x0 | <p>Crystal Startup Delay. Selects the wait time for the XO during the startup sequence. The default setting of 1 ms should be sufficient for all crystals. This setting is intended for debug purposes only.</p> <p>0x0 = 1 ms 0x1 = 2.5 ms 0x2 = 5 ms 0x3 = 7.5 ms 0x4 = 10 ms 0x5 = 0.5 ms 0x6 = 15 ms 0x7 = (10 us, for simulation speedup)</p> |

| DEVICE_CNFG Bit Field Descriptions | | | | |
|------------------------------------|--------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 11:8 | static_csel2 | RW | 0x2 | Static Configuration Select Bit 2. Selects the GPIO pin or fixed value used for static configuration select bit index 2. 0x0 = GPIO0 0x1 = GPIO1 0x2 = GPIO2 0x3 = GPIO3 0x4 = GPIO4 0x5 = GPIO5 0x6 = GPIO6 0xE = No pin selected, treated as 0 0xF = No pin selected, treated as 1 |
| 7:4 | static_csel1 | RW | 0x1 | Static Configuration Select Bit 1. Selects the GPIO pin or fixed value used for static configuration select bit index 1. 0x0 = GPIO0 0x1 = GPIO1 0x2 = GPIO2 0x3 = GPIO3 0x4 = GPIO4 0x5 = GPIO5 0x6 = GPIO6 0xE = No pin selected, treated as 0 0xF = No pin selected, treated as 1 |
| 3:0 | static_csel0 | RW | 0x0 | Static Configuration Select Bit 0. Selects the GPIO pin or fixed value used for static configuration select bit index 0. 0x0 = GPIO0 0x1 = GPIO1 0x2 = GPIO2 0x3 = GPIO3 0x4 = GPIO4 0x5 = GPIO5 0x6 = GPIO6 0xE = No pin selected, treated as 0 0xF = No pin selected, treated as 1 |

3.1.6 CNFG_LOCK

OTP Lock Control.

| CNFG_LOCK Bit Field Descriptions | | | | |
|----------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:1 | reserved | RO | 0x0 | Reserved |
| 0 | otp_lock | RW1S | 0x0 | OTP Lock. Prevents OTP programming when set to 1. This bit cannot be cleared by software. It is reset when the device is power cycled. Not used for TV. |

3.1.7 SW_RESET

Software Reset Bits.

| SW_RESET Bit Field Descriptions | | | | |
|---------------------------------|-----------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:12 | reserved | RO | 0x0 | Reserved |
| 11 | ssc_sw_rst | RW | 0x0 | Spread Spectrum Engine Software reset. The Spread Spectrum block is held in reset while this bit is set to 1. This bit will reset the divider to HPFOD0 and HPFOD1. Do not set this bit to 1 while HPFOD0 or HPFOD1 are in use. |
| 10 | xtalsw_sw_rst | RW | 0x0 | Crystal switching block Software reset. The Crystal switching block is held in reset while the corresponding bit is set to 1. |
| 9:5 | reserved | RO | 0x0 | Reserved |
| 4 | freqmon_sw_rst | RW | 0x0 | Output Frequency Monitor Software reset. The Output Frequency Monitor is held in reset while the corresponding bit is set to 1. |
| 3 | st_mon_sw_rst | RW | 0x0 | Crystal Short Term Monitor Software reset. The Crystal Short Term Monitor is held in reset while this corresponding bit is set to 1. |
| 2 | xtal_ppm_sw_rst | RW | 0x0 | Crystal PPM Monitor Software reset. The Crystal PPM Monitor is held in reset while this corresponding bit is set to 1. |
| 1:0 | losmon_sw_rst | RW | 0x0 | Crystal LOS Monitor Software reset. A Crystal LOS Monitor is held in reset while the corresponding bit is set to 1. Bit [1] = Crystal 1 LOS Monitor Bit [0] = Crystal 0 LOS Monitor |

3.1.8 FREQ_WINDOW_CNFG

Frequency Monitor Window Configuration.

| FREQ_WINDOW_CNFG Bit Field Descriptions | | | | |
|---|------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:24 | reserved | RO | 0x0 | Reserved |
| 23:16 | freq_slow_window | RW | 0x0 | Frequency Monitor Slow Window. Sets the duration of the slow frequency monitoring window, counted in fast frequency monitoring windows. Each frequency monitor independently selects the slow or fast window with freq_window_sel. |
| 15:0 | freq_fast_window | RW | 0x0 | Frequency Monitor Fast Window. Sets the duration of the fast frequency monitoring window, counted in crystal clock cycles. Each frequency monitor independently selects the slow or fast window with freq_window_sel. Minimum size for operation is 2. |

3.1.9 FREQ_CLOCK_SEL

Output Frequency Monitor Control.

| FREQ_CLOCK_SEL Bit Field Descriptions | | | | |
|---------------------------------------|------------|------------|---------------|-------------|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:25 | reserved | RO | 0x0 | Reserved |

| FREQ_CLOCK_SEL Bit Field Descriptions | | | | |
|---------------------------------------|---------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 24 | fm_shutdown | RW | 0x0 | Shutdown for output frequency monitoring. When set to 0x0, monitoring is enabled using the freq_out_sel and freq_outb_sel bits. When set to 0x1, all output frequency monitoring is disabled. 0x0 = enabled 0x1 = disabled |
| 23:12 | freq_outb_sel | RW | 0x0 | Complementary Output Clock Frequency Monitor Selection. Selects the complementary clock outputs (OUTxB) to monitor with the frequency monitors. The frequency monitor for the output clock's bank must be enabled and configured according to the expected frequency. If a freq_outb_sel bit is disabled (set to 0), that clocks freq_outb_sts will be set to '0'. Bit [11] = Enable Complementary Output Clock 11 frequency monitoring ... Bit [0] = Enable Complementary Output Clock 0 frequency monitoring |
| 11:0 | freq_out_sel | RW | 0x0 | Output Clock Frequency Monitor Selection. Selects the true clock outputs (OUTx) to monitor with the frequency monitors. The frequency monitor for the output clock's bank must be enabled and configured according to the expected frequency. If a freq_out_sel bit is disabled (set to 0), that clocks freq_out_sts will be set to '0'. Bit [11] = Enable Output Clock 11 frequency monitoring ... Bit [0] = Enable Output Clock 0 frequency monitoring |

3.1.10 MISC_CNFG

Configuration Settings.

| MISC_CNFG Bit Field Descriptions | | | | |
|----------------------------------|----------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:26 | reserved | RO | 0x0 | Reserved |
| 25 | sel_orig_ref_clock | RW | 0x0 | Controls which reference clock is used for VCO calibration and the frequency monitor. When set to 0x0, the vco calibration and output frequency monitor use the resampled reference clock. When set to 0x1, the vco_calibration and output frequency monitor uses the original non-resampled reference clock. This should be used if the reference clock will be faster than the maximum supported XTAL of 62.5MHz. 0x0 = resampled reference clock 0x1 = original reference clock |
| 24 | rstcon_enable_events | RW | 0x0 | Enable events during boot. When set, this bit allows the events to be latched during the boot procedure. When cleared (default behavior), event latching is disabled during boot and only is allowed after the reset procedure has finished. 0x0 = latching enable after boot 0x1 = latching enabled during boot |
| 23:19 | dcd_slow_update_rate | RW | 0x10 | DCD Calibration Slow Filter Update Rate. The DCD calibration slow filter mode update rate (in Hz) is: $1e6 \text{ Hz} / (2^{\text{dcd_slow_update_rate}})$ The valid range is 0 (1 MHz) to 20 (approximately 1 Hz). The default setting is ~15kHz. This setting is common to all FODs. |

| MISC_CNFG Bit Field Descriptions | | | | |
|----------------------------------|----------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 18:16 | dcd_slow_start_delay | RW | 0x5 | DCD Calibration Slow Filter Start Delay. When dcd_slow_en is set to 1, this setting specifies a delay before the slow filter mode is enabled internally, following the end of accelerated calibration. 0x0 = 0ms (no delay, enabled immediately) 0x1 = 1 ms 0x2 = 10 ms 0x3 = 100 ms 0x4 = 1 s 0x5 = 10 s 0x6 = 100 s |
| 15:14 | out_startup | RW | 0x0 | Output / monitoring disable on startup until PLL locks. Controls whether the clock output drivers / clock monitoring are disabled until the APLL locks during the startup sequence. 0x0: Clock output drivers / clock monitoring are disabled until APLL lock asserts 0x2: Clock output drivers /clock monitoring are not disabled by APLL lock status 0x0 = disabled until APLL lock 0x2 = unaffected by APLL lock status |
| 13:8 | reserved | RO | 0x0 | Reserved |
| 7 | ssc_sync | RW | 0x0 | Spectrum Spreading Sync. When the two SSC engines have the same modulation frequency, setting this bit to 1 aligns the phase of SSC 1 to SSC 0. Refer to ssc_en for restrictions on enabling the SSCs when ssc_sync is set to 1. Note: This field was named ssc_share in VC7. 0x0 = SSC 1 operates independently 0x1 = SSC 1 phase is aligned to SSC 0 |
| 6 | xtal_sel_pri | RW | 0x0 | Automatic Crystal Selection Priority. Sets the relative priority of the two crystals for automatic selection on device startup when both crystals are valid. 0x0 = Crystal 0 has priority over crystal 1 0x1 = Crystal 1 has priority over crystal 0 |
| 5 | reserved | RO | 0x0 | Reserved |
| 4:3 | xtal_sel_mode | RW | 0x2 | Crystal Selection Mode. Controls how the APLL reference crystal is selected. Automatic mode (option 0x2) is based on Crystal LOS and short term monitors and GPIO pin if in gpio_func 0x6 mode 0x0 = Force primary crystal 0x1 = Force backup crystal 0x2 = Automatic |
| 2 | reserved | RO | 0x0 | Reserved |

| MISC_CNFG Bit Field Descriptions | | | | |
|----------------------------------|------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 1 | csr_sig_err_mode | RW | 0x0 | <p>CSR Signature Check Error Mode. Determines the behavior when the CSR signature check detects an error.</p> <p>0x0: Set csr_sig_fail. The csr_sig_fail_fault_en bit would typically be set to 1, allowing the device to enter the safe state and assert the FAULT output.</p> <p>0x1: Set csr_sig_reload. The outputs are disabled, the user configuration is reloaded from OTP (with the exception of certain register fields), and the normal power-up sequence begins. The csr_sig_reload_int_en bit would typically be set to 1 so that the INT output asserts to notify the system.</p> <p>0x0 = Set csr_sig_fail 0x1 = Set csr_sig_reload</p> |
| 0 | csr_sig_timer | RW | 0x0 | <p>CSR Signature Check Timer Interval. Determines the interval at which the device self-checks the CSR signature.</p> <p>0x0 = Disabled 0x1 = 10ms</p> |

3.1.11 DIG_POST_CNFG

Digital POST Disable Controls.

| DIG_POST_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|-------------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:24 | reserved | RO | 0x0 | Reserved |
| 23 | csr_sig_post_dis | RW | 0x0 | CSR Signature Monitor POST Disable. When 1, disables CSR Signature Monitor Power on Self Test. |
| 22 | dual_xtal_fail_post_dis | RW | 0x0 | Dual XTAL Fail POST Disable. When 1, disables Dual XTAL failure Power on Self Test. Both XTALs must be enabled and POST_LOS_THRESH register must be programmed correctly to enable this POST test. |
| 21 | xtal_sw_post_dis | RW | 0x0 | XTAL Switching POST Disable. When 1, disables XTAL switching Power on Self Test. Both XTALs must be enabled and POST_LOS_THRESH register must be programmed correctly to enable this POST test. |
| 20:9 | freq_post_dis | RW | 0x0 | Output Frequency Monitor Fault Injection POST Disable. When 1, disables Frequency Monitor Power on Self Test for the given output. Enable this POST test only for correctly configured outputs/outputs that have monitoring enabled in FREQ_CLOCK_SEL. freq_post_dis must be set to '1' for any outputs where both freq_out_sel = 0 and freq_outb_sel = 0 unless all 12 freq_out_sel and freq_outb_sel bits are 0- then the Frequency Monitor Power on Self Test will be skipped automatically. POST_FREQMON_CNFG register must be programmed correctly to enable this POST test. |
| 8 | xtal1_st_err_post_dis | RW | 0x0 | XTAL1 Short Term POST Disable. When 1, disables XTAL1 Short Term Monitor Power on Self Test. Both XTALs must be enabled and ST_CNFG register must be programmed correctly to enable this POST test. |
| 7 | xtal0_st_err_post_dis | RW | 0x0 | XTAL0 Short Term POST Disable. When 1, disables XTAL0 Short Term Monitor Power on Self Test. Both XTALs must be enabled and ST_CNFG register must be programmed correctly to enable this POST test. |

| DIG_POST_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 6 | xtal_ppm_err_post_dis | RW | 0x0 | XTAL PPM Error POST Disable. When 1, disables XTAL PPM Error Power on Self Test. Both XTALs must be enabled and POST_PPM_CNFG register must be programmed correctly to enable this POST test. |
| 5 | xtal_ppm_warn_post_dis | RW | 0x0 | XTAL PPM Warning POST Disable. When 1, disables XTAL PPM Warning Power on Self Test. Both XTALs must be enabled and POST_PPM_CNFG register must be programmed correctly to enable this POST test. |
| 4 | los1_post_dis | RW | 0x0 | XTAL1 LOS POST Disable. When 1, disables XTAL1 Loss of Signal Power on Self Test. XTAL1 must be enabled and POST_LOS_THRESH register and LOSMON_CNFG register must be programmed correctly to enable this POST test. |
| 3 | los0_post_dis | RW | 0x0 | XTAL0 LOS POST Disable. When 1, disables XTAL0 Loss of Signal Power on Self Test. XTAL0 must be enabled and POST_LOS_THRESH register and LOSMON_CNFG register must be programmed correctly to enable this POST test. |
| 2 | apll_lol_post_dis | RW | 0x0 | APLL LOL POST Disable. When 1, disables APLL Loss of Lock Power on Self Test. POST_APLL_FB_DIV_LOL register must be programmed correctly to enable this POST test. |
| 1 | lbist_dis | RW | 0x1 | Digital LBIST Disable. When 1, disables digital logic BIST to run at startup. LBIST_SIGNATURE.lbist_signature must be set correctly in OTP for the length of time LBIST will run if lbist_dis is set to 0 in OTP. |
| 0 | dig_post_dis | RW | 0x0 | POST Disable. When 1, disables all Digital Power on Self Test to run when Power on self test is triggered including anything enabled in DIG_POST_CNFG. |

3.1.12 ANA_POST_CNFG

Analog POST Disable Controls.

| ANA_POST_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|---------------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:21 | reserved | RO | 0x0 | Reserved |
| 20 | bias_cal_ana_post_exclude | RW | 0x0 | Bias Calibration Exclude for Analog POST. When 1, excludes the Bias Calibration pass/fail status in the Analog POST status. |
| 19 | vco_cal_ana_post_exclude | RW | 0x0 | VCO Calibration Exclude for Analog POST. When 1, excludes the VCO Calibration pass/fail status in the Analog POST status. |
| 18 | ana_post_ldo_low_fault_det_dis | RW | 0x0 | Analog LDO Low Fault Detection POST Disable. When 1, disables Analog LDO Low Fault Detection POST to run when Power on Self Test is triggered. |
| 17 | ana_post_ldo_in_range_det_dis | RW | 0x0 | Analog LDO In Range Detection POST Disable. When 1, disables Analog LDO In Range Detection POST to run when Power on Self Test is triggered. |
| 16 | ana_post_ldo_high_fault_det_dis | RW | 0x0 | Analog LDO High Fault Detection POST Disable. When 1, disables Analog LDO High Fault Detection POST to run when Power on Self Test is triggered. |
| 15 | ana_post_ref_x1_ldo_dis | RW | 0x0 | Analog Reference X1 LDO POST Disable. When 1, disables Analog X1 Reference LDO POST to run when Power on Self Test is triggered. |

| ANA_POST_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|----------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 14 | ana_post_ref_x0_ldo_dis | RW | 0x0 | Analog Reference X0 LDO POST Disable. When 1, disables Analog X0 Reference LDO POST to run when Power on Self Test is triggered. |
| 13 | ana_post_apll_cp_ldo_dis | RW | 0x0 | Analog APLL CP LDO POST Disable. When 1, disables Analog APLL CP LDO POST to run when Power on Self Test is triggered. |
| 12 | ana_post_apll_pfd_ldo_dis | RW | 0x0 | Analog APLL PFD LDO POST Disable. When 1, disables Analog APLL PFD LDO POST to run when Power on Self Test is triggered. |
| 11 | ana_post_apll_vco_ldo_dis | RW | 0x0 | Analog APLL VCO LDO POST Disable. When 1, disables Analog APLL VCO LDO POST to run when Power on Self Test is triggered. |
| 10 | ana_post_od_iod0_ldo_dis | RW | 0x0 | Analog IOD0 Output Divider LDO POST Disable. When 1, disables Analog IOD0 Output Divider LDO POST to run when Power on Self Test is triggered. |
| 9 | ana_post_od_iod1_ldo_dis | RW | 0x0 | Analog IOD1 Output Divider LDO POST Disable. When 1, disables Analog IOD1 Output Divider LDO POST to run when Power on Self Test is triggered. |
| 8 | ana_post_od_hpfod2_ldo_dis | RW | 0x0 | Analog HPFOD2 Output Divider LDO POST Disable. When 1, disables Analog HPFOD2 Output Divider LDO POST to run when Power on Self Test is triggered. |
| 7 | ana_post_od_hpfod1_ldo_dis | RW | 0x0 | Analog HPFOD1 Output Divider LDO POST Disable. When 1, disables Analog HPFOD1 Output Divider LDO POST to run when Power on Self Test is triggered. |
| 6 | ana_post_od_hpfod0_ldo_dis | RW | 0x0 | Analog HPFOD0 Output Divider LDO POST Disable. When 1, disables Analog HPFOD0 Output Divider LDO POST to run when Power on Self Test is triggered. |
| 5 | ana_post_od_lpfod1_ldo_dis | RW | 0x0 | Analog LPFOD1 Output Divider LDO POST Disable. When 1, disables Analog LPFOD1 Output Divider LDO POST to run when Power on Self Test is triggered. |
| 4 | ana_post_od_lpfod0_ldo_dis | RW | 0x0 | Analog LPFOD0 Output Divider LDO POST Disable. When 1, disables Analog LPFOD0 Output Divider LDO POST to run when Power on Self Test is triggered. |
| 3 | ana_post_dig_fod_ldo_dis | RW | 0x0 | Analog Digital FOD LDO POST Disable. When 1, disables Analog Digital FOD LDO POST to run when Power on Self Test is triggered. |
| 2 | ana_post_dig_apll_ldo_dis | RW | 0x0 | Analog Digital APLL Divider LDO POST Disable. When 1, disables Analog Digital APLL Divider LDO POST to run when Power on Self Test is triggered. |
| 1 | ana_post_dig_block_ldo_dis | RW | 0x0 | Analog Digital Block LDO POST Disable. When 1, disables Analog Digital Block LDO POST to run when Power on Self Test is triggered. |
| 0 | ana_post_dis | RW | 0x0 | Analog POST Disable. When 1, disables all analog LDO POST to run when Power on Self Test is triggered. |

3.1.13 POST_FREQMON_CNFG

POST Output Frequency Monitor Configuration.

| POST_FREQMON_CNFG Bit Field Descriptions | | | | |
|--|----------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:20 | post_freq_window | RW | 0x1F4 | POST Monitor Fast Window. Sets the duration of the frequency monitoring window, counted in crystal clock cycles during POST. During POST the output dividers are used internally and forced to divide by 100 (example 100 MHz for 10 GHz VCO). Minimum size for operation is 2. This register must be set correctly for POST to pass. 10us duration required. |
| 19:10 | post_freq_max_thresh | RW | 0x1FF | POST Frequency Monitor Max Threshold. This gives the number of rising edges of the monitored clock at the end of a monitoring window during POST. Set for divider of 100 during POST. This register field or post_freq_min_threshold must be set to a value to cause a frequency error out of range for POST to pass. Set to 0 to disable the frequency monitor POST check. |
| 9:0 | post_freq_min_thresh | RW | 0xF | POST Frequency Monitor Min Threshold. This gives the number of rising edges of the monitored clock at the end of a monitoring window during POST. Set for divider of 100 during POST. This register field or post_freq_max_threshold must be set to a value to cause a frequency out of range error for POST to pass. |

3.1.14 POST_APLL_FB_DIV_LOL

POST APLL LOL Feedback Divider Integer Setting.

| POST_APLL_FB_DIV_LOL Bit Field Descriptions | | | | |
|---|----------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:12 | reserved | RO | 0x0 | Reserved |
| 11:10 | post_apll_lock_timer | RW | 0x2 | POST APLL Lock Timer. Controls the digital debounce interval for the lock indication for the APLL during POST. This duration is a function of the system clock cycles. 0x0 = 5 cycles of the system clock 0x1 = 285 cycles of the system clock 0x2 = 2850 cycles of the system clock 0x3 = 28500 cycles of the system clock. |
| 9:0 | post_apll_fb_div_lol | RW | 0x91 | POST APLL Feedback Divider Integer designed to cause APLL LOL. POST APLL feedback divider integer value error value to force a Loss-of-Lock- Recommend adding 40 to correct apll_fb_div value-adjust as needed based on correct value. |

3.1.15 POST_PPM_CNFG

POST Crystal PPM Monitor Configuration.

| POST_PPM_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|----------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:8 | post_ppm_err_thresh | RW | 0x3 | POST Crystal PPM Monitor Error Threshold. If the difference between the crystal counters at the end of the monitoring window exceeds this threshold, then the xtal_ppm_err bit is set. The granularity is 2 ppm/lsb. This register must be set correctly for POST to pass. Set to 0 to disable the check. |
| 7:0 | post_ppm_warn_thresh | RW | 0x1 | POST Crystal PPM Monitor Warning Threshold. If the difference between the crystal counters at the end of the monitoring window exceeds this threshold, but does not exceed ppm_err_thresh, then the xtal_ppm_warn bit is set. The granularity is 2 ppm/lsb. This register must be set correctly for POST to pass. Set to 0 to disable the check. |

3.1.16 POST_LOS_THRESH

POST LDO Bias Fault Detection Settings.

| POST_LOS_THRESH Bit Field Descriptions | | | | |
|--|-----------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | post_los_thresh_scale | RW | 0x0 | Scaling applied to LOSMON_CNFG.los_thresh during POST. Scales LOSMON_CNFG.los_thresh to allow for LOS check with unlocked APLL during POST. 0x0 = Increase value by 25% up to max 0x1 = Increase value by 50% up to max |
| 6:0 | post_los_thresh_det | RW | 0x1 | LOS Threshold to generate LOS detection for POST. Sets the maximum number of VCO calibration clock (593MHz to 669MHz) cycles from any rising edge of the crystal clock to the next rising edge, and from any falling edge to the next falling edge. If this threshold is reached before the next edge occurs in the same direction, then the monitor's los_sts and losX_evt bits are set; los_sts will remain set until the next crystal rising or falling edge occurs. Set to a value to cause LOS detection to trigger in POST (recommended 0x1). This register must be set correctly for POST to pass. LOSMON_CNFG.los_thresh must also be programmed correctly for POST to pass. |

3.2 SSI

I2C registers.

Table 4. SSI Register Index

| Offset (Hex) | Register Module Base Address: 0x40 | |
|--------------|------------------------------------|---------------------------|
| | Register Name | Register Description |
| 0x0 | I2C_FLTR_CNFG | I2C Filter Settings |
| 0x1 | I2C_TIMING_CNFG | I2C Timing Configuration |
| 0x2 | I2C_ADDR_CNFG | I2C Address Configuration |
| 0x3 | SSI_GLOBAL_CNFG | I2C Global Configuration |

3.2.1 I2C_FLTR_CNFG

I2C Filter Settings.

| I2C_FLTR_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|---------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:4 | reserved | RO | 0x0 | Reserved |
| 3:0 | i2c_spike_ftr | RW | 0x3 | I2C digital spike filter duration. Controls the duration of the digital spike filters on the SCL and SDA inputs, specified in number of system clock cycles (16.7 ns). 0 disables filtering. |

3.2.2 I2C_TIMING_CNFG

I2C Timing Configuration.

| I2C_TIMING_CNFG Bit Field Descriptions | | | | |
|--|-------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:4 | i2c_sda_high_hold | RW | 0x2 | I2C transmit one bit delay. Delays transmission of '1' value by this number of 133ns periods (8 system clock cycles). |
| 3:0 | i2c_sda_low_hold | RW | 0x2 | I2C transmit zero bit delay. Delays transmission of '0' value by this number of 133ns periods (8 system clock cycles). Allows data-hold-times on strongly pulled-down '0' value bits to be set to match data-hold-times on weakly (resistively) pulled-up '1' value bits. |

3.2.3 I2C_ADDR_CNFG

I2C Address Configuration.

| I2C_ADDR_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | reserved | RO | 0x0 | Reserved |
| 6:0 | i2c_addr | RW | 0x9 | I2C device address. Sets I2C device address that the SSI will acknowledge and accept accesses on. |

3.2.4 SSI_GLOBAL_CNFG

I2C Global Configuration.

| SSI_GLOBAL_CNFG Bit Field Descriptions | | | | |
|--|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:6 | reserved | RO | 0x0 | Reserved |
| 5 | i2c_crc_en | RW | 0x0 | I2C CRC Enable. Enables the I2C CRC check. 0x0 = CRC disabled 0x1 = CRC enabled |

| SSI_GLOBAL_CNFG Bit Field Descriptions | | | | |
|--|---------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 4:3 | sda_drv | RW | 0x0 | I2C Drive Strength. Selects the operating speed of the interface when configured for I2C mode. Only the output driver slew rate is affected by this setting (higher settings means higher drive strength). The I2C master must provide the appropriate SCL frequency and other timing requirements according to the selected speed. Drive strength increases as this setting increases. 0x0: 1.8V Standard mode (100 kHz) or 2.5V/3.3V standard (100kHz) and Fast mode (400kHz) 0x1: 1.8V Fast mode (400 kHz) 0x2: reserved 0x3: 1.8V/2.5V/3.3V Fast mode plus (1 MHz) 0x0 = 100kHz (1.8V), 400kHz (2.5V/3.3V) 0x1 = 400kHz (1.8V) 0x3 = 1MHz (1.8V/2.5V/3.3V) |
| 2 | ssi_addr_size | RW | 0x0 | SSI address size. When '0' the SSI expects 1-byte CSR addresses; when '1' the SSI expects 2-byte CSR addresses. Upper address bits are taken from the SSI's page register to create a full 16-bit CSR address. 0x0 = 1-byte address 0x1 = 2-byte address |
| 1:0 | ssi_enable | RW | 0x1 | SSI mode. Selects the serial interface mode. 0x0 = SSI is disabled 0x1 = SSI is in I2C mode |

3.3 XO

XO control registers.

Table 5. XO Register Index

| Offset (Hex) | Register Module Base Address: 0x48 | |
|--------------|------------------------------------|----------------------|
| | Register Name | Register Description |
| 0x0 | XO_CNFG | XO Configuration |

3.3.1 XO_CNFG

XO Configuration.

| XO_CNFG Bit Field Descriptions | | | | |
|--------------------------------|------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:30 | reserved | RO | 0x0 | Reserved |
| 29 | xo_ib_h_div_setb | RW | 0x1 | XO / Input Buffer High Frequency Divider Set. When cleared, the XO/IB high frequency divider is held in set mode (bit is active low). |
| 28:24 | xo_ib_h_div | RW | 0x0 | XO / Input Buffer high frequency divide ratio. Divide by 2 to 31. Bypass if set to 0. 1 is reserved. |

| XO_CNFG Bit Field Descriptions | | | | |
|--------------------------------|------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 23:22 | en_gain | RW | 0x1 | XO gain boosting control. Selects the number of gain boosting amplifiers enabled during startup. 0x0 = Gain boosting amplifiers are disabled 0x1 = One parallel amplifier is enabled 0x2 = Two parallel amplifiers are enabled 0x3 = All three parallel amplifiers are enabled |
| 21:16 | en_cap_x2 | RW | 0x28 | XO capacitance at X2 terminal. Controls the internal capacitance applied at the X2 terminal (XOUT_REFINb device pin)/connected to the integrated crystal. The capacitance rises monotonically in steps of 0.375fF from 0pF to 24pF as the control setting increases from 0x00 to the maximum of 0x3F. This must be set to 0 when sel_ib_xo is set to 0. |
| 15 | reserved | RO | 0x0 | Reserved |
| 14 | xo_buff_dis | RW | 0x0 | XO buffer disable. Forces the XO buffer to the core logic to be disabled. This setting is intended for debug purposes only. When the XO buffer is enabled (option 0x0), it is controlled by the hardware. It is enabled during the startup sequence and remains enabled until the device is power cycled. 0x0 = controlled by hardware 0x1 = disabled |
| 13:8 | en_cap_x1 | RW | 0x28 | XO capacitance at X1 terminal. Controls the internal capacitance applied at the X1 terminal (XIN_REFIN device pin)/connected to the integrated crystal. The capacitance rises monotonically in steps of 0.375fF from 0pF to 24pF as the control setting increases from 0x00 to the maximum of 0x3F. This must be set to 0 when sel_ib_xo is set to 0. |
| 7 | xo_en_hyst | RW | 0x1 | Hysteresis enable for monitor path. Writing this bit to a '1' adds hysteresis to reference monitor path. 0x0 = Hysteresis disabled for monitor path 0x1 = Hysteresis enabled for monitor path |
| 6:4 | xo_res | RW | 0x4 | XO Resistor Configuration. Series resistance array control for limiting driving power level. |
| 3 | xo_ib_en_dc_bias | RW | 0x0 | Input Buffer internal DC bias enable. When the input buffer clock input signal is AC-coupled external to the device, the internal DC bias voltage must be enabled. When internal DC bias is disabled (option 0x0), the input signal is DC-coupled. When it is enabled (option 0x1), the input signal is AC-coupled. 0x0 = disabled 0x1 = enabled |
| 2 | sel_ib_xo | RW | 0x1 | XO / Input Buffer select. Selects the mode of the XO / Input Buffer. 0x0 = Input buffer 0x1 = XO |

| XO_CNFG Bit Field Descriptions | | | | |
|--------------------------------|--------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 1 | xo_ib_cmos_sel | RW | 0x0 | Input Buffer CMOS / differential select. Configures the input buffer for single-ended CMOS or differential input signal. 0x0 = differential 0x1 = CMOS |
| 0 | xo_ib_p_n_diff_sel | RW | 0x1 | Input Buffer PMOS / NMOS select. Configures the input buffer according to the common mode voltage of the provided input signal. 0x0: PMOS input pair is enabled (low common mode voltage) 0x1: NMOS input pair is enabled (higher common mode voltage) 0x0 = PMOS 0x1 = NMOS |

3.4 SYSDIV

System clock registers.

Table 6. SYSDIV Register Index

| Offset (Hex) | Register Module Base Address: 0x50 | |
|--------------|------------------------------------|---------------------------------|
| | Register Name | Register Description |
| 0x0 | SYS_DIV_INT | System Clock Divider Setting |
| 0x1 | COUNTER_1US | One Microsecond Counter Setting |

3.4.1 SYS_DIV_INT

System Clock Divider Setting.

| SYS_DIV_INT Bit Field Descriptions | | | | |
|------------------------------------|-------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:5 | reserved | RO | 0x0 | Reserved |
| 4:0 | sys_div_int | RW | 0xC | Quadruple System Clock Divide Ratio. The quadruple system clock divide integer value must be set to produce a frequency between 180MHz and 280MHz, divided down from the APLL VCO frequency divided by 4. This clock is divided by 2 to generate the double system clock, and further divided by 2 to generate the system clock. The frequency picked will have side effects on various calculations done in other blocks (LOSMON, OTP). Normally expected to be between 210MHz and 240MHz, giving a system clock frequency between 52.5MHz and 60MHz. The minimum valid value for this field is 8. Note: The count_1us register field must be programmed according to the system clock frequency. **Note-scan_control3[12:8] must be set to the same value as this register if Logic BIST will be run. |

3.4.2 COUNTER_1US

One Microsecond Counter Setting.

| COUNTER_1US Bit Field Descriptions | | | | |
|------------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:0 | count_1us | RW | 0x3B | One microsecond counter interval. In system clock cycles, minus 1. This configures counters in the OTP. |

3.5 XTALMON

Crystal monitoring registers.

Table 7. XTALMON Register Index

| Offset (Hex) | Register Module Base Address: 0x58 | |
|--------------|------------------------------------|--|
| | Register Name | Register Description |
| 0x0 | ST_CNFG | Crystal Short Term Monitor Configuration |
| 0x4 | PPM_CNFG | Crystal PPM Monitor Configuration |

3.5.1 ST_CNFG

Crystal Short Term Monitor Configuration.

| ST_CNFG Bit Field Descriptions | | | | |
|--------------------------------|---------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:24 | st_max_thresh | RW | 0x0 | Crystal Short Term Monitor Max Threshold. If the absolute value of the difference between one crystal counter and the feedback counter at the end of a monitoring window exceeds this threshold, and the absolute value of the difference between the other crystal counter and the feedback counter is less than st_min_thresh, then either the xtal0_st_err or xtal1_st_err bit is set depending on whether crystal 0 or 1 exceeded st_max_thresh, respectively. The failing crystal's xtal_invalid bit is set to 1 while the frequency remains outside the threshold. Setting this threshold to 0 will disable the short term monitor. |
| 23:16 | st_min_thresh | RW | 0x0 | Crystal Short Term Monitor Min Threshold. Refer to st_max_thresh. |
| 15:12 | reserved | RO | 0x0 | Reserved |
| 11:0 | st_window | RW | 0x0 | Crystal Short Term Monitor Window. Sets the short term monitor window duration, counted in counted in VCO calibration clock (VCO clock divided by 16, approximately 592MHz to 669MHz) cycles. Set to 0 to disable the short term monitor. |

3.5.2 PPM_CNFG

Crystal PPM Monitor Configuration.

| PPM_CNFG Bit Field Descriptions | | | | |
|---------------------------------|-----------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:8 | ppm_err_thresh | RW | 0x0 | Crystal PPM Monitor Error Threshold. If the difference between the crystal counters at the end of the monitoring window exceeds this threshold, then the xtal_ppm_err bit is set. The granularity is 2 ppm/lb. Set to 0 to disable the check. |
| 7:0 | ppm_warn_thresh | RW | 0x0 | Crystal PPM Monitor Warning Threshold. If the difference between the crystal counters at the end of the monitoring window exceeds this threshold, but does not exceed ppm_err_thresh, then the xtal_ppm_warn bit is set. The granularity is 2 ppm/lb. Set to 0 to disable the check. |

3.6 LOSMON

LOS monitor registers.

Table 8. LOSMON Register Index

| Offset (Hex) | Register Module Base Address: 0x60 | |
|--------------|------------------------------------|-----------------------------------|
| | Register Name | Register Description |
| 0x0 | LOSMON_CNFG | LOS Monitor and Crystal Selection |

3.6.1 LOSMON_CNFG

LOS Monitor and Crystal Selection.

| LOSMON_CNFG Bit Field Descriptions | | | | |
|------------------------------------|---------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:12 | reserved | RO | 0x0 | Reserved |
| 11 | xtal_disable | RW | 0x0 | APLL Reference Clock Selection Disable. Controls whether this crystal may be selected as the APLL reference clock. When enabled (option 0x0), the crystal may be selected, subject to qualification by the Loss-of-Signal and Short Term monitors, and prioritization according to xtal_sel_pri. When disabled (option 0x1), the crystal cannot be selected and xtal_invalid is set to 1. 0x0 = enabled 0x1 = disabled |
| 10 | los_fail_mask | RW | 0x0 | LOS Monitor Failure Mask. Masks the LOS monitor status contribution to xtal_invalid. 0x0 = los_sts contributes to xtal_invalid 0x1 = los_sts does not contribute to xtal_invalid |

| LOSMON_CNFG Bit Field Descriptions | | | | |
|------------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 9:7 | reserved | RO | 0x0 | Reserved |
| 6:0 | los_thresh | RW | 0x0 | <p>LOS Threshold. Sets the maximum number of VCO calibration clock (593MHz to 669MHz) cycles from any rising edge of the crystal clock to the next rising edge, and from any falling edge to the next falling edge. If this threshold is reached before the next edge occurs in the same direction, then the monitor's los_sts and losX_evt bits are set; los_sts will remain set until the next crystal rising or falling edge occurs.</p> <p>This ratio can be calculated by the VCO calibration clock frequency (which is the VCO clock frequency/16) divided by the crystal clock frequency.</p> <p>For fractional values, of this ratio, this value should be rounded up to the next whole number for programming los_thresh and for integer (or near integer with fraction>0.9) values of this ratio, 1 should be added to the value for programming los_thresh.</p> <p>Set to 0 to disable the LOS monitor.</p> |

3.7 FREQMON

Bank output frequency monitor registers.

Table 9. FREQMON Register Index

| Offset (Hex) | Register Module Base Address: 0x70 | |
|--------------|------------------------------------|-------------------------------------|
| | Register Name | Register Description |
| 0x0 | FREQMON_THRESH | Output Frequency Monitor Thresholds |

3.7.1 FREQMON_THRESH

Output Frequency Monitor Thresholds.

| FREQMON_THRESH Bit Field Descriptions | | | | |
|---------------------------------------|-----------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 63:49 | reserved | RO | 0x0 | Reserved |
| 48 | freq_window_sel | RW | 0x0 | <p>Frequency Monitor Window Selection. Selects the fast or slow monitoring window. The slow window should be used if the clock frequency is less than 10MHz.</p> <p>For option 0x0 (fast window), see freq_fast_window. For option 0x1 (slow window), see freq_slow_window.</p> <p>0x0 = fast 0x1 = slow</p> |

| FREQMON_THRESH Bit Field Descriptions | | | | |
|---------------------------------------|-----------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 47:24 | freq_max_thresh | RW | 0x0 | Frequency Monitor Max Threshold. If the number of rising edges of the monitored clock at the end of a monitoring window exceeds this threshold, then the monitor's freq_sts and freqX_evt bits are set; freq_sts will remain set until the end of the next window where the counted number of rising edges is less than this threshold and greater than freq_min_thresh. Set to 0 to disable the frequency monitor. |
| 23:0 | freq_min_thresh | RW | 0x0 | Frequency Monitor Min Threshold. If the number of rising edges of the monitored clock at the end of a monitoring window is less than this threshold, then the monitor's freq_sts and freqX_evt bits are set; freq_sts will remain set until the end of the next window where the counted number of rising edges exceeds this threshold and is less than freq_max_thresh. |

3.8 APLL

APLL control registers.

Table 10. APLL Register Index

| Offset (Hex) | Register Module Base Address: 0xB0 | |
|--------------|------------------------------------|--|
| | Register Name | Register Description |
| 0x0 | APLL_FB_DIV_FRAC | APLL Feedback Divider Fraction Setting |
| 0x4 | APLL_FB_DIV_INT | APLL Feedback Divider Integer Setting |
| 0x6 | APLL_FB_SDM_CNFG | APLL Feedback Divider SDM Setting |
| 0x7 | APLL_CNFG | APLL Configuration |
| 0x8 | CP_CNFG | Charge Pump Configuration |
| 0xA | LPF_CNFG | Filter Configuration |
| 0xB | LPF_3RD_CNFG | Filter 3rd Pole Setting |
| 0xC | APLL_XTAL_CNFG | APLL XTAL/Switching Configuration |
| 0x10 | VCO_DAC_CNFG | VCO DAC Configuration |
| 0x16 | APLL_LOCK_CNFG | APLL Lock Configuration |
| 0x18 | APLL_LOCK_THRSH | APLL Lock Thresholds |
| 0x19 | ANA_CLK_EN | Ref/XTAL Clock Enables |
| 0x1C | BANK_MUX_CLK_EN | Output Mux Enables |
| 0x20 | VCO_CAL_CNFG | VCO Calibration Configuration |
| 0x22 | VCO_TRIM_CNFG | VCO Calibration Trim Configuration |

3.8.1 APLL_FB_DIV_FRAC

APLL Feedback Divider Fraction Setting.

| APLL_FB_DIV_FRAC Bit Field Descriptions | | | | |
|---|------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:27 | reserved | RO | 0x0 | Reserved |
| 26:0 | apll_fb_div_frac | RW | 0x0 | APLL Feedback Divider Fraction. APLL feedback divider numerator value. The denominator is a fixed value of 2^{27} . |

3.8.2 APLL_FB_DIV_INT

APLL Feedback Divider Integer Setting.

| APLL_FB_DIV_INT Bit Field Descriptions | | | | |
|--|-----------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:10 | reserved | RO | 0x0 | Reserved |
| 9:0 | apll_fb_div_int | RW | 0x69 | APLL Feedback Divider Integer. APLL feedback divider integer value. |

3.8.3 APLL_FB_SDM_CNFG

APLL Feedback Divider SDM Setting.

| APLL_FB_SDM_CNFG Bit Field Descriptions | | | | |
|---|---------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:6 | reserved | RO | 0x0 | Reserved |
| 5 | apll_fb_dither_en | RW | 0x0 | APLL Feedback SDM Dither Enable. Dither enable for the SDM controlling the APLL feedback divider. 0x0 = dither disabled 0x1 = dither enabled |
| 4 | apll_fb_dither_ns | RW | 0x0 | APLL Feedback SDM Dither Noise shaping. Dither noise shaping enable for the SDM controlling the APLL feedback divider. 0x0 = dither not shaped 0x1 = dither shaped |
| 3:2 | apll_fb_dither_gain | RW | 0x0 | APLL Feedback SDM Dither Gain. Gain control for the SDM controlling the APLL feedback divider. 0x0 = LSB 0x1 = 2*LSB 0x2 = 4*LSB 0x3 = 8*LSB |
| 1:0 | apll_fb_sdm_order | RW | 0x3 | APLL Feedback SDM Order. Selects the order of the SDM controlling the feedback divider for the APLL. 0x0 = Integer 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order |

3.8.4 APLL_CNFG

APLL Configuration.

| APLL_CNFG Bit Field Descriptions | | | | |
|----------------------------------|------------|------------|---------------|-------------|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:0 | reserved | RW | 0x3 | Reserved |

3.8.5 CP_CNFG

Charge Pump Configuration.

| CP_CNFG Bit Field Descriptions | | | | |
|--------------------------------|---------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:14 | reserved | RO | 0x0 | Reserved |
| 13 | cp_offset_en | RW | 0x0 | Charge Pump offset current enable. Writing this bit to a '1' enables the charge pump offset current. 0x0 = disabled 0x1 = enabled |
| 12 | cp_offset_boost | RW | 0x0 | Charge Pump offset current boost. Controls the charge pump offset range. This is the value applied before an XTAL switch or after ramping (if enabled) after an XTAL switch event. If the value programmed is 0, the value will remain at 0 before, during, and after an XTAL switch. 0x0 = 0uA to 145uA 0x1 = 0uA to 236uA |
| 11:8 | cnf_cp_offset | RW | 0x3 | Charge Pump offset current setting. This is the value applied before an XTAL switch or after ramping (if enabled) after an XTAL switch event. If the value programmed is 0x0, the value will remain at 0x0 before, during, and after an XTAL switch. 0x0 = 0uA 0x1 = 5uA 0x2 = 10uA 0x3 = 15uA 0x4 = 20uA 0x5 = 25uA 0x6 = 30uA 0x7 = 35uA 0x8 = 40uA 0x9 = 45uA |
| | cnf_cp_offset (continued) | | | 0xA = 50uA 0xB = 55uA 0xC = 60uA 0xD = 65uA 0xE = 70uA 0xF = 75uA |
| 7 | reserved | RW | 0x0 | Reserved |

| CP_CNFG Bit Field Descriptions | | | | |
|--------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 6:4 | cnf_cp_up | RW | 0x3 | Charge Pump up current setting. These bits control the charge pump up current. 0x0 = 250uA 0x1 = 500uA 0x2 = 750uA 0x3 = 1mA 0x4 = 1.25mA 0x5 = 1.5mA 0x6 = 1.75mA 0x7 = 2mA |
| 3 | reserved | RW | 0x0 | Reserved |
| 2:0 | cnf_cp_dn | RW | 0x3 | Charge Pump down current setting. These bits control the charge pump down current. 0x0 = 250uA 0x1 = 500uA 0x2 = 750uA 0x3 = 1mA 0x4 = 1.25mA 0x5 = 1.5mA 0x6 = 1.75mA 0x7 = 2mA |

3.8.6 LPF_CNFG

Filter Configuration.

| LPF_CNFG Bit Field Descriptions | | | | |
|---------------------------------|---------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | apll_vco_filter_byp | RW | 0x0 | VCO current source filter bypass. Writing this bit to a '1' bypasses the APLL VCO filter. 0x0 = filter active 0x1 = filter bypassed |
| 6:4 | cnf_lpf_cp | RW | 0x7 | Loop filter pole capacitor setting. These bits control the Low Pass Filter pole capacitor. 0x0 = 11pF 0x1 = 14.7pF 0x2 = 18.4pF 0x3 = 22.1pF 0x4 = 25.8pF 0x5 = 29.5pF 0x6 = 33.2pF 0x7 = 36.9pF |

| LPF_CNFG Bit Field Descriptions | | | | |
|---------------------------------|-------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 3:0 | cnf_lpf_res | RW | 0x4 | <p>Loop filter resistor setting. These bits control the Low Pass Filter resistor configuration.</p> <p>0x0 = 0ohm 0x1 = 400ohm 0x2 = 800ohm 0x3 = 1.2kohm 0x4 = 1.6kohm 0x5 = 2kohm 0x6 = 2.4kohm 0x7 = 2.8kohm 0x8 = 3.2kohm 0x9 = 3.6kohm</p> |
| | cnf_lpf_res (continued) | | | <p>0xA = 4kohm 0xB = 4.4kohm 0xC = 4.8kohm 0xD = 5.2kohm 0xE = 5.6kohm 0xF = 6kohm</p> |

3.8.7 LPF_3RD_CNFG

Filter 3rd Pole Setting.

| LPF_3RD_CNFG Bit Field Descriptions | | | | |
|-------------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | byp_p3 | RW | 0x0 | <p>Bypass 3rd pole. This bit may only be set to 1 when operating with an integer feedback divider.</p> <p>0x0 = 3rd pole active 0x1 = 3rd pole bypassed</p> |
| 6:4 | cnf_lpf_r3 | RW | 0x4 | <p>Loop filter 3rd pole resistor setting. These bits control the Low Pass Filter 3rd pole resistor configuration.</p> <p>0x0 = 0ohm 0x1 = 800ohm 0x2 = 1.6kohm 0x3 = 2.4kohm 0x4 = 3.2kohm 0x5 = 4kohm 0x6 = 4.8kohm 0x7 = 5.6kohm</p> |

| LPF_3RD_CNFG Bit Field Descriptions | | | | |
|-------------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 3 | reserved | RO | 0x0 | Reserved |
| 2:0 | cnf_lpf_c3 | RW | 0x4 | <p>Loop filter 3rd pole capacitor setting. These bits control the Low Pass Filter 3rd pole capacitor configuration.</p> <p>0x0 = 0pF 0x1 = 1pF 0x2 = 2pF 0x3 = 3pF 0x4 = 4pF 0x5 = 5pF 0x6 = 6pF 0x7 = 7pF</p> |

3.8.8 APLL_XTAL_CNFG

APLL XTAL/Switching Configuration.

| APLL_XTAL_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|------------------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:30 | reserved | RO | 0x0 | Reserved |
| 29:27 | apll_xtalsw_cp_step_interval | RW | 0x1 | <p>Sets the apll_cnf_cp_offset ramp step interval. This is the interval between each apll_cnf_cp_offset increment and after which apll_cnf_cp_offset_boost is enabled again (if enabled in the cp_offset_boost register field). When cnf_cp_offset=0, the apll_cnf_cp_offset_boost is set back to its register field setting (cp_offset_boost) after 2 apll_xtalsw_cp_step_interval times. Each 1 means a interval of 1us, the interval can be 1us-7us</p> <p>0x1 = 1us 0x2 = 2us 0x3 = 3us 0x4 = 4us 0x5 = 5us 0x6 = 6us 0x7 = 7us</p> |
| 26:24 | apll_xtalsw_cp_step_size | RW | 0x1 | <p>Sets the apll_cnf_cp_offset ramp step size. When apll_xtal_sw_cp_step_en=1, the apll_cnf_cp_offset will be set back to its original value (cnf_cp_offset register field) through series of steps after an XTAL switch. The apll_cnf_cp_offset is incremented with apll_xtalsw_cp_step_size between each step interval. After apll_cnf_cp_offset reaches its original value, apll_cnf_cp_offset_boost is enabled again (if enabled in the cp_offset_boost register field). The step size is between 1-7.</p> |
| 23 | apll_xtalsw_cp_step_en | RW | 0x1 | <p>Enables the ramping of apll_cnf_cp_offset from 0 to its original value after xtal switch. When setting to 0, apll_cnf_cp_offset and apll_cnf_cp_offset_boost will not be changed, when setting to one, apll_cnf_cp_offset and apll_cnf_cp_offset_boost will change to 0, then step back to original value according to setting of apll_xtal_sw_cp_step_size and apll_xtal_sw_cp_step_interval</p> <p>0x0 = ramp disabled 0x1 = ramp enabled</p> |

| APLL_XTAL_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|---------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 22:19 | apll_xtalsw_fb_rst_adj | RW | 0xC | APLL Feedback Divider Adjust Value. This signed offset value gets applied to the first two cycles of the APLL feedback divider after the reset is issued by the XTAL switching circuit, if apll_xtalsw_fb_rst_adj_en is set to 1. Defaults to -4. |
| 18 | apll_xtalsw_fb_rst_adj_en | RW | 0x0 | APLL Feedback Divider Override during XTAL Switch. When set, enables the feedback divider override during the xtal switching procedure. The value is overridden to the current value from the SDM plus the value from the apll_xtalsw_fb_rst_adj field. |
| 17:15 | apll_xtalsw_wait_fb_sel | RW | 0x3 | feedback divider is reset. The feedback divider will be reset until the selected positive edge of the doubler. E.g. setting it to 3 means the feedback divider is reset until the 3rd positive edge of doubler. Minimum is three. Maximum is six. 0x3 = 3rd edge 0x4 = 4th edge 0x5 = 5th edge 0x6 = 6th edge |
| 14:12 | apll_xtalsw_wait_cp_sel | RW | 0x4 | Controls the time that charge pump is disabled. The charge pump will remain disabled until the selected positive edge of the doubler. E.g. setting it to 4 means the charge pump remains disabled until the 4th positive edge of doubler. Minimum is three. Maximum is six. 0x3 = 3rd edge 0x4 = 4th edge 0x5 = 5th edge 0x6 = 6th edge |
| 11 | apll_en_xtalsw_fb_reset | RW | 0x1 | Enable pin for feedback reset block. If enabled (1), when the xtal breaks, it will reset APLL feedback divider. 0x0 = disabled 0x1 = enabled |
| 10 | apll_en_xtalsw_cp | RW | 0x1 | Active High enable pin for charge pump enable block. If enabled (1), when the xtal breaks and it switches to the other crystal (apll_xtal_sw=1), it will disable the charge pump to minimize excursion. 0x0 = disabled 0x1 = enabled |
| 9 | apll_en_dn_pw_limiter | RW | 0x1 | Enable pin for down pulse width limiter block. If enabled (1), it will limit the pulse width of down signal to a value set by cnf_pw_dn<3:0>. When the chip starts up, en_dn_pw_limiter needs to be zero (0). Once it locks, it can be enabled (1). 0x0 = disabled 0x1 = enabled |
| 8 | apll_en_up_pw_limiter | RW | 0x1 | Enable pin for up pulse width limiter block. If enabled (1), it will limit the pulse width of up signal to a value set by cnf_pw_up<3:0>. When the chip starts up, en_up_pw_limiter needs to be zero (0). Once it locks, it can be enabled (1). 0x0 = disabled 0x1 = enabled |

| APLL_XTAL_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|---------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:4 | apl_cnf_pw_dn | RW | 0x8 | 4 bit tuning capacitor to control the down pulse width. Controls the maximum pulse width of PFD pulse width limiter for down signal. Default value is 5, which limits the pulse width of down signal to 1ns. |
| 3:0 | apl_cnf_pw_up | RW | 0x8 | 4 bit tuning capacitor to control the up pulse width. Controls the maximum pulse width of PFD pulse width limiter for up signal. Default value is 5, which limits the pulse width of up signal to 1ns. |

3.8.9 VCO_DAC_CNFG

VCO DAC Configuration.

| VCO_DAC_CNFG Bit Field Descriptions | | | | |
|-------------------------------------|-------------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:4 | reserved | RO | 0x0 | Reserved |
| 3:0 | cnf_vco_dac | RW | 0x5 | VCO control voltage DAC setting. Controls the VCO DAC voltage as shown in the decode. 0x0 = 0V 0x1 = 75mV 0x2 = 150mV 0x3 = 225mV 0x4 = 300mV 0x5 = 375mV 0x6 = 450mV 0x7 = 525mV 0x8 = 600mV 0x9 = 675mV |
| | cnf_vco_dac (continued) | | | 0xA = 750mV 0xB = 825mV 0xC = 900mV 0xD = 975mV 0xE = 1.050V 0xF = 1.125V |

3.8.10 APLL_LOCK_CNFG

APLL Lock Configuration.

| APLL_LOCK_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|---------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:14 | reserved | RO | 0x0 | Reserved |
| 13 | apl_lock_xtalsw_byp | RW | 0x0 | Bypass the APLL lock gating after XTAL switch bypass. Directly pass chosen APLL lock through after XTAL switch and do not wait for number of cycles selected in apl_lock_gate_xtalw. 0x0 = lock gate in use 0x1 = lock gate is bypassed |

| APLL_LOCK_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 12:11 | apll_lock_gate_xtalsw | RW | 0x2 | APLL Lock gating after XTAL Switch. Gate any potential change in APLL lock for this many APLL reference clock cycles after an XTAL switch 0x0 = 1024 cycles 0x1 = 2048 cycles 0x2 = 4096 cycles 0x3 = 8192 cycles |
| 10 | use_raw_lock | RW | 0x0 | APLL Lock Status Select to Pin. When set, the raw lock is sent to a GPIO status pin configured to select the APLL lock status. |
| 9 | apll_precision_lock_en | RW | 0x1 | APLL Precision Lock Detector Enable. When set, enables the lock detector using the ranges controlled by apll_th_refl and apll_th_refh. |
| 8 | apll_lock_timer_byp | RW | 0x0 | APLL Lock Timer Bypass. When cleared, the APLL lock timer debounce is used. When set, the APLL lock timer is bypassed. Bypassing the APLL Lock timer results in 0us of debounce. Not recommended to be set to '1' if apll_lock_xtalsw_byp is not also = '1'. 0x0 = debounce enabled 0x1 = bypassed |
| 7:6 | apll_lock_timer | RW | 0x2 | APLL Lock Timer. Controls the digital debounce interval for the lock indication for the APLL. This duration is a function of the system clock cycles. 0x0 = 5 cycles 0x1 = 285 cycles 0x2 = 2850 cycles 0x3 = 28500 cycles |
| 5 | sel_1time_lock | RW | 0x0 | One time lock select. Controls whether lock detection will occur once or continuously. When set to 0x1, once the lock signal asserts it will remain asserted even if the APLL loses lock. 0x0 = real-time lock 0x1 = One time lock |
| 4 | lck_detect_cal_byp | RW | 0x0 | Lock detect during calibration enable. Selects when the lock detector is enabled. When cleared, the Lock detector is enabled after VCO calibration completes. When set, the lock detector is enabled during and after VCO calibration. 0x0 = after VCO calibration 0x1 = during and after VCO calibration |
| 3 | lck_byp | RW | 0x0 | Lock detector disable. When enabled (option 0x0), the lock detector is enabled according to lck_detect_cal_byp and sel_1time_lock. When disabled (option 0x1), the Lock detector is disabled and the lock signal is asserted. Writing this bit to a '1' bypasses the APLL lock detector circuit. 0x0 = enabled 0x1 = disabled |
| 2:0 | lck_detect_ref_sel | RW | 0x0 | Lock detector reference select. Controls phase difference between up/down for PLL lock signal. |

3.8.11 APLL_LOCK_THRSH

APLL Lock Thresholds.

| APLL_LOCK_THRSH Bit Field Descriptions | | | | |
|--|--------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:4 | apll_th_refh | RW | 0x6 | APLL Precision Lock High Threshold. Controls the high threshold voltage of the precision lock detector. The threshold is approximately $750\text{mV} + 20\text{mV} * \text{apll_th_refh}$. The default is around 870mV. |
| 3:0 | apll_th_refl | RW | 0xA | APLL Precision Lock Low Threshold. Controls the low threshold voltage of the precision lock detector. The threshold is approximately $50\text{mV} + 18\text{mV} * \text{apll_th_refl}$. The default is around 230mV. |

3.8.12 ANA_CLK_EN

Ref/XTAL Clock Enables.

| ANA_CLK_EN Bit Field Descriptions | | | | |
|-----------------------------------|-------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | reserved | RO | 0x0 | Reserved |
| 6 | en_apll_ref_omux | RW | 0x0 | APLL Reference Clock to Output Mux Enable. Enables fanout of the selected crystal clock to the output clock mux. 0x0 = disabled 0x1 = enabled |
| 5 | en_xtal1_hdiv_dig | RW | 0x1 | Crystal 1 Divided Clock to Digital Enable. Enables fanout of the crystal 1 Hdiv output clock to the digital logic. 0x0 = disabled 0x1 = enabled |
| 4 | en_xtal0_hdiv_dig | RW | 0x1 | Crystal 0 Divided Clock to Digital Enable. Enables fanout of the crystal 0 Hdiv output clock to the digital logic. 0x0 = disabled 0x1 = enabled |
| 3 | en_xtal1_dig | RW | 0x1 | Crystal 1 Clock to Digital Enable. Enables fanout of the crystal 1 clock to the digital logic. 0x0 = disabled 0x1 = enabled |
| 2 | en_xtal0_dig | RW | 0x1 | Crystal 0 Clock to Digital Enable. Enables fanout of the crystal 0 clock to the digital logic. 0x0 = disabled 0x1 = enabled |
| 1 | en_xtal1_apll | RW | 0x1 | Crystal 1 Clock to APLL Enable. Enables fanout of the crystal 1 clock to the APLL. 0x0 = disabled 0x1 = enabled |
| 0 | en_xtal0_apll | RW | 0x1 | Crystal 0 Clock to APLL Enable. Enables fanout of the crystal 0 clock to the APLL. 0x0 = disabled 0x1 = enabled |

3.8.13 BANK_MUX_CLK_EN

Output Mux Enables.

| BANK_MUX_CLK_EN Bit Field Descriptions | | | | |
|--|--------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:25 | reserved | RO | 0x0 | Reserved |
| 24 | en_clk_hpfod2_bnk6 | RW | 0x1 | HPFOD 2 to Bank 6 Output Mux Enable. Enables fanout of HPFOD 2 output clock to Bank 6 output mux. 0x0 = disabled 0x1 = enabled |
| 23 | en_clk_hpfod2_bnk5 | RW | 0x1 | HPFOD 2 to Bank 5 Output Mux Enable. Enables fanout of HPFOD 2 output clock to Bank 5 output mux. 0x0 = disabled 0x1 = enabled |
| 22 | en_clk_hpfod2_bnk4 | RW | 0x1 | HPFOD 2 to Bank 4 Output Mux Enable. Enables fanout of HPFOD 2 output clock to Bank 4 output mux. 0x0 = disabled 0x1 = enabled |
| 21 | en_clk_hpfod2_bnk3 | RW | 0x1 | HPFOD 2 to Bank 3 Output Mux Enable. Enables fanout of HPFOD 2 output clock to Bank 3 output mux. 0x0 = disabled 0x1 = enabled |
| 20 | en_clk_hpfod1_bnk6 | RW | 0x1 | HPFOD 1 to Bank 6 Output Mux Enable. Enables fanout of HPFOD 1 output clock to Bank 6 output mux. 0x0 = disabled 0x1 = enabled |
| 19 | en_clk_hpfod1_bnk5 | RW | 0x1 | HPFOD 1 to Bank 5 Output Mux Enable. Enables fanout of HPFOD 1 output clock to Bank 5 output mux. 0x0 = disabled 0x1 = enabled |
| 18 | en_clk_hpfod1_bnk4 | RW | 0x1 | HPFOD 1 to Bank 4 Output Mux Enable. Enables fanout of HPFOD 1 output clock to Bank 4 output mux. 0x0 = disabled 0x1 = enabled |
| 17 | en_clk_hpfod1_bnk3 | RW | 0x1 | HPFOD 1 to Bank 3 Output Mux Enable. Enables fanout of HPFOD 1 output clock to Bank 3 output mux. 0x0 = disabled 0x1 = enabled |
| 16 | en_clk_hpfod1_bnk2 | RW | 0x1 | HPFOD 1 to Bank 2 Output Mux Enable. Enables fanout of HPFOD 1 output clock to Bank 2 output mux. 0x0 = disabled 0x1 = enabled |
| 15 | en_clk_hpfod1_bnk1 | RW | 0x1 | HPFOD 1 to Bank 1 Output Mux Enable. Enables fanout of HPFOD 1 output clock to Bank 1 output mux. 0x0 = disabled 0x1 = enabled |

| BANK_MUX_CLK_EN Bit Field Descriptions | | | | |
|--|--------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 14 | en_clk_hpfod1_bnk0 | RW | 0x1 | HPFOD 1 to Bank 0 Output Mux Enable. Enables fanout of HPFOD 1 output clock to Bank 0 output mux. 0x0 = disabled 0x1 = enabled |
| 13 | en_clk_hpfod0_bnk3 | RW | 0x1 | HPFOD 0 to Bank 3 Output Mux Enable. Enables fanout of HPFOD 0 output clock to Bank 3 output mux. 0x0 = disabled 0x1 = enabled |
| 12 | en_clk_hpfod0_bnk2 | RW | 0x1 | HPFOD 0 to Bank 2 Output Mux Enable. Enables fanout of HPFOD 0 output clock to Bank 2 output mux. 0x0 = disabled 0x1 = enabled |
| 11 | en_clk_hpfod0_bnk1 | RW | 0x1 | HPFOD 0 to Bank 1 Output Mux Enable. Enables fanout of HPFOD 0 output clock to Bank 1 output mux. 0x0 = disabled 0x1 = enabled |
| 10 | en_clk_hpfod0_bnk0 | RW | 0x1 | HPFOD 0 to Bank 0 Output Mux Enable. Enables fanout of HPFOD 0 output clock to Bank 0 output mux. 0x0 = disabled 0x1 = enabled |
| 9 | en_clk_iod1_bnk6 | RW | 0x1 | IOD 1 to Bank 6 Output Mux Enable. Enables fanout of IOD 1 output clock to Bank 6 output mux. 0x0 = disabled 0x1 = enabled |
| 8 | en_clk_iod1_bnk5 | RW | 0x1 | IOD 1 to Bank 5 Output Mux Enable. Enables fanout of IOD 1 output clock to Bank 5 output mux. 0x0 = disabled 0x1 = enabled |
| 7 | en_clk_iod1_bnk4 | RW | 0x1 | IOD 1 to Bank 4 Output Mux Enable. Enables fanout of IOD 1 output clock to Bank 4 output mux. 0x0 = disabled 0x1 = enabled |
| 6 | en_clk_iod0_bnk6 | RW | 0x1 | IOD 0 to Bank 6 Output Mux Enable. Enables fanout of IOD 0 output clock to Bank 6 output mux. 0x0 = disabled 0x1 = enabled |
| 5 | en_clk_iod0_bnk5 | RW | 0x1 | IOD 0 to Bank 5 Output Mux Enable. Enables fanout of IOD 0 output clock to Bank 5 output mux. 0x0 = disabled 0x1 = enabled |
| 4 | en_clk_lpfod1_bnk2 | RW | 0x1 | LPFOD 1 to Bank 2 Output Mux Enable. Enables fanout of LPFOD 1 output clock to Bank 2 output mux. 0x0 = disabled 0x1 = enabled |

| BANK_MUX_CLK_EN Bit Field Descriptions | | | | |
|--|--------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 3 | en_clk_lpfod1_bnk1 | RW | 0x1 | LPFOD 1 to Bank 1 Output Mux Enable. Enables fanout of LPFOD 1 output clock to Bank 1 output mux. 0x0 = disabled 0x1 = enabled |
| 2 | en_clk_lpfod1_bnk0 | RW | 0x1 | LPFOD 1 to Bank 0 Output Mux Enable. Enables fanout of LPFOD 1 output clock to Bank 0 output mux. 0x0 = disabled 0x1 = enabled |
| 1 | en_clk_lpfod0_bnk1 | RW | 0x1 | LPFOD 0 to Bank 1 Output Mux Enable. Enables fanout of LPFOD 0 output clock to Bank 1 output mux. 0x0 = disabled 0x1 = enabled |
| 0 | en_clk_lpfod0_bnk0 | RW | 0x1 | LPFOD 0 to Bank 0 Output Mux Enable. Enables fanout of LPFOD 0 output clock to Bank 0 output mux. 0x0 = disabled 0x1 = enabled |

3.8.14 VCO_CAL_CNFG

VCO Calibration Configuration.

| VCO_CAL_CNFG Bit Field Descriptions | | | | |
|-------------------------------------|------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15 | vco_cal_div_en | RW | 0x1 | VCO Calibration Manual Divider Enable. When set, forces the VCO calibration divider to be enabled. This must be enabled to support the LOS monitor and XTAL switching logic. 0x0 = disabled 0x1 = enabled |
| 14:13 | vco_settle_count | RW | 0x3 | VCO Calibration settle count value. Selects the number of reference clock cycles for allowing the VCO to settle before doing the frequency measurement, as described in VCO Calibration). This field cannot be set to the same count value as the vco_cal_count field. 0x0 = 64 cycles 0x1 = 128 cycles 0x2 = 256 cycles 0x3 = 512 cycles |
| 12 | vco_trim_cal_en | RW | 0x1 | VCO Trim Calibration enable. Enables calibration of the trim bits in addition to the normal frequency band selection. When the bit is set, the trim bits are controlled by the calibration logic and not the vco_trim field. 0x0 = disable trim calibration 0x1 = enable trim calibration |
| 11 | vco_cal_div | RW | 0x1 | VCO Calibration divider value. Selects the clock divider value used for calibration (the VCOFixedDiv value described in VCO Calibration). 0x0 = divide by 32 0x1 = divide by 16 |

| VCO_CAL_CNFG Bit Field Descriptions | | | | |
|-------------------------------------|---------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 10:8 | vco_cal_count | RW | 0x2 | VCO Calibration timer value. Indicates the duration of each band calibration measurement (the REFCOUNT value described in VCO Calibration). For reference frequencies less than 30MHz, this field should be set to 0x5 (512 cycles). For frequencies less than 50MHz, it should be set to 0x0 (1024 cycles). For frequencies less than 120MHz, it should be set to 0x1 (2048 cycles). For frequencies less than 240MHz, it should be set to 0x2 (4096). For higher frequencies, it should be set to 0x3 (8192). This field cannot be set to the same count value as the vco_settle_count field. 0x0 = 1024 cycles 0x1 = 2048 cycles 0x2 = 4096 cycles 0x3 = 8192 cycles 0x4 = 256 cycles 0x5 = 512 cycles |
| 7 | reserved | RO | 0x0 | Reserved |
| 6 | vco_cal_byp | RW | 0x0 | VCO Calibration bypass. Disables automatic VCO calibration during startup. When VCO calibration is enabled, the band selected by the VCO calibration logic (vco_cap) is applied to the VCO. When VCO calibration is disabled, the band programmed in vco_sw_cap is applied to the VCO. 0x0 = enabled 0x1 = disabled |
| 5:0 | vco_sw_cap | RW | 0x20 | VCO Calibration bypass frequency band select. Provides the band to apply to the VCO when calibration is bypassed by setting vco_cal_byp to 1. |

3.8.15 VCO_TRIM_CNFG

VCO Calibration Trim Configuration.

| VCO_TRIM_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|-----------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | reserved | RO | 0x0 | Reserved |
| 6:4 | vco_cal_startup_count | RW | 0x2 | VCO Startup Count. Controls the delay period between asserting the signal indicating start of calibration and the actual start of the calibration search. This delay is to allow the charging of the control voltage capacitor. This period is in reference clock cycles (without doubler). 0x0 = 1200 cycles 0x1 = 2500 cycles 0x2 = 4000 cycles 0x3 = 6400 cycles 0x4 = 15625 cycles 0x5 = 28195 cycles 0x6 = 34375 cycles |
| 3 | reserved | RO | 0x0 | Reserved |

| VCO_TRIM_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|----------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 2 | vco_trim_wr_en | RW | 0x1 | VCO Trim Write Enable. Enables writing to the vco_trim field. This bit is programmed to 0 at the factory in the OTP common configuration. If the user must write to this register during the configuration load or during a serial port burst write, the value written should be 0x0. 0x0 = VCO_trim is read-only 0x1 = VCO_trim is write-able |
| 1:0 | vco_trim | RW | 0x1 | Coarse VCO Tuning. Shifts the VCO range to set the center frequency closest to 10.5 GHz. It may only be written when vco_trim_wr_en is set to 1. This value is programmed at the factory in the OTP common configuration. When vco_trim_cal_en is set to 1, the VCO calibration logic controls the trim value and this field is unused. |

3.9 SSC

Spread spectrum registers.

Table 11. SSC Register Index

| Offset (Hex) | Register Module Base Address: 0xF0 | |
|--------------|------------------------------------|-------------------------------|
| | Register Name | Register Description |
| 0x0 | SSC_CNFG | Spread Spectrum Configuration |

3.9.1 SSC_CNFG

Spread Spectrum Configuration.

| SSC_CNFG Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31 | ssc_en | RW | 0x0 | Spectrum Spreading Enable. Enable spread spectrum. The spread configuration is determined by the other register fields in this register. If the FOD0 and FOD1 SSC modulation frequencies are the same, the FOD1 SSC phase may be aligned to FOD0 SSC by setting ssc_sync to 1. Note: When ssc_sync is set to 1, then FOD1 ssc_en must be set to 1 before FOD0 ssc_en is set to 1 since FOD1 SSC will start when FOD0 ssc_en is set to 1. This restriction does not apply when loading the device configuration from OTP on startup, but does apply if dynamically changing these settings later by writing registers from the serial interface. 0x0 = SSC disabled 0x1 = SSC enabled |
| 30 | ssc_mode | RW | 0x0 | Spectrum Spreading Mode. Selects the spread direction. 0x0 = down spreading 0x1 = center spreading |
| 29:24 | reserved | RO | 0x0 | Reserved |

| SSC_CNFG Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 23:16 | ssc_ampl | RW | 0x51 | <p>Spectrum Spreading Amplitude. Sets the positive and negative spreading amplitude. For down spread, ssc_ampl is only used for the negative limit and the positive limit is internally set to 0. For center spread, the peak-to-peak spread amplitude is twice the specified amplitude (for a 1% peak-to-peak center spread, define ssc_ampl as 0.5%).</p> $\text{ssc_ampl} = \text{spread_percentage} / 100 * 2^{14}$ <p>for example, for 1% spread, set ssc_ampl to $0.01 * 2^{14} = 163$ decimal, or 0xA3</p> <p>The default value corresponds to a 0.5% down spread at 31.5kHz.</p> |
| 15:0 | ssc_step | RW | 0x2B8 C | <p>Spectrum Spreading Step Size. Set ramp step size to get the target modulation rate. For down spread:</p> $\text{ssc_step} = \text{ssc_ampl} * 2^{16} * \text{ssc_freq} / 15\text{MHz}$ <p>For center spread:</p> $\text{ssc_step} = 2 * \text{ssc_ampl} * 2^{16} * \text{ssc_freq} / 15\text{MHz}$ <p>where,</p> <p>ssc_freq is the target modulation rate from 30kHz to 63kHz 15MHz is the system clock divided by 8, assuming the system clock is 60MHz</p> <p>Example 1. For a 32kHz 1% down spread: $\text{ssc_ampl} = 163$ $\text{ssc_step} = 163 * 2^{16} * 32\text{kHz} / 15\text{MHz} = 0x5905$</p> <p>Example 2. For a 32kHz +/- 0.5% center spread: $\text{ssc_ampl} = 81$ $\text{ssc_step} = 2 * 81 * 2^{16} * 32\text{kHz} / 15\text{MHz} = 0x5879$</p> <p>The default value corresponds to a 0.5% down spread at 31.5kHz.</p> |

3.10 IOD

Integer Output Divider registers.

Table 12. IOD Register Index

| Offset (Hex) | Register Module Base Address: 0x100 | |
|--------------|-------------------------------------|---------------------------|
| | Register Name | Register Description |
| 0x0 | IOD_INT_CNFG | IOD Divider/Configuration |
| 0x4 | IOD_PHASE_CNFG | IOD Phase Configuration |

3.10.1 IOD_INT_CNFG

IOD Divider/Configuration.

| IOD_INT_CNFG Bit Field Descriptions | | | | |
|-------------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31 | iod_pd | RW | 0x0 | Integer Output Divider Power Down. Powers down the integer output divider by turning off the regulator. If this bit is set to 1, iod_rst must also be set to 1. When clearing this bit, iod_rst must remain set and then it may be cleared afterwards. 0x0 = divider is powered up 0x1 = divider is powered down |
| 30 | iod_dis | RW | 0x0 | Integer Output Divider Disable. Disables the integer output divider. If this bit is set to 1, iod_rst must also be set to 1. When clearing this bit, iod_rst must remain set and then it may be cleared afterwards. 0x0 = divider enabled 0x1 = divider disabled |
| 29 | iod_rst | RW | 0x0 | Integer Output Divider Reset. Resets the integer output divider. 0x0 = divider reset deasserted 0x1 = divider reset asserted |
| 28:25 | reserved | RO | 0x0 | Reserved |
| 24:0 | iod_int | RW | 0x64 | Integer Output Divider Ratio. Integer output divider ratio. The minimum value is 14. This register is atomic. When the most significant byte (bit [24]) is written, the new value is applied to the IOD. If the old or new iod_int value is less than 32 and the part is being programmed via serial bus (not OTP), please set iod_rst to '1', write the new iod_int value, and then set iod_rst to '0'. |

3.10.2 IOD_PHASE_CNFG

IOD Phase Configuration.

| IOD_PHASE_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|----------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15 | iod_ph_adj_now | RW1S | 0x0 | Integer Output Divider Phase Adjustment Now. When this bit is written from 0 to 1, the phase adjustment in iod_phase is applied to the divider. This bit self-clears when the adjust completes. This bit should not be set to 1 if iod_pd = 1 or iod_rst = 1. |
| 14 | iod_ph_adj_post_sync | RW | 0x0 | Integer Output Divider Phase Adjustment After Synchronization. When this bit is set to 1, the phase adjustment in iod_phase is applied to the divider whenever the divider is synchronized. This bit should not be set to 1 if iod_pd = 1 or iod_rst = 1. |
| 13:9 | reserved | RO | 0x0 | Reserved |
| 8:0 | iod_phase | RW | 0x0 | Integer Output Divider Phase Configuration. Signed 2's complementary value sets the phase, a positive value means lag from 0 phase, a negative value means lead from 0 phase, in steps of one VCO period. When negative, (iod_int/2 - iod_phase) must be >= 6. The available range is +/- 0~255 steps (approximately +/- 0~20ns). This register is atomic. When the most significant byte (bit [8]) is written, the new value is applied to the IOD according to iod_ph_adj_now and iod_ph_adj_post_sync. |

3.11 HPFOD

High Performance Fractional Output Divider registers.

Table 13. HPFOD Register Index

| Offset (Hex) | Register Module Base Address: 0x110 | |
|--------------|-------------------------------------|-----------------------------|
| | Register Name | Register Description |
| 0x0 | HPFOD_INT_CNFG | HPFOD Divider/Configuration |
| 0x8 | HPFOD_PHASE_CNFG | HPFOD Phase Configuration |

3.11.1 HPFOD_INT_CNFG

HPFOD Divider/Configuration.

| HPFOD_INT_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|-----------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 63 | hpfod_pd | RW | 0x0 | High Performance Fractional Output Divider Power Down. Powers down the HP fractional output divider by turning off the regulator. If this bit is set to 1, hpfod_rst must also be set to 1. When clearing this bit, hpfod_rst must remain set and then it may be cleared afterwards. 0x0 = divider is powered up 0x1 = divider is powered down |
| 62 | hpfod_dis | RW | 0x0 | High Performance Fractional Output Divider Disable. Disables the HP fractional output divider. If this bit is set to 1, hpfod_rst must also be set to 1. When clearing this bit, hpfod_rst must remain set and then it may be cleared afterwards. 0x0 = divider enabled 0x1 = divider disabled |
| 61 | hpfod_rst | RW | 0x0 | High Performance Fractional Output Divider Reset. Resets the HP fractional output divider. 0x0 = divider reset deasserted 0x1 = divider reset asserted |
| 60 | hpfod_acc_reset | RW | 0x0 | HPFOD SDM accumulator reset. Writing this bit to a '1' resets the HPFOD SDM accumulator. 0x0 = accumulator reset deasserted 0x1 = accumulator reset asserted |
| 59:26 | hpfod_frac | RW | 0x0 | High Performance Fractional Output Divider Ratio Fraction portion. Denominator is fixed to 2^{34} . This register field is part of an atomic group consisting of hpfod_1st_int and hpfod_frac. When the most significant byte (bits [33:30]) of hpfod_frac is written, the value of all these fields are applied to the HPFOD. Note: When an HPFOD has spread-spectrum, hpfod_frac[5:0] must be set to 0x0. |
| 25:9 | hpfod_2nd_int | RW | 0x0 | High Performance Fractional Output Divider Ratio High Performance 2nd Integer portion. Half integer divide ratio of second stage. The actual divide ratio is (hpfod_2nd_int * 2). A setting of 1 is invalid: the minimum divide ratio is 4. Set to 0 to bypass the second stage. |

| HPFOD_INT_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|---------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 8:0 | hpfod_1st_int | RW | 0x64 | High Performance Fractional Output Divider Ratio 1st Integer portion. Integer divide ratio of first stage (MMD). This register field is part of an atomic group consisting of hpfod_1st_int and hpfod_frac. When the most significant byte (bits [8:7]) of hpfod_1st_int or the most significant byte (bits [33:30]) of hpfod_frac is written, the value of all these fields are applied to the HP FOD. The allowed frequency range for after this first divider stage (hpfod_1st_int plus hpfod_frac) is 33MHz-650MHz. Only set divider values within this range. Note: Refer to hpfod_frac for details regarding serial bus writes to this register field. |

3.11.2 HPFOD_PHASE_CNFG

HPFOD Phase Configuration.

| HPFOD_PHASE_CNFG Bit Field Descriptions | | | | |
|---|------------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15 | hpfod_ph_adj_now | RW1S | 0x0 | High Performance Fractional Output Divider Phase High Performance Adjustment Now. When this bit is written from 0 to 1, the phase adjustment in hpfod_phase is applied to the divider. This bit self-clears when the adjust completes. |
| 14 | hpfod_ph_adj_post_sync | RW | 0x1 | High Performance Fractional Output Divider Phase Adjustment After Synchronization. When this bit is set to 1, the phase adjustment in hpfod_phase is applied to the divider whenever the divider is synchronized. |
| 13 | hpfod_slow_freq_en | RW | 0x0 | High Performance FOD Slow Frequency enable. Must be set to 1 when the MMD (first stage) frequency is under 70 MHz. |
| 12:10 | reserved | RO | 0x0 | Reserved |
| 9:0 | hpfod_phase | RW | 0x3F0 | High Performance Fractional Output Divider Phase Configuration. signed 2's complementary value sets the phase, a positive value means lag from 0 phase, a negative value means lead from 0 phase, in steps of 1/4 VCO period. The default value of -16 (decimal), or -4.0 VCO periods, approximately aligns the HP FOD output clock with the IOD output clock, when the HP FOD is configured with an integer divide ratio. This correction factor needs to be adjusted for fractional divide ratios. This register is atomic. When the most significant byte (bits [9:8]) is written, the new value is applied to the FOD according to hpfod_ph_adj_now and hpfod_ph_adj_post_sync. |

3.12 DCD

DCD control registers for HPFOD's.

Table 14. DCD Register Index

| Offset (Hex) | Register Module Base Address: 0x140 | |
|--------------|-------------------------------------|--------------------------------------|
| | Register Name | Register Description |
| 0x0 | DCD_CNFG | DCD Configuration |
| 0x4 | DCD_MAN_CNFG | DCD Manual Control |
| 0x6 | DCD_ACCEL_CNFG | DCD Accelerated Calibration Settings |
| 0x8 | DCD_CTRL | DCD Status Selection |

3.12.1 DCD_CNFG

DCD Configuration.

| DCD_CNFG Bit Field Descriptions | | | | |
|---------------------------------|-----------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:27 | dcd_slow_gain_shift | RW | 0x10 | DCD Calibration Slow Filter Gain Shift. Controls the gain shift in the DCD calibration slow filter mode. The suggested range is 15 to 17. |
| 26 | reserved | RO | 0x0 | Reserved |
| 25 | fod_spare | RW | 0x0 | FOD/DCD Spare Configuration Bits. Unused. |
| 24 | dcd_slow_en | RW | 0x0 | DCD Calibration Slow Filter Mode enable. Enables the DCD calibration slow filter mode, after dcd_slow_start_delay following the end of accelerated calibration. The gain shift is set by dcd_slow_gain_shift. The update rate (common to all FODs) is set by dcd_slow_update_rate. This bit must be set to 0 if either dcd_integer_mode or dcd_holdover_mode are set to 1. |
| 23:22 | dcd_fast_lock_lpf_sel | RW | 0x0 | DCD Fast Lock Low Pass Filter Coefficient selection. Selects the DCD calibration LPF coefficient used when dcd_fast_lock is set to 1. 0x0 = coefficient is 0x0B 0x1 = coefficient is 0x0C 0x2 = coefficient is 0x0D 0x3 = coefficient is 0x0E |
| 21 | dcd_fast_lock | RW | 0x0 | DCD Fast Lock Mode. Enables faster calibration, but with higher phase noise. This bit may be set to 1 to enable a quick initial calibration, and then should be set to 0 for normal operation. dcd_fast_lock_lpf_sel selects the LPF coefficient used during fast lock, instead of the normal dcd_calib_lpf. Fast lock is automatically enabled during accelerated calibration for the time interval specified by dcd_accel_fast_lock; this bit should be set to 0 unless performing a manual fast lock. This will be automatically controlled on startup to calibrate the DCD before the output clocks are enabled. |
| 20:16 | dcd_calib_deci | RW | 0xA | DCD Calibration Decimator Filter coefficient. The DCD calibration decimator coefficient used. Maximum value is 0xA = 'd10. |
| 15 | robust_gro_state_en | RW | 0x1 | Robust GRO State Decode enable. Set to 1 to enable detection of transient GRO states. 0x0 = Robust GRO state off 0x1 = Robust GRO state on |
| 14:13 | phase_wrap_ctrl | RW | 0x0 | GRO Phase Wrapping Algorithm. Selects the GRO phase wrapping algorithm. This is for debugging purposes only and should generally not be modified. When set to 0, assumes that the GRO phase has wrapped around if the absolute value of the delta of the two GRO cycles is less if 34 is added to the delta or subtracted from the delta. 0x0 = Assumes wrap when delta is less when adding or subtracting 34 0x1 = Assumes wrap when delta is greater than 17 0x2 = Assumes wrap when delta is greater than 12 |
| 12:8 | dcd_calib_lpf | RW | 0x18 | DCD Calibration Low Pass Filter coefficient. The DCD calibration LPF coefficient used when dcd_fast_lock is set to 0. Maximum value is 0x18 = 'd24. |

| DCD_CNFG Bit Field Descriptions | | | | |
|---------------------------------|-------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:6 | dac_clk_ctrl | RW | 0x1 | DCD DAC SDM Clock Select. Selects the divisor when generating the DAC SDM clock. 0x0 = divide by 4 0x1 = divide by 8 0x2 = divide by 16 0x3 = divide by 16 |
| 5 | dcd_holdover_mode | RW | 0x0 | DCD Calibration Holdover Mode. Enables DCD FOD calibration holdover. 0x0 = normal operation 0x1 = DCD calibration in holdover mode |
| 4 | dcd_integer_mode | RW | 0x0 | DCD FOD Integer Mode. When '1' force DAC output from calibration block to all '0's. If this bit is set before or during accelerated calibration, integer mode is enabled internally after accelerated calibration ends. If this bit is set to 1, then dcd_slow_en must be set to 0. It will be forced to 0 internally while SSC is active (FOD 0 and 1 only). 0x0 = normal 0x1 = use FOD in integer mode |
| 3:2 | dcd_dac_sdm_order | RW | 0x2 | DCD DAC SDM Order. Selects DAC SDM order. 0x0 = sdm off 0x1 = 1st order 0x2 = 2nd order 0x3 = Round to closest value, sdm off |
| 1 | dcd_bw_sel | RW | 0x0 | DCD analog filter for DAC selection. Selects between 50kHz analog filter bandwidth and 200kHz analog filter bandwidth. When 0x0, selects 50KHz bandwidth for lower FOD frequencies. When 0x1, selects 200KHz bandwidth for higher FOD frequencies. 0x0 = 50KHz bw 0x1 = 200KHz bw |
| 0 | clr_gro_st_cnt | RW | 0x0 | DCD Calibration GRO Clear. Write '1' to clear the invalid GRO state counter. This bit must be written to 0 before it may be triggered again by writing it to 1. |

3.12.2 DCD_MAN_CNFG

DCD Manual Control.

| DCD_MAN_CNFG Bit Field Descriptions | | | | |
|-------------------------------------|-----------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15 | dcd_calib_man | RW | 0x0 | DCD Manual Mode. Selects the DCD calibration mode. When set to manual (option 0x1), manual DCD gain will be used (dcd_manual_gain) 0x0 = auto 0x1 = manual |
| 14:0 | dcd_manual_gain | RW | 0x6F00 | DCD Manual Gain. In manual mode (when dcd_calib_man is set to 1), this field sets the DCD gain. This is a 15-bit signed 2's complement number. Note: The value obtained from reading i_err_sts may be written directly to dcd_manual_gain without any shifting. |

3.12.3 DCD_ACCEL_CNFG

DCD Accelerated Calibration Settings.

| DCD_ACCEL_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|---------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:9 | reserved | RO | 0x0 | Reserved |
| 8 | dcd_accel_int | RW | 0x1 | DCD Accelerated Calibration Integer select. Selects the HPFOD divider integer to use during the dcd_accel_fast_lock and dcd_accel_settle intervals. If a fixed integer is selected, a divider synchronization is automatically performed after the fraction reverts to hpfod_int; as with the initial divider synchronization, this occurs before the clock outputs are enabled. When set to 0x0, use the integer programmed in hpfod_int. When set to 0x1, use integer 100. 0x0 = hpfod_int 0x1 = 100 |
| 7:6 | dcd_accel_frac | RW | 0x1 | DCD Accelerated Calibration Fraction select. Selects the HPFOD divider fraction to use during the dcd_accel_fast_lock and dcd_accel_settle intervals. If a fixed fraction is selected, a divider synchronization is automatically performed after the fraction reverts to hpfod_frac; as with the initial divider synchronization, this occurs before the clock outputs are enabled. When set to 0x0, use the fraction programmed in hpfod_frac. Otherwise use the selected fraction. 0x0 = hpfod_frac 0x1 = 0.25 0x2 = 0.5 |
| 5:3 | dcd_accel_fast_lock | RW | 0x1 | DCD Accelerated Calibration Fast Lock Time Interval. The amount of time to run the DCD calibration with dcd_fast_lock set to 1 after the FOD comes out of reset (automatically during the startup sequence if fod_rst is 0 (on power-up or due to apll_reinit), or after startup when the fod_rst bit transitions from 1 to 0). If the dcd_accel_frac field is non-zero, the fraction is forced to a fixed value during this time. 0x0 = 0ms (disabled) 0x1 = 0.5ms 0x2 = 1.0ms 0x3 = 2ms 0x4 = 4ms 0x7 = 16us |
| 2:0 | dcd_accel_settle | RW | 0x0 | DCD Accelerated Calibration Settling Time Interval. The amount of time to run the DCD calibration with dcd_fast_lock set to 0 after the dcd_accel_fast_lock interval ends, and before enabling clock outputs. If the dcd_accel_frac field is non-zero, the fraction is forced to a fixed value during this time. 0x0 = 0ms (disabled) 0x1 = 0.5ms 0x2 = 1.0ms 0x3 = 2ms 0x4 = 4ms 0x7 = 16us |

3.12.4 DCD_CTRL

DCD Status Selection.

| DCD_CTRL Bit Field Descriptions | | | | |
|---------------------------------|----------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:2 | reserved | RO | 0x0 | Reserved |
| 1:0 | dcd_status_sel | RW | 0x0 | DCD Calibration Status Select. Selects the status to read back through gro_st_cnt and i_err_sts. Refer to those fields for details. |

3.13 LPFOD

Limited Performance Fractional Output Divider Registers.

Table 15. LPFOD Register Index

| Offset (Hex) | Register Module Base Address: 0x170 | |
|--------------|-------------------------------------|--|
| | Register Name | Register Description |
| 0x0 | LPFOD_INT_CNFG | LPFOD Divider/Configuration |
| 0x8 | LPFOD_PHASE_CNFG | LPFOD Phase Configuration |
| 0xA | LPFOD_MIN_DIV_PH_FRAC | LPFOD Minimum Divider for Phase and Fractional Support |

3.13.1 LPFOD_INT_CNFG

LPFOD Divider/Configuration.

| LPFOD_INT_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|-----------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 63 | lpfod_pd | RW | 0x0 | Limited Performance Fractional Output Divider Power Down. Powers down the LP fractional output divider by turning off the regulator. If this bit is set to 1, lpfod_rst must also be set to 1. When clearing this bit, lpfod_rst must remain set and then it may be cleared afterwards. 0x0 = powered up 0x1 = powered down |
| 62 | lpfod_dis | RW | 0x0 | Limited Performance Fractional Output Divider Disable. Disables the LP fractional output divider. If this bit is set to 1, lpfod_rst must also be set to 1. When clearing this bit, lpfod_rst must remain set and then it may be cleared afterwards. 0x0 = enabled 0x1 = disabled |
| 61 | lpfod_rst | RW | 0x0 | Limited Performance Fractional Output Divider Reset. Resets the LP fractional output divider. 0x0 = reset deasserted 0x1 = reset asserted |
| 60 | lpfod_sdm_order | RW | 0x0 | Limited Performance Fractional Output Divider SDM Order. Selects the order of the SDM controlling the LP FOD MMD. First order must be selected if lpfod_frac is non-zero. If the lpfod_int divider is less than the value in lpfod_min_div_ph_frac_supp, then fractional division is not supported and the order must be set to integer mode. 0x0 = Integer (no modulation) 0x1 = 1st order |

| LPFOD_INT_CNFG Bit Field Descriptions | | | | |
|---------------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 59:26 | lpfod_frac | RW | 0x0 | Limited Performance Fractional Output Divider Ratio Fraction portion. Denominator is fixed to 2^{34} . If the lpfod_int value is less than the value in lpfod_min_div_ph_frac_supp, the LPFOD does not support fractional dividers and this field will be ignored and overridden to 0. If applying a new lpfod_frac value through a serial bus write (not through OTP), please set lpfod_rst to '1', write the new value into the lpfod_frac field, and then set lpfod_rst to '0' to latch the new value. This register field is part of an atomic group consisting of lpfod_int and lpfod_frac. When the most significant byte (bits [33:30]) of lpfod_frac is written, the value of all these fields are applied to the LPFOD. |
| 25 | reserved | RO | 0x0 | Reserved |
| 24:0 | lpfod_int | RW | 0x64 | Limited Performance Fractional Output Divider Ratio Integer portion. Integer divide ratio. If the lpfod_int value is less than the value in lpfod_min_div_ph_frac_supp, fractional dividers and phase adjustments cannot be used and the field lpfod_ph_adj_post_sync should always be set to 0. This field should only be programmed when lpfod_rst is high. If applying a new lpfod_int value through a serial bus write (not through OTP), please set lpfod_rst to '1', write the new value into the lpfod_int field, and then set lpfod_rst to '0' to latch the new value. This register field is part of an atomic group consisting of lpfod_int and lpfod_frac. When the most significant byte (bits [33:30]) of lpfod_frac is written, the value of all these fields are applied to the LPFOD. Note: Refer to lpfod_frac for details regarding serial bus writes to this register field. |

3.13.2 LPFOD_PHASE_CNFG

LPFOD Phase Configuration.

| LPFOD_PHASE_CNFG Bit Field Descriptions | | | | |
|---|------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15 | lpfod_ph_adj_now | RW1S | 0x0 | Limited Performance Fractional Output Divider Phase Adjustment Now. When this bit is written from 0 to 1, the phase adjustment in lpfod_phase is applied to the divider. This bit self-clears when the adjust completes. If the lpfod_int value is less than the value in lpfod_min_div_ph_frac_supp, this bit should never be set. This bit should not be set if lpfod_pd = 1 or lpfod_rst = 1. |
| 14 | lpfod_ph_adj_post_sync | RW | 0x0 | Limited Performance Fractional Output Divider Phase Adjustment After Synchronization. When this bit is set to 1, the phase adjustment in lpfod_phase is applied to the divider whenever the divider is synchronized. If the lpfod_int value is less than the value in lpfod_min_div_ph_frac_supp, this bit should never be set. This bit should not be set if lpfod_pd = 1 or lpfod_rst = 1. |
| 13:9 | reserved | RO | 0x0 | Reserved |

| LPFOD_PHASE_CNFG Bit Field Descriptions | | | | |
|---|-------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 8:0 | lpfod_phase | RW | 0x0 | Limited Performance Fractional Output Divider Phase Configuration. Signed 2's complementary value sets the phase, a positive value means lag from 0 phase, a negative value means lead from 0 phase, in steps of 1 VCO period. The default value of 0 (decimal), or 0 VCO periods, approximately aligns the LP FOD output clock with the IOD output clock, when the LP FOD is configured with an integer divide ratio. If the lpfod_int value is less than the value in lpfod_min_div_ph_frac_supp, phase adjustments are not supported and this field should not be programmed. This register is atomic. When the most significant byte (bits [10:8]) is written, the new value is applied to the LPFOD according to lpfod_ph_adj_now and lpfod_ph_adj_post_sync. |

3.13.3 LPFOD_MIN_DIV_PH_FRAC

LPFOD Minimum Divider for Phase and Fractional Support.

| LPFOD_MIN_DIV_PH_FRAC Bit Field Descriptions | | | | |
|--|----------------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:6 | reserved | RO | 0x0 | Reserved |
| 5:0 | lpfod_min_div_ph_frac_supp | RW | 0x31 | Minimum allowed integer divide value for LPFOD phase adjust and fractional divider support. This value is used to control the minimum allowed integer divider value for which the LPFOD supports having the SDM turned on. If the programmed integer divider value is less than this value, the SDM is disabled, the LPFOD will divide only by the integer portion (ignore the fractional part), and phase adjustments are not allowed. This field is not meant to be modified, it is for debugging only. |

3.14 OUT

Output control registers.

Table 16. OUT Register Index

| Offset (Hex) | Register Module Base Address: 0x190 | |
|--------------|-------------------------------------|-----------------------------|
| | Register Name | Register Description |
| 0x0 | ODRV_EN | Output Driver Settings |
| 0x2 | ODRV_CNFG | Output Driver Configuration |

3.14.1 ODRV_EN

Output Driver Settings.

| ODRV_EN Bit Field Descriptions | | | | |
|--------------------------------|---------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | out_pd | RW | 0x0 | Output Driver Power Down. Powers down the output clock driver. 0x0 = output driver is powered up 0x1 = output driver is powered down |
| 6 | out_oe_mode | RW | 0x0 | Output Driver OE Mode. Controls whether the output enable acts synchronously or asynchronously with respect to the output divider clock. When OE is synchronized to the divider clock (option 0x0), enabling and disabling the output clock is glitchless. OE transitions take effect after 1 divider clock cycle. When OE is asynchronous to the divider clock (option 0x1), OE transitions while the divider clock is toggling may result in glitches/runt pulses. 0x0 = OE synchronized 0x1 = OE asynchronous |
| 5:3 | out_dis_group | RW | 0x0 | Output Driver OE Group. Sets which OE group this driver is in. 0x0 = group0 0x1 = group1 0x2 = group2 0x3 = group3 0x4 = group4 0x5 = none |
| 2:1 | out_dis_state | RW | 0x3 | OUT Driver disabled state. Controls the state of OUTx / OUTxb when the output driver is disabled. In LVDS mode options 0x0 and 0x03 result in a different state: * 0x0: Held Low/High * 0x3: Held High/Low 0x0 = High/Low (Low/High for LVDS) 0x1 = Low/High 0x2 = Hi-Z/Hi-Z 0x3 = Low/Low (High/Low for LVDS) |
| 0 | reserved | RO | 0x0 | Reserved |

3.14.2 ODRV_CNFG

Output Driver Configuration.

| ODRV_CNFG Bit Field Descriptions | | | | |
|----------------------------------|-------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15 | out_prog7 | RW | 0x0 | Output Driver Programmability Bit 7. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: reserved / flip output polarity / flip output polarity |
| 14 | out_prog6 | RW | 0x1 | Output Driver Programmability Bit 6. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: reserved / fmon = 17 Ohms / reserved |
| 13 | out_prog5 | RW | 0x0 | Output Driver Programmability Bit 5. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: reserved / cross point lower / cross point tune |
| 12 | out_prog4 | RW | 0x0 | Output Driver Programmability Bit 4. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: reserved / cross point increase for double termination / cross point tune |
| 11 | out_prog3 | RW | 0x0 | Output Driver Programmability Bit 3. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: tristate OUTx / driver impedance -5% / cross point tune |
| 10 | out_prog2 | RW | 0x0 | Output Driver Programmability Bit 2. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: tristate OUTxb / driver impedance +5% / cross point tune |
| 9 | out_prog1 | RW | 0x0 | Output Driver Programmability Bit 1. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: flip OUTx polarity / amplitude -10% / amplitude -10% |
| 8 | out_prog0 | RW | 0x0 | Output Driver Programmability Bit 0. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: flip OUTxb polarity / amplitude +5% / amplitude +5% |
| 7 | sel_fm_drv_predrv | RW | 0x0 | Output Driver Frequency Monitoring Control. Control signal for each output. Selects between driver or predriver to monitor output frequency. 0x0 = driver 0x1 = pre-driver |
| 6 | out_lpamp | RW | 0x0 | Output Driver LPHCSL amplitude control. Controls the amplitude of the output driver when LPHCSL mode is selected. 0x0 = 800mV 0x1 = 900mV |
| 5 | out_lpsr | RW | 0x1 | Output Driver LPHCSL slew rate control. Controls the slew rate of the output driver when LPHCSL mode is selected. Slew rates are measured from -150mV to +150mV from crossing point. 0x0 = slow, 2-4 V/ns 0x1 = fast, >4 V/ns |
| 4 | out_lpimp | RW | 0x1 | Output Driver LPHCSL impedance control. Controls the output impedance of the output driver when LPHCSL mode is selected. 0x0 = 85ohm 0x1 = 100ohm |

| ODRV_CNFG Bit Field Descriptions | | | | |
|----------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 3:2 | out_cmdrv | RW | 0x3 | Output Driver CMOS slew rate control. Controls the slew rate of the output driver (in V/ns) when CMOS mode is selected, according to the supply voltage level of 3.3V / 2.5V / 1.8V: 0x0 = 4.2 / 2.7 / 1.8 0x1 = 2.7 / 1.5 / 1.8 0x2 = 2.7 / 1.5 / 1.8 0x3 = 3.4 / 2.0 / 1.9 |
| 1:0 | out_mode | RW | 0x0 | Output Driver type. Selects the output driver type. 0x0 = LPHCSL 0x1 = LVDS 0x2 = LVDS 0x3 = CMOS |

3.15 BANK

Output bank control registers.

Table 17. BANK Register Index

| Offset (Hex) | Register Module Base Address: 0x1C0 | |
|--------------|-------------------------------------|--|
| | Register Name | Register Description |
| 0x0 | OUT_BANK_CNFG | Output Bank Configuration, Powerdown, and Source |

3.15.1 OUT_BANK_CNFG

Output Bank Configuration, Powerdown, and Source.

| OUT_BANK_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|---------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:6 | vdet_cnf | RW | 0x1 | Output bank trip point control. These bits control the VDD Detect Trip Point for each output bank. |
| 5 | out_fm_switch | RW | 0x1 | Enable frequency monitor feedback switch. This bit enables the analog path for the output frequency monitoring switch for each bank. 0x0 = disabled 0x1 = Analog output frequency monitoring switch enabled |
| 4 | bank_pd | RW | 0x0 | Output Bank Power Down. Powers down the output bank by turning off the regulator. 0x0 = powered up 0x1 = powered down |
| 3 | reserved | RO | 0x0 | Reserved |

| OUT_BANK_CNFG Bit Field Descriptions | | | | |
|--------------------------------------|-----------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 2:0 | output_bank_src | RW | 0x5 | Output Bank Source. Sets the clock source of each output bank. Some configurations may be reserved based on table Output Bank Source Mapping. When the APLL reference clock is selected (option 0x7), the selected crystal input for the APLL is used as the source. 0x0 = LP FOD0 0x1 = LP FOD1 0x2 = IOD1 0x3 = IOD0 0x4 = HP FOD0 0x5 = HP FOD1 0x6 = HP FOD2 0x7 = APLL ref clock |

3.16 GPI

GPI control registers.

Table 18. GPI Register Index

| Offset (Hex) | Register Module Base Address: 0x1F0 | |
|--------------|-------------------------------------|----------------------|
| | Register Name | Register Description |
| 0x0 | GPI_CNFG | GPI Configuration |

3.16.1 GPI_CNFG

GPI Configuration.

| GPI_CNFG Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | reserved | RO | 0x0 | Reserved |
| 6 | gpi_pol | RW | 0x0 | GPI Polarity. Sets the active polarity. This bit is ignored if gpi_func configures the pin as a clock input. 0x0 = active high 0x1 = active low |
| 5 | gpi_pull | RW | 0x0 | GPI Pull. Sets the internal pull-down mode. This bit is ignored and the internal pull-down is enabled if gpi_func configures the pin as a clock input. 0x0 = no pull 0x1 = pull-down |

| GPI_CNFG Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 4:0 | gpi_func | RW | 0x1F | GPI Functions. Sets the general purpose input function. For option 0x7, the input status may be read back via I2C in gpi0_sts/gpi1_sts 0x0 = OE[0], input, enable output drivers in OE group 0 0x1 = OE[1], input, enable output drivers in OE group 1 0x2 = OE[2], input, enable output drivers in OE group 2 0x3 = OE[3], input, enable output drivers in OE group 3 0x4 = OE[4], input, enable output drivers in OE group 4 0x5 = GOE, input, enable all output drivers 0x7 = GPI, input 0x1F = GPI function disabled, pin used as clock input |

3.17 GPIO

GPIO control registers.

Table 19. GPIO Register Index

| Offset (Hex) | Register Module Base Address: 0x200 | |
|--------------|-------------------------------------|----------------------|
| | Register Name | Register Description |
| 0x0 | GPIO_CNFG | GPIO Configuration |

3.17.1 GPIO_CNFG

GPIO Configuration.

| GPIO_CNFG Bit Field Descriptions | | | | |
|----------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:12 | reserved | RO | 0x0 | Reserved |
| 11 | gpo_sync | RW | 0x1 | GPO Sync outputs with system clock. GPO are synced with system clock when pad is configured as an output. 0x0 = not synced with system clock 0x1 = synced with system clock |
| 10:9 | gpo_drv | RW | 0x0 | GPO Drive Strength. Applies to the pad when configured as an output (gpio_type is 0x0 or 0x2). Drive strength increases as this setting increases. Open-drain mode (gpio_type is 0x0) 0x0: I2C: 1.8V Standard mode, 2.5V/3.3V Standard & Fast mode 0x1: I2C: 1.8V Fast mode 0x2: reserved 0x3: I2C: 1.8V/2.5V/3.3V Fast-mode Plus Push-pull mode only for GPIO0 (gpio_type is 0x2) 0x0: for 3.3V power 0x1: for 2.5V power 0x2: for 1.8V power 0x3: for 1.5V power (reserved) |

| GPIO_CNFG Bit Field Descriptions | | | | |
|----------------------------------|-----------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 8:7 | gpio_type | RW | 0x1 | GPIO type. Sets the direction and type following reset Push pull output (option 0x2) is only supported for GPIO0. 0x0 = output (open-drain) 0x1 = input 0x2 = push pull output (driven high/low) |
| 6 | gpio_pol | RW | 0x1 | GPIO Polarity. Sets the active polarity. 0x0 = active high 0x1 = active low |
| 5 | gpio_pull | RW | 0x1 | GPIO Pull. Sets the internal pull-down mode 0x0 = no pull 0x1 = pull-down |
| 4:0 | gpio_func | RW | 0x7 | GPIO Functions. Sets the general purpose input/output function. Additional information for options: * option 0x7: input status may be read back via I2C in gpio0_sts-gpio6_sts * option 0x8: used to control external functions (such as LEDs). The output value is set in gpo0_ctrl-gpo6_ctrl. * option 0x10: the clock rate is set by gpio_fault_clock_div * option 0x11: the clock rate is set by gpio_int_clock_div * option 0x1F: this is for GPIO0 only 0x0 = OE[0], input, enable output drivers in OE group 0 0x1 = OE[1], input, enable output drivers in OE group 1 0x2 = OE[2], input, enable output drivers in OE group 2 0x3 = OE[3], input, enable output drivers in OE group 3 0x4 = OE[4], input, enable output drivers in OE group 4 0x5 = GOE, input, enable all output drivers 0x6 = Primary xtal disable, input 0x7 = GPI, input 0x8 = GPO, output 0x9 = FAULT, output |
| | gpio_func (continued) | | | 0xA = INT, output 0xB = apll_lock_sts, output 0xC = Crystal 0 los_sts, output 0xD = Crystal 1 los_sts, output 0xE = device_ready, output 0xF = i2c_crc_err, output 0x10 = toggle for no FAULT, static for FAULT 0x11 = toggle for no INT, static for INT 0x1F = test clock according to test_clock_sel |

3.18 INT

Interrupt and fault registers.

Table 20. INT Register Index

| Offset (Hex) | Register Module Base Address: 0x220 | |
|--------------|-------------------------------------|------------------------------------|
| | Register Name | Register Description |
| 0x0 | AUTO_ACTION_EN | Automatic Action Enables |
| 0x4 | INT_EN | Interrupt Enable |
| 0x8 | FAULT_EN | Fault Enable |
| 0xC | DEVICE_EVENT | Device Event Latched Status |
| 0x10 | MISC_EVENT | Miscellaneous Latched Event Status |
| 0x14 | EVENT_GEN | Event Generation |
| 0x18 | MON_EN | Monitor Enables |
| 0x1C | SCRATCH0 | Scratch Register |

3.18.1 AUTO_ACTION_EN

Automatic Action Enables.

| AUTO_ACTION_EN Bit Field Descriptions | | | | |
|---------------------------------------|-------------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:29 | reserved | RO | 0x0 | Reserved |
| 28 | vco_cal_timeout_action_en | RW | 0x0 | VCO Calibration Timeout Automatic Action Enable. When this field is set to 1, the vco_cal_timeout event will trigger safe if this event occurs and its fault_en bit is set. |
| 27 | reserved | RO | 0x0 | Reserved |
| 26 | otp_crc_err_action_en | RW | 0x0 | Configuration Loader Error Automatic Action Enable. When this field is set to 1, the otp_crc_err event will trigger safe if this event occurs and its fault_en bit is set. |
| 25 | i2c_crc_err_action_en | RW | 0x0 | I2C CRC Error Automatic Action Enable. When this field is set to 1, the i2c_crc_err event will trigger safe if this event occurs and its fault_en bit is set. |
| 24 | csr_sig_reload_fail_action_en | RW | 0x0 | CSR Signature Check Reload Automatic Action Enable. When this field is set to 1, the csr_sig_reload_fail event will trigger safe if this event occurs and its fault_en bit is set. |
| 23 | csr_sig_fail_action_en | RW | 0x0 | CSR Signature Check Failure Automatic Action Enable. When this field is set to 1, the csr_sig_fail event will trigger safe if this event occurs and its fault_en bit is set. |
| 22 | dual_xtal_fail_action_en | RW | 0x0 | Dual Crystal Failure Automatic Action Enable. When this field is set to 1, the dual_xtal_fail event will trigger safe if this event occurs and its fault_en bit is set. |
| 21 | xtal_switch_action_en | RW | 0x0 | Crystal Switch Event Automatic Action Enable. When this field is set to 1, the xtal_switch event will trigger safe if this event occurs and its fault_en bit is set. |

| AUTO_ACTION_EN Bit Field Descriptions | | | | |
|---------------------------------------|-------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 20:9 | freq_action_en | RW | 0x0 | Output Clock Frequency Automatic Action Automatic Action Enable. When a bit in this field is set to 1, if the corresponding freqX_evt occurs, the output will be disabled. Safe state also will be triggered if the corresponding freqX_evt occurs and its fault_en bit is set. Bit [11] = freq11_evt ... Bit [0] = freq0_evt |
| 8:7 | xtal_st_err_action_en | RW | 0x0 | Crystal Short Term Automatic Action Automatic Action Enable. When a bit in this field is set to 1, the corresponding xtalX_st_err event will trigger safe if this event occurs and its fault_en bit is set. [Bit 1] = xtal1_st_err [Bit 0] = xtal0_st_err |
| 6 | xtal_ppm_err_action_en | RW | 0x0 | Crystal PPM Automatic Action Error Automatic Action Enable. When this field is set to 1, the xtal_ppm_err event will trigger safe if this event occurs and its fault_en bit is set. |
| 5 | xtal_ppm_warn_action_en | RW | 0x0 | Crystal PPM Automatic Action Warning Automatic Action Enable. When this field is set to 1, the xtal_ppm_warn event will trigger safe if this event occurs and its fault_en bit is set. |
| 4:3 | los_action_en | RW | 0x0 | Crystal Loss-of-Signal Automatic Action Enable. When a bit in this field is set to 1, the corresponding losX_evt event will trigger safe if this event occurs and its fault_en bit is set. [Bit 1] = los1_evt [Bit 0] = los0_evt |
| 2 | apll_lol_action_en | RW | 0x0 | APLL Loss-of-Lock Automatic Action enable. When this field is set to 1, the apll_lol event will trigger safe if this event occurs and its fault_en bit is set. |
| 1 | reserved | RO | 0x0 | Reserved |
| 0 | post_fail_action_en | RW | 0x0 | POST Failure Automatic Action Enable. When this field is set to 1, the post_fail event will trigger safe if this event occurs and its fault_en bit is set. |

3.18.2 INT_EN

Interrupt Enable.

| INT_EN Bit Field Descriptions | | | | |
|-------------------------------|------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31 | device_int_en | RW | 0x0 | Device Interrupt Enable. Overall device interrupt enable. When this field is set to 1, the device interrupt is asserted on the GPIO (selected by gpio_func) while device_int_sts is 1. |
| 30:29 | reserved | RO | 0x0 | Reserved |
| 28 | vco_cal_timeout_int_en | RW | 0x0 | VCO Calibration Timeout Interrupt Enable. When this field is set to 1, the vco_cal_timeout bit contributes to the device interrupt. |
| 27 | otp_load_fail_int_en | RW | 0x0 | Configuration Loader Failure Interrupt Enable. When this field is set to 1, the otp_load_fail bit contributes to the device interrupt. |
| 26 | otp_crc_err_int_en | RW | 0x0 | Configuration Loader Error Interrupt Enable. When this field is set to 1, the otp_crc_err bit contributes to the device interrupt. |

| INT_EN Bit Field Descriptions | | | | |
|-------------------------------|----------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 25 | i2c_crc_err_int_en | RW | 0x0 | I2C CRC Error Interrupt Enable. When this field is set to 1, the i2c_crc_err bit contributes to the device interrupt. |
| 24 | csr_sig_reload_fail_int_en | RW | 0x0 | CSR Signature Check Reload Interrupt Enable. When this field is set to 1, the csr_sig_reload_fail bit contributes to the device interrupt. |
| 23 | csr_sig_fail_int_en | RW | 0x0 | CSR Signature Check Failure Interrupt Enable. When this field is set to 1, the csr_sig_fail bit contributes to the device interrupt. |
| 22 | dual_xtal_fail_int_en | RW | 0x0 | Dual Crystal Failure Interrupt Enable. When this field is set to 1, the dual_xtal_fail bit contributes to the device interrupt. |
| 21 | xtal_switch_int_en | RW | 0x0 | Crystal Switch Event Interrupt Enable. When this field is set to 1, the xtal_switch bit contributes to the device interrupt. |
| 20:9 | freq_int_en | RW | 0x0 | Output Clock Frequency Monitor Interrupt Enable. When a bit in this field is set to 1, the corresponding freqX_evt bit contributes to the device interrupt. Bit [11] = freq11_evt ... Bit [0] = freq0_evt |
| 8:7 | xtal_st_err_int_en | RW | 0x0 | Crystal Short Term Monitor Interrupt Enable. When a bit in this field is set to 1, the corresponding xtalX_st_err bit contributes to the device interrupt. [Bit 1] = xtal1_st_err [Bit 0] = xtal0_st_err |
| 6 | xtal_ppm_err_int_en | RW | 0x0 | Crystal PPM Monitor Error Interrupt Enable. When this field is set to 1, the xtal_ppm_err bit contributes to the device interrupt. |
| 5 | xtal_ppm_warn_int_en | RW | 0x0 | Crystal PPM Monitor Warning Interrupt Enable. When this field is set to 1, the xtal_ppm_warn bit contributes to the device interrupt. |
| 4:3 | los_int_en | RW | 0x0 | Crystal Loss-of-Signal Interrupt Enable. When a bit in this field is set to 1, the corresponding losX_evt bit contributes to the device interrupt. [Bit 1] = los1_evt [Bit 0] = los0_evt |
| 2 | apll_lol_int_en | RW | 0x0 | APLL Loss-of-Lock interrupt enable. When this field is set to 1, the apll_lol bit contributes to the device interrupt. |
| 1 | reserved | RO | 0x0 | Reserved |
| 0 | post_fail_int_en | RW | 0x0 | POST Failure Interrupt Enable. When this field is set to 1, the post_fail bit contributes to the device interrupt. |

3.18.3 FAULT_EN

Fault Enable.

| FAULT_EN Bit Field Descriptions | | | | |
|---------------------------------|--------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31 | device_fault_en | RW | 0x0 | Device Fault Enable. Overall device fault enable. When this field is set to 1, the device fault is asserted on the GPIO (selected by gpio_func) and to set the part into safe state while device_fault_sts is 1. |
| 30:29 | reserved | RO | 0x0 | Reserved |
| 28 | vco_cal_timeout_fault_en | RW | 0x0 | VCO Calibration Timeout Fault Enable. When this field is set to 1, the vco_cal_timeout bit contributes to the device fault. |

| FAULT_EN Bit Field Descriptions | | | | |
|---------------------------------|------------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 27 | otp_load_fail_fault_en | RW | 0x0 | Configuration Loader Failure Fault Enable. When this field is set to 1, the otp_load_fail bit contributes to the device fault. |
| 26 | otp_crc_err_fault_en | RW | 0x0 | Configuration Loader Error Fault Enable. When this field is set to 1, the otp_crc_err bit contributes to the device fault. |
| 25 | i2c_crc_err_fault_en | RW | 0x0 | I2C CRC Error Fault Enable. When this field is set to 1, the i2c_crc_err bit contributes to the device fault. |
| 24 | csr_sig_reload_fail_fault_en | RW | 0x0 | CSR Signature Check Reload Fault Enable. When this field is set to 1, the csr_sig_reload_fail bit contributes to the device fault. |
| 23 | csr_sig_fail_fault_en | RW | 0x0 | CSR Signature Check Failure Fault Enable. When this field is set to 1, the csr_sig_fail bit contributes to the device fault. |
| 22 | dual_xtal_fail_fault_en | RW | 0x0 | Dual Crystal Failure Fault Enable. When this field is set to 1, the dual_xtal_fail bit contributes to the device fault. |
| 21 | xtal_switch_fault_en | RW | 0x0 | Crystal Switch Event Fault Enable. When this field is set to 1, the xtal_switch bit contributes to the device fault. |
| 20:9 | freq_fault_en | RW | 0x0 | Output Clock Frequency Monitor Fault Enable. When a bit in this field is set to 1, the corresponding freqX_evt bit contributes to the device fault. Bit [11] = freq11_evt ... Bit [0] = freq0_evt |
| 8:7 | xtal_st_err_fault_en | RW | 0x0 | Crystal Short Term Monitor Fault Enable. When a bit in this field is set to 1, the corresponding xtalX_st_err bit contributes to the device fault. [Bit 1] = xtal1_st_err [Bit 0] = xtal0_st_err |
| 6 | xtal_ppm_err_fault_en | RW | 0x0 | Crystal PPM Monitor Error Fault Enable. When this field is set to 1, the xtal_ppm_err bit contributes to the device fault |
| 5 | xtal_ppm_warn_fault_en | RW | 0x0 | Crystal PPM Monitor Warning Fault Enable. When this field is set to 1, the xtal_ppm_warn bit contributes to the device fault |
| 4:3 | los_fault_en | RW | 0x0 | Crystal Loss-of-Signal Fault Enable. When a bit in this field is set to 1, the corresponding losX_evt bit contributes to the device fault. [Bit 1] = los1_evt [Bit 0] = los0_evt |
| 2 | apll_lol_fault_en | RW | 0x0 | APLL Loss-of-Lock Fault enable. When this field is set to 1, the apll_lol bit contributes to the device fault. |
| 1 | reserved | RO | 0x0 | Reserved |
| 0 | post_fail_fault_en | RW | 0x0 | POST Failure Fault Enable. When this field is set to 1, the post_fail bit contributes to the device fault. |

3.18.4 DEVICE_EVENT

Device Event Latched Status.

| DEVICE_EVENT Bit Field Descriptions | | | | |
|-------------------------------------|---------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:29 | reserved | RO | 0x0 | Reserved |
| 28 | vco_cal_timeout | RW1C | 0x0 | VCO Calibration Timeout latched status. When high, indicates the VCO Calibration timed out or no XTAL is enabled for the calibration to use and VCO Calibration was not bypassed. |
| 27 | otp_load_fail | RW1C | 0x0 | Configuration Loader Failure latched status. When high, indicates the OTP load failed during device startup. Cleared by writing it to 1. |
| 26 | otp_crc_err | RW1C | 0x0 | Configuration Loader Error latched status. When high, indicates the OTP load encountered one or more CRC errors during device startup. Cleared by writing it to 1. |
| 25 | i2c_crc_err | RW1C | 0x0 | I2C CRC Error Event latched status. Set to 1 when an I2C CRC error is detected. |
| 24 | csr_sig_reload_fail | RW1C | 0x0 | CSR Signature Check Reload latched status. Set to 1 if the CRC-32 value calculated during a CSR check (readable in csr_sig_calc) does not match the expected value programmed in csr_sig_exp, and csr_sig_err_mode is set to 1 and the reload of the registers fails. |
| 23 | csr_sig_fail | RW1C | 0x0 | CSR Signature Check Failure latched status. Set to 1 if the CRC-32 value calculated during a CSR check (readable in csr_sig_calc) does not match the expected value programmed in csr_sig_exp, and csr_sig_err_mode is set to 0. |
| 22 | dual_xtal_fail | RW1C | 0x0 | Dual Crystal Failure latched status. Set to 1 when automatic crystal selection is enabled, the selected crystal becomes invalid, and the other crystal is also invalid. The device does not switch to the other crystal in this case. |
| 21 | xtal_switch | RW1C | 0x0 | Crystal Switch Event latched status. Set to 1 when the device automatically switches the crystal selected for the APLL reference clock. |
| 20 | freq11_evt | RW1C | 0x0 | Output Clock 11 Frequency Monitor event latched status. Set to 1 when the Output Clock 11 (True or Complement) Frequency Monitor detects a failure. |
| 19 | freq10_evt | RW1C | 0x0 | Output Clock 10 Frequency Monitor event latched status. Set to 1 when the Output Clock 10 (True or Complement) Frequency Monitor detects a failure. |
| 18 | freq9_evt | RW1C | 0x0 | Output Clock 9 Frequency Monitor event latched status. Set to 1 when the Output Clock 9 (True or Complement) Frequency Monitor detects a failure. |
| 17 | freq8_evt | RW1C | 0x0 | Output Clock 8 Frequency Monitor event latched status. Set to 1 when the Output Clock 8 (True or Complement) Frequency Monitor detects a failure. |
| 16 | freq7_evt | RW1C | 0x0 | Output Clock 7 Frequency Monitor event latched status. Set to 1 when the Output Clock 7 (True or Complement) Frequency Monitor detects a failure. |
| 15 | freq6_evt | RW1C | 0x0 | Output Clock 6 Frequency Monitor event latched status. Set to 1 when the Output Clock 6 (True or Complement) Frequency Monitor detects a failure. |
| 14 | freq5_evt | RW1C | 0x0 | Output Clock 5 Frequency Monitor event latched status. Set to 1 when the Output Clock 5 (True or Complement) Frequency Monitor detects a failure. |

| DEVICE_EVENT Bit Field Descriptions | | | | |
|-------------------------------------|---------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 13 | freq4_evt | RW1C | 0x0 | Output Clock 4 Frequency Monitor event latched status. Set to 1 when the Output Clock 4 (True or Complement) Frequency Monitor detects a failure. |
| 12 | freq3_evt | RW1C | 0x0 | Output Clock 3 Frequency Monitor event latched status. Set to 1 when the Output Clock 3 (True or Complement) Frequency Monitor detects a failure. |
| 11 | freq2_evt | RW1C | 0x0 | Output Clock 2 Frequency Monitor event latched status. Set to 1 when the Output Clock 2 (True or Complement) Frequency Monitor detects a failure. |
| 10 | freq1_evt | RW1C | 0x0 | Output Clock 1 Frequency Monitor event latched status. Set to 1 when the Output Clock 1 (True or Complement) Frequency Monitor detects a failure. |
| 9 | freq0_evt | RW1C | 0x0 | Output Clock 0 Frequency Monitor event latched status. Set to 1 when the Output Clock 0 (True or Complement) Frequency Monitor detects a failure. |
| 8 | xtal1_st_err | RW1C | 0x0 | Crystal 1 Short Term Monitor Error Event latched status. Set to 1 when the crystal short term monitor detects that the crystal 1 frequency exceeds the threshold (see st_max_thresh). |
| 7 | xtal0_st_err | RW1C | 0x0 | Crystal 0 Short Term Monitor Error Event latched status. Set to 1 when the crystal short term monitor detects that the crystal 0 frequency exceeds the threshold (see st_max_thresh). |
| 6 | xtal_ppm_err | RW1C | 0x0 | Crystal PPM Monitor Error Event latched status. Set to 1 when the crystal PPM monitor detects an error condition (see ppm_err_thresh). |
| 5 | xtal_ppm_warn | RW1C | 0x0 | Crystal PPM Monitor Warning Event latched status. Set to 1 when the crystal PPM monitor detects a warning condition (see ppm_warn_thresh). |
| 4 | los1_evt | RW1C | 0x0 | Crystal 1 Loss-of-Signal Event latched status. Set to 1 when the Crystal 1 LOS monitor detects Loss Of Signal. 0x0 = Loss-of-signal not detected since the last time the bit was cleared 0x1 = Loss-of-signal detected since the last time the bit was cleared |
| 3 | los0_evt | RW1C | 0x0 | Crystal 0 Loss-of-Signal Event latched status. Set to 1 when the Crystal 0 LOS monitor detects Loss Of Signal. 0x0 = Loss-of-signal not detected since the last time the bit was cleared 0x1 = Loss-of-signal detected since the last time the bit was cleared |
| 2 | apll_lol | RW1C | 0x0 | APLL Loss-of-lock event latched status. Set to 1 when the APLL lock status transitions from locked to unlocked. |
| 1 | reserved | RO | 0x0 | Reserved |
| 0 | post_fail | RW1C | 0x0 | POST Failure latched status. Set to 1 when POST detects a failure. |

3.18.5 MISC_EVENT

Miscellaneous Latched Event Status.

| MISC_EVENT Bit Field Descriptions | | | | |
|-----------------------------------|--------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | reserved | RO | 0x0 | Reserved |
| 6 | apll_rail_high_evt | RW1C | 0x0 | APLL Rail High event latched status. Set to 1 when the APLL lock detects a rail high status. Once asserted, this bit will remain asserted until cleared by a write of '1' to this bit position. This bit cannot contribute to an interrupt or fault. |
| 5 | apll_rail_low_evt | RW1C | 0x0 | APLL Rail Low event latched status. Set to 1 when the APLL lock detects a rail low status. Once asserted, this bit will remain asserted until cleared by a write of '1' to this bit position. This bit cannot contribute to an interrupt or fault. |
| 4 | otp_manual_rdy | RW1C | 0x0 | OTP Manual ready indicator latched status. When high, indicates an OTP manual request (including Program Assist) completed. Cleared by writing it to 1. This bit cannot contribute to an interrupt or fault. |
| 3 | status_latched | RW1C | 0x0 | OTP macro output pin latched status. Latched value of the OTP macro output pin. Can be cleared by writing 1 to it. If STATUS is still high when clearing is attempted, this bit will immediately be set to 1 again. Cannot contribute to the device interrupt or fault output. |
| 2 | vpp_error | RW1C | 0x0 | OTP VPP error. This error bit signals that the internal charge pump was idle longer than the maximum time permitted. See the OTP datasheet for details. This bit gets cleared by writing one to it. It cannot be cleared unless the internal condition has gone away (i.e., VPP_MON has been de-asserted). Cannot contribute to the device interrupt or fault output. |
| 1 | pgm_assist_fail | RW1C | 0x0 | Program Assist failure. When high, indicates that the Program Assist sequence failed to program one or more bits in the OTP word. Cannot contribute to the device interrupt or fault output. |
| 0 | otp_config_empty | RW1C | 0x0 | OTP Load of Empty Configuration. When high, indicates the OTP load attempted to load a configuration that did not select any blocks. Cleared by writing it to 1. Cannot contribute to the device interrupt or fault output. |

3.18.6 EVENT_GEN

Event Generation.

| EVENT_GEN Bit Field Descriptions | | | | |
|----------------------------------|---------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:29 | reserved | RO | 0x0 | Reserved |
| 28 | vco_cal_timeout_gen | WO | 0x0 | VCO Calibration Timeout Event Generate. When this field is set to 1, the vco_cal_timeout bit is set. This field always reads 0. |
| 27 | otp_load_fail_gen | WO | 0x0 | Configuration Loader Failure Event Generate. When this field is set to 1, the otp_load_fail bit is set. This field always reads 0. |
| 26 | otp_crc_err_gen | WO | 0x0 | Configuration Loader Error Event Generate. When this field is set to 1, the otp_crc_err bit is set. This field always reads 0. |
| 25 | i2c_crc_err_gen | WO | 0x0 | I2C CRC Error Event Generate. When this field is set to 1, the i2c_crc_err bit is set. This field always reads 0. |

| EVENT_GEN Bit Field Descriptions | | | | |
|----------------------------------|-------------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 24 | csr_sig_reload_fail_gen | WO | 0x0 | CSR Signature Check Reload Event Generate. When this field is set to 1, the csr_sig_reload_fail bit is set. This field always reads 0. |
| 23 | csr_sig_fail_gen | WO | 0x0 | CSR Signature Check Failure Event Generate. When this field is set to 1, the csr_sig_fail bit is set. This field always reads 0. |
| 22 | dual_xtal_fail_gen | WO | 0x0 | Dual Crystal Failure Event Generate. When this field is set to 1, the dual_xtal_fail bit is set. This field always reads 0. |
| 21 | xtal_switch_gen | WO | 0x0 | Crystal Switch Event Generate. When this field is set to 1, the xtal_switch bit is set. This field always reads 0. |
| 20 | freq11_gen | WO | 0x0 | Output Clock 11 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq11_evt bit is set. This field always reads 0. |
| 19 | freq10_gen | WO | 0x0 | Output Clock 10 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq10_evt bit is set. This field always reads 0. |
| 18 | freq9_gen | WO | 0x0 | Output Clock 9 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq9_evt bit is set. This field always reads 0. |
| 17 | freq8_gen | WO | 0x0 | Output Clock 8 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq8_evt bit is set. This field always reads 0. |
| 16 | freq7_gen | WO | 0x0 | Output Clock 7 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq7_evt bit is set. This field always reads 0. |
| 15 | freq6_gen | WO | 0x0 | Output Clock 6 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq6_evt bit is set. This field always reads 0. |
| 14 | freq5_gen | WO | 0x0 | Output Clock 5 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq5_evt bit is set. This field always reads 0. |
| 13 | freq4_gen | WO | 0x0 | Output Clock 4 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq4_evt bit is set. This field always reads 0. |
| 12 | freq3_gen | WO | 0x0 | Output Clock 3 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq3_evt bit is set. This field always reads 0. |
| 11 | freq2_gen | WO | 0x0 | Output Clock 2 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq2_evt bit is set. This field always reads 0. |
| 10 | freq1_gen | WO | 0x0 | Output Clock 1 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq1_evt bit is set. This field always reads 0. |
| 9 | freq0_gen | WO | 0x0 | Output Clock 0 Frequency Monitor Event Generate. When a bit in this field is set to 1, the freq0_evt bit is set. This field always reads 0. |
| 8 | xtal1_st_err_gen | WO | 0x0 | Crystal 1 Short Term Monitor Event Generate. When this field is set to 1, the xtal1_st_err bit is set. This field always reads 0. |
| 7 | xtal0_st_err_gen | WO | 0x0 | Crystal 0 Short Term Monitor Event Generate. When this field is set to 1, the xtal0_st_err bit is set. This field always reads 0. |
| 6 | xtal_ppm_err_gen | WO | 0x0 | Crystal PPM Monitor Error Event Generate. When this field is set to 1, the xtal_ppm_err bit is set. This field always reads 0. |
| 5 | xtal_ppm_warn_gen | WO | 0x0 | Crystal PPM Monitor Warning Event Generate. When this field is set to 1, the xtal_ppm_warn bit is set. This field always reads 0. |
| 4 | los1_gen | WO | 0x0 | Crystal 1 Loss-of-Signal Event Generate. When a bit in this field is set to 1, the los1_evt bit is set. This field always reads 0. |
| 3 | los0_gen | WO | 0x0 | Crystal 0 Loss-of-Signal Event Generate. When a bit in this field is set to 1, the los0_evt bit is set. This field always reads 0. |

| EVENT_GEN Bit Field Descriptions | | | | |
|----------------------------------|---------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 2 | apll_lol_gen | WO | 0x0 | APLL Loss-of-Lock Event Generate. When this field is written to 1, the apll_lol bit is set. This field always reads 0. |
| 1 | reserved | RO | 0x0 | Reserved |
| 0 | post_fail_gen | WO | 0x0 | POST Failure Event Generate. When this field is set to 1, the post_fail bit is set. This field always reads 0. |

3.18.7 MON_EN

Monitor Enables.

| MON_EN Bit Field Descriptions | | | | |
|-------------------------------|----------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:29 | reserved | RO | 0x0 | Reserved |
| 28 | vco_cal_timeout_mon_en | RW | 0x1 | VCO Calibration Timeout Monitor Enable. When this field is set to 1, the vco_cal_timeout is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. |
| 27 | reserved | RO | 0x0 | Reserved |
| 26 | otp_crc_err_mon_en | RW | 0x1 | Configuration Loader Error Monitor Enable. When this field is set to 1, the otp_crc_err is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. |
| 25 | i2c_crc_err_mon_en | RW | 0x1 | I2C CRC Error Monitor Enable. When this field is set to 1, the i2c_crc_err is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. |
| 24 | csr_sig_reload_fail_mon_en | RW | 0x1 | CSR Signature Check Reload Monitor Enable. When this field is set to 1, the csr_sig_reload_fail is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. |
| 23 | csr_sig_fail_mon_en | RW | 0x1 | CSR Signature Check Failure Monitor Enable. When this field is set to 1, the csr_sig_fail is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. |
| 22 | dual_xtal_fail_mon_en | RW | 0x1 | Dual Crystal Failure Monitor Enable. When this field is set to 1, the dual_xtal_fail is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. |
| 21 | xtal_switch_mon_en | RW | 0x1 | Crystal Switch Event Monitor Enable. When this field is set to 1, the xtal_switch is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. |
| 20:9 | freq_mon_en | RW | 0xFFF | Output Clock Frequency Monitor Enable. When a bit in this field is set to 1, the corresponding freqX_evt is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. Bit [11] = freq11_evt ... Bit [0] = freq0_evt |

| MON_EN Bit Field Descriptions | | | | |
|-------------------------------|----------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 8:7 | xtal_st_err_mon_en | RW | 0x3 | Crystal Short Term Monitor Enable. When a bit in this field is set to 1, the corresponding xtalX_st_err is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. Both crystals are needed for the short term monitor to function, so both xtal_st_err_mon_en bits should be enabled (set to 1) for dual crystal cases or both should be disabled (set to 0) for single crystal cases or if the short term monitor feature is not desired. [Bit 1] = xtal1_st_err [Bit 0] = xtal0_st_err |
| 6 | xtal_ppm_err_mon_en | RW | 0x1 | Crystal PPM Monitor Error Monitor Enable. When this field is set to 1, the xtal_ppm_err bit contributes to the device fault |
| 5 | xtal_ppm_warn_mon_en | RW | 0x1 | Crystal PPM Monitor Warning Monitor Enable. When this field is set to 1, the xtal_ppm_warn bit contributes to the device fault |
| 4:3 | los_mon_en | RW | 0x3 | Crystal Loss-of-Signal Monitor Enable. When a bit in this field is set to 1, the corresponding losX_evt is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. [Bit 1] = los1_evt [Bit 0] = los0_evt |
| 2 | apll_lol_mon_en | RW | 0x1 | APLL Loss-of-Lock Monitor enable. When this field is set to 1, the apll_lol is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. |
| 1 | reserved | RO | 0x0 | Reserved |
| 0 | post_fail_mon_en | RW | 0x1 | POST Failure Monitor Enable. When this field is set to 1, the post_fail is monitored for errors and can set the mapped bit in the DEVICE_EVENT register. |

3.18.8 SCRATCH0

Scratch Register.

| SCRATCH0 Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:0 | scratch0 | RW | 0x0 | Scratch register. For arbitrary software use. |

3.19 STATUS

Status registers.

Table 21. STATUS Register Index

| Offset (Hex) | Register Module Base Address: 0x280 | |
|--------------|-------------------------------------|------------------------------|
| | Register Name | Register Description |
| 0x0 | CSR_SIG_STS | CSR Signature Status |
| 0x4 | DEVICE_STS | Device Status |
| 0x8 | STARTUP_STS | Startup Bond/GPI/GPIO Status |
| 0xB | SSI_STS | I2C CRC Error Count |
| 0xC | GPIO_STS | GPI/GPIO Status |

Table 21. STATUS Register Index

| Offset (Hex) | Register Module Base Address: 0x280 | |
|--------------|-------------------------------------|---|
| | Register Name | Register Description |
| 0xE | BIAS_STS | Bias Status |
| 0x10 | APLL_STS | APLL Status |
| 0x11 | VCO_CAL_STS | VCO Calibration Status |
| 0x12 | VCO_TRIM_STS | VCO Trim Calibration Status |
| 0x14 | ANA_SPARE_STS | Analog Spare Status and Voltage Detector Status |
| 0x16 | LOSMON_STS | LOS Monitor Status |
| 0x17 | PPM_MON_STS | PPM Monitor Status |
| 0x18 | FREQMON_STS | Output Frequency Monitor Status |
| 0x1C | OTP_STS | OTP Status |
| 0x1D | OTP_ERR_CNT | OTP CRC Error Count |
| 0x1E | OTP_PARAM | OTP Parameters |
| 0x20 | DIG_POST_STS | Digital POST Status |
| 0x24 | ANA_POST_STS | Analog POST Status |
| 0x28 | DIG_POST_FSM_STS | Digital POST State Machine Status |
| 0x2A | ANA_POST_FSM_STS | Digital POST State Machine Status |

3.19.1 CSR_SIG_STS

CSR Signature Status.

| CSR_SIG_STS Bit Field Descriptions | | | | |
|------------------------------------|--------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:0 | csr_sig_calc | RO | 0x0 | Calculated CSR Signature. Provides the CRC-32 value calculated during the last CSR check. |

3.19.2 DEVICE_STS

Device Status.

| DEVICE_STS Bit Field Descriptions | | | | |
|-----------------------------------|------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:26 | reserved | RO | 0x0 | Reserved |
| 25 | device_int_sts | RO | 0x0 | Device interrupt status. Overall device interrupt status. This bit is the OR of all the event bits in the DEVICE_EVENT register after masking by their respective interrupt enable bits in the INT_EN register. This bit is masked by device_int_en. The resulting signal can be output on the assigned GPIO pin. |
| 24 | device_fault_sts | RO | 0x0 | Device fault status. Overall device fault status. This bit is the OR of all the event bits in the DEVICE_EVENT register after masking by their respective fault enable bits in the FAULT_EN register. This bit is masked by device_fault_en. The resulting signal can be output on the assigned GPIO pin and used to put the part into safe state. |

| DEVICE_STS Bit Field Descriptions | | | | |
|-----------------------------------|------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 23:20 | reserved | RO | 0x0 | Reserved |
| 19 | lbist_done | RO | 0x0 | Logic BIST Done Status. When set, indicates that the device has completed logic BIST. |
| 18 | reset_done | RO | 0x0 | Reset Done Status. When set, indicates that the device has completed its full boot sequence. |
| 17:14 | startup_seq_sts | RO | 0x0 | Startup Sequence Status. Status related to the startup sequence. This field is intended for debug purposes only. Bit 0: Bias calibration timeout (2ms) Bit 1: Configuration load timeout (15ms). Bit 2: APLL lock timeout (2ms) Bit 3: VCO Calibration timeout (programmable in vco_cal_timer) |
| 13 | ssc1_active | RO | 0x0 | Active status of SSC1. Indicates whether the SSC engine 1 is active. 0x0 = SSC is inactive or is done 0x1 = SSC is active |
| 12 | ssc0_active | RO | 0x0 | Active status of SSC0. Indicates whether the SSC engine 0 is active. 0x0 = SSC is inactive or is done 0x1 = SSC is active |
| 11 | ana_post_done | RO | 0x0 | Analog BIST Done. Set to 1 when analog logic BIST completes, if enabled to run during the POST by ana_post_en. Will be implemented for Rev A. |
| 10 | dig_post_done | RO | 0x0 | Digital BIST Done. Set to 1 when digital logic BIST completes, if enabled to run during the POST by dig_bist_en. Will be implemented for Rev A. |
| 9 | osc_fallback | RO | 0x0 | Power-on-Reset Ring Oscillator Fallback. Set to 1 if the system clock divider output does not begin toggling during the startup sequence and the reset controller muxes the ring oscillator clock onto the system clock instead. |
| 8 | xtal_sel_sts | RO | 0x0 | Selected Crystal Status. Indicates which crystal is currently selected. 0x0 = crystal 0 0x1 = crystal 1 |
| 7 | device_ready | RO | 0x0 | Device Ready. Set to 1 when the OTP configuration load completes during the startup sequence. |
| 6 | config_reg_ro | RO | 0x0 | Configuration register read-only status. When this bit is 1, writes to configuration registers are ignored. Writes to bits of type RW1C, self-clearing bits, reg_lock_key and certain RW and RW1S bits always succeed; refer to Configuration Register Lock for more details. This will be implemented in Rev A. Use the reg_lock_key field (only in Rev A and later) to set/clear this bit. |
| 5 | otp_detect_se | RO | 0x0 | OTP Loader Detected Single-Ended Mode. When high, indicates that the OTP loader detected that the OTP image is configured for single-ended mode. |
| 4 | otp_config_valid | RO | 0x0 | Valid OTP User Configuration Loaded. Indicates that the user configuration in config_loaded was successfully loaded from OTP. |
| 3:0 | config_loaded | RO | 0x0 | User Configuration Loaded. Indicates the user configuration loaded from OTP/EEPROM on start-up or a dynamic configuration load. Note that on startup, the common configuration is always loaded prior to the user configuration. |

3.19.3 STARTUP_STS

Startup Bond/GPI/GPIO Status.

| STARTUP_STS Bit Field Descriptions | | | | |
|------------------------------------|-----------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:10 | reserved | RO | 0x0 | Reserved |
| 9 | bond_id | RO | 0x0 | Bond ID value. Value of bond ID die pads. bit [0] = BOND0 |
| 8:7 | gpi_at_startup | RO | 0x0 | GPI Value Latched at Startup. Value of GPI pins latched at startup. Bit [1] = GPI1 Bit [0] = GPIO |
| 6:0 | gpio_at_startup | RO | 0x0 | GPIO Value Latched at Startup. Value of GPIO pins latched at startup. Bit [6] = GPIO6 ... bit [0] = GPIO0 |

3.19.4 SSI_STS

I2C CRC Error Count.

| SSI_STS Bit Field Descriptions | | | | |
|--------------------------------|-----------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:0 | i2c_crc_err_cnt | RW | 0x0 | I2C CRC Error Counter. This counter increments each time the I2C interface detects a CRC error, and saturates at 0xFF. It is cleared by writing it to 0x0, and may be preset by writing the desired value. Preset may be used either as a debug tool. |

3.19.5 GPIO_STS

GPI/GPIO Status.

| GPIO_STS Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:9 | reserved | RO | 0x0 | Reserved |
| 8 | gpi1_sts | RO | 0x0 | GPI1 Status. Indicates the status of the GPI1 pin without latching and without applying optional polarity inversion (gpi_pol). If a pin is configured to be a reference clock input (see gpi_func), the status reads back as 0. pin = XOUT1_REFIN1b_GPI1 |
| 7 | gpi0_sts | RO | 0x0 | GPIO Status. Indicates the status of the GPIO pin without latching and without applying optional polarity inversion (gpi_pol). If a pin is configured to be a reference clock input (see gpi_func), the status reads back as 0. pin = XIN1_REFIN1_GPIO |
| 6 | gpio6_sts | RO | 0x0 | GPIO6 Status. Indicates the status of the GPIO6 pin without latching and without applying optional polarity inversion (gpio_pol). |
| 5 | gpio5_sts | RO | 0x0 | GPIO5 Status. Indicates the status of the GPIO5 pin without latching and without applying optional polarity inversion (gpio_pol). |
| 4 | gpio4_sts | RO | 0x0 | GPIO4 Status. Indicates the status of the GPIO5 pin without latching and without applying optional polarity inversion (gpio_pol). |

| GPIO_STS Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 3 | gpio3_sts | RO | 0x0 | GPIO3 Status. Indicates the status of the GPIO3 pin without latching and without applying optional polarity inversion (gpio_pol). |
| 2 | gpio2_sts | RO | 0x0 | GPIO2 Status. Indicates the status of the GPIO2 pin without latching and without applying optional polarity inversion (gpio_pol). |
| 1 | gpio1_sts | RO | 0x0 | GPIO1 Status. Indicates the status of the GPIO1 pin without latching and without applying optional polarity inversion (gpio_pol). |
| 0 | gpio0_sts | RO | 0x0 | GPIO0 Status. Indicates the status of the GPIO0 pin without latching and without applying optional polarity inversion (gpio_pol). |

3.19.6 BIAS_STS

Bias Status.

| BIAS_STS Bit Field Descriptions | | | | |
|---------------------------------|------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:13 | reserved | RO | 0x0 | Reserved |
| 12 | bias_cal_in | RO | 0x0 | Bias Calibration comparator value. Raw bias_cal_in value. |
| 11:7 | cnf_bias_cal_eff | RO | 0x0 | Bias Calibration effective configuration value. Indicates the configuration value selected as sent to the bias control circuit (i.e., including the offset as configured in bias_cnf_rescal_offset). Valid when bias_cal_done is set to 1. |
| 6:2 | cnf_bias_cal | RO | 0x0 | Bias Calibration configuration value. Indicates the configuration value selected by the bias calibration logic. Valid when bias_cal_done is set to 1. |
| 1 | bias_cal_fail | RO | 0x0 | Bias Calibration failed. Indicates whether bias calibration completed successfully. Valid when bias_cal_done is set to 1. 0x0 = Bias calibration succeeded 0x1 = Bias calibration failed |
| 0 | bias_cal_done | RO | 0x0 | Bias Calibration done. Indicates whether bias calibration is running: 0x0 = Bias calibration is in progress 0x1 = Bias calibration is completed |

3.19.7 APLL_STS

APLL Status.

| APLL_STS Bit Field Descriptions | | | | |
|---------------------------------|--------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:3 | reserved | RO | 0x0 | Reserved |
| 2 | apll_rail_high_sts | RO | 0x0 | APLL Rail High real-time status. When high, indicates that the APLL is railed high. |

| APLL_STS Bit Field Descriptions | | | | |
|---------------------------------|-------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 1 | apll_rail_low_sts | RO | 0x0 | APLL Rail Low real-time status. When high, indicates that the APLL is railed low. |
| 0 | apll_lock_sts | RO | 0x0 | APLL lock status. Set to 1 when the APLL is locked to its reference. 0x0 = unlocked 0x1 = locked |

3.19.8 VCO_CAL_STS

VCO Calibration Status.

| VCO_CAL_STS Bit Field Descriptions | | | | |
|------------------------------------|--------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | vco_cal_fail | RO | 0x0 | VCO Calibration failed. Indicates whether VCO calibration completed successfully. Valid when vco_cal_done is set to 1. 0x0 = VCO calibration succeeded 0x1 = VCO calibration failed |
| 6 | vco_cal_done | RO | 0x0 | VCO Calibration done. Indicates whether VCO calibration is running: 0x0 = VCO calibration is in progress 0x1 = VCO calibration is completed |
| 5:0 | vco_cap | RO | 0x0 | VCO Calibration frequency band. Indicates the frequency band selected by the VCO calibration logic. Valid when vco_cal_done is set to 1. |

3.19.9 VCO_TRIM_STS

VCO Trim Calibration Status.

| VCO_TRIM_STS Bit Field Descriptions | | | | |
|-------------------------------------|--------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:2 | reserved | RO | 0x0 | Reserved |
| 1:0 | vco_trim_val | RO | 0x1 | Coarse VCO Tuning Value. Indicates the current VCO trim value. This reflects the value of vco_trim when vco_trim_cal_en is set to 0. When vco_trim_cal_en is set to 1, this field indicates the value selected by the VCO calibration logic. |

3.19.10 ANA_SPARE_STS

Analog Spare Status and Voltage Detector Status.

| ANA_SPARE_STS Bit Field Descriptions | | | | |
|--------------------------------------|---------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:7 | ana_spare_sts | RO | 0x0 | Analog Spare Status Bits. Spare register bits connected to analog. Unused. |
| 6 | vddo6_sts | RO | 0x0 | Bank 6 voltage detector status. Trip point detection for bank 6. 0x0 = Output driver 1.8V regulator is bypassed 0x1 = Output driver 1.8V regulator is enabled |

| ANA_SPARE_STS Bit Field Descriptions | | | | |
|--------------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 5 | vddo5_sts | RO | 0x0 | Bank 5 voltage detector status. Trip point detection for bank 5. 0x0 = Output driver 1.8V regulator is bypassed 0x1 = Output driver 1.8V regulator is enabled |
| 4 | vddo4_sts | RO | 0x0 | Bank 4 voltage detector status. Trip point detection for bank 4. 0x0 = Output driver 1.8V regulator is bypassed 0x1 = Output driver 1.8V regulator is enabled |
| 3 | vddo3_sts | RO | 0x0 | Bank 3 voltage detector status. Trip point detection for bank 3. 0x0 = Output driver 1.8V regulator is bypassed 0x1 = Output driver 1.8V regulator is enabled |
| 2 | vddo2_sts | RO | 0x0 | Bank 2 voltage detector status. Trip point detection for bank 2. 0x0 = Output driver 1.8V regulator is bypassed 0x1 = Output driver 1.8V regulator is enabled |
| 1 | vddo1_sts | RO | 0x0 | Bank 1 voltage detector status. Trip point detection for bank 1. 0x0 = Output driver 1.8V regulator is bypassed 0x1 = Output driver 1.8V regulator is enabled |
| 0 | vddo0_sts | RO | 0x0 | Bank 0 voltage detector status. Trip point detection for bank 0. 0x0 = Output driver 1.8V regulator is bypassed 0x1 = Output driver 1.8V regulator is enabled |

3.19.11 LOSMON_STS

LOS Monitor Status.

| LOSMON_STS Bit Field Descriptions | | | | |
|-----------------------------------|--------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:4 | reserved | RO | 0x0 | Reserved |
| 3:2 | xtal_invalid | RO | 0x0 | Crystal Clock Invalid status. Indicates whether this crystal is currently considered to be invalid. This occurs if the clock is disqualified by one or more of the Loss-of-Signal and Short Term monitors, or xtal_disable is set to 1. [Bit 1] = xtal1 invalid [Bit 0] = xtal0 invalid 0x0 = Crystal is valid 0x1 = Crystal is invalid |
| 1:0 | los_sts | RO | 0x0 | Loss-of-Signal status. Current value of the LOS status from the monitor. [Bit 1] = Crystal 1 LOS monitor [Bit 0] = Crystal 0 LOS monitor 0x0 = Clock meets the monitoring criteria 0x1 = Loss-of-signal detected |

3.19.12 PPM_MON_STS

PPM Monitor Status.

| PPM_MON_STS Bit Field Descriptions | | | | |
|------------------------------------|---------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:0 | xtal_ppm_diff | RO | 0x0 | PPM difference. Shows the raw ppm difference in 2ppm/lb measured by the crystal ppm monitoring block. This register is updated every 500 thousand xtal clk cycles, so the update rate depends on xtal clk frequency. For example: - 8MHz xtal clk, updates every 62.5ms - 62.5MHz xtal clk, updates every 8ms |

3.19.13 FREQMON_STS

Output Frequency Monitor Status.

| FREQMON_STS Bit Field Descriptions | | | | |
|------------------------------------|---------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:24 | reserved | RO | 0x0 | Reserved |
| 23:12 | freq_outb_sts | RO | 0x0 | Complementary Output Clock Frequency Monitor status. Value of the complementary output clock (OUTxB) frequency monitor status from the last monitoring window. Bit [11] = Complementary Output Clock 11 Frequency Monitor ... Bit [0] = Complementary Output Clock 0 Frequency Monitor 0x0 = Clock meets the monitoring criteria 0x1 = Clock does not meet the monitoring criteria, failure detected |
| 11:0 | freq_out_sts | RO | 0x0 | Output Clock Frequency Monitor status. Value of the true output clock (OUTx) frequency monitor status from the last monitoring window. Bit [11] = Output Clock 11 Frequency Monitor ... Bit [0] = Output Clock 0 Frequency Monitor 0x0 = Clock meets the monitoring criteria 0x1 = Clock does not meet the monitoring criteria, failure detected |

3.19.14 OTP_STS

OTP Status.

| OTP_STS Bit Field Descriptions | | | | |
|--------------------------------|-------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | manual_busy | RO | 0x0 | Manual access busy indicator. When high, indicates a manual request (including Program Assist) has started and is ongoing. |
| 6 | status | RO | 0x0 | OTP macro output pin status. Current value seen on the OTP macro output pin, synchronized to system clock. |
| 5 | vppmon | RO | 0x0 | OTP VPP_MON status. Current value of VPP_MON status, synchronized to system clock. |
| 4 | pwr_up | RO | 0x0 | OTP Power Up. Current value seen on the OTP PWR_UP pin, synchronized to system clock. |

| OTP_STS Bit Field Descriptions | | | | |
|--------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 3 | reserved | RO | 0x0 | Reserved |
| 2:0 | fsm_state | RO | 0x0 | OTP control FSM state. Current value of the FSM state. 0x0 = RESET 0x1 = PWR_UP_RECOVERY 0x2 = RESET_RECOVERY 0x4 = IDLE 0x5 = SETUP 0x7 = PULSE 0x3 = HOLD 0x6 = RECOVERY |

3.19.15 OTP_ERR_CNT

OTP CRC Error Count.

| OTP_ERR_CNT Bit Field Descriptions | | | | |
|------------------------------------|-----------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:4 | reserved | RO | 0x0 | Reserved |
| 3:0 | otp_crc_err_cnt | RW | 0x0 | OTP CRC Error Counter. This counter increments each time the loader detects a CRC error while reading the OTP, and saturates at 0xF. It is cleared by writing it to 0x0, and may be preset by writing the desired value. Preset may be used as a debug tool. Clear on read cannot be used due to read caching of the SSI AMBA master. This register can only be written if the block is not clock gated (otp_cg). |

3.19.16 OTP_PARAM

OTP Parameters.

| OTP_PARAM Bit Field Descriptions | | | | |
|----------------------------------|--------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:14 | otp_scr_size | RO | 0x2 | OTP Scratch Area Size in Words. Indicates the number of bytes reserved for the scratch area in the OTP: 0x0 = 0 bytes 0x1 = reserved 0x2 = 32 bytes 0x3 = reserved |
| 13:12 | otp_ea_size | RO | 0x1 | OTP Entry Address Size. Indicates the number of bytes used for the CSR address in the block entries. 0x0 = 1 bytes 0x1 = 2 bytes 0x2 = 4 bytes |
| 11 | otp_ba_size | RO | 0x1 | OTP Base Address Size. Indicates the number of bytes used for the base address pointer to each block within the OTP. 0x0 = 1 bytes 0x1 = 2 bytes |

| OTP_PARAM Bit Field Descriptions | | | | |
|----------------------------------|----------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 10:8 | otp_size | RO | 0x2 | OTP Size in Bytes. Indicates the effective number of bytes in the OTP. In differential mode, this indicates half of the physical number of bytes. 0x0 = 512B 0x1 = 1KB 0x2 = 2KB 0x3 = 4KB 0x4 = 8KB 0x5 = 16KB 0x6 = 32KB 0x7 = 64KB |
| 7:3 | otp_configs | RO | 0x7 | OTP User Configuration Count. Indicates the number of OTP user configurations supported, less one. 0x7 = 8 user configurations |
| 2:0 | otp_loader_ver | RO | 0x4 | OTP Loader Version. Indicates the OTP loader version. 0x0 = OTP loader used in Merlin test vehicle 0x1 = OTP loader used in Merlin rev A 0x2 = OTP loader used in VC7 test vehicle 0x3 = OTP loader used in VC7 rev A 0x4 = OTP loader used in Autoclock TV |

3.19.17 DIG_POST_STS

Digital POST Status.

| DIG_POST_STS Bit Field Descriptions | | | | |
|-------------------------------------|------------------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:24 | reserved | RO | 0x0 | Reserved |
| 23 | csr_sig_post_fail_sts | RO | 0x0 | CSR signature monitor POST failure. Indicates an error was found in the CSR Signature Monitor POST. |
| 22 | dual_xtal_fail_post_fail_sts | RO | 0x0 | Dual crystal fail POST failure. Indicates an error was found during the Dual XTAL fail POST. |
| 21 | xtal_sw_post_fail_sts | RO | 0x0 | Crystal switching POST failure. Indicates an error was found during the XTAL switching POST. |
| 20:9 | freq_post_fail_sts | RO | 0x0 | Frequency monitor POST failure. Indicates an error was found during the output frequency monitor POST for the given output. |
| 8 | xtal1_st_err_post_fail_sts | RO | 0x0 | XTAL1 ST error POST failure. Indicates an error was found during the XTAL1 short term monitor POST. |
| 7 | xtal0_st_err_post_fail_sts | RO | 0x0 | XTAL0 ST error POST failure. Indicates an error was found during the XTAL0 short term monitor POST. |
| 6 | xtal_ppm_err_post_fail_sts | RO | 0x0 | XTAL PPM error POST failure. Indicates an error was found during the XTAL PPM error POST. |
| 5 | xtal_ppm_warn_post_fail_sts | RO | 0x0 | XTAL PPM warning POST failure. Indicates an error was found during the XTAL PPM warning POST. |
| 4 | los1_post_fail_sts | RO | 0x0 | Loss-of-Signal xtal 1 POST failure. Indicates an error was found during the XTAL1 Loss of signal POST. |

| DIG_POST_STS Bit Field Descriptions | | | | |
|-------------------------------------|------------------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 3 | los0_post_fail_sts | RO | 0x0 | Loss-of-Signal xtal 0 POST failure. Indicates an error was found during the XTAL0 Loss of signal POST. |
| 2 | apll_lol_post_fail_sts | RO | 0x0 | APLL LOL POST failure. Indicates an error was found during the APLL LOL POST. |
| 1 | lbist_fail_sts | RO | 0x0 | Digital Logic BIST failure. Indicates an error was found in the digital logic BIST. |
| 0 | dig_post_fail_sts | RO | 0x0 | Digital POST failure. Indicates an error was found in the overall digital POST. |

3.19.18 ANA_POST_STS

Analog POST Status.

| ANA_POST_STS Bit Field Descriptions | | | | |
|-------------------------------------|--------------------------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:21 | reserved | RO | 0x0 | Reserved |
| 20 | bias_cal_ana_post_fail_sts | RO | 0x0 | Analog POST Bias calibration failure. When 1, indicates Bias Calibration included in Analog POST Failed. |
| 19 | vco_cal_ana_post_fail_sts | RO | 0x0 | Analog POST VCO calibration failure. When 1, indicates VCO Calibration included in Analog POST Failed. |
| 18 | ana_post_ldo_low_fault_det_fail_sts | RO | 0x0 | Analog LDO Low Fault Detection POST Fail. When 1, indicates Analog LDO Low Fault Detection POST Failed. |
| 17 | ana_post_ldo_in_range_det_fail_sts | RO | 0x0 | Analog LDO In Range Detection POST Fail. When 1, indicates Analog LDO In Range Detection POST Failed. |
| 16 | ana_post_ldo_high_fault_det_fail_sts | RO | 0x0 | Analog LDO High Fault Detection POST Fail. When 1, indicates Analog LDO High Fault Detection POST Failed. |
| 15 | ana_post_ref_x1_ldo_fail_sts | RO | 0x0 | Analog POST Reference X1 LDO Fail. When 1, indicates Analog Reference X1 LDO POST Failed. |
| 14 | ana_post_ref_x0_ldo_fail_sts | RO | 0x0 | Analog POST Reference X0 LDO Fail. When 1, indicates Analog Reference X0 LDO POST Failed. |
| 13 | ana_post_apll_cp_ldo_fail_sts | RO | 0x0 | Analog POST APLL CP LDO Fail. When 1, indicates Analog APLL CP LDO POST Failed. |
| 12 | ana_post_apll_pfd_ldo_fail_sts | RO | 0x0 | Analog POST APLL PFD LDO Fail. When 1, indicates Analog APLL PFD LDO POST Failed. |
| 11 | ana_post_apll_vco_ldo_fail_sts | RO | 0x0 | Analog POST APLL VCO LDO Fail. When 1, indicates Analog APLL VCP LDO POST Failed. |
| 10 | ana_post_od_iod0_ldo_fail_sts | RO | 0x0 | Analog POST Output Divider IOD0 LDO Fail. When 1, indicates Analog Output Divider IOD0 LDO POST Failed. |
| 9 | ana_post_od_iod1_ldo_fail_sts | RO | 0x0 | Analog POST Output Divider IOD1 LDO Fail. When 1, indicates Analog Output Divider IOD1 LDO POST Failed. |
| 8 | ana_post_od_hpfod2_ldo_fail_sts | RO | 0x0 | Analog POST Output Divider HPFOD2 LDO Fail. When 1, indicates Analog Output Divider HPFOD2 LDO POST Failed. |
| 7 | ana_post_od_hpfod1_ldo_fail_sts | RO | 0x0 | Analog POST Output Divider HPFOD1 LDO Fail. When 1, indicates Analog Output Divider HPFOD1 LDO POST Failed. |

| ANA_POST_STS Bit Field Descriptions | | | | |
|-------------------------------------|---------------------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 6 | ana_post_od_hpfod0_ldo_fail_sts | RO | 0x0 | Analog POST Output Divider HPFOD0 LDO Fail. When 1, indicates Analog Output Divider HPFOD0 LDO POST Failed. |
| 5 | ana_post_od_lpfod1_ldo_fail_sts | RO | 0x0 | Analog POST Output Divider LPFOD1 LDO Fail. When 1, indicates Analog Output Divider LPFOD1 LDO POST Failed. |
| 4 | ana_post_od_lpfod0_ldo_fail_sts | RO | 0x0 | Analog POST Output Divider LPFOD0 LDO Fail. When 1, indicates Analog Output Divider LPFOD0 LDO POST Failed. |
| 3 | ana_post_dig_fod_ldo_fail_sts | RO | 0x0 | Analog POST Digital FOD LDO Fail. When 1, indicates Analog Digital FOD LDO POST Failed. |
| 2 | ana_post_dig_apll_ldo_fail_sts | RO | 0x0 | Analog POST Digital APLL Divider LDO Fail. When 1, indicates Analog Digital APLL Divider LDO POST Failed. |
| 1 | ana_post_dig_block_ldo_fail_sts | RO | 0x0 | Analog POST Digital Block LDO Fail. When 1, indicates Analog Digital Block LDO POST Failed. |
| 0 | ana_post_fail_sts | RO | 0x0 | Analog POST Fail. When 1, indicates analog POST failed. |

3.19.19 DIG_POST_FSM_STS

Digital POST State Machine Status.

| DIG_POST_FSM_STS Bit Field Descriptions | | | | |
|---|------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:0 | dig_post_fsm_sts | RO | 0x0 | Digital POST state machine status. Indicates the current state of the Digital POST state machine. |

3.19.20 ANA_POST_FSM_STS

Digital POST State Machine Status.

| ANA_POST_FSM_STS Bit Field Descriptions | | | | |
|---|--------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:9 | reserved | RO | 0x0 | Reserved |
| 8:4 | ana_post_count_sts | RO | 0x0 | Analog POST state machine status. Indicates the current count of the analog POST state machine. |
| 3:0 | ana_post_fsm_sts | RO | 0x0 | Analog POST state machine status. Indicates the current state of the analog POST state machine. |

3.20 DCD_STATUS

DCD Status registers.

Table 22. DCD_STATUS Register Index

| Offset (Hex) | Register Module Base Address: 0x2C0 | |
|--------------|-------------------------------------|------------------------------------|
| | Register Name | Register Description |
| 0x0 | DCD_CALIB_STS | DCD Calibration Status |
| 0x4 | DCD_CALIB2_STS | DCD Accelerated Calibration Status |

3.20.1 DCD_CALIB_STS

DCD Calibration Status.

| DCD_CALIB_STS Bit Field Descriptions | | | | |
|--------------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:15 | gro_st_cnt | RO | 0x0 | DCD Calibration GRO State Counter. The status read through this field is selected by dcd_status_sel: 0x0: Invalid GRO state counter. 0x1: GRO phase status bits 20:15 in gro_st_cnt[5:0]. gro_st_cnt[16:6] are zero. 0x2: Captured GRO status 0x3: GRO status from analog All status information in this register is latched when the register is read. The read back value is the previously latched value. Therefore, the first time the register is read, the read data must be ignored, and subsequent reads return the data latched when the prior read occurred. Also, this register must be read using a 4-byte burst read to get a consistent value across all 4 bytes. |
| 14:0 | i_err_sts | RO | 0x0 | DCD Calibration i_error Status. The status read through this field is selected by dcd_status_sel: 0x0: DCD calibration low pass filter value. This is a signed 2's complement number. 0x1: GRO phase status bits 14:0 0x2: DAC control value in i_err_sts[7:0]. i_err_sts[14:8] are zero. 0x3: Slow calibration value All status information in this register is latched when the register is read. The read back value is the previously latched value. Therefore, the first time the register is read, the read data must be ignored, and subsequent reads return the data latched when the prior read occurred. Also, this register must be read using a 4-byte burst read to get a consistent value across all 4 bytes. |

3.20.2 DCD_CALIB2_STS

DCD Accelerated Calibration Status.

| DCD_CALIB2_STS Bit Field Descriptions | | | | |
|---------------------------------------|------------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:1 | reserved | RO | 0x0 | Reserved |
| 0 | dcd_accel_active | RO | 0x0 | DCD Accelerated Calibration Status. Indicates whether accelerated calibration (duration set by dcd_accel_fast_lock and dcd_accel_settle) is in progress. 0x0 = accelerated calibration completed or FOD is in reset 0x1 = accelerated calibration is active |

3.21 CTRL

Control registers.

Table 23. CTRL Register Index

| Offset (Hex) | Register Module Base Address: 0x2E0 | |
|--------------|-------------------------------------|--------------------------------|
| | Register Name | Register Description |
| 0x0 | CSR_SIG | Expected CSR Signature |
| 0x4 | REG_LOCK | Register Lock Key |
| 0x5 | INIT_SYNC | Init/Synchronization Register |
| 0x6 | MISC_CTRL | VCO/Bias/CSR Signature Control |

Table 23. CTRL Register Index

| Offset (Hex) | Register Module Base Address: 0x2E0 | |
|--------------|-------------------------------------|----------------------|
| | Register Name | Register Description |
| 0x7 | GPO_CTRL | GPO Output Control |
| 0x8 | OUT_CTRL | Output Control |

3.21.1 CSR_SIG

Expected CSR Signature.

| CSR_SIG Bit Field Descriptions | | | | |
|--------------------------------|-------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 31:0 | csr_sig_exp | RW | 0x0 | Expected CSR Signature. Sets the expected value of the CRC-32 calculated over all CSRs up to the STATUS CSRs. If the CRC-32 value calculated during a CSR check (readable in csr_sig_calc) does not match csr_sig_exp, then either the csr_sig_reload or csr_sig_fail event bit is set to 1 according to csr_sig_err_mode. |

3.21.2 REG_LOCK

Register Lock Key.

| REG_LOCK Bit Field Descriptions | | | | |
|---------------------------------|--------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:0 | reg_lock_key | WO | 0x0 | Configuration register lock key. Writing this field with 0xCB sets the config_reg_ro bit to 1. Writing this field with 0x34 clears the config_reg_ro bit to 0. This will be implemented for Rev A. |

3.21.3 INIT_SYNC

Init/Synchronization Register.

| INIT_SYNC Bit Field Descriptions | | | | |
|----------------------------------|--------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:3 | reserved | RO | 0x0 | Reserved |
| 2 | out_rst | RW | 0x0 | Output Driver Reset. This bit resets and disables all output drivers. Reset assertion acts asynchronously and may causes output glitches or runt pulses. Reset assertion acts synchronously. Inverted and connected to sync_done. |
| 1 | divider_sync | RW1S | 0x0 | Divider Synchronization. Writing this bit to 1 synchronizes the Output Dividers. The output clocks will be squelched for approximately 10us. Self-cleared when the synchronization completes. |
| 0 | apll_reinit | RW1S | 0x0 | APLL Reinitialization. Writing this bit to 1 re-starts the startup sequence from the VCO calibration step, including divider synchronization. Self-cleared when the reinitialization completes. |

3.21.4 MISC_CTRL

VCO/Bias/CSR Signature Control.

| MISC_CTRL Bit Field Descriptions | | | | |
|----------------------------------|--------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7:4 | reserved | RO | 0x0 | Reserved |
| 3 | vco_recal | RW | 0x0 | VCO Calibration trigger. Triggers VCO re-calibration when written to 1. This bit must be written to 0 before it may be triggered again by writing it to 1. This is for debugging only. For full APLL locking, appl_reinit is required. |
| 2 | bias_recal | RW | 0x0 | Bias Calibration trigger. Triggers bias re-calibration when written to 1. This bit must be written to 0 before it may be triggered again by writing it to 1. |
| 1 | reserved | RO | 0x0 | Reserved |
| 0 | csr_sig_trig | WO | 0x0 | CSR Signature Check Trigger. Manually triggers a CSR signature check when written to 1, if an automatic check is not already in progress. Self clears. |

3.21.5 GPO_CTRL

GPO Output Control.

| GPO_CTRL Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|---|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 7 | reserved | RO | 0x0 | Reserved |
| 6 | gpo6_ctrl | RW | 0x0 | GPO output control signal value for GPIO6. Sets the value to drive on GPIO6 pin when configured as a general purpose output by gpio_func. |
| 5 | gpo5_ctrl | RW | 0x0 | GPO output control signal value for GPIO5. Sets the value to drive on GPIO5 pin when configured as a general purpose output by gpio_func. |
| 4 | gpo4_ctrl | RW | 0x0 | GPO output control signal value for GPIO4. Sets the value to drive on GPIO4 pin when configured as a general purpose output by gpio_func. |
| 3 | gpo3_ctrl | RW | 0x0 | GPO output control signal value for GPIO3. Sets the value to drive on GPIO3 pin when configured as a general purpose output by gpio_func. |
| 2 | gpo2_ctrl | RW | 0x0 | GPO output control signal value for GPIO2. Sets the value to drive on GPIO2 pin when configured as a general purpose output by gpio_func. |
| 1 | gpo1_ctrl | RW | 0x0 | GPO output control signal value for GPIO1. Sets the value to drive on GPIO1 pin when configured as a general purpose output by gpio_func. |
| 0 | gpo0_ctrl | RW | 0x0 | GPO output control signal value for GPIO0. Sets the value to drive on GPIO0 pin when configured as a general purpose output by gpio_func. |

3.21.6 OUT_CTRL

Output Control.

| OUT_CTRL Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 15:13 | reserved | RO | 0x0 | Reserved |
| 12 | goe | RW | 0x1 | Output Global OE. This bit allows manual CSR control of the global output OE. |
| 11 | out11_dis | RW | 0x0 | OUT11 and/or OUT11b Driver disable. Forces both OUT11 and OUT11b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information. When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means. 0x0 = enabled 0x1 = disabled |
| 10 | out10_dis | RW | 0x0 | OUT10 and/or OUT10b Driver disable. Forces both OUT10 and OUT10b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information. When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means. 0x0 = enabled 0x1 = disabled |
| 9 | out9_dis | RW | 0x0 | OUT9 and/or OUT9b Driver disable. Forces both Out9 and Out9b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information. When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means. 0x0 = enabled 0x1 = disabled |
| 8 | out8_dis | RW | 0x0 | OUT8 and/or OUT8b Driver disable. Forces both OUT8 and OUT8b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information. When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means. 0x0 = enabled 0x1 = disabled |
| 7 | out7_dis | RW | 0x0 | OUT7 and/or OUT7b Driver disable. Forces both OUT7 and OUT7b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information. When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means. 0x0 = enabled 0x1 = disabled |

| OUT_CTRL Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 6 | out6_dis | RW | 0x0 | <p>OUT6 and/or OUT6b Driver disable. Forces both OUT6 and OUT6b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information.</p> <p>When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means.</p> <p>0x0 = enabled 0x1 = disabled</p> |
| 5 | out5_dis | RW | 0x0 | <p>OUT5 and/or OUT5b Driver disable. Forces both OUT5 and OUT5b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information.</p> <p>When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means.</p> <p>0x0 = enabled 0x1 = disabled</p> |
| 4 | out4_dis | RW | 0x0 | <p>OUT4 and/or OUT4b Driver disable. Forces both OUT4 and OUT4b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information.</p> <p>When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means.</p> <p>0x0 = enabled 0x1 = disabled</p> |
| 3 | out3_dis | RW | 0x0 | <p>OUT3 and/or OUT3b Driver disable. Forces both OUT3 and OUT3b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information.</p> <p>When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means.</p> <p>0x0 = enabled 0x1 = disabled</p> |
| 2 | out2_dis | RW | 0x0 | <p>OUT2 and/or OUT2b Driver disable. Forces both OUT2 and OUT2b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information.</p> <p>When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means.</p> <p>0x0 = enabled 0x1 = disabled</p> |

| OUT_CTRL Bit Field Descriptions | | | | |
|---------------------------------|------------|------------|---------------|--|
| Bit Field | Field Name | Field Type | Default Value | Description |
| 1 | out1_dis | RW | 0x0 | <p>OUT1 and/or OUT1b Driver disable. Forces both OUT1 and OUT1b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information.</p> <p>When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means.</p> <p>0x0 = enabled 0x1 = disabled</p> |
| 0 | out0_dis | RW | 0x0 | <p>OUT0 and/or OUT0b Driver disable. Forces both OUT0 and OUT0b Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. Refer to Output Enable Control for more information.</p> <p>When option 0x0 is selected the OUTx and/or OUTxb Driver is enabled if it is not disabled by other means.</p> <p>0x0 = enabled 0x1 = disabled</p> |

4. Revision History

| Revision | Date | Description |
|----------|--------------|------------------|
| 1.00 | Apr 25, 2024 | Initial release. |

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