User's Manual

Diagnostic Software Safety Manual

User's Manual

Renesas Synergy™ Platform
Renesas Synergy™ Tools & Kits
Tools: Synergy S3 Series MCU Diagnostic Software

Renesas Electronics
www.renesas.com

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Precautions

This Renesas Synergy™ S3 Series MCU Diagnostic Software is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. - There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

• Ensure attached cables do not lie across the equipment.

• Reorient the receiving antenna.

• Increase the distance between the equipment and the receiver.

• Connect the equipment into an outlet on a circuit different from that which the receiver is connected.

• Power down the equipment when not in use.

• Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

• The user is advised that mobile phones should not be used within 10 m of the product when in use.

• The user is advised to take ESD precautions when handling the equipment.

The Renesas Synergy™ S3 Series MCU Diagnostic Software does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

1. Glossary

1.1 Use of Words

Use of the words "shall", "should", "must", "will", and "may" within this Specification observe the following rules:

- The word SHALL in the text expresses a mandatory requirement of the Specification
- The word SHOULD in the text expresses a recommendation or advice on implementing such a requirement of the Specification. REE expects such recommendations or advice to be followed unless good reasons are stated for not doing so.
- The word MUST in the text is used for legislative or regulatory requirements (for example, Health and Safety) with which both REE and the Supplier shall comply. It is not used to express a requirement of the Specification.
- The word WILL in the text expresses a provision or service by REE or an intention by REE in connection with a requirement of the Specification. The Supplier is implicitly authorized to rely on such service or intention.
- The word MAY in the text expresses a permissible practice or action. It does not express a requirement of the Specification.

2. Abbreviations

Ordered	Unordered
ALU	Arithmetic Logic Unit
CISC	Complex Instruction Set Computer
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DC	Direct Current
DFT	Design For Test
DM	Diagnostic Measure
DMA	Direct Memory Access (Controller)
FIT	Failure In Time
FPU	Floating Point Unit
FSCC	Functional Safety Competence Centre
HFT	Hardware Fault Tolerance
HW	Hardware
I/O	Input/Output
MCU	Microcontroller Unit
MPU	Memory Protection Unit
RAM	Random Access Memory
REE	Renesas Electronics Europe
ROM	Read-Only Memory
SC	Systematic Capability
SER	Soft Error Rate
SFF	Safe Failure Fraction
SIL	Safety Integrity Level
SRAM	Static Random Access Memory
SW	Software
WDT	Watchdog Timer

3. Document Scope

This Safety Manual specifies the user's responsibilities for installation and operation in order to use the following item in safety related systems maintaining the specified safety integrity level:

- Renesas Diagnostics Software for Synergy S3 MCU, Version 1.0.1, including:
  - CPU Test, Version (see §4.1)
  - RAM Test, Version (see §4.2)
  - ROM Test, Version (see §4.3)
  - CAC Configuration, Version (see §4.4)
  - iWDT Management, Version (see §4.5)
  - LVD Configuration, Version (see §4.6)

The Renesas Diagnostics Software was developed for use with the Synergy S3 MCU following the IEC61508, 2nd Edition, targeting max. SIL3 applications. It is intended to provide diagnostic coverage for random permanent faults in the CPU, the User RAM and the Flash ROM. It was developed in accordance with IEC61508:2010, Systematic Capability of 3 (SC 3). It can be used in safety related applications up to SIL 3 / SC 3.

The hosting MCU itself has a Hardware Fault Tolerance of 0 (HFT=0) and is a type "B" element according to IEC61508-2:2010.

This document is based on the assumption that the MCU is only used in customer applications adopting fail-silent / fail-flagging system design (fail-operational requirement for MCU is out of scope).

The Renesas Diagnostics Software User Guide [3] is a mandatory reference document for this Safety Manual and has to be followed in order to guarantee full functionality of the Diagnostics Software, avoid unwanted impact on application software and enable Diagnostics Software to be used in safety related applications. In the following sections mainly additional information is given in order to avoid duplication of information.

4. Renesas Diagnostic Software

4.1 CPU Software Tests

4.1.1 Description of functions

The objective of the CPU Software Test is to test the correct functionality of the CPU adopting mainly an instruction based diagnosis with the aim to detect permanent hardware failures of the CPU Core and it's intended to be executed periodically at run-time.

All instructions listed in [2] with the only exception of the BKPT, SEV, WFE, WFI and DMB instructions are used for the core testing.

The CPU Software Test supports the Synergy family members based on the ARM Cortex M4 CPU.

Following parts of the MCU are target of the CPU Software Test with a medium diagnostic coverage:

- ARM Cortex M4 CPU Core Module

Additionally CPU Software Test also utilizes the following modules, but without special requirement of providing a specific diagnostic coverage value:

- Interface to external modules
- Memory Protection Unit (MPU)
- Nested Vectored Interrupt Controller (NVIC)

It has to be noted that the interface modules mentioned above are tested by the RAM Test and the ROM Test of the Renesas Diagnostics Software.

Please refer to Renesas Diagnostics Software User Guide [3] for more detailed description of the functions related to CPU Software Test.

Note: diagnostic measures required for the integrity of the interrupts are in the responsibility of the user.

4.1.2 Software version

All information given in this document is referring to the CPU Software Test, Version 1.0.2.

4.1.3 Recommended configuration

Please refer to the Renesas Diagnostics Software User Guide [3].

4.1.4 Outstanding anomalies

No outstanding anomaly of the CPU Software test is known. Customers will be informed by Renesas in case of anomalies detected on this version.

4.1.5 Compatibility

The CPU Software Test is a porting of the previous PA024 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.1.6 Development environment

The CPU Software Test was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD to be used in safety related applications up to SIL3.

The user shall use this development environment for building the CPU Software Test.

For detailed configuration to be used for the compiler please see [3].

4.1.7 Installation instructions

Please see [3] for instructions how to install the CPU Software Test into the integrated system.

4.1.8 CPU Software Test diagnostic coverage validation

Renesas performed safety validation of the CPU Software Test.

Fault injection performed involves the deliberate introduction of a fault into the netlist to evaluate the effect of a net in the netlist being shorted to VCC or Ground considering the stuck-at fault model. This is a common approach for fault injection and allows the effectiveness of the Diagnostics Software at detecting faults to be evaluated.

Although only stuck-at fault model is used for fault injection the DC fault model is considered for this validation by estimating impact of further fault models (bridge, stuck-open, stuck-on).

The diagnostic coverage value for the CPU Software Test is listed in Table 4.1. The coverage value is evaluated with the precondition that software flow control is temporal monitored.

Table 4.1 Diagnostic coverage of CPU Software Test evaluated by netlist fault injection

Diagnostic coverage value considering DC fault mode	Medium

Diagnostic coverage value is valid for the CPU Software Test including all Test Segments. If different CPU Software Test configuration is used by e.g. leaving out some Test Segments the diagnostic coverage value will decrease.

4.2 RAM Software Test

4.2.1 Description of functions

Objective of the RAM Software Test is to test the embedded RAM memory.

Main features of the RAM Software Test are the following:

- Whole memory check including stack(s)
  - Memory size programmable at compile time
- Block-wise implementation of the test.
  - Size of the block programmable at compile time
- Support of two testing algorithms
  - Extended March C-
  - WALPAT
- Word-wise implementation of the testing algorithms supporting 32 bits width
- Support for destructive and non-destructive memory testing.

Extended March C- test is a very efficient test in terms of fault coverage and execution time. The WALPAT test misses detection of some faults that the Extended March C- test is detecting but has the advantage to detect also sense amplifier faults.

Both tests are giving medium coverage for permanent random hardware faults and the selected one is expected to be executed periodically during the application. This coverage value is valid under the condition that for both tests the minimum block size chosen is not lower than 512 bytes. Transient faults (soft errors) are not covered by the RAM Tests and have to be considered separately.
The SW is intended to be executed periodically at run-time at least for the RAM memories not protected by parity/ECC.

Please see [3] for more information.

4.2.2 Software version

All information given in this document is referring to the RAM Software Test, Version 1.0.1.

4.2.3 Recommended configuration

Please refer to the Renesas Diagnostics Software User Guide [3].

4.2.4 Outstanding anomalies

No outstanding anomaly of the RAM Software test is known. Customers will be informed by Renesas in case of anomalies detected on this version.

4.2.5 Compatibility

The RAM Software Test is a porting of the previous PA024 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.2.6 Development environment

The RAM Software Test was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD to be used in safety related applications up to SIL3.

The user shall use this development environment for building the RAM Software Test.

For detailed configuration to be used for the compiler please see [3].

4.2.7 Installation instructions

Please see [3] for instructions how to install the RAM Software Test into the integrated system.

4.3 ROM Software Test

4.3.1 Description of functions

Objective of the ROM Software Test is to test the whole embedded ROM adopting CRC technique. Error detection is achieved according to the following steps.

1. A range of addresses is chosen, which defines the block under test.
2. A reference checksum value is calculated by the IAR linker and saved inside the ROM.
3. During the ROM Software Test execution, the CRC hardware peripheral (see [1] for the peripheral details) is used to produce an actual checksum value of the ROM content under test in order to check its integrity.
4. Checksum calculated value is compared with the one stored in ROM and an error is flagged if the two values do not match.
5. Previous steps are repeated for a different block of the ROM up to the whole coverage of the used ROM.

Three different CRC polynomials are supported:

- 8-bit CRC:
    1. x^8+x^2+x+1
- 16-bit CRC:
    2. $x^{16}+x^{15}+x^2+1$
    3. $x^{16}+x^{12}+x^5+1$

Please see [3] for more information.

ROM test using the 8-bit CRC gives medium coverage against permanent random hardware faults while the ROM test using the 16-bit CRC gives high coverage in relation to permanent and transient failures.

4.3.2 Software version

All information given in this document is referring to the ROM Software Test, Version 1.0.1.

4.3.3 Recommended configuration

Please refer to the Renesas Diagnostics Software User Guide [3].

4.3.4 Outstanding anomalies

No outstanding anomaly of the ROM Software test is known. Customers will be informed by Renesas in case of anomalies detected on this version.

4.3.5 Compatibility

The ROM Software Test is a porting of the previous PA024 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.3.6 Development environment

The ROM Software Test was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD to be used in safety related applications up to SIL3.

The user shall use this development environment for building the ROM Software Test.

For detailed configuration to be used for the compiler please see [3]..

4.3.7 Installation instructions

Please see [3] for instructions how to install the ROM Software Test into the integrated system.

4.4 CAC Configuration Software

4.4.1 Description of functions

The Synergy S3 has a Clock Frequency Accuracy Measurement Circuit (CAC) which can be used to monitor the system clock frequency during run time to detect deviations.

The objective of the CAC Configuration Software is to configure the CAC. This SW shall be used to:

- Select PCLKB as measurement target clock for the CAC;
- Select Sub-clock oscillator as measurement reference clock for the CAC.

This configuration allows to detect deviations of the Main clock oscillator and PLL due to systematic or random hardware failures.

Note: to ensure effectiveness of this diagnostic measures the application shall configure the Clock Generation Circuit to generate PCLKB via Main clock oscillator and PLL[1].

Note: for the operation of the CAC it is necessary that the reference clock (i.e. the sub-clock oscillator) is supplied. The user shall enable the Sub-clock oscillator through the SOSCCR register (i.e. SOSCCR.SOSTP = 0b, see User Manual [3]). The user can confirm the operation of the sub-clock oscillator by checking that the value of CAC.CACNTBR is not fixed to 0x0000.

The CAC Configuration Software also enables the Synergy S3 Oscillation Stop Detection Circuit functionality. This circuit, in case the Main clock Oscillator stops, is in charge to switch to the Middle-Speed On-Chip oscillator and generate an NMI interrupt. This is provided as additional protection mainly to help diagnosis of problems on the Main clock Oscillator and for fault reaction support.

Please refer to Renesas Diagnostics Software User Guide [3] for more detailed description of the functions related to CAC Configuration Software.

4.4.2 Software version

All information given in this document is referring to the CAC Configuration Software, Version 1.0.2.

4.4.3 Recommended configuration

Please refer to the Renesas Diagnostics Software User Guide [3].

4.4.4 Outstanding anomalies

No outstanding anomaly of the CAC Configuration Software is known. Customers will be informed by Renesas in case of anomalies detected.

4.4.5 Compatibility

The CAC Configuration Software is a porting of the previous PA024 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.4.6 Development environment

The CAC Configuration Software was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD to be used in safety related applications up to SIL3.

The user shall use this development environment for building the CAC Configuration Software.

For detailed configuration to be used for the compiler please see [3].

4.4.7 Installation instructions

Please see [3] for instructions how to install the CAC Configuration Software into the integrated system.

[11] Faults of muxes and dividers involved in the generation of PCLKB are also detectable.

4.5 IWDT Management Software

4.5.1 Description of functions

The Independent Watchdog Timer (IWDT) of the Synergy S3 can be used to detect an abnormal program execution. If a program is not running as expected the IWDT will not be refreshed by software as it is required to be and will therefore react triggering a programmed action.

The IWDT also includes a windowing feature so that the refresh must happen within a specified 'window' rather than just before a specified time. It can be configured to generate an internal reset or a NMI interrupt if an error is detected. Further this Watchdog Timer is also operated on a different and independent clock from the one used for the CPU (ICLK). Consequently also protecting against abnormal program execution caused by random hardware failures. In particular it complements CAC (refer to Section 4.4.1) providing high level of coverage against faults of the mux generating ICLK.

Note: the IWDT is operated by a dedicated on-chip oscillator having a tolerance of 10%. System integrator has to consider if this tolerance is adequate for the target application.

Objective of the IWDT Management Software is to enable the Independent Watchdog peripheral and provide an API to refresh it periodically (based on application requirements). In addition the SW provides to the user an API to check whether the IWDT was the initiator of the last reset.

4.5.2 Software version

All information given in this document is referring to the IWDT Management Software, Version 1.0.1.

4.5.3 Recommended configuration

Please refer to the Renesas Diagnostics Software User Guide [3].

4.5.4 Outstanding anomalies

No outstanding anomaly of the IWDT Management Software is known. Customers will be informed by Renesas in case of anomalies detected on this version.

4.5.5 Compatibility

The IWDT Software Test is a porting of the previous PA024 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.5.6 Development environment

The IWDT Management Software was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD to be used in safety related applications up to SIL3.

The user shall use this development environment for building the IWDT Management Software.

For detailed configuration to be used for the compiler please see [3].

4.5.7 Installation instructions

Please see [3] for instructions how to install the IWDT Management Software into the integrated system.

4.6 LVD Configuration Software

4.6.1 Description of functions

The Synergy S3 has a Voltage Detection Circuit. This can be used to detect the power supply voltage (Vcc) falling below a specified voltage. The supplied sample code demonstrates using Voltage Detection Circuit 1 to generate a NMI interrupt when Vcc drops below a specified level.

Objective of the LVD Configuration Software is to configure the Low Voltage Detection Circuit peripheral according to the user setting provided by its API.

Using this SW it is possible to reach at least a medium level of coverage against permanent random hardware faults leading to Vcc going below Vdet1 threshold (under voltage, drift to lower voltage and spikes to lower voltage longer than 200μs).

Note: this diagnostic measure has to be accompanied by an external voltage monitoring as for example overvoltage conditions are not detected and may lead to damage of the circuit.

4.6.2 Software version

All information given in this document is referring to the LVD Configuration Software, Version 1.0.1.

4.6.3 Recommended configuration

Please refer to the Renesas Diagnostics Software User Guide [3].

4.6.4 Outstanding anomalies

No outstanding anomaly of the LVD Configuration Software is known. Customers will be informed by Renesas in case of anomalies detected on this version.

4.6.5 Compatibility

The LVD Configuration Software is a porting of the previous PA024 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.6.6 Development environment

The LVD Configuration Software was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD to be used in safety related applications up to SIL3.

The user shall use this development environment for building the LVD Configuration Software.

For detailed configuration to be used for the compiler please see [3].

4.6.7 Installation instructions

Please see [3] for instructions how to install the LVD Configuration Software into the integrated system.

4.7 Assumptions and recommendations for use of Renesas Diagnostic Software

Please see [3] for all safety related conditions of use of the Renesas Diagnostics Software.

4.8 User Expertise

User has to have good expertise on embedded programming of the target MCU. Expertise on assembly programming and C level/assembly interface is necessary.

4.9 Degree of reliance information

4.9.1 Independent assessment

An independent assessment of the Renesas Diagnostics Software including all related documentation and development process with respect to the requirements of IEC61508:2010, targeting max. SIL3 applications, was performed by TÜV Rheinland.

4.9.2 Development of environment safety guidelines

Development of the Renesas Diagnostics Software was following the IAR Embedded Workbench Safety Guide [4].

4.9.3 Verification of Renesas Diagnostic Software

A thorough verification of the Renesas Diagnostics Software was performed. Verification includes:

- Software Requirement Verification
- Static Verification
- Dynamic Verification
- Verification of Software Requirements Coverage

For the dynamic verification the IAR Embedded Workbench was used which enables implementation of efficient software tests. More than 40 test cases were re-executed for dynamic verification.

4.9.4 Further information

The Renesas Diagnostics Software was developed almost completely in assembly language with C-User-Interface. No complex structures are involved and branches/jumps are avoided as much as possible. This is an important factor for avoiding systematic failures in the Renesas Diagnostics Software.

4.10 Change Control

In case any changes to the CPU Software Test, RAM Software Test or ROM Software Test are required to fulfill certain requirements of the system integrator a related change request could be addressed to:

Renesas Electronics Europe GmbH
Industrial & Communications Business Group (ICBG)
Arcadiastrasse 10
40472 Düsseldorf
Germany

5. Appendix A: Product Variants

Table 5.1 lists all product variants that are covered by this safety manual.

Table 5.1 Product variants covered by this Safety Manual

Part Number	Family	Product Group	Product Description	Package
R7FS3A77C2A01CLK	MCU	S3A7	1 MB Code flash, 16 KB Data flash, 192 KB SRAM, -40 to +85°C	PTLG0145KA-A
R7FS3A77C3A01CFB	MCU	S3A7	1 MB Code flash, 16 KB Data flash, 192 KB SRAM, -40 to +105°C	PLQP0144KA-B
R7FS3A77C2A01CBJ	MCU	S3A7	1 MB Code flash, 16 KB Data flash, 192 KB SRAM, -40 to +85°C	PLBG0121JA-A
R7FS3A77C3A01CFP	MCU	S3A7	1 MB Code flash, 16 KB Data flash, 192 KB SRAM, -40 to +105°C	PLQP0100KB-B
R7FS3A77C2A01CLJ	MCU	S3A7	1 MB Code flash, 16 KB Data flash, 192 KB SRAM, -40 to +85°C	PTLG0100JA-A
R7FS3A77C3A01CFM	MCU	S3A7	1 MB Code flash, 16 KB Data flash, 192 KB SRAM, -40 to +105°C	PLQP0064KB-C
R7FS3A77C3A01CNB	MCU	S3A7	1 MB Code flash, 16 KB Data flash, 192 KB SRAM, -40 to +105°C	PWQN0064LA-A
R7FS3A6783A01CFP	MCU	S3A6	256 KB Code flash, 8 KB Data flash, 32 KB SRAM, -40 to +105°C	PLQP0100KB-B
R7FS3A6782A01CLJ	MCU	S3A6	256 KB Code flash, 8 KB Data flash, 32 KB SRAM, -40 to +85°C	PTLG0100JA-A
R7FS3A6783A01CFM	MCU	S3A6	256 KB Code flash, 8 KB Data flash, 32 KB SRAM, -40 to +105°C	PLQP0064KB-C
R7FS3A6783A01CNB	MCU	S3A6	256 KB Code flash, 8 KB Data flash, 32 KB SRAM, -40 to +105°C	PWQN0064LA-A
R7FS3A6783A01CFL	MCU	S3A6	256 KB Code flash, 8 KB Data flash, 32 KB SRAM, -40 to +105°C	PLQP0048KB-B
R7FS3A6783A01CNE	MCU	S3A6	256 KB Code flash, 8 KB Data flash, 32 KB SRAM, -40 to +105°C	PWQN0048KB-A
R7FS3A6783A01CNF	MCU	S3A6	256 KB Code flash, 8 KB Data flash, 32 KB SRAM, -40 to +105°C	PWQN0040KC-A
R7FS3A37A2A01CLK	MCU	S3A3	512 KB Code flash, 8 KB Data flash, 96 KB SRAM, -40 to +85°C	PTLG0145KA-A
R7FS3A37A3A01CFB	MCU	S3A3	512 KB Code flash, 8 KB Data flash, 96 KB SRAM, -40 to +105°C	PLQP0144KA-B
R7FS3A37A2A01CBJ	MCU	S3A3	512 KB Code flash, 8 KB Data flash, 96 KB SRAM, -40 to +85°C	PLBG0121JA-A
R7FS3A37A3A01CFP	MCU	S3A3	512 KB Code flash, 8 KB Data flash, 96 KB SRAM, -40 to +105°C	PLQP0100KB-B
R7FS3A37A2A01CLJ	MCU	S3A3	512 KB Code flash, 8 KB Data flash, 96 KB SRAM, -40 to +85°C	PTLG0100JA-A
R7FS3A37A3A01CFM	MCU	S3A3	512 KB Code flash, 8 KB Data flash, 96 KB SRAM, -40 to +105°C	PLQP0064KB-C
R7FS3A37A3A01CNB	MCU	S3A3	512 KB Code flash, 8 KB Data flash, 96 KB SRAM, -40 to +105°C	PWQN0064LA-A
R7FS3A17C2A01CLK	MCU	S3A1	1MB Code flash, 8 KB Data flash, 192 KB SRAM, -40 to +85°C	PTLG0145KA-A
R7FS3A17C3A01CFB	MCU	S3A1	1MB Code flash, 8 KB Data flash, 192 KB SRAM, -40 to +105°C	PLQP0144KA-B
R7FS3A17C2A01CBJ	MCU	S3A1	1MB Code flash, 8 KB Data flash, 192 KB SRAM, -40 to +85°C	PLBG0121JA-A
R7FS3A17C3A01CFP	MCU	S3A1	1MB Code flash, 8 KB Data flash, 192 KB SRAM, -40 to +105°C	PLQP0100KB-B
R7FS3A17C2A01CLJ	MCU	S3A1	1MB Code flash, 8 KB Data flash, 192 KB SRAM, -40 to +85°C	PTLG0100JA-A
R7FS3A17C3A01CFM	MCU	S3A1	1MB Code flash, 8 KB Data flash, 192 KB SRAM, -40 to +105°C	PLQP0064KB-C
R7FS3A17C3A01CNB	MCU	S3A1	1MB Code flash, 8 KB Data flash, 192 KB SRAM, -40 to +105°C	PWQN0064LA-A

6. References

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2. Cortex - M4 Devices – Generic User guide, 16 December 2010.
3. Synergy Group: Renesas Diagnostics Software User Guide.
4. IAR Embedded Workbench Safety Guide (SafetyEW-1), February 2013, IAR Internal Reference: M13, ISUD.

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
0.1	Dec 16, 2016	-	First version
0.2	Jan 4, 2017	19	Updated References format
0.3	Feb 10, 2017	All	Updated template
0.4	Jun 8, 2017	All	Updated all software versions
			Updated Section title of section 4.7. Added Product variants in Appendix A.
1.0	Jun 9, 2017	-	Internal approval
1.1	Jul 16, 2018	References	Removed revision information from documentation
1.2	Sep 27, 2018	All	Updated the functional safety version of the IAR Embedded Workbench.
		-	Removed “ADC14 Comparator Software” and TSN “Management Software” sections.
		-	Updated latest release of CPU,RAM,ROM,CAC,IWDT and LVD tests.
		All	Replaced “S3A7” Synergy name with “S3”.
		4.9.3	Rephrased a sentence.
		5	Added product variants.

Synergy S3 Series MCU Diagnostic Software Safety User's Manual

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