

Contents

| | |
|--|-----------|
| 1. Internal Memory | 4 |
| 1.1 Block Diagram..... | 4 |
| 1.2 Offset..... | 6 |
| 1.3 Slope..... | 7 |
| 1.3.1. Slope of Transfer Function..... | 7 |
| 1.3.2. Slope example..... | 7 |
| 1.4 Clamping..... | 8 |
| 1.4.1. Clamping Example..... | 9 |
| 1.5 LinInt0..... | 10 |
| 1.5.1. Linear Error Correction..... | 10 |
| 1.6 LinInt1..... | 11 |
| 1.7 LinInt2..... | 12 |
| 1.8 LinInt3..... | 13 |
| 1.9 LinInt4..... | 14 |
| 1.10 Coil Offset..... | 15 |
| 1.11 CalMode..... | 16 |
| 1.11.1. Output Mode..... | 17 |
| 1.11.2. Correction Mode..... | 18 |
| 1.12 Output..... | 19 |
| 1.13 Trimming..... | 22 |
| 1.14 AGC0..... | 23 |
| 1.15 AGC1..... | 24 |
| 1.16 Mask..... | 25 |
| 1.17 Traceability0..... | 27 |
| 1.18 Traceability1..... | 27 |
| 1.19 Misc..... | 27 |
| 1.20 Afe_Agc..... | 28 |
| 1.21 Xsine..... | 28 |
| 1.22 Ycosine..... | 29 |
| 1.23 Angle..... | 29 |
| 1.24 Cordic Magnitude..... | 30 |
| 1.25 SPA..... | 30 |
| 1.26 Pos0..... | 31 |
| 1.27 Pos1..... | 31 |
| 2. Glossary | 32 |
| 3. Revision History | 32 |

List of Figures

| | |
|---|----|
| Figure 1. Internal Memory of the ZMID4200 | 4 |
| Figure 2. Internal Memory of the ZMID4200 | 7 |
| Figure 3. Clamping Example | 9 |
| Figure 4. Linear Error Correction Example | 10 |
| Figure 5. Linear Output Mode Example with Slope = 2, Offset = 90° | 17 |
| Figure 6. Modulus Output Example with Slope = 2, Offset = 60° | 17 |
| Figure 7. Pre-Calibration Process | 18 |
| Figure 8. Post-Calibration Process | 18 |
| Figure 9. Output PWM Diagnostic Level | 20 |
| Figure 10. Output Analog Diagnostic Level | 21 |
| Figure 11. Gain Control | 23 |

List of Tables

| | |
|---|----|
| Table 1. Internal Memory | 4 |
| Table 2. Offset Register Description | 6 |
| Table 3. Offset Register Description Modulo 360 | 6 |
| Table 4. Slope Register Description | 7 |
| Table 5. CLAMP Register Description | 8 |
| Table 6. LinInt0 Register Description | 10 |
| Table 7. LinInt1 Register Description | 11 |
| Table 8. LinInt2 Register Description | 12 |
| Table 9. LinInt3 Register Description | 13 |
| Table 10. LinInt4 Register Description | 14 |
| Table 11. Amplitude Offset Register Description | 15 |
| Table 12. CalMode Register Description | 16 |
| Table 13. Output Register Description | 19 |
| Table 14. Trim0 Register Description | 22 |
| Table 15. AGC0 Register Description | 23 |
| Table 16. AGC0 Register Description | 24 |
| Table 17. Mask Register Description | 25 |
| Table 18. Traceability0 Register Description | 27 |
| Table 19. Traceability1 Register Description | 27 |
| Table 20. Misc Register Description | 27 |
| Table 21. Afe_Agc Register Description | 28 |
| Table 22. Xsine Register Description | 28 |
| Table 23. Ycosine Register Description | 29 |
| Table 24. Angle Register Description | 29 |
| Table 25. Mag Register Description | 30 |
| Table 26. Spa Register Description | 30 |

Table 27. Pos0 Register Description 31
Table 28. Pos1 Register Description 31

1. Internal Memory

1.1 Block Diagram

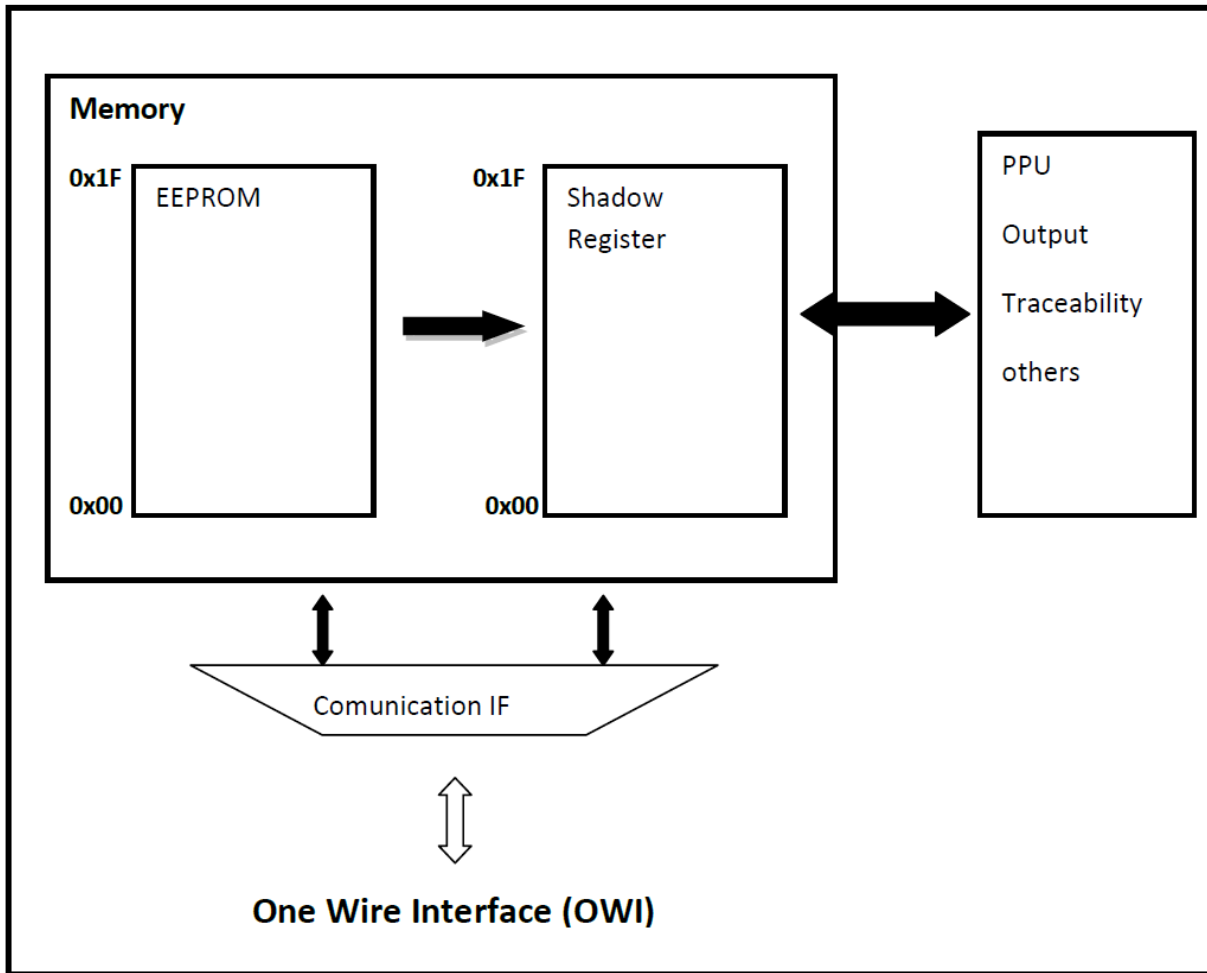


Figure 1. Internal Memory of the ZMID4200

Figure 1 shows the internal memory topology of the ZMID4200 products which is split up into a non-volatile EEPROM (E2P) and a volatile shadow ram (SWR) section. After chip start up the E2P content is copied into the SWR. During IC operation in OWI mode, changes in the SWR will take immediate effect whereas changes in the E2P require an IC power cycle. (Power off/Power on).

Definitions:

0b Binary number prefix.

0x Hexadecimal number prefix.

Table 1. Internal Memory

| Address | Name | Type | Location | Function |
|---------|----------|------|----------|---|
| 0x00 | Offset | R/W | E2P/SWR | 14-bit zero- Zero Angle offset of output signal |
| 0x01 | Slope | R/W | E2P/ SWR | 13-bit slope value of output signal |
| 0x02 | Clamping | R/W | E2P/SWR | Clamp values of output signal |

| Address | Name | Type | Location | Function |
|---------|---------------------|------|----------|---|
| 0x03 | LinInt0 | R/W | E2P/SWR | Linear interpolation of output signal corr1@12.5% (45°) - bit15...8 corr0@0%(0°) - bit7...0 |
| 0x04 | LinInt1 | R/W | E2P/SWR | Linear interpolation of output signal corr3@37.5% (135°) - bit15...8 corr2@25%(90°) - bit7...0 |
| 0x05 | LinInt2 | R/W | E2P/SWR | Linear interpolation of output signal corr5@62.5% (225°) - bit15...8 corr4@50%(180°) - bit7...0 |
| 0x06 | LinInt3 | R/W | E2P/SWR | Linear interpolation of output signal corr7@87.5% (315°) - bit15...8 corr6@75%(270°) - bit7...0 |
| 0x07 | LinInt4 | R/W | E2P/SWR | Linear interpolation of output signal not used - bit15...8 corr8@100%(360°) - bit7...0 |
| 0x08 | Coil offset | R/W | E2P/SWR | Signal Offset correction of the demodulated input signals - sin and cos (r1,r2 - Ycos,Xsin); Only apply if constant input gain setting is activated. |
| 0x09 | CalMode | R/W | E2P/SWR | Calibration mode register contains control bits for output Mode like linear or modulo360 mode sensor; linear correction mode like pre-&post-calibration; Angle offset for linearity correction like 0° or -22.5°; Swap receiver coils polarity |
| 0x0A | Output | R/W | E2P/SWR | Output register is used for configuration of the output SENT CRC, SENT Pause, PWM slope current, PWM freq, Analog diagnostic level. |
| 0x0B | Trimming | R/W | E2P/SWR | This register contains control parameters for: PWM slope time, OSR, LC oscillator current, VDDT voltage calibration |
| 0x0C | AGC0 | R/W | E2P/SWR | Basic configurations of the analog front-end in terms of timing and gain e.g: Automated gain scheduling in number of samples; Integrator gain stage; |
| 0x0D | AGC1 | R/W | E2P/SWR | Configurations of excitation coil frequency limits (alarm setting); CORDIC magnitude limits; Interlink mode (integration time adaption and gain adaption) |
| 0x0E | Mask | R/W | E2P/SWR | Diagnostic mask register is controlling which alarms are generating an output diagnostic flag e.g: Receiver coil1 open/short; Excitation coil break; |
| 0x0F | Trace0 | R/W | E2P | factory traceability code 0 |
| 0x10 | Trace1 | R/W | E2P | factory traceability code 1 |
| 0x11 | Misc | R/W | E2P/SWR | Configuration of voltage regulators and oscillators; e.g. switch off VDDT regulator in case of excitation coil alarm |
| 0x13 | Afe_agc | R | SWR | Analog front-end/ Automatic gain regulation. Polarity of R1 & R2 ADC gain. AGC nr. of integration cycles |
| 0x14 | Xsine | R | SWR | 13-bit Cordic raw input signal |
| 0x15 | Ycosine | R | SWR | 13-bit Cordic raw input signal |
| 0x16 | Angle | R | SWR | 15-bit Cordic output angle (0° to 90°) |
| 0x17 | Cordic Magnitude | R | SWR | 15-bit Cordic output magnitude |
| 0x18 | Spa | R | SWR | Spatial angle 16-bit output angle (0° to 360°) before output calibration and linear error correction. |
| 0x19 | Pos0 | R | SWR | Position0 16-bit output angle (0° to 360°) after output calibration; If linearization done before output calibration this value = Position1; If linearization done after output calibration this value ≠ Position1 |
| 0x1A | Pos1 | R | SWR | Position1 16-bit output angle (0° to 360°) after output calibration and linearization; This value is always affected by |

1.2 Offset

Address of register: 0x00.

Default value: 0x0000.

The offset parameter is used for the calibration of the position transfer function. The notation of the offset parameter depends on the output mode (see 1.12). Two output modes can be selected (modulo360 or linear).

Output mode: Modulo360 (set out_mod = 0b1 (1.10), for selecting the output mode “360Modulo”)

Table 2. Offset Register Description

| Bits | Symbol | Description | | | | | | | | | | | | | | | | | | | | |
|-----------------|----------|--|-----------------|-----------------|--------|---|--------|----|--------|----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|
| Off.15 - Off.14 | Reserved | Not used, read as 0 (SWR). | | | | | | | | | | | | | | | | | | | | |
| Off.13 - Off.0 | Offset | Offset of output transfer function. | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>Offset Value</th> <th>Value in Degree</th> </tr> </thead> <tbody> <tr><td>0x0000</td><td>0</td></tr> <tr><td>0x0800</td><td>45</td></tr> <tr><td>0x1000</td><td>90</td></tr> <tr><td>0x1800</td><td>135</td></tr> <tr><td>0x2000</td><td>180</td></tr> <tr><td>0x2800</td><td>225</td></tr> <tr><td>0x3000</td><td>270</td></tr> <tr><td>0x3800</td><td>315</td></tr> <tr><td>0x3FFF</td><td>360</td></tr> </tbody> </table> | Offset Value | Value in Degree | 0x0000 | 0 | 0x0800 | 45 | 0x1000 | 90 | 0x1800 | 135 | 0x2000 | 180 | 0x2800 | 225 | 0x3000 | 270 | 0x3800 | 315 | 0x3FFF | 360 |
| | | Offset Value | Value in Degree | | | | | | | | | | | | | | | | | | | |
| | | 0x0000 | 0 | | | | | | | | | | | | | | | | | | | |
| | | 0x0800 | 45 | | | | | | | | | | | | | | | | | | | |
| | | 0x1000 | 90 | | | | | | | | | | | | | | | | | | | |
| | | 0x1800 | 135 | | | | | | | | | | | | | | | | | | | |
| | | 0x2000 | 180 | | | | | | | | | | | | | | | | | | | |
| | | 0x2800 | 225 | | | | | | | | | | | | | | | | | | | |
| | | 0x3000 | 270 | | | | | | | | | | | | | | | | | | | |
| | | 0x3800 | 315 | | | | | | | | | | | | | | | | | | | |
| 0x3FFF | 360 | | | | | | | | | | | | | | | | | | | | | |

Note: The reserved bits off.15 & off.14 can be written and read to/from the block E2P. The copy process copies only bits (off.13 down to off.0) to the SWR.

Output mode: Linear (set out_mod = 0b0 (see section 1.11.1), for selecting Linear Output mode).

Table 3. Offset Register Description Modulo 360

| Bits | Symbol | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----------|--|-----------------|-----------------|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|------|--------|------|--------|------|--------|------|--------|-----|--------|---|--------|------|--------|------|--------|------|--------|------|--------|------|--------|-------|--------|-------|
| Off.15 - Off.14 | Reserved | Not used, read as 0 (SWR). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Off.13 - Off.0 | Offset | Offset of output transfer function. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>Offset Value</th> <th>Value in Degree</th> </tr> </thead> <tbody> <tr><td>0x0000</td><td>180</td></tr> <tr><td>0x0400</td><td>360</td></tr> <tr><td>0x0800</td><td>540</td></tr> <tr><td>0x0C00</td><td>720</td></tr> <tr><td>0x1000</td><td>900</td></tr> <tr><td>0x1400</td><td>1080</td></tr> <tr><td>0x1800</td><td>1260</td></tr> <tr><td>0x1C00</td><td>1440</td></tr> <tr><td>0x1FFF</td><td>1620</td></tr> <tr><td>0x2000</td><td>180</td></tr> <tr><td>0x2400</td><td>0</td></tr> <tr><td>0x2800</td><td>-180</td></tr> <tr><td>0x2C00</td><td>-360</td></tr> <tr><td>0x3000</td><td>-540</td></tr> <tr><td>0x3400</td><td>-720</td></tr> <tr><td>0x3800</td><td>-900</td></tr> <tr><td>0x3C00</td><td>-1080</td></tr> <tr><td>0x3FFF</td><td>-1260</td></tr> </tbody> </table> | Offset Value | Value in Degree | 0x0000 | 180 | 0x0400 | 360 | 0x0800 | 540 | 0x0C00 | 720 | 0x1000 | 900 | 0x1400 | 1080 | 0x1800 | 1260 | 0x1C00 | 1440 | 0x1FFF | 1620 | 0x2000 | 180 | 0x2400 | 0 | 0x2800 | -180 | 0x2C00 | -360 | 0x3000 | -540 | 0x3400 | -720 | 0x3800 | -900 | 0x3C00 | -1080 | 0x3FFF | -1260 |
| | | Offset Value | Value in Degree | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x0000 | 180 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x0400 | 360 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x0800 | 540 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x0C00 | 720 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x1000 | 900 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x1400 | 1080 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x1800 | 1260 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x1C00 | 1440 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x1FFF | 1620 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x2000 | 180 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x2400 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x2800 | -180 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x2C00 | -360 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x3000 | -540 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x3400 | -720 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x3800 | -900 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x3C00 | -1080 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0x3FFF | -1260 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note: The reserved bits off.15 & off.14 can be written and read to/from the block E2P. The copy process copies only bits (off.13 down to off.0) to the SWR.

1.3 Slope

Address of register: 0x01.

Default value: 0x0400.

1.3.1. Slope of Transfer Function

The slope parameter is used for the calibration of the position transfer function. It is a multiplication factor for the spatial angle. The slope notation is independent from the out_mode parameter (see section 1.12).

Table 4. Slope Register Description

| Bits | Symbol | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|-----------------|---|--------------|-----------------|--------|-----|--------|------|--------|-----|--------|------|--------|-----|--------|-----|--------|-----|--------|-------|--------|------|--------|-------|--------|-----|--------|------|--------|------|--------|------|--------|------|--------|--------|
| slp.15 - slp.13 | Reserved | Not used, read as 0 (SWR) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| slp.12 - slp.0 | Slope | Slope of output transfer function. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>Offset Value</th> <th>Value in Degree</th> </tr> </thead> <tbody> <tr><td>0x0000</td><td>0.0</td></tr> <tr><td>0x0100</td><td>0.25</td></tr> <tr><td>0x0200</td><td>0.5</td></tr> <tr><td>0x0300</td><td>0.75</td></tr> <tr><td>0x0400</td><td>1.0</td></tr> <tr><td>0x0800</td><td>2.0</td></tr> <tr><td>0x0C00</td><td>3.0</td></tr> <tr><td>0x0FFF</td><td>3.999</td></tr> <tr><td>0x1000</td><td>-0.0</td></tr> <tr><td>0x1100</td><td>-0.25</td></tr> <tr><td>0x1200</td><td>0.5</td></tr> <tr><td>0x1300</td><td>0.75</td></tr> <tr><td>0x1400</td><td>-1.0</td></tr> <tr><td>0x1800</td><td>-2.0</td></tr> <tr><td>0x1C00</td><td>-3.0</td></tr> <tr><td>0x1FFF</td><td>-3.999</td></tr> </tbody> </table> | Offset Value | Value in Degree | 0x0000 | 0.0 | 0x0100 | 0.25 | 0x0200 | 0.5 | 0x0300 | 0.75 | 0x0400 | 1.0 | 0x0800 | 2.0 | 0x0C00 | 3.0 | 0x0FFF | 3.999 | 0x1000 | -0.0 | 0x1100 | -0.25 | 0x1200 | 0.5 | 0x1300 | 0.75 | 0x1400 | -1.0 | 0x1800 | -2.0 | 0x1C00 | -3.0 | 0x1FFF | -3.999 |
| Offset Value | Value in Degree | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0000 | 0.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0100 | 0.25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0200 | 0.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0300 | 0.75 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0400 | 1.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0800 | 2.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0C00 | 3.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0FFF | 3.999 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x1000 | -0.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x1100 | -0.25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x1200 | 0.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x1300 | 0.75 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x1400 | -1.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x1800 | -2.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x1C00 | -3.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x1FFF | -3.999 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note: The reserved bits slp.15, slp.14 and slp.13 can be written and read to/from the block E2P.

1.3.2. Slope example

Slope value coded on 13bits with a range between -4 to +4, 1 bit is the sign and defines the sign of (slope).

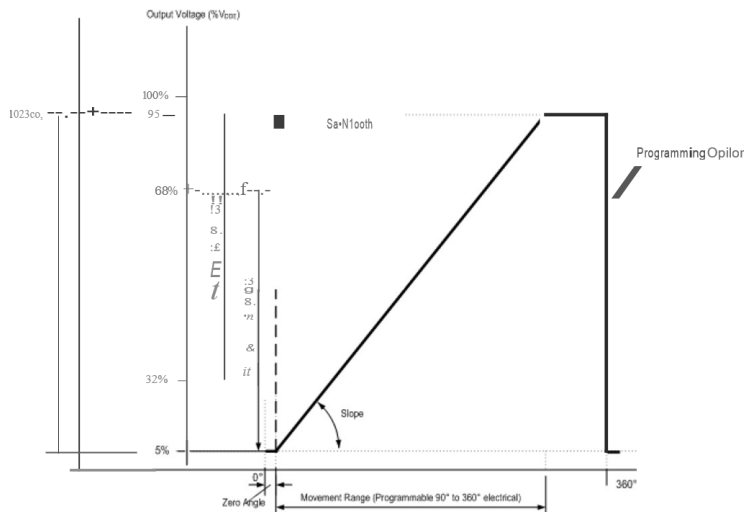


Figure 2. Internal Memory of the ZMID4200

Figure 2 shows the internal memory topology of the ZMID4200 products which is split up into a non-volatile EEPROM (E2P) and a volatile shadow ram (SWR) section. After chip start up the E2P content is copied into the SWR. During IC operation in OWI mode, changes in the SWR will take immediate effect whereas changes in the E2P require an IC power cycle. (Power off/Power on).

1.4 Clamping

Address of register: 0x02.

Default value: 0x0000.

The clamping parameters clamp_low and clamp_high are located in the clamp memory. These two parameters are used for position calibration if the output protocol mode is for ZMID4200. For the Analog output mode the complete 100% position range is mapped to a voltage range from 250mV to 4750mV. The stepping rate of the clamping parameters is 1%, so that the analog voltage stepping rate is 47.5 mV / 1 %. The diagnostic low level is less or equal 200mV, the high level is higher or equal 4800mV.

For the PWM output mode the position range is mapped to the Pulse Pause Ratio (PPR) of a periodic analog output signal. 100% position range is mapped to the PPR-range from 5% to 95%. So a clamping step of 1% is mapped to a PPR change of 0.9% (e.g. clamp_low = 10% & pos <= clamp_low --> PPR = 5% + 9%). The diagnostic low level is mapped to 2.5% PPR, the high level is mapped to 97.5% PPR.

Table 5. CLAMP Register Description

| Bits | Symbol | Description | |
|-----------------------|------------|---|-----------------|
| clamp. 15 - clamp. 14 | Reserved | Not used, read as 0 (SWR) | |
| clamp. 13 - clamp. 8 | clamp_high | Position output clamp high descend from 4750 mV (Analog) resp. 95% (PWM). | |
| | | clamp_high (CLAMP13 - CLAMP08) | Rate (%) |
| | | 0x00 | 0 |
| | | 0x01 | 1 |
| | | 0x02 | 2 |
| | | | |
| | | | |
| | | | |
| | | | |
| | | 0x3F | 63 |
| clamp. 7 - clamp.6 | Reserved | Not used, read as 0 (SWR) | |
| clamp. 5 - clamp. 0 | clamp_low | Position output clamp low rising from 250mV (Analog) resp. 5% (PWM) | |
| | | clamp_low (CLAMP5 - CLAMP00) | Rate (%) |
| | | 0x00 | 0 |
| | | 0x01 | 1 |
| | | 0x02 | 2 |
| | | | |
| | | | |
| | | | |
| | | | |
| | | 0x3F | 63 |

Note: The reserved bits clamp.15, clamp.14, clamp.7 and clamp.6 can be written and read to/from the block E2P. The copy process copies only bits (clamp.13 down to clamp.8) and (clamp.5 down to clamp.0) to the SWR.

1.4.1. Clamping Example

Clamps (applicable for Analog and PWM Output, not for SENT).

Clamp_low (6 bits): min value is 5%, steps of 1% from minimum value. Max Clamp_low value is: 68%.

Clamp_high (6 bits): max value is 95%, steps of -1% from max value. Min Clamp_high value is: 32%.

In the below example the clamping levels are 5% and 95%.

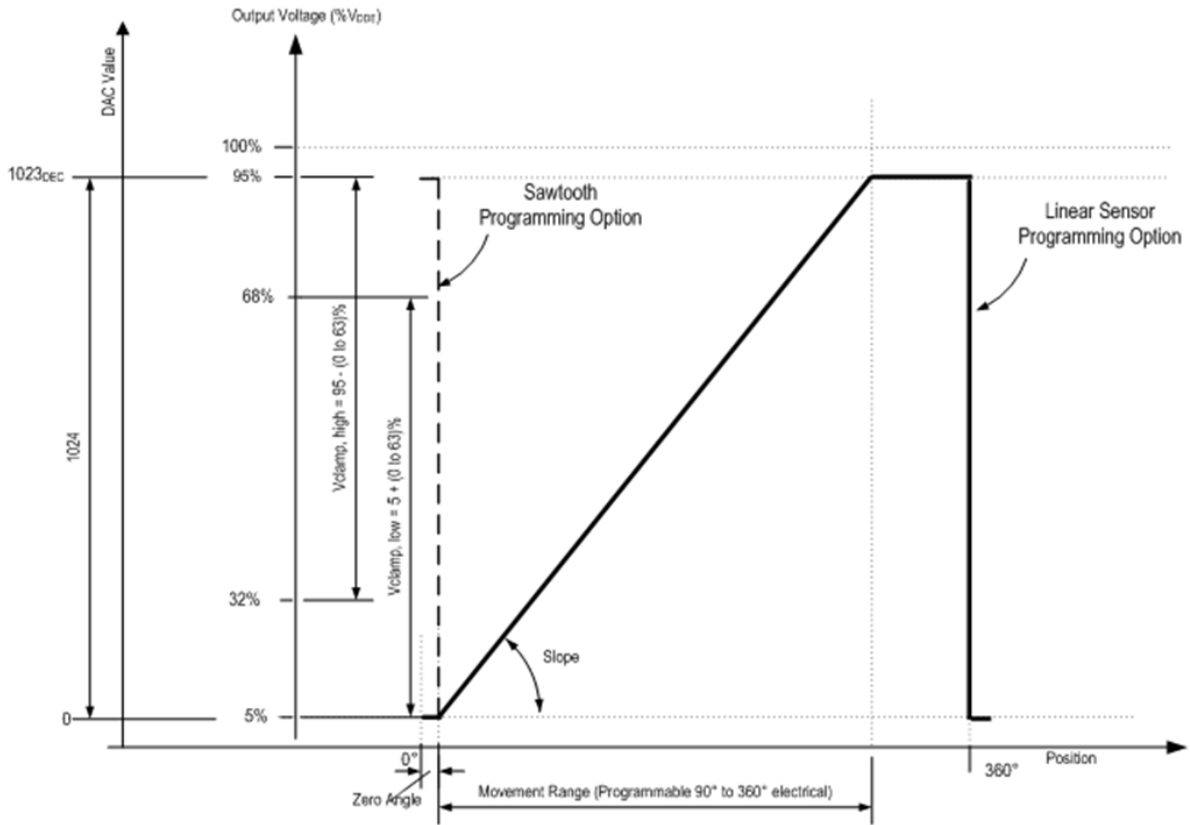


Figure 3. Clamping Example

1.5 LinInt0

Address of register: 0x03.

Default value: 0x0000.

The linearity of the position transfer function can be modified by a 9-point correction curve over the whole position range. The correction curve is defined by 9 points: corr0....corr8. The correction factor can be calculated by a linear interpolation over the 9 corresponding points. The correction factor is applied on the 11 most significant position bits.

Table 6. LinInt0 Register Description

| Bits | Symbol | Description | |
|------------------------|--------|--|--------------------------|
| linint0.15 - linint0.8 | corr1 | Correction factor 1 for position 12.5% (45 deg). | |
| | | Corr0 (linint7 - linint0) | Correction Factor |
| | | 0x00 | 0 |
| | | 0x01 | 1 |
| | | | |
| | | | |
| | | | |
| | | 0x7F | 127 |
| | | 0x10 | -0 |
| | | 0x11 | -1 |
| | | | |
| | | | |
| | | | |
| 0xFF | -127 | | |
| Linint0.7 - linint0.0 | corr0 | Correction factor 0 for position 0% (0 deg) | |
| | | Corr0 (linint7 - linint0) | Correction Factor |
| | | 0x00 | 0 |
| | | 0x01 | 1 |
| | | | |
| | | | |
| | | | |
| | | 0x7F | 127 |
| | | 0x10 | -0 |
| | | 0x11 | -1 |
| | | | |
| | | | |
| | | | |
| 0xFF | -127 | | |

Note: The notation of the correction factor is sign & abs. with a range of +127...+0.....-127.

1.5.1. Linear Error Correction

The linear error correction function has 9 equidistant fixed correction points (one dimensional). Between each pair of grid points a linear interpolation function evaluates the correction factor.

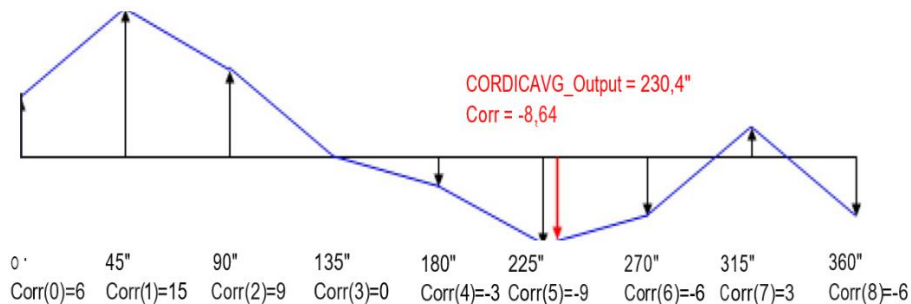


Figure 4. Linear Error Correction Example

1.6 LinInt1

Address of register: 0x04.

Default value: 0x0000.

The linearity of the position transfer function can be modified by a correction curve over the whole position range. The correction curve is defined by 9 points: corr0....corr8. The correction factor can be calculated by a linear interpolation over the 9 corresponding points. The correction factor is applied on the 11 most significant position bits.

Table 7. LinInt1 Register Description

| Bits | Symbol | Description | |
|------------------------|--------|---|--------------------------|
| Linint1.15 - linint1.8 | Corr3 | Correction factor 3 for position 37.5% (135 deg). | |
| | | Corr3 (linint15 - linint8) | Correction Factor |
| | | 0x00 | 0 |
| | | 0x01 | 1 |
| | | | |
| | | | |
| | | | |
| | | 0x7F | 127 |
| | | 0x10 | -0 |
| | | 0x11 | -1 |
| | | | |
| | | | |
| | | | |
| | | 0xFF | -127 |
| Linint1.7 - linint1.0 | Corr2 | Correction factor 2 for position 25% (90 deg). | |
| | | Corr2 (linint7 - linint0) | Correction Factor |
| | | 0x00 | 0 |
| | | 0x01 | 1 |
| | | | |
| | | | |
| | | | |
| | | 0x7F | 127 |
| | | 0x10 | -0 |
| | | 0x11 | -1 |
| | | | |
| | | | |
| | | | |
| | | 0xFF | -127 |

Note: The notation of the correction factor is sign & abs. with a range of +127...+ 0.....-127.

1.7 LinInt2

Address of register: 0x05.

Default value: 0x0000.

The linearity of the position transfer function can be modified by a correction curve over the whole position range. The correction curve is defined by 9 points: corr0....corr8. The correction factor can be calculated by a linear interpolation over the 9 corresponding points. The correction factor is applied on the 11 most significant position bits.

Table 8. LinInt2 Register Description

| Bits | Symbol | Description | | |
|------------------------|--------|---|------|--------------------------|
| Linint2.15 - linint2.8 | Corr5 | Correction factor 5 for position 62.5% (225 deg). | | |
| | | Corr5 (linint15 - linint8) | | Correction Factor |
| | | 0x00 | 0 | |
| | | 0x01 | 1 | |
| | | | | |
| | | | | |
| | | | | |
| | | 0x7F | 127 | |
| | | 0x10 | -0 | |
| | | 0x11 | ... | |
| | | | | |
| | | | | |
| | | | | |
| 0xFF | -127 | | | |
| Linint2.7 - linint2.0 | Corr4 | Correction factor 4 for position 50% (180 deg). | | |
| | | Corr4 (linint7 - linint0) | | Correction Factor |
| | | 0x00 | 0 | |
| | | 0x01 | 1 | |
| | | | | |
| | | | | |
| | | | | |
| | | 0x7F | 127 | |
| | | 0x10 | -0 | |
| | | 0x11 | ... | |
| | | | | |
| | | | | |
| | | | | |
| 0xFF | -127 | | | |

Note: The notation of the correction factor is sign & abs. with a range of +127 ... +- 0.....-127.

1.8 LinInt3

Address of register: 0x06.

Default value: 0x0000.

The linearity of the position transfer function can be modified by a correction curve over the whole position range. The correction curve is defined by 9 points: corr0....corr8. The correction factor can be calculated by a linear interpolation over the 9 corresponding points. The correction factor is applied on the 11 most significant position bits.

Table 9. LinInt3 Register Description

| Bits | Symbol | Description | |
|------------------------|--------|--|--------------------------|
| Linint3.15 - linint3.8 | Corr7 | Correction factor 7 for position 87.5% (315deg). | |
| | | Corr7 (linint3.15 - linint3.8) | Correction Factor |
| | | 0x00 | 0 |
| | | 0x01 | 1 |
| | | | |
| | | | |
| | | | |
| | | 0x7F | 127 |
| | | 0x10 | -0 |
| | | 0x11 | -1 |
| | | | |
| | | | |
| | | | |
| | | 0xFF | -127 |
| Linint3.7 - linint3.0 | Corr6 | Correction factor 6 for position 75% (270deg). | |
| | | Corr6 (linint3.7 - linint3.0) | Correction Factor |
| | | 0x00 | 0 |
| | | 0x01 | 1 |
| | | | |
| | | | |
| | | | |
| | | 0x7F | 127 |
| | | 0x10 | -0 |
| | | 0x11 | -1 |
| | | | |
| | | | |
| | | | |
| | | 0xFF | -127 |

Note: The notation of the correction factor is sign & abs. with a range of +127 ... +- 0..... -127.

1.9 LinInt4

Address of register: 0x07.

Default value: 0x0000.

The linearity of the position transfer function can be modified by a correction curve over the whole position range. The correction curve is defined by 9 points: corr0....corr8. The correction factor can be calculated by a linear interpolation over the 9 corresponding points. The correction factor is applied on the 11 most significant position bits.

Table 10. LinInt4 Register Description

| Bits | Symbol | Description | |
|------------------------|----------|--|--------------------------|
| Linint4.15 - linint4.8 | Reserved | Not used, read as 0 (SWR) | |
| Linint4.7 - linint4.0 | Corr8 | Correction factor 8 for position 100% (360deg) | |
| | | Corr8 (linint4.15 - linint4.8) | Correction Factor |
| | | 0x00 | 0 |
| | | 0x01 | 1 |
| | | | |
| | | | |
| | | | |
| | | 0x7F | 127 |
| | | 0x10 | -0 |
| | | 0x11 | -1 |
| | | | |
| | | | |
| | | | |
| 0xFF | -127 | | |

Note: The notation of the correction factor is sign & abs. with a range of +127 ...+0.....-127.

1.10 Coil Offset

Address of register: 0x08.

Default value: 0x0000.

The defined register offset values are added/ subtracted to/from the amplitude values (13-bit) of the receiver coil R2 and coil R1 values. When using the signal offset compensation the automated gain control (AGC1) must be switched off. (agc_mode = 0b00 => Automatic gain OFF, integration time adaption OFF).

Table 11. Amplitude Offset Register Description

| Bits | Symbol | Description | | |
|----------------|-----------|--|------------------------------|------------------------------------|
| amp.15 | mult_r1 | Multiplication factor for amplitude offset_r1 | | |
| | | mult_r1 (amp.15) | Multiplication Factor | |
| | | 0b0 | 2 | |
| | | 0b1 | 4 | |
| amp.14 - amp.8 | offset_r1 | Offset value which is added/subtracted to/from receiver coil R1 amplitude | | |
| | | mult_r1 | offset_r1 | Correction Factor (Decimal) |
| | | 0b0 | 0b0111111 | Ycosine + 126 |
| | | | 0b0000000 | Ycosine + 0 |
| | | | 0b1000000 | Ycosine - 0 |
| | | | 0b1111111 | Ycosine - 126 |
| | | 0b1 | 0b0111111 | Ycosine + 252 |
| | | | 0b0000000 | Ycosine + 0 |
| | | | 0b1000000 | Ycosine - 0 |
| | | | 0b1111111 | Ycosine - 252 |
| amp.7 | mult_r2 | Multiplication factor for offset_r2 | | |
| | | mult_r2 (amp.7) | Multiplication Factor | |
| | | 0b0 | 2 | |
| | | 0b1 | 4 | |
| amp.6 - amp.0 | offset_r2 | Offset value which is added/subtracted to/from receiver coil R2 amplitude. | | |
| | | mult_r2 | offset_r2 | Correction Factor (Decimal) |
| | | 0b0 | 0b0111111 | Xsine + 126 |
| | | | 0b0000000 | Xsine + 0 |
| | | | 0b1000000 | Xsine - 0 |
| | | | 0b1111111 | Xsine - 126 |
| | | 0b1 | 0b0111111 | Xsine + 252 |
| | | | 0b0000000 | Xsine + 0 |
| | | | 0b1000000 | Xsine - 0 |
| | | | 0b1111111 | Xsine - 252 |

Note: abs (Xsine + offset_r2) exceeds max.value of 0x1FFF → amplitude DSP overflow alarm is asserted.

1.11 CalMode

Address of register: 0x09.

Default value: 0x0000.

The calibration mode register contains some control bits which configure the calibration mode and evaluation of the correction curve.

Table 12. CalMode Register Description

| Bits | Symbol | Description | |
|-----------------------|--|--|---|
| calmod.15 - calmod.13 | Reserved | Not used, read as 0 (SWR) | |
| calmod.12 | out_mod | Output Mode | |
| | | Out_mod | Output Mode |
| | | 0b0 | Linear |
| 0b1 | Modulo360 | | |
| calmod.11 – calmod.9 | Reserved | Not used, read as 0 (SWR) | |
| calmod.8 | corr_mod | Correction Mode. Defines how the correction curve has to be applied to correct the linearity of the output transfer function. | |
| | | Corr_mod | Correction Mode |
| | | 0b0 | Linear error correction pre-calibration |
| 0b1 | Linear error correction post-calibration | | |
| calmod.7 – calmod.5 | Reserved | Not used, read as 0 (SWR) | |
| calmod.4 | angle_offset | Linearization angle offset. If (angle_offset) = 1, -22,5° offset is added to the CORDIC calculation only in the case of an Interpolation correction before the Slope calibration (Corr_MOD) = 0 | |
| | | Angle_offset | Angle Offset in Degree |
| | | 0b0 | 0 |
| 0b1 | -22.5 | | |
| calmod.3 | swap_rc_pol | Testing bits for Renesas | |
| calmod.2 | swap_rc_amp | Testing bits for Renesas | |
| calmod.1 | invppr2 | Testing bits for Renesas | |
| calmod.0 | invppr1 | Testing bits for Renesas | |

1.11.1. Output Mode

Linear (Out_Mod = 0): Linear Output Mode is a non-repeating output mode in which the sensor output signal is clamped at the mechanical end points with a range of $-1260^{\circ} \dots + 1620^{\circ}$.

Modulo 360 (Out_Mod = 1): The Modulo 360 Output (Sawtooth Output) Mode is a repeating output mode in which the sensor output signal is not clamped at the mechanical end points, but is switched back to its origin with a range between 0° to 360° .

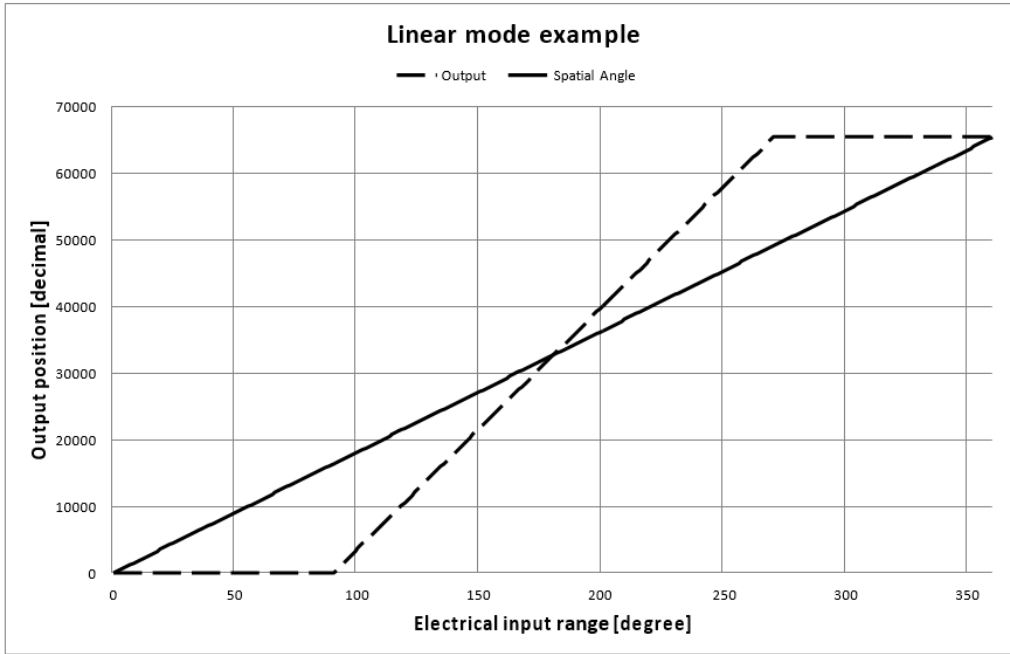


Figure 5. Linear Output Mode Example with Slope = 2, Offset = 90°

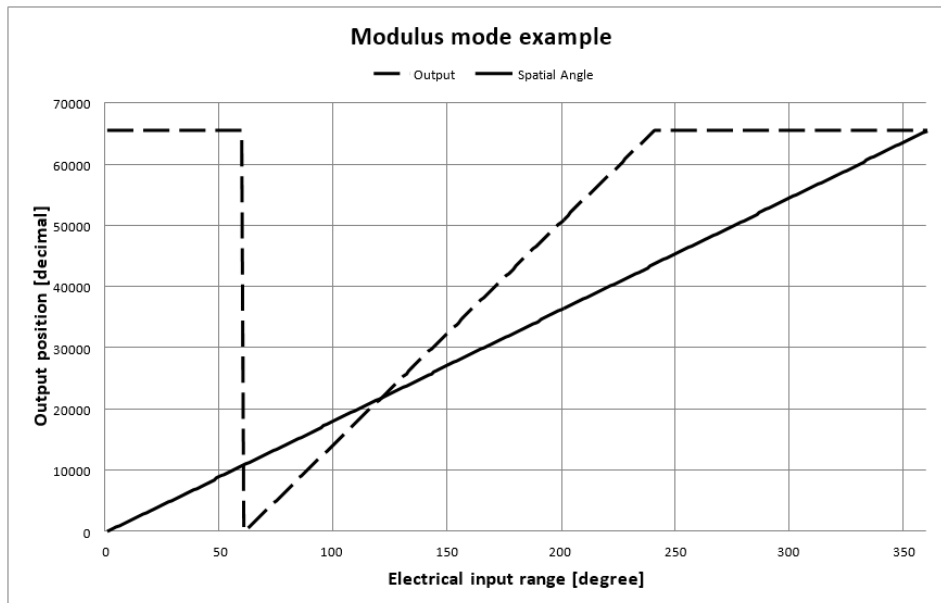


Figure 6. Modulus Output Example with Slope = 2, Offset = 60°

1.11.2. Correction Mode

Pre Calibration; if (Corr_MOD) = 0 then linearity correction is done before "Slope & Offset".

The pre-calibration should be used if the electric input covers a range of a 360°. Using pre-calibration is an advantage when slope and offset needs to be changed after linearization.

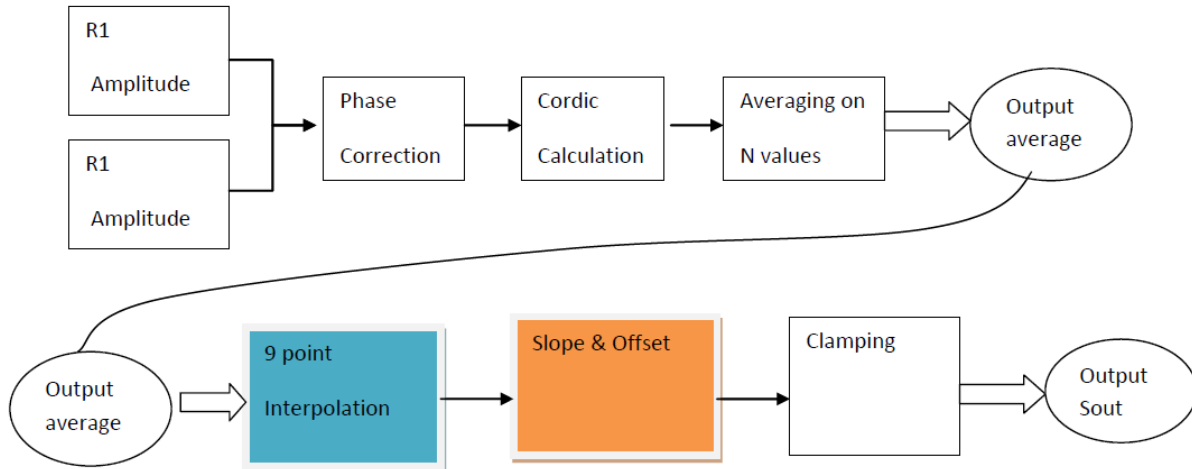


Figure 7. Pre-Calibration Process

Post Calibration; if (Corr_MOD) = 1 then linearity correction is done after " Slope & Offset ". The post-calibration should be the default standard type of calibration.

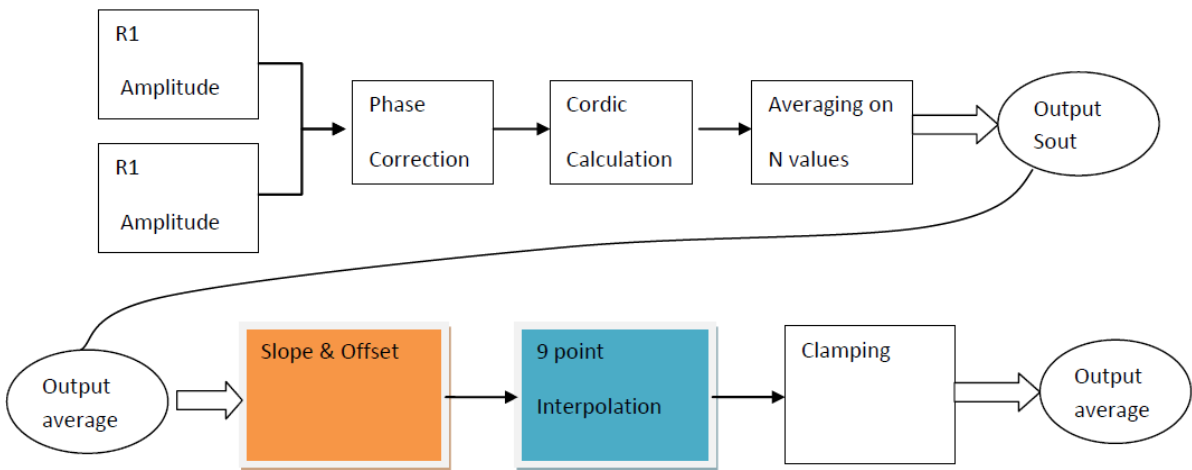


Figure 8. Post-Calibration Process

Note: The reserved bits can be written and read to/from the block E2P. The copy process copies only bits (calmod.12, calmod.8, calmod.4, calout1 and calmod.0) to the SWR.

Note: Individual swapping of receiver polarity & amplitude is only for testing purpose. For application mode both control bits have to be set 0b1 respectively 0b0.

1.12 Output

Address of register: 0x0A Default value: 0x0802

The output register configuration.

Table 13. Output Register Description

| Bits | Symbol | Description | | | | | | | | | | | | | | | | | | |
|----------------------|---|---|----------------|--------------------|-------|--|-------|---|-------|------|-------|------|-------|-----|-------|-----|-------|-----|-------|-----|
| output.15 | Reserved | Not used, read as 0 (SWR) | | | | | | | | | | | | | | | | | | |
| output.14 | sent_crc | <p>Only for SENT output SENT CRC The SENT CRC bit switched between CRC calculation according Legacy implementation of SAE J 2716.</p> <table border="1"> <thead> <tr> <th>SENT CRC</th> <th>CRC Calculation</th> </tr> </thead> <tbody> <tr> <td>0b0</td> <td>CRC calculation according rev. Feb 2008</td> </tr> <tr> <td>0b1</td> <td>CRC calculation according SAE J 2716, Rev 3</td> </tr> </tbody> </table> | SENT CRC | CRC Calculation | 0b0 | CRC calculation according rev. Feb 2008 | 0b1 | CRC calculation according SAE J 2716, Rev 3 | | | | | | | | | | | | |
| SENT CRC | CRC Calculation | | | | | | | | | | | | | | | | | | | |
| 0b0 | CRC calculation according rev. Feb 2008 | | | | | | | | | | | | | | | | | | | |
| 0b1 | CRC calculation according SAE J 2716, Rev 3 | | | | | | | | | | | | | | | | | | | |
| output.13 | sent_pause | <p>Only for SENT output SENT Pause The sent pause bit switches between a constant SENT frame length according SAE J 2716 rev3 by including a pause pulse and a variable SENR frame length according rev2.</p> <table border="1"> <thead> <tr> <th>Sent pause</th> <th>Frame Length</th> </tr> </thead> <tbody> <tr> <td>0b0</td> <td>SENT frame according to SAE J 2716 Rev.2</td> </tr> <tr> <td>0b1</td> <td>SENT frame length according SAE J 2716, Rev3.</td> </tr> </tbody> </table> | Sent pause | Frame Length | 0b0 | SENT frame according to SAE J 2716 Rev.2 | 0b1 | SENT frame length according SAE J 2716, Rev3. | | | | | | | | | | | | |
| Sent pause | Frame Length | | | | | | | | | | | | | | | | | | | |
| 0b0 | SENT frame according to SAE J 2716 Rev.2 | | | | | | | | | | | | | | | | | | | |
| 0b1 | SENT frame length according SAE J 2716, Rev3. | | | | | | | | | | | | | | | | | | | |
| output.12 | sent_ssn | <p>Only for SENT output: SENT SSN The sensor payload is transferred by the 3 data nibbles of signal1. The payload structure of signal2 depends on the SENT single secure nibble bit.</p> <table border="1"> <thead> <tr> <th>SENT SSN</th> <th>Frame Length</th> </tr> </thead> <tbody> <tr> <td>0b0</td> <td>nibble #4, #5, #6 set to zero</td> </tr> <tr> <td>0b1</td> <td>nibble #4 & nibble #5 = value of 8-bit rolling counter with rollover back to zero.nibble #6 = inverted copy of nibble #1.</td> </tr> </tbody> </table> | SENT SSN | Frame Length | 0b0 | nibble #4, #5, #6 set to zero | 0b1 | nibble #4 & nibble #5 = value of 8-bit rolling counter with rollover back to zero.nibble #6 = inverted copy of nibble #1. | | | | | | | | | | | | |
| SENT SSN | Frame Length | | | | | | | | | | | | | | | | | | | |
| 0b0 | nibble #4, #5, #6 set to zero | | | | | | | | | | | | | | | | | | | |
| 0b1 | nibble #4 & nibble #5 = value of 8-bit rolling counter with rollover back to zero.nibble #6 = inverted copy of nibble #1. | | | | | | | | | | | | | | | | | | | |
| output.11 - output.8 | pwm_slope_curr | <p>Only for PWM output PWM slope current The fall time of the PWM output signal is controlled by several current sources related to a master current source. The current of the master source can be programmed.</p> <table border="1"> <thead> <tr> <th>Pwm_slope_curr</th> <th>PWM Slope Current</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Minimum</td> </tr> <tr> <td>0xF</td> <td>Maximum</td> </tr> </tbody> </table> | Pwm_slope_curr | PWM Slope Current | 0x0 | Minimum | 0xF | Maximum | | | | | | | | | | | | |
| Pwm_slope_curr | PWM Slope Current | | | | | | | | | | | | | | | | | | | |
| 0x0 | Minimum | | | | | | | | | | | | | | | | | | | |
| 0xF | Maximum | | | | | | | | | | | | | | | | | | | |
| output.7 | Reserved | Not used, read as 0 (SWR) | | | | | | | | | | | | | | | | | | |
| output.6 - output.4 | pwm_freq | <p>Only for PWM output PWM frequency</p> <table border="1"> <thead> <tr> <th>Pwm_freq</th> <th>PWM Frequency (Hz)</th> </tr> </thead> <tbody> <tr> <td>0b000</td> <td>2023</td> </tr> <tr> <td>0b001</td> <td>1517</td> </tr> <tr> <td>0b010</td> <td>1214</td> </tr> <tr> <td>0b011</td> <td>1011</td> </tr> <tr> <td>0b100</td> <td>758</td> </tr> <tr> <td>0b101</td> <td>506</td> </tr> <tr> <td>0b110</td> <td>253</td> </tr> <tr> <td>0b111</td> <td>126</td> </tr> </tbody> </table> | Pwm_freq | PWM Frequency (Hz) | 0b000 | 2023 | 0b001 | 1517 | 0b010 | 1214 | 0b011 | 1011 | 0b100 | 758 | 0b101 | 506 | 0b110 | 253 | 0b111 | 126 |
| Pwm_freq | PWM Frequency (Hz) | | | | | | | | | | | | | | | | | | | |
| 0b000 | 2023 | | | | | | | | | | | | | | | | | | | |
| 0b001 | 1517 | | | | | | | | | | | | | | | | | | | |
| 0b010 | 1214 | | | | | | | | | | | | | | | | | | | |
| 0b011 | 1011 | | | | | | | | | | | | | | | | | | | |
| 0b100 | 758 | | | | | | | | | | | | | | | | | | | |
| 0b101 | 506 | | | | | | | | | | | | | | | | | | | |
| 0b110 | 253 | | | | | | | | | | | | | | | | | | | |
| 0b111 | 126 | | | | | | | | | | | | | | | | | | | |
| output.3 | pwm_diag | <p>Only for PWM output PWM diagnostic level The output protocol PWM allows two PPR for the diagnostic flag: diagnostic low & diagnostic high. Bit output.3 allows to select one of the two levels if diagnostic alarm is asserted.</p> | | | | | | | | | | | | | | | | | | |
| output.2 | ana_diag | <p>Only for Analog output ANALOG diagnostic level The output protocol ANALOG allows two voltage ranges for the diagnostic flag: diagnostic low & diagnostic high. bit output.2 allows to select one of the two levels if diagnostic alarm is asserted.</p> | | | | | | | | | | | | | | | | | | |

| Bits | Symbol | Description | | | | | | | | | | |
|--------------------|---------------------------------|---|---------|---------|------|-----|------|-----|------|---------------------------------|------|------|
| output.1- output.0 | out_pro | Output interface: These bits are used to configure the output interface. The default output is analog. | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>out_pro</th> <th>Outputs</th> </tr> </thead> <tbody> <tr> <td>0b00</td> <td>OWI</td> </tr> <tr> <td>0b01</td> <td>PWM</td> </tr> <tr> <td>0b10</td> <td>Analog output voltage (default)</td> </tr> <tr> <td>0b11</td> <td>SENT</td> </tr> </tbody> </table> | out_pro | Outputs | 0b00 | OWI | 0b01 | PWM | 0b10 | Analog output voltage (default) | 0b11 | SENT |
| out_pro | Outputs | | | | | | | | | | | |
| 0b00 | OWI | | | | | | | | | | | |
| 0b01 | PWM | | | | | | | | | | | |
| 0b10 | Analog output voltage (default) | | | | | | | | | | | |
| 0b11 | SENT | | | | | | | | | | | |

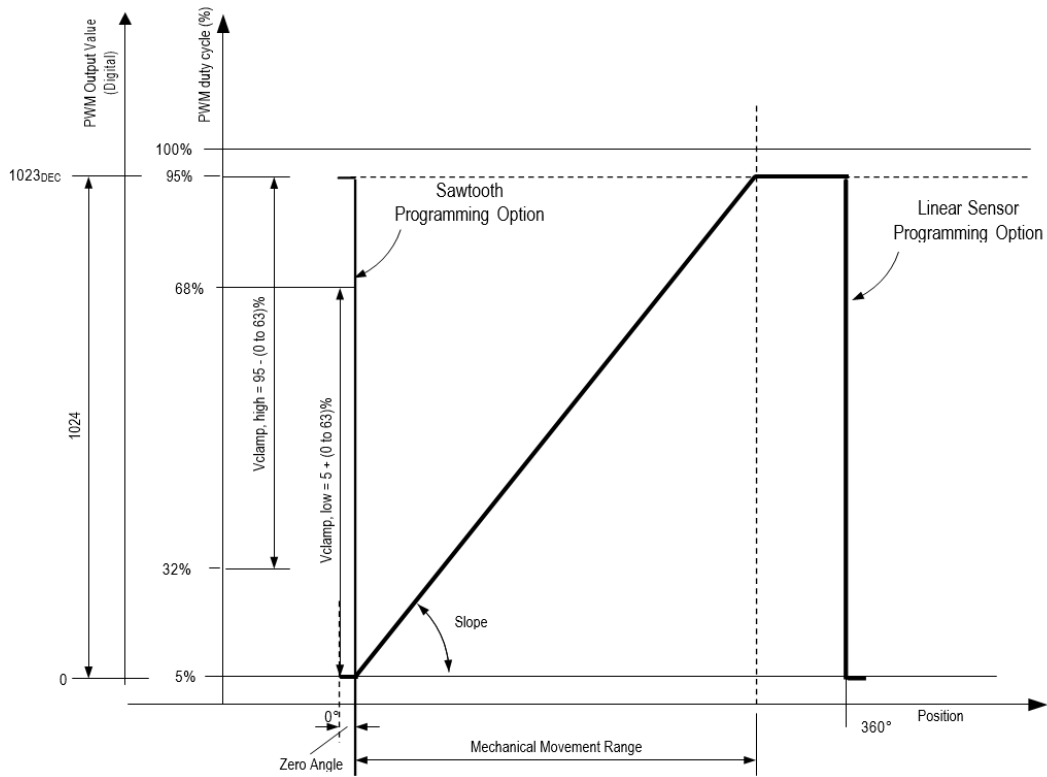


Figure 9. Output PWM Diagnostic Level

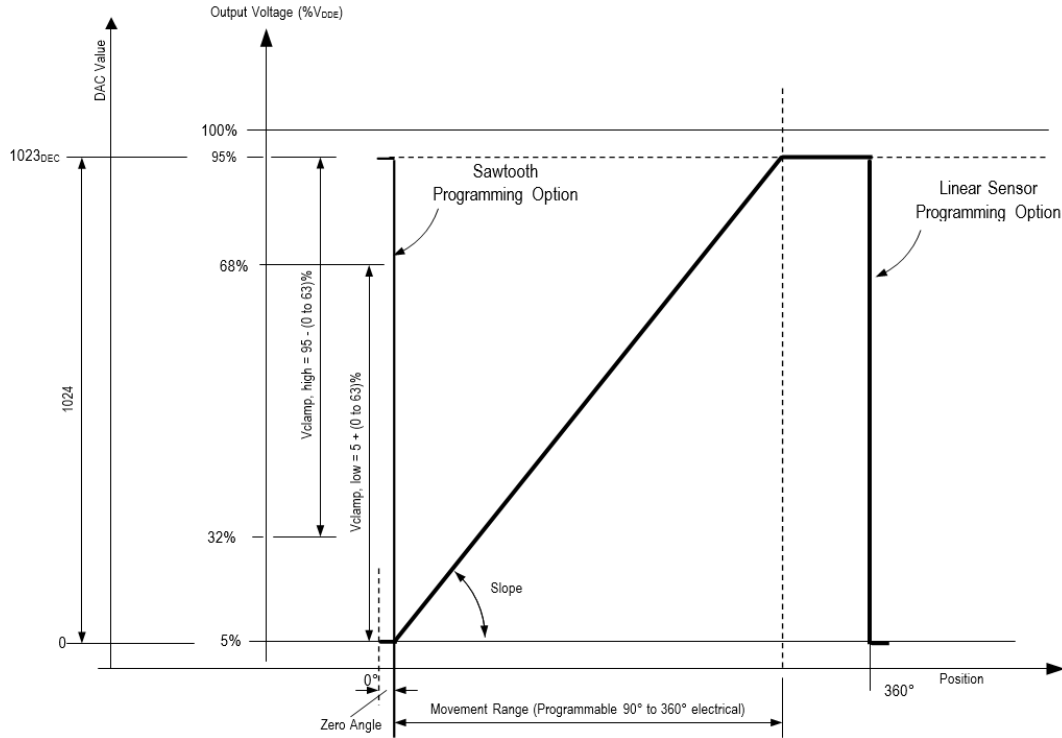


Figure 10. Output Analog Diagnostic Level

Note: The reserved bits can be written and read to/from the block E2P. The copy process copies only defined bits to the SWR.

Note: PWM & SENT timing parameters are based on the ZMID4200 internal oscillator period. To fulfill the electrical specification the oscillator has to be calibrated to 16MHz (see 1.14).

1.13 Trimming

Address of register: 0x0B Default value: 0x8107

Trimming and OSR

The Trimming parameters controls the I_c current and the v_{ddt} voltage regulator. The OSR parameter defines the decimation of ADC samples for calculating the position processing update rate.

Table 14. Trim0 Register Description

| Bits | Symbol | Description | | | | | | | | | | |
|---------------------|---------------------------|--|--------|---------------------------|----------|------------|----------|-------------|------|----|------|----|
| trim0.15 - trim0.14 | pwm_slope_time | <p>PWM slope time</p> <p>The fall time of the PWM output signal is controlled by current sources. The current sources are switched on in 5 consecutive steps. The time between the steps is defined by the pwm_slope_time parameter.</p> <p>pwm_slope_time= 0b00. 435ns / step pwm_slope_time= 0b01.580ns / step</p> | | | | | | | | | | |
| trim0.13 - trim0.12 | osr | <p>Oversampling Rate</p> <p>The oversampling rate defines the number of samples per receive channel which are accumulated and used for the PPU.</p> <table border="1"> <thead> <tr> <th>OSR</th> <th>Samples/Channel</th> </tr> </thead> <tbody> <tr> <td>0b00</td> <td>4</td> </tr> <tr> <td>0b01</td> <td>8</td> </tr> <tr> <td>0b10</td> <td>16</td> </tr> <tr> <td>0b11</td> <td>32</td> </tr> </tbody> </table> | OSR | Samples/Channel | 0b00 | 4 | 0b01 | 8 | 0b10 | 16 | 0b11 | 32 |
| OSR | Samples/Channel | | | | | | | | | | | |
| 0b00 | 4 | | | | | | | | | | | |
| 0b01 | 8 | | | | | | | | | | | |
| 0b10 | 16 | | | | | | | | | | | |
| 0b11 | 32 | | | | | | | | | | | |
| trim0.11 - trim0.9 | Reserved | Not used, read as 0 (SWR) | | | | | | | | | | |
| trim0.8 - trim0.4 | lc_cal | <p>LC Oscillator Calibration (excitation coil)</p> <table border="1"> <thead> <tr> <th>lc_cal</th> <th>Current (Excitation Coil)</th> </tr> </thead> <tbody> <tr> <td>0b0.0000</td> <td>Min (0 mA)</td> </tr> <tr> <td>0b1.1111</td> <td>Max (15 mA)</td> </tr> </tbody> </table> | lc_cal | Current (Excitation Coil) | 0b0.0000 | Min (0 mA) | 0b1.1111 | Max (15 mA) | | | | |
| lc_cal | Current (Excitation Coil) | | | | | | | | | | | |
| 0b0.0000 | Min (0 mA) | | | | | | | | | | | |
| 0b1.1111 | Max (15 mA) | | | | | | | | | | | |
| trim0.3 | Reserved | Not used, read as 0 (SWR) | | | | | | | | | | |
| trim0.2 - trim0.0 | vddt_trim | Renesas internal parameter for testing | | | | | | | | | | |

1.14 AGC0

Address of register: 0x0C Default value: 0x0836

Basic configurations of the analog front end (R1/2 input receive path) gain regulation are controlled by the AGC register. The incoming time division multiplexed signals are amplified by the integrator and the S&H circuit (Figure 6). Both parameters 'ext' and 'gain' will modify the amplification factor of the sampled signals.

The parameter 'smp_cycle' is a 'timing-factor' in number of sample periods for the adaptive gain regulation to determine the point time for gain / integration time setting. A change of the smp_cycle parameter should only be done in dependency of the OSR parameter.

Parameter smp_cycle zero indexed: smp_cycle = 0 .1st sample. smp_cycle = 1 .2nd sample.

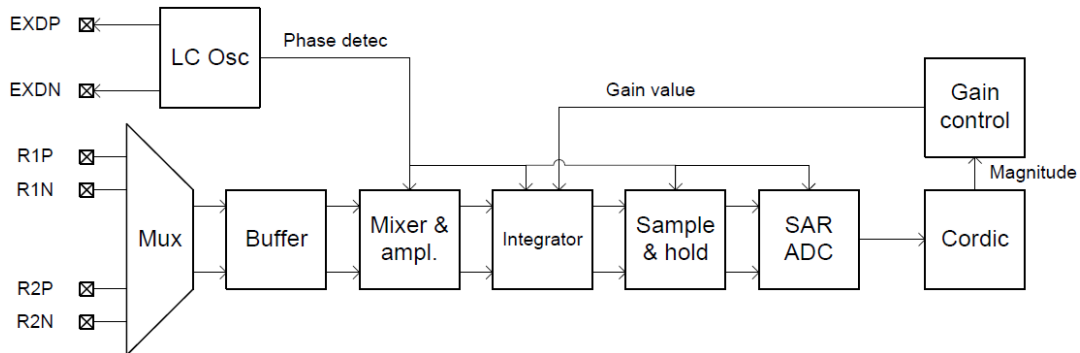


Figure 11. Gain Control

Table 15. AGC0 Register Description

| Bits | Symbol | Description | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------------------|--|--|-------------------------------|-----------------------|-------------|-------------------------------|------|-----|-----|-----------|------|--------------|-----|--------------|------|--------------|-----|--------------|-------------------------------------|-----------------|----------------------------------|---------------------------|---------------------------|--|--|--|
| agc0.15 | Reserved | Not used, read as 0 (SWR) | | | | | | | | | | | | | | | | | | | | | | | | |
| agc0.14 - agc0.9 | smp_cycle | Only when OSR is changed to a non-default value (4) and the AGC control is turned on the sample cycle value needs to be adapted accordingly: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>OSR</th> <th>Samples/Channel</th> <th>2 × Channel</th> <th>Recommended smp_cycle Setting</th> </tr> </thead> <tbody> <tr> <td>0b00</td> <td>4</td> <td>8</td> <td>0b00.0100</td> </tr> <tr> <td>0b01</td> <td>8</td> <td>16</td> <td>0b00.1100</td> </tr> <tr> <td>0b10</td> <td>16</td> <td>32</td> <td>0b01.1100</td> </tr> <tr> <td>0b11</td> <td>32</td> <td>64</td> <td>0b11.1100</td> </tr> </tbody> </table> | OSR | Samples/Channel | 2 × Channel | Recommended smp_cycle Setting | 0b00 | 4 | 8 | 0b00.0100 | 0b01 | 8 | 16 | 0b00.1100 | 0b10 | 16 | 32 | 0b01.1100 | 0b11 | 32 | 64 | 0b11.1100 | | | | |
| OSR | Samples/Channel | 2 × Channel | Recommended smp_cycle Setting | | | | | | | | | | | | | | | | | | | | | | | |
| 0b00 | 4 | 8 | 0b00.0100 | | | | | | | | | | | | | | | | | | | | | | | |
| 0b01 | 8 | 16 | 0b00.1100 | | | | | | | | | | | | | | | | | | | | | | | |
| 0b10 | 16 | 32 | 0b01.1100 | | | | | | | | | | | | | | | | | | | | | | | |
| 0b11 | 32 | 64 | 0b11.1100 | | | | | | | | | | | | | | | | | | | | | | | |
| agc0.8 - agc0.4 | ext | Renesas internal | | | | | | | | | | | | | | | | | | | | | | | | |
| agc0.3 - agc0.0 | gain_stage | Integrator gain stage <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Gain_stage</th> <th>Integrator Gain Stage</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Minimum gain</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0xC</td> <td>Maximum gain</td> </tr> <tr> <td>...</td> <td>Maximum gain</td> </tr> <tr> <td>...</td> <td>Maximum gain</td> </tr> <tr> <td>0xF</td> <td>Maximum gain</td> </tr> </tbody> </table> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>AGC Mode (AGC1.13, AGC1.12) in AGC1</th> <th>Integrator Gain</th> </tr> </thead> <tbody> <tr> <td>Gain regulation OFF (0b00, 0b01)</td> <td>Fixed gain stage setting.</td> </tr> <tr> <td>Gain regulation ON (0b10)</td> <td>Maximum gain stage value for gain regulation. This is limiting the gain regulation. It clamps the upper gain stage value. First applicable value for AGC is fixed 0x3.</td> </tr> <tr> <td></td> <td>Maximum gain stage value for gain regulation. This is limiting the gain regulation. It clamps the upper gain stage value. After start-up IntegrationTim adaptation is active with gain stage 0x6. Consecutive gainstage adaptation starts with gain stage 0x3.</td> </tr> </tbody> </table> | Gain_stage | Integrator Gain Stage | 0x0 | Minimum gain | ... | ... | ... | ... | 0xC | Maximum gain | ... | Maximum gain | ... | Maximum gain | 0xF | Maximum gain | AGC Mode (AGC1.13, AGC1.12) in AGC1 | Integrator Gain | Gain regulation OFF (0b00, 0b01) | Fixed gain stage setting. | Gain regulation ON (0b10) | Maximum gain stage value for gain regulation. This is limiting the gain regulation. It clamps the upper gain stage value. First applicable value for AGC is fixed 0x3. | | Maximum gain stage value for gain regulation. This is limiting the gain regulation. It clamps the upper gain stage value. After start-up IntegrationTim adaptation is active with gain stage 0x6. Consecutive gainstage adaptation starts with gain stage 0x3. |
| Gain_stage | Integrator Gain Stage | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0 | Minimum gain | | | | | | | | | | | | | | | | | | | | | | | | | |
| ... | ... | | | | | | | | | | | | | | | | | | | | | | | | | |
| ... | ... | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0xC | Maximum gain | | | | | | | | | | | | | | | | | | | | | | | | | |
| ... | Maximum gain | | | | | | | | | | | | | | | | | | | | | | | | | |
| ... | Maximum gain | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0xF | Maximum gain | | | | | | | | | | | | | | | | | | | | | | | | | |
| AGC Mode (AGC1.13, AGC1.12) in AGC1 | Integrator Gain | | | | | | | | | | | | | | | | | | | | | | | | | |
| Gain regulation OFF (0b00, 0b01) | Fixed gain stage setting. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Gain regulation ON (0b10) | Maximum gain stage value for gain regulation. This is limiting the gain regulation. It clamps the upper gain stage value. First applicable value for AGC is fixed 0x3. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Maximum gain stage value for gain regulation. This is limiting the gain regulation. It clamps the upper gain stage value. After start-up IntegrationTim adaptation is active with gain stage 0x6. Consecutive gainstage adaptation starts with gain stage 0x3. | | | | | | | | | | | | | | | | | | | | | | | | | |

1.15 AGC1

Address of register: 0x0D Default value: 0x0255.

Automatic Gain Control.

Table 16. AGC0 Register Description

| Bits | Symbol | Description | | | | | | | | | | | | | | | | | | |
|-------------------|---------------------------------|--|---------------|---------------------------------|-----------------------------|------|-------|-----|-------|-----|-------|------|-------|-----|-------|----|-------|----|-------|----|
| agc1.15 | agc_suppress | Renesas internal | | | | | | | | | | | | | | | | | | |
| agc1.14 | agc_interlink | Renesas internal | | | | | | | | | | | | | | | | | | |
| agc1.13 - agc1.12 | agc_mode | Extend integration cycle related to excitation clock period effective integration time = (7 + ext) x lc_period. <table border="1"> <thead> <tr> <th>Agc_mode</th> <th>Automatic Gain</th> <th>Integration Gain Adaptation</th> </tr> </thead> <tbody> <tr> <td>0b00</td> <td>Off</td> <td>Off</td> </tr> <tr> <td>0b01</td> <td>Off</td> <td>On</td> </tr> <tr> <td>0b10</td> <td>On</td> <td>Off</td> </tr> <tr> <td>0b11</td> <td>On</td> <td>On</td> </tr> </tbody> </table> | Agc_mode | Automatic Gain | Integration Gain Adaptation | 0b00 | Off | Off | 0b01 | Off | On | 0b10 | On | Off | 0b11 | On | On | | | |
| Agc_mode | Automatic Gain | Integration Gain Adaptation | | | | | | | | | | | | | | | | | | |
| 0b00 | Off | Off | | | | | | | | | | | | | | | | | | |
| 0b01 | Off | On | | | | | | | | | | | | | | | | | | |
| 0b10 | On | Off | | | | | | | | | | | | | | | | | | |
| 0b11 | On | On | | | | | | | | | | | | | | | | | | |
| agc1.11 - agc1.10 | exc_freq_high | High limit for excitation coil frequency range alarm. <table border="1"> <thead> <tr> <th>Exc_freq_high</th> <th>Excitation Coil Frequency [MHz]</th> </tr> </thead> <tbody> <tr> <td>0b00</td> <td>6.0</td> </tr> <tr> <td>0b01</td> <td>6.5</td> </tr> <tr> <td>0b10</td> <td>7.0</td> </tr> <tr> <td>0b11</td> <td>8.0</td> </tr> </tbody> </table> <p>An additional variance of about +/- 20% has to be taken into account to frequency variation of ZMID502X internal oscillator over temperature and voltage. The measurement time is ~ 100 us.</p> | Exc_freq_high | Excitation Coil Frequency [MHz] | 0b00 | 6.0 | 0b01 | 6.5 | 0b10 | 7.0 | 0b11 | 8.0 | | | | | | | | |
| Exc_freq_high | Excitation Coil Frequency [MHz] | | | | | | | | | | | | | | | | | | | |
| 0b00 | 6.0 | | | | | | | | | | | | | | | | | | | |
| 0b01 | 6.5 | | | | | | | | | | | | | | | | | | | |
| 0b10 | 7.0 | | | | | | | | | | | | | | | | | | | |
| 0b11 | 8.0 | | | | | | | | | | | | | | | | | | | |
| agc1.9 - agc1.8 | exc_freq_low | Low limit for excitation coil frequency range alarm. <table border="1"> <thead> <tr> <th>Exc_freq_low</th> <th>Excitation Coil Frequency [MHz]</th> </tr> </thead> <tbody> <tr> <td>0b00</td> <td>1.0</td> </tr> <tr> <td>0b01</td> <td>1.5</td> </tr> <tr> <td>0b10</td> <td>2.0</td> </tr> <tr> <td>0b11</td> <td>2.5</td> </tr> </tbody> </table> <p>An additional variance of about +/- 20% has to be taken into account to frequency variation of ZMID4200 internal oscillator over temperature and voltage. The measurement time is ~ 100 us.</p> | Exc_freq_low | Excitation Coil Frequency [MHz] | 0b00 | 1.0 | 0b01 | 1.5 | 0b10 | 2.0 | 0b11 | 2.5 | | | | | | | | |
| Exc_freq_low | Excitation Coil Frequency [MHz] | | | | | | | | | | | | | | | | | | | |
| 0b00 | 1.0 | | | | | | | | | | | | | | | | | | | |
| 0b01 | 1.5 | | | | | | | | | | | | | | | | | | | |
| 0b10 | 2.0 | | | | | | | | | | | | | | | | | | | |
| 0b11 | 2.5 | | | | | | | | | | | | | | | | | | | |
| agc1.7 | Reserved | Not used, read as 0 (SWR). | | | | | | | | | | | | | | | | | | |
| agc1.6 - agc1.4 | cordmagul | Cordic magnitude upper level. (100%0x34B6.....13494d) <table border="1"> <thead> <tr> <th>Cordmagul</th> <th>Magnitude Upper Level [%]</th> </tr> </thead> <tbody> <tr> <td>0b111</td> <td>90</td> </tr> <tr> <td>0b110</td> <td>85</td> </tr> <tr> <td>0b101</td> <td>80</td> </tr> <tr> <td>0b100</td> <td>75</td> </tr> <tr> <td>0b011</td> <td>70</td> </tr> <tr> <td>0b010</td> <td>65</td> </tr> <tr> <td>0b001</td> <td>60</td> </tr> <tr> <td>0b000</td> <td>55</td> </tr> </tbody> </table> | Cordmagul | Magnitude Upper Level [%] | 0b111 | 90 | 0b110 | 85 | 0b101 | 80 | 0b100 | 75 | 0b011 | 70 | 0b010 | 65 | 0b001 | 60 | 0b000 | 55 |
| Cordmagul | Magnitude Upper Level [%] | | | | | | | | | | | | | | | | | | | |
| 0b111 | 90 | | | | | | | | | | | | | | | | | | | |
| 0b110 | 85 | | | | | | | | | | | | | | | | | | | |
| 0b101 | 80 | | | | | | | | | | | | | | | | | | | |
| 0b100 | 75 | | | | | | | | | | | | | | | | | | | |
| 0b011 | 70 | | | | | | | | | | | | | | | | | | | |
| 0b010 | 65 | | | | | | | | | | | | | | | | | | | |
| 0b001 | 60 | | | | | | | | | | | | | | | | | | | |
| 0b000 | 55 | | | | | | | | | | | | | | | | | | | |
| agc1.3 | Reserved | Not used, read as 0 (SWR). | | | | | | | | | | | | | | | | | | |
| agc1.2 - agc1.0 | cordmagul | Cordic magnitude lower level. <table border="1"> <thead> <tr> <th>Cordmagul</th> <th>Magnitude Upper Level [%]</th> </tr> </thead> <tbody> <tr> <td>0b111</td> <td>55</td> </tr> <tr> <td>0b110</td> <td>50</td> </tr> <tr> <td>0b101</td> <td>45</td> </tr> <tr> <td>0b100</td> <td>40</td> </tr> <tr> <td>0b011</td> <td>35</td> </tr> <tr> <td>0b010</td> <td>30</td> </tr> <tr> <td>0b001</td> <td>25</td> </tr> <tr> <td>0b000</td> <td>20</td> </tr> </tbody> </table> | Cordmagul | Magnitude Upper Level [%] | 0b111 | 55 | 0b110 | 50 | 0b101 | 45 | 0b100 | 40 | 0b011 | 35 | 0b010 | 30 | 0b001 | 25 | 0b000 | 20 |
| Cordmagul | Magnitude Upper Level [%] | | | | | | | | | | | | | | | | | | | |
| 0b111 | 55 | | | | | | | | | | | | | | | | | | | |
| 0b110 | 50 | | | | | | | | | | | | | | | | | | | |
| 0b101 | 45 | | | | | | | | | | | | | | | | | | | |
| 0b100 | 40 | | | | | | | | | | | | | | | | | | | |
| 0b011 | 35 | | | | | | | | | | | | | | | | | | | |
| 0b010 | 30 | | | | | | | | | | | | | | | | | | | |
| 0b001 | 25 | | | | | | | | | | | | | | | | | | | |
| 0b000 | 20 | | | | | | | | | | | | | | | | | | | |

Notes: The reserved bits can be written and read to/from the block E2P. The copy process copies only defined bits to the SWR. The Cordic magnitude upper level should be higher than the lower level.

1.16 Mask

Address of register: 0x0E Default value: 0xBFFF.

The diagnostic mask, in the case that the output is set in the diagnostic state allows to prevent a diagnostic flag. The status of the latched diagnostic flags can be monitored by reading the diagnostic register.

Table 17. Mask Register Description

| Bits | Symbol | Description | |
|---------|---------------|--|---|
| mask.15 | agc_low gain | AGC low gain status | |
| | | Agc_low Gain | AGC Low Gain Alarm |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.14 | ee_ded | EEPROM double error detection | |
| | | Ee_ded | Double Error Alarm |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.13 | r2_coil_fail | Receiver coil2 short/open check status | |
| | | R2_coil_fail | Receiver Coil2 Short/Open Check Status |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.12 | r1_coil_fail | Receiver coil1 short/open check status | |
| | | R1_coil_fail | Receiver Coil1 Short/Open Check Status |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.11 | Open | R1 or R2 receiver coil open | |
| | | Open | R1 or R2 Receiver Coil Open |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.10 | rc_coil_short | R1 or R2 receiver coil short | |
| | | Rc_coil_short | R1 or R2 Receiver Coil Short |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.9 | rc_gnd_short | R1 or R2 receiver coil short to gnd | |
| | | Rc_gnd_short | R1 or R2 Receiver Coil Short to GND |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.8 | exc_break_p | Not used, read as 0 (SWR). | |
| | | Exc_break_p | Excitation Coil Break P |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.7 | exc_break_n | Cordic magnitude lower level. | |
| | | Exc_break_n | Excitation Coil Break N |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.6 | srb_parity | Shadow Register bank parity | |
| | | Srb_parity | Shadow Register Bank Parity |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.5 | adc_dsp_ovfl | ADC digital signal processing overflow | |
| | | Adc_dsp_ovfl | ADC Digital Signal Processing Overflow (Alarm) |
| | | 0b0 | Enable |
| | | 0b1 | Disable |
| mask.4 | amp_dsp_ovfl | Amplitude digital signal processing overflow | |
| | | Amp_dsp_ovfl | Amplitude Digital Signal Processing Overflow |
| | | 0b0 | Enable |
| | | 0b1 | Disable |

| Bits | Symbol | Description |
|--------|--------------|---|
| mask.3 | lc_osc_fail | LC oscillator range check |
| | | Lc_osc_fail LC Oscillator Range Check |
| | | 0b0 Enable |
| | | 0b1 Disable |
| mask.2 | lc_osc_stuck | LC oscillator stuck check |
| | | C_osc_stuck LC Oscillator Stuck Check |
| | | 0b0 Enable |
| | | 0b1 Disable |
| mask.1 | mag_low | Cordic magnitude is below threshold (lower limit, see section 1.16) |
| | | C_osc_stuck Cordic Magnitude is Below Threshold (Lower Limit, 1.14) |
| | | 0b0 Enable |
| | | 0b1 Disable |
| mask.0 | mag_high | Cordic magnitude is above threshold (upper limit, see section 1.16) |
| | | mag_high Cordic Magnitude is Above Threshold (Upper Limit, 1.14) |
| | | 0b0 Enable |
| | | 0b1 Disable |

1.17 Traceability0

E2P

Address of register: 0X0F.

Default value: none, read only.

Renesas identification and version number.

Table 18. Traceability0 Register Description

| Bits | Symbol | Description |
|----------------------|--------|--|
| trace0.15 - trace0.0 | IDT_id | Renesas Identification and version number. |

1.18 Traceability1

E2P

Address of register: 0x10.

Default value: none, read only.

Renesas identification and version number.

Table 19. Traceability1 Register Description

| Bits | Symbol | Description |
|----------------------|--------|--|
| Trace1.15 - Trace1.0 | IDT_id | Renesas Identification and version number. |

1.19 Misc

Address of register: 0x11.

Default value: 0x00C2.

Table 20. Misc Register Description

| Bits | Symbol | Description | | | | | | |
|---|---------------------------|--|----------------------------|----------------------------|-----|--------------------|-----|--------------|
| misc.15 - misc.9 | IDT | Renesas internal | | | | | | |
| misc.8 | agc_offset_sat_mode | AGC offset saturation mode. If this mode is activated an offset saturation detection forces the gain regulation to decrement the gain step to decrease the ADC input signal level. | | | | | | |
| | | <table border="1"> <thead> <tr> <th>agc_offset_sat_mode</th> <th>AGC Offset Saturation Mode</th> </tr> </thead> <tbody> <tr> <td>0b0</td> <td>Extension off</td> </tr> <tr> <td>0b1</td> <td>Extension on</td> </tr> </tbody> </table> | agc_offset_sat_mode | AGC Offset Saturation Mode | 0b0 | Extension off | 0b1 | Extension on |
| | | agc_offset_sat_mode | AGC Offset Saturation Mode | | | | | |
| 0b0 | Extension off | | | | | | | |
| 0b1 | Extension on | | | | | | | |
| <table border="1"> <thead> <tr> <th>exc_type</th> <th>Coil Alarm Type Selection</th> </tr> </thead> <tbody> <tr> <td>0b0</td> <td>Event alarm type</td> </tr> <tr> <td>0b1</td> <td>Latched alarm type</td> </tr> </tbody> </table> | exc_type | Coil Alarm Type Selection | 0b0 | Event alarm type | 0b1 | Latched alarm type | | |
| exc_type | Coil Alarm Type Selection | | | | | | | |
| 0b0 | Event alarm type | | | | | | | |
| 0b1 | Latched alarm type | | | | | | | |
| misc.7 | exc_type | Excitation coil alarm type selection (exc_break_p, exc_break_n) | | | | | | |
| misc.6- misc.0 | IDT | Renesas internal | | | | | | |

1.20 Afe_Agc

Address of register: 0x13.

Default value: none, read only.

The integration time regulation adapts the number of integration time cycles that a constant integration time independent of the LC-frequency is achieved. The adjusted cycle number can be monitored by reading the parameter agc_intgr. The automatic gain regulation process (AGC1) modify the gain by a decision circuit which compares the actual cordic magnitude with the programmed cordic magnitude limits. The adjusted gain value can be monitored by reading the register. The phase information is the polarity of the incoming R1/R2 signal respectively the polarity of the decimated samples R1/2.

Table 21. Afe_Agc Register Description

| Bits | Symbol | Description | |
|-------------------------|----------------|---|-------------------------------------|
| afe_agc.15 - afe_agc.13 | Reserved | Not used, read as 0 (SWR). | |
| afe_agc.12 - afe_agc.8 | agc_intgr | AGC adjusted number of integration cycles effective integration time = (7 + agc_intgr) x I _c clock period. | |
| afe_agc.7 - afe_agc.4 | agc_gain stage | AGC adjusted gain stage value range 0x0...0xC. | |
| afe_agc.3 | r1_polarity | Polarity of receiver coil R1 | |
| | | R1_polarity | Polarity of Receiver Coil R1 |
| | | 0b0 | Negative |
| | | 0b1 | Positive |
| afe_agc.2 | r2_polarity | Polarity of receiver coil R2 | |
| | | R2_polarity | Polarity of Receiver Coil R2 |
| | | 0b0 | Negative |
| | | 0b1 | Positive |
| afe_agc.1 | y_cos_pol | Phase polarity of Ycosine amplitude parameter. The sensor position is calculated based on the receiver amplitude (see sections 1.21 and 1.22) and related phase polarity. | |
| afe_agc.0 | x_sin_pol | Phase polarity of Xsine amplitude parameter. The sensor position is calculated based on the receiver amplitude (see sections 1.21 and 1.22) and related phase polarity. | |

1.21 Xsine

Address of register: 0x14.

Default value: none, read only.

The amplitude of the receiver coils after decimation and amplitude offset evaluation (sampler output) can be monitored by reading the register Xsine.

Table 22. Xsine Register Description

| Bits | Symbol | Description |
|--------------------|-----------|---|
| xsine.15 -xsine.13 | Reserved | Not used, read as 0 (SWR). |
| xsine.12 -xsine.0 | x_sin_amp | Amplitude of receiver coil. Absolute amplitude after decimation and amplitude offset evaluation. |

1.22 Ycosine

Address of register: 0x15.

Default value: none, read only.

The amplitude of the receiver coil after decimation and amplitude offset evaluation (sampler output) can be monitored by reading the register Ycosine.

Table 23. Ycosine Register Description

| Bits | Symbol | Description |
|--------------------|-----------|---|
| xsine.15 -xsine.13 | Reserved | Not used, read as 0 (SWR). |
| xsine.12 –xsine.0 | y_cos_amp | Amplitude of receiver coil absolute amplitude after decimation and amplitude offset evaluation. |

1.23 Angle

Address of register: 0x16.

Default value: None; read only.

The sensor position is calculated based on the x_sin_amp (see section 1.21) and y_cos_amp (see section 1.22) parameter. The result of 90 degree angle is calculated by $\arctan\left(\frac{x_sin_amp}{y_cos_amp}\right)$.

The trigonometric function is implemented by an iterative CORDIC (Coordinate Rotation Digital Computer) architecture. The chosen number of iteration steps is 16. CORDIC works by rotating the coordinate system through constant angles until the angle is reduced to zero and the result vector is aligned with the X axis. The result of the vectoring operation is a rotation angle (0deg <= angle <= 90deg) and the scaled magnitude of the original vector. The calculated rotation angle is mapped to a 15-bit vector and can be monitored by the angle register read access.

Table 24. Angle Register Description

| Bits | Symbol | Description | | | | | | | | |
|--------------------|----------------|--|--------------|----------------|--------|---|-------|-------|--------|----|
| angle.15 | Reserved | Not used, read as 0 (SWR). | | | | | | | | |
| angle.14 – angle.0 | cordic angle | Rotational CORDIC angle from 0 degree to 90 degree. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th>Cordic Angle</th> <th>Angle [Degree]</th> </tr> </thead> <tbody> <tr> <td>0x0000</td> <td>0</td> </tr> <tr> <td>.....</td> <td>.....</td> </tr> <tr> <td>0x7FFF</td> <td>90</td> </tr> </tbody> </table> | Cordic Angle | Angle [Degree] | 0x0000 | 0 | | | 0x7FFF | 90 |
| Cordic Angle | Angle [Degree] | | | | | | | | | |
| 0x0000 | 0 | | | | | | | | | |
| | | | | | | | | | | |
| 0x7FFF | 90 | | | | | | | | | |

1.24 Cordic Magnitude

Address of register: 0x17

Default value: None: read only

The CORDIC algorithm in vectoring mode works by seeking to minimize the Ycosine component of the residual vector at each rotation. The result of the vectoring operation is a rotation angle (see section 1.23) and the scaled magnitude of the original vector $\sqrt{Xsine^2 + Ycosine^2}$.

The aggregate constant of all 16 iteration steps resp. the scale factor is $\frac{1}{0.607}$

It follows for the cordic magnitude:

$$\text{Cordic magnitude} = \frac{\sqrt{Xsine^2 + Ycosine^2}}{0.607}$$

Assumption: Saturation of both receiver channels:

$$Xsine = Ycosine = 0x1FFF$$

$$\text{cordic magnitude(sat)} = 0x4A8B$$

Assumption: Signals of both receive channels at ideal amplification (below saturation).

$$Xsine = 0x1FFF \quad Ycosine = 0x0000$$

$$\text{cordic magnitude(opt)} = 0x34B6$$

Conclusion: The cordic magnitude is a monitor for gain respectively integration time setting. It is important that the magnitude does not exceed the optimum level. Otherwise this will lead to a failure in the position calculation (nonlinearity).

Table 25. Mag Register Description

| Bits | Symbol | Description | |
|--------------------|--------------|--|------------------|
| angle.15 | Reserved | Not used, read as 0 (SWR). | |
| angle.14 – angle.0 | cordic angle | Rotational CORDIC magnitude from minimum magnitude saturation. | |
| | | Cordic Mag | Magnitude |
| | | 0x4A8B | Sat |
| | | 0x34B6 | Opt |
| | | 0x0000 | Min |

1.25 SPA

Address of register: 0x18.

Default value: None: read only.

The CORDIC processor output angle is expanded by the phase polarity information (y_cos_pol & x_sin_pol) to a range from 0 deg to 360 deg. The ZMID4200 internal notation is a 17-bit vector (4 x angle 15-bit). Due to the 16-bit wide data structure of the OWI interface, the spatial angle vector is truncated to 16 bits (17 down to 1) for the read-access.

Table 26. Spa Register Description

| Bits | Symbol | Description | |
|-----------------|---------------|--|-------------------------------|
| spa.15 - spat.0 | spatial angle | Spatial angle | |
| | | Expanded cordic angle to 360 degree range. The value is before calibration and linear error correction. The ZMID4200 internal notation is a 17-bit wide vector. From 0 deg to 360 deg. | |
| | | Spatial Angle | Spatial Angle [Degree] |
| | | 0x0000 | 0 min |
| | | 0xFFFF | 360 max |

Note: Due to the truncation of the spatial angle number range to 16-bit (OWI access), the number range of the cordic angle has to be also truncated by one bit (14 down to 1) for direct comparison of this two parameters.

1.26 Pos0

Address of register: 0x19.

Default value: None: read only.

The spatial angle is modified by the calibration parameter slope & offset (see sections 1.2 and 1.3) and the linearity error correction. The pos0 value is the calculated value with linearity error correction before calibration (see section 1.11, corr_mod = 0).

Table 27. Pos0 Register Description

| Bits | Symbol | Description | | | | | | |
|---------------------|------------------------|---|---------------|------------------------|--------|---|--------|-----|
| pos0.15 - pos0.0 | pos_so_corr0 | Position before calibration & linearity error correction (linear error correction pre-calibration corr_mode = 0), see section 1.11. | | | | | | |
| | | <table border="1"> <thead> <tr> <th>Spatial Angle</th> <th>Spatial Angle [Degree]</th> </tr> </thead> <tbody> <tr> <td>0x0000</td> <td>0</td> </tr> <tr> <td>0xFFFF</td> <td>360</td> </tr> </tbody> </table> | Spatial Angle | Spatial Angle [Degree] | 0x0000 | 0 | 0xFFFF | 360 |
| Spatial Angle | Spatial Angle [Degree] | | | | | | | |
| 0x0000 | 0 | | | | | | | |
| 0xFFFF | 360 | | | | | | | |

1.27 Pos1

Address of register: 0x1A Default value: None: read only.

The spatial angle is modified by the calibration parameter slope & offset (see sections 1.2 and 1.3) and the linearity error correction. The pos1 value is the calculated value with linearity error correction after calibration (see section 1.11, corr_mod = 1).

Table 28. Pos1 Register Description

| Bits | Symbol | Description | | | | | | |
|------------------|------------------------|---|---------------|------------------------|--------|---|--------|-----|
| pos0.15 - pos0.0 | pos_so_corr1 | Position after calibration & linearity error correction (linear error correction post-calibration, corr_mod= 1), see section 1.11. | | | | | | |
| | | <table border="1"> <thead> <tr> <th>Spatial Angle</th> <th>Spatial Angle [Degree]</th> </tr> </thead> <tbody> <tr> <td>0x0000</td> <td>0</td> </tr> <tr> <td>0xFFFF</td> <td>360</td> </tr> </tbody> </table> | Spatial Angle | Spatial Angle [Degree] | 0x0000 | 0 | 0xFFFF | 360 |
| Spatial Angle | Spatial Angle [Degree] | | | | | | | |
| 0x0000 | 0 | | | | | | | |
| 0xFFFF | 360 | | | | | | | |

Note: For the different output protocols the calculated position is truncated from MSB down to 1/5/7. For the SENT respectively PWM/Analog the remainder is rounded.

Note: If corr_mod = 0b0 (1.10, calout.3) pos_so_corr1 is equal pos_so_corr0 (1.25).

2. Glossary

| Acronym | Definition |
|---------|---|
| ADC | Analog Digital Converter |
| ATE | Automatic Test Equipment |
| ATPG | Automatic Test Pattern Generation |
| PPU | Position Processing Unit |
| E2P | Electrically Erasable Programmable Read Only Memory |
| ECU | Electronic Control Unit |
| ECC | Error Correction Code |
| FEC | Forward Error Correction |
| GND | Ground |
| IC | Integrated Circuit |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| OWI | One Wire Interface |
| OSR | Over Sampling Rate |
| PPR | Pulse Pause Ratio |
| SWR | Shadow Word Register bank |
| TDM | Time Division Multiplexer |

3. Revision History

| Revision Date | Description of Change |
|------------------|--|
| October 16, 2024 | Corrected typos: <ul style="list-style-type: none"> ▪ output 7, 3, 2 on page 19 ▪ on page 18 ▪ on page 30 |
| July 21, 2021 | Initial release |

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Disclaimer Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/