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# 1. Introduction

The 5P49V6967 and 5P45V6968 Evaluation Boards are designed to help users evaluate the VersaClock® 6E 5P49V6967 and 5P49V6968 respectively. When the Evaluation Board (EVB) is connected via USB to the user's computer running the IDT's *VersaClock 6E Timing Commander™ Software*, the 5P49V6967/68 can be configured and programmed to generate frequencies with best-in-class performance. In addition to one single-ended output and three programmable differential outputs, the 5P49V6967 has four additional LP-HCSL outputs and the 5P49V6968 has eight additional LP-HCSL outputs.

# 2. Board Overview

**Figure 1. 5P49V6967 EVB – Top View**

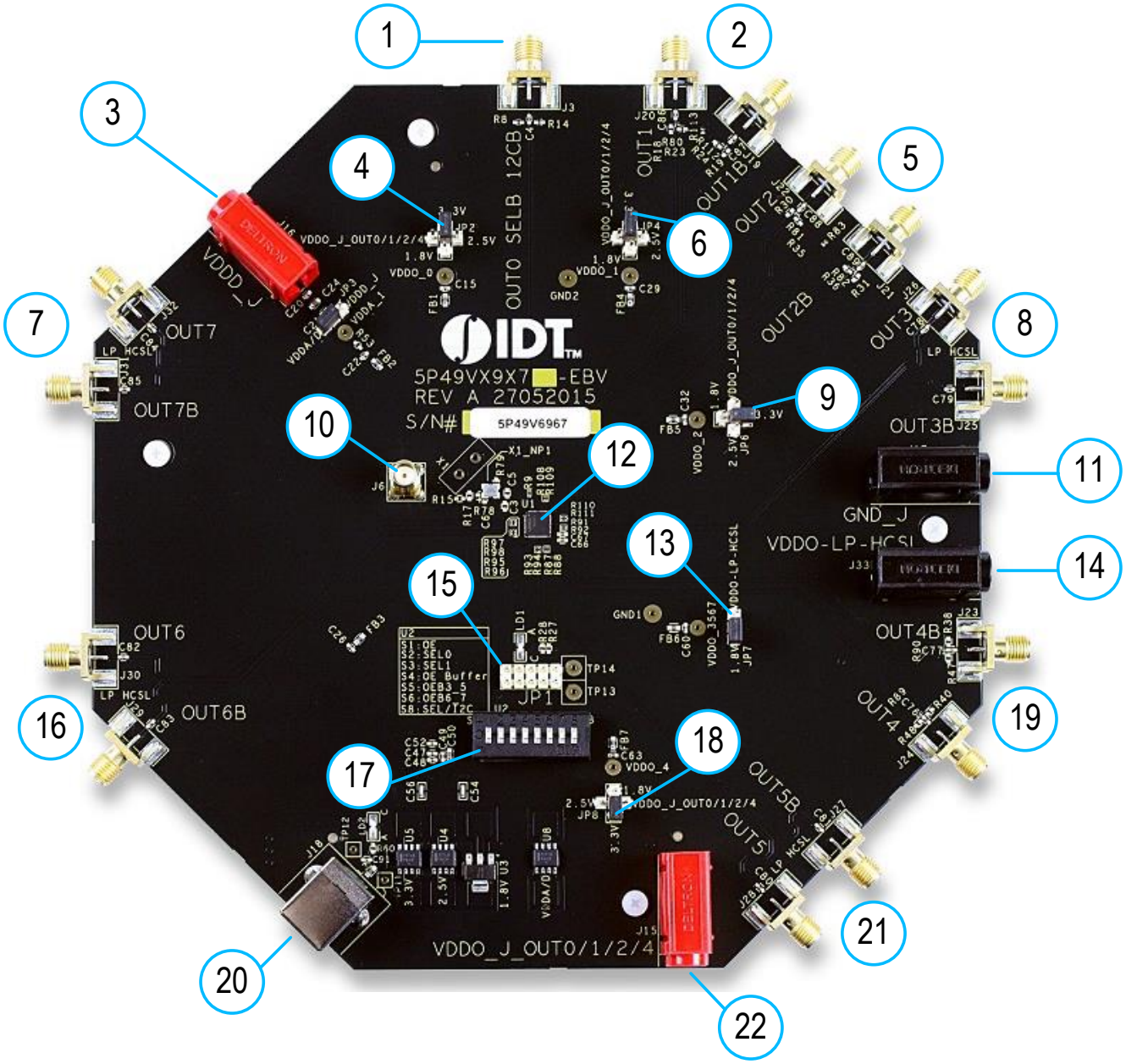


**Table 1. 5P49V6967 – EVB Pins and Functions**

Note: See Figure 1 for reference numbers in the following table.

| Ref. | Name | On-Board Connector Label | Function |
|---|---|---|---|
| 1 | Output 0 | J3 | Single-ended LVCMOS clock output |
| 2 | Output 1 | J19, J20 | Differential clock output |
| 3 | VDDD_J | J16 | VDD jack for VDD digital external power supply |
| 4 | VDDO_0 | JP2 | Power supply voltage selector for Output 0 |
| 5 | Output 2 | J21, J22 | Differential clock output |
| 6 | VDDO_1 | JP4 | Power supply voltage selector for Output 1 |
| 7 | Output 7 | J31, J32 | LP-HCSL differential clock output |
| 8 | Output 3 | J25, J26 | Differential clock output |
| 9 | VDDO_2 | JP6 | Power supply voltage selector for Output 2 |
| 10 | XIN | J6 | Input for overdriving XIN pin |
| 11 | Ground Jack | J17 | Ground jack for external power supply |
| 12 | 5P49V6967 | U1 | Evaluation device |
| 13 | VDDO_3 5 6 7 | JP7 | Power supply selector for LP-HCSL outputs |
| 14 | VDDO LP-HCSL Jack | J33 | VDD jack for VDDO_LP-HCSL (1.8V) external power supply |
| 15 | Aardvark Connector | JP1 | For Aardvark connection |
| 16 | Output 6 | J29, J30 | LP-HCSL differential clock output |
| 17 | DIP Switch | U2 | S1: Output Enable (OE/SD)<br>S2: Sel0<br>S3: Sel1<br>S4: OE Buffer<br>S5: $OEB_{3,5}$<br>S6: $OEB_{6,7}$<br>S8: Sel [1:0] ; Default: I2C mode |
| 18 | VDDO_4 | JP8 | Power supply voltage selector for Output 4 |
| 19 | Output 4 | J23, J24 | Differential clock output |
| 20 | USB Interface | J18 | Used for connection with the user's computer for interaction with the *IDT Timing Commander Software.* |
| 21 | Output 5 | J27, J28 | LP-HCSL differential clock output |
| 22 | VDDO Jack | J15 | VDD jack for external power supply |

**Figure 2. 5P49V6968 EVB – Top View**

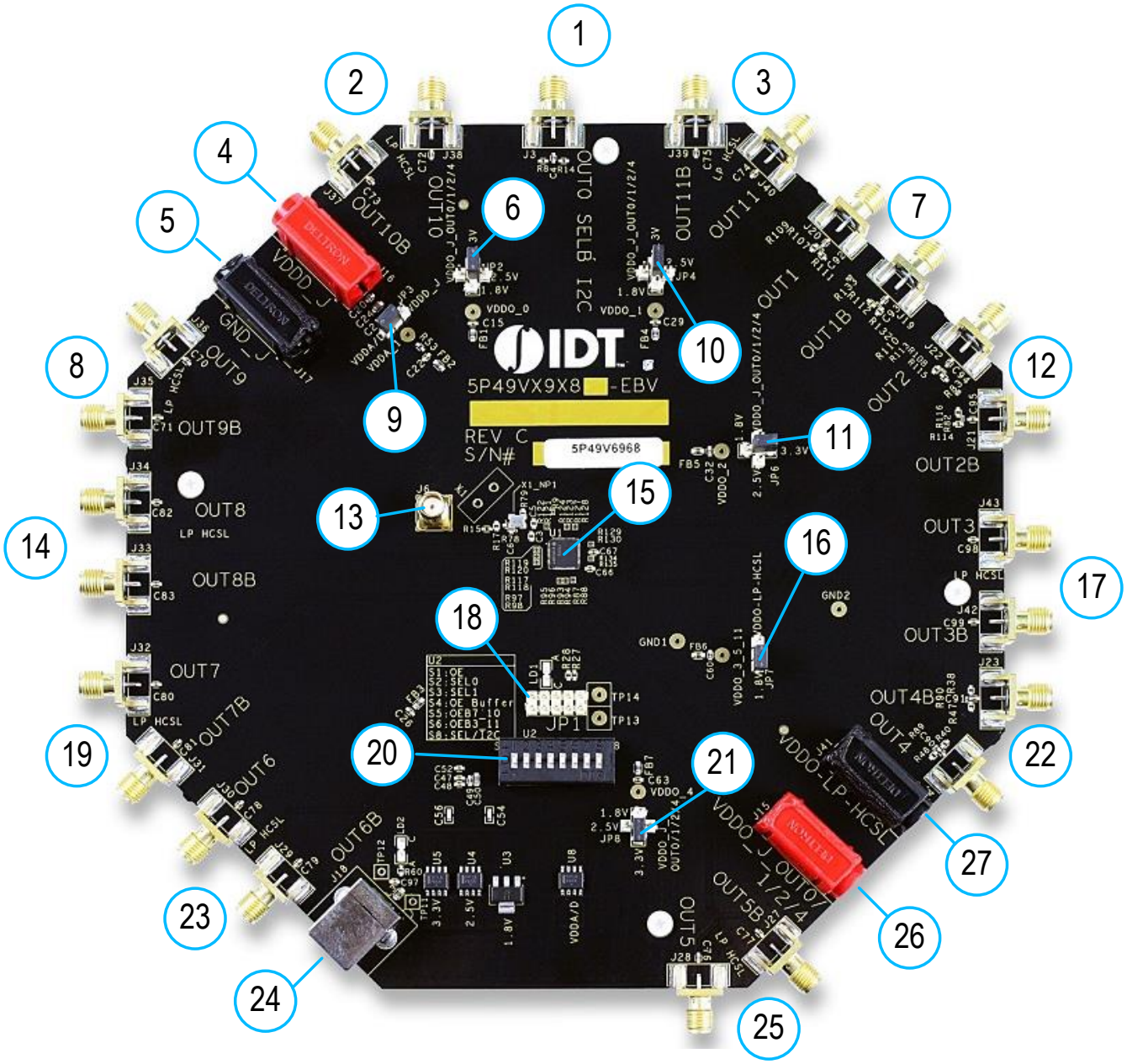


**Table 2. 5P49V6968 – EVB Pins and Functions**

Note: See Figure 2 for reference numbers in the following table.

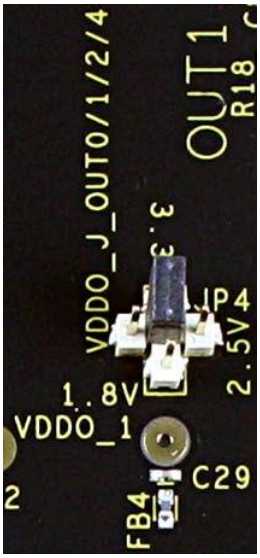
| Ref. | Name | On-Board Connector Label | Function |
|---|---|---|---|
| 1 | Output 0 | J3 | Single-ended LVCMOS clock output |
| 2 | Output 10 | J37, J38 | LP-HCSL differential clock output |
| 3 | Output 11 | J39, J40 | LP-HCSL differential clock output |
| 4 | VDDD_J | J16 | VDD jack for VDD digital external power supply |
| 5 | Ground Jack | J17 | Ground jack for external power supply |
| 6 | VDDO_0 | JP2 | Power supply voltage selector for Output 0 |
| 7 | Output 1 | J19, J20 | Differential clock output |
| 8 | Output 9 | J35, J36 | LP-HCSL differential clock output |
| 9 | VDDA/D | JP3 | Power supply voltage selector for VDDA and VDDD |
| 10 | VDDO_1 | JP4 | Power supply voltage selector for Output 1 |
| 11 | VDDO_2 | JP6 | Power supply voltage selector for Output 2 |
| 12 | Output 2 | J21, J22 | Differential clock output |
| 13 | XIN | J6 | Input for overdriving the XIN pin. |
| 14 | Output 8 | J33, J34 | LP-HCSL differential clock output |
| 15 | 5P49V6968 | U1 | Evaluation device |
| 16 | VDDO_3_5_11 | JP7 | Power supply selector for LP-HCSL outputs |
| 17 | Output 3 | J42, J43 | Differential clock output |
| 18 | Aardvark Connector | JP1 | For Aardvark connection |
| 19 | Output 7 | J31, J32 | LP-HCSL differential clock output |
| 20 | DIP Switch | U2 | S1: Output Enable (OE/SD)<br>S2: Sel0<br>S3: Sel1<br>S4: OE Buffer<br>S5: $OEB_{7-10}$<br>S6: $OEB_{3-11}$<br>S8: Sel [1:0] ; Default: I2C mode |
| 21 | VDDO_4 | JP8 | Power supply voltage selector for Output 4 |
| 22 | Output 4 | J23, J24 | Differential clock output |
| 23 | Output 6 | J29, J30 | LP-HCSL differential clock output |
| 24 | USB Interface | J18 | Used for connection with the user's computer for interaction with the *IDT Timing Commander Software.* |
| 25 | Output 5 | J27, J28 | LP-HCSL differential clock output |
| 26 | VDDO Jack | J15 | VDD jack for external power supply |
| 27 | VDDO LP-HCSL Jack | J41 | VDD jack for VDDO_LP-HCSL (1.8V) external power supply. |

# 3. Board Power Supply

The voltage for each of the 4 VDDO pins can be selected with jumpers. In the 5-pin configuration, the center pin is connected to the VDDO pin on the 5P49V6967/68 device. The 4 pins around it are connected to different power sources. A jumper connects the VDDO pin to a power source of choice.

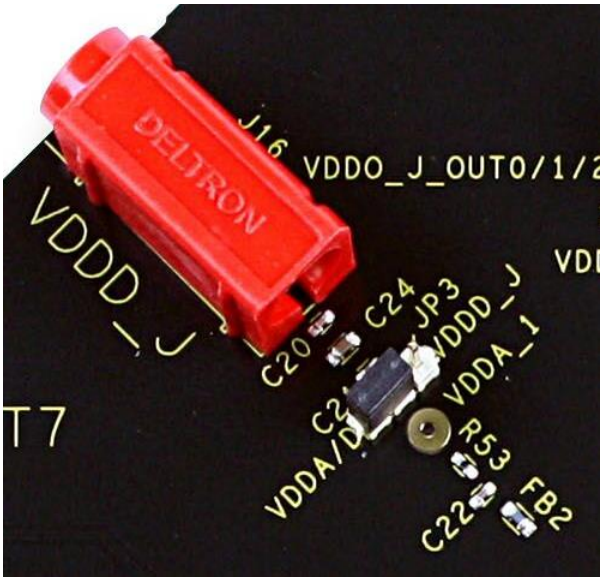
In Figure 3, the voltage for VDDO_1 is chosen to be 3.3V. Move the jumper to the right side to select 2.5V, to the bottom to select 1.8V, or to the left to select the VDDO_J Jack. The 3.3V, 2.5V, and 1.8V supplies are from on-board regulators that get their power from the USB connector. The VDD jacks are for connecting to a bench power supply.

**Figure 3. 5VDDO_1 Voltage Selector on the 5P49V6967 and 5P49V6968 EVBs**



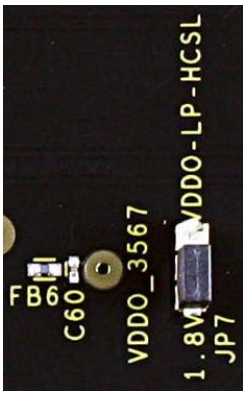

For both EVBs, JP3 selects the power source for the VDDA and VDDD pins: either an on-board 3.3V regulator or the VDDD_J jack for a bench power supply. In Figure 4, the source for VDDA and VDDD is chosen to be the on-board 3.3V regulator.

**Figure 4. VDDA/D Power Source Selector – 5P49V6967 EVB Example**



For both EVBs, JP7 selects the power source for the VDDO LP-HCSL pins between an on-board 1.8V regulator and the VDDO-LP-HCSL jack for a bench power supply. In Figure 5, the source for VDDO LP-HCSL is chosen to be the on-board 1.8V regulator.

**Figure 5. VDDO LP-HCSL Power Source Selector – 5P49V6967 EVB Example**



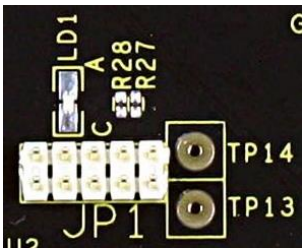

# 4. Connecting the Board to a Computer

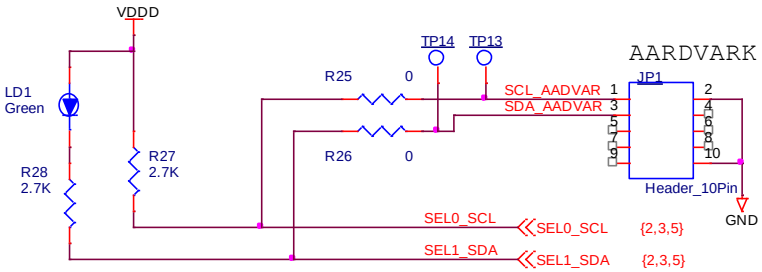
The Evaluation Board can be connected to a computer via the USB connector. The on-board USB-to-I2C bridge (FTDI chip) handles the data communication and the +5V in the USB bus powers the on-board regulators. Using a bench power supply with the VDD jacks is optional. The board can fully function with just the USB cable to a computer.

IDT's *Timing Commander Software* can control the 5P49V6967/68 on the board. *Timing Commander* is compatible with both the on-board USB-to-I2C bridge and the Aardvark adapter. *Timing Commander* displays a block diagram for entering the configuration and allows programming that configuration into the 5P49V6967 or 5P49V6968 on the board. *Timing Commander* handles defining the proper hex-code sequence to program into the device.

The Aardvark adapter can be plugged into JP1 as shown in Figure 6. In this case, also connect the USB port to a computer to power the FTDI chip so it does not load the SDA and SCL lines. With the USB cable connected to a computer, the USB can be used to power the 5P49V6967 or 5P49V6968 EVB as well.

**Figure 6. Aardvark Connector on the 5P49V6967 and 5P49V6968 EVBs**

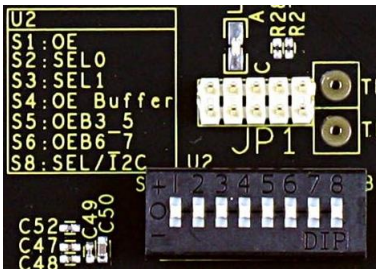


# 5. Functions of the U2 Switches on the 5P49V6967

On the 5P49V6967, the switch block U2 has 8 switches. Only 7 of the switches are used.

**Figure 7. U2 Switches on the 5P49V6967**




The switches connect to pins on the 5P49V6967 device. The middle position leaves the pin open. This is the default for each switch. Move to the "+" side to pull the pin HIGH and move to the "–" side to pull the pin LOW.

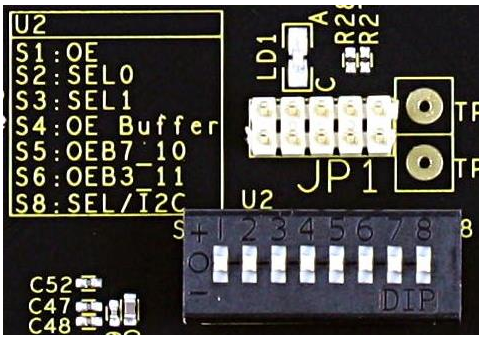
**Table 3. Functions of U2 Switches on the 5P49V6967**

| Switch | Name | Function |
|---|---|---|
| 1 | OE | Connects to the SD/OE pin for Output Enable or Shut-Down operation. |
| 2 | SEL0 | Connects to the SEL0/SCL pin. The main purpose of this switch is to operate SEL0 when the device has started in Hardware Select Mode. This switch can also be used to add an extra pull-up (10KΩ) on the SCL line for I2C operation. |
| 3 | SEL1 | Connects to the SEL1/SDA pin. The main purpose of this switch is to operate SEL1 when the device has started in Hardware Select Mode. This switch can also be used to add an extra pull-up (10KΩ) on the SDA line for I2C operation. |
| 4 | OE Buffer | Connects to the OE Buffer pin to enable/disable only the LP-HCSL outputs. |
| 5 | $OEB_{3,5}$ | Connects to the $OEB_{3,5}$ pin to enable/disable only outputs 3 and 5. |
| 6 | $OEB_{6,7}$ | Connects to the $OEB_{6,7}$ pin to enable/disable only outputs 6 and 7. |
| 7 | | Unused. |
| 8 | | Pulls on the OUT0_SELB_I2C pin on the device to select the operation mode at power up. The state of the OUT0_SELB_I2C pin is latched at power up. The operation mode effectively sets the function of the SEL0/SCL and SEL1/SDA pins. The OUT0_SELB_I2C pin has an on-chip pull-down so switch 8 in the center or "–" position has the same effect and results in startup with the I2C Mode. In I2C Mode, the two pins have the SDA and SCL function for I2C operation. With the switch in the "+" position, the device will start in Hardware Select Mode. In Hardware Select Mode, the two pins have the SEL0 and SEL1 function for selecting a preprogrammed configuration. |

# 6. Functions of the U2 Switches on the 5P49V6968

On the 5P49V6968, the switch block U2 has 8 switches. Only 7 of the switches are used.

**Figure 8. U2 Switches on the 5P49V6968**




The switches connect to pins on the 5P49V6968 device. The middle position leaves the pin open. This is the default for each switch. Move to the "+" side to pull the pin HIGH and move to the "–" side to pull the pin LOW.

**Table 4. Functions of U2 Switches on the 5P49V6968**

| Switch | Name | Function |
|---|---|---|
| 1 | OE | Connects to the SD/OE pin for Output Enable or Shut-Down operation. |
| 2 | SEL0 | Connects to the SEL0/SCL pin. The main purpose of this switch is to operate SEL0 when the device has started in Hardware Select Mode. This switch can also be used to add an extra pull-up (10KΩ) on the SCL line for I2C operation. |
| 3 | SEL1 | Connects to the SEL1/SDA pin. The main purpose of this switch is to operate SEL1 when the device has started in Hardware Select Mode. This switch can also be used to add an extra pull-up (10KΩ) on the SDA line for I2C operation. |
| 4 | OE Buffer | Connects to the OE Buffer pin to enable/disable only the LP-HCSL outputs. |
| 5 | $OEB_{7\_10}$ | Connects to the $OEB_{7\_10}$ pin to enable/disable only outputs 7, 8, 9 and 10. |
| 6 | $OEB_{3\_11}$ | Connects to the $OEB_{3\_11}$ pin to enable/disable only outputs 3, 5, 6 and 11. |
| 7 | | Unused. |
| 8 | | Pulls on the OUT0_SELB_I2C pin on the device to select the operation mode at power up. The state of the OUT0_SELB_I2C pin is latched at power up. The operation mode effectively sets the function of the SEL0/SCL and SEL1/SDA pins. The OUT0_SELB_I2C pin has an on-chip pull-down so switch 8 in the center or "–" position has the same effect and results in startup with the I2C Mode. In I2C Mode, the two pins have the SDA and SCL function for I2C operation. With the switch in the "+" position, the device will start in Hardware Select Mode. In Hardware Select Mode, the two pins have the SEL0 and SEL1 function for selecting a preprogrammed configuration. |

# 7. Operating Modes

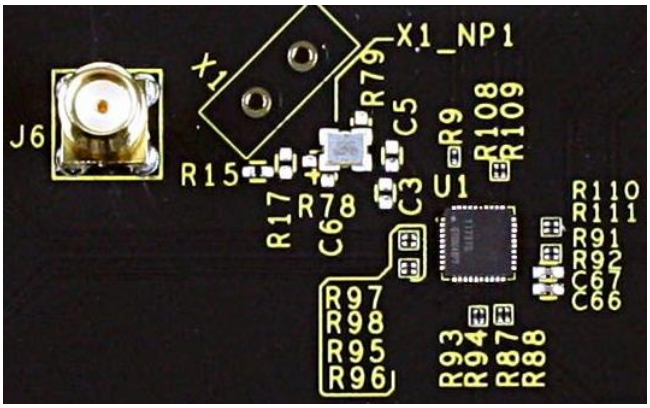
As explained above at switch 8, the 5P49V6967/68 can start up in two different operating modes: I2C Mode or Hardware Select Mode. The Evaluation Board is shipped with a "blank" 5P49V6967/68 device, without a configuration preprogrammed into the one-time-programmable (OTP) memory. Without a configuration preprogrammed, the Hardware Select Mode cannot be used. The "blank" device will start with a default or "test" configuration where output 0 and output 1 are enabled. Output 0 will be 25MHz and output 1 will be 100MHz with LVCMOSD logic. Next, *Timing Commander* can be used to program a configuration into the volatile registers in the device to test a configuration. This works without "burning" the permanent OTP memory, and most users of this Evaluation Board do not burn the OTP. This way the board can be used repeatedly to test configurations. Burning configurations into OTP is only useful when studying the Hardware Select Mode and the transition from one configuration to another.

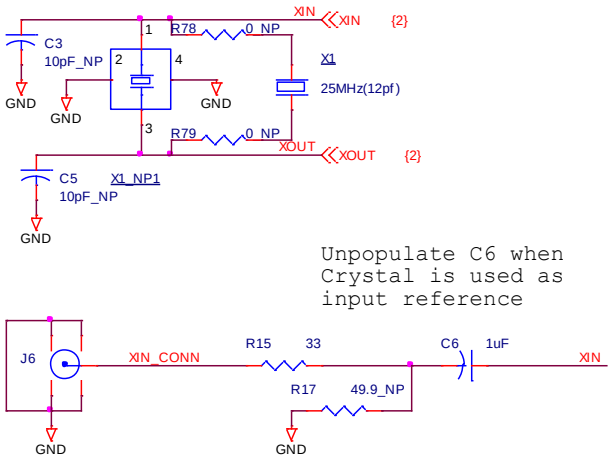
**Important Note:** Burning configurations into the OTP is permanent and cannot be undone.

# 8. On-Board Crystal

A 25MHz crystal (X1_NP) is installed on the 5P49V6967/68 Evaluation Board. Figure 9 shows the location on the board and the schematic for the 5P49V6967 EVB. Refer to Figure 15 for the schematic for the 5P49V6968 EVB.

**Figure 9. Crystal Circuit – 5P49V6967 EVB Example**




The board is shipped with a small 25MHz SMD crystal installed. The crystal can be replaced with a different frequency if needed.

**Note:** The output 1 with the default or "test" mode will only work when using a 25MHz crystal.

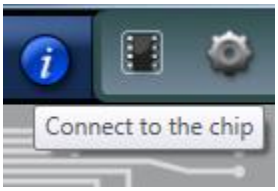
A thru-hole crystal can be assembled in the X1 position. In this case, remove the small 25MHz crystal and also assemble the resistors R78 and R79 to connect the thru-hole crystal.

Another useful modification can be to remove the 25MHz crystal and assemble C6 to connect the SMA connector J6. Now a clock from a generator or other source can be used to drive the XIN pin. In this case, also assemble R17 when termination of the external clock is needed. See the requirements for the XIN amplitude in the *5P49V6967/68 Datasheet.* Essentially, the amplitude on XIN should not exceed 1.2Vpp. Recommendation: Use 1.0Vpp for most tests. When doing phase noise measurements of the output clocks, use a very low noise clock for XIN. The best phase noise at the outputs is achieved when using a crystal. Only the very best of low noise RF signal generators connected to XIN can result in the same phase noise performance.

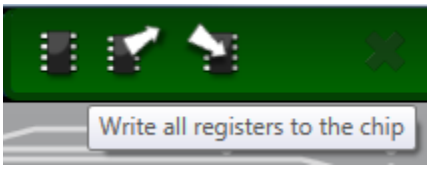
# 9. Configuration and Setup

Use the following steps to setup the 5P49V6967/68 EVB using I2C and start the configuration of the board.

1. Set the SEL switch (switch 8) of the U2 dip switch bank to "O" to select I2C Mode.
2. Connect J18 to a USB port of the user's computer using the USB cable supplied with the board.
3. Launch IDT's *VersaClock 6E Timing Commander Software* according to the instructions in the *VersaClock 6E Timing Commander User Guide*. The software and guide can be downloaded on the product pages:
   - www.IDT.com/5P49V6967
   - www.IDT.com/5P49V6968
4. Following the "Getting Started" steps in the *Timing Commander Software*, an I2C connection is established between the GUI software and the VersaClock 6E 5P49V6967/68.
5. Select "Open Settings File" to use existing settings, or select "New Settings File" and choose 5P49V6967 or 5P49V6968 depending on the Evaluation Board. On the same screen, browse for a personality file to be used with the Evaluation Board by clicking on the button at the bottom right.
6. Connect to the EVB by clicking on the microchip icon located at the top right of the *Timing Commander* screen.



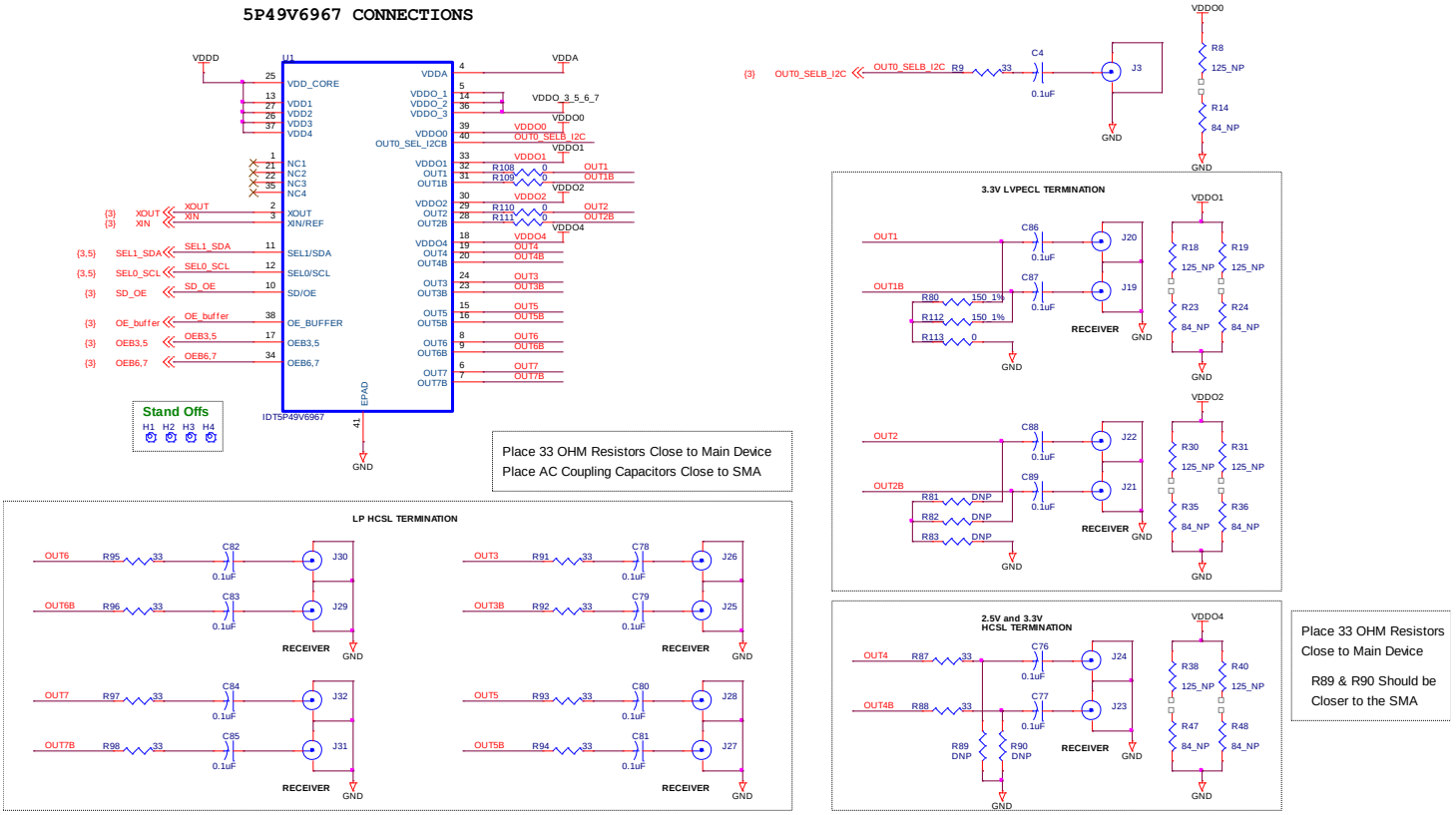

7. Once the EVB is connected, new options will be available on a green background indicating that the EVB has successfully connected with the board. Write settings to the chip by clicking on the "Write all registers to the chip" option.



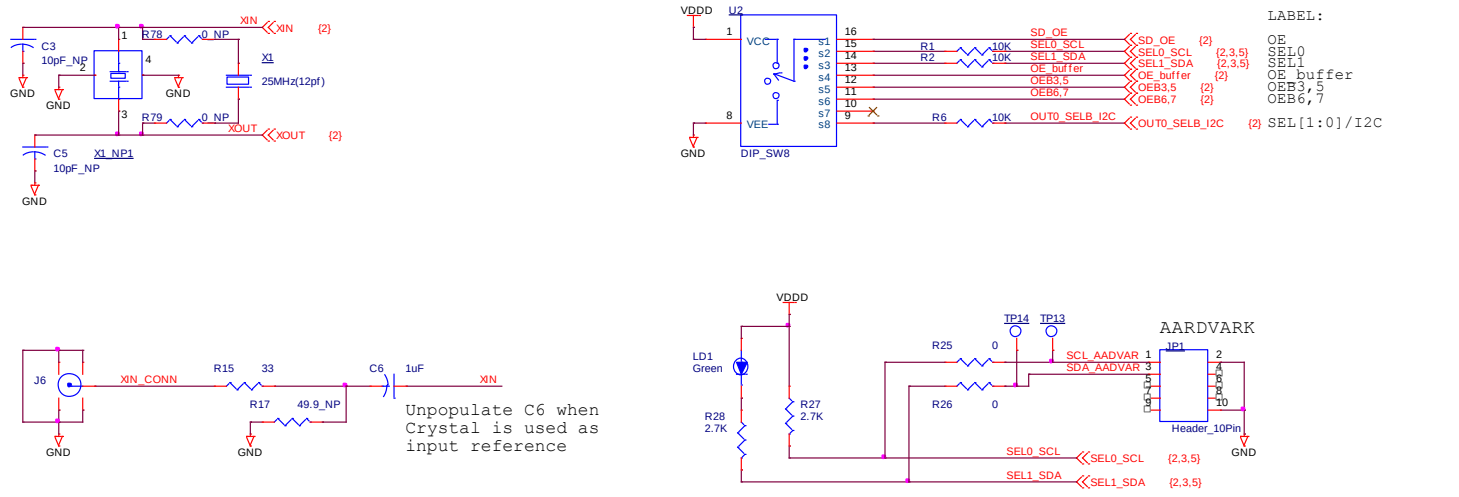

8. All enabled outputs should now be available for measurement.

# 10. Board Schematics

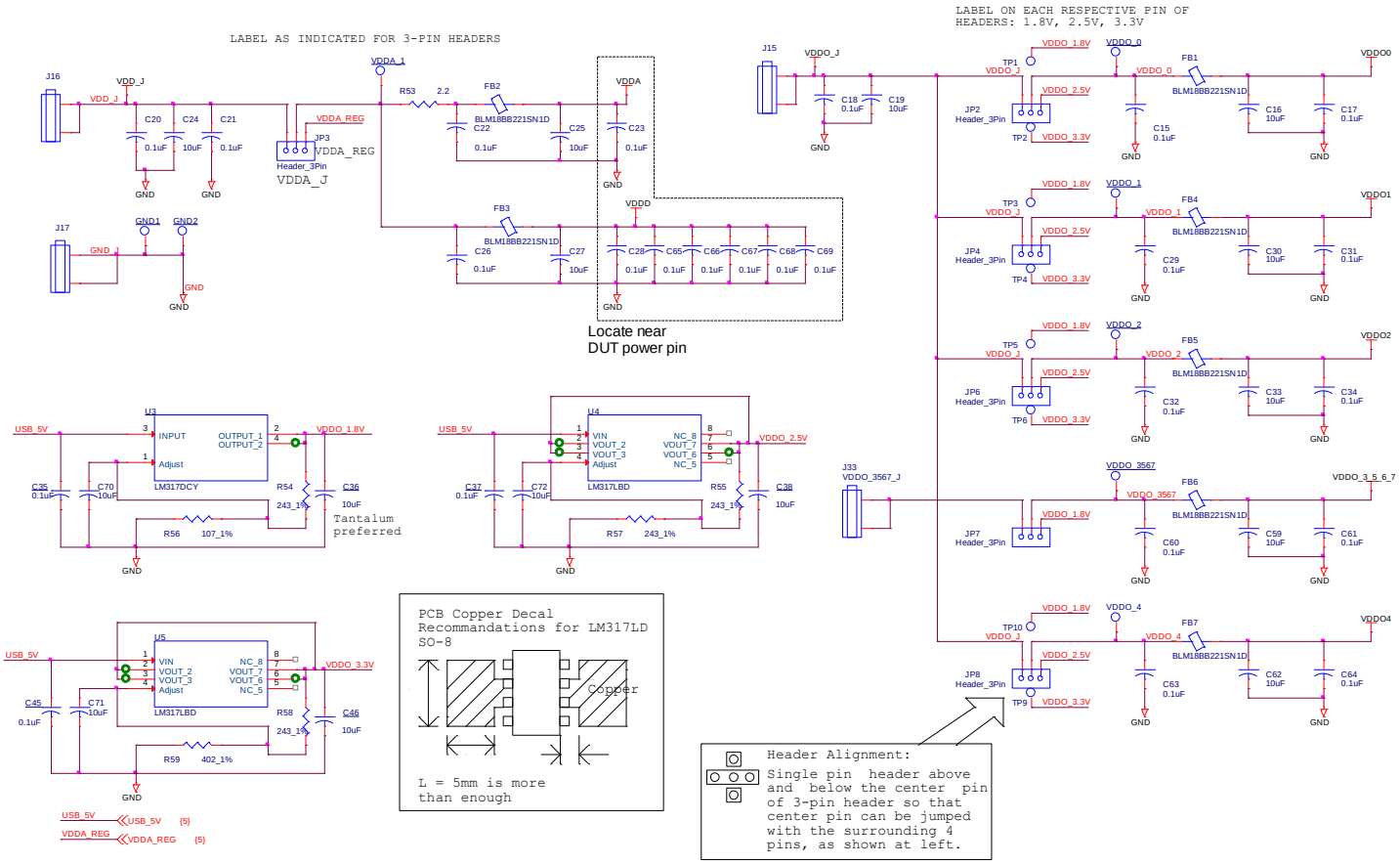
## Figure 10. 5P49V6967 Evaluation Board Schematics – Page 1



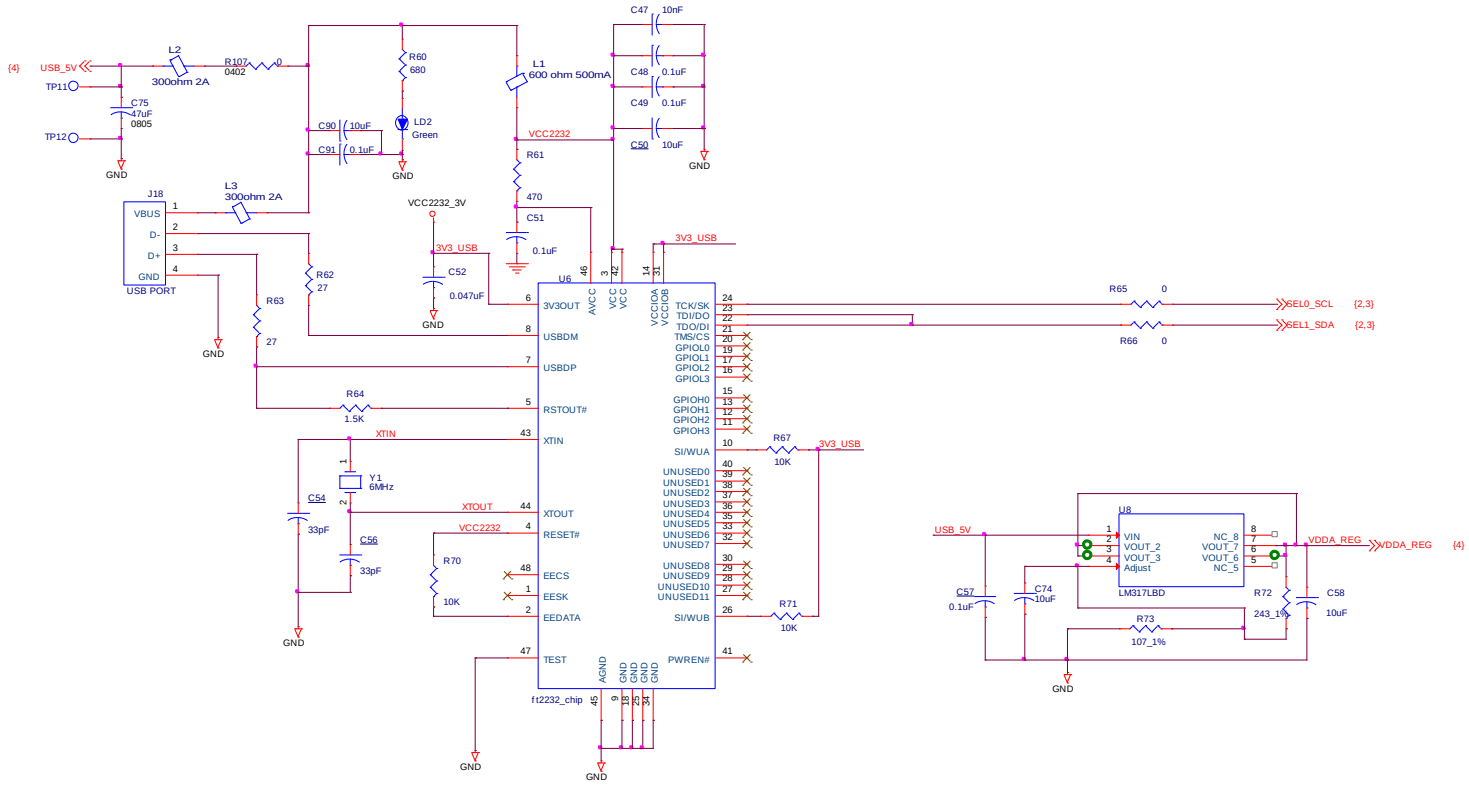

## Figure 11. 5P49V6967 Evaluation Board Schematics – Page 2



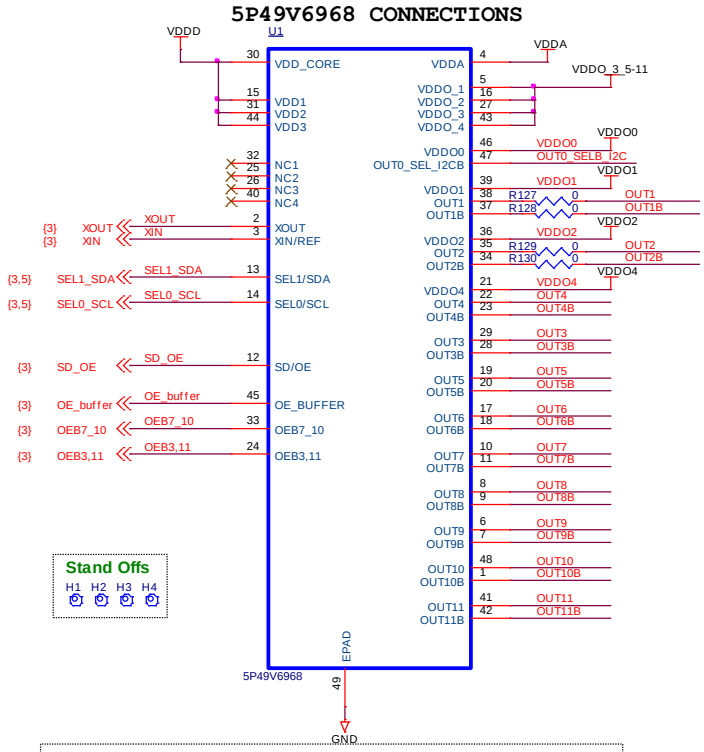
## Figure 12. 5P49V6967 Evaluation Board Schematics – Page 3



## Figure 13. 5P49V6967 Evaluation Board Schematics – Page 4

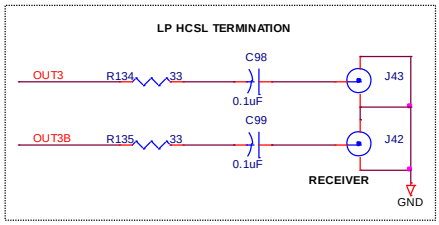


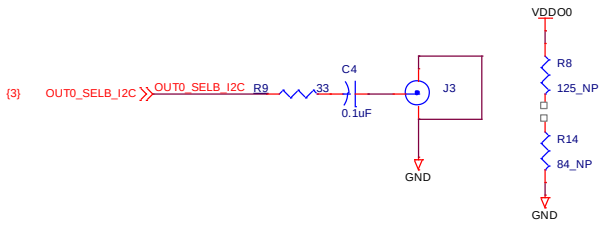
## Figure 14. 5P49V6968 Evaluation Board Schematics – Page 1

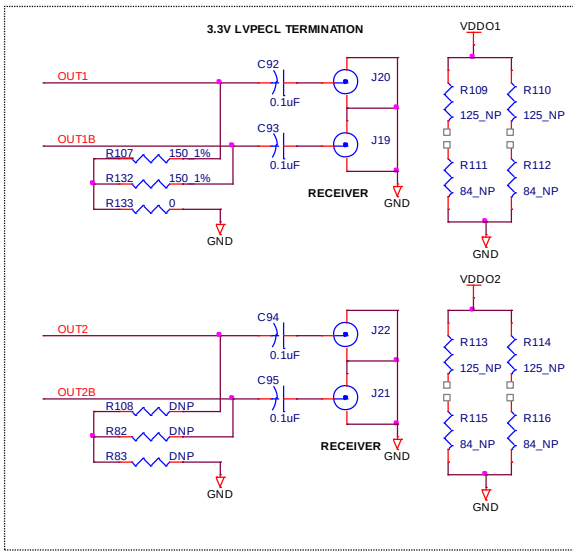


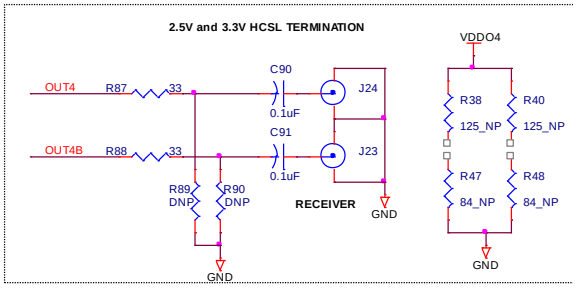

Place 33 OHM Resistors Close to Main Device For LP HCSL TERMINATION
Place AC Coupling Capacitors Close to SMA

Place R87 & R88 33 OHM Resistors Close to Main Device For HCSL TERMINATION
R89 & R90 Should be Closer to the SMA

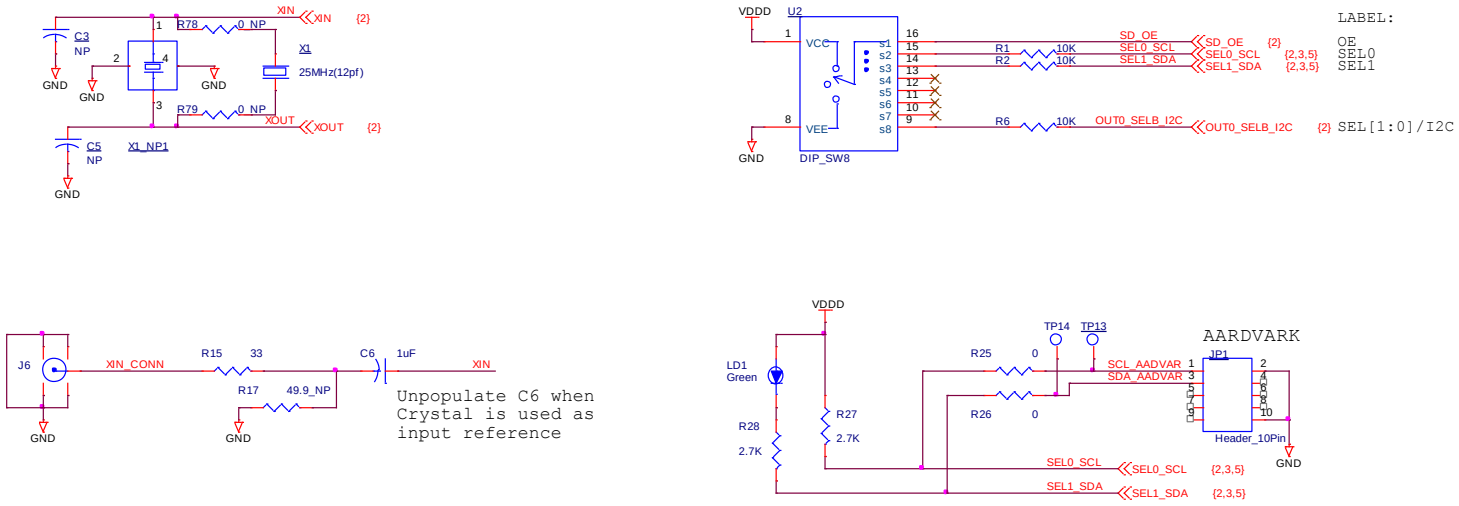


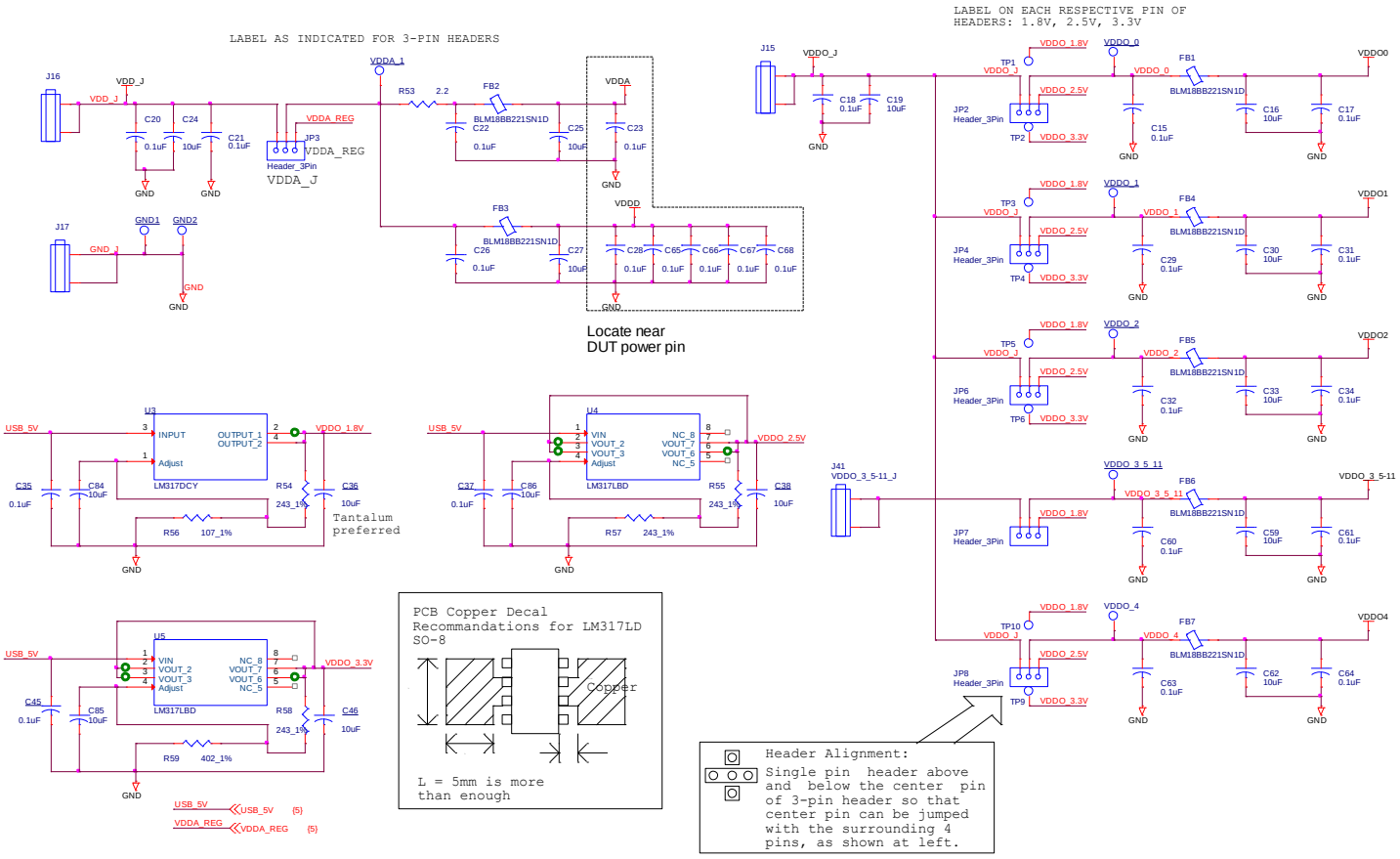



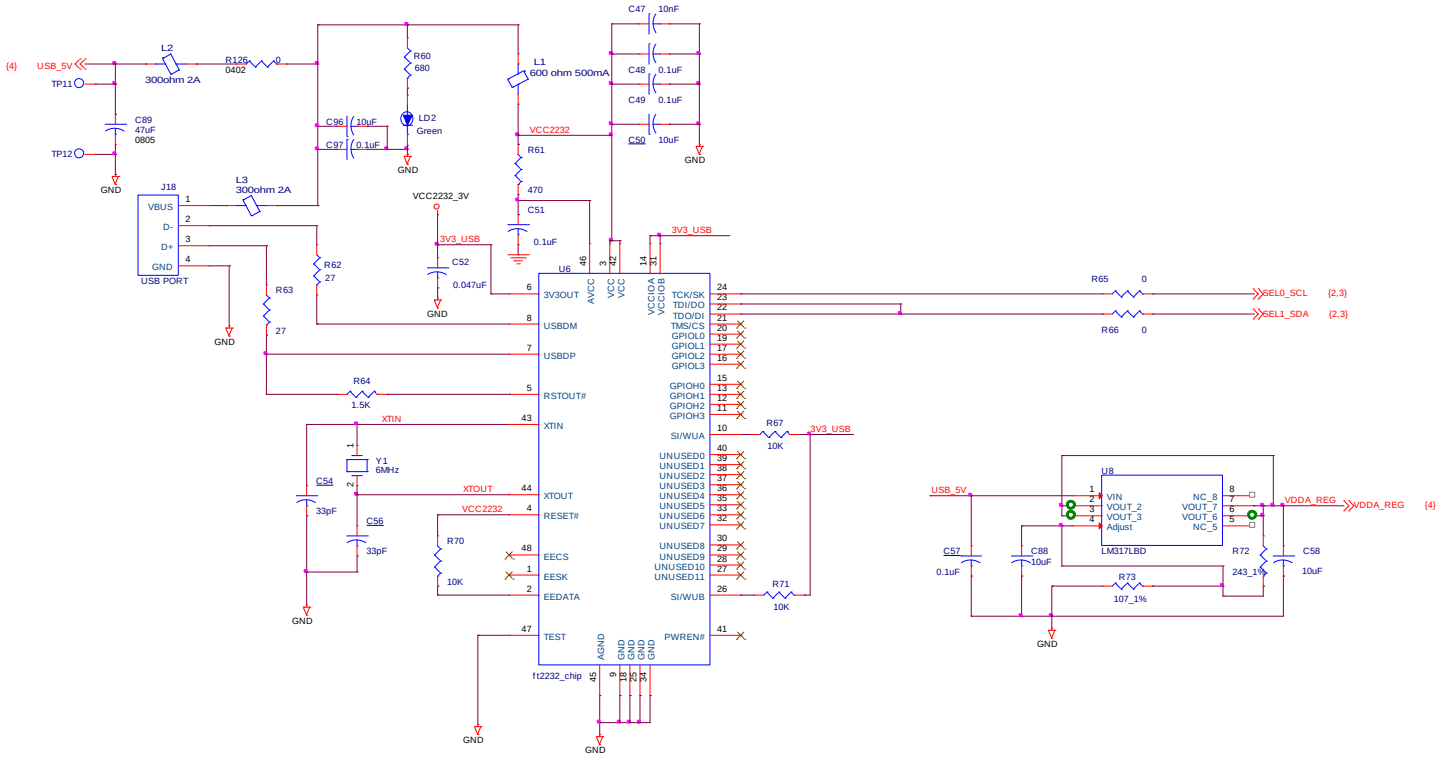
## Figure 15. 5P49V6968 Evaluation Board Schematics – Page 2




## Figure 16. 5P49V6968 Evaluation Board Schematics – Page 3



## Figure 17. 5P49V6968 Evaluation Board Schematics – Page 4

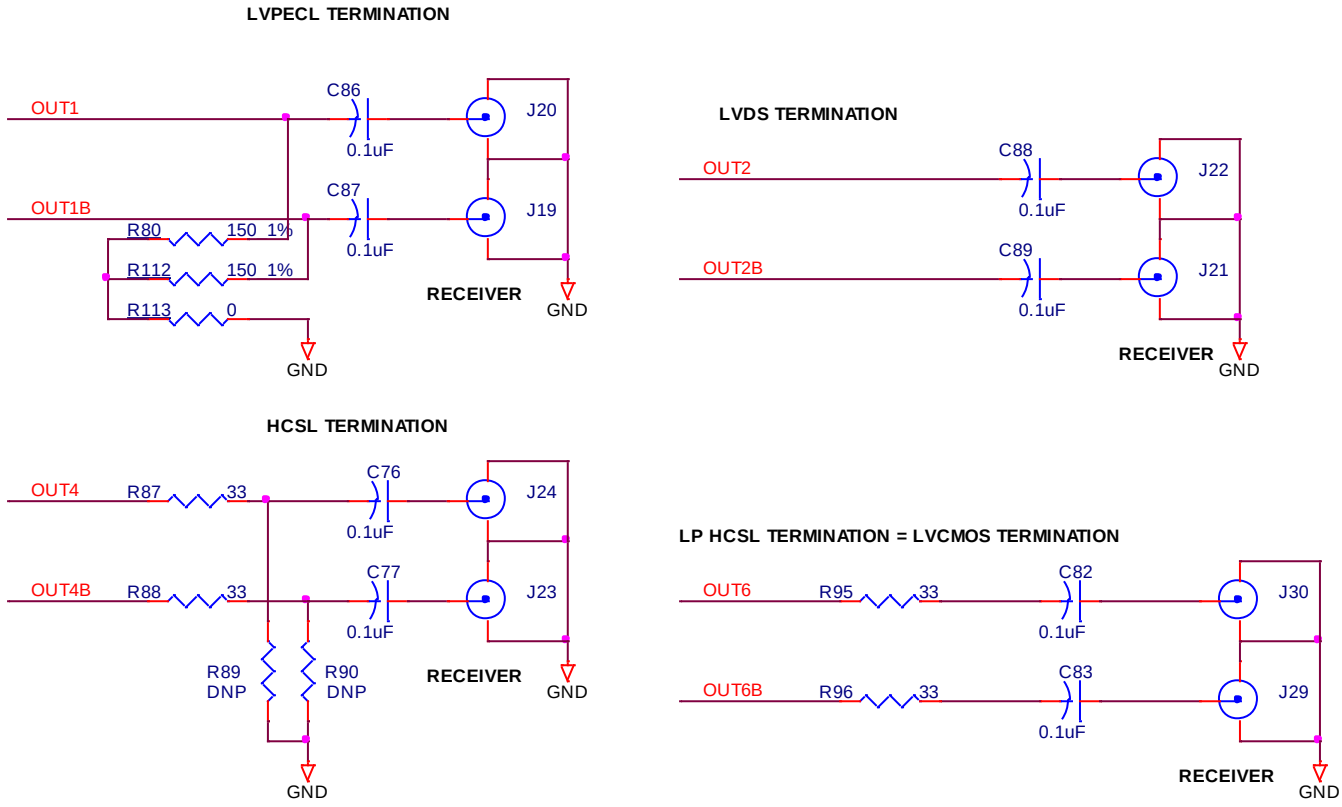


# 11. Signal Termination Options

Termination options for OUTPUT 1 – 4 for the 5P49V6967/68 Evaluation Board are shown in Figure 18. The termination circuits are designed to optionally terminate the output clocks in LVPECL, LVDS, LVCMOS and HCSL signal types by populating (or not-populating) some resistors. DC or AC coupling of these outputs is also supported.

Table 4 through Table 9 define the components that must be installed to support LVPECL, HCSL, LVCMOS and LVDS signal types for OUTPUT1 – 4 on the 5P49V6967/68 EVB. Note that with the specified components the output signals should be measured and terminated by test equipment with a 50Ω internal termination.

**Figure 18. 5P49V6967/68 Output Termination Options**



## 11.1 Termination Options for the 5P49V6967 Board

Note: In the tables in this section, the components given for the HCSL termination scheme are the default configuration of the Evaluation Board. This scheme allows quick measurements of every logic type without modification of the Evaluation Board. When using the unmodified board with equipment with AC coupled inputs, such as a spectrum analyzer or phase noise test set, use a 3dB or 6dB attenuator to facilitate a DC path to ground to allow the output driver to toggle. This is only needed with LVPECL and HCSL logic.

**Table 5. 5P49V6967 Termination Options for OUTPUT1**

| Signal Type | Series Resistors: R108, R109 | 150Ω Pull-Down: R80, R112, R113 | Series Capacitor: C86, C87 |
|---|---|---|---|
| LVPECL | 0Ω | Installed (see Figure 18) | 0.1µF |
| HCSL | 33Ω | Not installed | 0Ω (short) |
| LVCMOS | 33Ω | Not installed | 0.1µF |
| LVDS | 0Ω | Not installed | 0.1µF |

**Table 6. 5P49V6967 Termination Options for OUTPUT2**

| Signal Type | Series Resistors: R110, R111 | 150Ω Pull-Down: R81, R82, R83 | Series Capacitor: C88, C89 |
|---|---|---|---|
| LVPECL | 0Ω | Installed (see Figure 18) | 0.1µF |
| HCSL | 33Ω | Not installed | 0Ω (short) |
| LVCMOS | 33Ω | Not installed | 0.1µF |
| LVDS | 0Ω | Not installed | 0.1µF |

**Table 7. 5P49V6967 Termination Options for OUTPUT4**

| Signal Type | Series Resistors: R87, R88 | 150Ω Pull-Down: R89, R90 | Series Capacitor: C76, C77 |
|---|---|---|---|
| LVPECL | 0 Ω | Installed (see Figure 18) | 0.1µF |
| HCSL | 33Ω | Not installed | 0Ω (short) |
| LVCMOS | 33Ω | Not installed | 0.1µF |
| LVDS | 0Ω | Not installed | 0.1µF |

## 11.2 Termination Options for the 5P49V6968 Board

Note: In the tables in this section, the components given for the HCSL termination scheme are the default configuration of the Evaluation Board. This scheme allows quick measurements of every logic type without modification of the Evaluation Board. When using the unmodified board with equipment with AC coupled inputs, such as a spectrum analyzer or phase noise test set, use a 3dB or 6dB attenuator to facilitate a DC path to ground to allow the output driver to toggle. This is only needed with LVPECL and HCSL logic.

**Table 8. 5P49V6968 Termination Options for OUTPUT1**

| Signal Type | Series Resistors: R127, R128 | 150Ω Pull-Down: R107, R132, R133 | Series Capacitor: C92, C93 |
|---|---|---|---|
| LVPECL | 0 Ω | Installed (see Figure 18) | 0.1µF |
| HCSL | 33Ω | Not installed | 0Ω (short) |
| LVCMOS | 33Ω | Not installed | 0.1µF |
| LVDS | 0Ω | Not installed | 0.1µF |

**Table 9. 5P49V6968 Termination Options for OUTPUT2**

| Signal Type | Series Resistors: R129, R130 | 150Ω Pull-Down: R108, R82, R83 | Series Capacitor: C94, C95 |
|---|---|---|---|
| LVPECL | 0 Ω | Installed (see Figure 18) | 0.1µF |
| HCSL | 33Ω | Not installed | 0Ω (short) |
| LVCMOS | 33Ω | Not installed | 0.1µF |
| LVDS | 0Ω | Not installed | 0.1µF |

**Table 10. 5P49V6968 Termination Options for OUTPUT4**

| Signal Type | Series Resistors: R87, R88 | 150Ω Pull-Down: R89, R90 | Series Capacitor: C90, C91 |
|---|---|---|---|
| LVPECL | 0 Ω | Installed (see Figure 18) | 0.1µF |
| HCSL | 33Ω | Not installed | 0Ω (short) |
| LVCMOS | 33Ω | Not installed | 0.1µF |
| LVDS | 0Ω | Not installed | 0.1µF |

# 12. Ordering Information

| Orderable Part Number | Description |
|---|---|
| 5P49V6967-EVK | 5P49V6967 Evaluation Board; A-male to B-male USB cable. |
| 5P49V6968-EVK | 5P49V6968 Evaluation Board; A-male to B-male USB cable. |

# 13. Revision History

| Revision Date | Description of Change |
|---|---|
| January 15, 2018 | Initial release. |

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