DA1459x

Pro-Development Kit

This document explains the DA1459x Development Kit Pro hardware which provides a tested reference platform, access to all signals for connecting peripherals and advanced debugging features.

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1. Terms and Definitions

LPF	Low Pass Filter
PCB	Printed Circuit Board
Pro DevKit	Professional Development Kit
Pro-MB	Professional Motherboard
Pro-DB	Professional Daughterboard
SDK	Software Development Kit
SoC	System on Chip
SWD	Serial Wire Debug

2. References

[1] DA1459x, Datasheet, Renesas Electronics

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

This document describes the hardware of DA1459x Pro Development Kit (Pro DevKit). The DA1459x Pro DevKit is available as a motherboard, two variants of a daughterboard (FCQFN52/WLCSP39) and the power measurement module PMM2, Figure 1.

When combined with the DA1459x SDK and SmartSnippets tools, the Pro DevKit provides an easy to use and complete platform for software/hardware development.

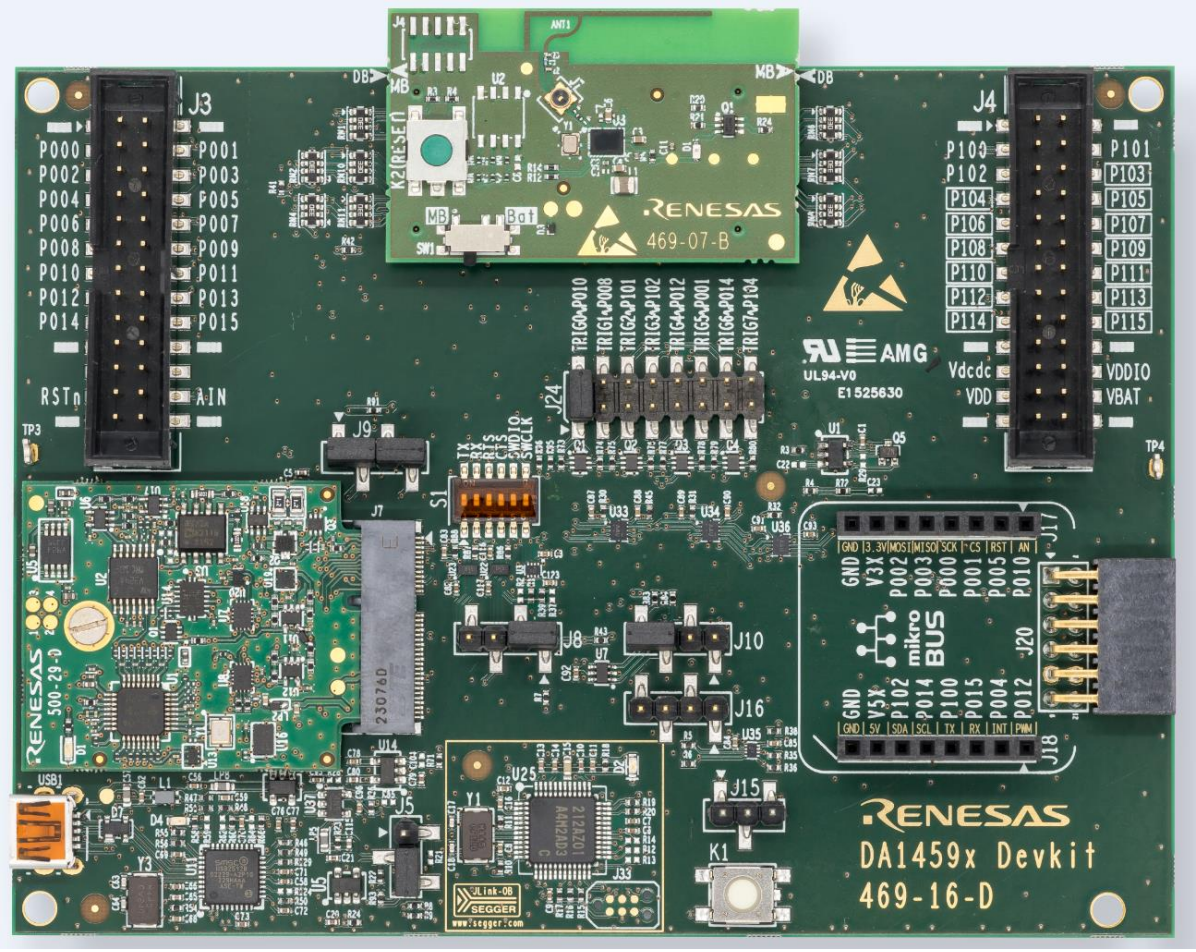


Figure 1. DA1459x Pro DevKit with Pro-motherboard and Pro-daughterboard

3.1 Features of DA1459x Pro-Daughterboard

- Embedded printed antenna
- Coaxial switch for conducted RF measurements
- Option for QSPI-Flash memory or PSRAM
- Reset button
- LED
- Flexible battery options
- Crystals 32 MHz, 32.768 kHz (optional – only for FCQFN52 package)
- Support for coin cell battery.

3.2 Features of DA1459x Pro-Motherboard

- Mating connectors for connecting a DA1459x Pro-daughterboard which hosts either DA1459x FCQFN52 or WLCSP39 SoC
- Headers for I/O monitoring and expandability

- Option to support MikroBUS click boards
- Provisions for automated test
- On-board basic peripherals for demo and development
- JTAG(SWD) debugger and connectivity to PC.

3.3 Pro DevKit Hardware Block Diagram

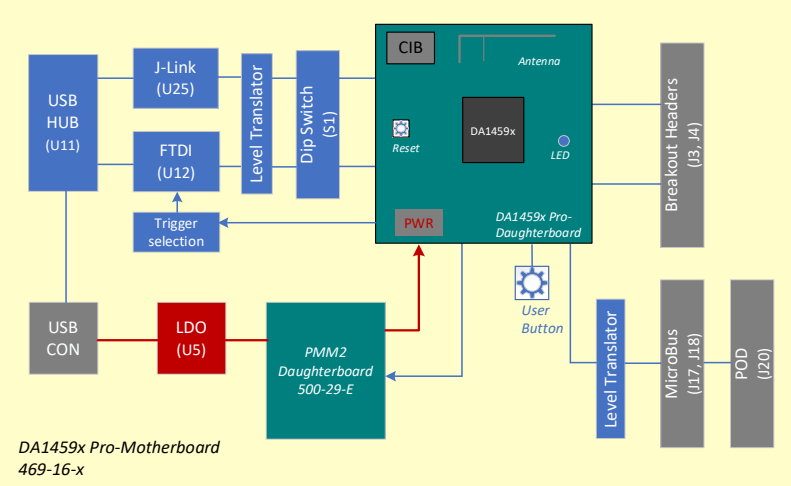


Figure 2. System block diagram

4. Getting to Know DA1459x Pro DevKit

4.1 The Hardware Components of the DA1459x Pro DevKit

In this document we focus on the DA1459x Pro DevKit which consists of the following parts:

- Pro-Motherboard, DA1459x Pro-motherboard: PCBA reference number 469-16-D.
- Pro-Daughterboard (two options, interchangeable).
  - FCQFN52 Pro-daughterboard: it uses DA1459x -FCQFN52. PCBA reference number 469-08-B.
  - WLCSP39 Pro-daughterboard: it uses DA1459x-WLCSP39. PCBA reference number 469-07-B.
- Power measurement module, PMM2. PCBA reference number 500-29-E.

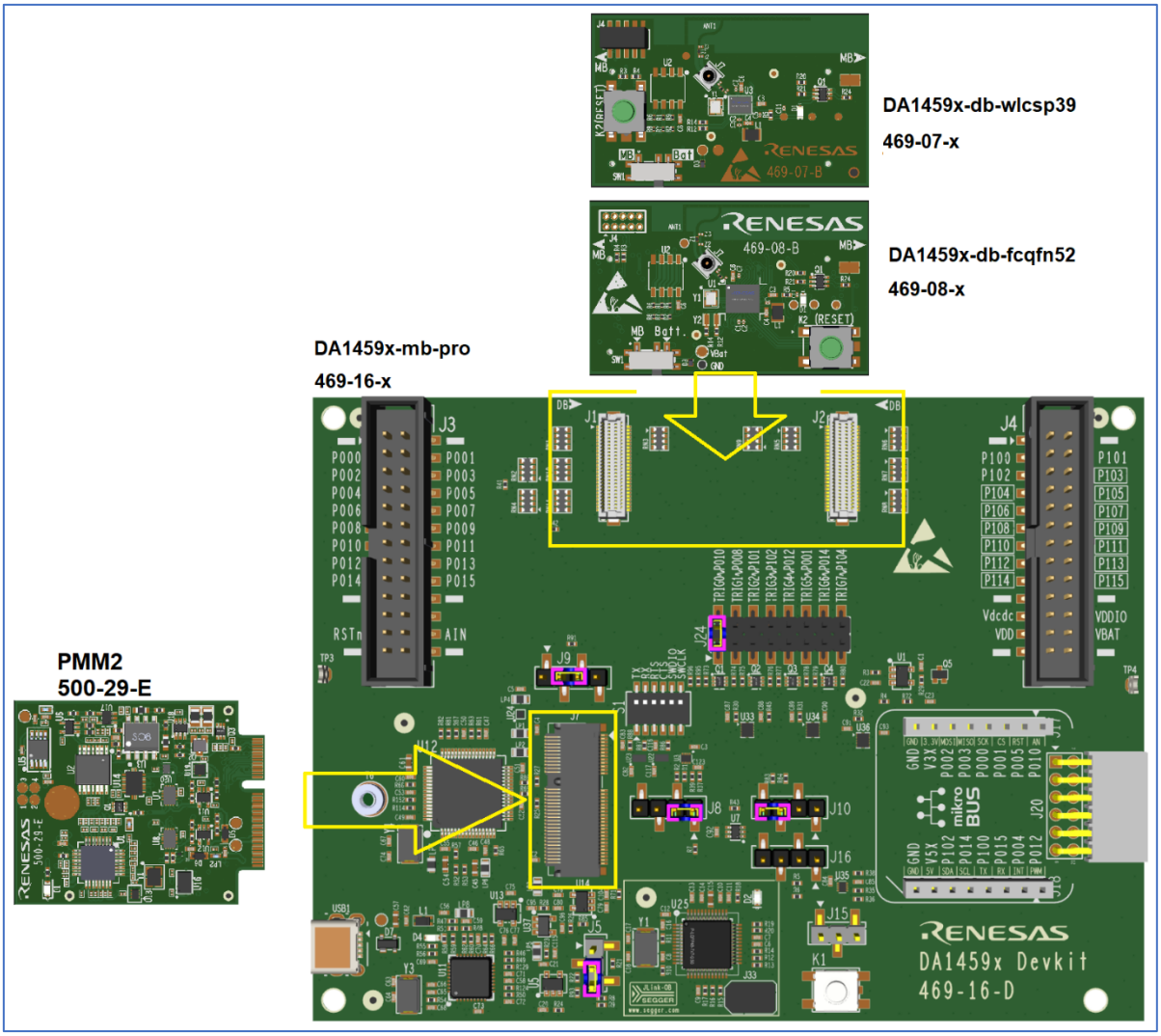


Figure 3. DA1459x Pro DevKit components

4.1.1 Set Up Hardware of DA1459x DevKit with PMM2

1. Mount Pro-Daughterboard (469-08-x or 469-07-x). Ensure the proper orientation, by checking the alignment marks of the two PCBAs.
2. Mount PMM2 as shown in Figure 4. The mounting screw (M2x4, D5x0.5 or similar) must be also applied.
3. Mount two jumpers on J9, between pins 1-2 and pins 3-4.

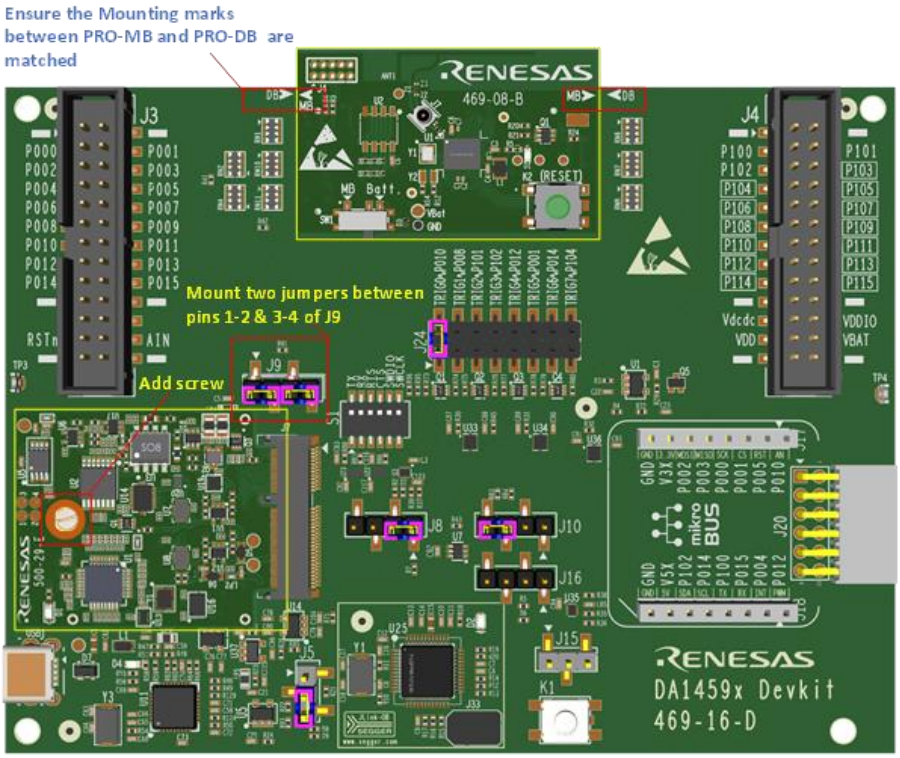


Figure 4. Default hardware setup of DA1459x Pro DevKit with PMM2

4.1.2 Set Up Hardware of DA1459x DevKit without PMM2

1. Mount Pro-Daughterboard (469-08-x or 469-07-x). Ensure the proper orientation by checking the alignment marks of the two PCBAs.
2. Mount one jumper on J9, between pins 2 and 3.

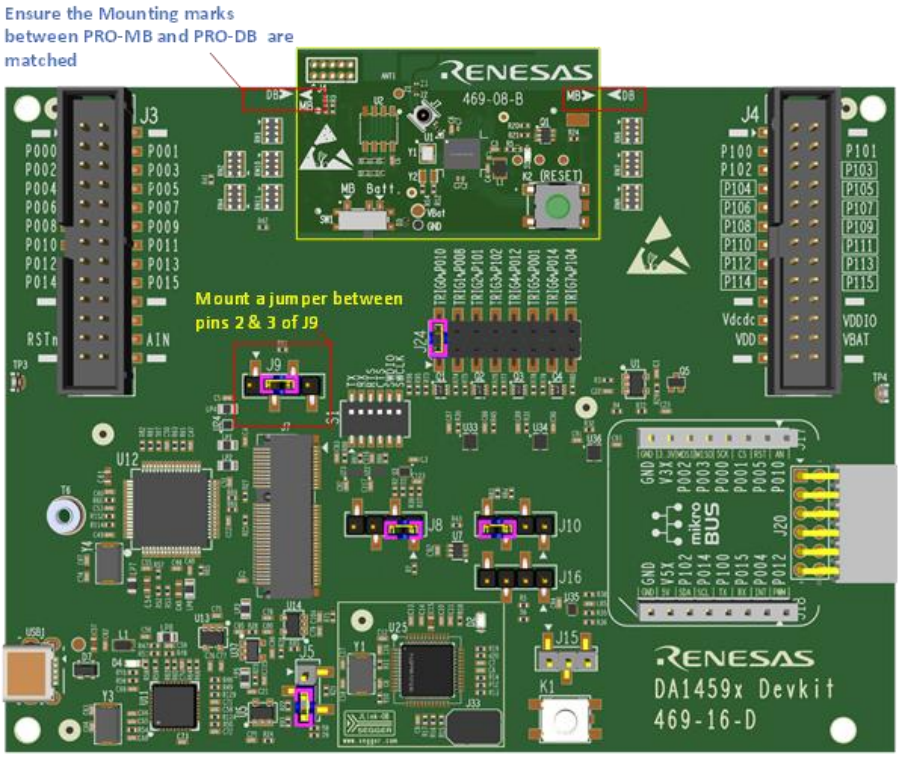


Figure 5. Hardware setup of DA1459x Pro DevKit without PMM2

4.1.3 Jumper Settings

Table 1. Headers and jumper settings of DA1459x Pro DevKit

HDR	Function of headers	Jumper options		Default jumper setting
J5	DA1459x input voltage, generated from LDO (U5)	1.8 V	Mount pos. 1-2 Or No mount 1-2	Mounted 2-3
		3.0 V	Mount pos. 2-3	
J8	K1, general purpose push button and (pins 1-2) Force enable Power_Enable (3-4), for supplying Pro DevKit with a power source without USB data connection	Enable K1	Mount pos. 1-2	Mounted 1-2
		Force Power_Enable	Mount pos. 3-4	No mounted 3-4
J9	Power Measurement Module PMM2	PMM2 Bypass	Mount pos. 2-3	*PMM2 mounted:* Mounted 1-2 Mounted 3-4 *PMM2 no mounted:* Mounted 2-3
		PMM2 Enable	Mount pos.1-2 Mount pos. 3-4	
J10	Reset source options	Activate Reset driven from serial interface (U_RSTn)	Mount pos.1-2	Not mounted 1-2
		Activate Reset driven from Debugger (T_Reset)	Mount pos. 3-4	Mounted 3-4
J15	Enable Pullups of I2C for PMOD and MikroBUS	Disable I2C	No jumper Mount	-
		Power Pull-ups with 3.3 V	Mount pos.1-2	No mounted 1-2
		Power Pull-ups with 5 V	Mount pos.2-3	No mounted 3-4
J16	Enable I2C signals for PMOD and MikroBUS	Enable SDA	Mount pos.1-2	No mounted 1-2
		Enable SCL	Mount pos.3-4	No mounted 3-4
J24	Software Trigger activation	TRIG_0 mapped to P0_10 TRIG_1 mapped to P0_08 TRIG_2 mapped to P1_01 TRIG_3 mapped to P1_02 TRIG_4 mapped to P0_12 TRIG_5 mapped to P0_01 TRIG_6 mapped to P0_14 TRIG_7 mapped to P1_04	Mount pos.1-2 Mount pos.3-4 Mount pos.5-6 Mount pos.7-8 Mount pos. 9-10 Mount pos.11-12 Mount pos.13-14 Mount pos.15-16	Mounted 1-2

For enabling I2C for MikroBUS or PMOD, both J15 and J16 must be set.

4.2 DA1459x Pro-Daughterboard

On Pro-daughterboard, system consists of DA1459x SoC, crystals 32 MHz and 32 kHz (for FCQFN52 package only)), Switch SW1 for power source selection, radio section (printed antenna and RF connector), LED and RESET button (Figure 6). There are two versions of the DA1459x SoC, WLCSP39 and FCQFN52 with the ordering information in Table 2.

Table 2. DA1459x ordering information

Part number	Package	Size (mm)
DA14592-01000O92	WLCSP39	3.32 x 2.48 x 0.37
DA14592-010006F2	FCQFN52	5.1 x 4.3 x 0.78
DA14594-00000O92	WLCSP39	3.32 x 2.48 x 0.37
DA14594-000006F2	FCQFN52	5.1 x 4.3 x 0.78

There are two variants of Pro-daughterboard (Figure 7):

- for the FCQFN52 package (469-08-x)
- for the WLCSP39 package (469-07-x).

The difference between the two daughterboards, apart from layout differences, is that the FCQFN52 daughterboard exposes more GPIOs to the motherboard and provides a place holder for a 32 kHz crystal. Both variants provide a place holder for external Flash.

On the power section, both variants provide a place holder for a coin cell battery. DA1459x SoC can be supplied from the battery through switch SW1.

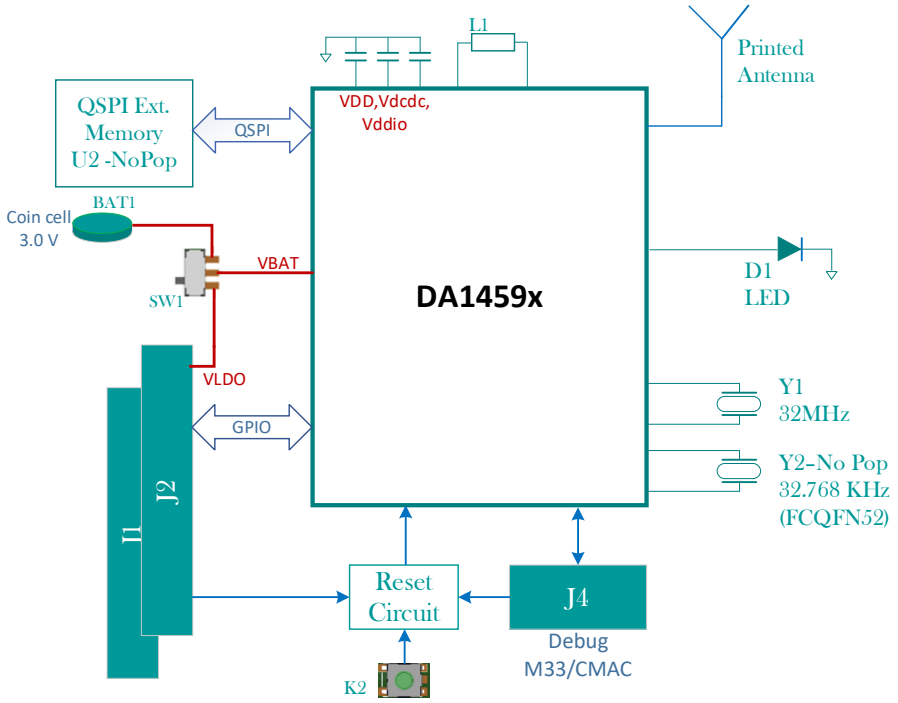


Figure 6. System block diagram of DA1459x Pro-daughterboard (32 kHz only on FCQFN52)

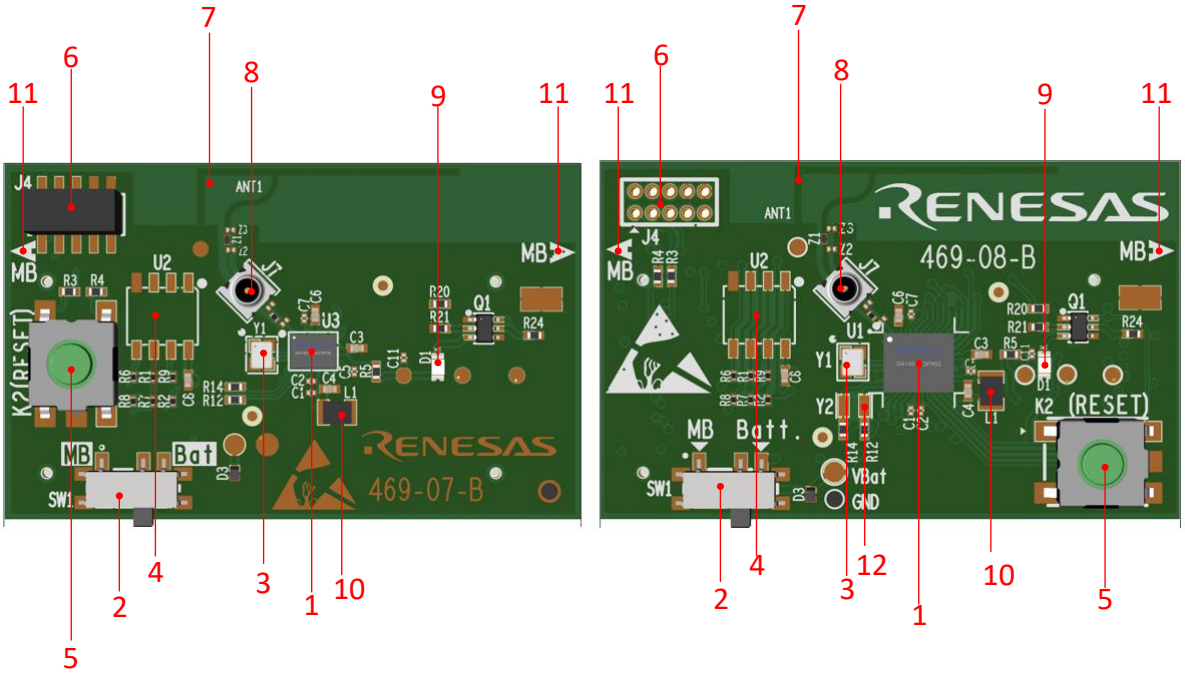


Figure 7. Top side, WLCSP39 Pro-daughterboard (left), FCQFN52 Pro-daughterboard (right)

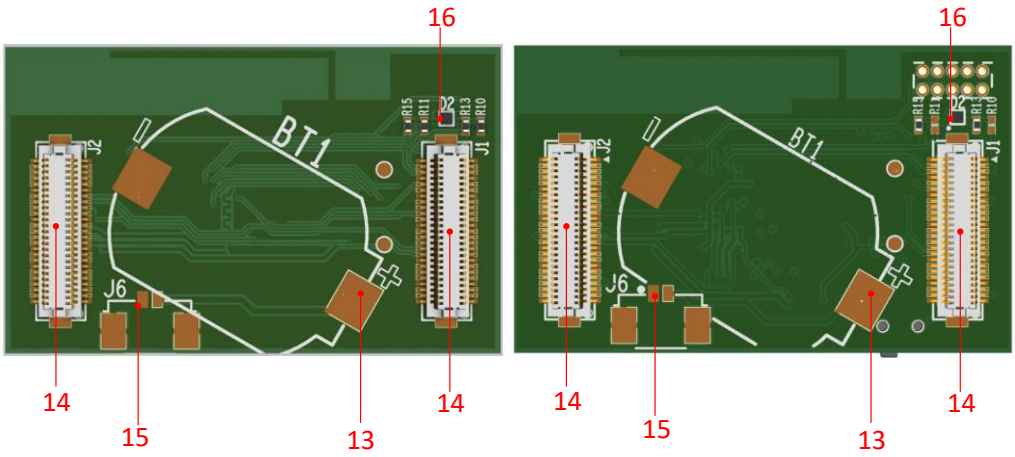


Figure 8. Bottom side, WLCSP39 Pro-daughterboard (left), FCQFN52 Pro-daughterboard (right)

1. DA1459x SoC
2. Power Switch, (SW1)
3. 32 MHz crystal (Y1)
4. External QSPI memory (U2)
5. Reset push button (K2)
6. Debugging connector (J4)
7. Printed antenna
8. RF electromechanical switch (J7)
9. LED (D1)
10. Power inductor (L1)
11. Mounting marking
12. 32 kHz crystal (Y2) – applied (not populated) only for FCQFN52 package.
13. Place holder for Coin cell Battery (BT1)
14. Mating connectors to Pro-motherboard (J1, J2)
15. Place holder for 2-pins battery connector (J6)
16. ESD diode for Debugging connector.

4.2.1 WLCSP39 based Pro-Daughterboard

Signals of DA1459x WLCSP39 (da1459x-db-wlcsp39_469-07-x) are routed to J1, J2 interface board (mating) connectors on the DA1459x Daughterboard. See Figure 9.

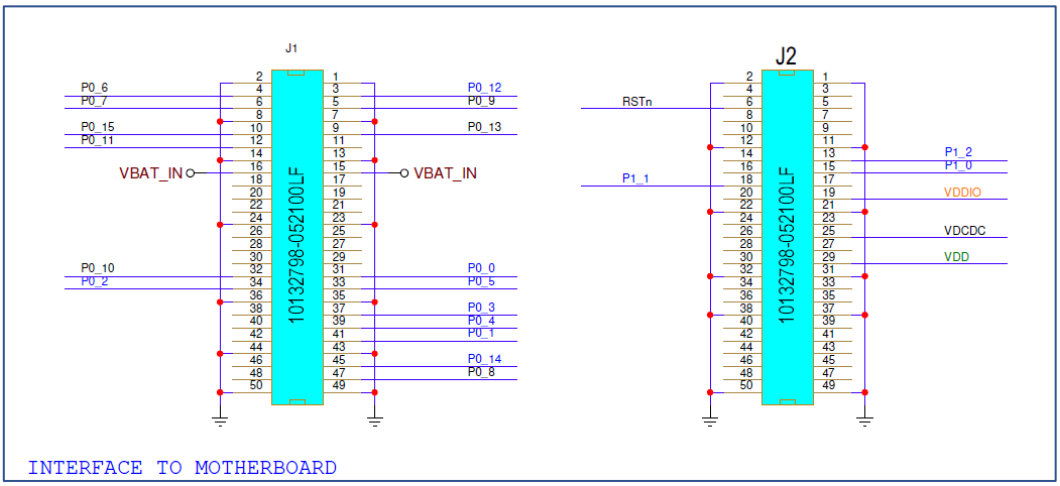


Figure 9. DA1459x interface header of WLCSP39 to DA1459x Pro-motherboard

Signals of DA1459x WLCSP39 are mapped to Pro-motherboard. Table 3 describes the mapping of the signals.

Table 3. DA1459x WLCSP39 pins assignment

GPIO	GPIO multiplexing	DevKit function	MikroBUS	PMOD
P0_0	QSPI_CLK	-	SCK	SCK
P0_1	QSPI_CS	TRIG_5	CS1#	
P0_2	QSPI _D0	-	MOSI	MOSI
P0_3	QSPI _D1	-	MISO	MISO
P0_4	QSPI _D2	-	INT1	-
P0_5	QSPI _D3	-	RST1#	-
P0_6	M33_SWDIO	SWDIO	-	-
P0_7	M33_SWCLK	SWCLK	-	-
P0_8	CMAC_SWDIO/DIVN	TRIG_1	-	INT2
P0_9	CMAC_SWCLK	-	-	RST2#
P0_10	PWM_2/GPADC_2/SDADC_2	BUTTON/DTRIG_0	AN	-
P0_11	XTAL32M	UCTS	-	CS1#
P0_12	LPCLK/PWM_1	TRIG_4	PWM	-
P0_13	BOOT_UART_TX	UTX	-	-
P0_14	WAKEUP_1	TRIG_6	SCL	SCL
P0_15	BOOT_UART_RX	URX	RX	-
P1_0	PGA_INp/GPADC_0/SDADC_0	URTS	TX	-
P1_1	PGA_INn/GPADC_1/SDADC_1	TRIG_2	-	-
P1_2	RC32M/GPADC_3/SDADC_3	TRIG_3	SDA	SDA

4.2.2 FCQFN52 based Pro-Daughterboard

Signals of DA1459x FCQFN52 (da1459x_db_fcqfn52_469-08-x) are routed to J1, J2 interface board (mating) connectors on the DA1459x Daughterboard. See Figure 10.

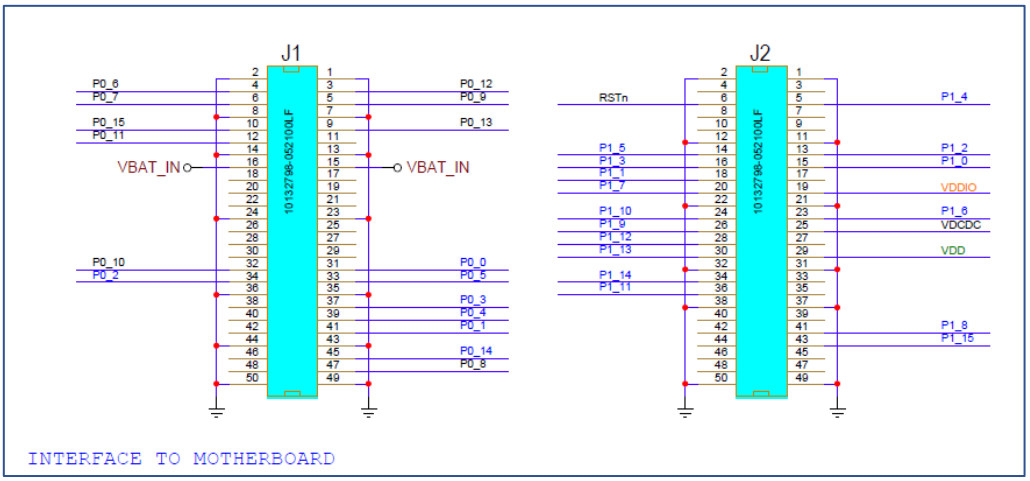


Figure 10. DA1459x interface header of FCQFN52 to DA1459x Pro-motherboard

Signals of DA1459x FCQFN52 are mapped to DA1459x Pro-Motherboard. Table 4 describes the mapping of the signals.

Table 4. DA1459x FCQFN52 pins assignment

GPIO	GPIO multiplexing	DevKit function	MikroBUS	PMOD	DBs mating headers J1 and J2 (Note 1)
P0_0	QSPI_CLK	-	SCK	SCK	J1.31
P0_1	QSPI_CS	TRIG_5	CS1#	-	J1.41
P0_2	QSPI _D0	-	MOSI	MOSI	J1.34
P0_3	QSPI _D1	-	MISO	MISO	J1.37
P0_4	QSPI _D2	-	INT1	-	J1.39
P0_5	QSPI _D3	-	RST1#	-	J1.33
P0_6	M33_SWDIO	SWDIO	-	-	J1.4
P0_7	M33_SWCLK	SWCLK	-	-	J1.6
P0_8	CMAC_SWDIO/DIVN	TRIG_1	-	INT2	J1.47
P0_9	CMAC_SWCLK	-	-	RST2#	J1.5
P0_10	PWM_2/GPADC_2/SDADC_2	BUTTON/TRIG_0	AN	-	J1.32
P0_11	XTAL32M	UCTS	-	CS1#	J1.12
P0_12	LPCLK/PWM_1	TRIG_4	PWM	-	J1.3
P0_13	BOOT_UART_TX	UTX	-	-	J1.09
P0_14	WAKEUP_1	TRIG_6	SCL	SCL	J1.45
P0_15	BOOT_UART_RX	URX	RX	-	J1.10
P1_0	PGA_INp/GPADC_0/SDADC_0	URTS	TX	-	J2.15
P1_1	PGA_INn/GPADC_1/SDADC_1	TRIG_2	-	-	J2.18
P1_2	RC32M/GPADC_3/SDADC_3	TRIG_3	SDA	SDA	J2.13
P1_3	-	-	-	-	J2.16
P1_4	WAKEUP_2	TRIG_7	-	-	J2.5
P1_5	GPADC_4/SDADC_4/SDADC_REFp/SDADC_INT_REF	-	-	-	J2.14
P1_6	GPADC_5/SDADC_5/SDADC_REFn	-	-	-	J2.23
P1_7	-	-	-	-	J2.20
P1_8	-	-	-	-	J2.41
P1_9	GPADC_6/SDADC_6	-	-	-	J2.26
P1_10	-	-	-	-	J2.24
P1_11	GPADC_7/SDADC_7	-	-	-	J2.36
P1_12	-	-	-	-	J2.28
P1_13	XTAL32km	-	-	-	J2.30
P1_14	XTAL32kp	-	-	-	J2.34
P1_15	-	-	-	-	J2.43

Note 1 QSPI (GPIO) pads input voltage must not exceed VDDIO voltage level since there is no backdrive protection on those pads.

4.2.3 XTAL, 32 MHz (Y1)

The main clock of the system is generated from a 32 MHz crystal which is connected to the internal crystal oscillator of DA1459x SoC. The crystal used is the Murata XRCGB32M000F1H00R0 or XRCGB32M000F1S1AR0.

Table 5. Crystal specification

Item	Specification
Nominal Frequency	32.0000 MHz
Frequency Tolerance	±10 ppm max.
Frequency Shift by Temperature	±10 ppm/max. from initial value (-30 to +85°C)
Frequency Aging	±2 ppm max/year
Equivalent Series Resistance	60 Ω max. or 50 Ω max (Note 1)
Load Capacitance	6.0±0.1 pF
Operating Temperature Range	-30 to +85°C
Size	2.0 x 1.6 mm

Note 1 60 Ω for XRCGB32M000F1H00R0
50 Ω for XRCGB32M000F1S1AR0

4.2.4 XTAL, 32 kHz (Y2)

An optional 32 kHz external crystal can be placed on the daughterboard. This crystal is not mandatory as there is an internal RCX oscillator in DA1459x that can be used instead. In WLCSP Pro- daughterboard this crystal is not placed, while in FCQFN daughterboard there is a placeholder, but crystal is not populated.

4.2.5 Debugging Connector (J4)

On both daughterboards there is an optional JTAG connector that can be used for debugging via SWD or for communication via UART.

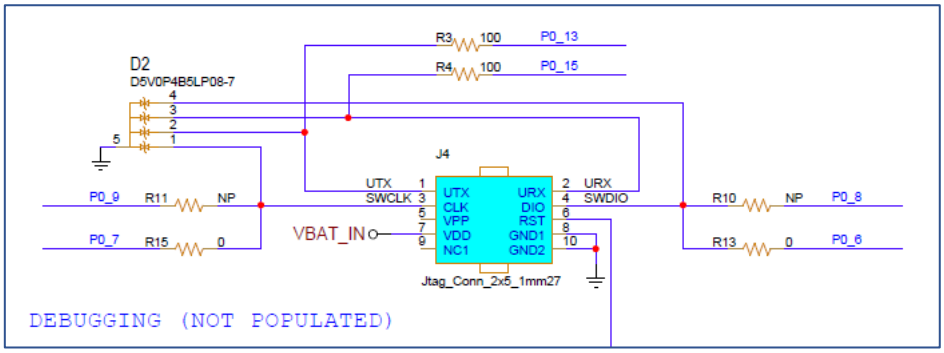


Figure 11. The debugging header, J4

As described in the datasheet, DA1459x contains two processors, an Arm® Cortex-M33™ and an Arm® Cortex-M0+™. Both processors can be accessed from J4, through their SWD bus. By default, the SWD of M33 is enabled. For enabling SWD bus of M0+, two resistors must be removed (R10, R15) and two others to be mounted (R11, R13).

Table 6. Debugging header – pins assignment

Pin №	Pin function	Default signals	Optional signals	Comments
1	UTX	P0_13	-	Through 100 Ω
2	URX	P0_15	-	Through 100 Ω
3	SWCLK	P0_7 (SWCLK_M33)	P0_9 (SWCLK_M0+)	To Enable optional signal: solder R11/remove R15
4	SWDIO	P0_6 (SWDIO_M33)	P0_8 (SWDIO_M0+)	To Enable optional signal: solder R13/remove R10
5	VPP	No Connect	-	-
6	RST	RST	-	Driven to DA1459x through inverter
7	VDD	VBAT_IN	-	-
8	GND	GND	-	-
9	No Connect	No Connect	-	-
10	GND	GND	-	-

SWD of M33 is also connected to the Pro-motherboard onboard J-Link debugger. Consequently, by enabling the SWD of M0+ connectivity on J4, you can access both processors (M33 and M0+) of DA1459x.

4.2.6 QSPI External Memory (U2)

On both daughterboards, an optional external QSPI memory place holder, U2 is applied. This is a footprint for a SOP-8, 150 mils. By default, it is not populated as DA1459x contains an embedded flash memory.

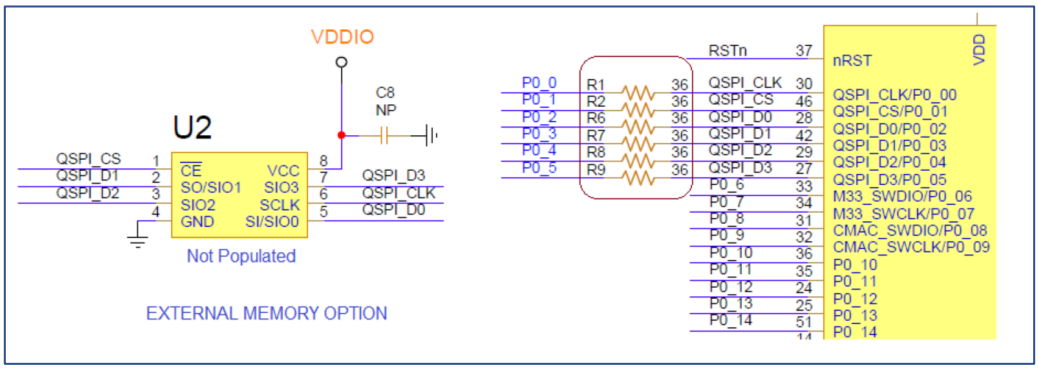


Figure 12. The External QSPI memory, (U2) place holder

On the Software Development Kit (SDK) the following components are supported:

- Macronix MX25U3235, 32 MBit
- Winbond W25Q32JWIM, 32 MBit
- Winbond W25Q32JWIQ, 32 Mbit.

For enabling the external memory option, you can populate U2, C8 (= 1 µF) and remove resistors R1, R2 and R6 to R9 (= 36 Ω) for isolating memory from Pro-motherboard.

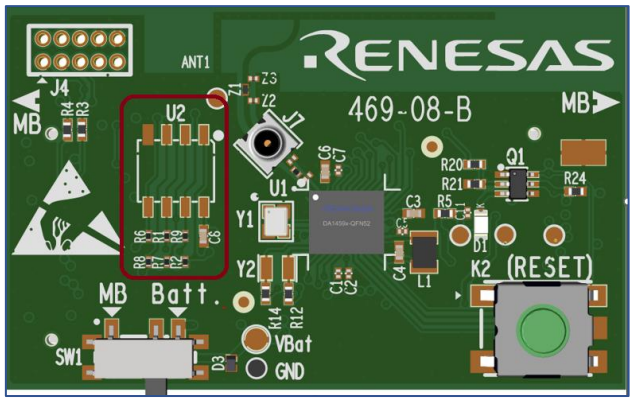


Figure 13. External memory placeholder and the components

4.2.7 General Purpose LED (D1)

On both daughterboards, there is one red LED (D1) that can be used for optical indications. LED is driven from P1_1 through a N-FET.

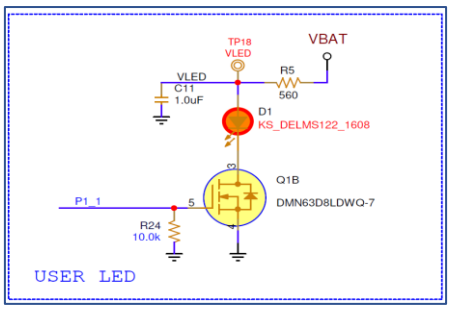


Figure 14. Red LED (D1) circuitry

4.2.8 The RESET on DA1459x Pro-Daughterboard

Reset is active low. If it is not driven low, nRst pin of DA1459x is set high by an internal pull up, 25 K, to VBAT_IN.

On DA1459x Pro DevKit, there are four ways for activating Reset.

- By pressing button (K2).
- Through Debugger connector J4. As the Reset signal of J4 is active high, a nFET is added.
- Through T-Reset signal on DA1459x Pro-motherboard, see Section 4.3.6. This connected directly (wired-OR) to DA1459x chip pin.
- Through U_RSTn signal on DA1459x Pro-motherboard, see Section 4.3.6. This signal is tied together with T_Reset and connected directly (wired-OR) to DA1459x chip pin. This option requires additional software. By default, it is not enabled.

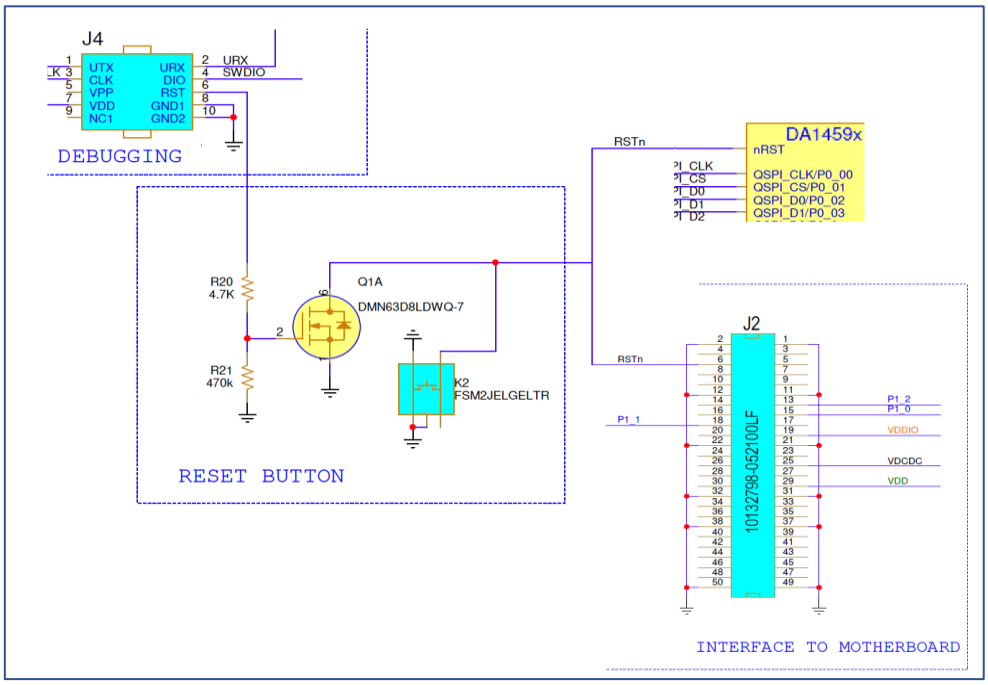


Figure 15. Reset circuitry on Pro-daughterboard

4.2.9 Power Section of DA1459x Pro-Daughterboard

The DA1459x has a complete integrated Power Management Unit (PMU). This includes a buck DC-DC converter and several LDOs for the different power rails of the system. Voltage rails are:

- VBAT: input voltage of the DA1459x SoC. VBAT is provided either from Pro-motherboard or a battery. Selection is done from SW1.
- VDCDC: produced from internal synchronous Single Inductance (L1) Single Output Buck DC-DC converter with programmable output 1.1 V to 1.4 VDCDC.
- VDD: LDO (active and retention) for the digital core with 20 mA (2 mA on retention) driving capability.
- VDDIO: LDO (active and retention) for the I/O-s with bypass functionality of 1.8 V voltage range.

Figure 16 shows the configuration of PMU on daughterboard.

The power section consists of a Switch (SW1) that can be used for selecting a power supply source for the chip.

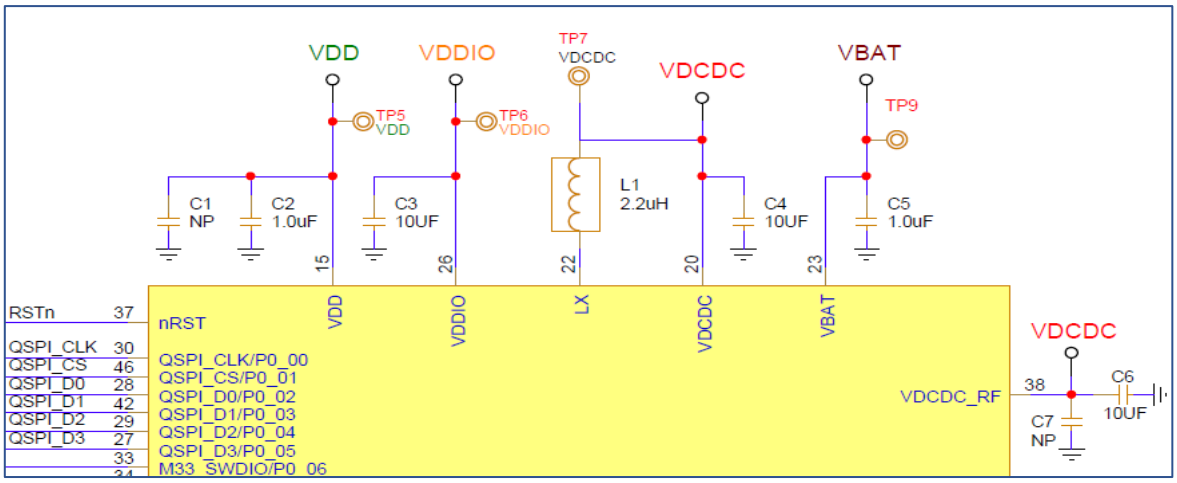


Figure 16. DA1459x SoC, power pins

There are two options available:

- Supply from LDO on Pro-motherboard by setting SW1 to **MB**, see Figure 17.
- Supply directly from Battery by setting SW1 to **Bat** see Figure 17.

Two Battery options are available:

- Place holder for a Coin cell 2016 lithium battery socket (BT1) on the bottom layer of each daughterboard (Figure 17).
- Place holder for a two pins Battery connector (J6).

NOTE
Battery Information and Conformity Declaration For the **Coin Cell Battery**: this product requires the use of a **button cell battery** to operate. The recommended and required battery type is a **CR2032** cell, specifically the **CR2032W-1714569** model by **Murata**. For the **two pins Battery Connector**: do not use a LiPo battery because its voltage can go higher than 3.6 V and this can damage DA1459x SoC. Absolute maximum voltage of VBAT pin of DA1459x is 3.6 V. You must ensure that the battery used conforms to the **IEC standard 60086-4** for button cell batteries to guarantee safe and optimal performance of the product. The use of any other battery model or non-compliant battery may result in improper functioning or safety hazards. For safety reasons, always use the specified battery model and ensure it complies with the required product standards.

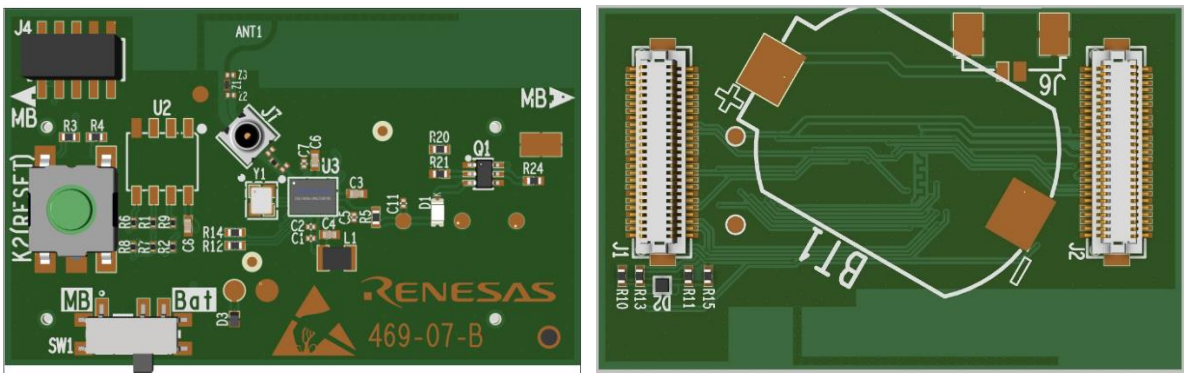


Figure 17. SW1 (left), available battery sockets on the bottom side of the daughterboards (right)

4.2.10 RF Section

The RF section consists of a printed antenna, a matching circuit, a Low Pass Filter (LPF), and an RF coaxial switch that can be used for conducted RF measurements instead of the antenna. If a cable is connected on the RF coaxial switch, then the antenna gets disconnected from the chip.

The DA1459x RFIO pin is connected to the printed antenna through a 50 Ω RF stripline, an LPF and a matching circuit.

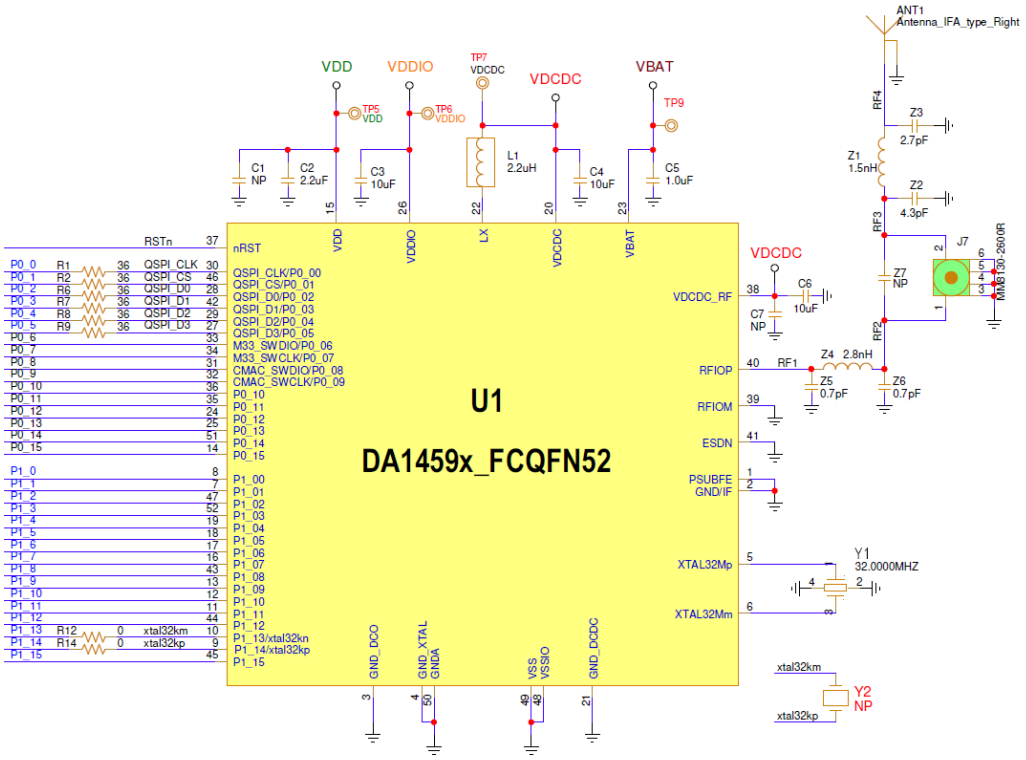


Figure 18. RF section of DA1459x Pro-daughterboard

RF coaxial connector J7, is the Murata MM8130-2600RB8. You must use an appropriate mating coaxial cable to SMA, (MXHS83QE3000).

4.3 DA1459x Pro-Motherboard

The Pro-motherboard, with design name DA1459x-mb-pro and reference number 469-16-D, hosts the DA1459x Pro-daughterboard as well as the components which are required for evaluation and software development. Figure 19 shows Pro-motherboards main blocks.

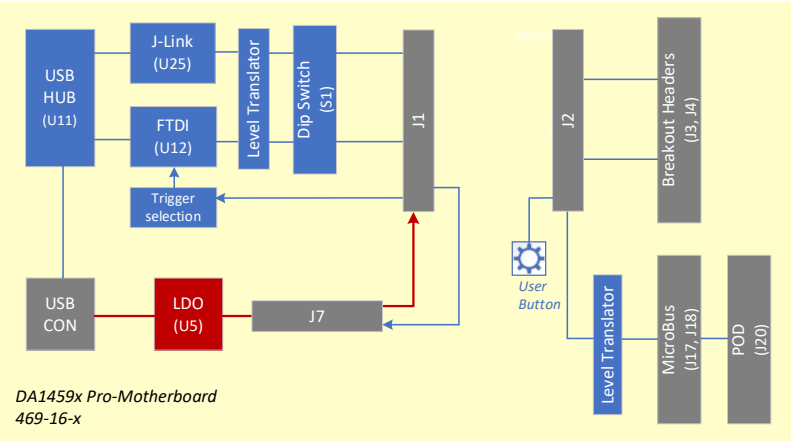


Figure 19. DA1459x Pro-motherboard block diagram

- Pro-Daughterboard mating headers (J1 and J2)
- Power section and Power Measurement Module (PMM2) daughterboard for measuring the current that DA1459x draws (it needs SmartSnippets toolbox)

- FTDI chip for UART communication between DA1459x and the PC
- MCU SEGGER chip for SWD debugging through Jlink
- DIP switch (S1) for allowing communication with FTDI and SEGGER
- Breakout headers (J3 and J4) for exposing the DA1459x GPIOs
- MikroBUS (J17 and J18) and PMOD (J20) interfaces – parallel connected
- General purpose push button
- Configuration headers.

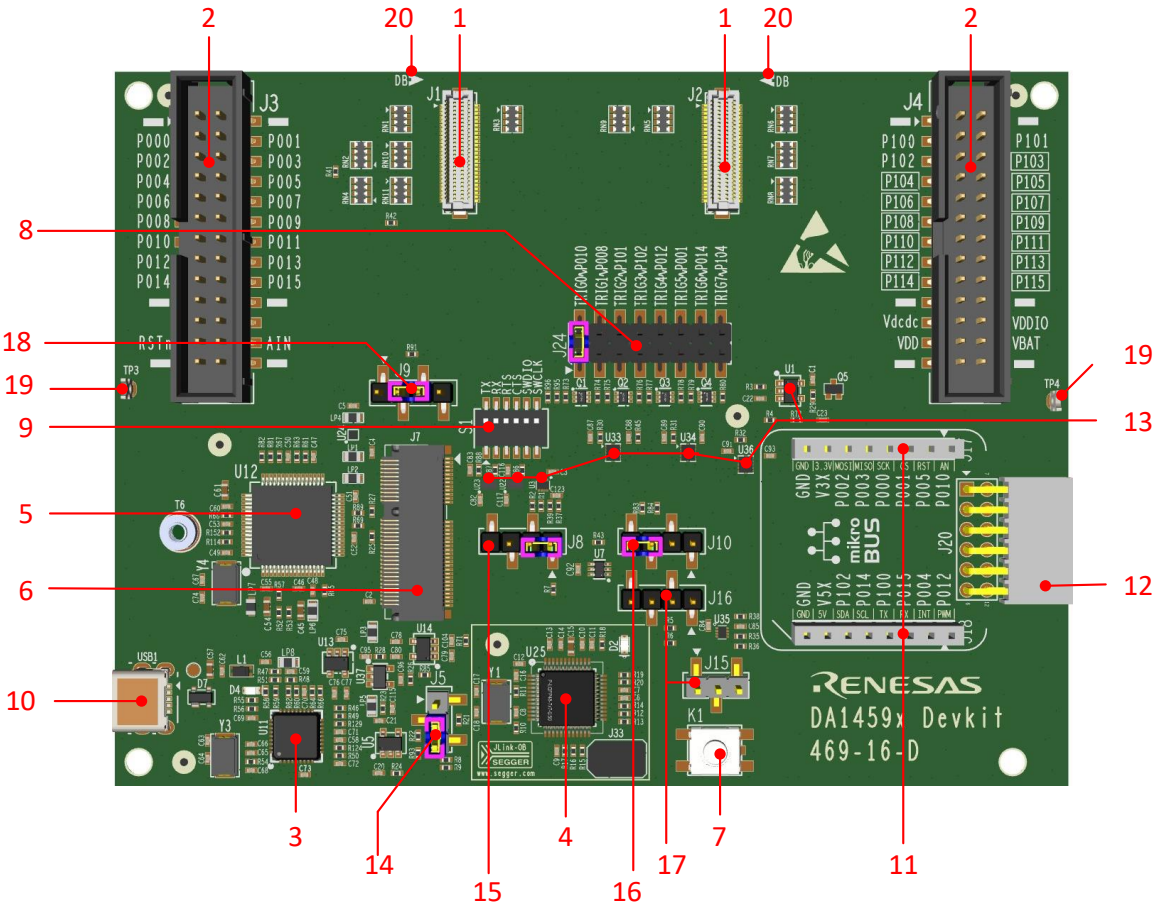


Figure 20. DA1459x Pro-motherboard, 469-16-x

1. Daughterboard Mating Headers, J1 and J2
2. Breakout Header, J3 and J4
3. USB HUB, U11
4. USB to SWD (Segger), U25
5. USB to UART, U12
6. PMM2 Mounting Connector, J7
7. Push Button, K1
8. Digital Trigger Header, J24
9. Debug Section DIP Switches, S1
10. USB port, USB1
11. MikroBUS Connectors, J17 and J18
12. PMOD Connector, J20
13. Level Translators
14. Header of Power Supply options, J5
15. Header of Push Button enable and LDO_EN, J8
16. Header of Reset Options, J10
17. Header for Enabling Level Translators for I2C of MikroBUS and PMOD, J15 and J16
18. Header of PMM2 Enable, J9
19. GND pins, TP3 and TP4
20. Daughterboard alignment Mark.

4.3.1 DA1459x Signals Distribution on Pro-Motherboard

The signals of DA1459x are routed to Pro-daughterboard through J1, J2 mating connectors, and they are distributed into the Pro-motherboard. They are either used for debugging purposes or they are connected to MikroBUS/PMOD interfaces. All signals are exposed to break out headers for monitoring purposes.

Table 7 describes the mapping of Signals of DA1459x on Pro-motherboard.

Table 7. DA1459x signal connectivity on Pro-motherboard

GPIO	GPIO multiplexing	DevKit function	MikroBUS	PMOD	DBs mating headers J1 and J2	Breakout headers J3 and J4
P0_0	QSPI_CLK	-	SCK	SCK	J1.31	J3.3
P0_1	QSPI_CS	TRIG_5	CS1#	-	J1.41	J3.4
P0_2	QSPI _D0	-	MOSI	MOSI	J1.34	J3.5
P0_3	QSPI _D1	-	MISO	MISO	J1.37	J3.6
P0_4	QSPI _D2	-	INT1	-	J1.39	J3.7
P0_5	QSPI _D3	-	RST1#	-	J1.33	J3.8
P0_6	M33_SWDIO	SWDIO	-	-	J1.4	J3.9
P0_7	M33_SWCLK	SWCLK	-	-	J1.6	J3.10
P0_8	CMAC_SWDIO/DIVN	TRIG_1	-	INT2	J1.47	J3.11
P0_9	CMAC_SWCLK	-	-	RST2#	J1.5	J3.12
P0_10	PWM_2/GPADC_2/SDADC_2	BUTTON/ TRIG_0	AN	-	J1.32	J3.13
P0_11	XTAL32M	UCTS	-	-	J1.12	J3.14
P0_12	LPCLK/PWM_1	TRIG_4	PWM	-	J1.3	J3.15
P0_13	BOOT_UART_TX	UTX	-	-	J1.09	J3.16
P0_14	WAKEUP_1	TRIG_6	SCL	SCL	J1.45	J3.17
P0_15	BOOT_UART_RX	URX	RX	-	J1.10	J3.18
P1_0	PGA_INp/GPADC_0/SDADC_0	URTS	TX	-	J2.15	J4.3
P1_1	PGA_INn/GPADC_1/SDADC_1	TRIG_2	-	-	J2.18	J4.4
P1_2	RC32M/GPADC_3/SDADC_3	TRIG_3	SDA	SDA	J2.13	J4.5
P1_3	-	-	-	-	J2.16	J4.6
P1_4	WAKEUP_2	TRIG_7	-	-	J2.5	J4.7
P1_5	GPADC_4/SDADC_4/ SDADC_REFp/ SDADC_INT_REF	-	-	-	J2.14	J4.8
P1_6	GPADC_5/SDADC_5/ SDADC_REFn	-	-	-	J2.23	J4.9
P1_7	-	-	-	-	J2.20	J4.10
P1_8	-	-	-	-	J2.41	J4.11
P1_9	GPADC_6/SDADC_6	-	-	-	J2.26	J4.12
P1_10	-	-	-	-	J2.24	J4.13
P1_11	GPADC_7/SDADC_7	-	-	-	J2.36	J4.14
P1_12	-	-	-	-	J2.28	J4.15
P1_13	XTAL32km	-	-	-	J2.30	J4.16
P1_14	XTAL32kp	-	-	-	J2.34	J4.17

GPIO	GPIO multiplexing	DevKit function	MikroBUS	PMOD	DBs mating headers J1 and J2	Breakout headers J3 and J4
P1_15	-	-	-	-	J2.43	J4.18

4.3.2 USB Port (USB1) and USB HUB (U11)

DA1459x DevKit power and data port is the USB connector USB1. This is a mini-USB connector. Power connection is protected from surges with a Common Mode Choke whereas data connections are protected with ESD diodes.

The USB HUB of DA1459x Pro-motherboard is implemented by U11, USB2512B. This chip is supplied with 3.3 V from U13.

The signal PWR_ENABLE is generated from U11 and it is an active high signal. It enables the power components (LDOs and DC-DC converter) for UART, JTAG, and the current sensing circuit. The system powers up only after the USB HUB has enumerated properly. PWR_ENABLE signal can be manually activated by adding a jumper between positions 3 and 4 of header J8.

Its operation is indicated through the green LED D4 on DA1459x Pro-motherboard. A 24 MHz crystal (Y3) is required for chip operation.

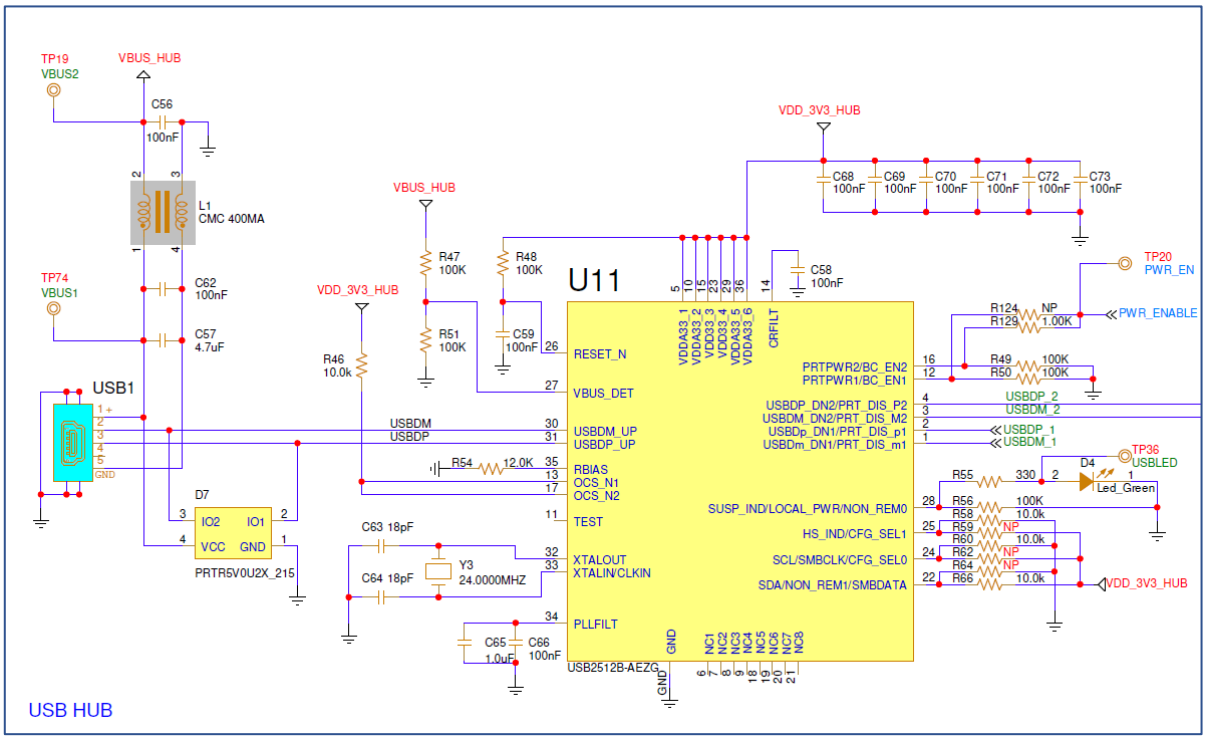


Figure 21. USB HUB circuitry of DA14531 Pro-motherboard

4.3.3 USB to UART (U12)

The USB to UART function is implemented by U12, FT2232HL. This chip is supplied with 3.3 V from U14. A 12 MHz crystal (Y4) is required for the chip operation. U12 is connected to the USB hub.

Functions served by U12 are the following:

- Connecting a PC to the UART port of DA1459x SoC. This is a Full UART which is connected to DA1459x through DIP Switch (S1) and level translators.
- Connecting a PC to the current sensing circuitry:
  - SPI connection with PMM2.
  - Connection to 8 software triggers, including the software cursor triggering (**TRIG_3**/**P1_02**) as defined in the SDK.
- Reset capability of the DA1459x SoC through the U_RSTn signal (not enabled).

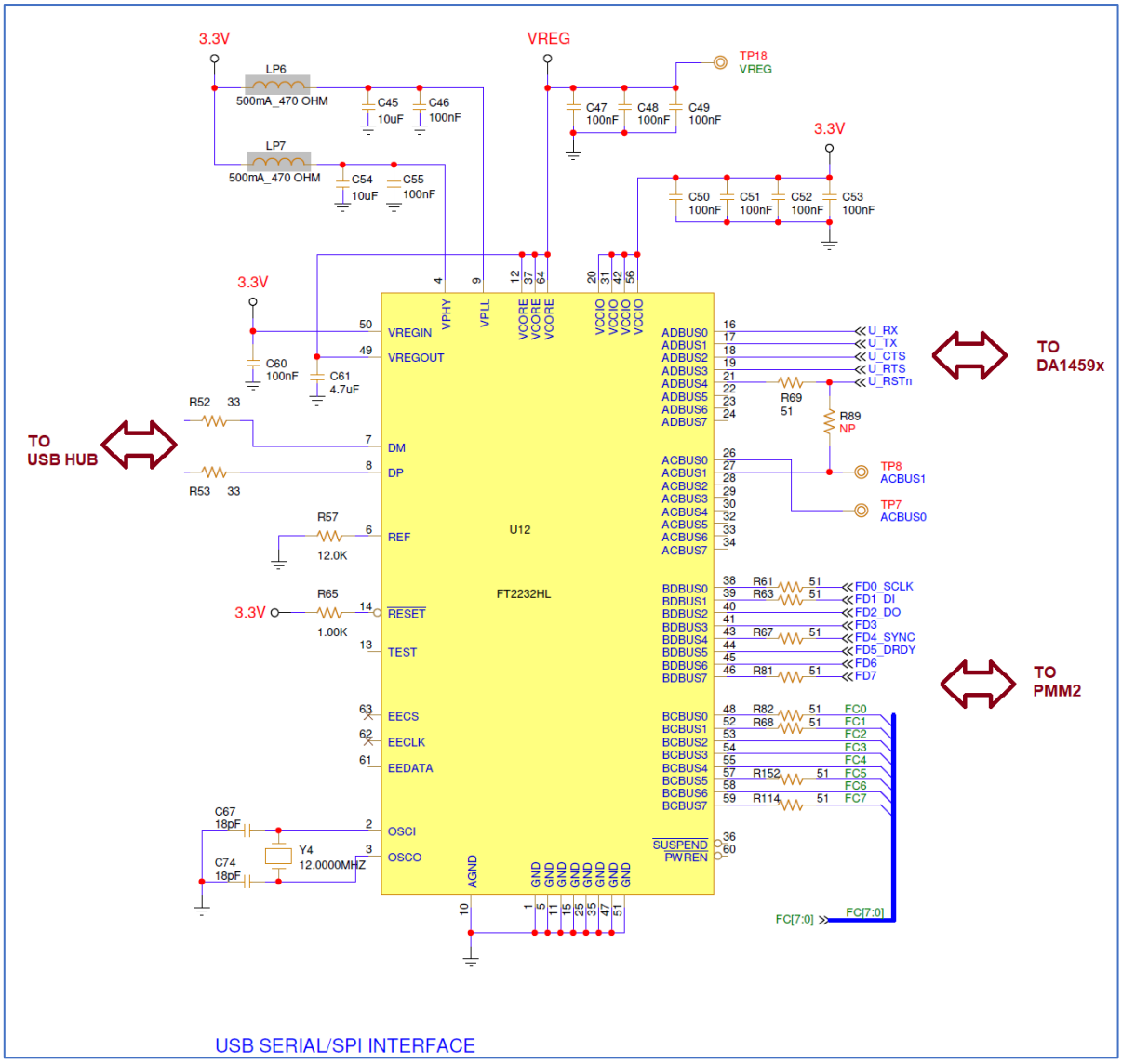


Figure 22. USB to UART (U12)

4.3.4 USB to SWD (U5)

The USB to SWD function is implemented by U5, R7FA4M2AD3CFL. On the Flash of U5, the JLink-OB firmware from SEGGER is loaded. Its operation is indicated via the green LED D2 on the DA1459x Pro-motherboard. This chip is supplied with 3.3 V from U14. U14 is enabled by the PWR_ENABLE signal.

Functions served by U5 include:

- Connecting a PC to the SWD port of DA1459x SoC
- Reset capability of the DA1459x SoC through the T_RESET signal.

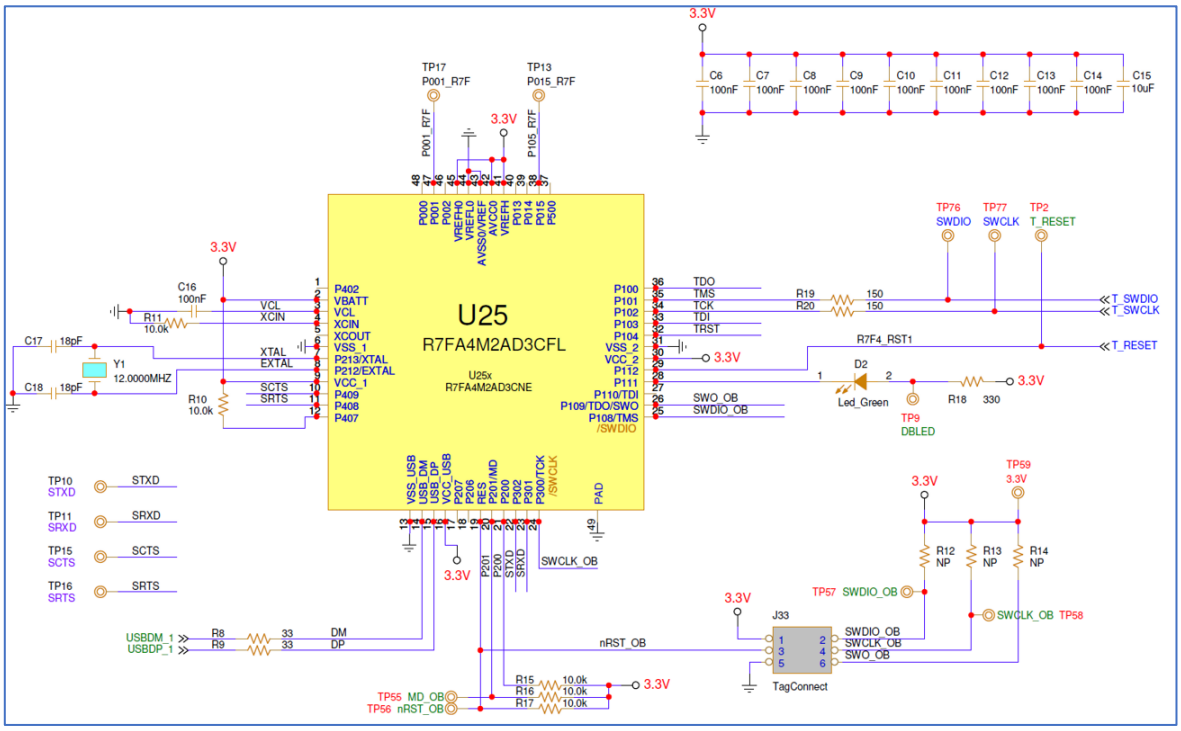


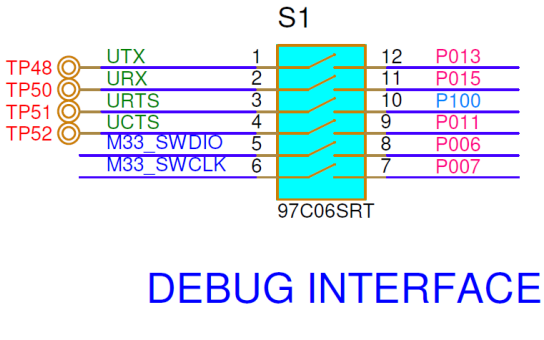
Figure 23. USB to SWD (U4)

4.3.5 Debugging Signals, DIP Switch, and Level Translation

On Pro-motherboard, there is a DIP switch (S1) that can connect or disconnect the DA1459x UART and SWD signals from the FTDI and SEGGER, respectively. Table 8 shows the mapping of these signals.

Table 8. Signal mapping on DIP switch (S1)

Pin name	Signal name
P0_10	SWDIO
P0_11	SWCLK
P0_9	UTX
P0_8	URX
P1_0	URTS
P0_7	UCTS



All the signals that are mapped on the DIP switch require voltage translation for avoiding leakage through the pins because the DA1459x I/O voltage is set to 1.8 V voltage range (LDO_IO) whereas the other side (on board interfaces, JTAG/UART) is fixed at 3.3 V, (Figure 24).

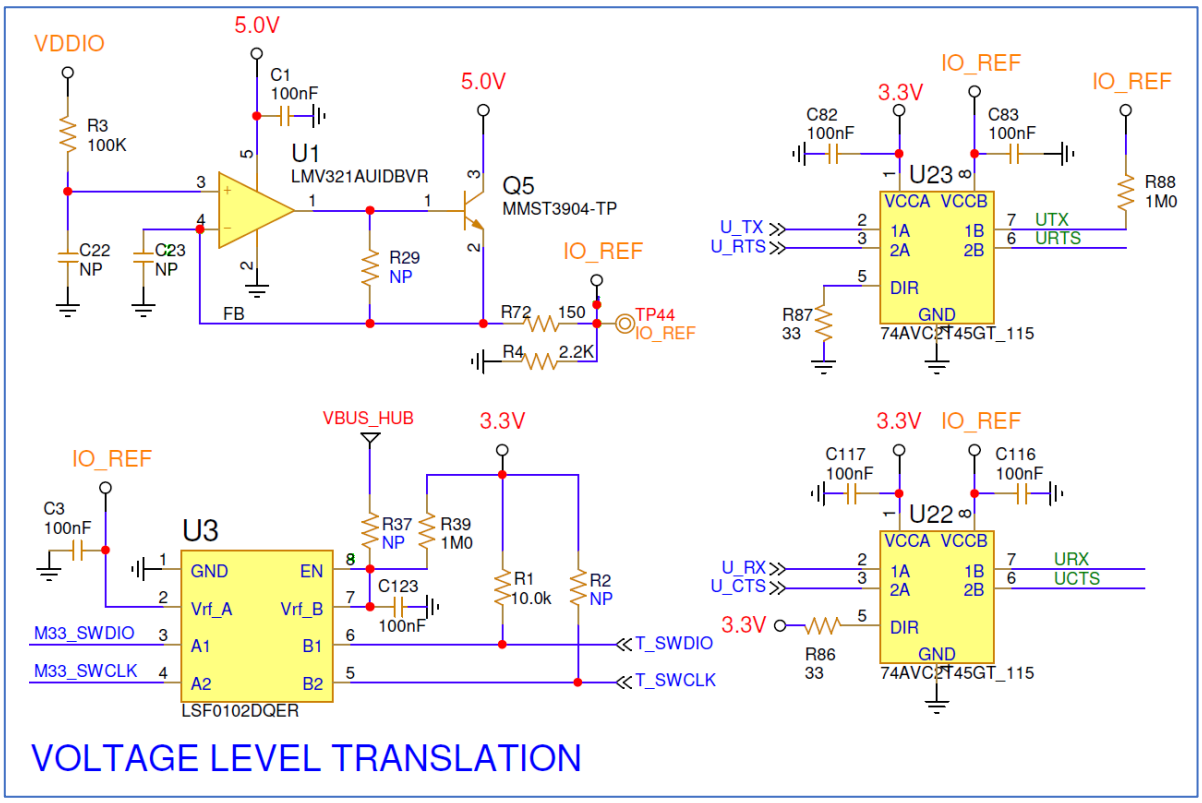


Figure 24. Voltage level translation circuit

IO_REF is a buffered version of the voltage used in the DA1459x side I/O. This voltage rail powers a dual buffer gate (U22) with direction from motherboard to DA1459x pins, and also on DA1459x side the single bidirectional transceiver used for SWDIO (U3).

The direction from DA1459x to the motherboard is handled by U23, powered from the motherboard 3.3 V.

4.3.6 Reset

The reset (RSTn) of DA1459x is active low, and in general, there are four ways for being activated:

- On DA1459x Pro-Daughterboard:
  - Press the **Push** button (K2) on Pro_DB, see Figure 15.
  - Enable external signal on pin6 of J4 on Pro_DB, see Figure 11.
- On DA1459x Pro-Motherboard:
  - Enable T_RESET on Pro_MB. This signal is connected to pin28 of U25 and it is controlled from the J-Link debugger. To enable it, place a jumper on header J10 between pins 3 and 4.
  - Enable U_RSTn on Pro_MB. U_RSTn is driven from the USB to UART chip (U12). It is connected to ADBUS4 (default) or ACBUS1. These pins must be actively controlled by software.
  - URSTn function is not enabled by default. Consequently, the jumper of J10 between pins 1 and 2 must not be placed or the DA1459x may go to reset condition.

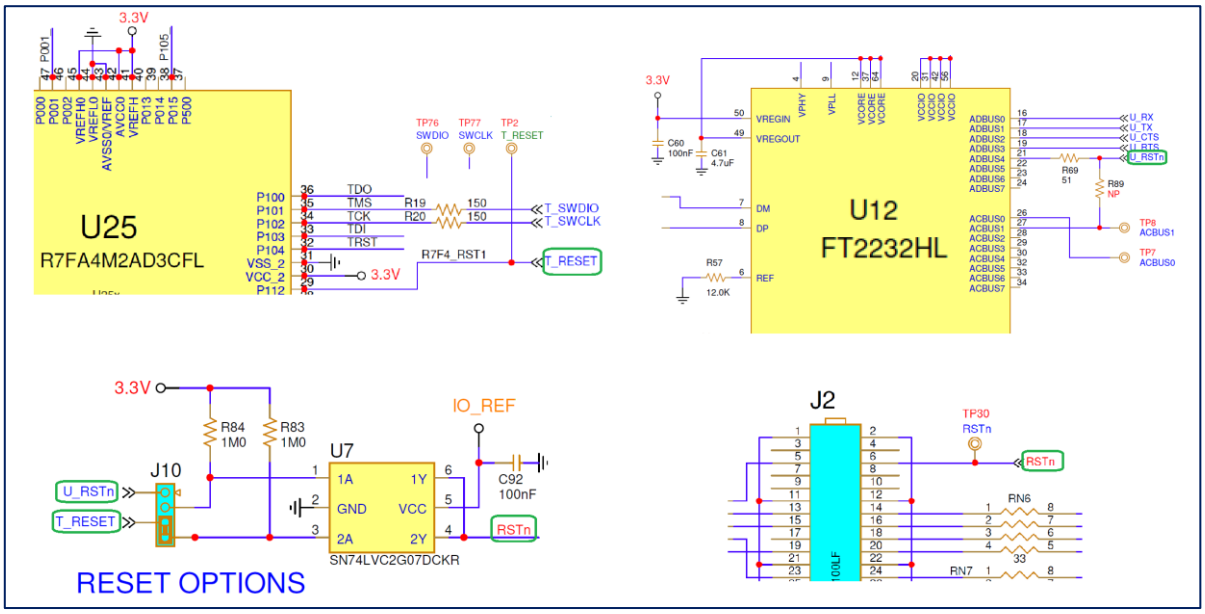


Figure 25. RESET circuit on DA1459x Pro-motherboard

4.3.7 Push Button (K1)

A general-purpose push button, K1 is applied on DA1459x Pro_MB. Press the **Push** button to drive P0_10 to GND through 1 kΩ resistor (R7). The Push button logic is active low and its operation is hardware enabled (default) from header J8, pins 1 and 2.

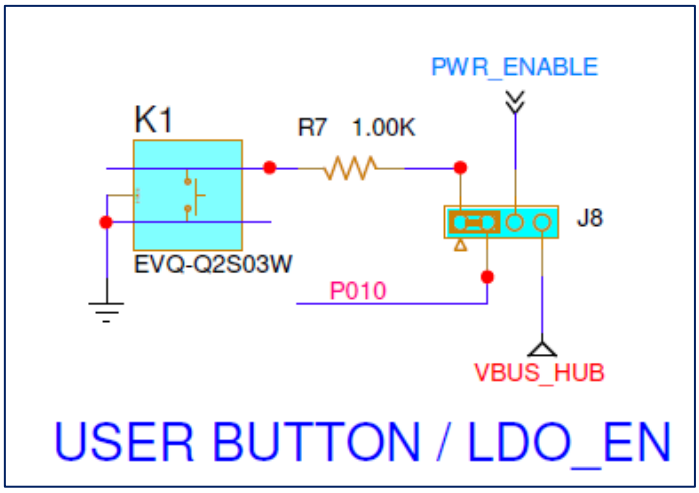


Figure 26. General purpose push button K1

4.3.8 MikroBUS and PMOD Interface

MikroBUS and PMOD share the same signals, except reset, chip select, and interrupt. This means that either MikroBUS or PMOD can be used. Since DA1459x IO-signal level is 1.8 V, voltage translators were added for the MikroBUS and PMOD signals. The connections of I2C signals are controlled by headers J15 and J16 (by default disabled). Termination resistors (33 Ω) are applied between level translators and DA1459x Pro-daughterboard.

MikroBUS is supplied by V5P, a 4.5 V voltage rail, which is produced from U37. Both MikroBUS and PMOD are supplied by V3X, a 3.3 V voltage rail. The current drawn from V3X can be monitored from PMM2.

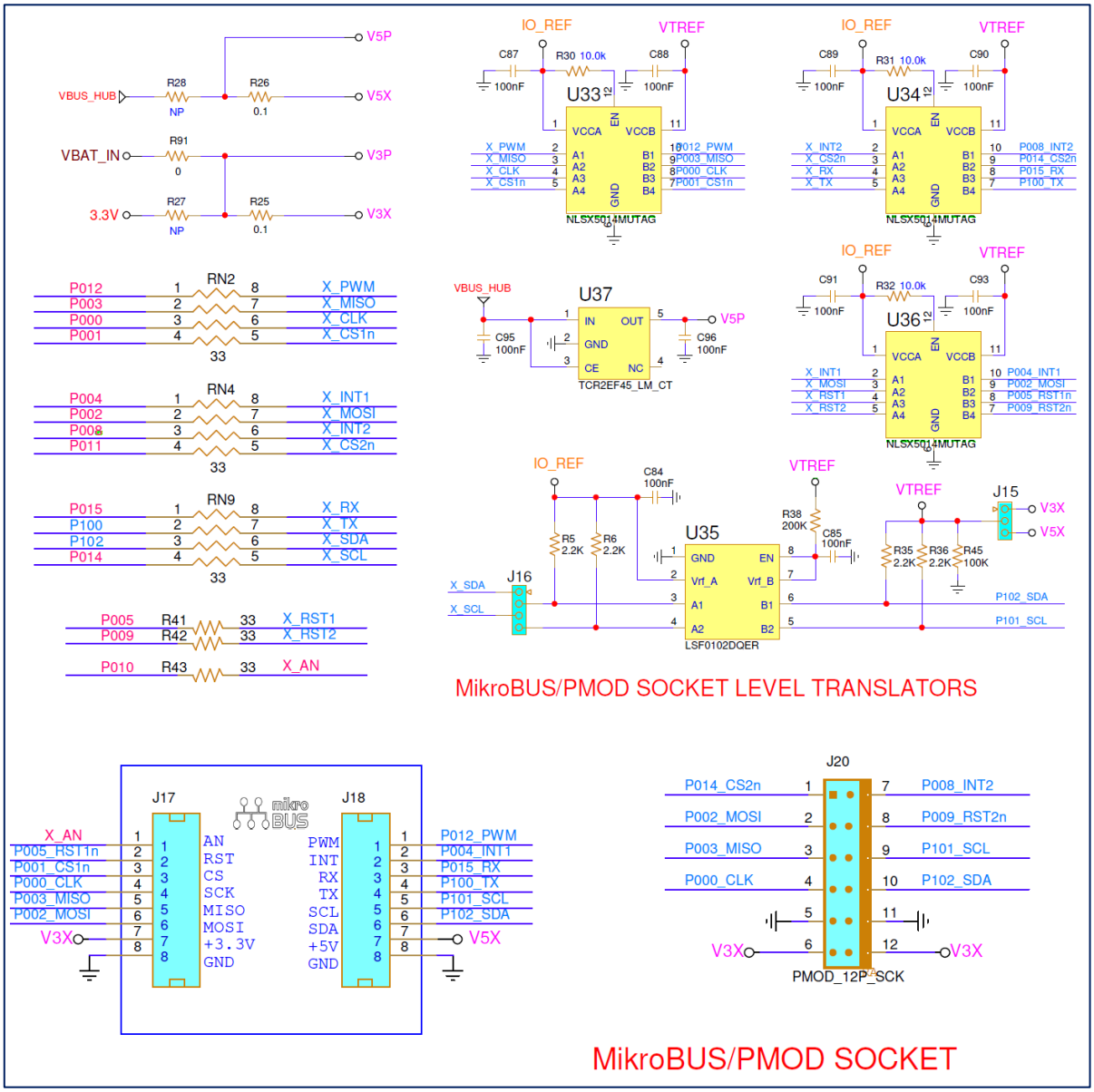


Figure 27. MikroBUS and PMOD

MikroBUS is implemented with two female headers (8 position 0.100 inches, through hole, socket type), J17 and J18. PMOD is implemented with female header (right angle 10 positions 0.100 inches through hole, socket type), J20. Pins assignment is presented on Table 9.

Table 9. MikroBUS and PMOD signals

GPIO	GPIO multiplexing	MikroBUS		PMOD	
P0_0	QSPI_CLK	SCK	J17.4	SCK	J20.4
P0_1	QSPI_CS	CS1#	J17.3	-	-
P0_2	QSPI _D0	MOSI	J17.6	MOSI	J20.2

GPIO	GPIO multiplexing	MikroBUS		PMOD	
P0_3	QSPI _D1	MISO	J17.5	MISO	J20.3
P0_4	QSPI _D2	INT1	J18.2	-	-
P0_5	QSPI _D3	RST1n	J17.2	-	-
P0_8	CMAC_SWDIO/DIVN	-	-	INT2	J20.7
P0_9	CMAC_SWCLK	-	-	RST2#	J20.8
P0_10	PWM_2/GPADC_2/SDADC_2	AN	J17.1	-	-
P0_11	XTAL32M/UCTS on Pro-motherboard	-	-	CS2#	J20.1
P0_12	LPCLK/PWM_1	PWM	J18.1	-	-
P0_14	WAKEUP_1	SCL	J18.5	SCL	J20.9
P0_15	BOOT_UART_RX	RX	J18.3	-	-
P1_0	PGA_INp/GPADC_0/SDADC_0	TX	J18.4	-	-
P1_2	RC32M/GPADC_3/SDADC_3	SDA	J18.6	SDA	J20.10

Limitation: QSPI bus of DA1459x is used for SPI interface for both MikroBUS and PMOD. When an external memory is applied on Pro-Daughterboard, the SPI interface is not available.

4.3.9 Power Section

Power section includes the power circuitry for supplying the DA1459x Pro-Daughterboard as well as the supporting circuits on Pro-Motherboard. Figure 28 shows block diagram.

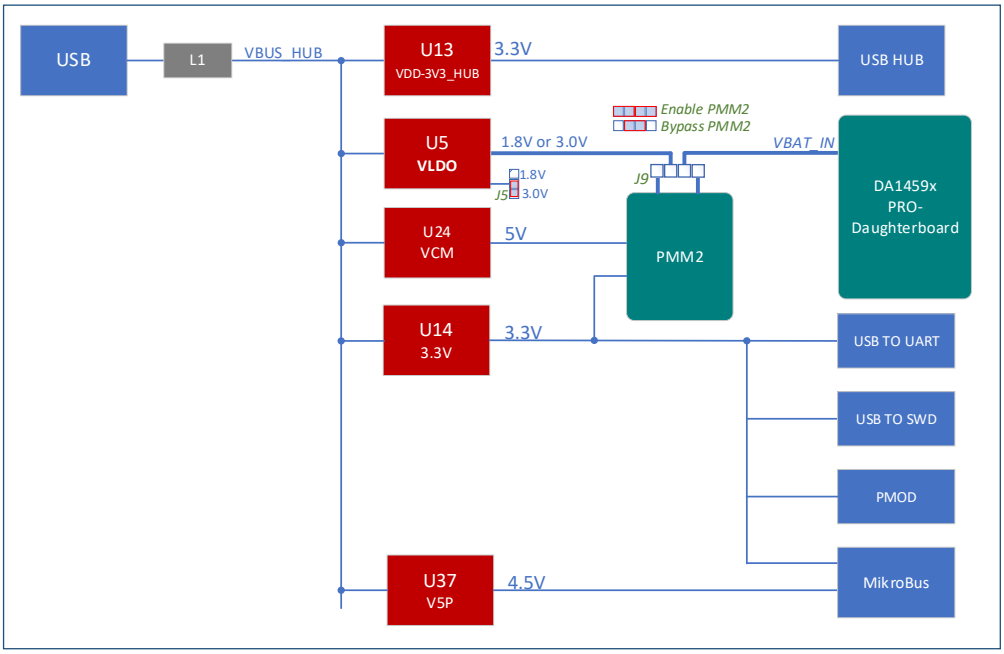


Figure 28. DA1459x Pro-motherboard power section block diagram block

The system is supplied from the USB connector (USB1). Input current passes through a common mode chock (L1) for suppressing the incoming noise. USB Hub is supplied from U13. The rest of the Development kit is supplied from two LDOs U14 and U5. Both these components are enabled from control signal Power_Enable, which is produced from USB_HUB (U11). When a communication between USB_HUB and PC is established, Power_Enable is set high.

For the case when DA1459x Development Kit is powered by a source with no USB functionality, Power_Enable can be activated by adding a jumper on header J8 between pins 3 and 4.

Pro-Motherboard circuits, including USB to UART, USB to SWD, MikroBUS and PMOD, are supplied with 3.3 V generated from LDO U14. Level translators are supplied from the same linear voltage regulator and the USB 5V voltage rail.

DA1459x Pro-Daughterboard is supplied by LDO U5, with the capability of providing either 3.0 V (default) or 1.8 V by removing jumper on header J5. The Current of VLDO can be monitored and measured from PMM2. This is accomplished by applying two jumpers on header J9, between pins 1-2 and 3-4. PMM2 can be bypassed if a jumper is applied on J9 between pins 2 and 3.

PMM2 is supplied by 5 V (= VCM) and 3.3 V. VCM is generated from a power switch which is enabled when Power_Enable is set high. 3.3 V is generated from U14.

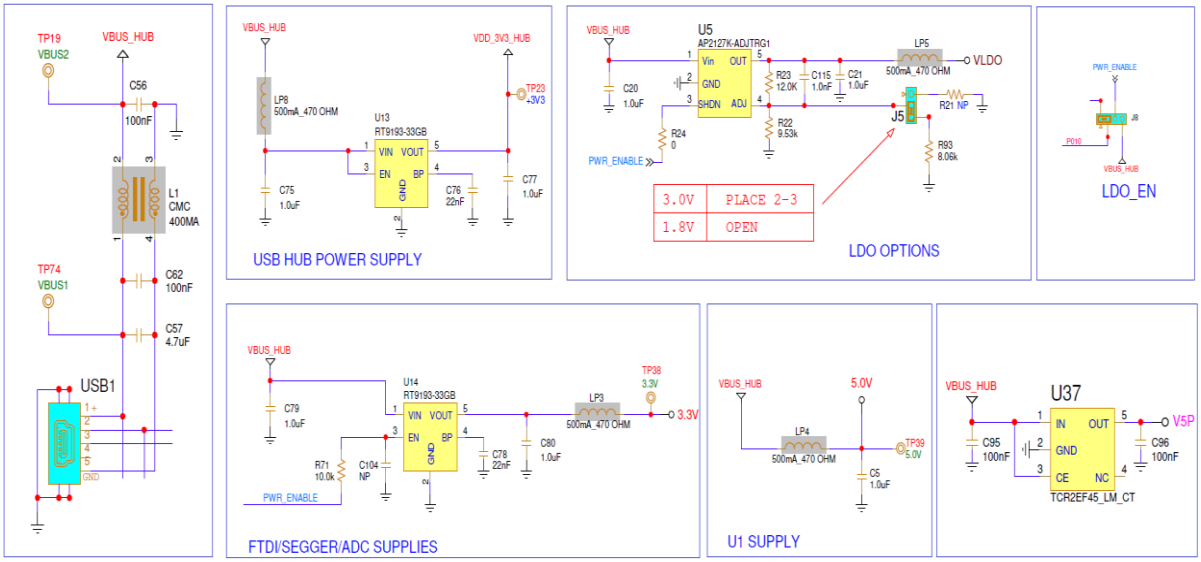


Figure 29. DA1459x Pro-motherboard power section

4.3.10 Measurements and Software Triggers

On DA1459x Development kit, user can monitor the critical current and voltages of the system. This is implemented with a power measurement circuitry which consists of the power measurement module (PMM2) and the monitoring circuit, which resides on the DA1459x Pro-motherboard. The Power profiler of Renesas SmartSnippets Toolbox provides a good visualization of the system current drawn and various voltages. Measurements are quite accurate, but for precise measurements, use an external calibrated instrument.

PMM2 features are:

- DA1459x current measurement (1 µA-100 mA at 128 kHz)
- Measurement of two additional system currents
- 2 x DA1459x system voltage measurement
- 9 x DA1459x system voltage monitoring
- Monitoring and measuring up to 8 Digital signals with capability to be configured as software triggers.

Figure 30 shows the block diagram of PMM2. The analog frontend and ADC converter are implemented on the PMM2 module, whereas the SPI to USB bridge (FT2232H, U12) and digital signals reside on the motherboard.

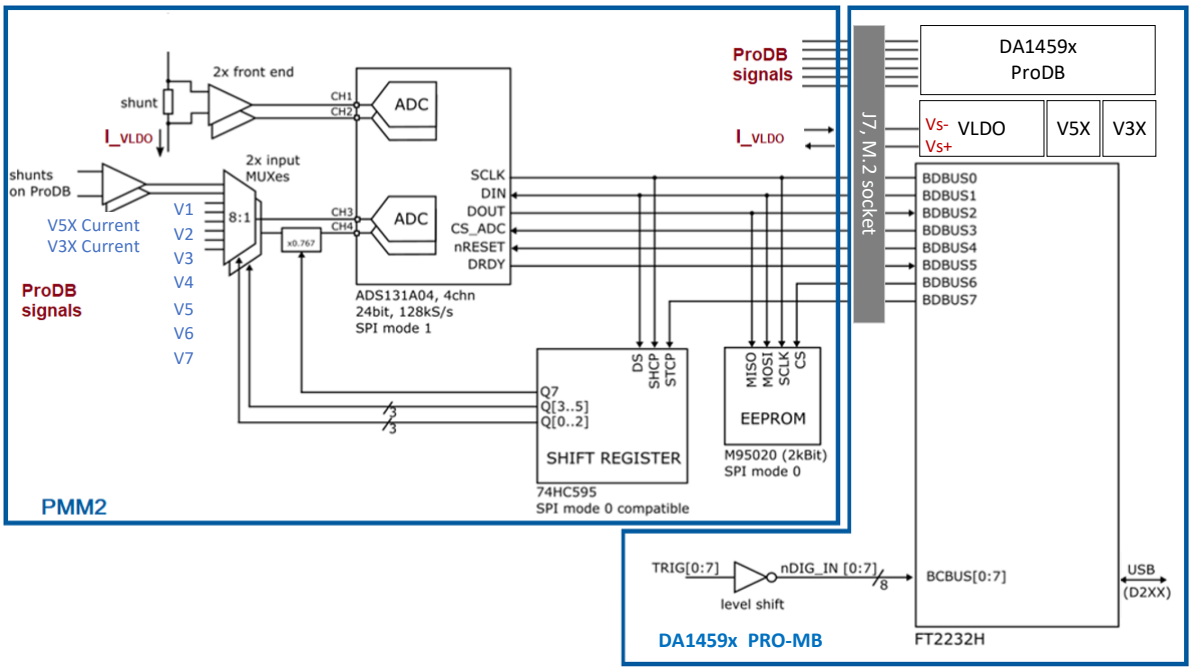


Figure 30. Power measurement module (PMM2) block diagram

An EEPROM is also provided on the module to store production data and allow autodetection from the host software.

The power measurement module (PMM2) is connected to Pro-Motherboard via J7, M.2 socket. PMM2 is supplied from 3.3 V and VCM through power switch U24.

The DA1459x does not employ shunt voltage drop compensation. The voltage drop on the PMM2 is $V_{PMM2\_dropout} = 2.4*I_{VBAT}$. Use cases for the DA1459x rarely draw more than 40-50 mA of current in which case the max voltage drop of about 100 mV due to the PMM2 should not cause problems.

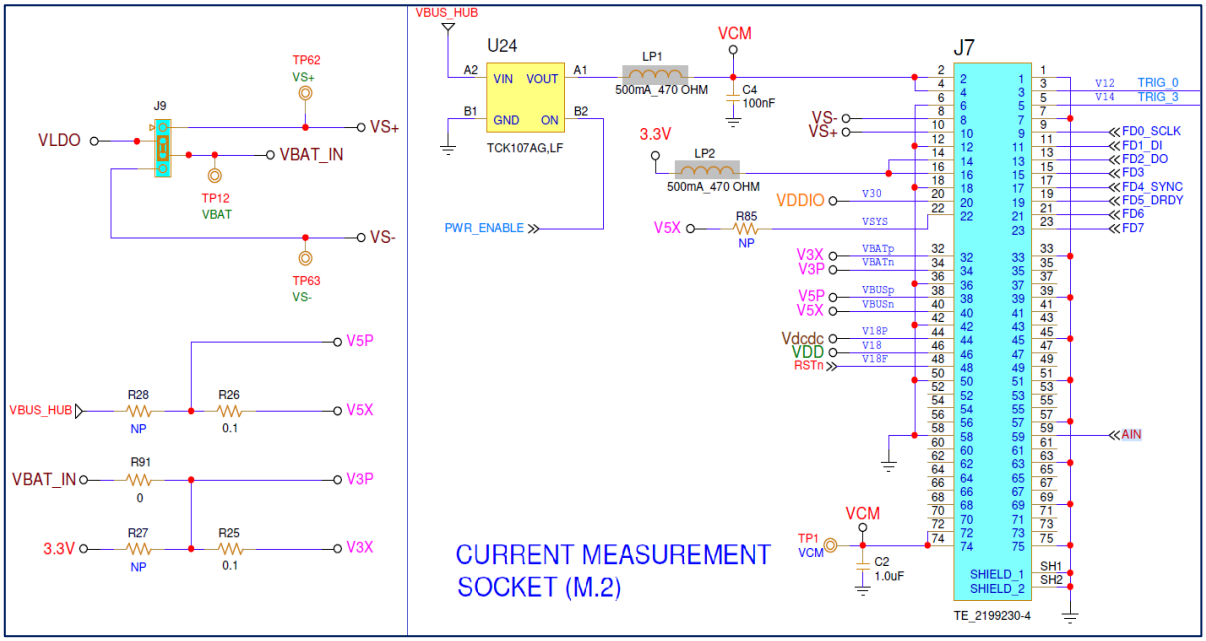


Figure 31. Current measurement socket (M2)

Table 10. Monitored power sources

PMM2 pins (Note 1)	DA1459x signals	Comments
V1	VDDIO	1.8 V voltage rail, applied on pin J7.20. Sourced from Pro-Daughterboard.
V2	V5X	5 V rail powering MikroBUS. It is not activated. For enabling, populate R85 = 0.
V3	Vdcdc	1.1 V voltage rail, applied on pin J7.44. Sourced from Pro-Daughterboard.
V4	VDD	0.9 to 1.2 V voltage rail, applied on pin J7.46. Sourced from Pro-Daughterboard.
V5	RSTn	Reset pin applied on pin J7.48.
V6	TRIG_0	Pin P0_10 or another signal connected on J24.1. Applied on pin J7.3.
V7	TRIG_3	Pin P1_02 or another signal connected on J24.7. Applied on pin J7.5.
V8	AIN	Any signal connected on J3.24. Applied on J7.59.
VLDOp, VLDOn	Vs+, Vs-	DA1459x VBAT current measurement. Sourced from Pro-Motherboard. Current enters PMM2 from Vs+ (pin J7.10) and exits from Vs- (pin J7.8).
C1p, C1n	V3P, V3X	3.3 V voltage rail. V3X current measurement. The current drawn from PMOD.
C2p, C2n	V5P, V5X	5 V voltage rail. V5X current measurement. The current drawn from MikroBUS or PMOD.

Note 1 See PMM2 daughterboard pinout.

There are eight TRIG options defined (TRIG_0 to TRIG_7).

Figure 32 shows the suitable jumper block (J7) allows you to directly select any of the available signals. Any other GPIO can be used as a trigger source by connecting a TRIG pin on J7 with a jumper wire to the desired position at breakout headers (J3, J5).

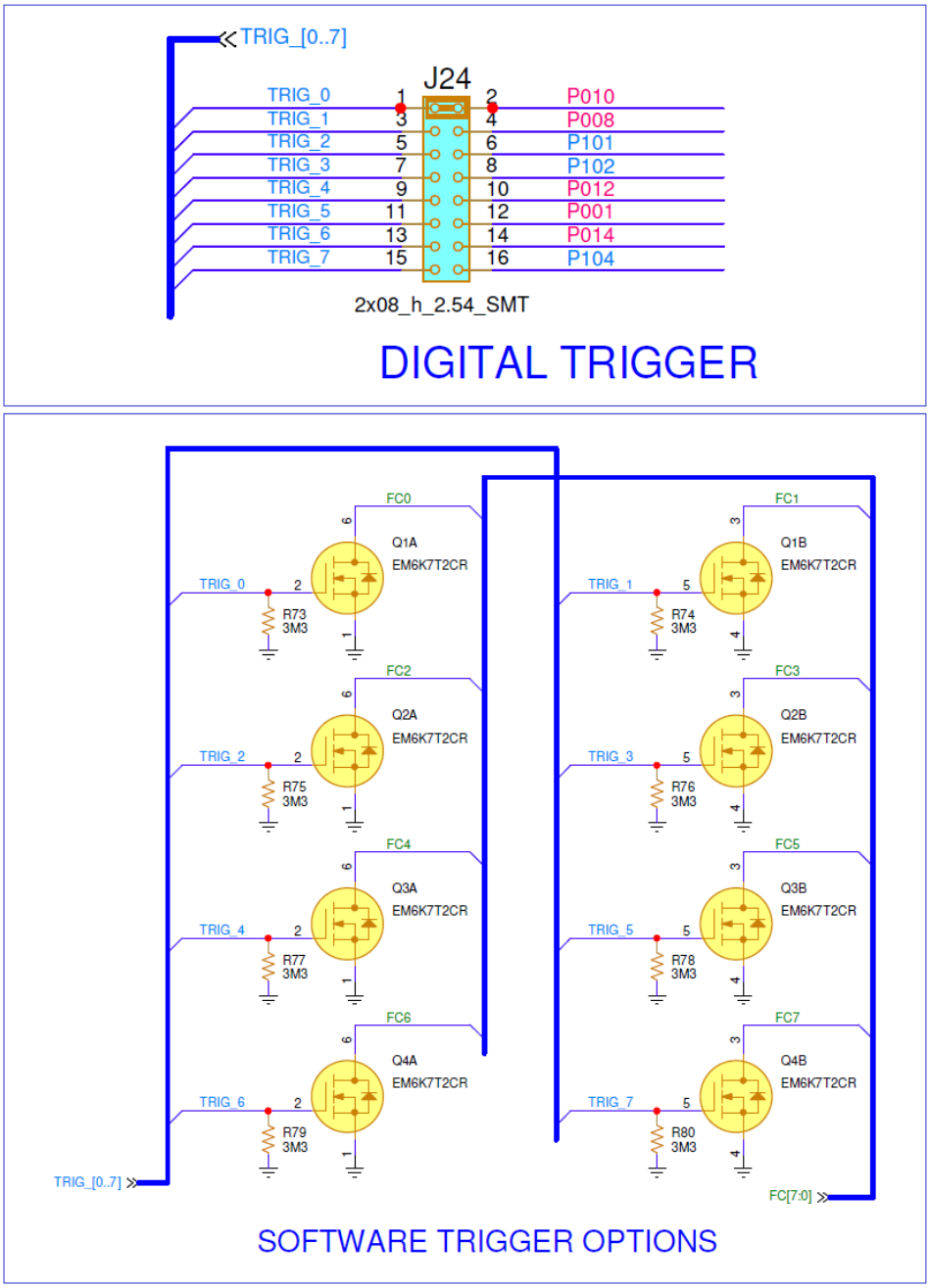


Figure 32. Selection jumper block (J24) and buffer MOSFETS for I/O levels compatibility

The dual Mosfets Q1 to Q4 buffer the signals to provide compatibility with 1.2 to 5 V I/O levels.

Renesas SmartSnippets Toolbox is required for capturing the waveforms of DA1459x system. By using Power profiler, you can monitor simultaneously, on separated windows, the DA1459x VBAT current, two analog waveforms (voltages or currents), and up to eight digital signals, see Figure 33.

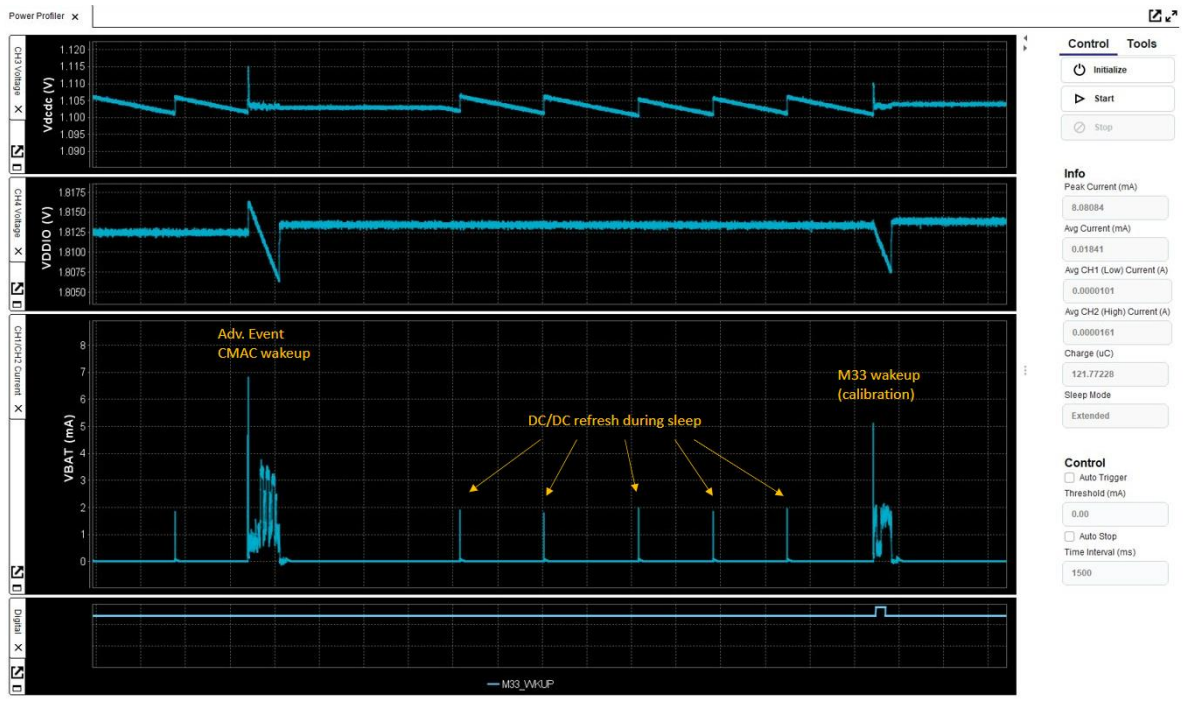


Figure 33. DA1459x waveforms, captured from power profiler of SmartSnippets Toolbox

This functionality, coupled with the digital trigger signals allows profiling the power footprint of software operations and provides a better insight of how the system works. Digital signals can be used either as monitoring signals or as triggers to start/stop capture of data so the user can isolate specific events. The trigger functionality is implemented in SDK.

4.4 The Power Measurement Module 2 (PMM2), (500-29-x)

The power measurement module (PMM2) is an external add-on board that is interfaced (connected) on the Pro-Motherboard via connector J7.

The current measurement unit has the following features:

- Full scale range 640 mA at 3 V (for currents >50-100 mA dropout compensation is recommended – not implemented in the DA1459x Pro DevKit)
- Measure accurately down to 1 µA
- Dedicated Hibernation mode to measure down to 100 nA
- Current sense resistors
  - 2.4 Ω in series to VLDO (located on PMM2)
  - 0.1 Ω in series for measuring current on C1p/C1n (located externally to PMM2)
  - 0.1 Ω in series for measuring current on C2p/C2n (located externally to PMM2)
- Analog processing blocks
- Fast quad channel 24-bit ADC with SPI interface
- FTDI chip for transferring data to the PC
- Software trigger inputs
- System voltage measurement
- External analog input 0-5 V.

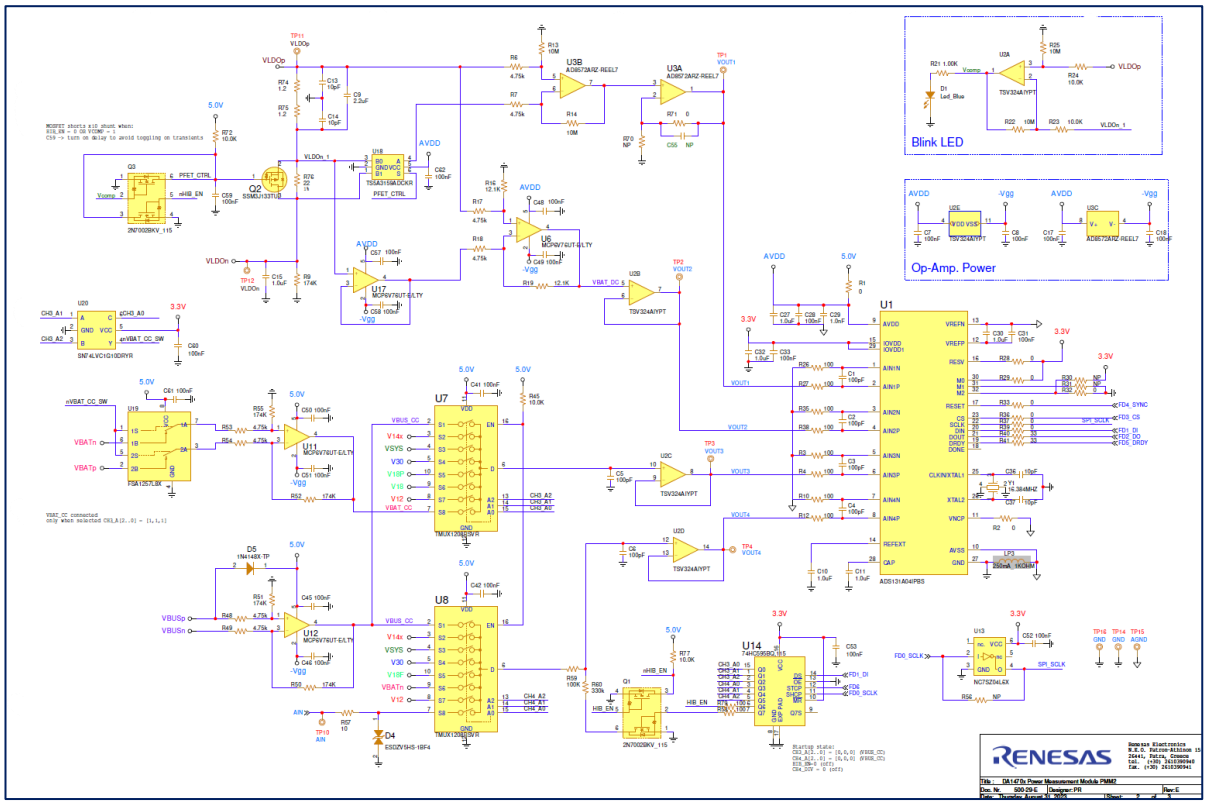


Figure 34. PMM2 current measurement circuit

The input to the circuit is the voltage across the sense resistors R74 and R75. The voltage across the sense resistors is sampled simultaneously by two differential amplifier stages and is converted by the ADC to a digital value. The low range has a conversion gain of 5053 V/A and covers from 1 µA up to about 790 µA. The high scale has a conversion gain of 6.114 V/A and covers up to about 600 mA depending on the VBAT voltage. Both channels are sampled simultaneously, and the host software selects the correct channel using a threshold of 750 µA. R9 provides a constant offset which helps avoid the nonlinear region of the low scale. A blue LED serves as a visual indicator of the range. It switches on close to 750 µA and allows you to have a quick indication of the state of the system (on when active, off when sleeping).

Multiplexers U7 and U8 select among the available system voltages and feed channels 3 and 4 of the ADC. A divider formed by R59 and R60 can be selected on CH4 to allow for 5 V input signal range (the full-scale voltage of the ADC is 4 V). Two analog front ends around U11 and U12 are provided for measuring the C1 (VBATp/n) and C2 (VBUSp/n) currents. The switch in front of U11 prevents the leakage current of the differential amplifier stage from C1 (VBATp/n) to be measured as system current.

A shift register and associated logic control the multiplexers and the rest of the functions of the module. An EEPROM memory is used to store production data and allows the host software to autodetect the module. Charge pump U6 generates a slightly negative voltage (-230 mV) to allow the output of the frontend OPAMPs to reach true zero.

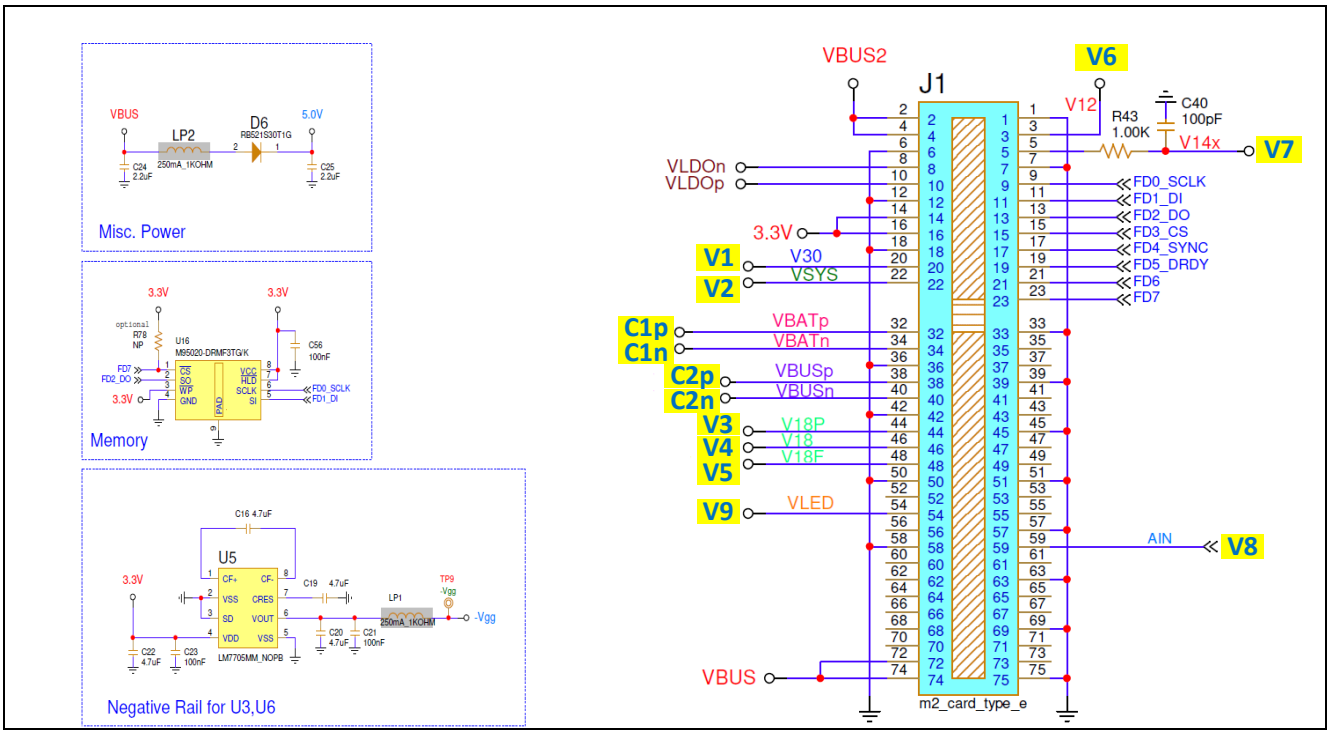


Figure 35. PMM2 on board peripherals (power supply, memory and so on)

The circuit can be set in a Low Current Measurement mode from the host (hibernation mode). This is useful to measure the current of the SoC in Hibernation (Shipping) mode, which is in the order of some hundreds of nA. The measurement range of the circuit in this mode is from 100 nA to 60 µA. This is achieved with a significantly larger sense resistor (R76) which is shorted by Q2 in normal operation. In Hibernation mode, Q2 switches off and R76 is placed in series with R74 and R75 forming a 24.4 Ω sense resistor. The lower sampling point of the low range is moved to the terminals of this series combination with the help of analog switch U18. The high range connections remain unchanged, and it monitors the current through R74 and R75 only. To avoid excessive voltage, drop due to the large sense resistor in case the system wakes up and draws large currents, the LED indicator output also overrides the control of Q2 when the measured current exceeds ~600-700 µA. This ensures that the system can wake up normally and its operation is not affected by the Hibernation mode. The Hibernation mode is intended for measuring low level and mostly stable currents.

The offset of the circuit can be calibrated in the SmartSnippets Toolbox software. The procedure necessitates disconnecting the daughterboard either physically or by sliding the daughterboard power selection switch to the right.

Sampling rate is by default 128 kS/s but can be further reduced to 84 kS/s when using slower machines or lower speed USB ports. All analog and digital signals are sampled simultaneously.

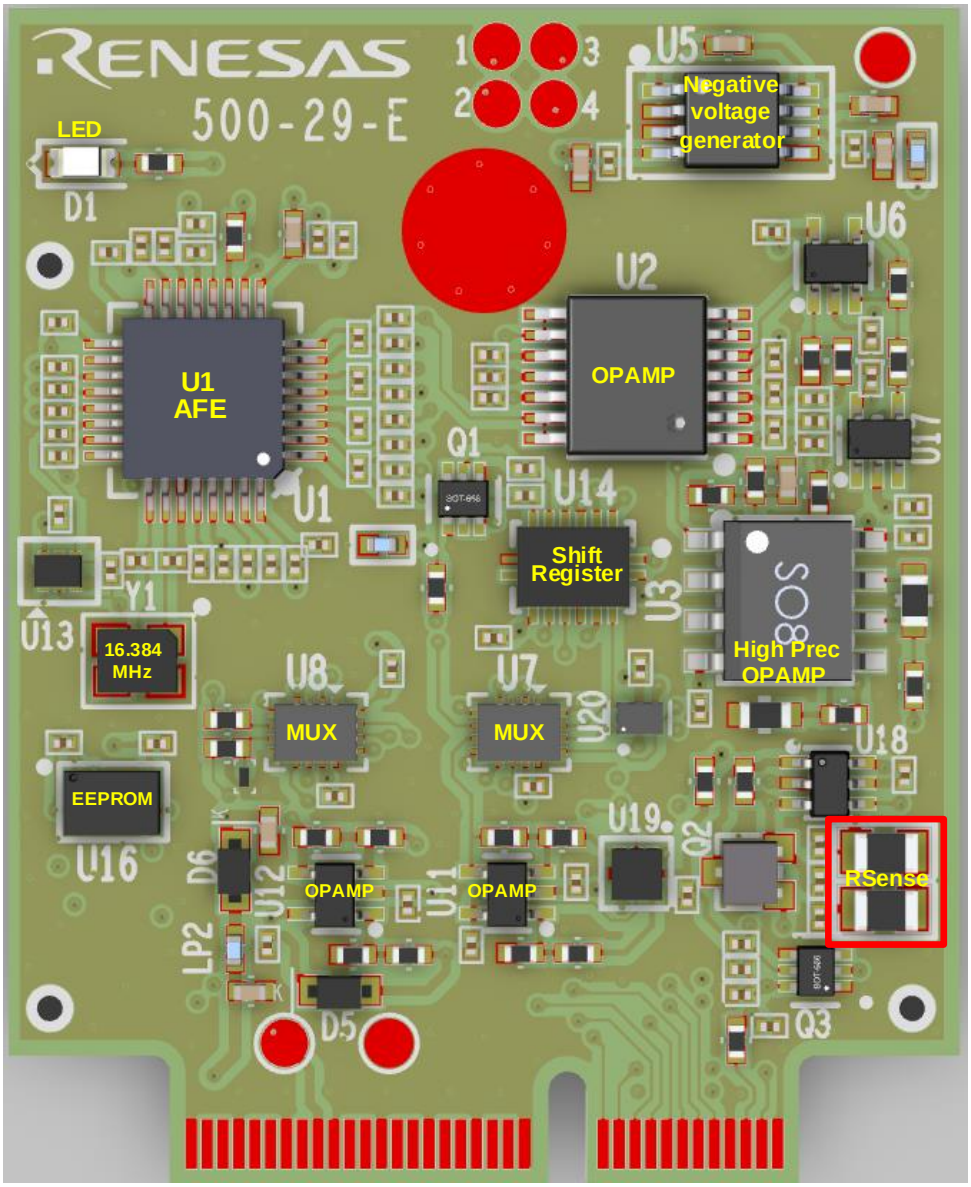


Figure 36. Current measurement unit PCBA (Top)

4.4.1 Accuracy of Current Measurement for VBAT System (VLDO)

The total measuring range of the current measurement circuit of the power measurement module two is 100 nA to 500 mA for VLDO = 3 V, implemented into two scales. The current measurement range is covered by two operating modes, the default (1 µA to 500 mA) and the Hibernation mode (100 nA to 60 µA). Switching from Default to Hibernation mode is done manually over SmartSnippets Toolbox (a version supporting this mode must be used).

The circuit accuracy is measured by applying a constant current, monitoring the same current with an external instrument and the ADC of the PMM2 module, then comparing the two. In general, the inaccuracy presented in the current measurement circuit is less than 5% (practically less than 2%) in most of the current range, (Table 11). Note that the values presented in Figure 37 are averages of multiple points.

Table 11. Accuracy of the current measurement circuit

Channel	Range	Error (%)	Comment
CH1/CH2: VBAT current hibern.	100 nA-60 µA	±15% at 100 nA, <±2% at 1 µA-60 µA	Mode automatically overridden in hardware if current > ~750 µA
CH1/CH2: VBAT current active	1 µA-640 mA	±10% at 1 µA, <±2% at 100 µA-640 mA	2 ranges [1 µA-750 µA/750 µA-640 mA]

Channel	Range	Error (%)	Comment
CH3, CH4 current: C1p/n, C2p/n	1 mA-1 A	±5%	Range and accuracy depend on external R_{sense}. Values shown with 0.1 Ω/1% shunt
CH3 voltage	0-4 V	±2%	
CH4 voltages	0-4 V/0-5 V	±2%	0-5 V range available with 0.776x divider enabled

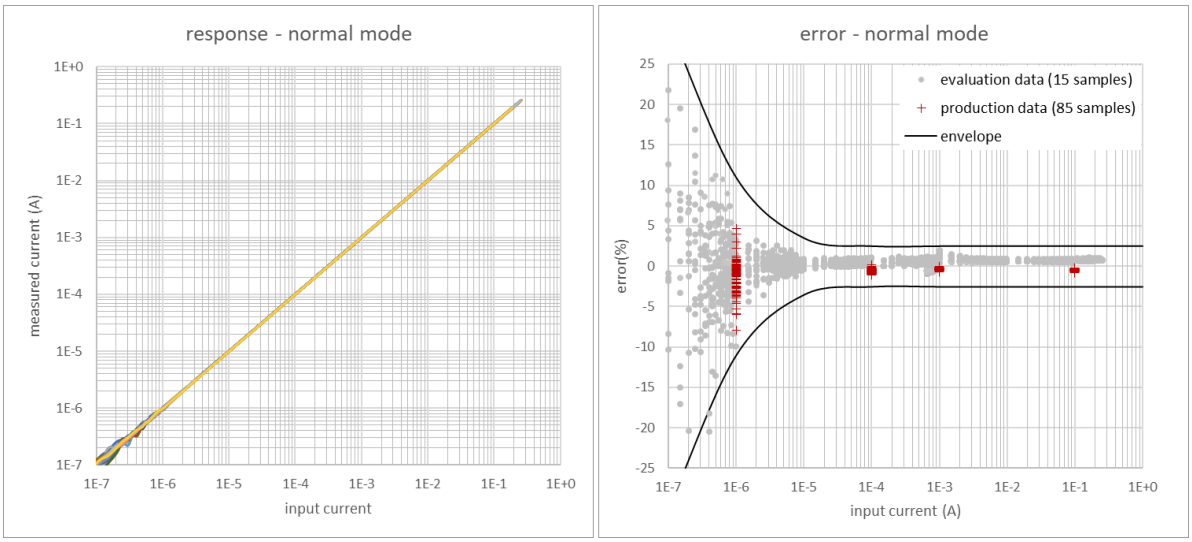


Figure 37. Normal mode (1 µA to 640 mA at 3.3 V) data after offset calibration

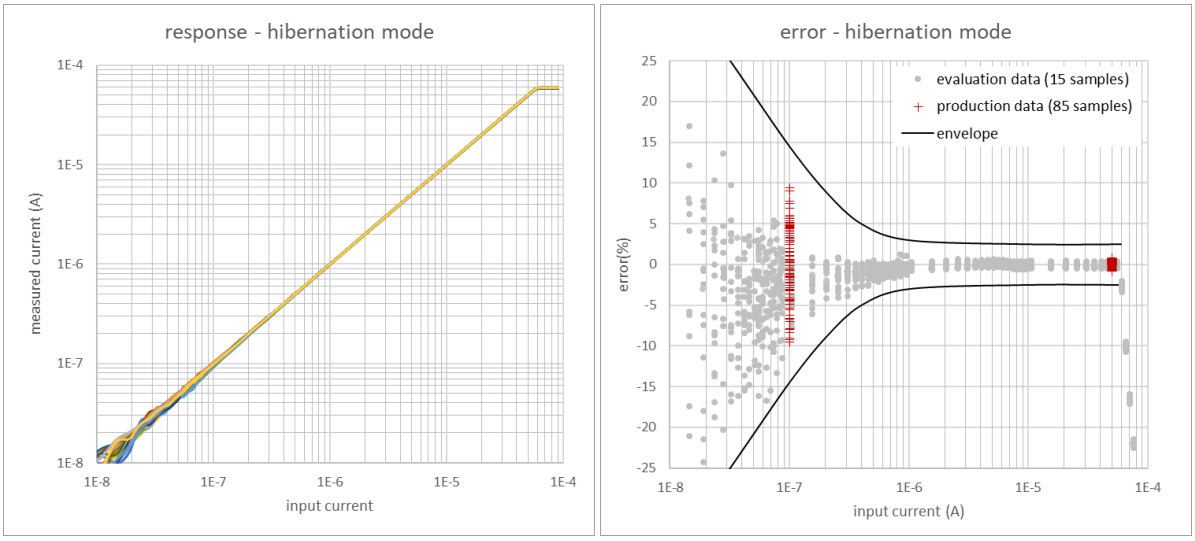


Figure 38. Hibernation mode (100 nA to 60 µA at 3.3 V) data after offset calibration

Appendix A Schematics

A.1 DA1459x Pro-Motherboard Schematic

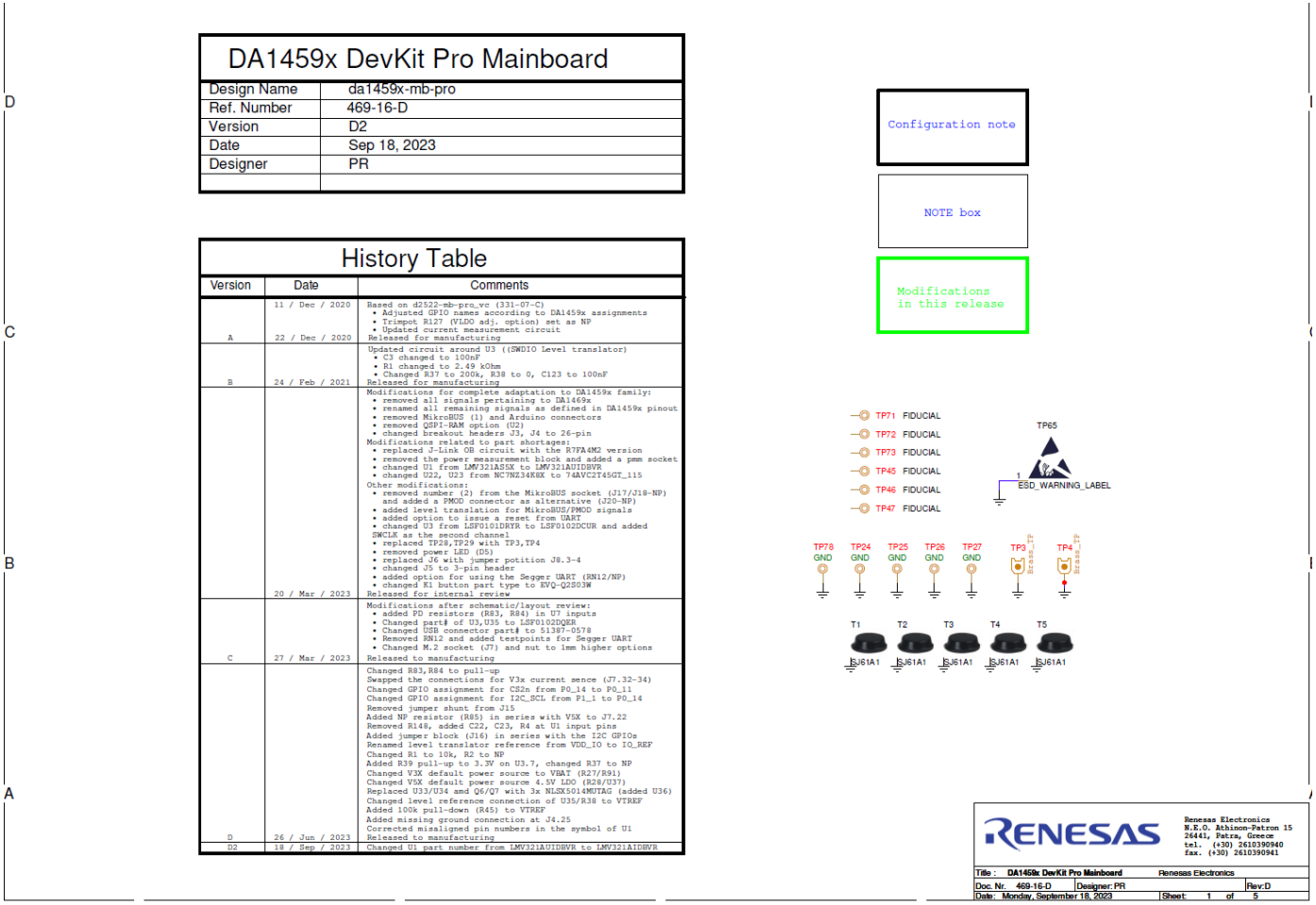


Figure 39. DA1459x Pro-motherboard schematic, modification history page

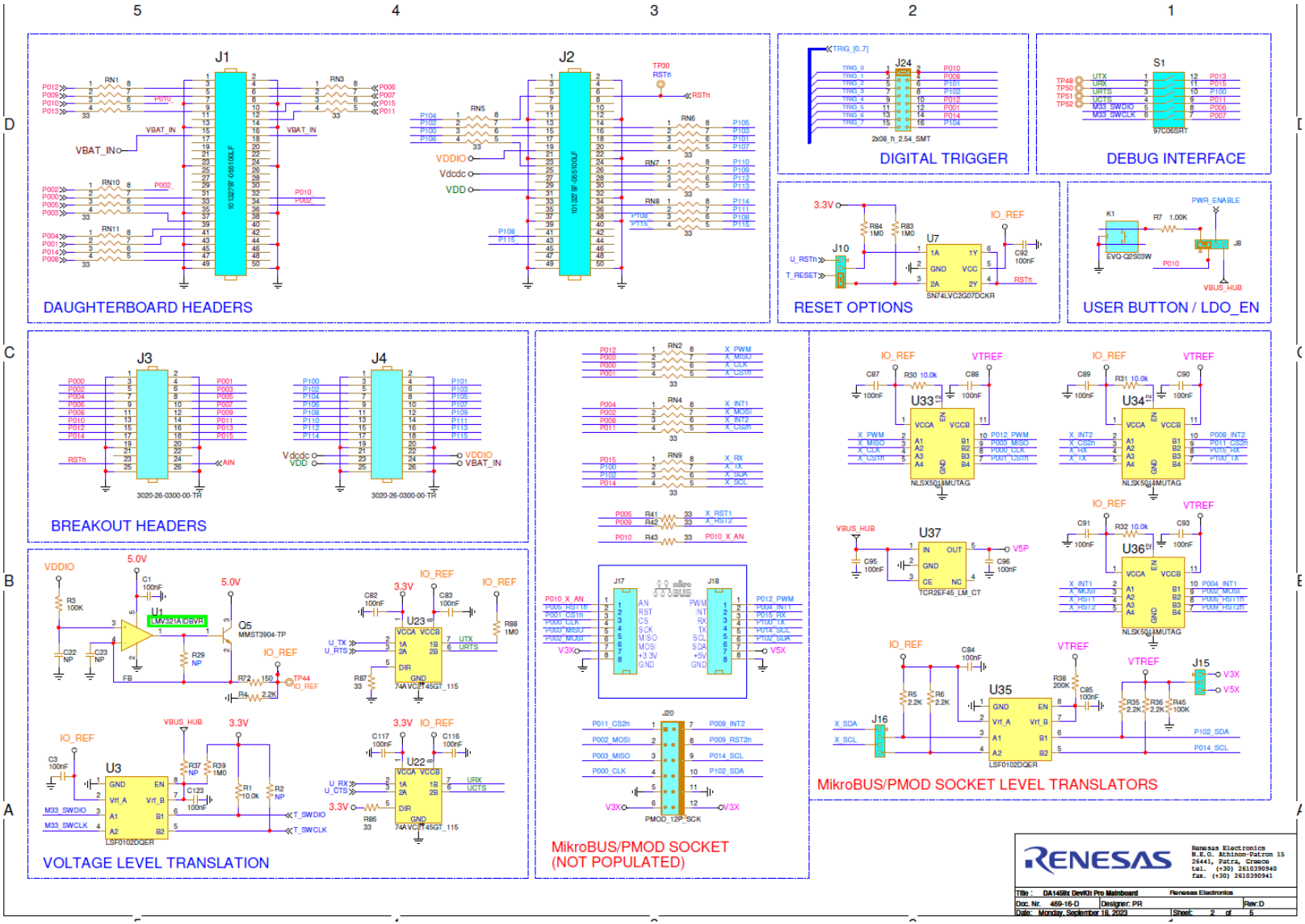


Figure 40. DA1459x Pro-motherboard schematic, connectivity, and level translators

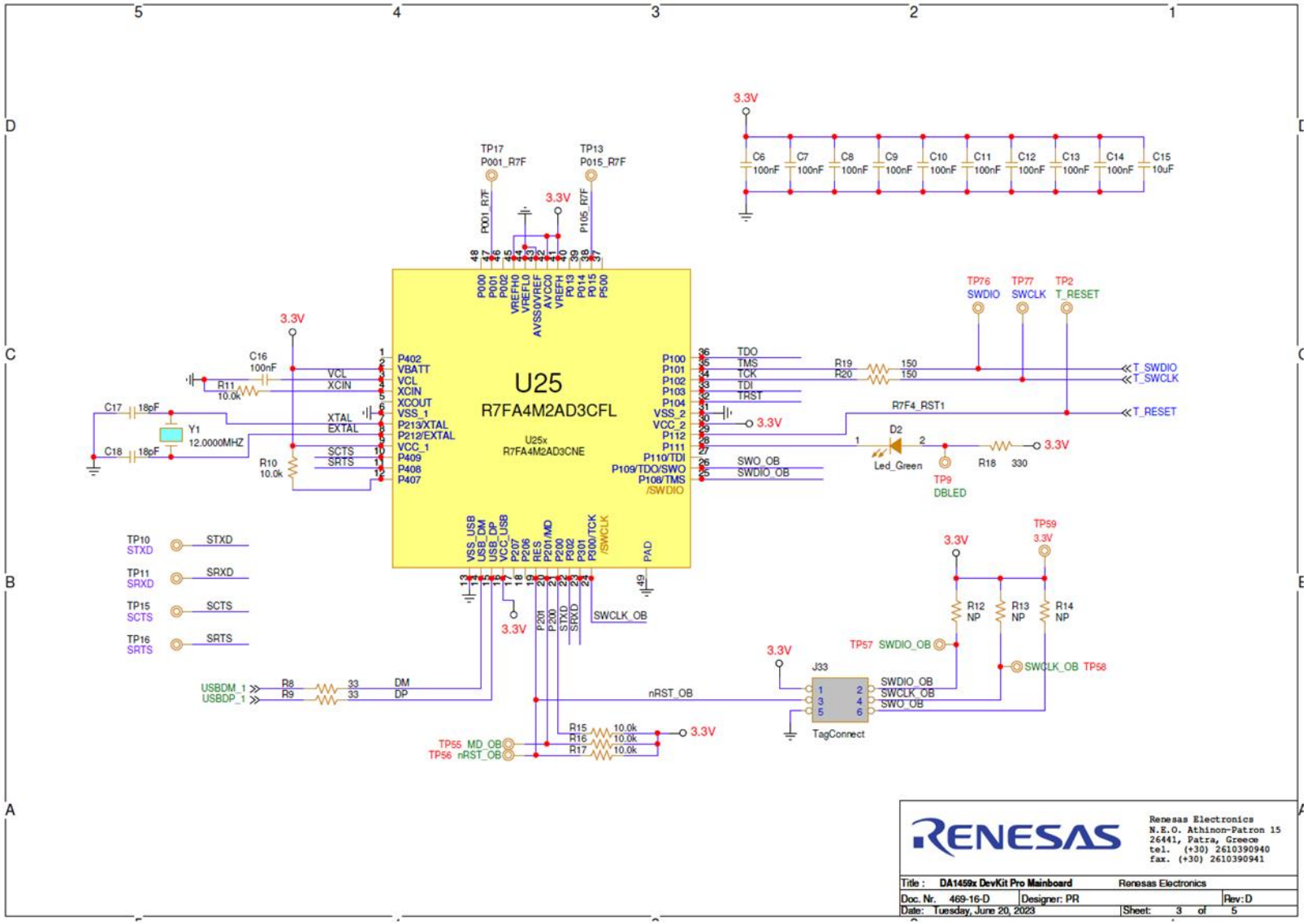


Figure 41. DA1459x Pro-motherboard schematic, SWD implementation

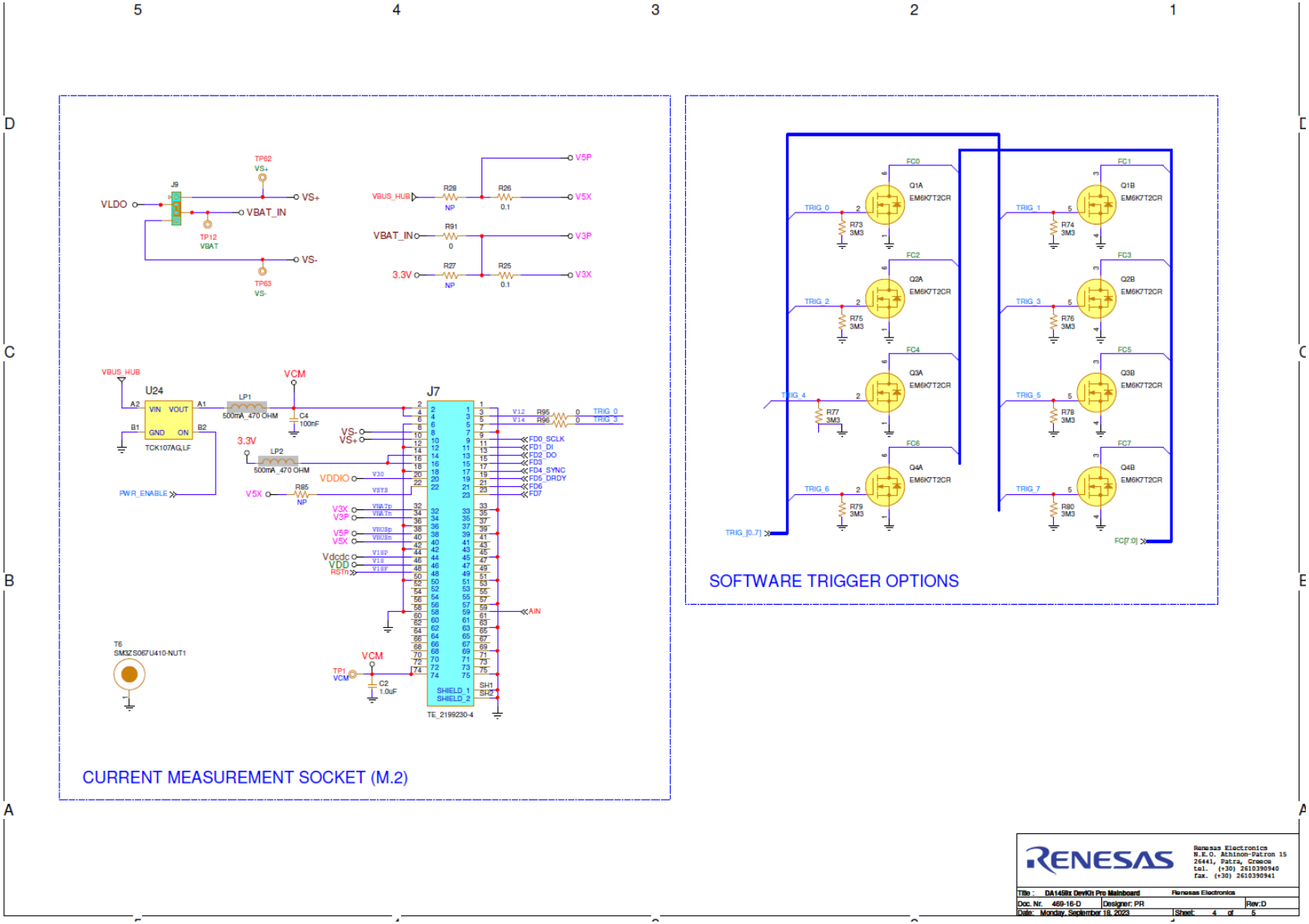


Figure 42. DA1459x Pro-motherboard schematic, PMM2 interface and software trigger buffers

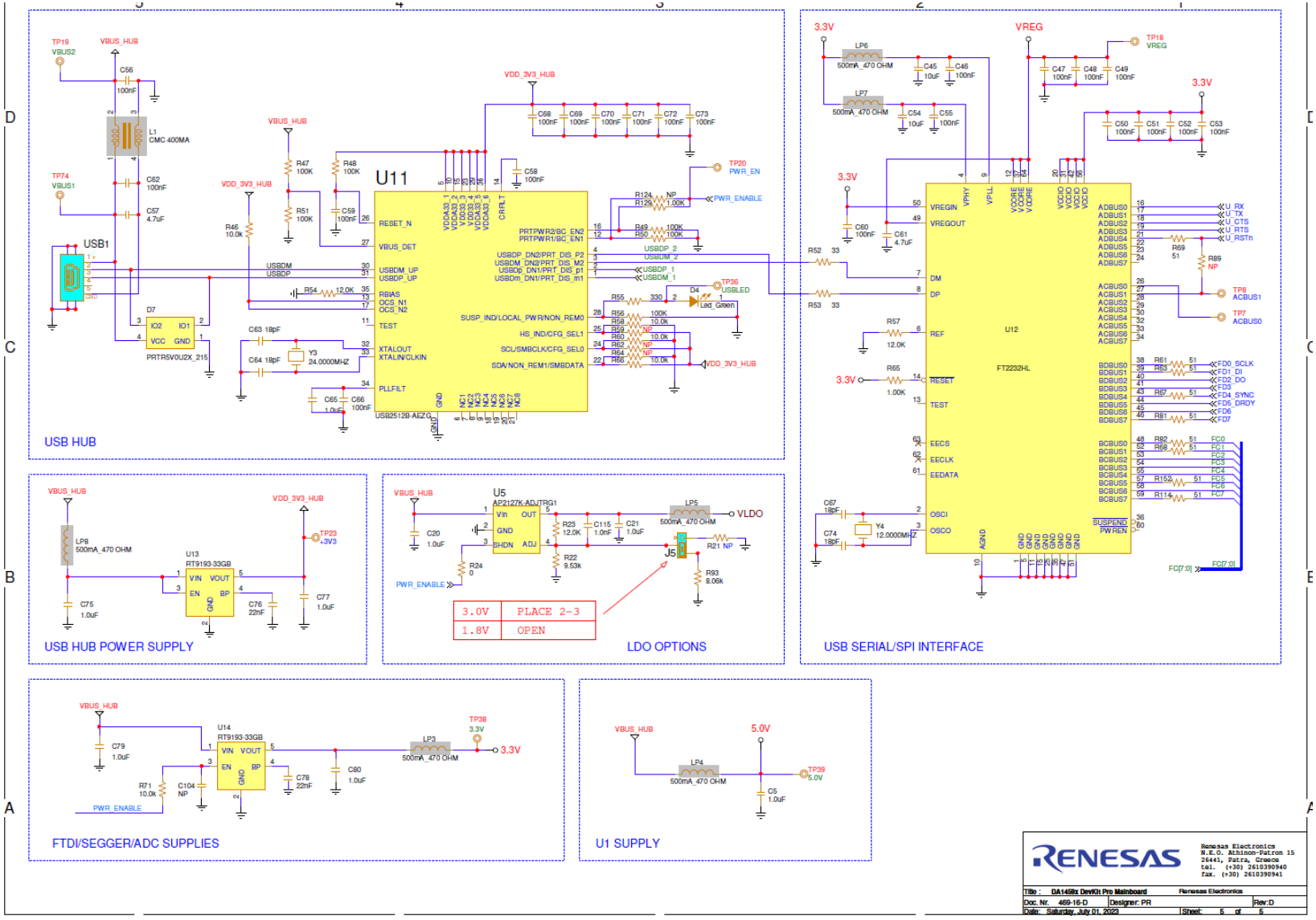


Figure 43. DA1459x Pro-motherboard schematic, USB Hub, UART to USB and power supply

A.2 DA1459x_db_fcqfn52 Schematic

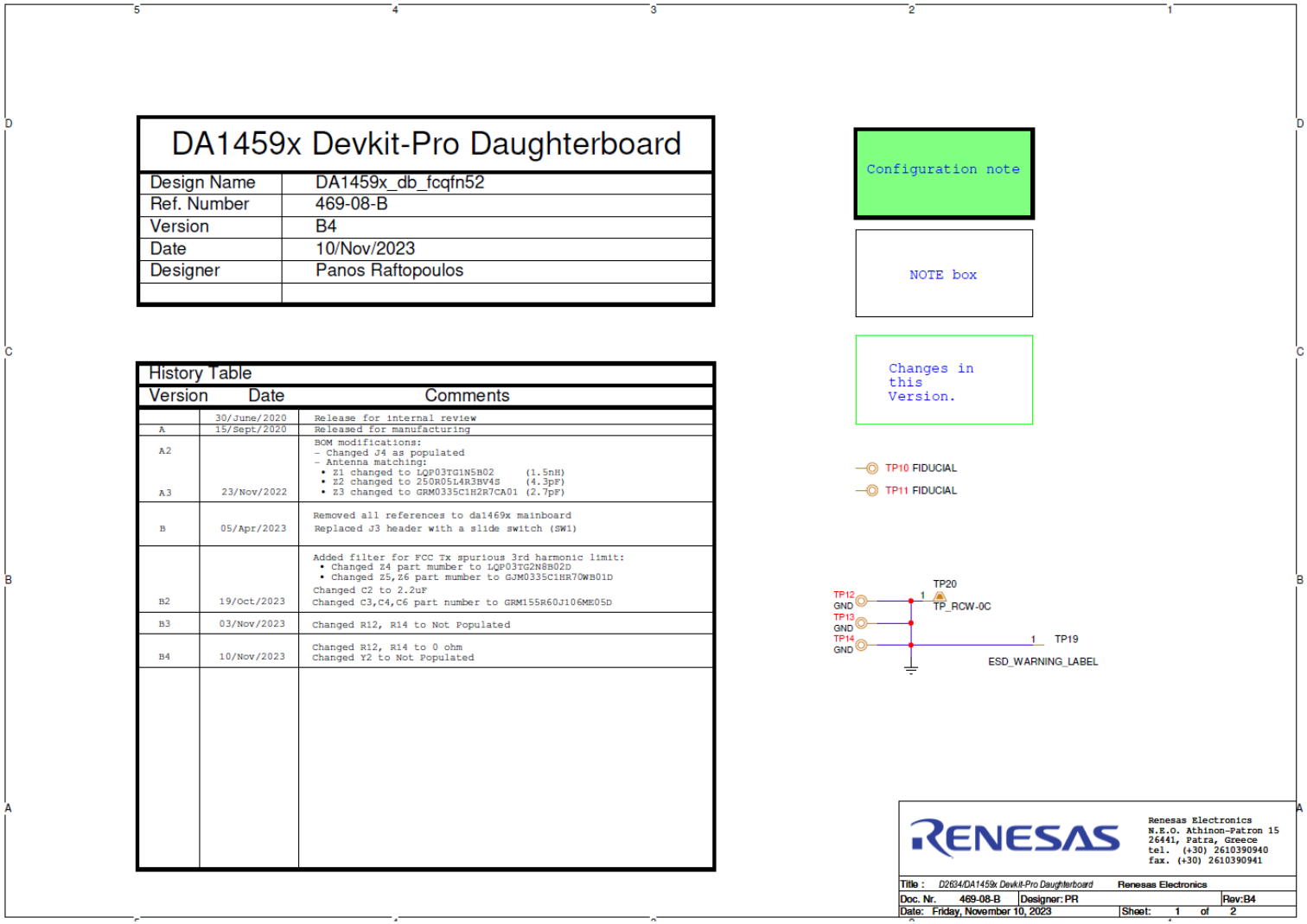


Figure 44. DA1459x_db_fcqfn52, modification history page

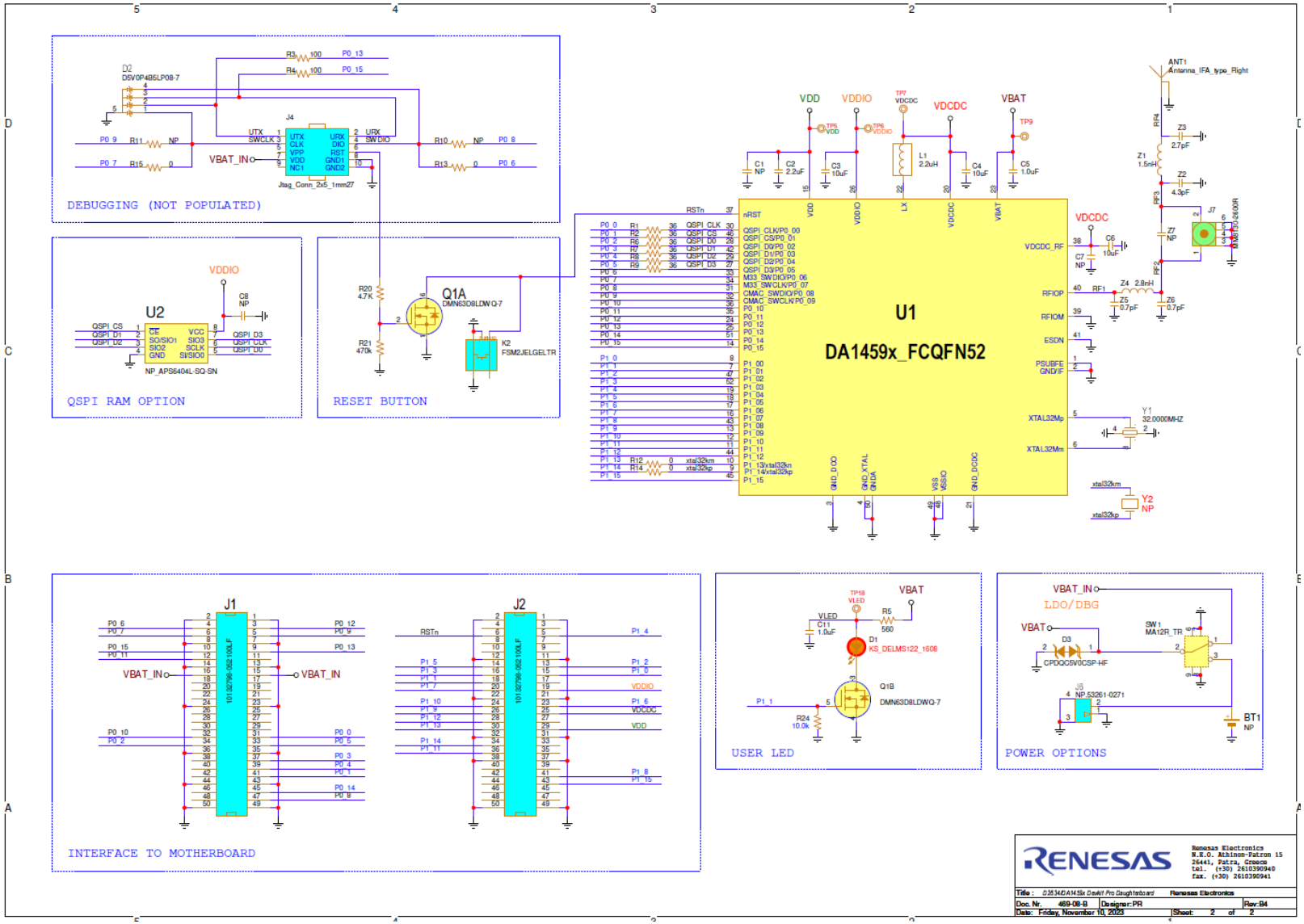
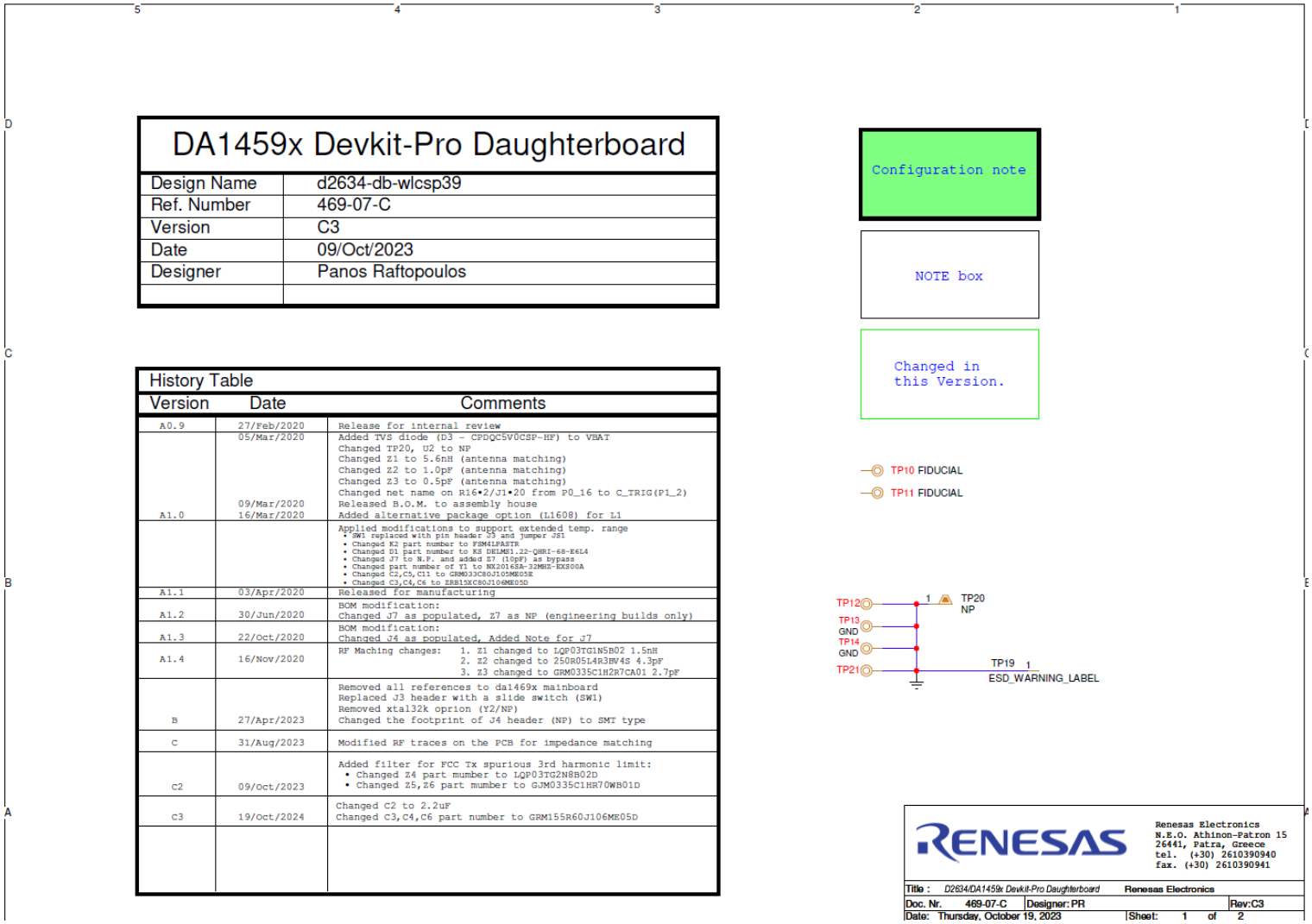


Figure 45. DA1459x_db_fcqfn52, the circuit

A.3 DA1459x-db-wlcsp39 Schematic



DA1459x Devkit-Pro Daughterboard

Design Name	d2634-db-wlcsp39
Ref. Number	469-07-C
Version	C3
Date	09/Oct/2023
Designer	Panos Raftopoulos

History Table

Version	Date	Comments
A0.9	27/Feb/2020	Release for internal review
A1.0	05/Mar/2020 09/Mar/2020 16/Mar/2020	Added TVS diode (D3 - CPDQC5V0CSP-HF) to VBAT Changed TP20, U2 to NP Changed Z1 to 5.6nH (antenna matching) Changed Z2 to 1.0pF (antenna matching) Changed Z3 to 0.5pF (antenna matching) Changed net name on R16•2/J1•20 from P0_16 to C_TRIG(P1_2) Released B.O.M. to assembly house Added alternative package option (L1608) for L1
		Applied modifications to support extended temp. range • SW1 replaced with pin headar S3 and jumper JB1 • Changed K2 part number to FSM4LPASTR • Changed D1 part number to KS DRLMS1.22-QHRI-68-E6L4 • Changed J7 to N.P. and added Z7 (10pF) as bypass • Changed part number of Y1 to NX2016SA-32MHZ-EXS00A • Changed C2,C5,C11 to GRM033C80J105ME05E • Changed C3,C4,C6 to ERB1XC80J106ME05D
A1.1	03/Apr/2020	Released for manufacturing
A1.2	30/Jun/2020	BOM modification: Changed J7 as populated, Z7 as NP (engineering builds only)
A1.3	22/Oct/2020	BOM modification: Changed J4 as populated, Added Note for J7
A1.4	16/Nov/2020	RF Maching changes: 1. Z1 changed to LQP03TG1N5B02 1.5nH 2. Z2 changed to 250R05L4R3HV4S 4.3pF 3. Z3 changed to GRM0335C1H2R7CA01 2.7pF
B	27/Apr/2023	Removed all references to da1469x mainboard Replaced J3 header with a slide switch (SW1) Removed xtal32k oprion (Y2/NP) Changed the footprint of J4 header (NP) to SMT type
C	31/Aug/2023	Modified RF traces on the PCB for impedance matching
C2	09/Oct/2023	Added filter for FCC Tx spurious 3rd harmonic limit: • Changed Z4 part mumber to LQP03TG2N8B02D • Changed Z5,Z6 part mumber to GJM0335C1HR70WB01D
C3	19/Oct/2024	Changed C2 to 2.2uF Changed C3,C4,C6 part number to GRM155R60J106ME05D

Configuration note

NOTE box

Changed in this Version.

TP10 FIDUCIAL

TP11 FIDUCIAL

TP12 TP13 GND TP14 GND TP21 — 1 TP20 NP — TP19 1 ESD_WARNING_LABEL

RENESAS

Renesas Electronics
N.E.O. Athinon-Patron 15
26441, Patra, Greece
tel. (+30) 2610390940
fax. (+30) 2610390941

Title : D2634/DA1459x Devkit-Pro Daughterboard Renesas Electronics
Doc. Nr. 469-07-C Designer: PR Rev:C3
Date: Thursday, October 19, 2023 Sheet: 1 of 2

Figure 46. DA1459x-db-wlcsp39, modification history page

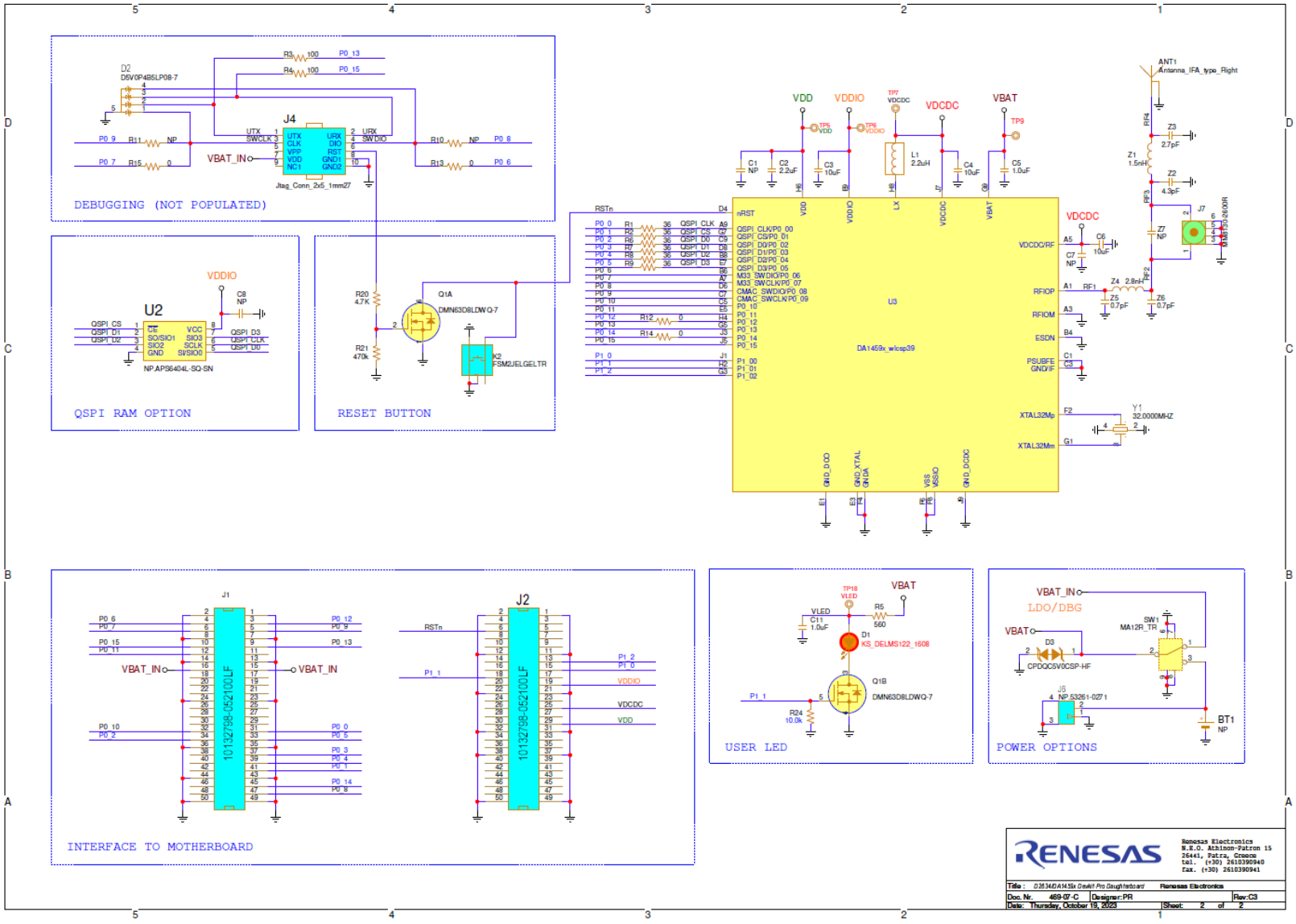


Figure 47. DA1459x-db-wlcsp39, the circuit

Appendix B Conformity Assessment

The DA14592 Daughterboards (FCQFN52 and WLCSP39) and DA1459x Motherboard comply with regulations described in the following subsections.

B.1 FCC Notice (Applicable To Evaluation Kits Not FCC-Approved)

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18, or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

B.2 CE Compliance (Europe)

The DA1459x Pro-motherboard has been tested and found to comply with **EMC Directive (2014/30/EU)** for electromagnetic compatibility. Applicable standards are:

- **EN 55032 (2015) / AC (2016) / A11 (2020) & EN 55035 (2017) / A11 (2020)**.

The DA14592 FCQFN52 and WLCSP39 daughterboards have been tested to **RED 2014/53/EU Essential Requirements for Health, Safety, and Radio**. The applicable standards are:

- **Radio**: EN 300 328 V2.2.2 (2019-07)
- **Health**: EN IEC 62311:2020, IEC 62479:2010
- **Safety**: EN 62368-1:2014 + AC:2015 + A11:2017, IEC 62368-1:2014 + COR1:2015 + COR2:2015
- **EMC**: ETSI EN 301 489-1 V2.2.3 (2019-11), Final Draft ETSI EN 301 489-17 V3.3.0 (2024-07).

Simplified Declaration of Conformity
Hereby, Renesas Design Netherlands B.V. declares that radio type equipment DA14592 FCQFN52 and DA14592 WLCSP39 are in compliance with Directive 2014/53/EU, DA1459x Pro-motherboard is in compliance with **EMC Directive (2014/30/EU)**. The full text of the EU declaration of conformity is available at the following internet address: www.renesas.com

NOTE
For DA14594 Daughterboards (FCQFN52 and WLCSP39) Renesas Declaration of Similarity is applied, www.renesas.com

B.3 UKCA (UK)

The DA1459x Pro-motherboard has been tested and found to comply with the **Electromagnetic Compatibility (EMC) Regulations 2016** (UK) for electromagnetic compatibility. The applicable standards are:

- EN 55032 (2015) / AC (2016) / A11 (2020) & EN 55035 (2017) / A11 (2020).

The DA14592 FCQFN52 and WLCSP39 daughterboards have been tested to meet the **Radio Equipment Regulations 2017** (UK) Essential Requirements for Health, Safety, and Radio. The applicable standards are:

- **Radio**: EN 300 328 V2.2.2 (2019-07)
- **Health**: EN IEC 62311:2020, IEC 62479:2010
- **Safety**: EN 62368-1:2014 + AC:2015 + A11:2017, IEC 62368-1:2014 + COR1:2015 + COR2:2015
- **EMC**: ETSI EN 301 489-1 V2.2.3 (2019-11), Final Draft ETSI EN 301 489-17 V3.3.3 (2024-07)

Simplified Declaration of Conformity
Hereby, Renesas Design Netherlands B.V. declares that radio type equipment DA14592 FCQFN52 and DA14592 WLCSP39 are in compliance with the Radio Equipment Regulations 2017 (UK), and the DA1459x Pro-motherboard is in

Simplified Declaration of Conformity
compliance with the Electromagnetic Compatibility (EMC) Regulations 2016 (UK). The full text of the UKCA declaration of conformity is available at the following internet address: www.renesas.com

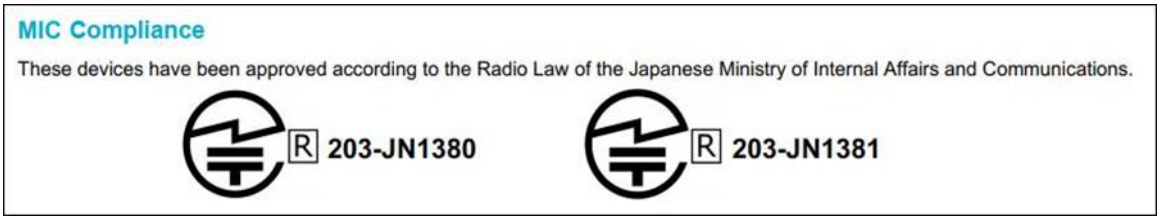
NOTE
For DA14594 Daughterboards (FCQFN52 and WLCSP39) Renesas Declaration of Similarity is applied, www.renesas.com

B.4 MIC (JAPAN)

The DA14592 FCQFN52 and WLCSP39 have received type certification as required to conform to the technical standards regulated by the Ministry of Internal Affairs and Communications (MIC) of Japan pursuant to the Radio Act of Japan.

Model no: DA14592 FCQFN52, MIC ID: 203-JN1380

Model no: DA14592 WLCSP39, MIC ID: 203-JN1381



B.5 WEEE Directive (2012/19/EU)

The Waste Electrical and Electronic Equipment Regulations 2013

For Customers in the UK and European Union

The WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union. This equipment (including all accessories) is not intended for household use. After use, the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled, and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back the end of line equipment. Register for this service at https://www.renesas.com/eu/en/support/regional-customer-support/weee.

B.6 RoHS Compliance

Renesas' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

Revision History

Revision	Date	Description
1.2	Jan 31, 2024	▪ Added Appendix B. ▪ Added DA14594 information. ▪ Converted to Renesas template.
1.1	Mar 1, 2024	Updated schematics to latest revisions. Editorial.
1.0	Nov 30, 2023	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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