

EL7535EVAL1, EL7535IY-EVAL

Evaluation Board

TB448
Rev.0.00
Feb 17, 2005

Using the Evaluation Board

EL7535 is a high efficiency 350mA synchronous step-down PWM regulator in a tiny MSOP10 package. The internal compensation makes it possible for the full-featured 350mA converter to occupy less than 0.18in² of PCB area with all components on one side.

1. Output Adjustment

Use R₁ and R₂ to adjust output voltage according to the following formula:

$$V_O = 0.8 \times \left(1 + \frac{R_2}{R_1} \right)$$

The evaluation board is set to V_O = 1.8V.

2. Chip Enable

When EN pin is pulled to Ground, the regulator is disabled. It consumes less than 1μA of current. R₅ can be connected to V_{IN} directly if this function is not needed, reducing the component counts.

3. RSI/POR Function

When powering up, the open-collector Power-On-Reset output holds low for 100ms after V_O reaches the preset voltage. When a reset signal RSI is issued, POR goes to low for the same period of time while the output power is still on (Please refer to the datasheet for the timing diagram). When the function is not used, connect RSI to ground and leave R₄ open, further reduce the total components counts and the overall PCB area to less than 0.18in².

The POR output also serves as a 100ms delayed Power Good signal when the pull-up resistor R₄ is installed. The RSI pin needs to be directly (or indirectly through R₆) connected to Ground for this to function properly.

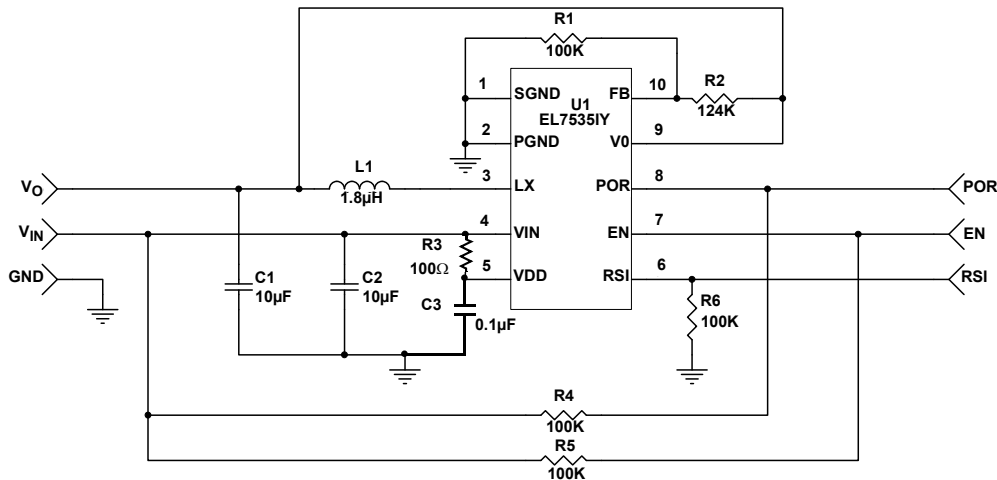


FIGURE 1. DEMO BOARD SCHEMATIC

Evaluation Board Bill of Materials

REFERENCE DESIGNATOR	VALUE	PACKAGE	MANUFACTURER	MANUFACTURER'S PART NUMBER	MANUFACTURER'S PHONE NUMBER
C ₁ , C ₂	10μF/MLCC, X7R	1206	TDK	C3216X7R1A106K	847-803-6100
C ₃	0.1μF	0603/0402	Any		
L ₁	1.8μH		Coilcraft	1008PS-182M	847-639-6400
R ₂	124K, 1%	0603/0402	Any		
R ₁ , R ₄ , R ₅ , R ₆	100K, 1%	0603/0402	Any		
R ₃	100Ω, 1%	0603/0402	Any		
U ₁	EL7535IY	MSOP10	Intersil	EL7535IY	888-ELANTEC

Demo Board Layout (Actual Size - 3" x 2")

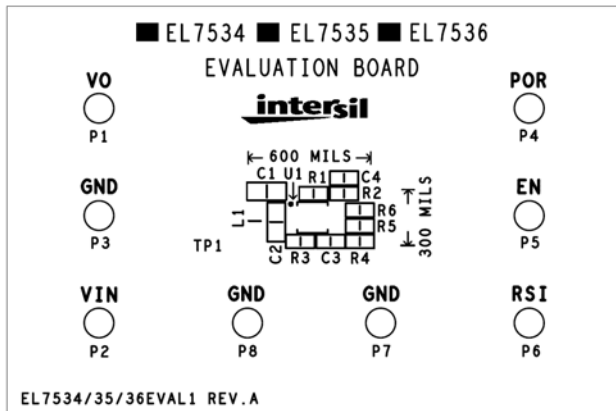


FIGURE 2. SILKSCREEN

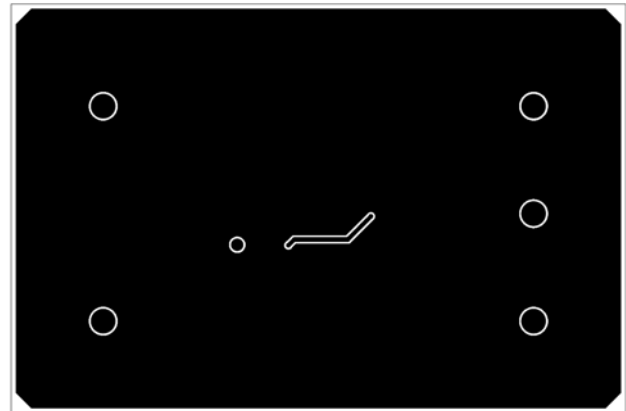


FIGURE 4. BOTTOM LAYER

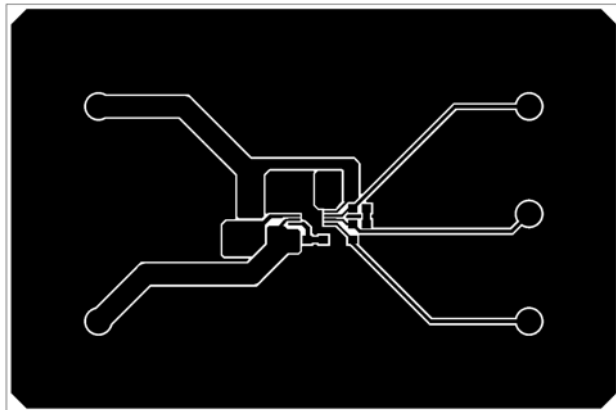


FIGURE 3. TOP LAYER

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