ISL70005SEHEV2Z

The ISL70005SEHEV2Z evaluation board evaluates the performance of the ISL70005SEH 3A buck regulator and 1A source/sink LDO. The same board can be used to demonstrate the ISL73005SEH part, which is the same silicon die offered with different radiation assurance screening. The evaluation board is optimized for 3V to 5.5V input operation to generate a 3A, 1.8V to 3.3V buck output and a 1A source/sink, 1.2V LDO output. Input and output connections, toggle switches, and jumper settings on the board provide the customer an easy-to-use evaluation platform for dual rail supplies for point-of-load, FPGA, and DDR memory power.

Key Features

- Dual point-of-load regulator: 3A buck and 1A source/sink LDO
- Fully independent enable, soft-start, and power-good indicator
- 3V to 5.5V operating voltage
- On-board transient load current generators

Specifications

- Analog and buck regulator input voltage range (PVIN): 3V to 5.5V
- Maximum buck output current: 3A
- Buck preset switching frequency: 1MHz
- LDO input voltage (L_VIN) range: 1.0V to PVIN
- Maximum LDO output (L_OUT) current: 1A sourcing or 1A sinking
- Board dimension: 13.75cm width x 8cm height
- Board layers: Four
- Board PCB copper weight: 2oz.
- Board revision: B

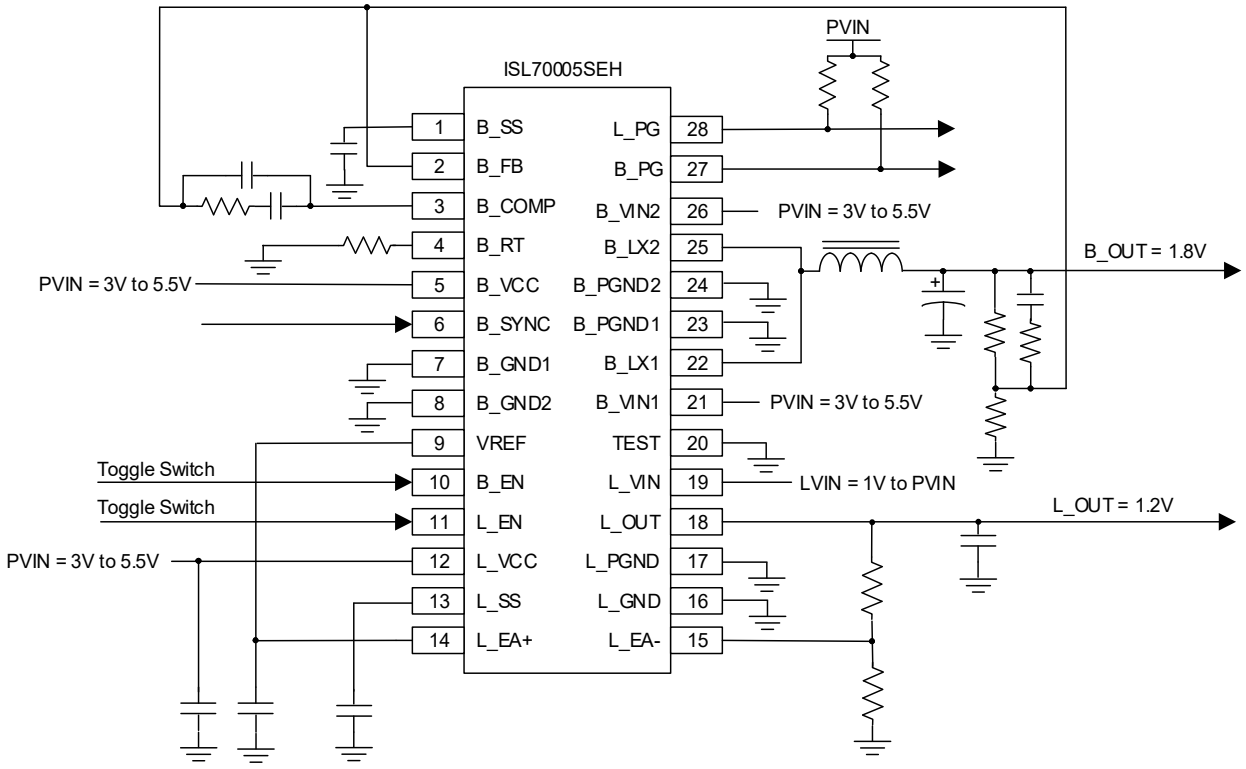

Figure 1. ISL70005SEHEV2Z Block Diagram

Contents

1. Functional Description

1.1 Operating Range

The ISL70005SEHEV2Z has two input supply rails. One for the analog supply and buck power stage input (PVIN) and the other for the LDO input (L_VIN). The PVIN accepts an input voltage range of 3V to 5.5V while the L_VIN accepts an input voltage of 1.0V up to PVIN.

The buck regulator output (B_OUT) is capable of sourcing up to 3A. The buck output voltage is board jumper selectable at 1.8V, 2.5V, 3.3V, or 4.0V. The buck regulator is preset with 1MHz switching frequency with a 2.2µH output inductor and 150µF output capacitor with the option of being synchronized to an external clock. The LDO regulator output (L_OUT) is capable of sourcing or sinking up to 1A. The LDO reference input (L_EA+) to the error amplifier is board jumper selectable to either the 0.6V VREF pin voltage on the ISL70005SEH or ½ the buck output voltage for DDR VTT rail applications. The LDO output voltage is board jumper selectable to 1.2V or set to equal the L_EA+ reference voltage.

On-board transient load generators are available for both the buck and LDO for evaluation purposes.

1.2 Quick Start Guides

1.2.1 Dual Independent Buck and LDO Output

1. See Table 1 to set up the jumpers properly to adjust the buck output voltage and configure the LDO for independent output.
2. Ensure jumper on JP1, JP4, and JP10 are removed. Populate jumper JP6 in the 1-2 position.
3. Apply voltage (3V to 5.5V) to PVIN banana connectors BA1 and BA2.
4. Apply voltage (1.5V to PVIN) to L_VIN banana connectors BA5 and BA7.
5. If the buck enable switch SW1 is on (up position), the buck is enabled and switching at 1MHz. A voltage defined by the jumper settings of JP2 and JP3 is present on B_OUT at BA3. If SW1 is off (down position), the buck is disabled and B_OUT = 0V.
6. If the LDO enable switch SW2 is on (up position), the LDO is enabled and a voltage of 1.2V is present on L_OUT at BA6. If SW2 is off (down position), the LDO is disabled and L_OUT = 0V.

Table 1. Jumper Settings for ISL70005SEHEV2Z

Jumper	Function	Description	Application Configuration	
			Independent Buck and LDO Regulator	Buck and LDO for DDR Power
JP1	Connects B_EN and L_EN Together	Populate for single switch control of L_EN and B_EN.	Remove jumper	Populate jumper
JP2	Connects R8 to B_FB	Populate for buck output voltage 3.3V. Ensure JP3 is removed. If no jumper present on JP2 and JP3, buck output voltage is 1.8V. If JP2 and JP3 both have a jumper, buck output voltage is programmed to 4V.	-	-
JP3	Connects R7 to B_FB	Populate for buck output voltage 2.5V. Ensure JP2 is removed. If no jumper present on JP2 and JP3, buck output voltage is 1.8V. If JP2 and JP3 both have a jumper, buck output voltage is programmed to 4V.	-	-
JP4	Shorts resistor R21	Populate for LDO unity gain, setting L_OUT = L_EA+.	Remove jumper	Populate jumper

Table 1. Jumper Settings for ISL70005SEHEV2Z (Cont.)

Jumper	Function	Description	Application Configuration	
			Independent Buck and LDO Regulator	Buck and LDO for DDR Power
JP5	External signal input to SW3	Do not populate with jumper. This is a 2-pin header for connecting an external signal to drive the HI input of HIP2100 when SW3 is in the 2-3 position.	-	-
JP6	Connects L_EA+ to VREF or buck output	Populate in the 1-2 position for connecting L_EA+ to VREF pin. Populate in the 2-3 position for connecting to buck output voltage divided down by the ratio of R15 and R14.	Jumper in 1-2 position	Jumper in 2-3 position
JP9	Connects L_OUT to transient load generator	Populate for connecting to on board LDO transient load generator.	-	-
JP10	Connects buck V_{OUT} to resistor divider	Populate for connecting buck V_{OUT} to the R14 and R15 resistor divider network.	Remove jumper	Populate jumper
J1	Connects R18 to BNC1	Populate for enabling the sinking transient load current generator on LDO.	-	-
J2	Connects R19 to BNC1	Populate for enabling the sourcing transient load current generator on LDO.	-	-
J3	L_OUT voltage sensing	Do not populate with jumper. This is a 2-pin header for sensing LDO output voltage.	-	-
J4	Buck B_LXx voltage sensing	Do not populate with jumper. This is a 2-pin header for sensing buck regulator switching node.	-	-
J5	PVIN voltage sensing	Do not populate with jumper. This is a 2-pin header for sensing PVIN voltage.	-	-
J6	L_VIN voltage sensing	Do not populate with jumper. This is a 2-pin header for sensing LDO input voltage.	-	-
J7	B_OUT voltage sensing	Do not populate with jumper. This is a 2-pin header for sensing buck output voltage.	-	-

1.2.2 Buck with LDO in DDR Tracking Mode

1. See Table 1 to set up the jumpers properly to adjust the buck output voltage and configure the LDO for tracking buck output.
2. Ensure jumper on JP1, JP4, and JP10 are populated. Ensure either SW1 or SW2 is off (down position). Populate jumper JP6 in the 2-3 position.
3. Place a banana cable from BA3 to BA5 to connect B_OUT to L_VIN.
4. Apply voltage (3V to 5.5V) to PVIN banana connectors BA1 and BA2.
5. Because JP1 is populated, connecting B_EN and L_EN together, either SW1 or SW2 toggle switch enables (up position) and disables (down position) both the buck and LDO together.
6. The LDO L_OUT (VTT rail) is one-half of the buck output voltage (VDDQ rail) determined by the jumper settings on JP2 and JP3.
7. **IMPORTANT:** With the buck output powering the LDO input, care must be taken on the output current loading of the buck regulator. When the LDO is sourcing current, it is supplied by the buck regulator and the buck output B_OUT 3A limit to external loading is decreased by the LDO load. For example, if LDO is sourcing 1A, the buck can only provide an additional 2A to the external load.

1.3 Changing Output Voltage on Buck

Jumpers JP2 and JP3 are made available to easily configure the buck output voltage quickly. With no jumpers on JP2 and JP3, the output voltage is 1.8V. With JP3 only populated, it is 2.5V. With JP2 only populated, it is 3.3V. If JP2 and JP3 are both populated, it is 4V. If a different output voltage is needed, you must change the R7, R8, or R43 values. Renesas recommends not changing R10 to preserve the characteristics of the Type III compensation network.

Table 2. Buck V_{OUT} Jumper Settings

V_{OUT} (V)	JP2 Jumper	JP3 Jumper
1.8	Off	Off
2.5	Off	On
3.3	On	Off
4V	On	On

Note: The buck regulator has minimum on and off times on the B_LXx pins, combined with the switching frequency, can hit duty cycle limitations for producing the desired output voltage.

1.4 Changing Buck Switching Frequency

The ISL70005SEHEV2Z is configured for 1MHz switching by using a R4 = 45.3kΩ resistor on B_RT pin to B_GND. The evaluation board includes a 2.2µH inductor and 150µF tantalum capacitor for the LC output filter. If you need to select a different switching frequency, see Figure 2 for selecting the appropriate R4 value on B_RT to set the switching frequency. The ISL70005SEHEV2Z includes a dual footprint for the inductor to allow for a higher inductance value with similar saturation current characteristics for the lower switching frequencies.

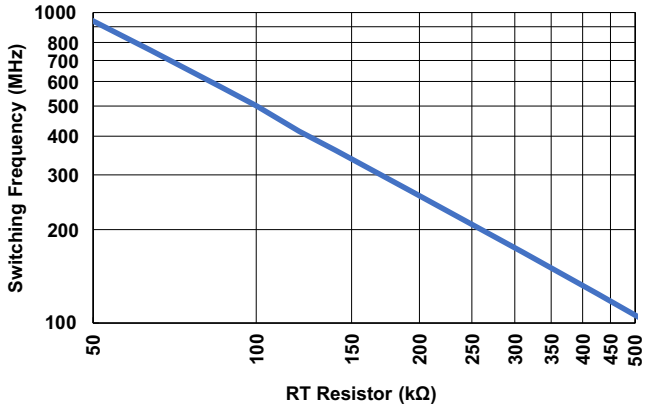

Figure 2. Buck f_{SW} vs RT Resistor on B_RT Pin

1.5 Using External Clock for Buck Switching Frequency

If you need to synchronize the buck switching frequency to an external clock, a test point TP1 is made available for connection. Refer to the *ISL70005SEH Datasheet* for more information about external synchronization.

1.6 Changing Buck Output Inductor

The ISL70005SEHEV2Z is populated with a 2.2µH inductor on the L1A footprint targeted for 1MHz switching frequency. The inductor used on the ISL70005SEHEV2Z is a Coilcraft XFL4020-222ME. If you need to use a lower switching frequency, a larger inductance must be used to maintain a similar ripple current. The L1B footprint (inductor not populated) is physically larger to accommodate a larger inductance value with similar saturation current ratings. For example, with f_{SW} = 100kHz the L1B footprint is sized to accommodate a Coilcraft XAL6060-153ME 15µH inductor.

1.7 Using the Buck Regulator Transient Load Generator

An on-board load transient generator is made available to the buck regulator output. This circuit is shown in Figure 7 and comprises of an open-drain active NMOS FET load switch driven by a Renesas HIP2100 N-MOSFET driver. The HIP2100 requires 10V bias applied between TP9 (positive) and TP5 (GND) for proper operation. The load current is set by a resistance R_{LOAD} inserted between the NMOS drain and buck output voltage B_OUT. Six 2512 sized resistor SMD pads (R32-R34; R40-R42) are made available for you to connect the desired resistance.

To control the load transient timing with an external signal, put switch SW3 in the down position (2-3). Connect the external pulse generator to the JP5 2-pin header. The HIP2100 uses TTL inputs and requires 0V-10V signal levels. Logic high drives the load on and logic low turns off the load.

The HIP2100 can be configured in an a-stable oscillation state where the load current is periodically pulsed, with the transient duration set by RC timing components. To set the HIP2100 in a-stable state, ensure switch SW3 is in the up position (1-2). In the first state, assume driver output HO = 0V, which turns MOSFET Q2 off. This allows R28+R29 to charge up C34 with an RC time constant τ = (R28+R29) × C34. When the voltage across C34 (which is connected to HI) reaches the logic-high threshold of HI, HO goes into the second state and drives to a voltage HO = VDD. HO drives the Q3 MOSFET gate with turn-on (R30) and turn-off (R31) gate-limiting resistors. When HO is high, Q3 is on, and the buck output is loaded by the resistance across B_OUT and Q3 drain, with the load current I_{LOAD} = B_OUT/R_{LOAD}. At the same time when HO is high, Q2 is on discharging C34 through R29 with RC time constant τ = R29 × C34. When the voltage across C34 reaches the logic low threshold of HI, HO = 0, returning to its first state. Therefore, the transient load current interval is set by:

- $Vc(t) = Vf + (Vi-Vf)\times e^{-t/RC}$
- Discharging C34: Vf = 0V; Vi = V_{IH}; Vc(t) = V_{IL}
- $VIL = 0V + (V_{IH})\times e^{-t/(R29\times C34)}$
- The $\ln [V_{IL}/V_{IH}] = -t/(R29\times C34)$
- Load Active Time: $t = -(R29\times C34) \times \ln [V_{IL}/V_{IH}]$ to discharge C34/HI from V_{IH} to V_{IL} of HIP2100.

- Charging C34: Vf = VDD; Vi = V_{IL}; Vc(t) = V_{IH}
- $V_{IH} = V_{DD} + (V_{IL}-V_{DD})\times e^{-t/((R28+R29)\times C34)}$
- The $\ln [(V_{IH}-V_{DD})/(V_{IL}-V_{DD})] = -t / ((R28+R29)\times C34)$
- Load Inactive Time: $t = -(R28+R29)\times C34 \times \ln [(V_{IH}-V_{DD})/(V_{IL}-V_{DD})]$ to charge C34/HI from V_{IL} to V_{IH} of HIP2100.

- The HIP2100 typical input thresholds are V_{IH} = 4.86V and V_{IL} = 4.46V. The a-stable operation operates the HIP2100 between the hysteresis window of the HI input pin.
- The load active time with R29 = 1kΩ and C34 = 10µF is approximately 860µs.
- The load inactive time with R28 = 48.7kΩ, R29 = 1kΩ and C34 = 10µF is approximately 30ms.

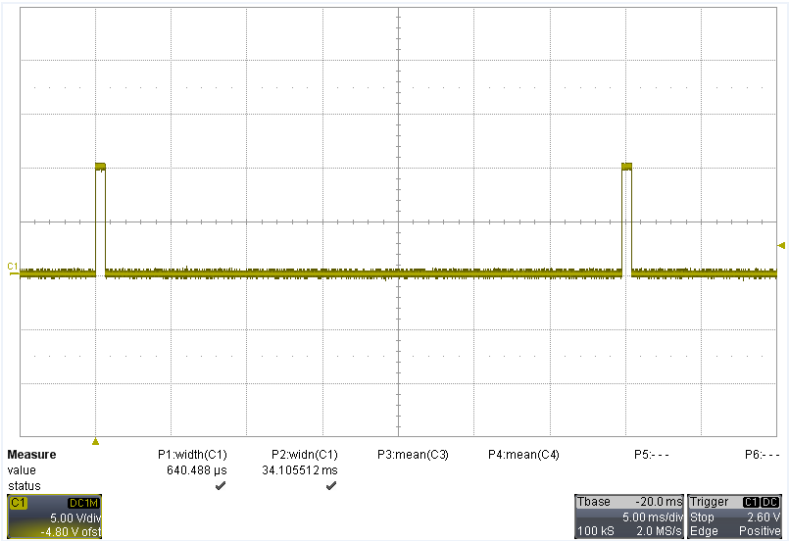

Figure 3. A-Stable Transient Load Current Timing Control

1.8 Changing Output Voltage on LDO

The LDO output voltage is set by the equation: L_OUT = L_EA+ × (R21/R22 + 1)

There are three variables to control LDO output voltage. The L_EA+ voltage can be connected to the ISL70005SEH VREF = 0.6V by setting the jumper in the 1-2 position of JP6 or to one-half of the buck output voltage by setting the jumper in the 2-3 position. Additionally, you can put in an external reference by not having a jumper on JP6 and applying a voltage to pin 2 of JP6 and GND. The ISL70005SEHEV2Z is preset with a feedback gain of 2 with R21 = R22 = 1kΩ. You can populate jumper JP4 to short out R21 for unity gain feedback to set L_OUT = L_EA+. You can also change the R21 and R22 resistor values for the desired feedback gain.

1.9 Using the LDO Regulator Transient Load Generator

To use the transient load generator for the LDO, first set up the board properly. JP9 must have a jumper installed. For sourcing transient load, J2 must have a jumper. For sinking transient load, J1 must have a jumper. An external voltage higher than L_OUT must be applied to load power (BA8) for sinking current.

An on-board load transient generator is made available to the LDO regulator output. This circuit is shown in Figure 6 (bottom left corner of the schematic) and is comprised of one open-drain NMOS and one open-drain PMOS connected in a push-pull configuration to allow for sourcing and sinking current on the LDO. The source and sink transient load currents are controlled by a single input on BNC1.

The sourcing circuit includes the lower NMOS FET Q1 and the resistor network R6//R35//R37. A 0V (off) to 5V (on) signal from a signal generator is adequate to control the sourcing MOSFET Q1. When NMOS Q1 is on, the LDO sourcing load current is I_{SOURCE} = L_OUT / (R6//R35//R37). The ISL70005SEH is populated with R6 = 1Ω with R35 and R37 as DNP.

The sinking circuit includes the upper PMOS FET Q1 and the resistor network R5//R27//R36. A 5V (off) to -5V (on) signal from a signal generator is adequate to control the sinking MOSFET Q1. When PMOS Q1 is on, the LDO sinking load current is ISINK = (LOAD_POWER – L_OUT) / (R5//R27//R36) where LOAD_POWER is the external voltage applied to BA8. The ISL70005SEH is populated with R5 = 1Ω with R27 and R36 as DNP.

Note: R5 and R6 are 1W 2512 sized SMD resistors. When sourcing or sinking 1A, the power dissipation is at its maximum rating.

Note: When using the sinking load current circuit, if an external voltage less than L_OUT-0.7V is applied to LOAD_POWER on terminal BA8, the LDO L_OUT can potentially source current through R5 and body-drain diode of the Q1 PMOS even with zero gate-source voltage. Ensure that external voltage applied to BA8 is higher than L_OUT to avoid back biasing the PMOS.

2. PCB Layout Guidelines

2.1 ISL70005SEHEV2Z Evaluation Board

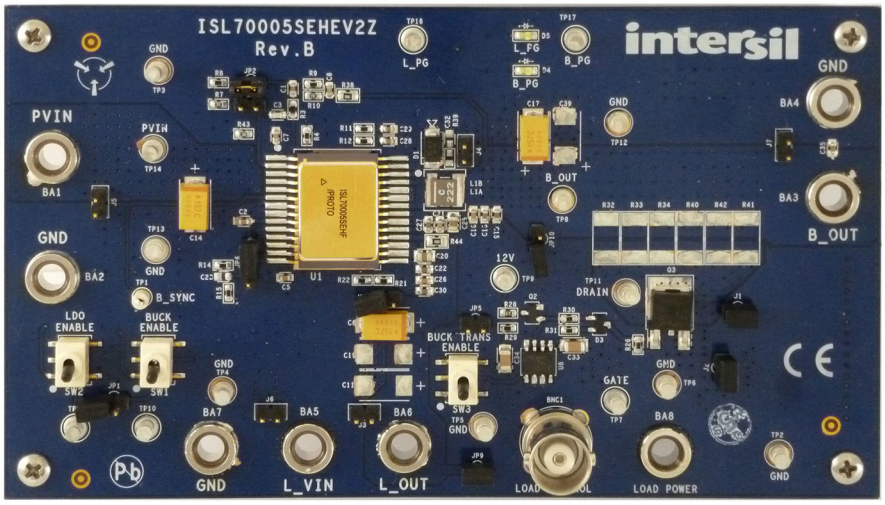

Figure 4. ISL70005SEHEV2Z Evaluation Board (Top)

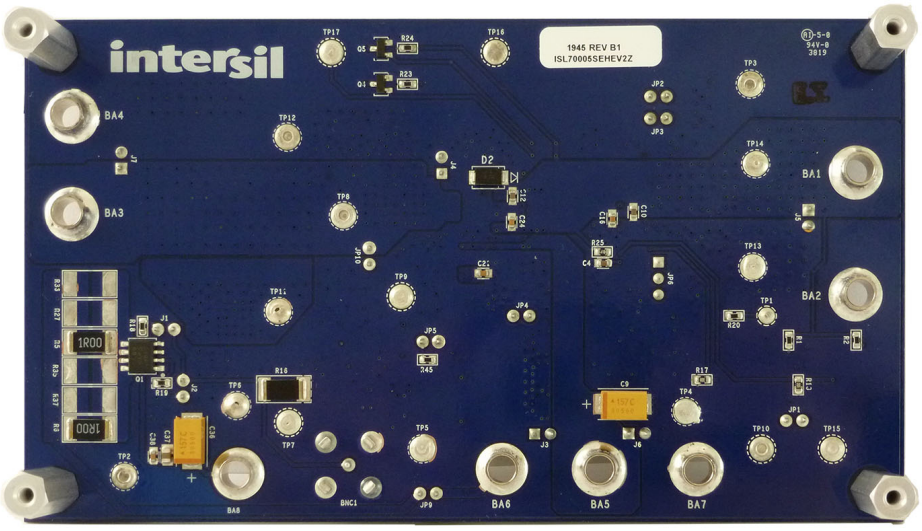

Figure 5. ISL70005SEHEV2Z Evaluation Board (Bottom)

2.2 ISL70005SEHEV2Z Schematic

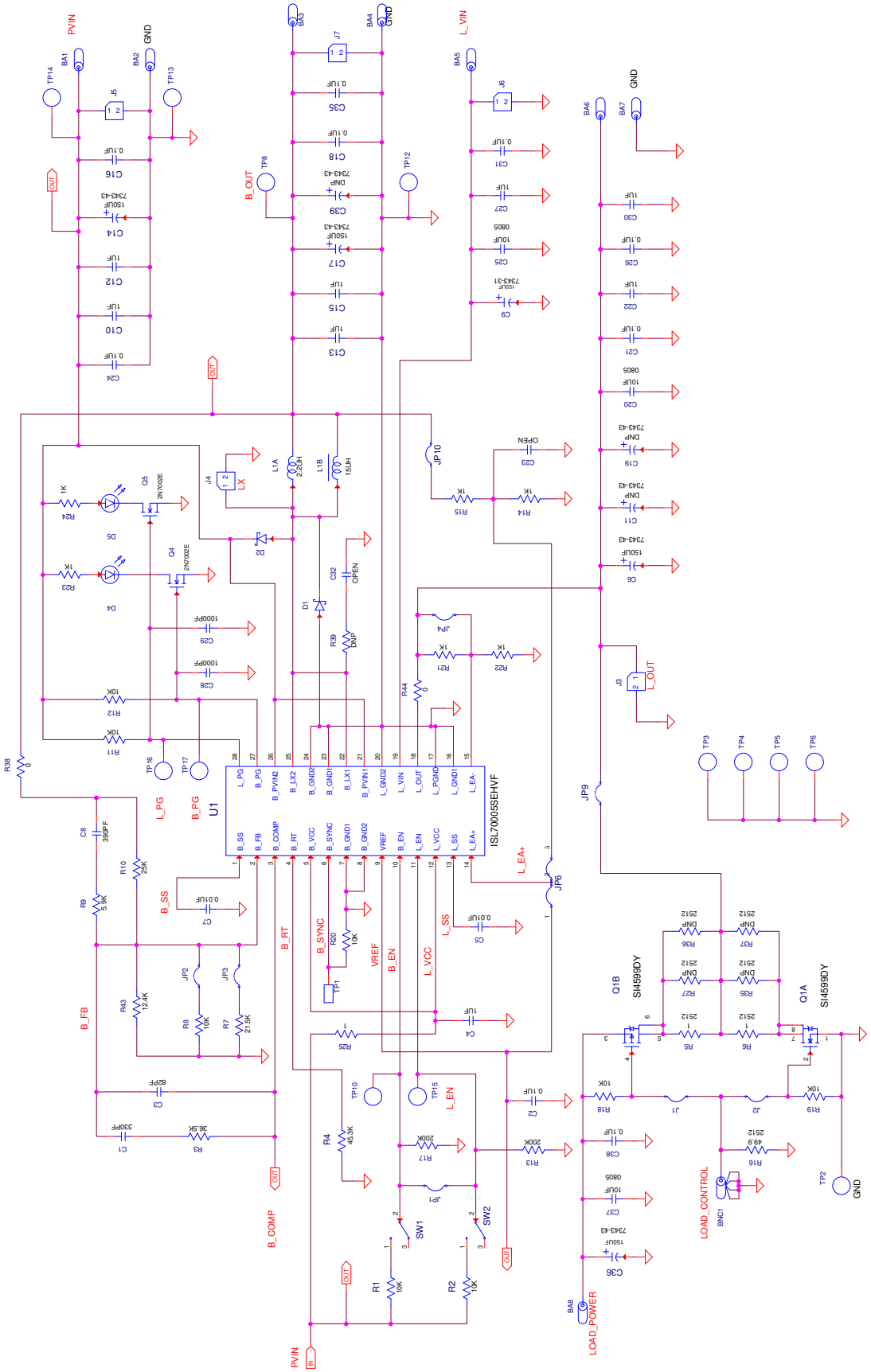

Figure 6. Schematic - Page 1

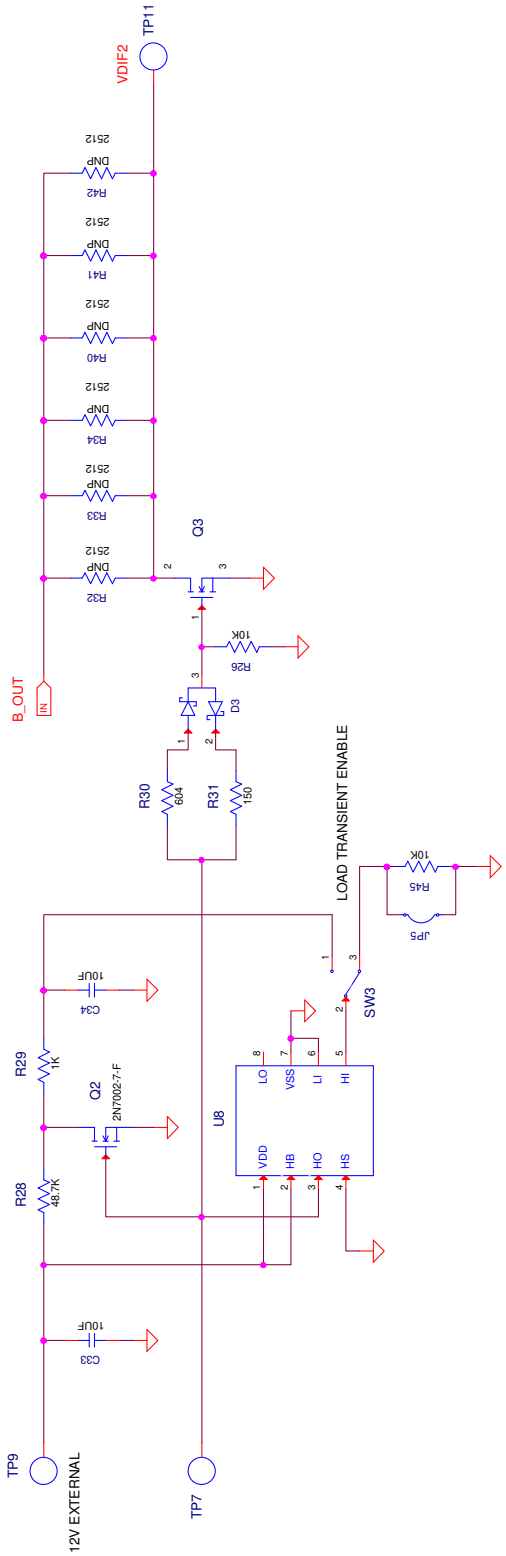

Figure 7. Schematic - Page 2 - Load Transient Generator

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL70005SEHEV2Z, REVB, ROHS	Imagineering Inc	ISL70005SEHEV2ZREVBPCB
8	C4, C10, C12, C13, C15, C22, C27, C30	CAP, SMD, 0603, 1.0µF, 16V, 10%, X7R, ROHS	TDK	C1608X7R1C105K
3	C20, C25, C37	CAP, SMD, 0805, 10µF, 16V, 20%, X7R, ROHS	Taiyo Yuden	EMK212BB7106MG-T
2	C28, C29	CAP, SMD, 0603, 1000pF, 16V, 10%, X7R, ROHS	Venkel	C0603X7R160102KNE
2	C5, C7	CAP, SMD, 0603, 0.01µF, 16V, 10%, X7R, ROHS	Venkel	C0603X7R160-103KNE
9	C2, C16, C18, C21, C24, C26, C31, C35, C38	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS	Murata	GCM188R71C104KA37D
1	C1	CAP, SMD, 0603, 330pF, 50V, 10%, X7R, ROHS	Yageo	CC0603KRX7R9BB331
1	C8	CAP, SMD, 0603, 390pF, 50V, 10%, X7R, ROHS	Venkel	C0603X7R500-391KNE
1	C3	CAP, SMD, 0603, 82pF, 50V, 10%, C0G, ROHS	Venkel	C0603COG500-820KNE
0	C23, C32	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	-	-
2	C33, C34	CAP, SMD, 1206, 10µF, 16V, 10%, X5R, ROHS	Venkel	C1206X5R160-106KNE (Pb-Free)
5	C6, C9, C14, C17, C36	CAP-TANT, LOWESR, SMD, 7.3x4.3mm, 150µF, 16V, 10%, 30mΩ, ROHS	AVX	TPME157K016R0030
1	L1A	COIL-PWR INDUCTOR, SMD, 4mm, 2.2µH, 20%, 3.5A, 21.3mΩ, ROHS	Coilcraft	XFL4020-222MEB
16	TP2-TP17	CONN-DBL TURRET, TH, 0.218x0.078 PCB MNT, TIN/BRASS, ROHS	Keystone	1502-1
1	BNC1	CONN-BNC, RECEPTACLE, TH, 4 POST, 50Ω, SILVERCONTACT, ROHS	Amphenol	31-5329-51RFX
1	TP1	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	Keystone	5002
8	BA1-BA8	CONN-JACK, MINI BANANA, 0.175 PLUG, NICKEL/BRASS, ROHS	Keystone	575-4
1	JP6	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
14	J1, J2, J3, J4, J5, J6, J7, JP1, JP2, JP3, JP4, JP5, JP9, JP10	CONN-HEADER, 1x2, RETENTIVE, 2.54mm, 0.230x0.120, ROHS	BERG/FCI	69190-202HLF

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
8	J1, J2, JP1, JP2, JP4, JP9, JP10, JP6-Pins 2-3	CONN-JUMPER, SHORTING, 2PIN, BLACK, GOLD, ROHS	Sullins	SPC02SYAN
2	D1, D2	DIODE-SCHOTTKY RECITIFIER, SMD, 2P, SMA, 20V, 1A, ROHS, DNP-PLACE HOLDER	-	-
1	D3	DIODE-SCHOTTKY, DUALDIODE, SMD, 3P, SOT23, 30V, 200mA, ROHS	Fairchild	BAT54S
2	D4, D5	LED-GaAs RED, SMD, 2X1.25mm, 100mW, 40mA, 10mcd, ROHS	Liteon/Vishay	LTST-C170CKT
1	U8	IC-HI FREQ BRIDGE DRIVER, 8P, SOIC, 100V, ROHS	Renesas Electronics America	HIP2100IBZ
1	U1	IC-RAD HARD LDO REGULATOR, SMD, 28P, CFP, ROHS	Renesas Electronics America	ISL70005SEHF/PROTO
1	Q2	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	Diodes, Inc.	2N7002-7-F
2	Q4, Q5	TRANSIST-MOS, N-CHANNEL, SMD, SOT23, 60V, 0.24A, ROHS	Vishay/Siliconix	2N7002E
1	Q1	TRANSISTOR-N/P CHANNEL, 8P, SOIC, 40V, 6.8/5.8A, ROHS	Vishay/Siliconix	SI4599DY-T1-GE3
1	Q3	TRANSISTOR-MOS, N-CHANNEL, SMD, TO-252, 30V, 90A, ROHS	Vishay	SUD50N03-06AP-E3
1	R16	RES-AEC-Q200, SMD, 2512, 49.9Ω, 1W, 1%, TF, ROHS	Vishay/Dale	CRCW251249R9FKEG
0	R39	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER	-	-
1	R25	RES, SMD, 0603, 1Ω, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3RQF1R0V
7	R14, R15, R21, R22, R23, R24, R29	RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1001V
10	R1, R2, R8, R11, R12, R18, R19, R20, R26, R45	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
1	R43	RES, SMD, 0603, 12.4k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1242FT (Pb-Free)
1	R31	RES, SMD, 0603, 150Ω, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1500FT
2	R13, R17	RES, SMD, 0603, 200k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2003FT

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	R7	RES, SMD, 0603, 21.5k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2152FT
1	R10	RES, SMD, 0603, 24.9k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF2492V
1	R3	RES, SMD, 0603, 36.5k, 1/10W, 1%, TF, ROHS	Vishay	CRCW060336K5FKEA
1	R4	RES, SMD, 0603, 45.3k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-0745K3L
1	R28	RES, SMD, 0603, 48.7k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF4872V
1	R9	RES, SMD, 0603, 5.90k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF5901V
1	R30	RES, SMD, 0603, 604Ω, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF6040V
2	R38, R44	RES, SMD, 0805, 0Ω, 1/8W, TF, ROHS	Yageo	RC0805JR-070RL
2	R5, R6	RES, SMD, 2512, 1Ω, 1W, 1%, TF, ROHS	Vishay	CRCW2512-1R00F
0	R27, R32-R37, R40, R41, R42	RES, SMD, 2512, DNP, DNP, DNP, TF, ROHS	-	-
3	SW1-SW3	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	ITT Industries/C&K Division	GT11MSCBE
4	Four corners	SCREW, 4-40x1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Building Fasteners	PMSSS 440 0025 PH
4	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	Keystone	2204
0	C11, C19, C39 (TPME157K016R0030)	DO NOT POPULATE OR PURCHASE	-	-
0	L1B (XAL6060-153MEC)	DO NOT POPULATE OR PURCHASE	-	-

2.4 Board Layout

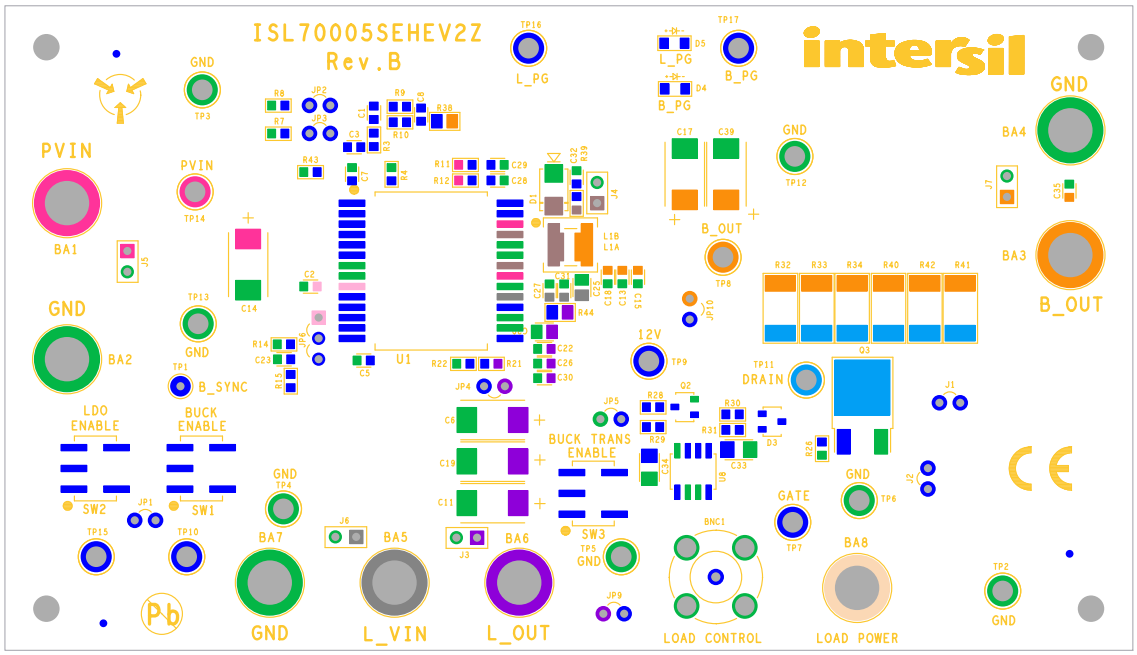

Figure 8. Silkscreen Top Layer

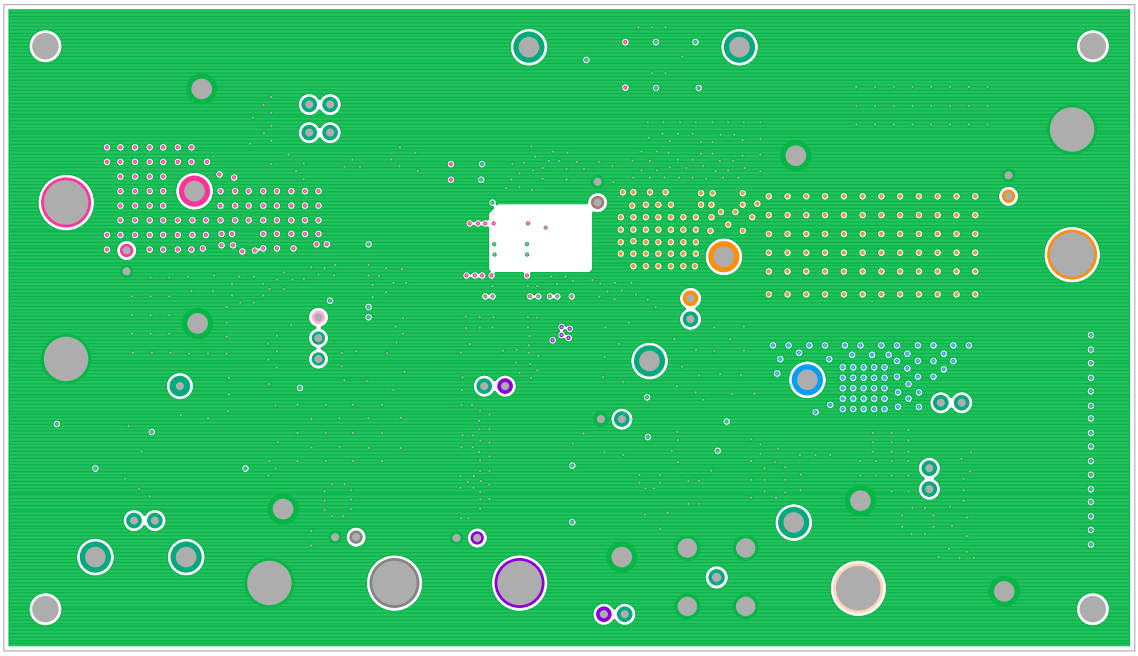

Figure 9. Top Layer

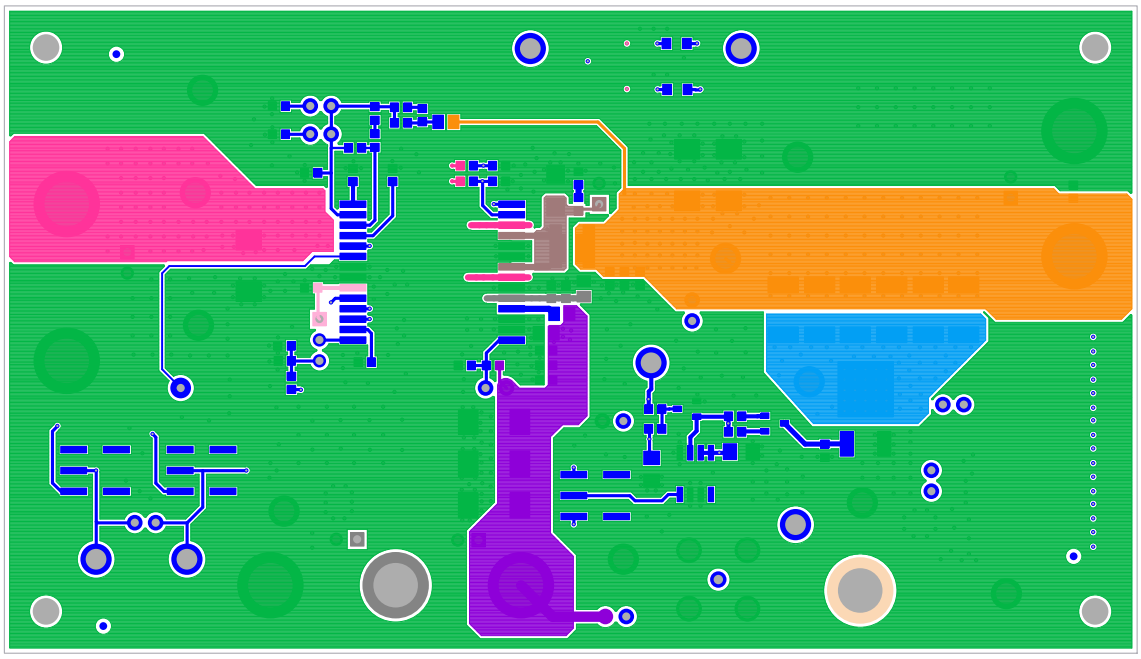

Figure 10. Layer 2

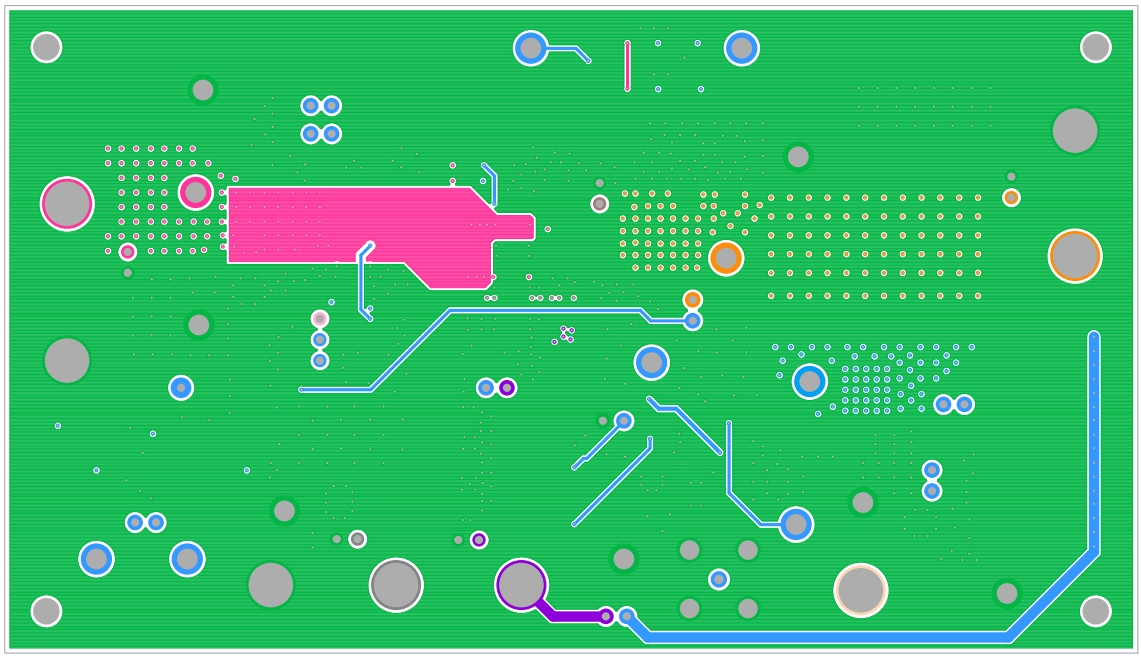

Figure 11. Layer 3

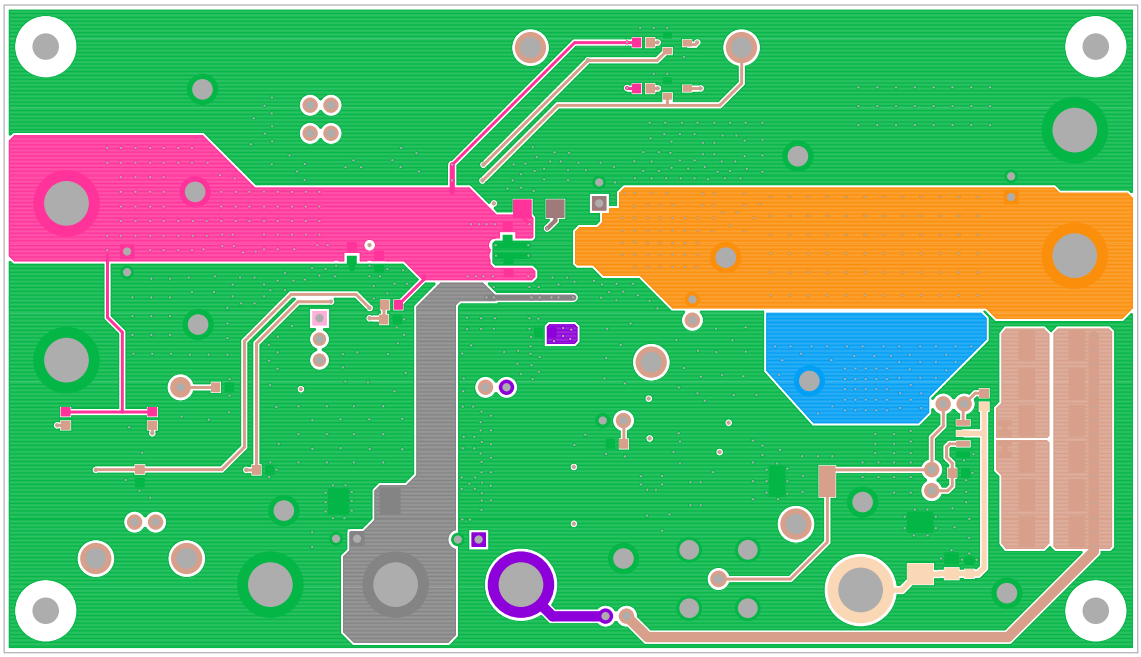

Figure 12. Layer 4

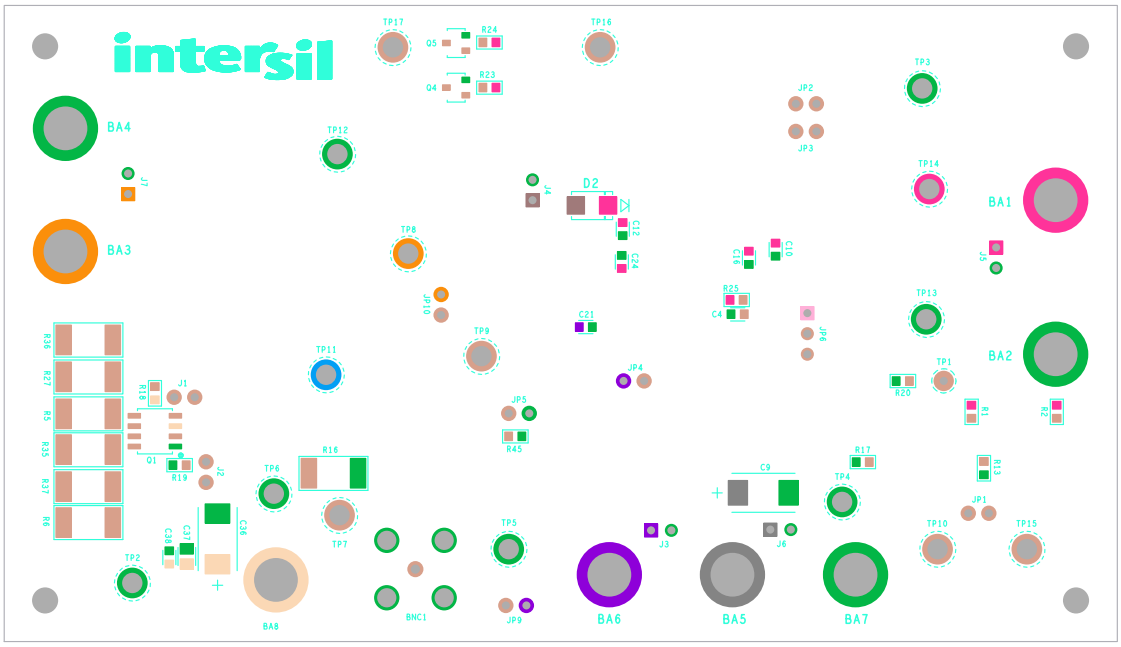

Figure 13. Silkscreen Bottom Layer

3. Typical Performance Curves

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C.

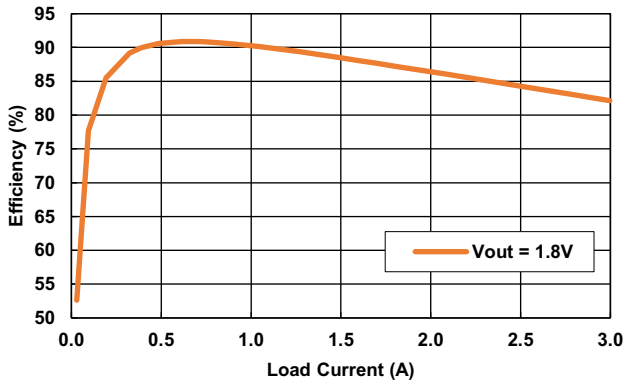

Figure 14. Efficiency vs I_{OUT}; B_VIN = 3V; 1MHz

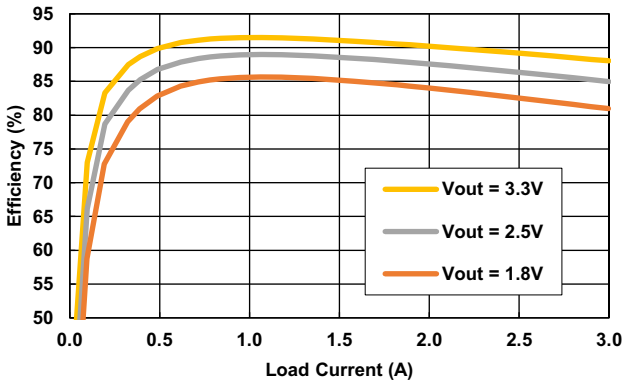

Figure 15. Efficiency vs I_{OUT}; B_VIN = 5V; 1MHz

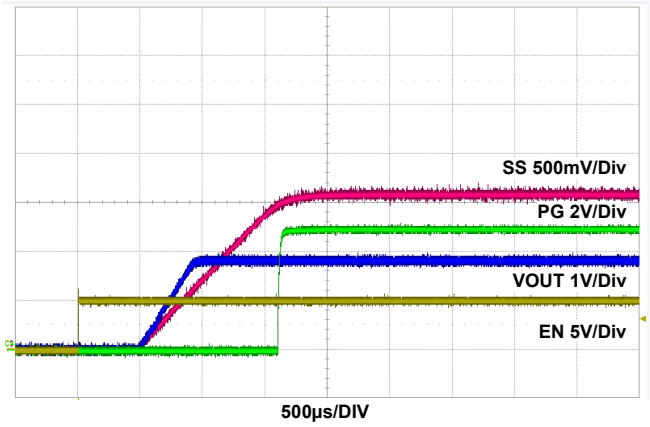

Figure 16. Buck Soft-Start; Load = 0.68Ω; LDO Disabled

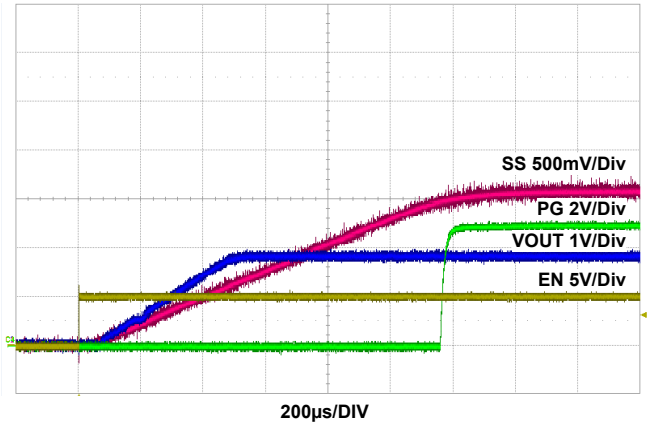

Figure 17. Buck Soft-Start; Load = 0.68Ω; LDO Enabled

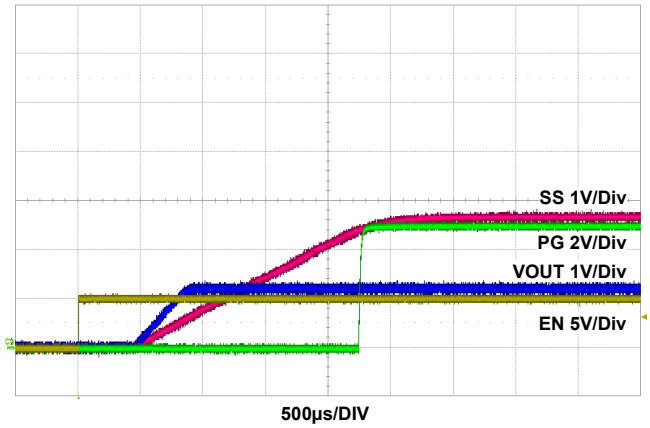

Figure 18. LDO Soft-Start; Load = 1.5Ω to GND; Buck Disabled

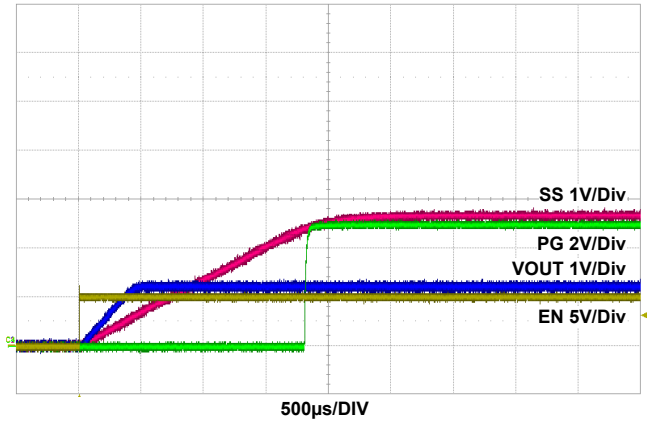

Figure 19. LDO Soft-Start; Load = 1.5Ω to GND; Buck Enabled

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. (Cont.)

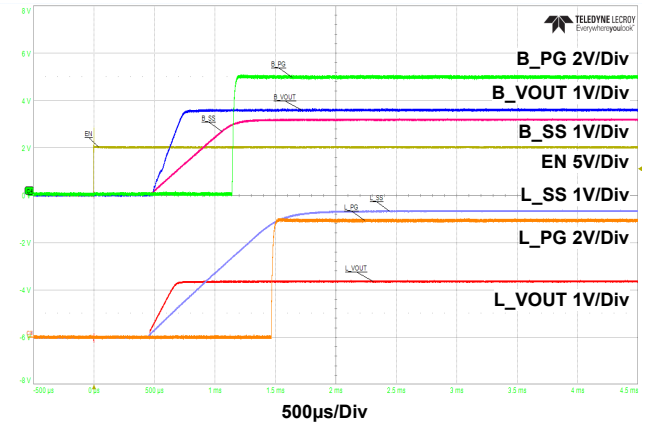

Figure 20. Buck and LDO Soft-Start; B_EN = L_EN; 0.68Ω Load on Buck; 1.5Ω Load on LDO; FPGA Configuration

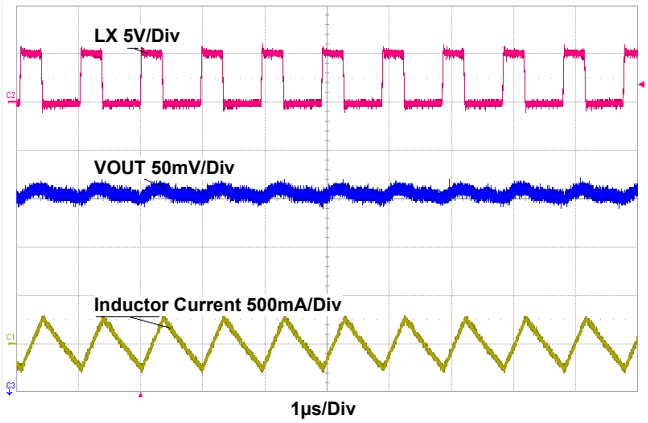

Figure 21. Buck Steady State Operation; Load = 0A

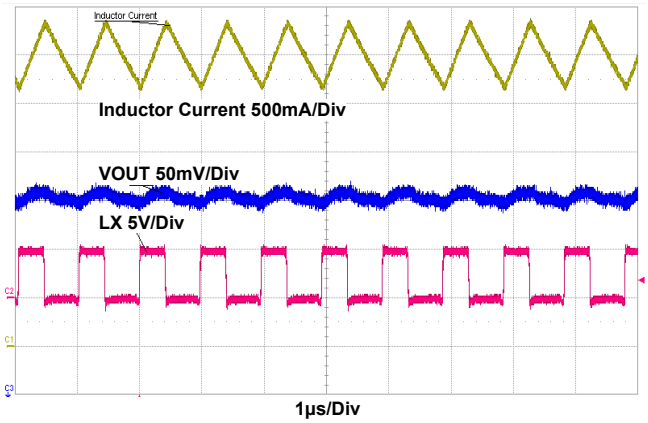

Figure 22. Buck Steady State Operation; Load = 3A

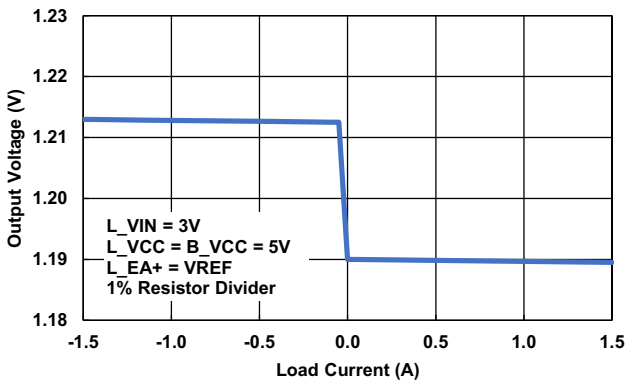

Figure 23. LDO Load Regulation Av = 2

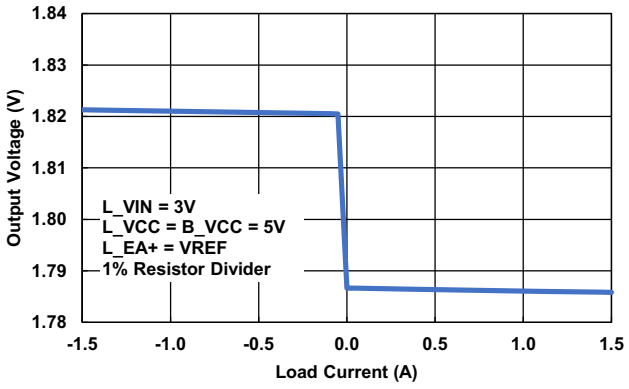

Figure 24. LDO Load Regulation Av = 3

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. (Cont.)

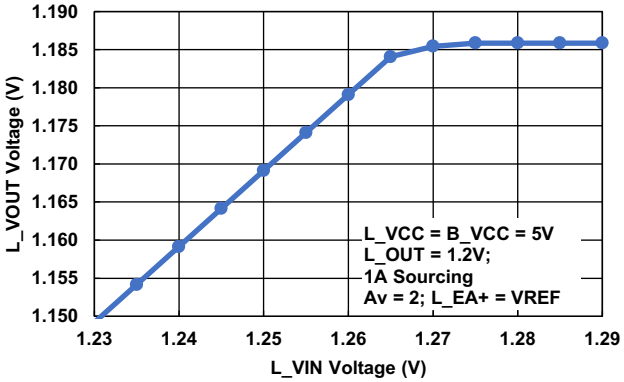

Figure 25. LDO Dropout Voltage; Av = 2

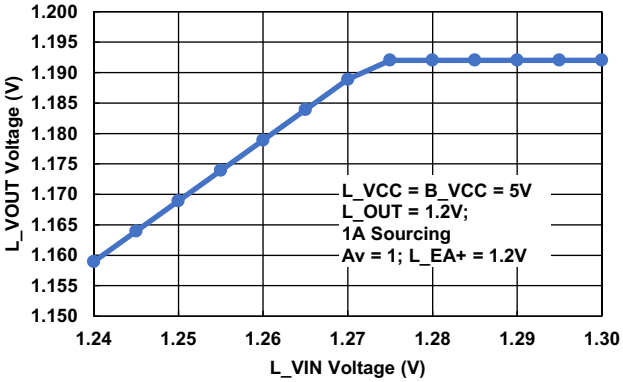

Figure 26. LDO Dropout Voltage; Av = 1

4. Ordering Information

Part Number	Description
ISL70005SEHEV2Z	ISL70005SEH evaluation board

5. Revision History

Rev.	Date	Description
1.03	Aug 22, 2023	Applied new template. Updated Using the Buck Regulator Transient Load Generator section.
1.02	Nov 16, 2022	Added reference to ISL73005SEH on page 1.
1.01	Jan 6, 2020	Changed diode D1 and D2 in BOM to DNP.
1.00	Dec 11, 2019	Initial release

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