ISL73148SEHEV1Z

The ISL73148SEHEV1Z board evaluates the operation of the Renesas ISL73148SEH radiation hardened 14-bit 900ksps/480kps SAR ADC. The evaluation boards are intended to be used with the RHADC-FMCEV1Z data capture board.

The ISL73148SEH device on the evaluation board supports operation of the ISL73148SEH with AVCC set to 5V. DVCC can be set to 2.5V or 3.3V (default setting is 2.5V). The reference voltage to the ADC is set to 2.5V. The digital I/O voltage of the CPLD can be set to 2.5V or 3.3V operation as well, but matched to the DVCC setting of the ISL73148SEH. The supply voltage for the CPLD by default is also connected to the digital I/O voltage. The supply voltages to the analog input amplifier circuit is set to +7.5/-4.5V. These voltages are all derived from the ±10V supply inputs to the board.

Specifications

- ±10V power supply inputs
- VITA 57.1 FMC connector for interoperability
- Supports -55°C to +125°C operation of the ISL73148SEH
- Supporting components operate over temperature range of -40°C to +85°C
- Jumper selectable for +2.5V or +3.3V DVCC and Digital I/O operation

Features

These evaluation boards evaluate the common performance metrics of the ISL73148SEH listed in the datasheet for the device. These parameters include:

- Signal-to-Noise Ratio (SNR)
- Signal-to-Noise-and-Distortion Ratio (SINAD)
- Effective Number of Bits (ENOB)
- Total Harmonic Distortion (THD)
- Spurious Free Dynamic Range (SFDR)
- Input voltage range (Analog input)
- REF input voltage range (VREF input)

Required Equipment

- ISL73148SEHEV1Z ADC evaluation board
- RHADC-FMCEV1Z data capture board
- Low phase noise analog signal source (such as the Rohde-Schwarz SMA100B)
- Low phase noise clock source (such as the clock synthesis on the Rohde-Schwarz SMA100B)
- ±10V DC power supply
- 5V DC wall supply
- USB 2.0 Cable and port on PC
- PC running Windows 10 or greater
- Renesas iRADAnalyzer software

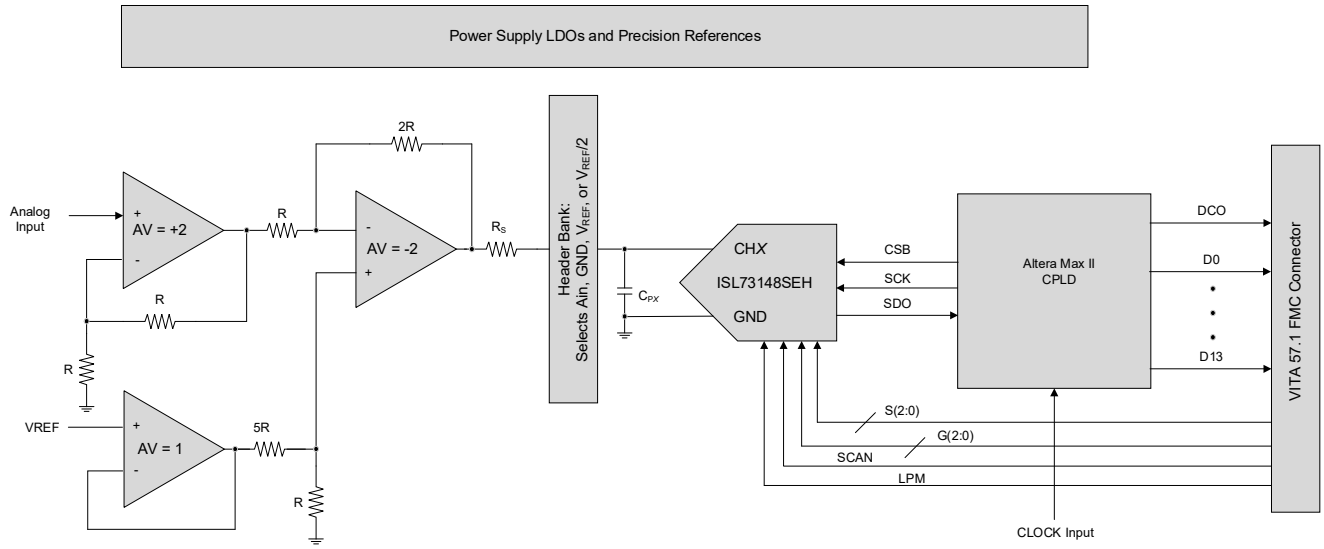

Figure 1. Block Diagram

Contents

1. Functional Description

The digitized data from the ADC is passed to the RHADC-FMCEV1Z using the VITA 57.1 FMC mezzanine connector. The iRADAnalyzer application software controls the capture of data and provides FFT performance data of the ADC. Figure 3 shows the GUI interface of the application software.

Figure 2 shows the location and position of the jumpers on the ISL73148SEHEV1Z board. The default positions of the jumpers select the use of the on-board LDOs to drive the various power supply domains.

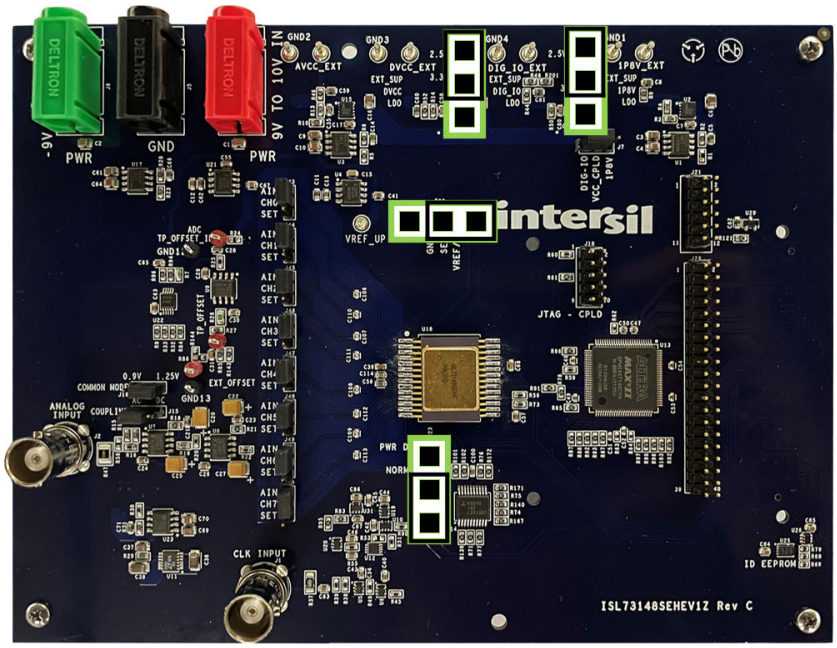

Figure 2. ISL73148SEHEV1Z Evaluation Board Jumper Location

Figure 1 provides a view of the ISL73148SEH evaluation board along and the RHADC-FMCEV1Z data capture board with the required external connections. Renesas power products ISL80410 and ISL80505 provide the voltages for the various supply domains while the ISL21090 provides reference voltages for the ADC on the ISL73148SEH evaluation board. A Renesas digital potentiometer, the ISL23315, divides down the voltage from one of the ISL21090 references to allow for proper common mode adjustment when operating the ISL73148SEH in unipolar mode. An Altera MAXII CPLD captures the serial data from the ADC and parallelizes the data to present it at the 40-pin parallel connector and the VITA 57.1 FMC mezzanine connector.

Power for the system is provided by ±10V external power supplies on the three banana jack terminals J4, J5, and J6. Connect the red banana jack (J4) to +10V, the black banana jack (J5) to ground, and the green banana jack (J6) to -10V.

Apply the analog input for the ADC to the BNC connector (J2). This input is terminated to ground using a 50Ω resistor. This input should be a clean, low phase noise input source. A typical input frequency of 20.3kHz can be used with an amplitude of approximately 600mV$_{P-P}$, setting the input level to the ADC at -1dBFS. Renesas recommends using a bandpass filter with sufficient stop-band attenuation to limit the harmonic distortion from the analog input source. A Q70 series bandpass filter of 30% bandwidth of less from TTE or equivalent is recommended.

Apply the input clock to the BNC connector (J1). This is the master clock reference for the ISL73148SEH evaluation board. The sample rate of the ISL73148SEH is dependent on the input clock frequency and the mode of operation. For the maximum 900ksps sample rate operation of the ISL73148SEH ADC, an input clock rate of 100MHz is required, and the ADC must be operated with the PGA bypassed. While the ADC supports sample rates near DC (extremely sparse sampling over time), the evaluation board hardware minimum capture size is 32k samples; therefore, for low sample rates, consider the acquisition time to collect this amount of samples. Renesas recommends using a sample rate of at least 10ksps or higher because of the length of time required to acquire

32k samples. In addition, keep the input frequency appropriate to avoid severely undersampling the ADC (for example, set an input frequency <10x the sample rate).

The Altera Max II CPLD on the ISL73148SEH evaluation board takes the serial ADC data and parallelizes the data. The data output from the CPLD to the FMC connector is delivered to the Virtex 5 FPGA on the RHADC-FMCEV1Z data capture board. It is collected on the data capture board and passed using a USB to the PC to the iRADAnalyzer software application for processing.

The evaluation board can operate in standalone mode where the digitized data from the ADC can be accessed from the 40-pin parallel port connector. In this case, you are required to process the data from the ADC.

1.1 Operating Range

The ISL73148SEH device on the evaluation board supports operation from -55°C to +125°C. However, many of the components used on the evaluation board support a commercial temperature range of -40°C to +85°C. This evaluation board as a whole is intended to operate under ambient temperature conditions at 25°C for evaluation purposes. The ISL73148SEH device is heated or cooled across its operating temperature from -55°C to +125°C if an appropriate device (such as a Thermostream or similar) sets the temperature of the device itself.

1.2 Connecting the Evaluation and Data Capture Boards

1. Connect the supplied CUI 5V switching power supply to the RHADC-FMCEV1Z then connect a USB cable between the PC and the RHADC-FMCEV1Z. The board should be listed in the device manager on the PC as Renesas RHADC-FMCEV1Z under Universal Serial Bus Controllers as shown in Figure 3.

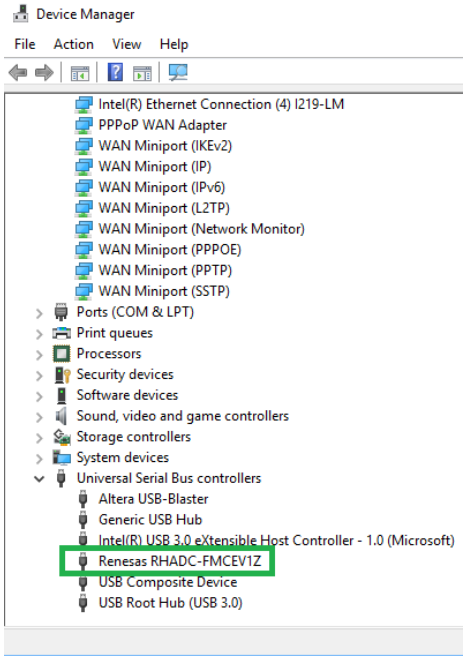

Figure 3. USB Device Driver in Device Manager

2. Connect the ISL73148SEH ADC evaluation board to the RHADC-FMCEV1Z data capture board. There are four standoff guides on the RHADC-FMCEV1Z that fit into alignment holes on the ISL73148SEH evaluation board that help to align the FMC connectors of the two boards. Carefully press the ISL73148SEH evaluation board into place on the RHADCFMCEV1Z board.
3. Make sure the jumpers on the ADC evaluation board are in place as shown in Figure 2.
4. Supply ±10V and ground to the banana jacks on the ADC evaluation board.
5. Provide a clean, low phase noise 100MHz input clock to the CLK INPUT connector (J1) on the ADC evaluation board. This provides the reference clock to the board, which sets the Convert Start Bar (CSB) signal to the ADC.

6. Provide a clean, low phase noise 20.3kHz analog input tone to the ANALOG INPUT connector (J2) on the ADC evaluation board through a bandpass filter such as the Q70 series 30% bandwidth TTE bandpass filter.
7. Make all connections as shown in Figure 4.

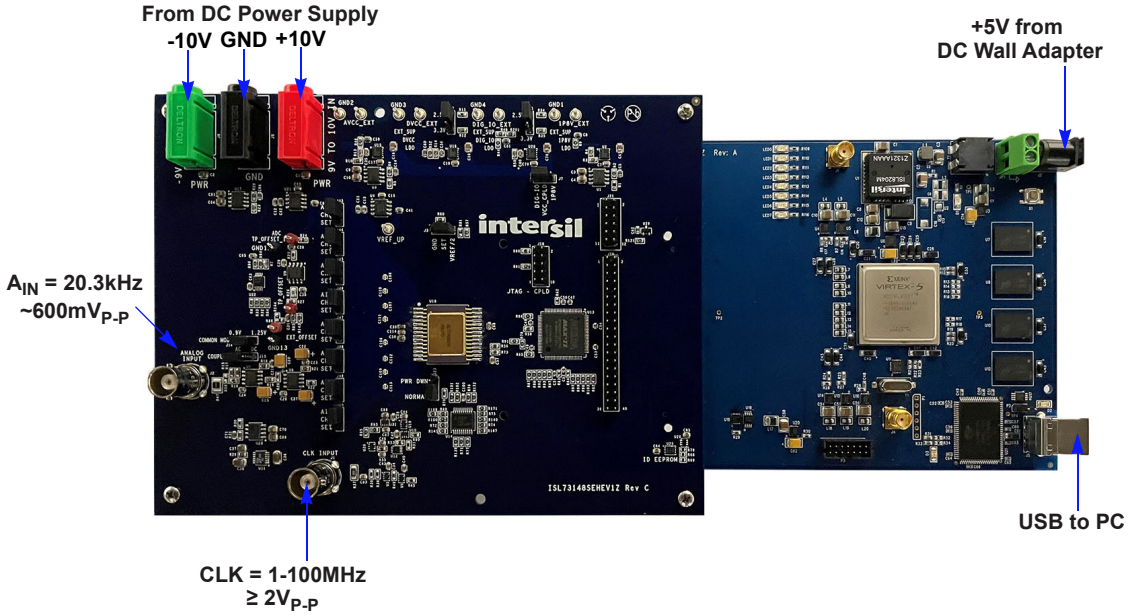

Figure 4. ISL73148SEHEV1Z/RHADC-FMCEV1Z Connection Diagram

1.2.1 iRADAnalyzer RHADC-FMCEV1Z Board Initialization

When the ISL73148SEHEV1Z board and the RHADC-FMCEV1Z board have been connected and setup properly, open iRADAnalyzer on the PC by clicking **Start→Renesas iRADAnalyzer→iRADAnalyzer**. When the board is detected and configured by the iRADAnalyzer software application, it should indicate **Board Initialized** in the status window of the GUI as shown in Figure 5.

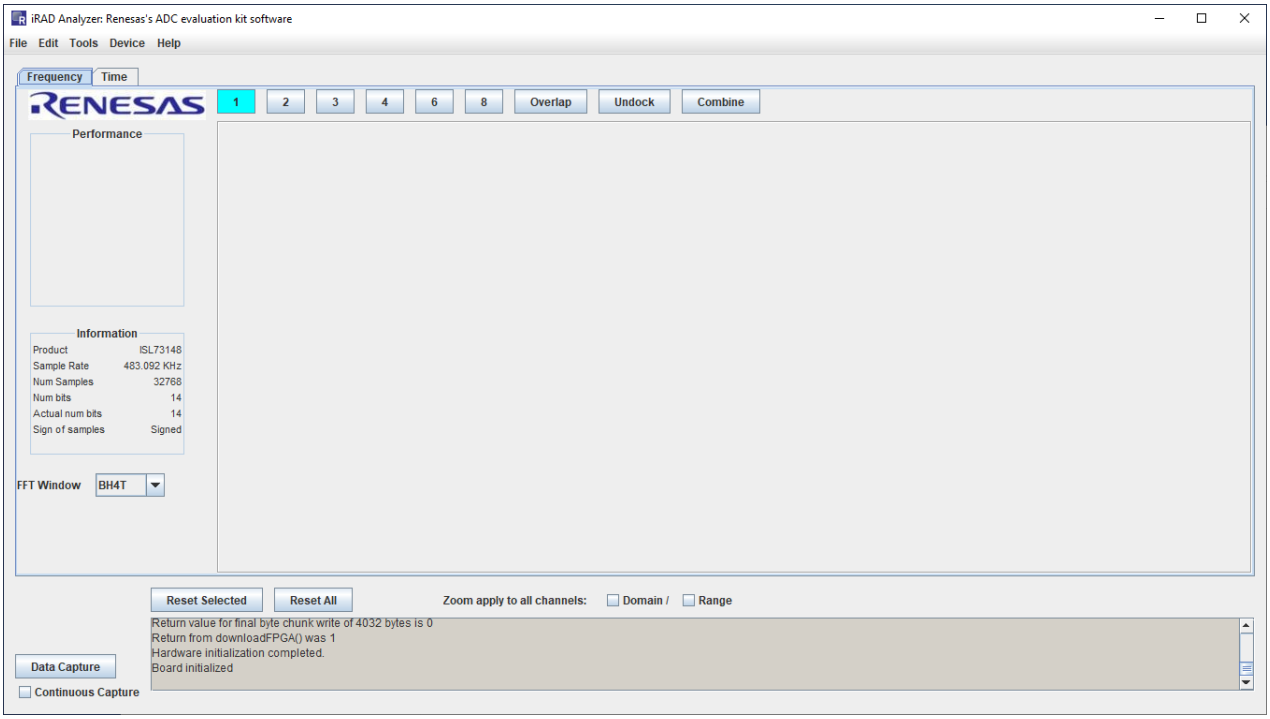

Figure 5. iRADAnalyzer Board Initialization

1.2.2 iRADAnalyzer Data Capture Settings

Verify the Data Capture settings under the **Edit->Data Capture** menu match the hardware configuration. The default input clock is set to 100MHz. If another frequency is required, enter it here and the iRADAnalyzer automatically calculates the sample rate based on the ISL73148SEH device configuration. In this example, the ISL73148SEH has bee configured with the PGA enabled to a gain of 2 in normal mode with the data format set to bipolar and no information bits are selected.

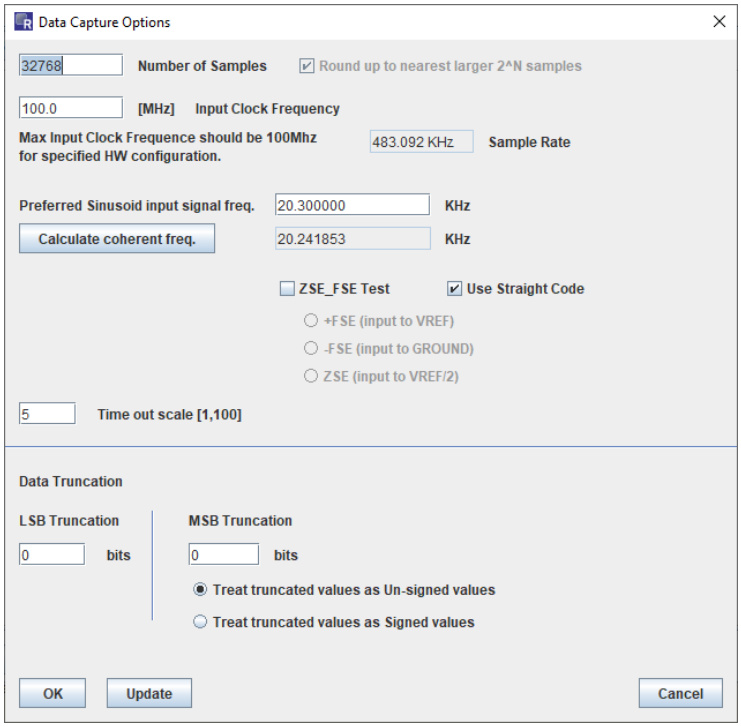

Figure 6. iRADAnalyzer Data Capture Settings

1.2.3 iRADAnalyzer Device Settings

The ISL73148SEH may be configured into different modes of operation. This is configured from the Settings selections under the **Device** menu in iRADAnalyzer. The ISL73148SEH has an integrated Programmable Gain Amplifier (PGA) and an 8-channel multiplexer. The PGA may be bypassed if required and, when enabled, has available gain settings of 1, 2, 3, 4, 6, 8, 12, and 16. The data format defaults to signed data (bipolar mode), but the software can configure the ISL73148SEH for unsigned data (unipolar mode). Up to eight channels can be selected for data capture. Each channel can have a different gain setting if required. However, iRADAnalyzer changes the gain setting using the gain select pins G[2:0] between data captures for each channel because there is one PGA inside the ISL73148SEH. When operating the ISL73148SEH with unsigned data (unipolar mode), the input common mode must be decreased by the same factor as the gain selection. For example, if gain = 2, the input common mode should be 1.25V/2 = 0.625V. Regardless of data format, the analog input common mode is adjusted by iRADAnalyzer using a digital potentiometer on the evaluation board. For bipolar (signed) data format, the common mode is set to VREF/2 = 1.25V and when operating in unipolar (unsigned) data format, the common mode is set based on the selected gain setting (see the *ISL73148SEH Datasheet* for further details on the analog input voltage requirements).

The ISL73148SEH can be operated in normal mode or, to reduce power consumption, can be operated in low power mode. In either of these modes, the ISL73148SEH can provide channel and gain information (Info Bits) along with the sample data on the output SPI port. If operating with the PGA bypassed, the evaluation system provides only the channel information if Info Bits is selected and does not provide the gain information. The resolution and data format are also selected here. The resolution defaults to 14 bits, which is the resolution of the ISL73148SEH.

For more information about the operating modes, see the *ISL73148SEH Datasheet*.

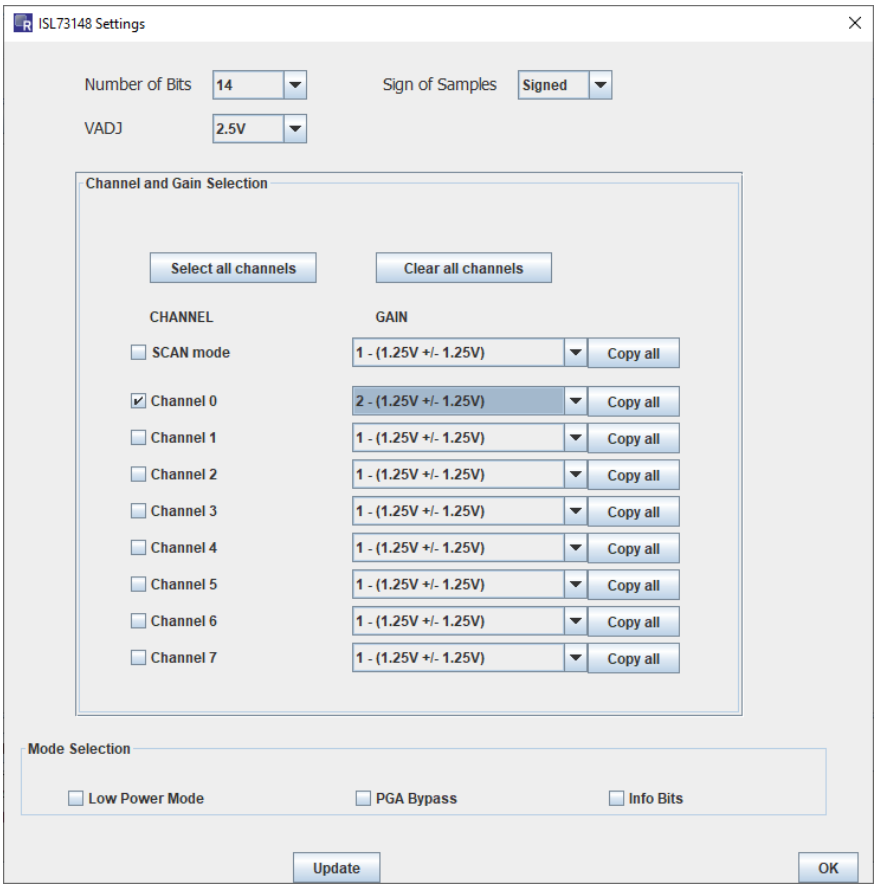

Figure 7. iRADAnalyzer Device Settings (Normal Mode, PGA Gain = 2, Signed/Bipolar)

Table 1 provides the information on the information bits, sample period, and sample rate for all the various modes of the ISL73148SEH. The first three columns correspond to the three check boxes under **Mode Selection** in the **Device Settings** menu shown in Figure 7. The sample period and sample rate shown are based on an input clock frequency of 100MHz. If another input clock frequency is used, the sample period and sample rate change accordingly. To calculate the sample rate with a different input clock frequency, multiple the number in the sample period column by 100 and divide the input clock frequency by that result. For example, when operating in normal mode with PGA bypassed and no info bits if an input clock frequency of 90MHz is used, the resulting sample rate is 90MHz/111 = 818.818ksps. While the ISL73148SEH has no lower limit on the sample frequency, care should be taken to consider the sample collection time when using low sample rates because the minimum capture size is 32k samples.

Table 1. ISL73148SEH Evaluation Board Operating Mode Information

Mode	PGA	Info Bits	Channel Bits	Gain Bits	Sample Period (µs)	Sample Rate (ksps)
Normal	Bypassed	No	No	No	1.11	900.901
Normal	Bypassed	Yes	Yes	No	1.17	854.701
Normal	Enabled	No	No	No	2.07	483.092
Normal	Enabled	Yes	Yes	Yes	2.19	456.621
Low Power	Bypassed	No	No	No	1.46	684.932
Low Power	Bypassed	Yes	Yes	No	1.52	657.895
Low Power	Enabled	No	No	No	2.42	413.223
Low Power	Enabled	Yes	Yes	Yes	2.54	393.701

1.2.4 iRADAnalyzer Data Capture - FFT

To begin the data capture from the ADC evaluation board, click on the **Data Capture** button in the iRADAnalyzer software application. The software captures the data and provides an FFT of the results as shown in Figure 8.

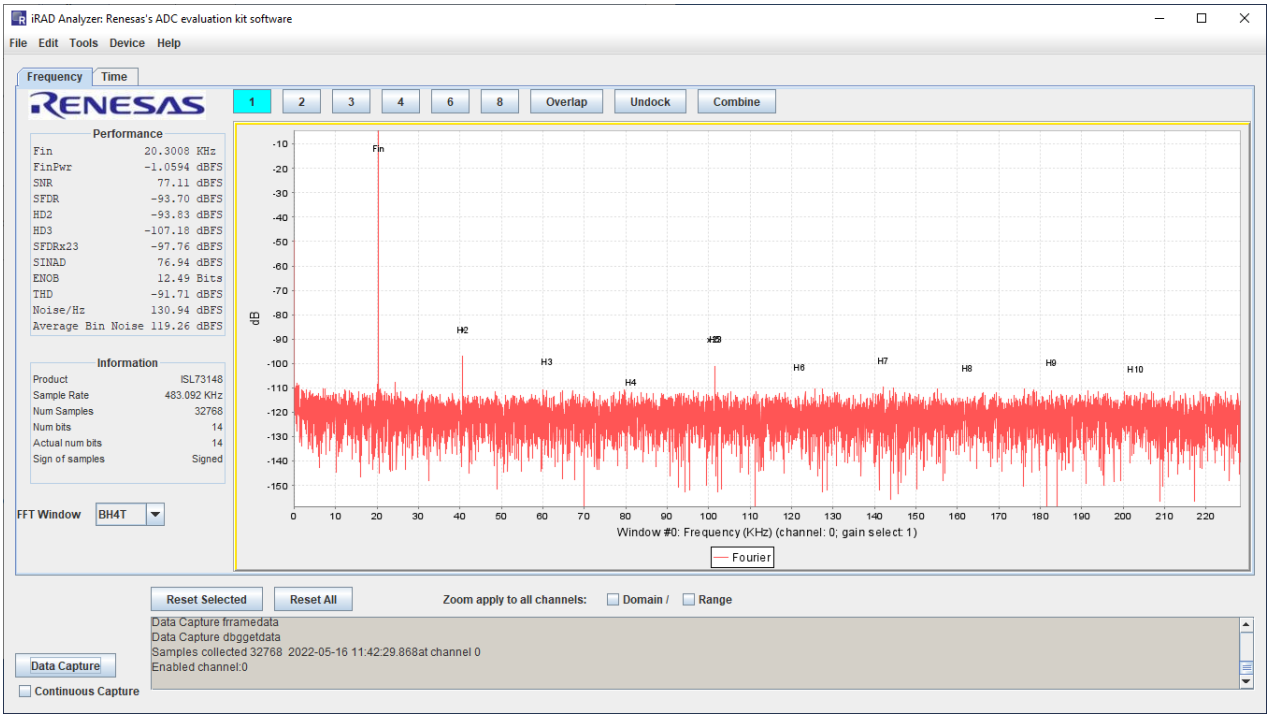

Figure 8. iRADAnalyzer FFT Plot

1.2.5 iRADAnalyzer Data Capture - Channel and Mode Selections

Up to eight channels may be displayed simultaneously on the ISL73148SEH in iRADAnalyzer. The channels can be selected from the **Settings** menu under the **Device** tab. From this menu, the number of bits (default is 14), the data format (signed/unsigned), the VADJ voltage, the required channels, the required gains, the power mode, the PGA function, and the info bits can all be selected. The ISL73148SEH data format can be selected from the drop down box at the top of this window and can be set to unsigned (unipolar) or signed (bipolar). The VADJ voltage can also be selected here and should match the jumper settings on the ISL73148SEHEV1Z evaluation board for the DVCC and DIG_IO supply domains (that is if DVCC and DIG_IO are set to 2.5V the VADJ must match that voltage and also be set to 2.5V). The required channels and required gains can be set using the selections in this window as well. Any number channels can be selected and any gain value may be chosen. The **Select all channels**, **Clear all channels**, and **Copy all** shortcut buttons can be used to make channel selection easier. The check boxes can be selected to determine if Low Power Mode, PGA Bypass, or Info Bits are enabled. To apply the selections click **Update** and then **OK** to apply the settings and close the window.

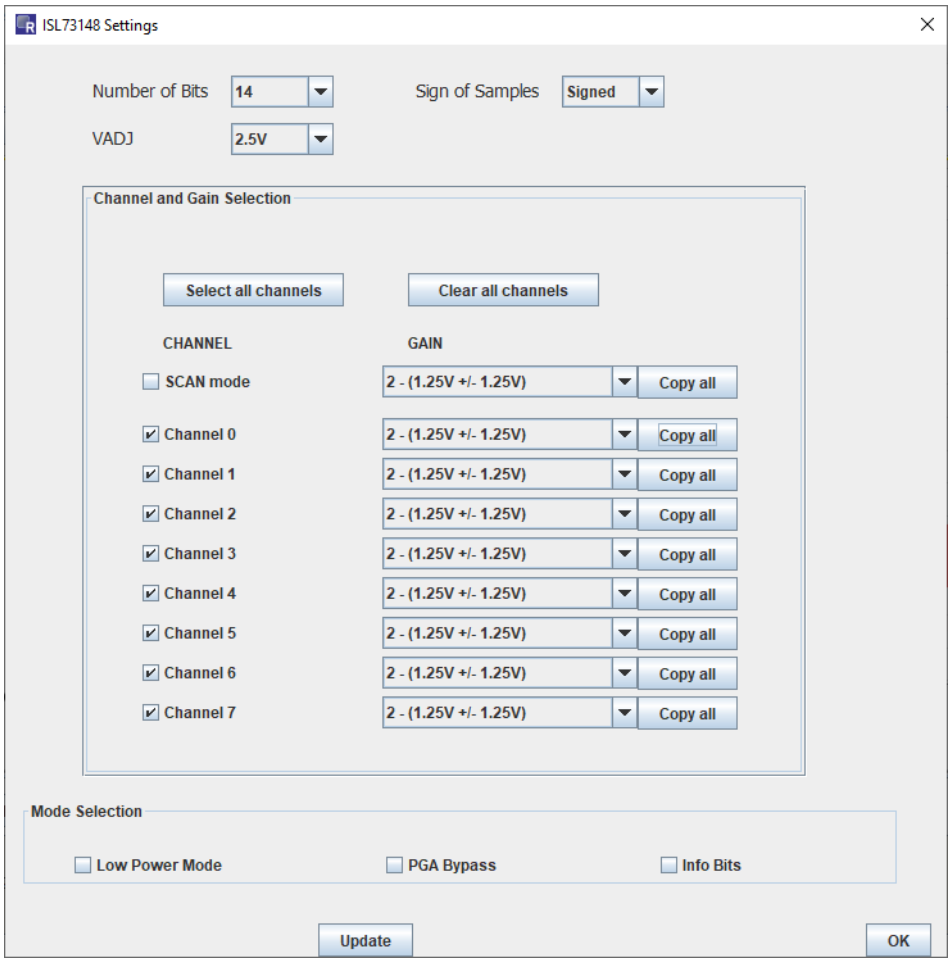

Figure 9. iRADAnalyzer Channel Selection Settings

The numbered boxes above the graph can be used to select 1, 2, 3, 4, 6, or 8 channels to display. When channels have been selected for measurement, the required channels for display must be chosen by clicking on one of these boxes. In this example, all 8 channels are selected. A shortcut box can be used to select all 8 channels to display.

Figure 10. iRADAnalyzer Channel Selection for Plotting

When the required channels for plotting are shown, a measurement can be performed. The active graph is highlighted in yellow. A display of eight channels with channel 0 highlighted is shown in Figure 11. In this case, all 8 channels are configured on the evaluation board to receive the same input signal. Each channel display can be zoomed independently if required by clicking and dragging to create a box in the required plot window for the zoomed in area. The selected plot can be reset by clicking **Reset Selected** to restore it to the full data plot. In addition, the **Reset All** button restores all the channels to the full data plot.

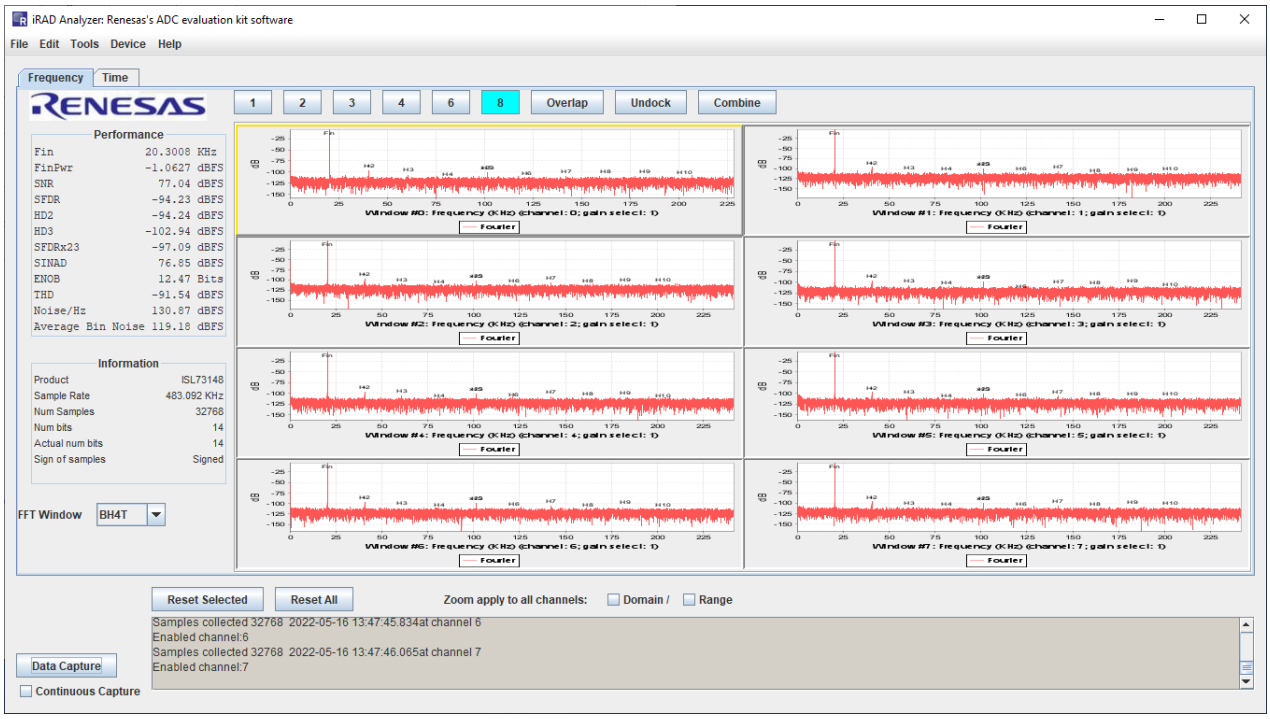

Figure 11. iRADAnalyzer FFT Plot of 8 Channel

In this example, all eight channels are selected for display. Similarly, SCAN mode can be enabled by clicking the check box, which places the ISL73148SEH into SCAN mode where the ADC sequences through all eight channel inputs in order from Ch 0 to Ch 7 in a repeating manner. At each falling edge of CSB, the ISL73148SEH increments the channel. This results in a reduction of the sample rate of each individual channel by a factor of 8. If SCAN mode is enabled, the Info Bits check box must also be enabled. This allows the iRADAnalyzer to read the information bits in the output data of the ISL73148SEH to synchronize data collection to the proper channel.

The data from the channels can be displayed in a few different ways using the buttons above the plots. The plots can be overlapped into a signal plot using the **Overlap** button. This combines all selected channels into one plot giving each channel a different color. This is shown in Figure 12. This feature is enabled and disabled by clicking the **Overlap** button.

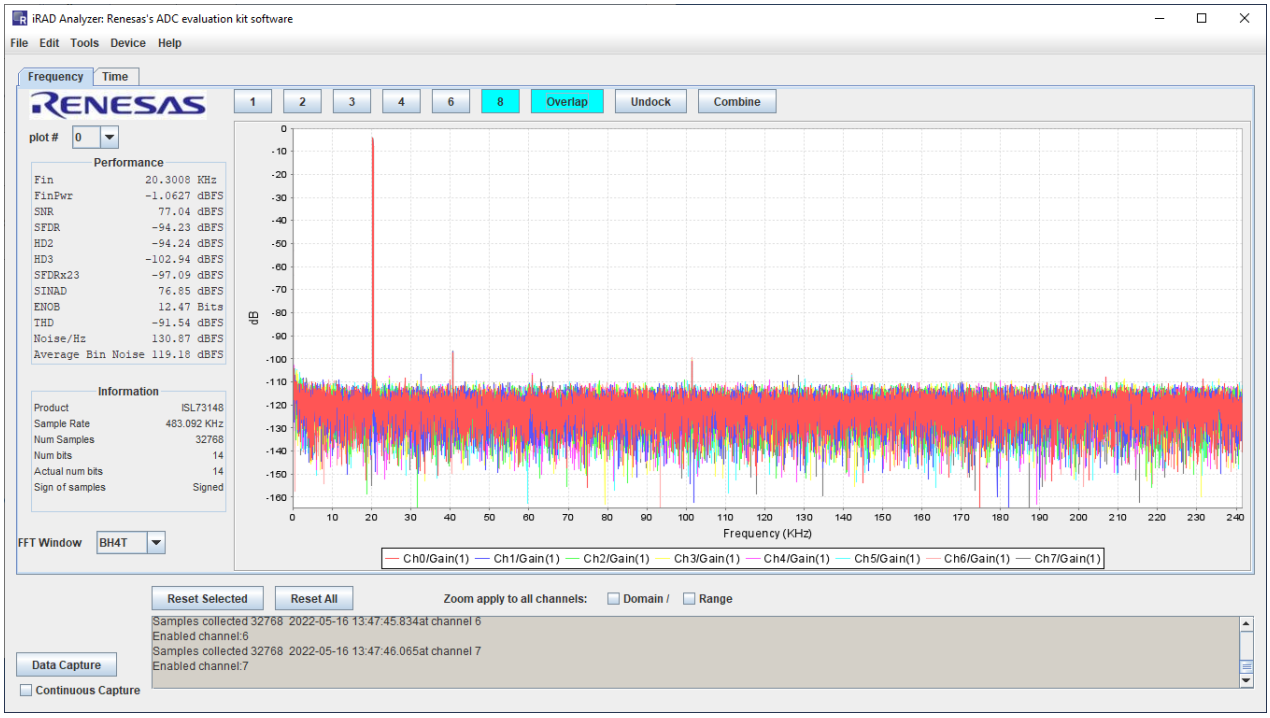

Figure 12. iRADAnalyzer Overlap of 8 Channels

The channel that is currently selected (indicated by the yellow highlight around the box) can be undocked for individual display. This is accomplished by clicking the **Undock** button. Any number of channels that have been measured can be undocked from the main display into a separate window. Each window is labeled with the channel number and gain selection. As an example, the undocked window for Channel 2 is shown in Figure 13.

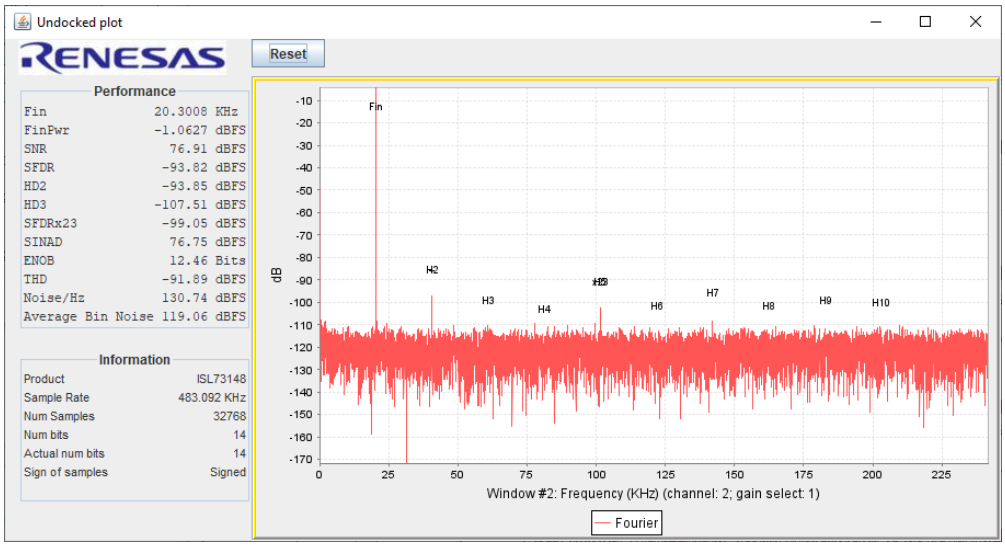

Figure 13. iRADAnalyzer Undocked Window for Channel 2

Individual plots can be combined into one plot by using the **Combine** button. This can be accomplished by selecting the first required plot so that it is highlighted in yellow and then clicking the **Combine** button. Clicking the **Combine** button adds the selected plot to a separate plot window and allows for the selection of an additional plot

to combine from the main window as shown in Figure 14. To add additional channels, click to select the next plot (highlighted in yellow) and then click the **Add** button. It appears in the main window after clicking the **Combine** button.

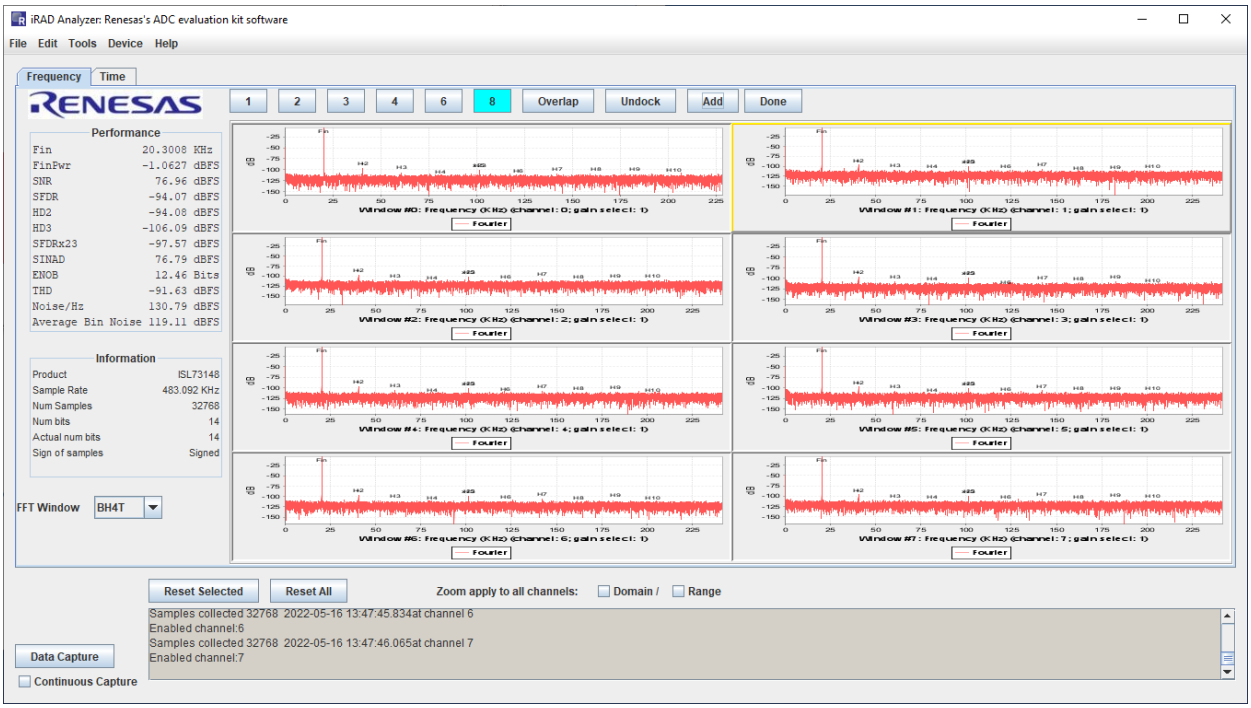

Figure 14. iRADAnalyzer Main Window for Combining Multiple Plots

In this example, the data from Channel 1 and Channel 2 are combined into a separate plot window as shown in Figure 15. When all required plots have been added, click the **Done** button in the main window. Similar to the main window, the plots selected to be combined can also be overlapped from within the combined window by clicking the **Overlap** button in the window.

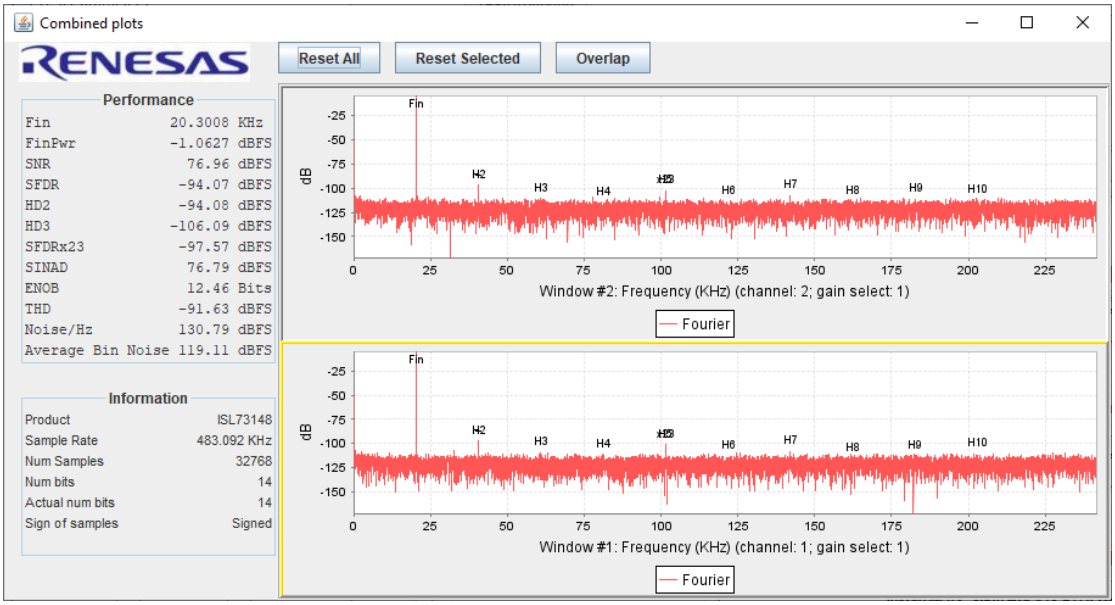

Figure 15. iRADAnalyzer Window with Combined Plots

1.2.6 iRADAnalyzer Data Capture - Time Domain

The time domain plot of the captured data can also be viewed. To do so, click on the **Time** tab in the iRADAnalyzer GUI. This plots the entire data capture in time domain, so Renesas recommends using the mouse to click and drag a zoom box in the time domain plot to be able to see the waveform as shown in Figure 16.

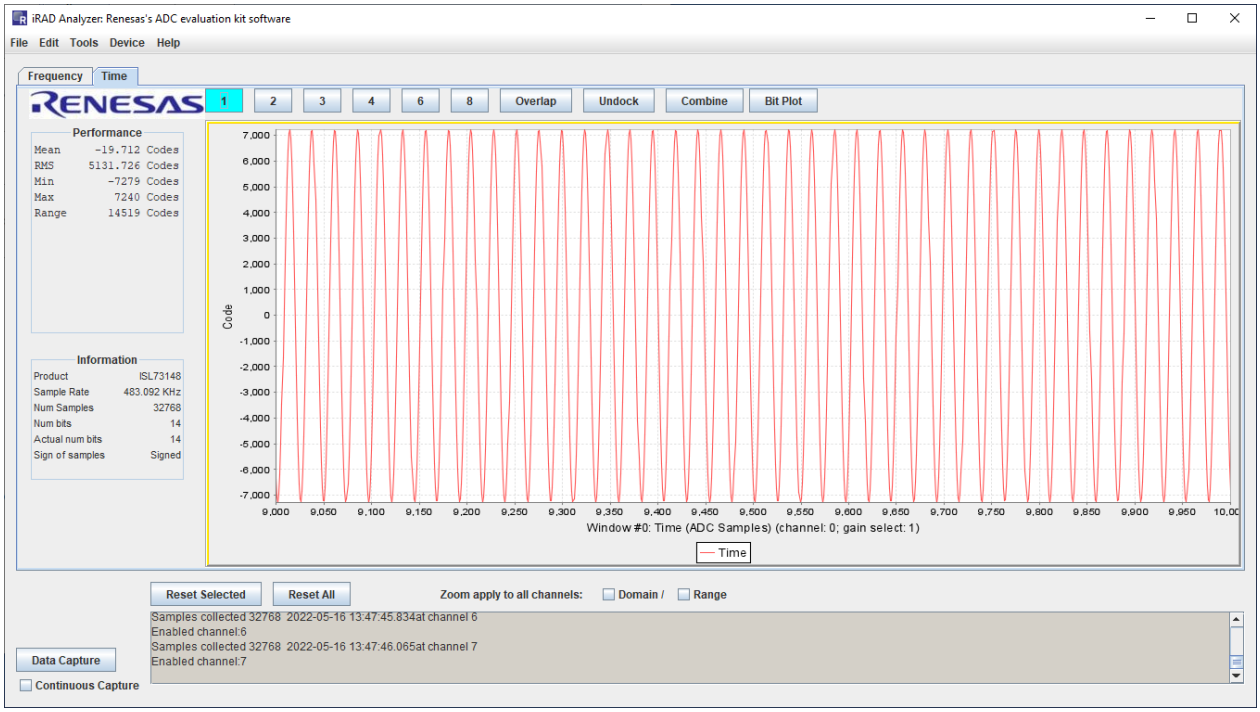

Figure 16. iRADAnalyzer Time Domain Plot

All of the plot features, overlap, undock, and combine, can be used when viewing the time domain plots in iRADAnalyzer and operate in the same manner as when viewing the frequency domain plots. The **Time domain** tab (shown in Figure 17) offers an additional view called Bit Plot, which shows the individual bits plotted over time.

Figure 17. iRADAnalyzer 8-Channel Time Domain Plot

To activate the Bit Plot, first select a channel to highlight it in yellow. It brings up a separate window as shown in Figure 18. This plot can be zoomed and reset similar to the frequency and time domain plots. Renesas recommends zooming as shown in the figure so that the bits are more easily visible. The individual bits can be separated into separate plots if required by using the **Split** button. When the plots are split, a **Consolidate** button appears and can be used to recombine the bits into the same plot again.

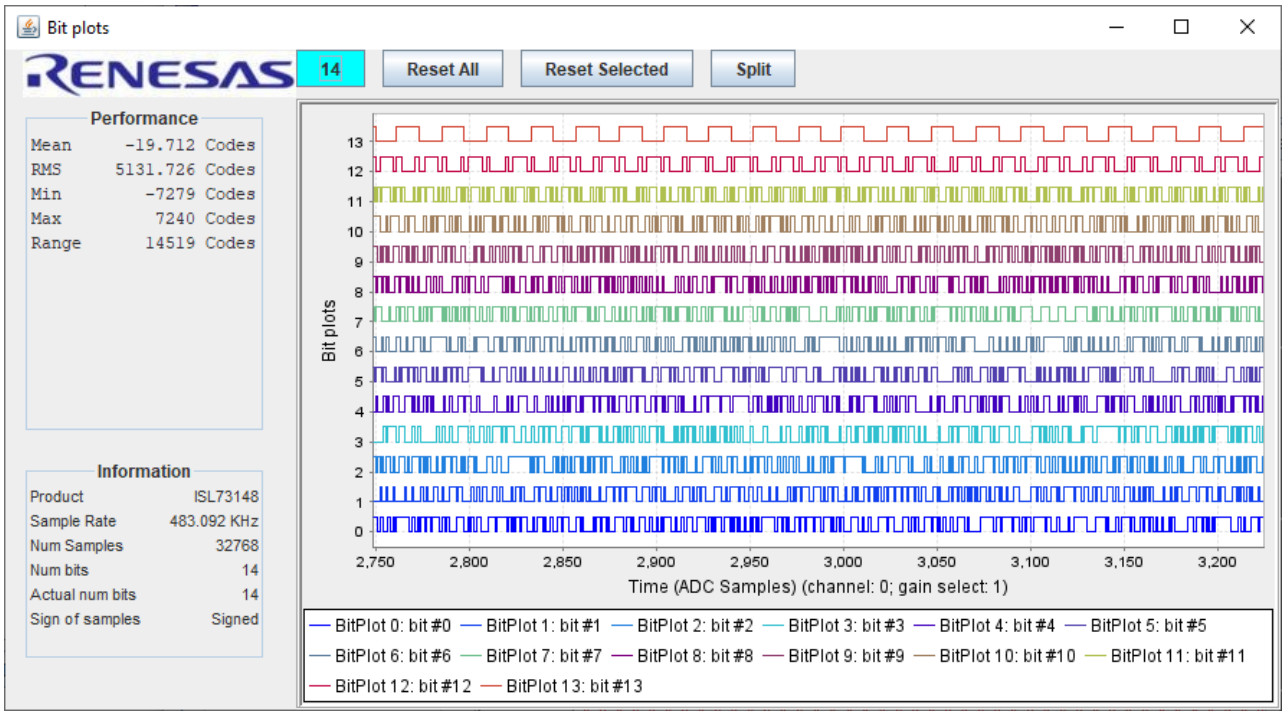

Figure 18. iRADAnalyzer Time Domain Bit Plot

1.2.7 iRADAnalyzer - Save Data Files

When the required data is collected, the iRADAnalyzer GUI can save the raw decimal data or the FFT data to a file. To save the raw decimal data to a file, select **File→Save Data File→SaveTime Domain**. To save the FFT data to a file, select **File→Save Data File→Save Fourier Domain**. The menu options are shown in Figure 19.

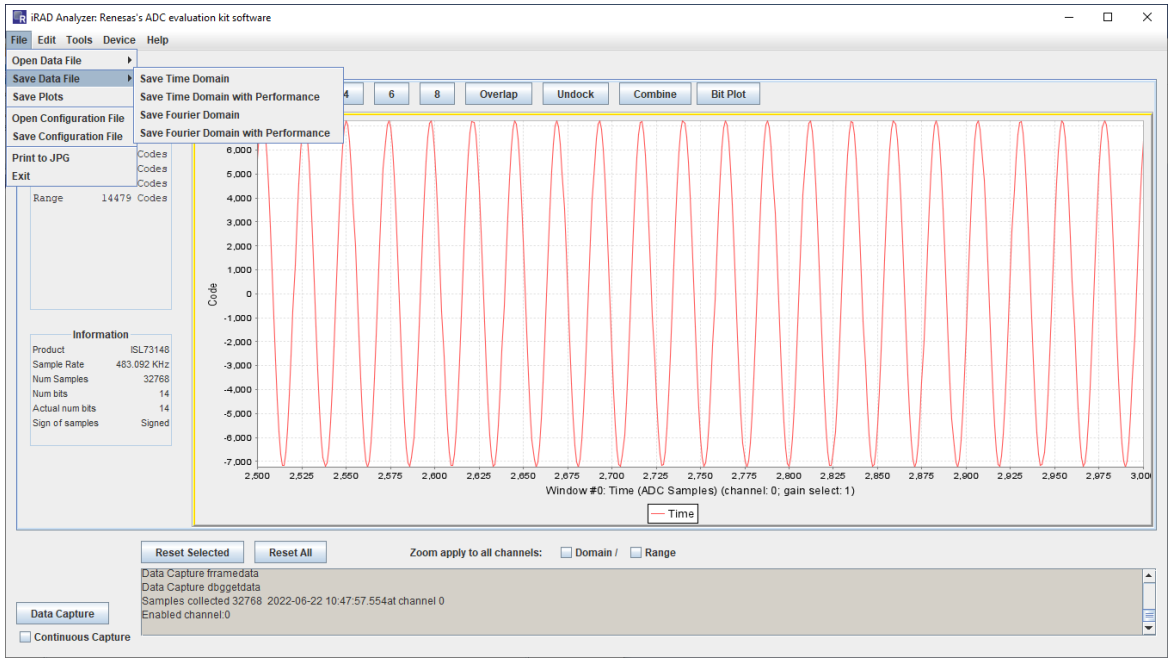

Figure 19. Using iRADAnalyzer to Save Data Files

2. Board Design

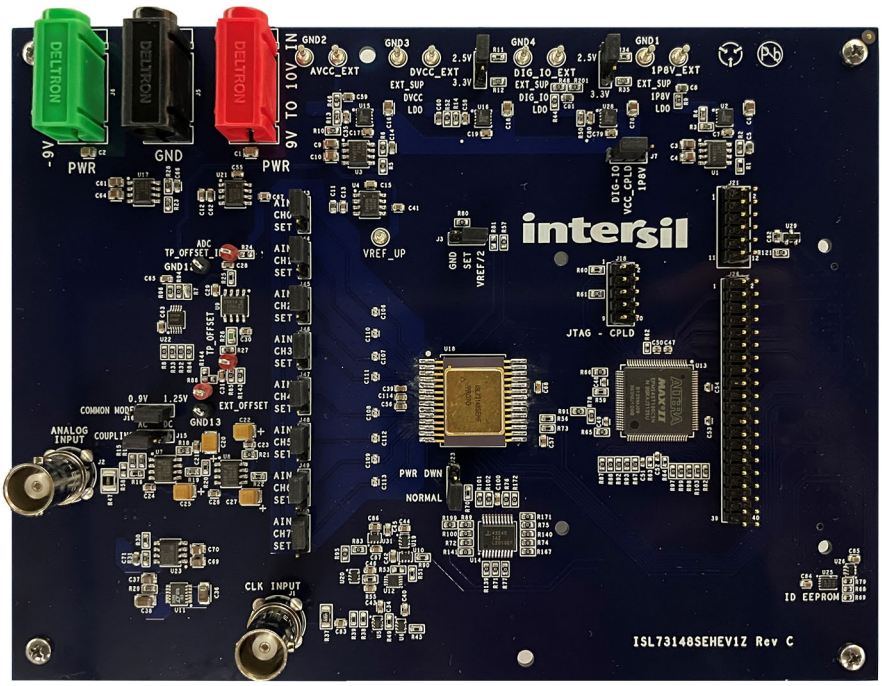

Figure 20. ISL73148SEHEV1Z Evaluation Board (Top)

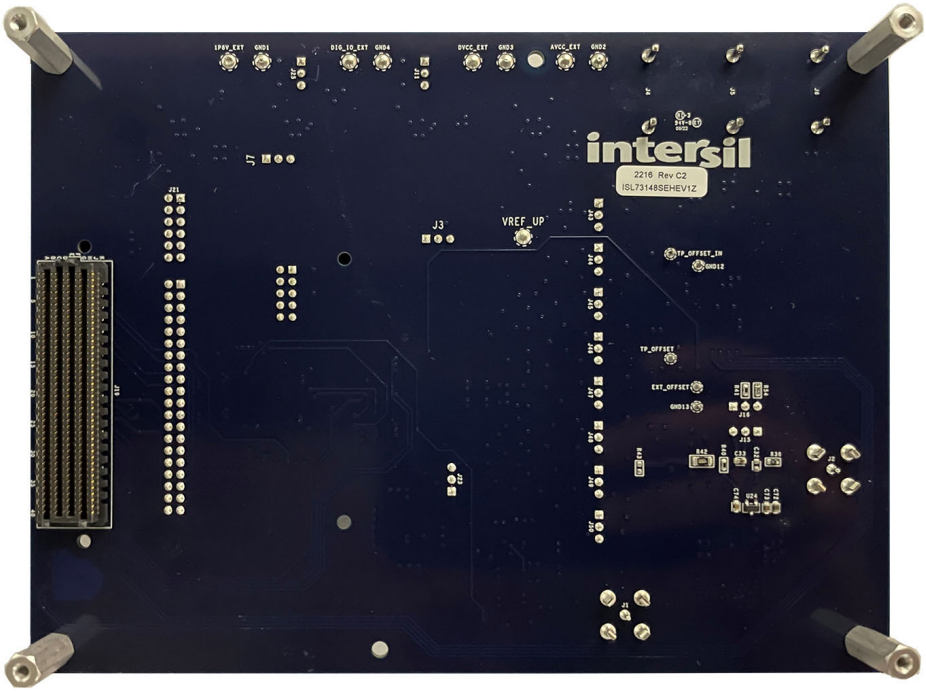

Figure 21. ISL73148SEHEV1Z Evaluation Board (Bottom)

2.1 Layout Guidelines

For information about layout guidelines, see the *ISL73148SEH Datasheet*.

2.2 Board Schematics

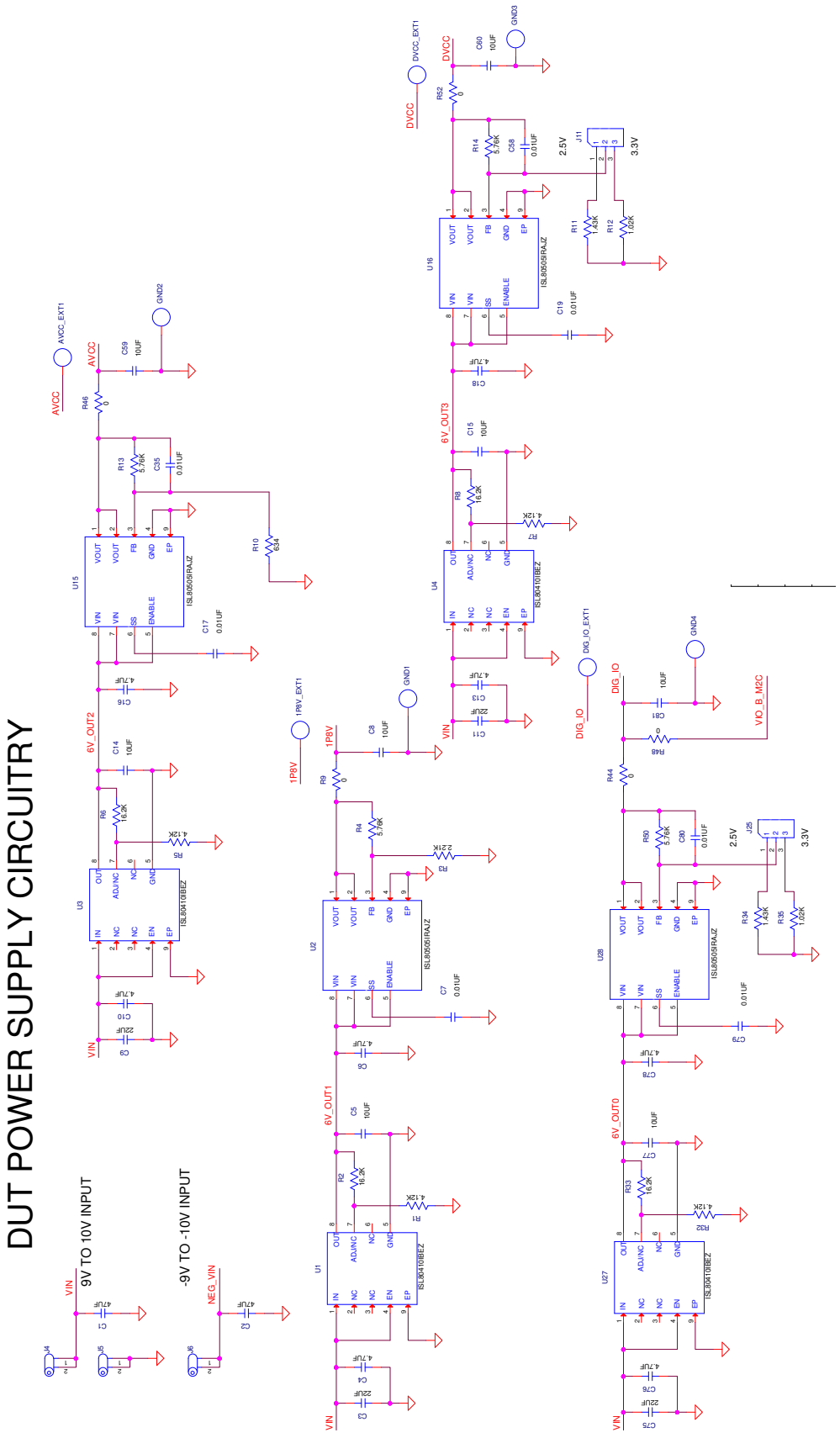

Figure 22. ISL73148SEH Board Schematic - DUT Power Supply Circuit

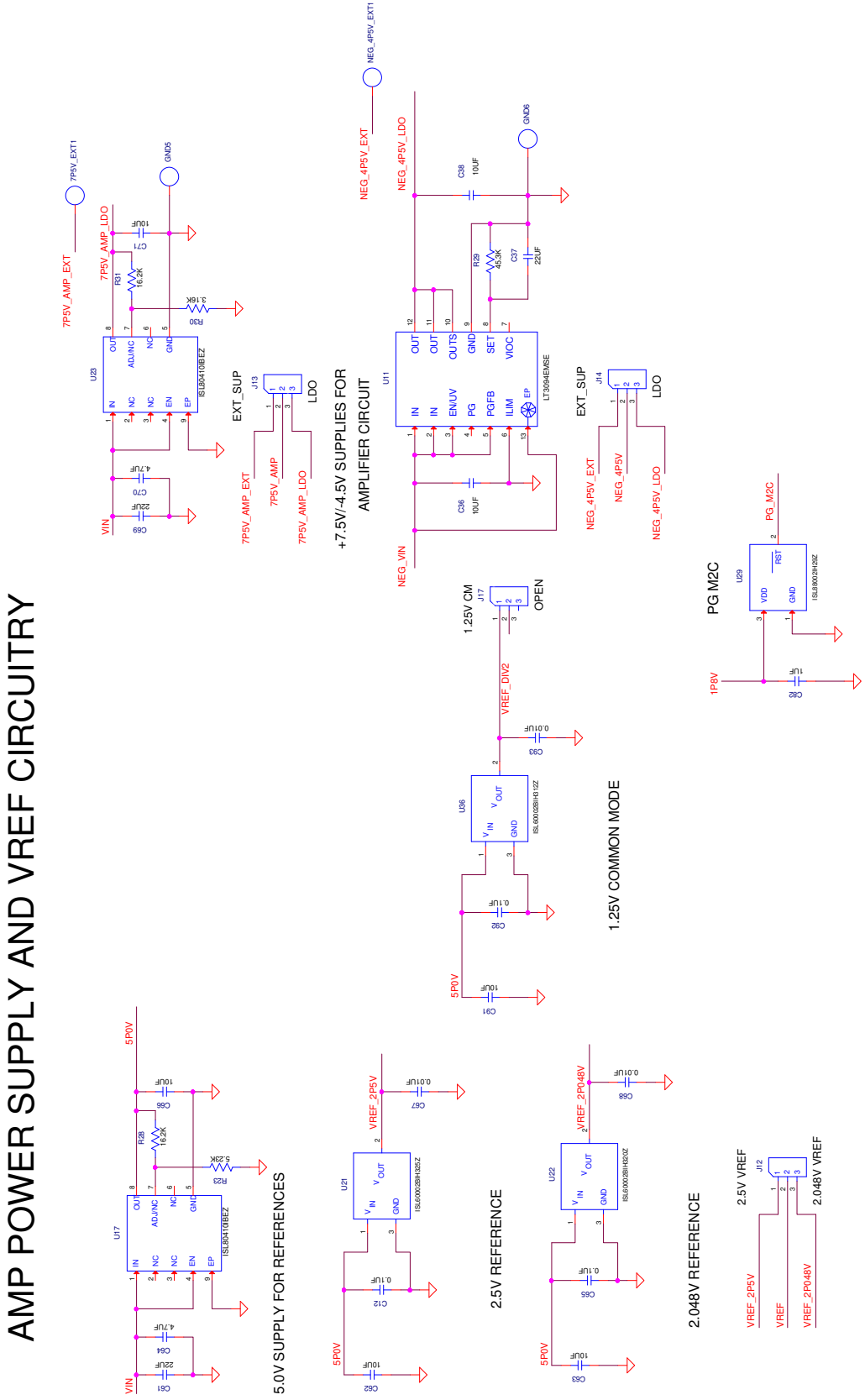

Figure 23. Amplifier Power Supply and VREF Circuits

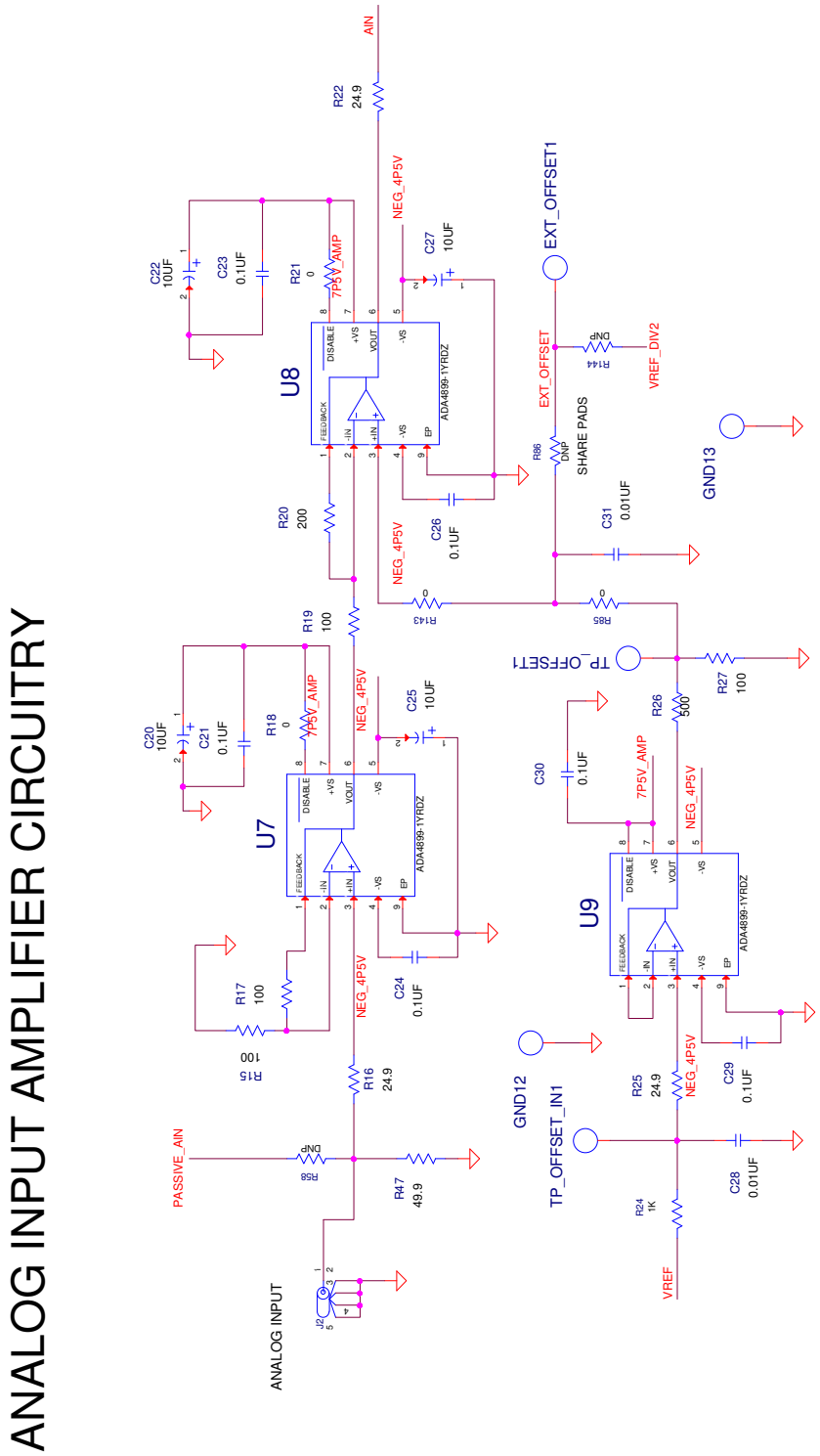

Figure 24. Analog Input Amplifier Circuit

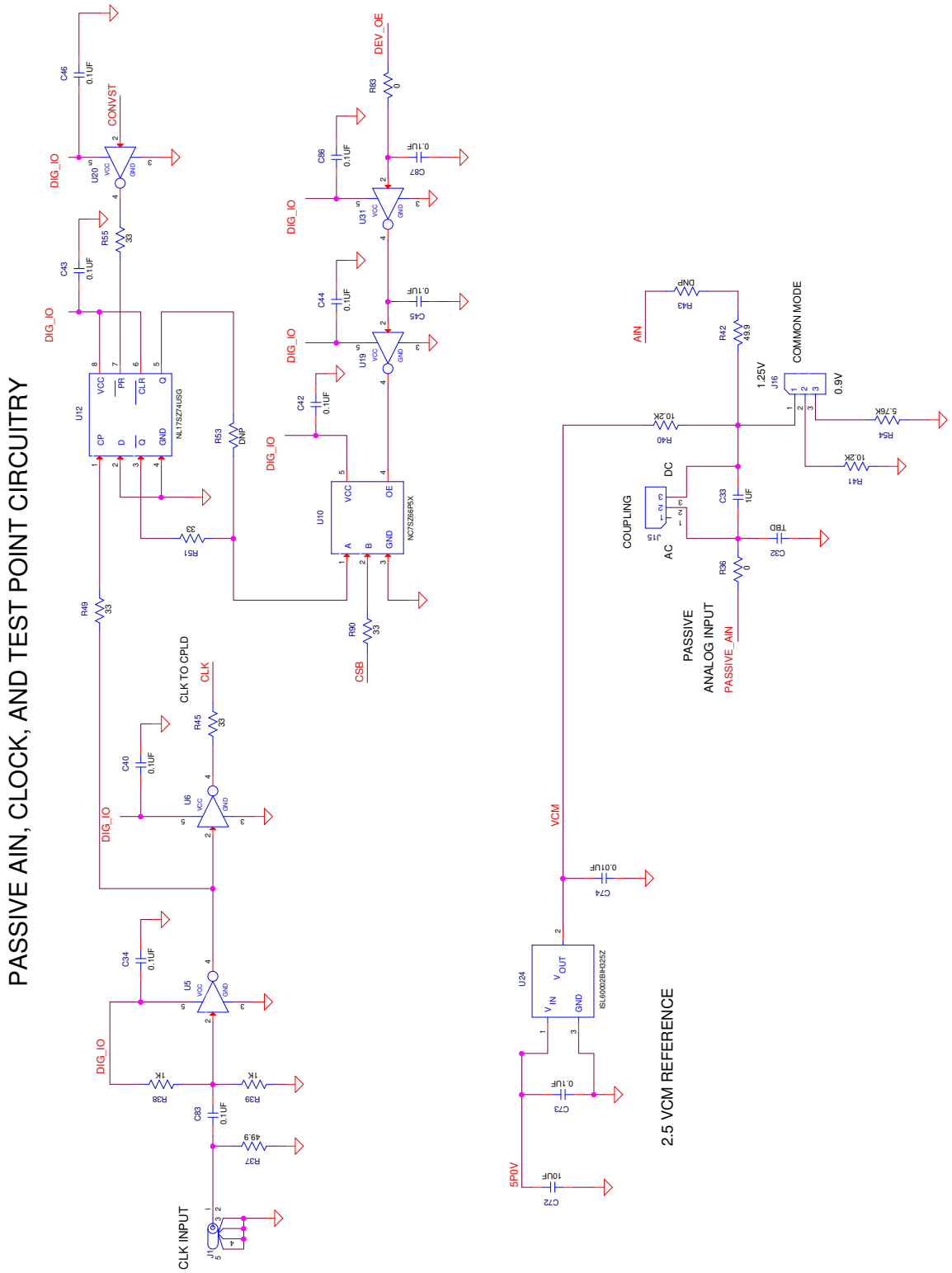

Figure 25. Passive Analog Input and Clock Circuits

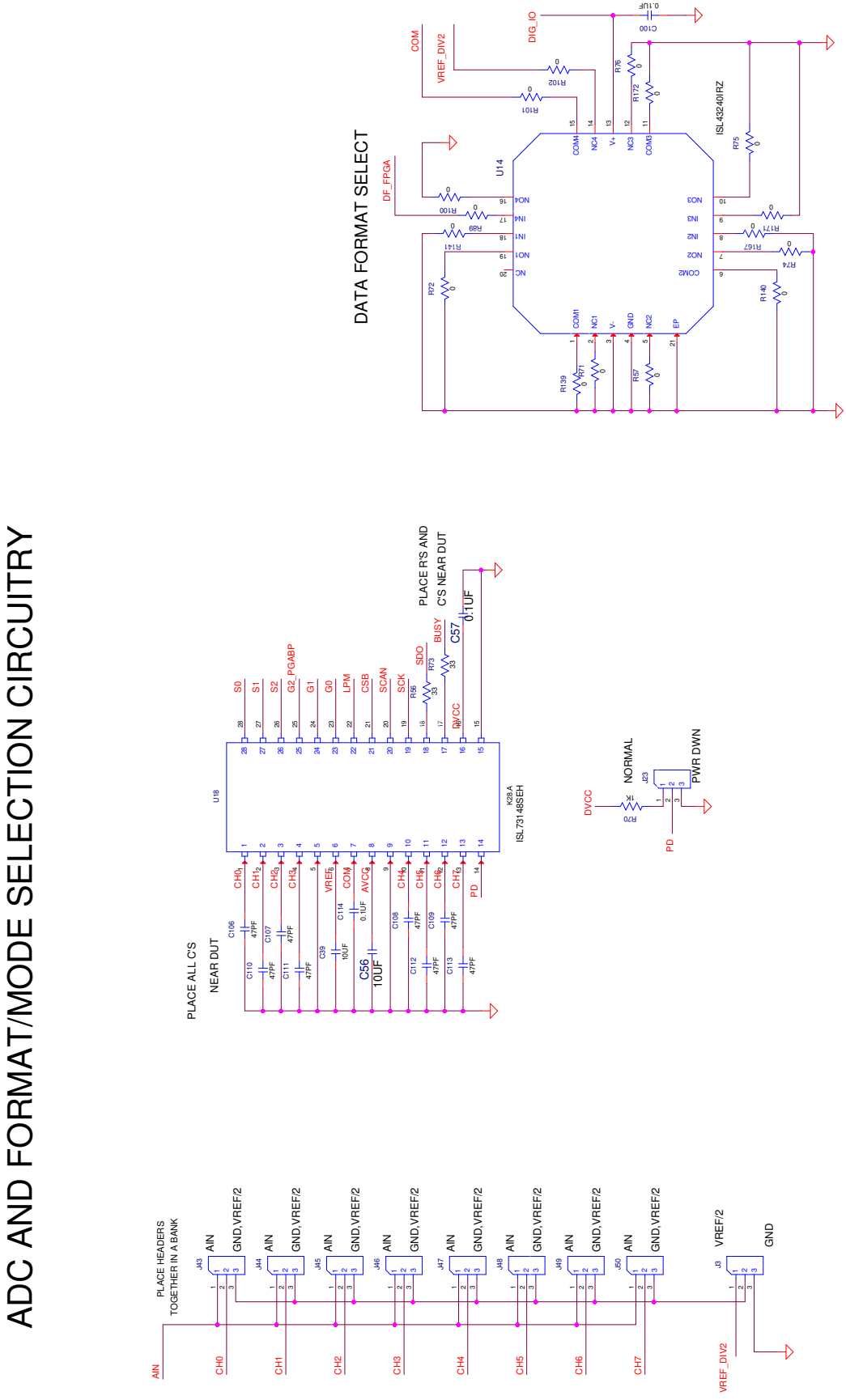

Figure 26. ADC and Format/Mode Selection Circuits

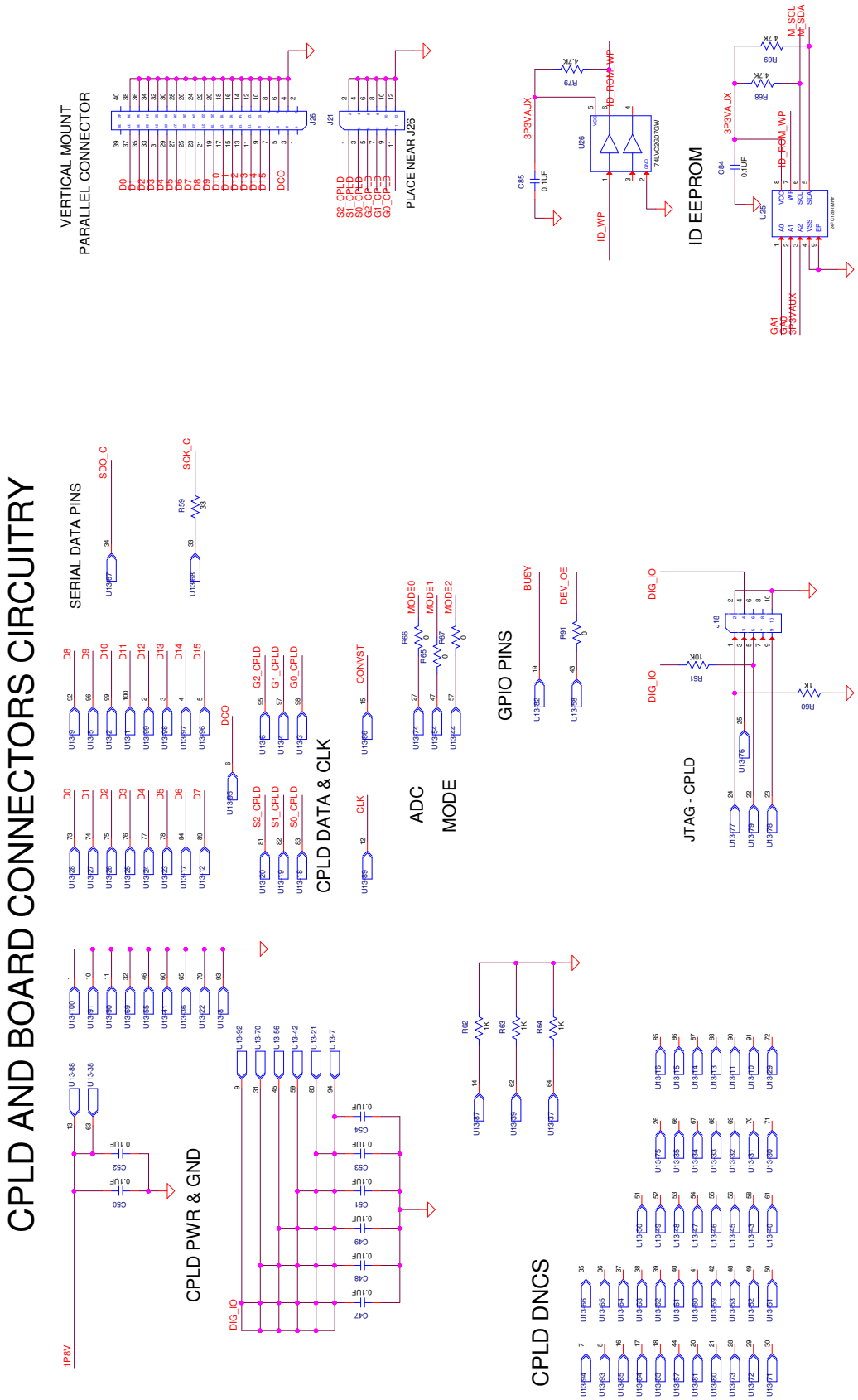

Figure 27. CPLD and Board Connector Circuits

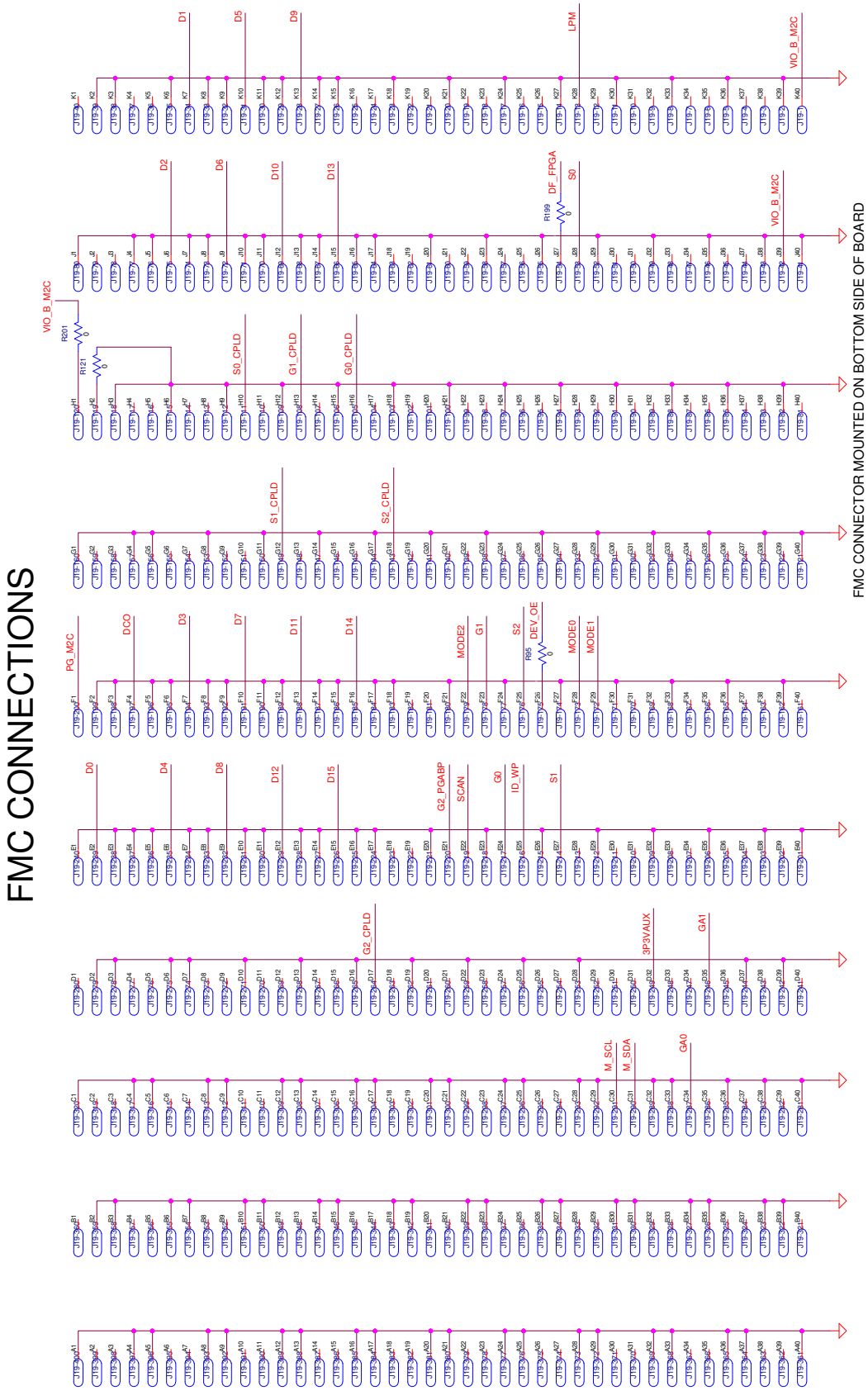

Figure 28. FMC Connector Circuit

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PCB, ISL73148SEHEV1Z, REVC, ROHS	Avanti	ISL73148SEHEV1ZREVCPCB
28	C12, C13, C21, C23, C24, C26, C29, C30, C34, C40, C41, C42, C43, C44, C45, C46, C57, C63, C65, C67, C73, C83, C84, C85, C86, C87, C100, C114	CAPACITOR, SMD, 0603, 0.10µF, 50V, 10%, X7R	TDK	C1608X7R1H104K
8	C4, C6, C10, C16, C18, C64, C70, C78	CAP-AEC-Q200, SMD, 0805, 4.7µF, 25V, 10%, X7R, ROHS	TDK	CGA4J1X7R1E475K125AC
12	C5, C8, C11, C14, C56, C59, C60, C62, C66, C71, C72, C81	CAP, SMD, 0603, 10µF, 16V, 20%, X5R, ROHS	Murata	GRM188R61C106MA73D
1	C39	CAP, SMD, 0603, 10µF, 10V, 20%, X7R, ROHS	Murata	GRM188Z71A106MA73D
5	C3, C9, C37, C61, C69	CAP-AEC-Q200, SMD, 0805, 22µF, 25V, 20%, X5R, ROHS	Murata	GRT21BR61E226ME13L
8	C47-C54	CAP, SMD, 0402, 0.1µF, 16V, 10%, X7R, ROHS	Venkel	C0402X7R160-104KNE
8	C106-C113	CAP, SMD, 0402, 47pF, 50V, 10%, C0G/NP0, ROHS	AVX	04025A470KAT2A
3	C15, C55, C68	CAP, SMD, 0603, 1000pF, 50V, 10%, X7R, ROHS	AVX	06035C102KAT2A
10	C7, C17, C19, C28, C31, C35, C58, C74, C79, C80, C32	CAP, SMD, 0603, 0.01µF, 50V, 10%, X7R, ROHS	AVX	06035C103KAT2A
2	C1, C2	CAP, SMD, 0805, 47µF, 10V, 20%, X5R, ROHS	TDK	C2012X5R1A476M125AC
4	C20, C22, C25, C27	CAP, TANT, SMD, B, 10µF, 16V, 10%, ROHS	Venkel	TA016TCR106KBR
2	C33, C82	CAP, SMD, 0603, 1.0µF, 25V, 10%, X7R, ROHS	Taiyo Yuden	TMK107B7105KA-T
2	C36, C38	CAP, SMD, 1206, 10µF, 25V, 10%, X7R, ROHS	Taiyo Yuden	TMK316B7106KL-TD
9	1P8V_EXT, AVCC_EXT, DIG_IO_EXT, DVCC_EXT, GND1-GND4, VREF_UP	CONN-GEN, TURRET, SILVER, 0.082 LENGTH, 0.076 MOUNT HOLE	Cambion	160-2043-02-01-00
2	J1, J2	CONN-BNC, RECEPTACLE, TH, 4 POST, 50Ω, SILVERCONTACT, ROHS	Amphenol	31-5329-51RFX
3	EXT_OFFSET, TP_OFFSET, TP_OFFSET_IN	CONN-COMPACT TEST PT, VERTICAL, RED, ROHS	Keystone	5005
2	GND12, GND13	CONN-COMPACT TEST PT, VERTICAL, BLK, ROHS	Keystone	5006
1	J5	CONN-PLUG, BANA-INSUL-SDRLESS, BLACK, 4mm, RA	Deltron	571-0100

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	J6	CONN-PLUG, BANA-INSUL-SDRLESS, GREEN, 4mm, ROHS, RA	Deltron	571-0400
1	J4	CONN-PLUG, BANA-INSUL-SDRLESS, RED, 4mm, RA	Deltron	571-0500
1	J26	CONN-HEADER, 2x20, BRKAWY-2x36, 2.54mm, ROHS	BERG/FCI	67996-272HLF
1	J18	CONN-HEADER, 2x5, BRKAWY-2x36, 2.54mm, ROHS	BERG/FCI	67996-272HLF
1	J21	CONN-HEADER, 2X6, BRKAWY-2x36, 2.54mm, ROHS	BERG/FCI	67996-272HLF
15	J3, J7, J11, J15, J16, J23, J25, J43, J44, J45, J46, J47, J48, J49, J50	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
1	J19	CONN-SOCKET ARRAY, SMD, 400P, 0.05 PITCH, CUSTOM, ROHS	Samtec	ASP-134602-01
15	PINS 1-2: J3, J7, J11, J15, J16, J23, J25, J43, J44, J45, J46, J47, J48, J49, J50	CONN-JUMPER, SHUNT, 2P, 2.54mmPITCH, BLK, 6mm, OPEN, ROHS	Sullins	SPC02SYAN
1	U25	IC-128KBIT, I2C SERIAL EEPROM, 1.7-5.5V, 8P, TDFN, ROHS	Microchip Technology	24FC128T-I/MNY
1	U26	IC-BUFFER/LINE DRIVER, NON-INVERT, OPEN DRAIN, 6P, TSSOP, ROHS	NXP Semiconductor	74LVC2G07GW, 125
3	U7-U9	IC-OP AMP, HI SPEED, LOW NOISE, 8P, SOIC, ROHS	Analog Devices	ADA4899-1YRDZ
1	U13	IC-2.5-V, 3.3-V CPLD, 100P, TQFP, ROHS	Altera	EPM240T100C5N
2	U4, U21	IC-PREC.VOLTAGE REFERENCE, 8P, SOIC, 2.5VOUT, ROHS	Renesas Electronics America	ISL21090BFB825Z-TK
1	U22	IC-LOW VOLTAGE DCP, 10LD MSOP, ROHS	Renesas Electronics America	ISL23315WFUZ
1	U14	IC-QUAD SPDT ANALOG SWITCH, 20P, SSOP, ROHS	Renesas Electronics America	ISL43240IAZ
1	U24	IC-2.5V, PREC.VOLT.REFERENCE, SMD, 3P, SOT-23, ROHS	Renesas Electronics America	ISL60002BIH325Z-TK
1	U18	14-bit 8-Ch 900/480ksps Precision SAR ADC	Renesas Electronics America	ISL73148SEH/PROTO
4	U1, U3, U17, U23	IC-40V, 150mA LDO REGULATOR, 8P, EPSOIC, ROHS	Renesas Electronics America	ISL80410IBEZ
4	U2, U15, U16, U28	IC-Single 500mA, AdjVout LDO, 3x3, 8ld, DFN, Pb-FREE W/ANNEAL	Renesas Electronics America	ISL80505IRAJZ

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	U29	IC-2.92V VOLTAGE SUPERVISOR, SMD, 3P, SOT-23, ROHS	Renesas Electronics America	ISL88002IH29Z
1	U11	IC-500mA, -2.3V, ADJ. VOLTAGE REGULATOR, 12P, MSOP, ROHS	Linear Tech/Analog Devices	LT3094EMSE#PBF
1	U5	IC-INVERTER, SINGLE CIRCUIT/INPUT, SMD, 5P, SC70-5, ROHS	ON Semiconductor	NC7S04P5X
4	U6, U19, U20, U31	IC-INVERTER, SINGLE CIRCUIT/INPUT, SMD, 5P, SC70-5, ROHS	ON Semiconductor	NC7SVU04P5X
1	U10	IC-BUS SWITCH, SPST, SMD, 5P, SC70-5, ROHS	ON Semiconductor	NC7SZ66P5X
1	U12	IC-FLIP FLOP, 1 ELEMENT D-TYPE, 8P, VFSOP, ROHS	ON Semiconductor	NL17SZ74USG
4	R15, R17, R19, R27	RES-AEC-Q200, SMD, 0603, 100Ω, 1/10W, 0.1%, THINFILM, ROHS	Panasonic	ERA-3AEB101V
0	R43, R53, R58, R81, R86, R144	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER		
3	R62, R63, R64	RES, SMD, 0402, 1k, 1/16W, 1%, TF, ROHS	Venkel	CR0402-16W-1001FT
3	R68, R69, R79	RES, SMD, 0402, 4.7k, 1/16W, 1%, TF, ROHS	Venkel	CR0402-16W-4701FT
8	R45, R49, R51, R55, R56, R59, R73, R90	RES, SMD, 0603, 33Ω, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-33R0FT
54	R7, R8, R9, R18, R21, R32, R33, R36, R44, R46, R48, R52, R57, R65, R66, R67, R71, R72, R74, R75, R76, R77, R78, R80, R82, R83, R84, R85, R87, R88, R89, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101, R102, R103, R121, R139, R140, R141, R143, R167, R171, R172, R199, R201	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	Venkel	CR0603-10W-000T
4	R38, R39, R60, R70	RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1001V
1	R61	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
2	R12, R35	RES, SMD, 0603, 1.02k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-071K02L
2	R40, R41	RES, SMD, 0603, 10.2k, 1/10W, 1%, TF, ROHS	Yageo	9C06031A1022FKHFT
2	R11, R34	RES, SMD, 0603, 1.43k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1431V

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
4	R2, R6, R28, R31	RES, SMD, 0603, 16.2k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1622V
1	R20	RES, SMD, 0603, 200Ω, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2000FT
1	R3	RES, SMD, 0603, 2.21k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-072K21L
3	R16, R22, R25	RES, SMD, 0603, 24.9Ω, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF24R9V
1	R30	RES, SMD, 0603, 3.16k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF3161V
1	R29	RES, SMD, 0603, 45.3k, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-0745K3L
1	R5	RES, SMD, 0603, 4.64k, 1/10W, 1%, TF, ROHS	Yageo	9C06031A4641FKHFT
1	R23	RES, SMD, 0603, 5.23k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF5231V
5	R4, R13, R14, R50, R54	RES, SMD, 0603, 5.76k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-5761FT
1	R10	RES, SMD, 0603, 634Ω, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-07634RL
1	R1	RES, SMD, 0603, 9.53k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-9531FT
2	R37, R42	RES, SMD, 1206, 49.9Ω, 1/4W, 1%, TF, ROHS	Vishay/Dale	CRCW120649R9FKEA
1	R47	RES, SMD, 1210, 49.9Ω, 1/4W, 1%, TF, ROHS	Venkel	CR1210-4W-49R9FT
1	R26	RES, SMD, 0805, 500Ω, 1/10W, 0.1%, 25ppm, THINFILM, ROHS	KOA	RN732ATTD5000B25
4	Four corners	SCREW, 4-40X1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Building Fasteners	PMSSS 440 0025 PH
4	Four corners	STANDOFF, 4-40x5/8in, F/F, HEX, ALUMINUM, 1/4in.OD, ROHS	McMaster-Carr	91780A165

2.4 Evaluation Board Layout

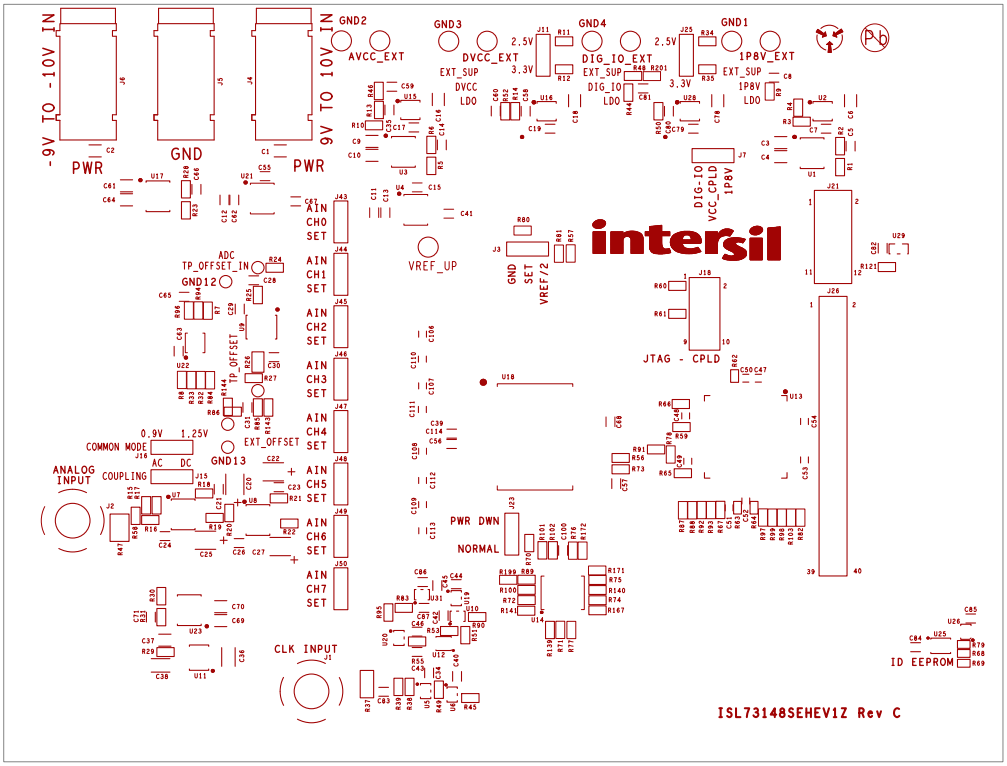

Figure 29. Top Silkscreen

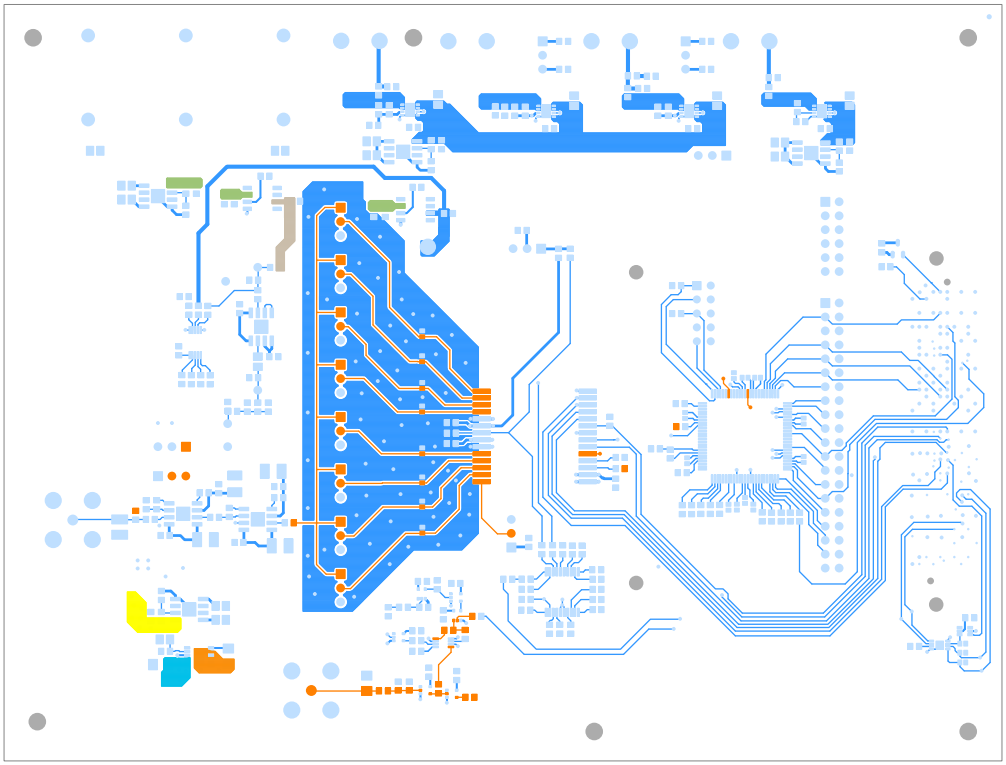

Figure 30. Top Layer

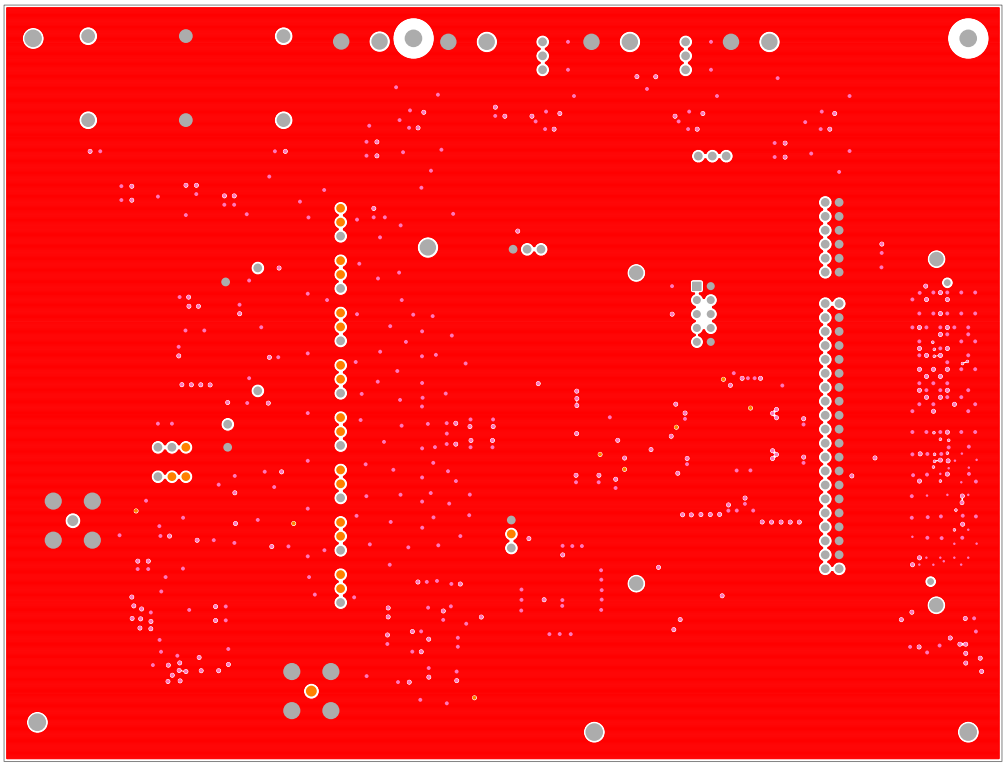

Figure 31. Layer 2

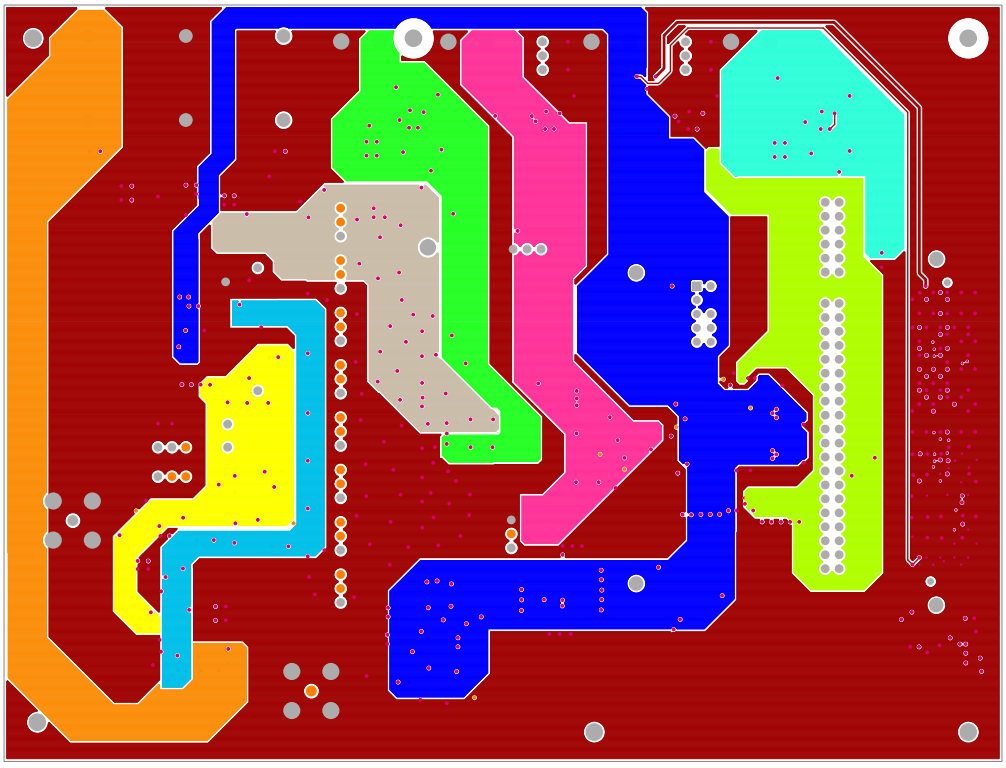

Figure 32. Layer 3

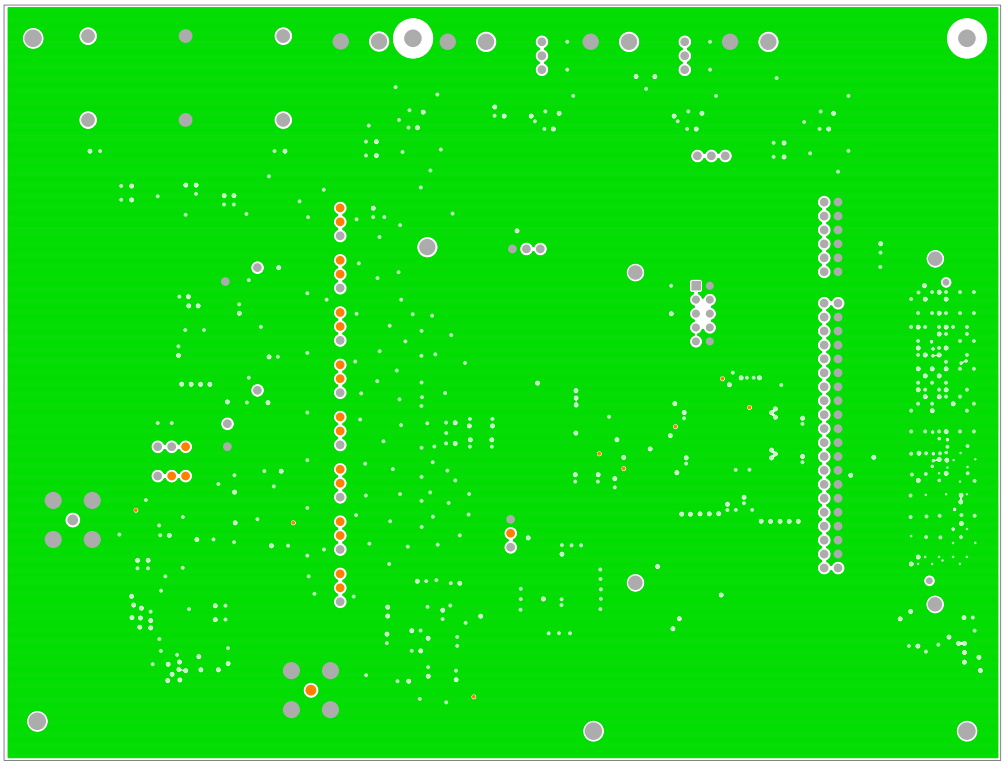

Figure 33. Layer 4

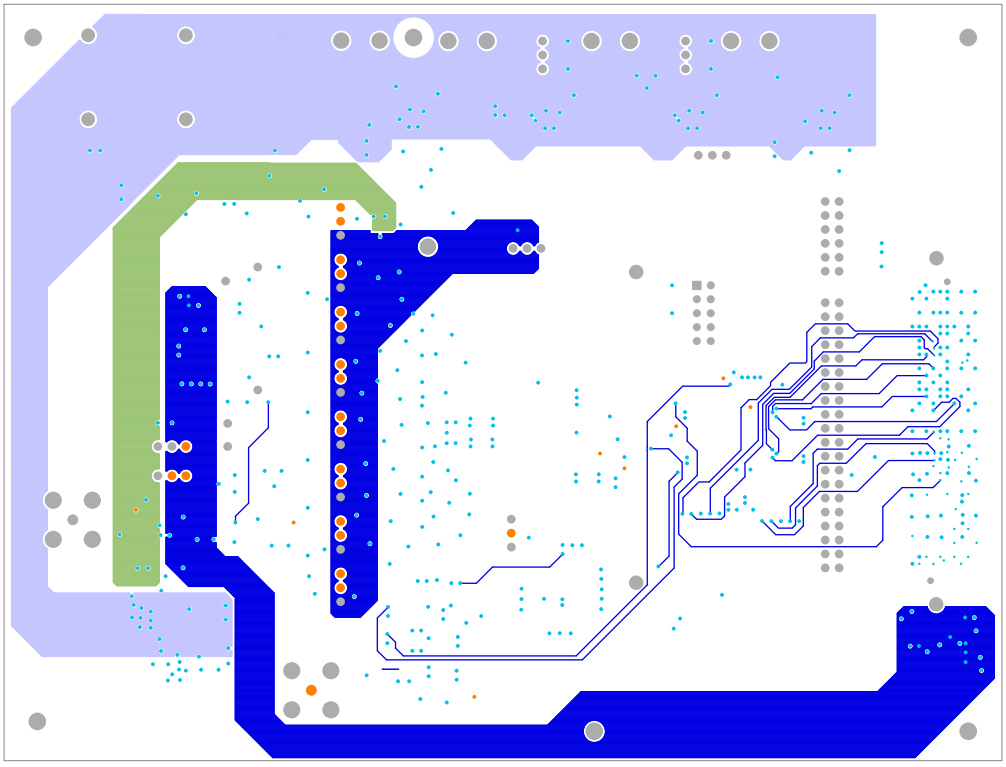

Figure 34. Layer 5

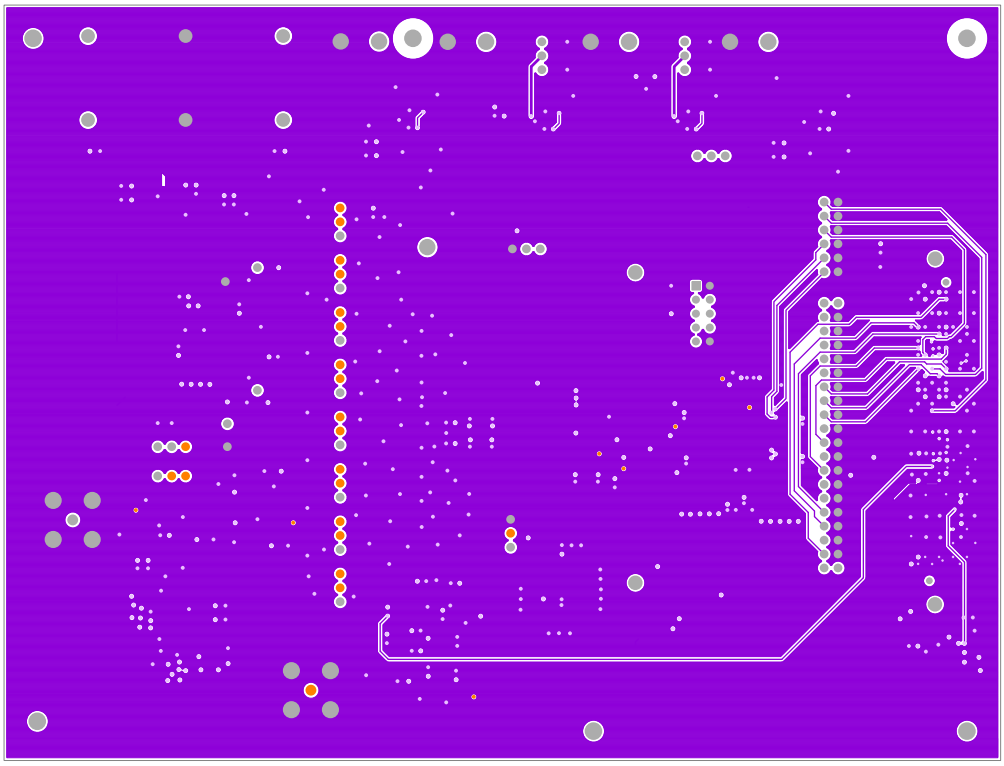

Figure 35. Layer 6

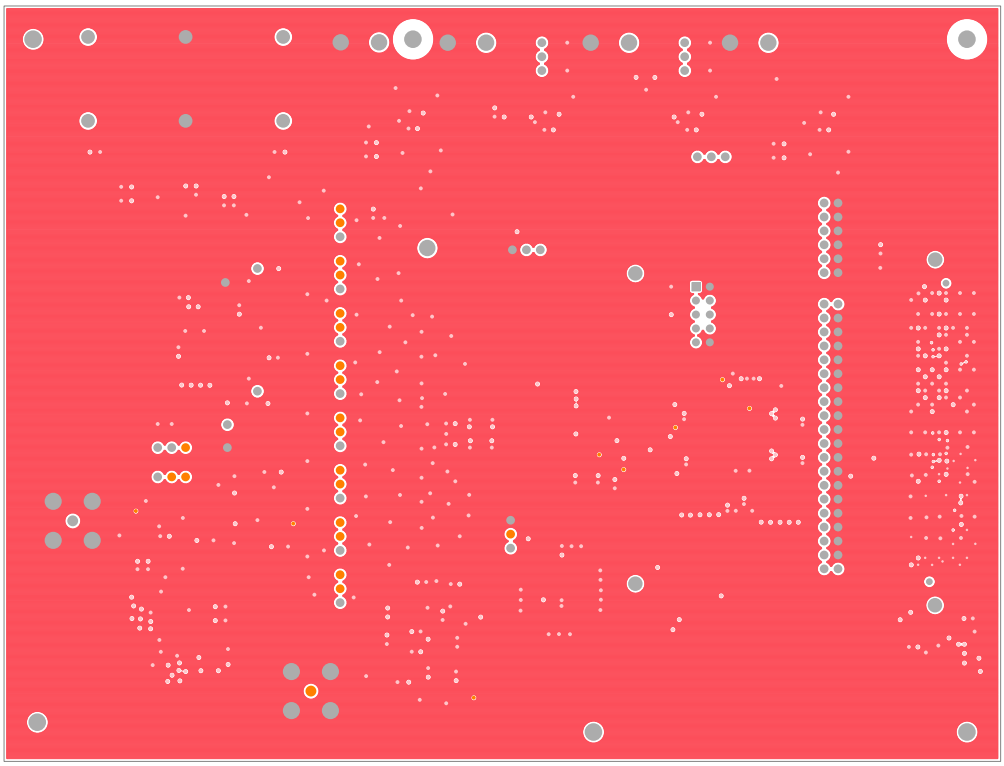

Figure 36. Layer 7

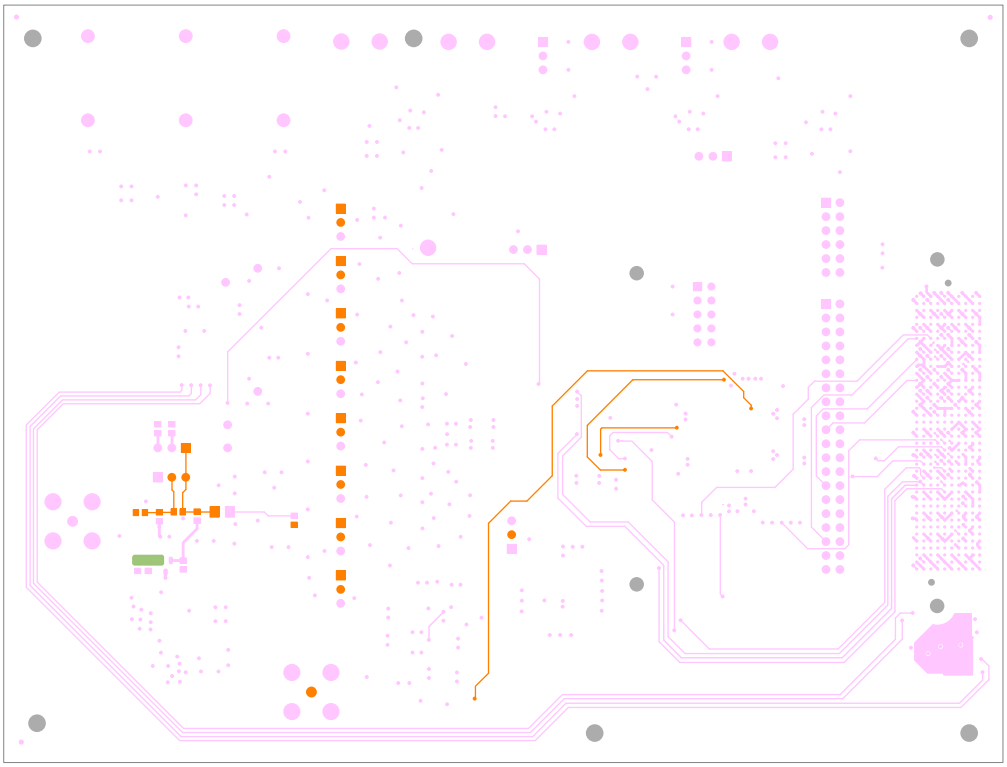

Figure 37. Bottom Layer

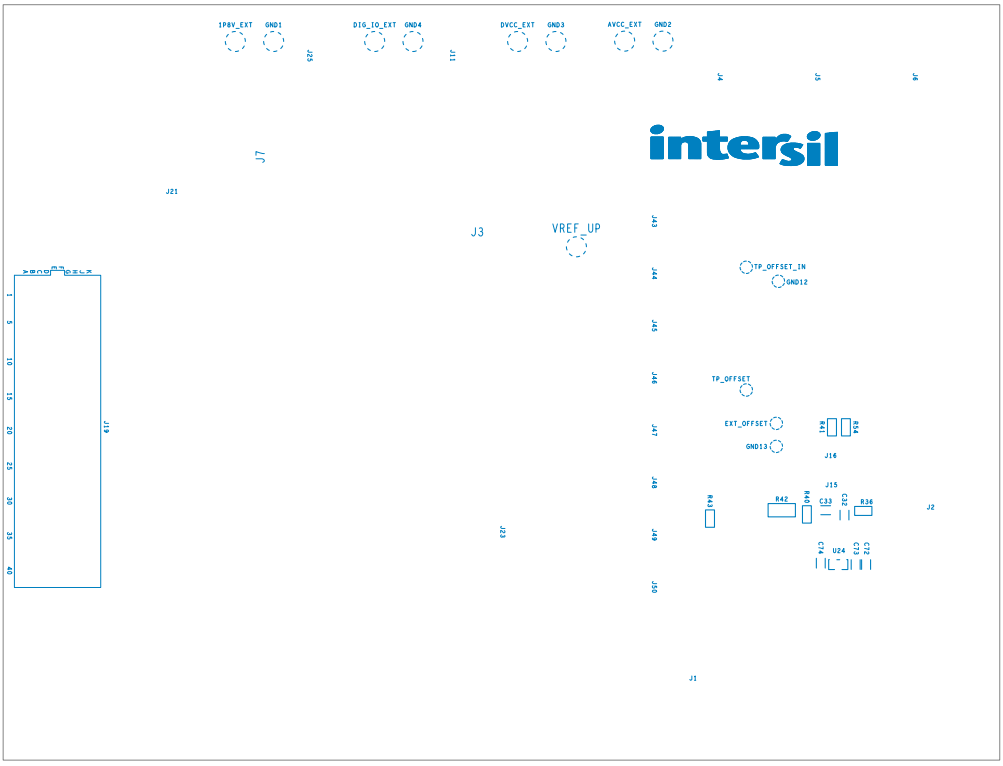

Figure 38. Bottom Silkscreen

3. Ordering Information

Part Number	Description
ISL73148SEHEV1Z	ISL73148SEH 14-Bit 900ksps SAR ADC evaluation board

4. Revision History

Revision	Date	Description
1.03	Jun 18, 2024	Added the Required Equipment section on page 1.
1.02	Feb 1, 2024	Updated Figure 1 and Table 1.
1.01	Apr 11, 2023	Updated the Bill of Materials.
1.00	Jul 5, 2022	Initial release

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