User's Manual

ISL78083DEMO1Z

User's Manual: Demonstration Board

Automotive

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ISL78083DEMO1Z

Demonstration Board

The ISL78083DEMO1Z demonstrates the performance of the ISL78083 multi-output DC/DC regulator comprised of a primary high voltage buck regulator, two secondary low voltage synchronous buck regulators, and a secondary low voltage LDO regulator. The ISL78083 is intended for high-density power applications, requiring few external components and minimal board space. The ISL78083 provides up to four regulated outputs with full protection and offers three power-good indicators and a reset/fault indicator.

Key Features

- V_{IN} operating range from 4.0V to 42V
  - Start range: 4.5V to 42V
- Fixed switching frequency: 2.2MHz with optional pseudo-random spread spectrum
- Three synchronous bucks with internal compensation and one LDO
  - Buck1 output range: 3.3V to 5.05V
  - Buck2 output range: 1.0V to 3.3V
  - Buck3 output range: 1.0V to 3.3V
  - LDO4 output range: 2.8V to 3.4V
- Output UV/OV thresholds, OTP: ±4%, ±6%, ±8%, ±12%
- OTP power up/down sequence and delay
- Optional output discharge on Buck2, Buck3, and LDO4
- Current at VIN input under shutdown: <1µA typical
- Protection features
  - Input voltage UVLO
  - Output OV/UV
  - Positive and negative current limits on bucks
  - Overcurrent protection on internal and output LDOs
  - Fail-safe controller
  - CRC of OTP registers
- OTP hiccup or latch-off fault response

Specifications

- V_{IN} = 4V to 42V (start range: 4.5V to 42V)
- Buck1 output range: 3.3V to 5.05V, up to 0.75A
- Buck2 output range: 1.0V to 3.3V, up to 0.75A
- Buck3 output range: 1.0V to 3.3V, up to 0.75A
- LDO4 output range: 2.8V to 3.4V, up to 0.3A
- Three power-good indicators
- Reset output/fault indicator

Ordering Information

Part Number	Description
ISL78083DEMO1Z	ISL78083 demonstration board

Related Literature

For a full list of related documents, visit our website:

- ISL78083 device page

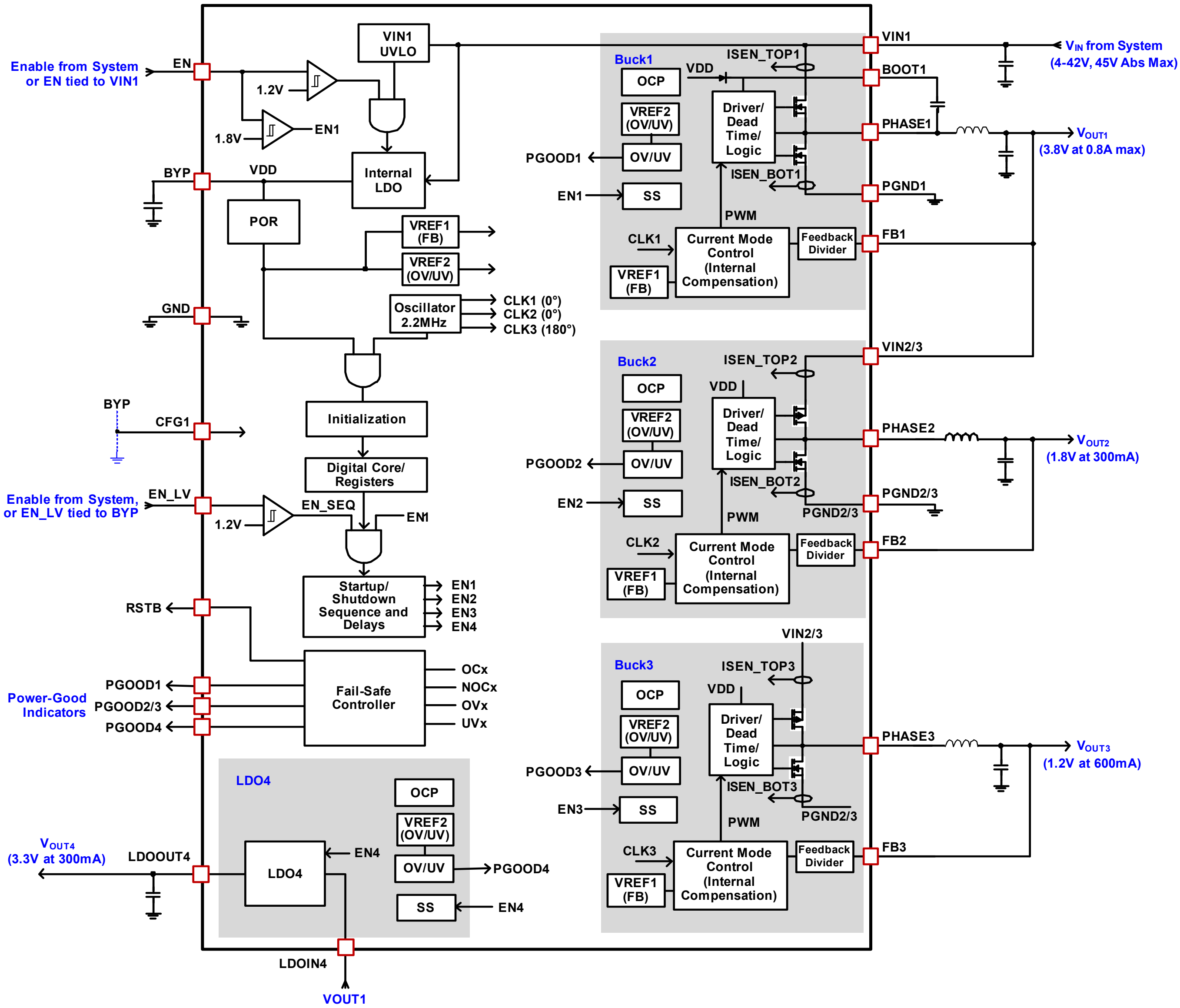

Figure 1. Block Diagram

1. Functional Description

The ISL78083DEMO1Z provides all circuits required to demonstrate the features of the ISL78083. A majority of the features of the ISL78083, such as four regulated outputs, output enable, and Power Good indicators are available on this demonstration board.

1.1 Required Equipment

- 0V to 42V power supply with 2A source current capability
- Up to four electronic loads capable of sinking current up to 1A
- Digital Multimeters (DMMs)
- Oscilloscope (Optional)

1.2 Quick Start Guide

The ISL78083 can provide up to four regulated DC output voltages derived from a single DC input.

1. Ensure that the circuit is correctly connected to the input supply and loads before applying any power.
2. Connect the high voltage bias supply to VIN1, with the plus terminal to VIN1, and the negative return to GND.
3. Connect each load, if used, to the plus terminal and the negative return terminal of the output being loaded. **Note:** It is not necessary to connect a load to each output to operate the board. Each output regulates with or without a load connected.
4. Ensure that the jumpers for the EN input (see Figure 2 on page 5) and the EN_LV input are connected to GND.
5. Ensure that the loads are off or set to zero current.
6. Connect an input power supply of 12V to VIN1. The input current should be approximately zero. Output voltages VOUT1, VOUT2, VOUT3, VOUT4 should read approximately zero.
7. Connect the 2-pin jumper for EN to VIN. The output of VOUT1 should regulate at 3.8V.
8. Connect the 2-pin jumper for EN_LV to BYP. The outputs should read as follows:
   - VOUT1: 3.8V
   - VOUT2: 1.8V
   - VOUT3: 1.2V
   - VOUT4 (LDOOUT4): 3.3V

1.2.1 System Voltage Regulation

1. Set the power supply to 12V.
2. Connect the 2-pin jumper for EN to VIN.
3. Connect the 2-pin jumper for EN_LV to BYP.
4. Each output can now be loaded independently to measure output voltage regulation, and also power efficiency, output ripple, and load transient response. **Note:** Loads on VOUT2, VOUT3, and VOUT4 appear as loads for VOUT1.

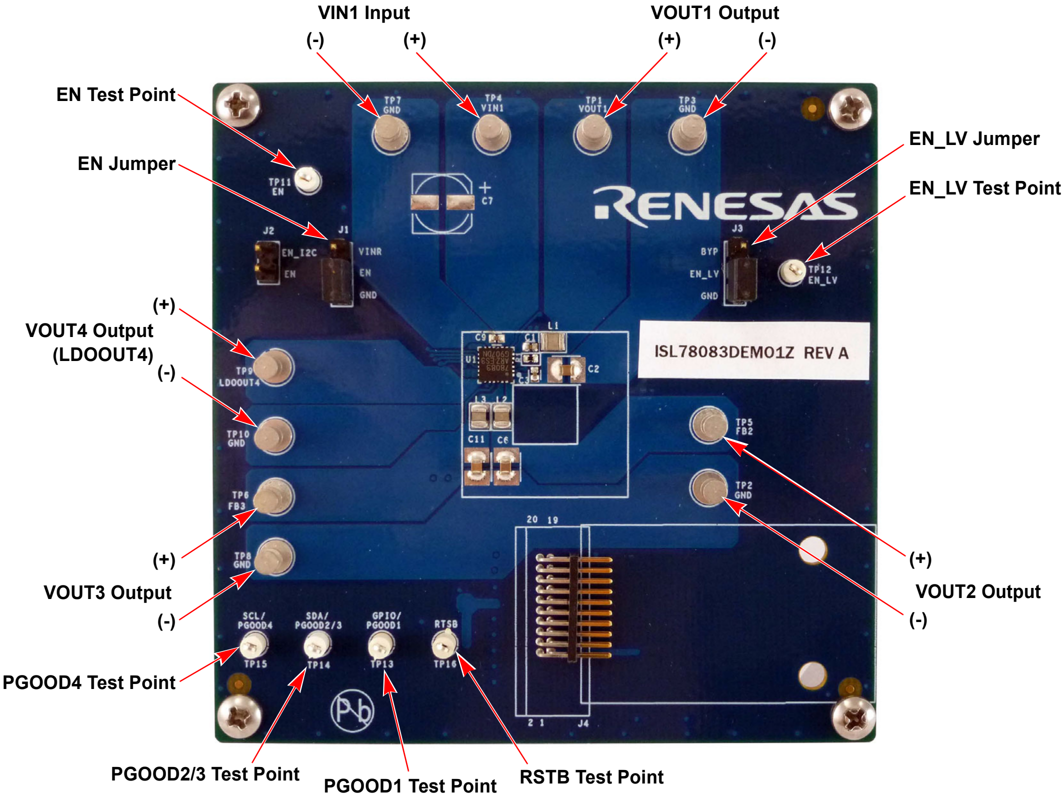

Figure 2. Demonstration Board Connection Guideline

2. PCB Layout Guidelines

2.1 ISL78083DEMO1Z Demonstration Board

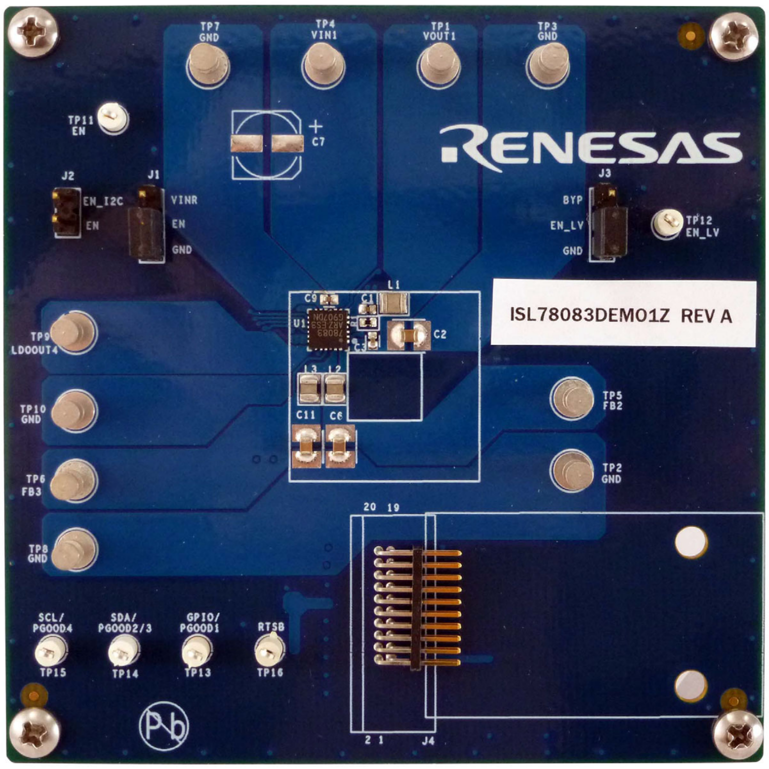

Figure 3. Top of Board

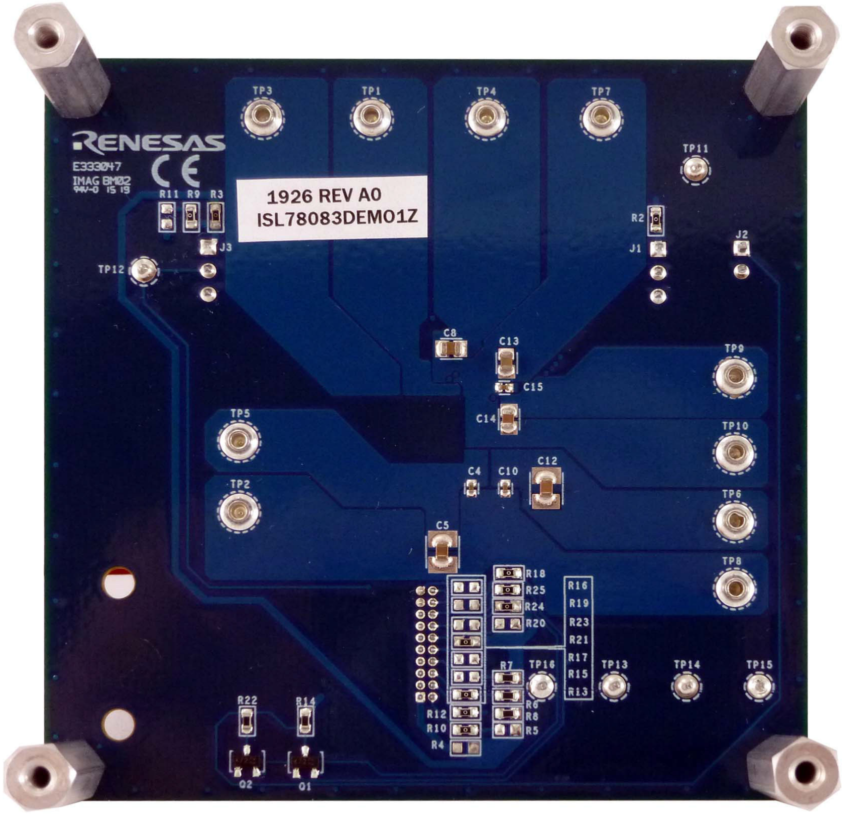

Figure 4. Bottom of Board

2.2 Layout Guidelines

As with all switching regulators, the PCB layout requires careful attention to achieve good performance. Proper PCB layout minimizes the effects of voltage and current spikes which are inherent to fast-switching MOSFET circuits. See the ISL78083 datasheet for more information. The following are layout considerations:

- The PCB should have a minimum of four copper layers. Use a full ground plane in the internal layer directly below the top layer. For all components that connect to ground, make sure that each component has one or more vias nearby, to provide a low-impedance path to the ground plane.
- VIN1 input capacitance: Place the input filter capacitors between VIN1 and PGND, as close to the IC pins as possible. Place the high-frequency decoupling capacitor closest to the IC. The loop formed by the input capacitors, VIN1, and PGND must be small to minimize high frequency noise. The copper traces between the capacitors and the IC should be as short and direct as possible.
- Place the Buck1 inductor near the PHASE1 pin of the IC and connect directly to the pin with short, wide copper.
- Place the boot capacitor next to Pins 5 and 6 and use short, direct copper connections.
- Place the VIN2/3 input capacitors near the VIN2/3 pin (Pin 1). Place the high-frequency decoupling capacitor closest to the IC. Connect the capacitors to the VIN2/3 pin using short, wide copper. Place multiple ground vias at the ground connection of each capacitor, to provide a low-impedance ground path to the IC (PGND2/3, Pin 22).
- Place the Buck2 and Buck3 inductors next to their respective pins, PHASE2 and PHASE3. Route to the inductors using short, wide copper.
- Place the Buck2 and Buck3 output capacitors near the inductors and connect using short, wide traces. Use multiple vias and copper on other layers if needed to connect from the output capacitors to their load circuits.
- Place multiple ground vias at the ground connection of the Buck2 and Buck3 output capacitors, to provide a low-impedance ground path to the Buck2/3 ground return at the IC (PGND2/3, Pin 22).
- Route the feedback for Buck3 directly from the Buck3 output capacitor to the FB3 pin (Pin 21). Provide some space clearance between the FB3 trace (which is noise-sensitive) and the high-noise PHASE3 trace.
- Route the feedback for Buck2 on an inner layer, connecting from the Buck2 output capacitor to FB2 (Pin 22). FB2 is a noise-sensitive input. Route the trace so that it avoids passing underneath the inductors L_2, L_3, or L_1, and also avoids passing underneath under the PHASE signals or pins. Renesas recommends routing the trace on an inner layer, routing away from the IC to avoid routing under the Buck2 and Buck3 inductors, and then routing to Pin 22.
- LDOIN4 and FB1 (Pins 18 and 17) must be connected to VOUT1, which is the output of Buck1 and is also connected to the VIN2/3 pin (Pin 1). Use wide copper to route from VOUT1 to LDOIN4. The LDOIN4 pin is the input for the LDOOUT4 output, which dictates that the LDOIN4 trace must carry all the LDO load current. When routing the connection from VOUT1 to LDOIN4, avoid routing underneath any of the inductors and also any PHASE nodes. Renesas recommends using inner layer copper, connecting from VOUT1 to LDOIN4, routing directly underneath the IC, while avoiding the PHASE and BOOT pins of the IC (Pins 5, 6, 23, 24). **Note:** The LDOIN4 pin also functions as the overvoltage and undervoltage sense point for Buck1. To minimize I•R voltage drop due to copper resistance, use a wide trace to route to LDOIN4.
- FB1 (Pin 17) is the feedback input for Buck1. This pin connects to the same net as LDOIN4. It is possible to combine the path for FB1 and LDOIN4 into a single trace, however the trace needs to be wide to minimize I•R voltage drop due to the LDOIN4 loading. Alternatively, a separate trace on an inner layer can route from the V_{OUT1} output to the FB1 pin. Route this trace away from all high-noise nodes and components, including the inductors, input capacitors, and the PHASE and BOOT nodes.
- Place input and output capacitors for the LDO near the IC and routed directly with short wide traces. Place multiple ground vias at the ground connection of the capacitors to provide a low-impedance ground path to the ground return at the IC.

- Connect all the grounds pins (Pins 10, 11, and 22) and the thermal PAD (Pin 25) together using a single wide copper pad under the IC. Connect this copper pad to the ground plane using multiple vias, to provide a low-impedance path to the ground plane and also to provide heatsinking through the PCB copper.

Place the BYP capacitor very near the BYP pin (Pin 12). Route to the capacitor using a short, wide PCB trace, for both the BYP and the ground paths. If needed, place multiple ground vias at the ground connection of the BYP capacitor to provide a low-impedance ground path to the ground of the IC (PGND2/3, Pin 22).

2.3 ISL78083DEMO1Z Schematic

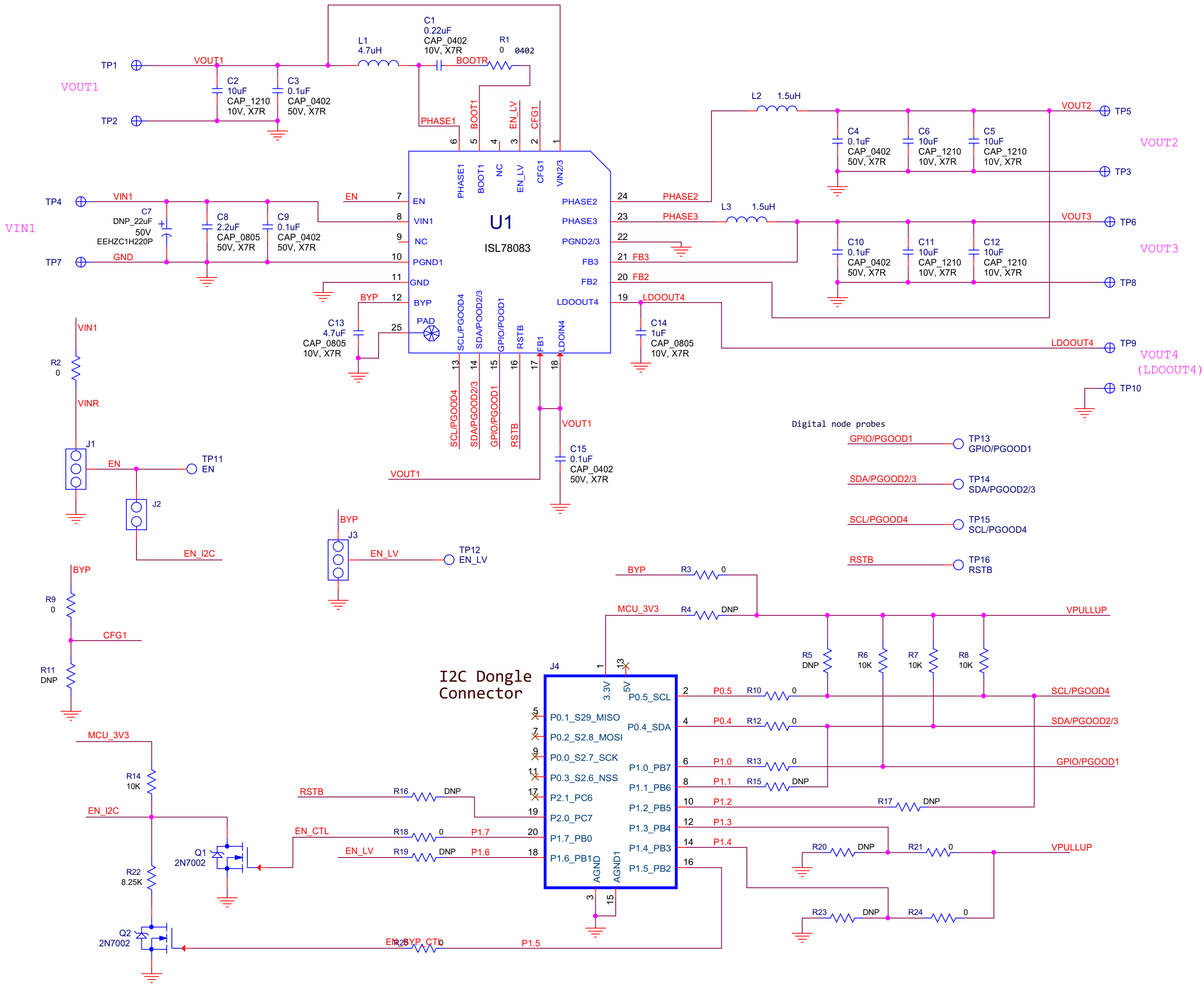

Figure 5. ISL78083DEMO1Z Board Schematic

2.4 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL78083DEMO1Z, REVA, ROHS	Imagineering Inc	ISL78083DEMO1ZREVAPCB
4	C3, C4, C10, C15	CAP-AEC-Q200, SMD, 0402, 0.1µF, 16V, 10%, X7R, ROHS	Murata	GCM155R71C104KA55D
1	C1	CAP-AEC-Q200, SMD, 0402, 0.22µF, 16V, 10%, X7R, ROHS	Murata	GCM155R71C224KE02D
1	C9	CAP-AEC-Q200, SMD, 0402, 0.1µF, 50V, 10%, X7R, ROHS	Murata	GCM155R71H104KE02D
5	C2, C5, C6, C11, C12	CAP-AEC-Q200, SMD, 0805, 10µF, 10V, 10%, X7R, ROHS	Murata	GCM21BR71A106KE22K
1	C14	CAP, SMD, 0805, 1.0µF, 50V, 10%, X7R, ROHS	Murata	GRM21BR71H105KA12L
1	C8	CAP, SMD, 0805, 2.2µF, 50V, 10%, X7R, ROHS	TDK	C2012X7R1H225K125AC
1	C13	CAP, SMD, 0805, 4.7µF, 16V, 10%, X7R, ROHS	Murata	GCJ21BR71C475KA01L
2	L2, L3	COIL-INDUCTOR, AEC-Q200, SMD, 2x1.6mm, 1.5µH, 20%, 2.3A, ROHS	TDK	TFM201610ALMA1R5MTAA
1	L1	COIL-INDUCTOR, AEC-Q200, SMD, 2.5x2mm, 4.7µH, 20%, 1.6A, ROHS	TDK	TFM252012ALMA4R7MTAA
10	TP1-TP10	CONN-TURRET, TERMINAL POST, TH, ROHS	Keystone	1514-2
6	TP11, TP12, TP13, TP14, TP15, TP16	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	Keystone	5002
2	J1, J3	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	Berg/FCI	68000-236HLF
1	J2	CONN-HEADER, 1x2, RETENTIVE, 2.54mm, 0.230x0.120, ROHS	Berg/FCI	69190-202HLF
1	J4	CONN-HEADER, TH, 2x10, 1.27mm PITCH, R/A, ROHS	Harwin Inc	M50-3901042
1	U1	IC-BUCK REGULATOR, LDO, 24P, QFN, 4x4, ROHS	Renesas Electronics America	ISL78083ARZ
2	Q1, Q2	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	Diodes, Inc.	2N7002-7-F
1	R1	RES, SMD, 0402, 0Ω, 1/16W, 5%, TF, ROHS	Venkel	CR0402-16W-00T
10	R2, R3, R9, R10, R12, R13, R18, R21, R24, R25	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	Venkel	CR0603-10W-000T
4	R6, R7, R8, R14	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
1	R22	RES, SMD, 0603, 8.25kΩ, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF8251V
0	R4, R5, R11, R15, R16, R17, R19, R20, R23	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS		
4	Four corners	SCREW, 4-40x1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Building Fasteners	PMSSS 440 0025 PH
4	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	Keystone	2204
0	C7	DO NOT POPULATE OR PURCHASE		

2.5 Board Layout

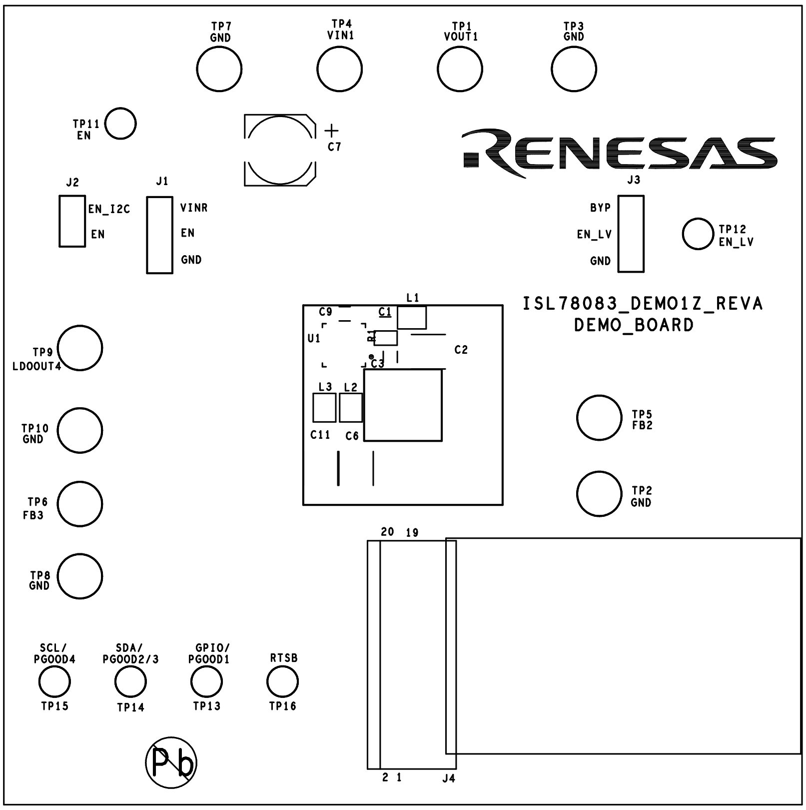

Figure 6. Top Assembly

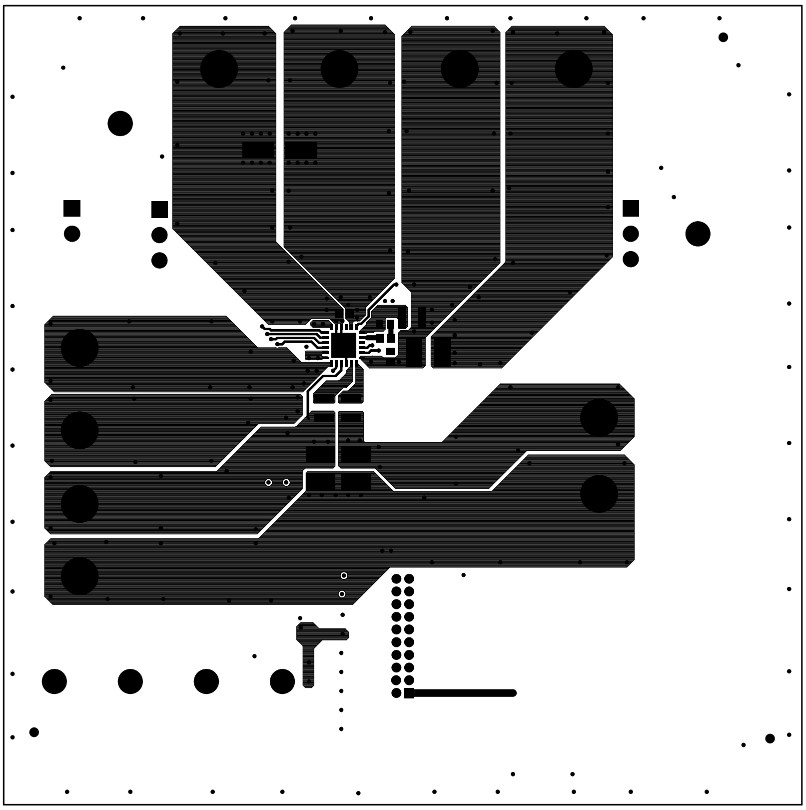

Figure 7. Top Assembly with Copper

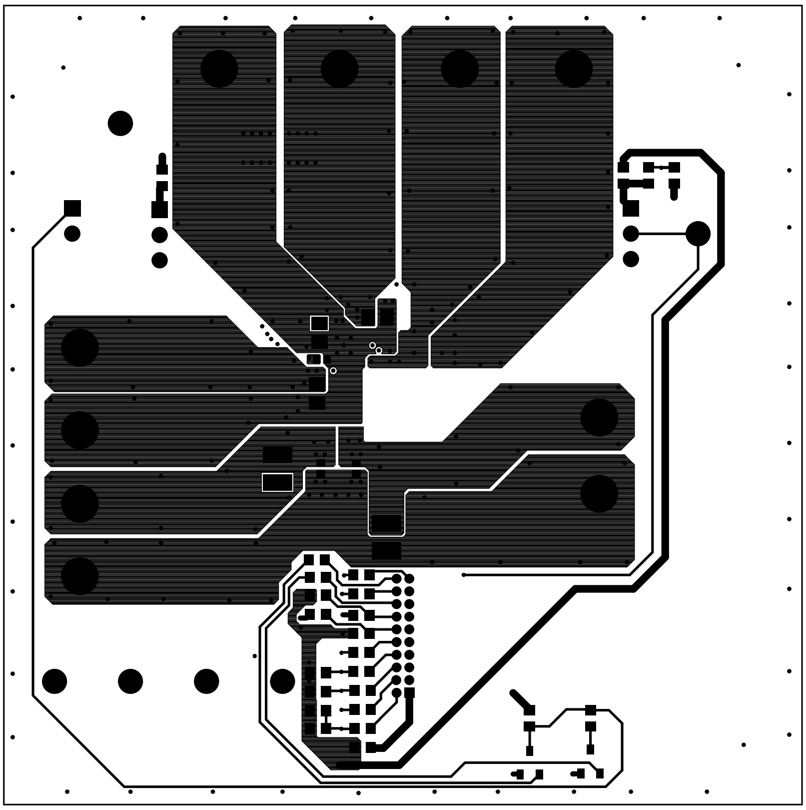

Figure 8. Bottom Assembly with Copper

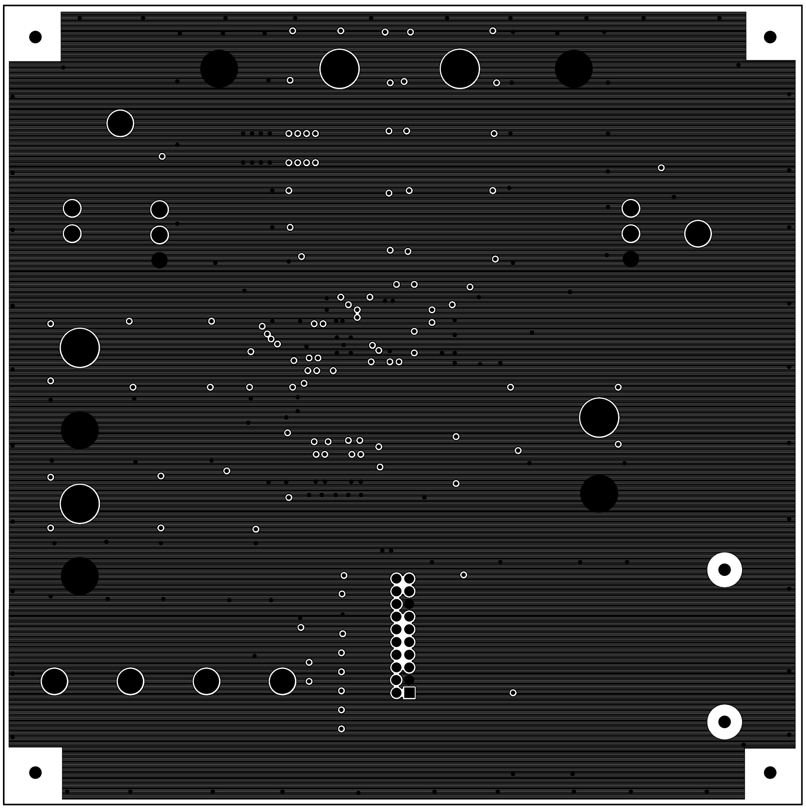

Figure 9. Layer 2 Copper

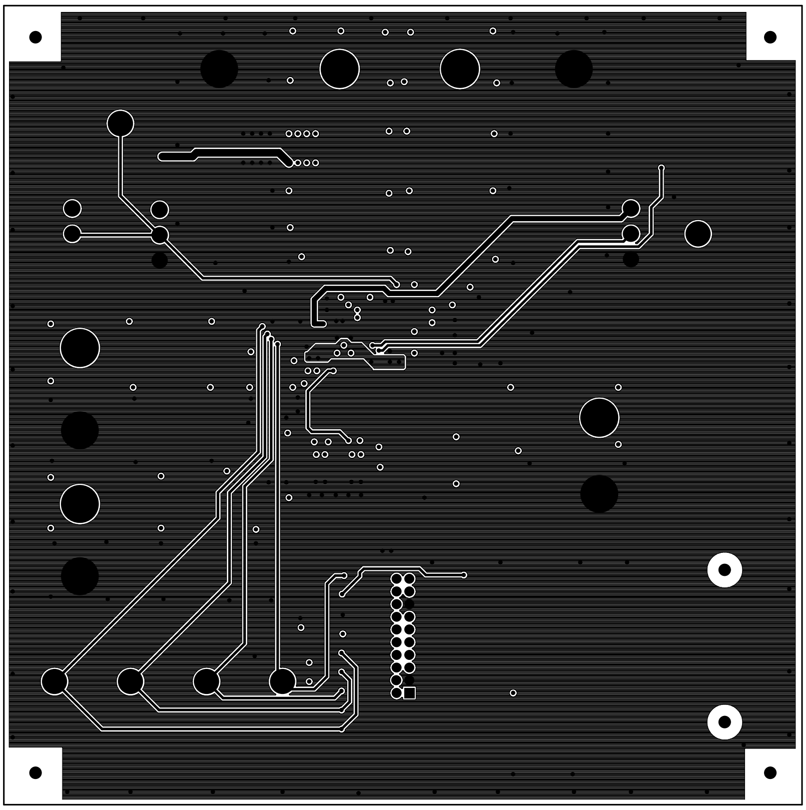

Figure 10. Layer 3 Copper

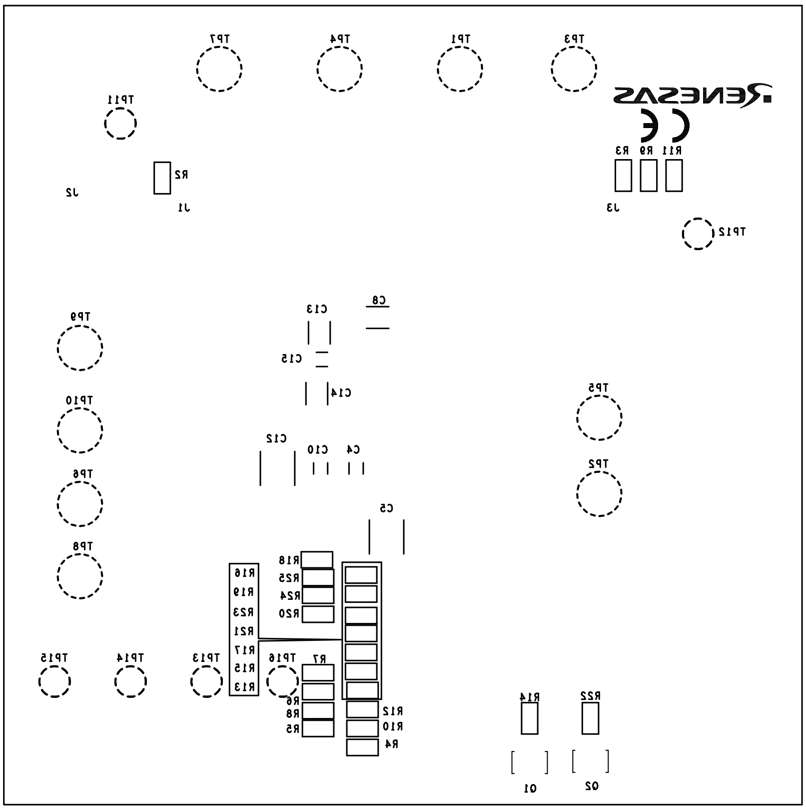

Figure 11. Bottom Assembly

3. Typical Performance

3.1 Efficiency, Input Current

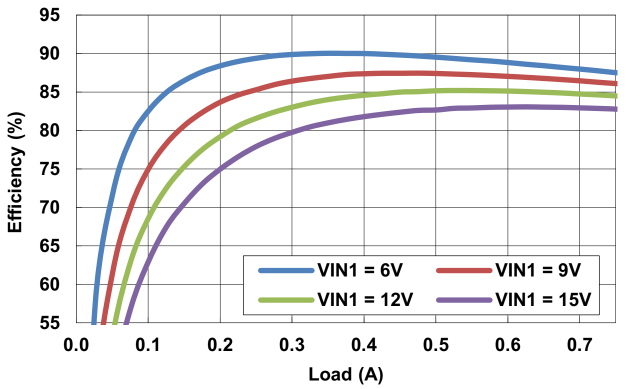

Figure 12. One-Stage Efficiency vs Load, VOUT1 = 3.8V

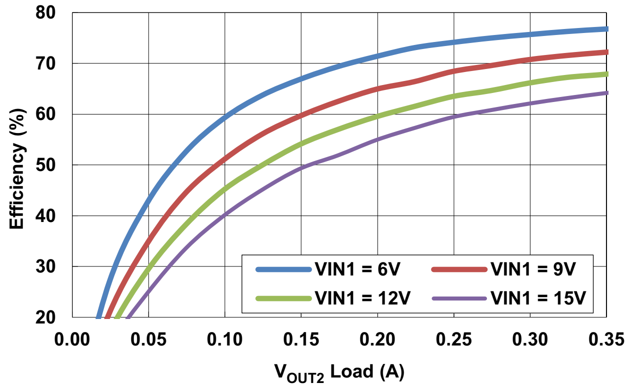

Figure 13. Two-Stage Efficiency vs Load, VOUT1 = 3.8V, VOUT2 = 1.8V

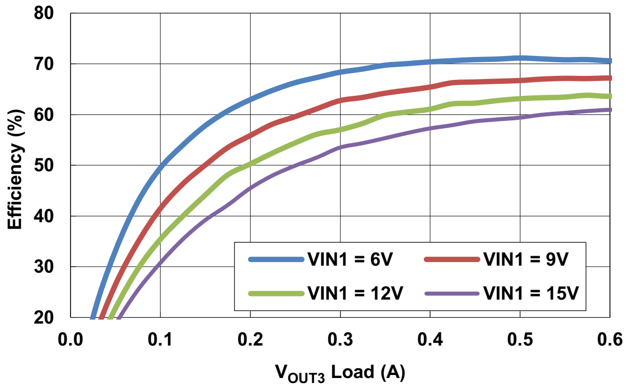

Figure 14. Two-Stage Efficiency vs Load, VOUT1 = 3.8V, VOUT3 = 1.2V

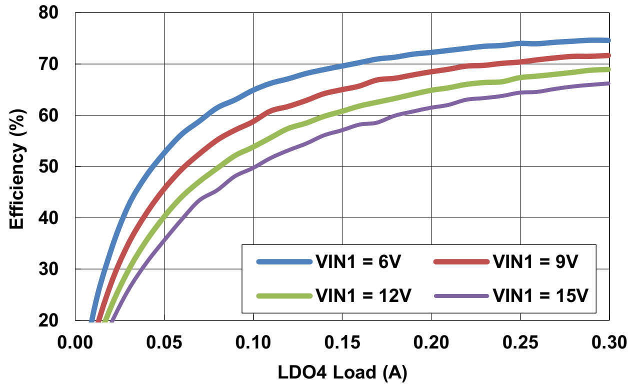

Figure 15. Two-Stage Efficiency vs Load, VOUT1 = 3.8V, LDO4 = 3.3V

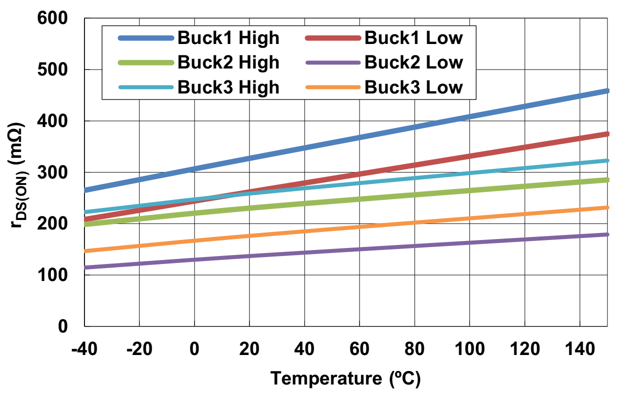

Figure 16. $r_{DS(ON)}$ vs Temperature, V_{IN1} = 12V, VOUT1 = 38V

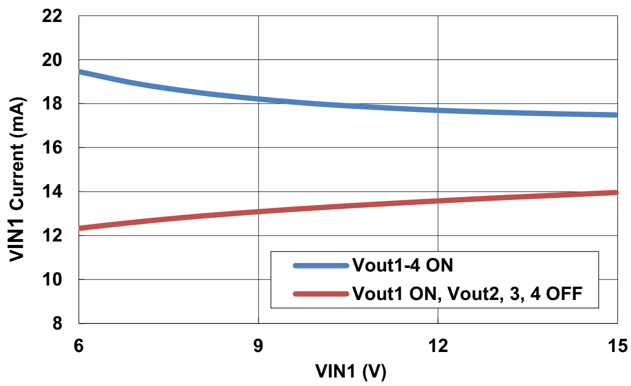

Figure 17. VIN1 Operating Current, No Load, External Pull-Up Supply for PGOOD1, 2/3, 4

3.2 Load Regulation

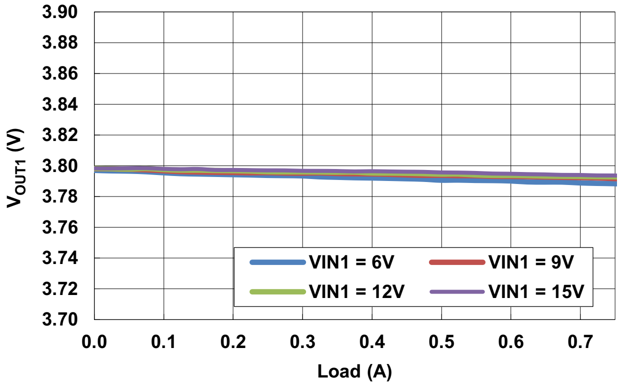

Figure 18. VOUT1 Load Regulation

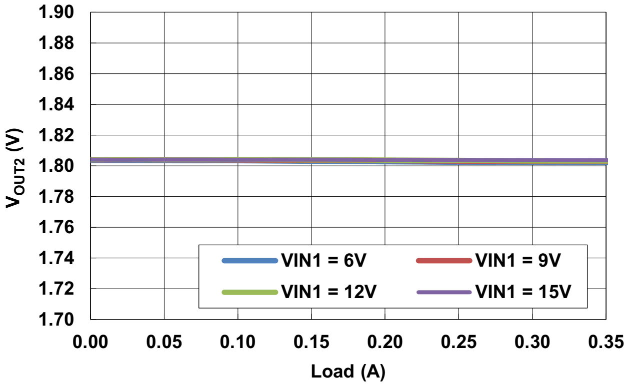

Figure 19. VOUT2 Load Regulation

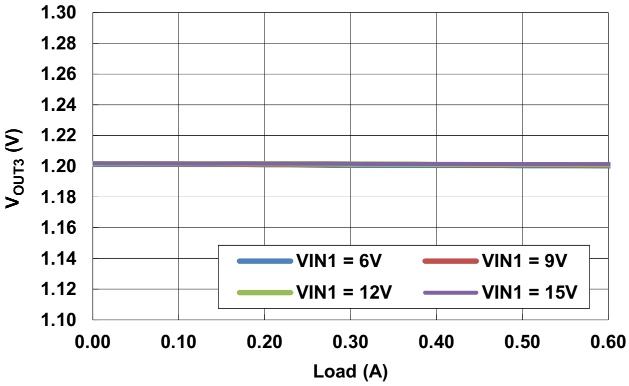

Figure 20. VOUT3 Load Regulation

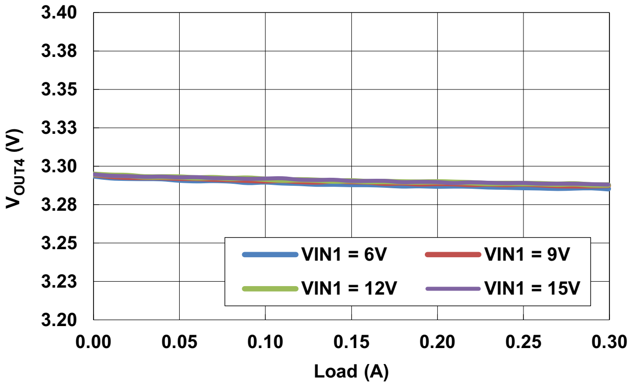

Figure 21. VOUT4 Load Regulation

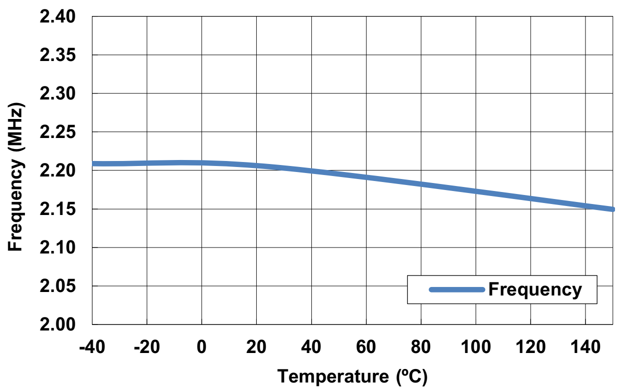

Figure 22. Frequency vs Temperature

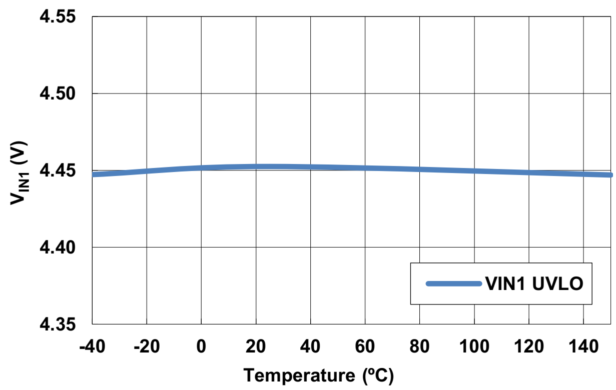

Figure 23. VIN1 UVLO Rising Edge vs Temperature

4. Revision History

Rev.	Date	Description
1.00	Nov.21.19	Initial release

Corporate Headquarters

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