

# ISL8215MEVAL1Z

## User's Manual: Evaluation Board

Industrial Analog and Power

## ISL8215MEVAL1Z

Evaluation Board

UG105  
Rev.0.00  
Aug 14, 2017

### 1. Overview

The ISL8215MEVAL1Z evaluation board (shown in [Figure 1](#)) features the [ISL8215M](#). The ISL8215M is a single channel synchronous step-down power supply, capable of delivering up to 15A of continuous current and optimized for high power density applications without the need for airflow or heatsink.

The ISL8215MEVAL1Z evaluation board is a 1.8inx3in 4-layer FR4 board with 2oz. copper on all layers. Operating from a single 7V to 42V wide input power rail, the ISL8215MEVAL1Z evaluation board offers adjustable output voltages down to 0.6V and efficiencies of up to 96.5%. It is based on a valley current mode PWM control scheme with  $V_{IN}$  feed forward, which provides a fast transient response and excellent loop stability. The ISL8215MEVAL1Z evaluation board is designed to program switching frequencies up to 2MHz, with the additional option of synchronizing to an external clock through the SYNC pin. A selectable Pulse Skipping Mode (PSM) with Diode Emulation Mode (DEM) can be enabled easily to improve light-load efficiency for battery-related applications. The evaluation board also features output voltage tracking which can be implemented through the SS/TRK pin.

By default, the board is set to a 3.3V output voltage with a 300kHz switching frequency.

#### 1.1 Key Features

- Wide input voltage range from 7V to 42V
- Adjustable output voltage from 0.6V to 12V with  $\pm 1.5\%$  accuracy over line, load, and temperature
- Up to 96.5% conversion efficiency
- High light-load efficiency with pulse skipping DEM operation
- Programmable soft-start with output voltage tracking
- Prebias output start-up
- External frequency synchronization up to 1MHz
- Dedicated enable pin and PGOOD indicator
- UVLO, programmable overcurrent, overvoltage, and over-temperature
- Thermally enhanced 19mmx13mmx5.3mm HDA package

#### 1.2 Specifications

The evaluation board has been configured and optimized for the following operating conditions:

- $V_{IN} = 7V$  to 42V
- $V_{OUT} = 3.3V$
- $I_{OUT-MAX} = 15A$
- $f_{SW} = 300kHz$
- Set to PWM mode by default

#### 1.3 Ordering Information

Part Number	Description
ISL8215MEVAL1Z	ISL8215M single 15A power module evaluation board

## 1.4 Related Literature

- For a full list of related documents, visit our website
- [ISL8215M](#) product page

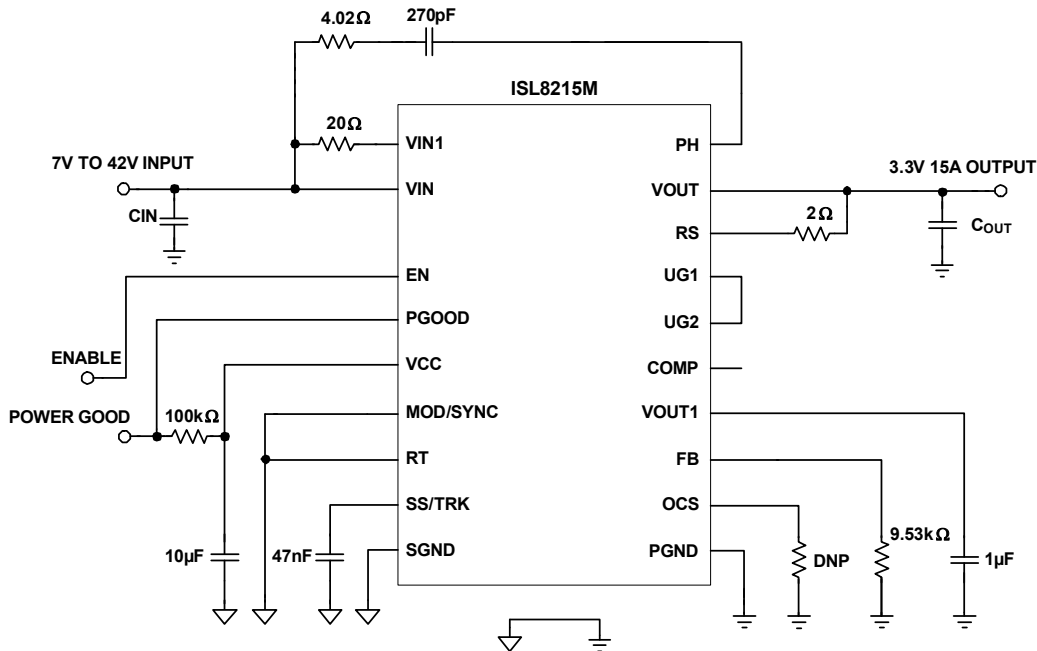


Figure 1. ISL8215MEVAL1Z Block Diagram

## 1.5 Recommended Testing Equipment

- 0V to 42V power supply with at least 12A source current capability
- Electronic loads capable of sinking current up to 15A
- Digital Multimeters (DMMs)
- Oscilloscope with higher than 100MHz bandwidth

## 2. Functional Description

The ISL8215MEVAL1Z provides the peripheral circuitry to evaluate the feature set of the ISL8215M. The evaluation board is designed with mechanical switches for ENABLE, several connectors, test points, and jumpers, which makes validation of the module easy. The converter can be enabled and disabled by toggling the ENABLE switch as shown in [Figure 2 on page 6](#). Connecting a jumper across the pins as shown in [Figure 2](#) enables the PSM/DEM mode of operation, which can lead to higher efficiencies at light loads. Selecting features like external frequency synchronization can be performed by hooking the signal generator (square pulse waveform clock signal) to the MOD/SYNC pin. The output voltage (0.6V - 12V) and the switching frequency (300kHz to 2MHz) can be programmed by changing the resistors as shown in [Figure 3 on page 6](#).

### 2.1 Quick Test Guide

- (1) Disable the module by toggling the ENABLE switch as shown in [Figure 2 on page 6](#).
- (2) Use the appropriate cables to connect the DC input power supply to banana sockets J1 and J4 and the electronic load to sockets J3 and J2. Ensure that the polarity for the power leads is correct and the input voltage is within the operating range (7V - 42V) of the module. Use test points TP1 (VIN) and TP2 (PGND) for accurately measuring the input voltage.
- (3) Turn on the input power supply.
- (4) Turn the ENABLE switch to position “SW1 ENABLE” for enabling the module.
- (5) Probe test points TP3 (VOUT) and TP4 (PGND) to observe the output voltage. The output voltage should read 3.3V.
- (6) Adjust input voltage,  $V_{IN}$ , within the specified range and observe output voltage. The output voltage variation should be within  $\pm 1.5\%$ .
- (7) Adjust the load current to within the specified range (0 - 15A) and observe output voltage. The output voltage variation should be within  $\pm 1.5\%$ .
- (8) To change  $V_{OUT}$ , disconnect the evaluation board from the setup and populate a standard 0603 resistor at the  $R_2$  placeholder location on the bottom layer. The “Output Voltage Resistor Settings” table in the [ISL8215M](#) datasheet can be used as a reference for programming different output voltages. Refer to the “ISL8215M Design Guide Matrix” table in the [ISL8215M](#) datasheet for correct input and output capacitors, switching frequency, and output voltage combinations.
- (9) The switching frequency can be modified by populating a standard 0603 resistor at the  $R_{11}$  placeholder location on the bottom layer. Refer to “Equation 2” in the [ISL8215M](#) datasheet for selecting the correct value of  $R_{11}$  within admissible operating range (300kHz - 2MHz).

### 2.2 Thermal Considerations and Current Derating

Board layout is very critical so that the module can operate safely and deliver the maximum allowable power. For the board to operate properly at high ambient temperature environments and carry full load current, the board layout needs to be carefully designed to maximize thermal performance. To achieve this, use enough trace width, copper weight, and proper connectors.

The ISL8215MEVAL1Z evaluation board is capable of operating at 15A full load current at room temperature without the need for additional cooling systems. However, if the board is to operate at elevated ambient temperatures, then the available output current may need to be derated. Refer to the derated current curves in the [ISL8215M](#) datasheet to determine the maximum output current the evaluation board can supply.

### 3. PCB Layout Guidelines

The ISL8215MEVAL1Z evaluation board is a 1.8in x 3in four-layer FR-4 board with 2oz. copper on all the layers. The board can be used as a single 15A reference design. Refer to [Figures 15](#) through [20](#) for board layout information.

The ISL8215MEVAL1Z board layout has been optimized for electrical performance, low loss, and good thermal performance. Similar performance can be obtained for designs involving ISL8215M, while adhering to the following layout design tips:

#### 3.1 Layout Considerations

- (1) The input capacitors and high frequency decoupling ceramic capacitors are placed between VIN and PGND, as close to the module as possible. The loop formed by the input capacitor, VIN pad, and PGND is kept as small as possible, to minimize the high frequency noise. The output capacitors are placed closer towards the load. Short, wide copper planes are used to connect the output capacitors to the load for avoiding any parasitic inductances and resistances.
- (2) Large copper planes are used for VIN, VOUT, and PGND to minimize conduction loss and thermal stress. Multiple vias are used to connect the power planes in different layers.
- (3) Ground planes are used in the internal layers (Layer 2 and Layer 3) with shared SGND and PGND to simplify the layout design. The controller SGND has a solid connection to the PGND through multiple vias. The bottom layer is used to route EN and VCC signals. PGOOD is routed on the top layer.
- (4) For achieving a tight output voltage regulation, the V<sub>OUT+</sub> point is connected to the Remote Sense (RS) pin by routing the trace through inner Layer 3. A 2Ω resistor is placed close to the RS pin for damping the noise on the traces.
- (5) To avoid ground bouncing issues, place the V<sub>IN</sub> return and the V<sub>OUT</sub> return diagonally opposite to each other. This ensures that the switching noise generated by the power-train will have a minimal effect on the controller operation.
- (6) Because the phase nodes are subjected to very high dv/dt voltages, the parasitic capacitor formed between these islands and the surrounding circuitry will tend to couple the switching noise. The PHASE node is placed in Layer 3 and the bottom layer of the PCB to minimize its impact on the operation of the controller. The sensitive signal traces (EN, VCC, and PGOOD) are routed away from the PHASE node plane to minimize noise coupling.
- (7) The VCC bypass capacitor is placed underneath the VCC pin, and its ground is connected to the PGND pad. The low-side feedback resistor, R<sub>2</sub>, and the decoupling capacitor, C<sub>25</sub>, are connected to the SGND pad through multiple vias.
- (8) For a switching frequency of 300kHz, a 4.02Ω 1206 resistor and a 270pF 100V X7R 0603 capacitor in series from PH to VIN is required. De-rate the resistor size for switching frequencies higher than 300kHz. Calculate the power dissipated in resistor (P<sub>cal</sub>) by using the formula  $C \cdot V^2 \cdot f$ , where,
  - C = 270pF
  - V = Input voltage
  - f = Frequency of operation.

For derating purposes, the nominal power handling capability of the resistor package size should be at least P<sub>cal</sub>/0.65. The 65% derating is derived by looking at the resistor operation at +100°C ambient temperature. Use a standard thick film chip resistor datasheet to find the correct resistor package size for different switching frequencies and input voltage.



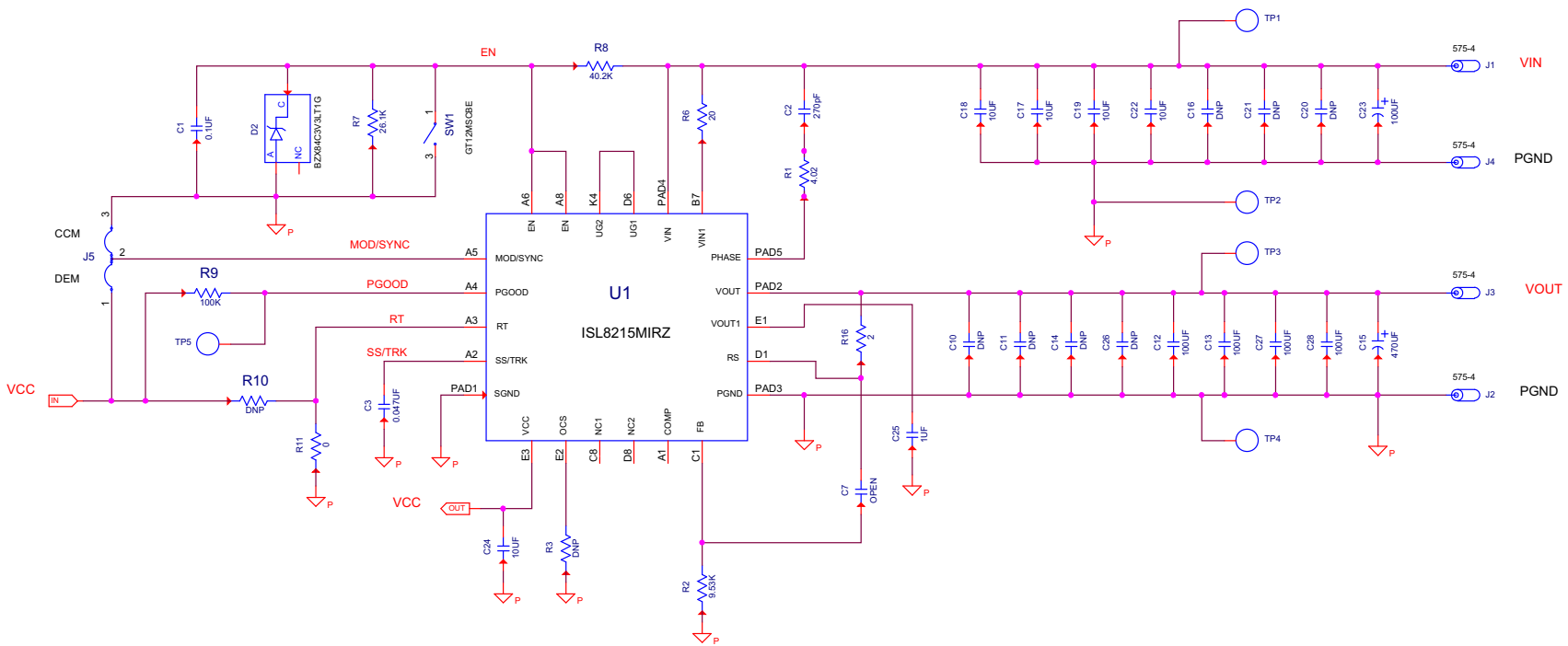


Figure 4. Schematic

### 3.2 ISL8215MEVAL1Z Schematic

### 3.3 Typical Evaluation Board Performance Curves

The following data was acquired using the ISL8215MEVAL1Z evaluation board at +25°C ambient and free air 0LFM.

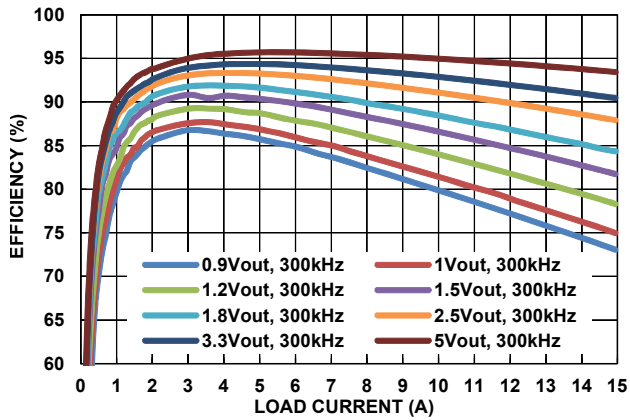


Figure 5. Efficiency vs Load Current at  $V_{IN} = 12V$ , CCM Mode

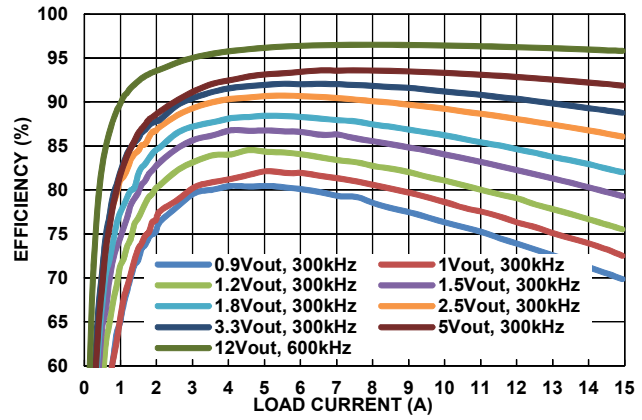


Figure 6. Efficiency vs Load Current at  $V_{IN} = 24V$ , CCM Mode

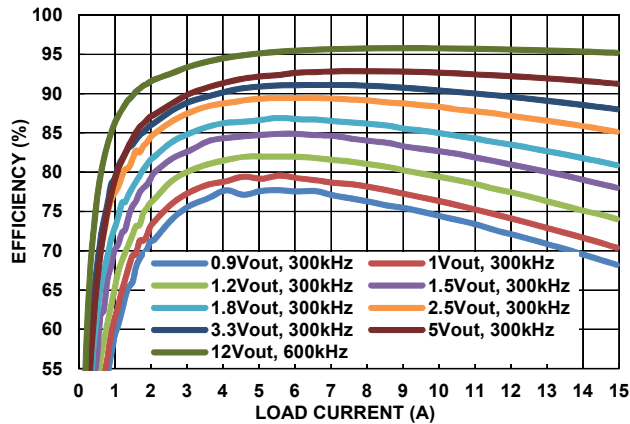


Figure 7. Efficiency vs Load Current at  $V_{IN} = 30V$ , CCM Mode

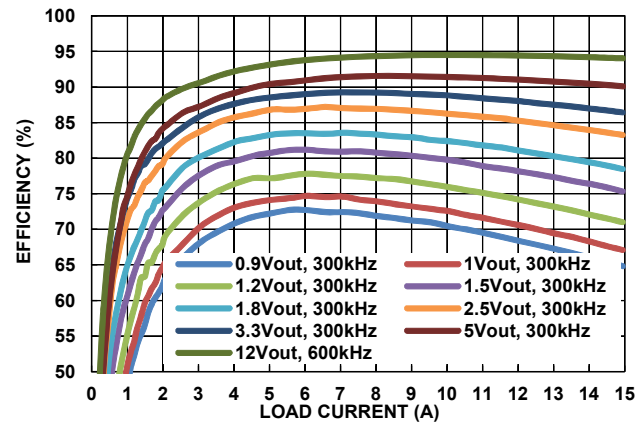


Figure 8. Efficiency vs Load Current at  $V_{IN} = 42V$ , CCM Mode

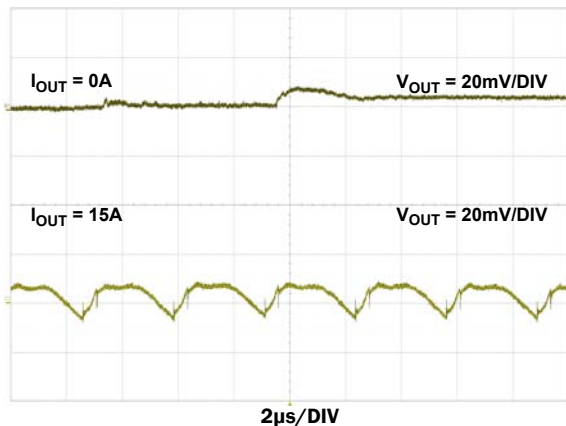


Figure 9. Output Ripple,  $V_{IN} = 24V$ ,  $V_{OUT} = 3.3V$ , PSM/DEM Mode,  $C_{OUT} = 4 \times 100\mu F$  Ceramic +  $1 \times 470\mu F$  POSCAP

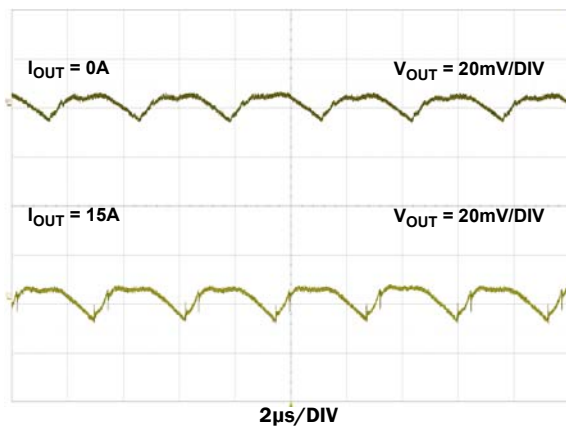


Figure 10. Output Ripple,  $V_{IN} = 24V$ ,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 300kHz$ , CCM Mode,  $C_{OUT} = 4 \times 100\mu F$  Ceramic +  $1 \times 470\mu F$  POSCAP



### 3.4 Typical Evaluation Board Performance Data

Operating condition:  $V_{IN} = 24V$ ,  $f_{SW} = 300kHz$ , CCM Mode, unless otherwise noted.

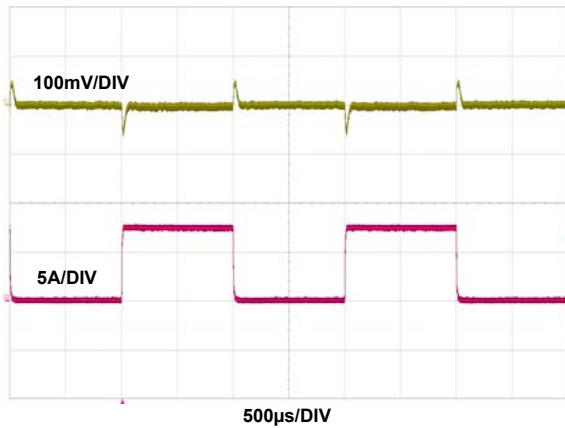


Figure 11. Transient Response,  $V_{OUT} = 3.3V$ , 0A to 7.5A, 2.5A/ $\mu s$  Step Load,  $C_{OUT} = 4 \times 100\mu F$  Ceramic + 1x470 $\mu F$  POSCAP

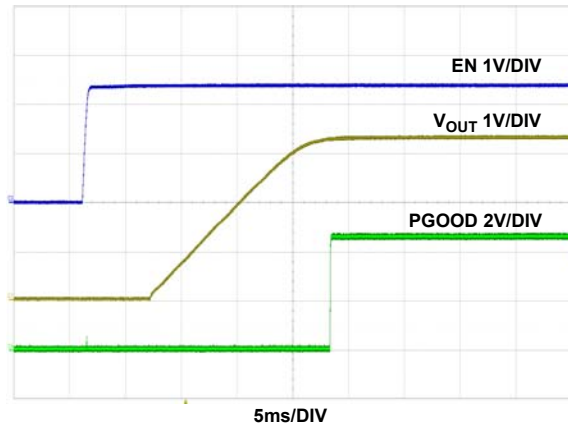


Figure 12. Start-Up Waveform,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 15A$ ,  $C_{OUT} = 4 \times 100\mu F$  Ceramic + 1x470 $\mu F$  POSCAP

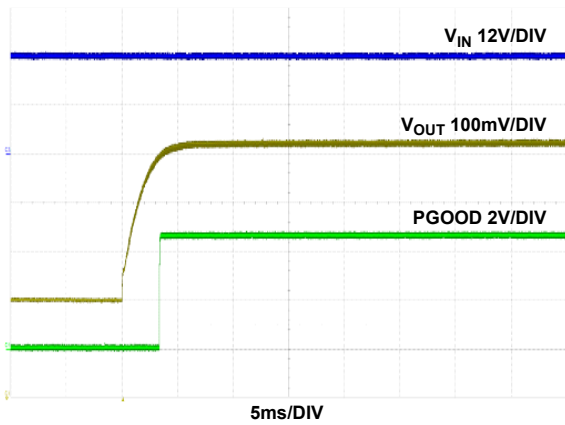


Figure 13. Prebiased Power-Up Waveform, Prebiased Voltage = 3.0V,  $V_{OUT} = 3.3V$ ,  $I_{OUT} =$  No Load,  $C_{OUT} = 4 \times 100\mu F$  Ceramic + 1x470 $\mu F$  POSCAP

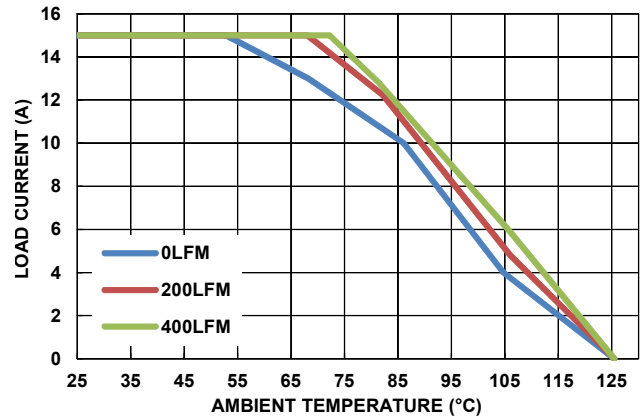


Figure 14. Derating Curve,  $V_{OUT} = 3.3V$ ,  $C_{OUT} = 4 \times 100\mu F$  Ceramic + 1x470 $\mu F$  POSCAP

### 3.5 Bill of Materials

Reference Designators	Qty	Value	Tol.	Voltage	Power	Package Type	Manufacturer	Part Number	Description
C15	1	470 $\mu$ F	$\pm$ 20%	6.3V		2917	Panasonic	6TPF470MAH	POSCAP
C12, C13, C27, C28	4	100 $\mu$ F	$\pm$ 20%	10V		1210	Murata	LMK325BJ107MM-T	Ceramic Capacitor
C10, C11, C14, C26	4	OPEN	$\pm$ 20%	10V		1210	Murata	LMK325BJ107MM-T	Ceramic Capacitor
C17, C18, C19, C22	4	10 $\mu$ F	$\pm$ 10 %	50V		1210	Murata	GRM32ER71H106KA12L-T	Ceramic Capacitor
C16, C20, C21	3	OPEN	$\pm$ 10 %	50V		1210	Murata	GRM32ER71H106KA12L-T	Ceramic Capacitor
C23	1	100 $\mu$ F	$\pm$ 20%	50V		Radial, Can - SMD	United Chemi-Con	EMZA500ADA101MHA0G	Aluminum Electrolytic Capacitor
C3	1	0.047 $\mu$ F	$\pm$ 5%	25V		0402	Kemet	C0402C473J3RAC7867	Multilayer Capacitor
C25	1	1.0 $\mu$ F	$\pm$ 10%	25V		0603	Murata	GRM188R71E105KA12D	Ceramic Chip Capacitor
C7	1	OPEN	$\pm$ 10%	25V		0402	Generic		Multilayer Capacitor
C1	1	0.1 $\mu$ F	$\pm$ 10%	25V		0603	Murata	GRM188R71E104KA01D	Ceramic Capacitor
C2 <a href="#">(Note 1)</a>	1	270pF	$\pm$ 10%	100V		0603	Murata	GRM188R72A271KA01D	Ceramic Capacitor
C24	1	10 $\mu$ F	$\pm$ 10%	25V		0805	TDK	C2012X5R1E106K	Multilayer Capacitor
J1-J4	4					CONN-JACK	Keystone	575-4	Solder Mount Banana Jack
TP1-TP5	5					CONN-MINI TEST POINT	Keystone	5002	Miniature PC Test Point
J5	1					CONN-HEADER	FCI/Amphenol	68000-236HLF	Three Pin Jumper
SW1	1					SMD	C&K Componenets	GT12MSCBE	SPDT ON/OFF Toggle Switch
D2	1		$\pm$ 6%	3.3V	225mW	SOT-23-3	On-Semi	BZX84C3V3LT1G	Zener Diodes
U1	1					19X13 HDA	Intersil	ISL8215MIRZ	IC-42V 15A Step-Down Power Module
R1 <a href="#">(Note 1)</a>	1	4.02 $\Omega$	$\pm$ 1%		1/4W	1206	Yageo	RC1206FR-074R02L	Chip Resistor
R2	1	9.53k $\Omega$	$\pm$ 1%		1/10W	0603	Venkel	CR0603-10W-9531FT	Thick Film Chip Resistor

Reference Designators	Qty	Value	Tol.	Voltage	Power	Package Type	Manufacturer	Part Number	Description
R10	1	DNP	±1%		1/10W	0603			Metal Film Chip Resistor
R3	1	475kΩ	±1%		1/16W	0402	Yageo	RC0402FR-07475KL	Chip Resistor
R6	1	20Ω	±1%		1/10W	0603	Panasonic	ERJ-3EKF20R0V	Chip Resistor
R11	1	0Ω			1/10W	0603	Venkel	CR0603-10W-000T	Chip Resistor
R9	1	100kΩ	±1%		1/10W	0603	Venkel	CR0603-10W-1003FT	Chip Resistor
R7	1	26.1kΩ	±1%		1/10W	0603	Yageo	9C06031A2612FKHFT	Chip Resistor
R8	1	40.2kΩ	±1%		1/10W	0603	Yageo	RC0603FR-0740K2L	Chip Resistor
R16	1	2Ω	±1%		1/16W	0402	Venkel	CR0402-16W-02R0FT	Chip Resistor

## Note:

1. R1 and C2 do not have a reference designator or footprint on the evaluation board. The resistor and capacitor are soldered on the bottom of the PCB.

### 3.6 ISL8215MEVAL1Z PCB Layout

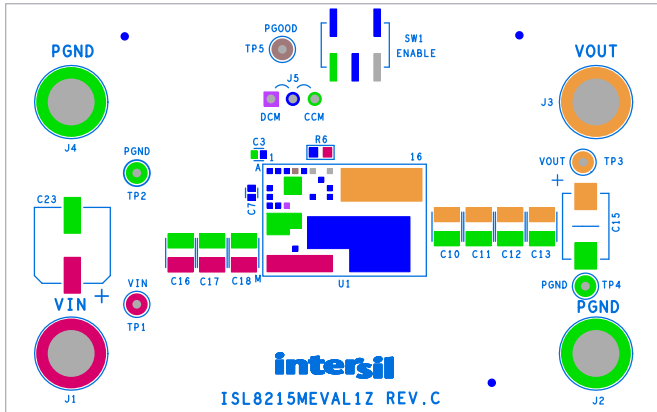


Figure 15. Silkscreen Top

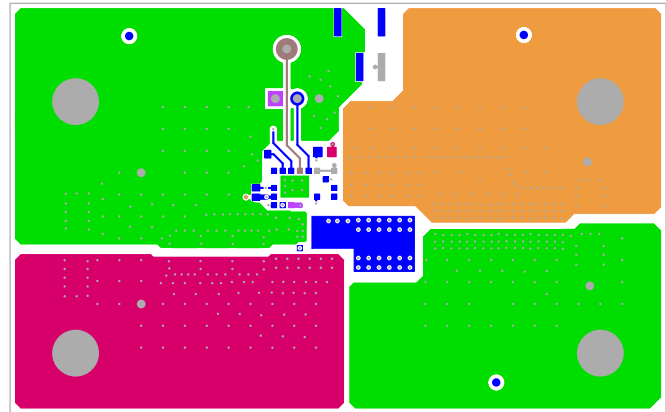


Figure 16. Top Layer Component Side

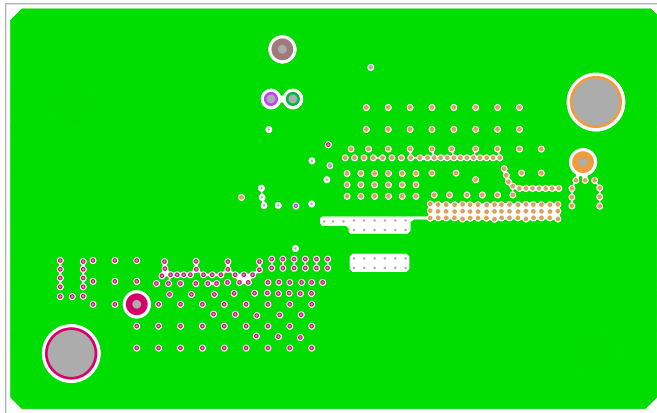


Figure 17. Inner Layer 2

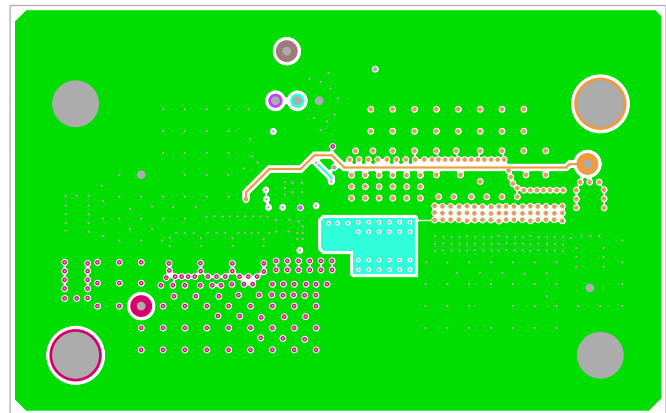


Figure 18. Inner Layer 3

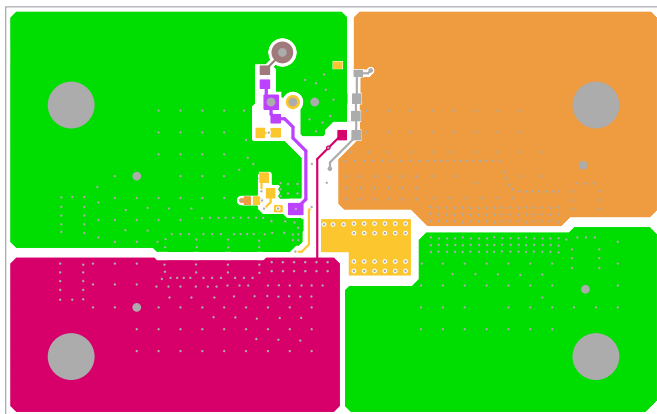


Figure 19. Bottom Layer Solder Side

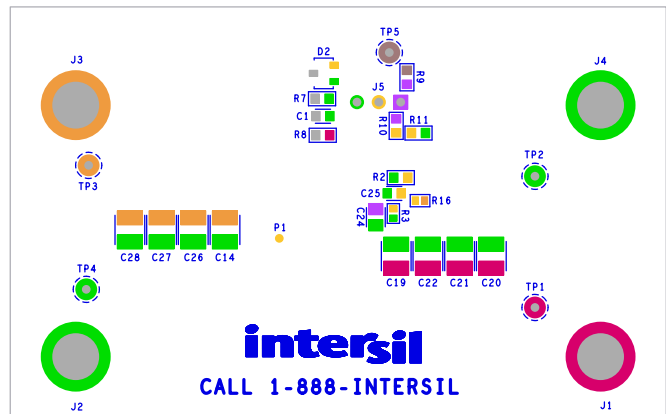


Figure 20. Silkscreen Bottom

## 4. Revision History

Rev.	Date	Description
0.00	Aug 14, 2017	Initial release

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