User's Manual

ISL8282MEVAL1Z

User's Manual: Evaluation Board

Industrial Analog and Power

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1. Overview

The ISL8282MEVAL1Z evaluation board (shown in Figures 4 and 5) is designed for evaluating the ISL8282M. The ISL8282M is a single channel step-down, synchronous DC/DC power supply module that is capable of delivering up to 15A of continuous current. The proprietary Renesas R4 Technology control scheme has extremely fast transient performance, accurately regulated frequency control, and all internal compensation. The ISL8282M includes an SMBus/PMBus/I^2C interface for module configuration, telemetry (V_{IN}, V_{OUT}, I_{OUT}, and temperature) and fault reporting, and allows for easy R4 loop optimization that results in fast transient performance across a wide range of applications, which includes all ceramic output filters. The ISL8282M integrates the controller, all power components, and most passive components. The device requires only a few external components to operate, which significantly reduces design complexity and board space, and it optimizes for high power density applications without the need for airflow or a heatsink.

The ISL8282MEVAL1Z evaluation board is a 3x3.4 inch six-layer FR4 board with 2oz. copper on all layers. The ISL8282MEVAL1Z operates from a single 4.5V to 15V wide input power rail and offers adjustable output voltages down to 0.5V and efficiencies of up to 95%. The ISL8282MEVAL1Z comes with placeholders for pin-strap resistors to program output voltage, PFM/PWM mode, temperature compensation (TCOMP), PMBus address, switching frequency (f_{SW}), AV gain, OCP retry/latchoff, ultrasonic PFM enable, soft-start ramp rate, RR impedance, and AV gain multiplier (1x or 2x).

The ISL8282MEVALZ ships with the ZLUSBEVAL3Z (USB to PMBus adapter), which connects the evaluation board to a PC to activate the PMBus communication interface. The PMBus command set is accessed by using the Renesas PowerNavigator™ evaluation software from a PC running Microsoft Windows. The ISL8282MEVAL1Z can operate in Pin-Strap mode without needing the ZLUSBEVAL3Z adapter or PMBus communication.

By default, the ISL8282MEVAL1Z is set to a 1V output voltage with a 400kHz switching frequency, 49 AV gain, and 200kΩ RR.

1.1 Key Features

- Input voltage range: 4.5V to 15V, capable of delivering up to 15A of continuous current, and up to 95% conversion efficiency
- Adjustable output voltage: 0.5V to 5V with ±1.5% load/line/temperature regulation with remote sense
- Proprietary Renesas R4 Technology
- Programmable V_{OUT}, PFM/PWM mode, TCOMP, PMBus address, f_{SW}, AV gain, OCP retry/latchoff, ultrasonic PFM enable, soft-start ramp rate, RR, and AV gain multiplier
- Monitor: V_{IN}, V_{OUT}, I_{OUT}, temperature, switching frequency, duty cycle, and faults
- Startup into precharged load
- Dedicated enable pin and PGOOD indicator
- Comprehensive fault protection for high system reliability: over-temperature protection, output overcurrent and short-circuit protection, output overvoltage and undervoltage protection, open remote sense protection, input UVLO and power sequence, and fault reset
- Thermally enhanced 12mmx11mmx5.3mm HDA package
- Compatible with Renesas PowerNavigator software

1.2 Specifications

The ISL8282MEVAL1Z is configured and optimized for the following operating conditions:

- V_{IN} = 4.5V to 15V
- V_{OUT} = 1V
- $I_{OUT-MAX}$ = 15A
- f_{SW} = 400kHz
- AV gain multiplier = 2x, AV gain = 49, RR = 200kΩ
- PMBus address = 0x60h
- TCOMP = +5°C

1.3 Ordering Information

Part Number	Description
ISL8282MEVAL1Z	15A high efficiency SMBus/PMBus/I2C step-down power module evaluation board

1.4 Related Literature

For a full list of related documents, visit our website:

- ISL8282M device page

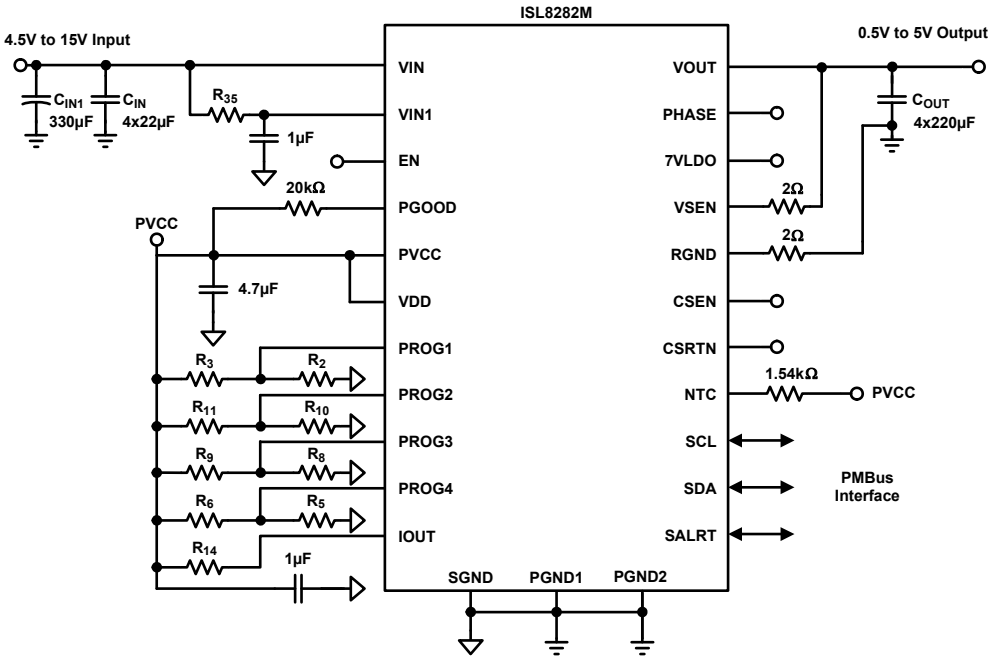

Figure 1. ISL8282MEVAL1Z Block Diagram

1.5 Recommended Testing Equipment

- DC power supply with minimum 15V/12A source current capability
- Electronic loads capable of sinking current up to 15A
- Digital Multimeters (DMMs)
- Oscilloscope with greater than 100MHz bandwidth

2. Functional Description

The ISL8282MEVAL1Z evaluation board provides the peripheral circuitry to evaluate the ISL8282M feature set. The ISL8282MEVAL1Z includes several connectors, test points, and external pin-strap resistors that simplify validation of the module. Figures 4 and 5 on page 24 show the top and bottom of the ISL8282MEVAL1Z.

2.1 Quick Start Guide

2.1.1 Pin-Strap Option

The ISL8282MEVAL1Z can be configured in Pin-Strap mode with standard 1% resistors. The PMBus interface is not required to evaluate ISL8282M in Pin-Strap mode. V_{OUT}, PFM/PWM mode, TCOMP, PMBus address, f_{SW}, AV gain, OCP retry/latchoff, ultrasonic PFM enable, soft-start ramp rate, RR, and AV gain multiplier can be changed by populating the recommended resistors at placeholders provided in the ISL8282MEVAL1Z. Complete the following steps to evaluate the ISL8282M with the Pin-Strap option.

(1) Disable the module by toggling the mechanical switch SW1 to **2-3** as shown in Figure 4.

(2) Connect the DC input power supply to the banana sockets J_4 and J_3 and the electronic load to sockets J_{14} and J_{15}. Ensure that the polarity for the power leads is correct and the input voltage is within the ISL8282MEVAL1Z's operating range of 4.5V to 15V. Use test points TP_1 (VIN) and TP_3 (GND) to accurately measure the input voltage.

(3) Toggle the mechanical switch SW_1 to **1-2** to enable the module.

(4) Turn on the DC input power supply.

(5) Probe test points TP_3 (VOUT) and TP_4 (PGND) to observe the output voltage. The output voltage should read 1V.

(6) Adjust the input voltage, V_{IN}, within the specified range and observe the output voltage. The output voltage variation should be within ±1.5%.

(7) Adjust the load current to within the specified range of 0A to 15A and observe the output voltage. The output voltage variation should be within ±1.5%.

(8) To change V_{OUT}, disconnect the ISL8282MEVAL1Z from the setup and populate 1% standard 0402 resistors at the R_2 and R_3 placeholder locations on the bottom layer. Table 1 on page 6 is a reference for programming different output voltages. See the "ISL8282M Design Guide Matrix of Typical Applications" table in the ISL8282M datasheet for typical application recommended values.

(9) To change the PFM/PWM mode, TCOMP, and PMBus address, disconnect the ISL8282MEVAL1Z from the setup and populate 1% standard 0402 resistors at the R_{10} and R_{11} placeholder locations on the bottom layer. Table 2 on page 11 is a reference for customizing module specifications. Renesas recommends using +5°C as the TCOMP.

(10) To change the OCP retry/latchoff, f_{SW}, AV gain, and ultrasonic PFM enable, disconnect the ISL8282MEVAL1Z from the setup and populate 1% standard 0402 resistors at the R_8 and R_9 placeholder locations on the bottom layer. Table 3 on page 18 is a reference for customizing module specifications. See the "ISL8282M Design Guide Matrix of Typical Applications" table in the ISL8282M datasheet for typical application recommended values.

(11) To change the soft-start ramp rate, RR, and AV gain multiplier, disconnect the ISL8282MEVAL1Z from the setup and populate 1% standard 0402 resistors at the R_5 and R_6 placeholder locations on the bottom layer. Table 4 on page 21 is a reference for customizing module specifications. See the "ISL8282M Design Guide Matrix of Typical Applications" table in the ISL8282M datasheet for typical application recommended values. Note: The AV gain multiplier (AVMLTI) can be set by external R_5 and R_6 only.

2.1.2 PMBus Option

The ISL8282MEVAL1Z can be configured using the provided ZLUSBEVAL3Z dongle and Power Navigator evaluation software. Complete the following steps to evaluate the ISL8282M with the PMBus option.

(1) Install PowerNavigator.

(2) Disable the module by switching the mechanical switch SW_1 to **2-3** as shown in Figure 4.

(3) Connect the DC input power supply to the banana sockets J_4 and J_3 and the electronic load to sockets J_{14} and J_{15}. Ensure that the polarity for the power leads is correct and the input voltage is within the ISL8282MEVAL1Z's operating range of 4.5V to 15V. Use test points TP_1 (VIN) and TP_3 (GND) to accurately measure the input voltage.

(4) Connect the ZLUSBEVAL3Z dongle (USB to PMBus adapter) to J_8 on the ISL8282MEVAL1Z.

(5) Connect the supplied USB cable from the computer through USB to the ZLUSBEVAL3Z dongle.

(6) Turn on the DC input power supply.

(7) Launch PowerNavigator.

(8) Toggle the mechanical switch SW_1 to **1-2** to enable the module. Alternatively, use the PMBus ON_OFF_CONFIG and OPERATION commands in PowerNavigator to allow PMBus Enable.

(9) Monitor and configure the ISL8282MEVAL1Z using the PMBus commands (see the "SMBus, PMBus, and I^2C Supported Commands" table in the ISL8282M datasheet) in PowerNavigator. Note: The AV gain multiplier (AVMLTI) can be set by external R_5 and R_6 only.

(10) Adjust the input voltage, V_{IN}, within the specified range and observe the output voltage. The output voltage variation should be within ±1.5%.

(11) Adjust the load current to within the specified range of 0A to 15A and observe the output voltage. The output voltage variation should be within ±1.5%.

(12) Populate 1% standard 0402 resistors at the R_{10} and R_{11} placeholder locations on the bottom layer to evaluate multiple power modules using a single ZLUSBEVAL3Z dongle. Table 2 on page 11 is a reference for programming different PMBus addresses. Make sure that each ISL8282MEVAL1Z is assigned to a unique PMBus address as shown in the "SMBus/PMBus/I^2C 7-Bits Format Address (Hex)" table in the ISL8282M datasheet. Connect J_8 on the next ISL8282MEVAL1Z together with J_{10} on the previous ISL8282MEVAL1Z.

PowerNavigator tutorial videos are available on the Renesas website.

2.2 Thermal Considerations and Current Derating

Proper board layout is critical so that the board can operate safely and deliver the maximum allowable power. For the board to operate properly at high ambient temperature environments and carry full load current, carefully design the board layout to maximize thermal performance. For best thermal performance, use enough trace width, copper weight, and proper connectors.

The ISL8282MEVAL1Z is capable of operating at 15A full load current at room temperature without the need for additional cooling systems. However, if the ISL8282MEVAL1Z needs to operate at elevated ambient temperatures, the available output current needs to be derated. See the derated current curves in the ISL8282M datasheet to determine the maximum output current that the ISL8282MEVAL1Z can supply.

2.3 Programming the Resistor Reader

This section contains information about operating the resistor reader with the ISL8282M's four programming pins (PROG1, PROG2, PROG3, and PROG4) to customize module specifications. See the "Programming Pin Descriptions" table in the ISL8282M datasheet for the detailed descriptions of each programming pin.

Table 1. PROG 1 Resistor Reader

PROG1 (DC)	R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
01h	49.9	12.4	0.500
02h	45.3	12.7	0.508
03h	42.2	13.3	0.516
04h	38.3	13.3	0.523
05h	35.7	13.7	0.531
06h	34	14.3	0.539
07h	31.6	14.7	0.547
08h	29.4	15	0.555
09h	28	15.4	0.562
0Ah	26.7	16.2	0.570
0Bh	25.5	16.5	0.578
0Ch	24.3	17.4	0.586
0Dh	23.2	17.8	0.594
0Eh	22.1	18.2	0.602
0Fh	21	19.1	0.609
10h	20	19.6	0.617
11h	19.6	20.5	0.625
12h	18.7	21.5	0.633
13h	18.2	22.6	0.641
14h	17.4	23.2	0.648
15h	16.9	24.3	0.656
16h	16.5	26.1	0.664
17h	15.8	26.7	0.672
18h	15.4	28.7	0.680
19h	15	30.1	0.688
1Ah	14.7	32.4	0.695
1Bh	14	34	0.703
1Ch	13.7	36.5	0.711
1Dh	13.3	39.2	0.719
1Eh	13	43.2	0.727
1Fh	107	26.7	0.734
22h	97.6	27.4	0.742
23h	90.9	28.7	0.750
24h	82.5	28.7	0.758
25h	76.8	29.4	0.766
26h	71.5	30.1	0.773
27h	68.1	31.6	0.781
28h	63.4	32.4	0.789
00h	Open	10	0.797
2Ah	57.6	34.8	0.805

Table 1. PROG 1 Resistor Reader (Continued)

PROG1 (DC)	R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
2Bh	54.9	35.7	0.812
2Ch	52.3	37.4	0.820
2Dh	49.9	38.3	0.828
2Eh	47.5	39.2	0.836
2Fh	45.3	41.2	0.844
20h	Open	21.5	0.852
31h	42.2	44.2	0.859
32h	40.2	45.3	0.867
33h	39.2	48.7	0.875
34h	37.4	49.9	0.883
35h	36.5	52.3	0.891
40h	Open	34.8	0.898
37h	34	57.6	0.906
38h	33.2	61.9	0.914
39h	32.4	66.5	0.922
3Ah	30.9	68.1	0.930
3Bh	30.1	73.2	0.938
3Ch	29.4	78.7	0.945
60h	Open	52.3	0.953
3Eh	28	93.1	0.961
41h	174	43.2	0.969
42h	158	44.2	0.977
43h	147	46.4	0.984
44h	133	46.4	0.992
80h	Open	75	1.000
46h	118	49.9	1.008
47h	110	51.1	1.016
48h	102	52.3	1.023
49h	97.6	53.6	1.031
4A	93.1	56.2	1.039
A0h	Open	105	1.047
4Ch	84.5	60.4	1.055
4Dh	80.6	61.9	1.062
4Eh	76.8	63.4	1.070
4Fh	73.2	66.5	1.078
50h	69.8	68.1	1.086
51h	68.1	71.5	1.094
C0h	Open	147	1.102
53h	63.4	78.7	1.109
54h	60.4	80.6	1.117
55h	59	84.5	1.125

Table 1. PROG 1 Resistor Reader (Continued)

PROG1 (DC)	R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
56h	57.6	90.9	1.133
57h	54.9	93.1	1.141
58h	53.6	100	1.148
59h	52.3	105	1.156
5Ah	49.9	110	1.164
5Bh	48.7	118	1.172
5Ch	47.5	127	1.180
5Dh	46.4	137	1.188
5Eh	45.3	150	1.195
E0h	Open	499	1.203
62h	237	66.5	1.211
63h	221	69.8	1.219
64h	200	69.8	1.227
65h	187	71.5	1.234
66h	178	75	1.242
67h	165	76.8	1.250
68h	154	78.7	1.258
69h	147	80.6	1.266
6Ah	140	84.5	1.273
6Bh	133	86.6	1.281
6Ch	127	90.9	1.289
6Dh	121	93.1	1.297
6Eh	115	95.3	1.305
6Fh	110	100	1.312
70h	105	102	1.320
71h	102	107	1.328
72h	97.6	110	1.336
73h	95.3	118	1.344
1Fh	10	Open	1.352
75h	88.7	127	1.359
76h	86.6	137	1.367
77h	82.5	140	1.375
78h	80.6	150	1.383
79h	78.7	162	1.391
7Ah	75	165	1.398
7Bh	73.2	178	1.406
7Ch	71.5	191	1.414
7Dh	69.8	205	1.422
7Eh	68.1	226	1.430
81h	374	93.1	1.438
82h	340	95.3	1.445

Table 1. PROG 1 Resistor Reader (Continued)

PROG1 (DC)	R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
83h	316	100	1.453
84h	287	100	1.461
85h	267	102	1.469
86h	255	107	1.477
87h	237	110	1.484
88h	221	113	1.492
3Fh	21.5	Open	1.500
8Ah	200	121	1.508
8Bh	191	124	1.516
8Ch	182	130	1.523
8Dh	174	133	1.531
8Eh	165	137	1.539
8Fh	158	143	1.547
90h	150	147	1.555
91h	147	154	1.562
92h	140	158	1.570
93h	137	169	1.578
94h	130	174	1.586
95h	127	182	1.594
96h	124	196	1.602
97h	118	200	1.609
98h	115	215	1.617
99h	113	232	1.625
9Ah	110	243	1.633
9Bh	105	255	1.641
9Ch	102	274	1.648
9Dh	100	294	1.656
9Eh	97.6	324	1.664
A1h	523	130	1.672
A2h	475	133	1.680
A3h	442	140	1.688
A4h	402	140	1.695
A5h	374	143	1.703
A6h	357	150	1.711
A7h	332	154	1.719
A8h	309	158	1.727
A9h	294	162	1.734
AAh	280	169	1.742
ABh	267	174	1.750
ACh	255	182	1.758
ADh	243	187	1.766

Table 1. PROG 1 Resistor Reader (Continued)

PROG1 (DC)	R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
AEh	232	191	1.773
AFh	221	200	1.781
B0h	210	205	1.789
5Fh	34.8	Open	1.797
B2h	196	226	1.805
B3h	191	237	1.812
B4h	182	243	1.820
B5h	178	255	1.828
B6h	174	274	1.836
B7h	165	280	1.914
B8h	162	301	1.992
B9h	158	324	2.070
BAh	154	340	2.148
BBh	147	357	2.227
BCh	143	383	2.305
BDh	140	412	2.383
BEh	137	453	2.461
C1h	732	182	2.469
C2h	665	187	2.477
C3h	619	196	2.484
C4h	576	200	2.492
7Fh	52.3	Open	2.500
C6h	499	210	2.508
C7h	464	215	2.516
C8h	432	221	2.523
C9h	412	226	2.602
CAh	392	237	2.68
CBh	374	243	2.758
CCh	357	255	2.836
CDh	340	261	2.914
CEh	324	267	2.992
9Fh	75	Open	3.000
CFh	309	280	3.070
D0h	301	294	3.148
D1h	287	301	3.227
D2h	274	309	3.281
D3h	267	332	3.289
BFh	105	Open	3.297
D5h	249	357	3.305
D6h	243	383	3.312
D7h	232	392	3.320

Table 1. PROG 1 Resistor Reader (Continued)

PROG1 (DC)	R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
D8h	226	422	3.328
D9h	221	453	3.406
DAh	215	475	3.484
DBh	205	499	3.562
DCh	200	536	3.641
DDh	196	576	3.719
DEh	191	634	3.797
E1h	1000	249	3.875
E2h	909	255	3.953
E3h	845	267	4.031
E4h	768	267	4.109
E5h	715	274	4.188
E6h	665	280	4.266
E7h	634	294	4.344
E8h	590	301	4.422
E9h	562	309	4.500
EAh	536	324	4.578
EBh	511	332	4.656
ECh	487	348	4.734
EDh	464	357	4.812
EEh	442	365	4.891
EFh	422	383	4.969
F0h	402	392	4.977
F1h	392	412	4.984
F2h	374	422	4.992
DFh	147	Open	5.000
F4h	348	464	5.008
FFh	499	Open	0.000

Table 2. PROG 2 Resistor Reader

PROG2 (DD)	R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Comp (°C)	PM_ADDR (7-Bit)
08h	29.4	15	Enabled	+30	40h
09h	28	15.4	Enabled	+30	41h
0Ah	26.7	16.2	Enabled	+30	42h
0Bh	25.5	16.5	Enabled	+30	43h
0Ch	24.3	17.4	Enabled	+30	44h
0Dh	23.2	17.8	Enabled	+30	45h
0Eh	22.1	18.2	Enabled	+30	46h
0Fh	21	19.1	Enabled	+30	47h
00h	Open	10	Enabled	+30	60h

Table 2. PROG 2 Resistor Reader (Continued)

PROG2 (DD)	R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Comp (°C)	PM_ADDR (7-Bit)
01h	Open	10	Enabled	+30	61h
02h	45.3	12.7	Enabled	+30	62h
03h	42.2	13.3	Enabled	+30	63h
04h	38.3	13.3	Enabled	+30	64h
05h	35.7	13.7	Enabled	+30	65h
06h	34	14.3	Enabled	+30	66h
07h	31.6	14.7	Enabled	+30	67h
10h	20	19.6	Enabled	+30	70h
11h	19.6	20.5	Enabled	+30	71h
12h	18.7	21.5	Enabled	+30	72h
13h	18.2	22.6	Enabled	+30	73h
14h	17.4	23.2	Enabled	+30	74h
15h	16.9	24.3	Enabled	+30	75h
16h	16.5	26.1	Enabled	+30	76h
17h	15.8	26.7	Enabled	+30	77h
18h	15.4	28.7	Enabled	+30	78h
19h	15	30.1	Enabled	+30	79h
1Ah	14.7	32.4	Enabled	+30	7Ah
1Bh	14	34	Enabled	+30	7Bh
1Ch	13.7	36.5	Enabled	+30	7Ch
1Dh	13.3	39.2	Enabled	+30	7Dh
1Eh	13	43.2	Enabled	+30	7Eh
1Fh	10	Open	Enabled	+30	7Fh
28h	63.4	32.4	Enabled	+15	40h
29h	60.4	33.2	Enabled	+15	41h
2Ah	57.6	34.8	Enabled	+15	42h
2Bh	54.9	35.7	Enabled	+15	43h
2Ch	52.3	37.4	Enabled	+15	44h
2Dh	49.9	38.3	Enabled	+15	45h
2Eh	47.5	39.2	Enabled	+15	46h
2Fh	45.3	41.2	Enabled	+15	47h
20h	Open	21.5	Enabled	+15	60h
21h	107	26.7	Enabled	+15	61h
22h	97.6	27.4	Enabled	+15	62h
23h	90.9	28.7	Enabled	+15	63h
24h	82.5	28.7	Enabled	+15	64h
25h	76.8	29.4	Enabled	+15	65h
26h	71.5	30.1	Enabled	+15	66h
27h	68.1	31.6	Enabled	+15	67h
30h	43.2	42.2	Enabled	+15	70h

Table 2. PROG 2 Resistor Reader (Continued)

PROG2 (DD)	R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Comp (°C)	PM_ADDR (7-Bit)
31h	42.2	44.2	Enabled	+15	71h
32h	40.2	45.3	Enabled	+15	72h
33h	39.2	48.7	Enabled	+15	73h
34h	37.4	49.9	Enabled	+15	74h
35h	36.5	52.3	Enabled	+15	75h
36h	34.8	54.9	Enabled	+15	76h
37h	34	57.6	Enabled	+15	77h
38h	33.2	61.9	Enabled	+15	78h
39h	32.4	66.5	Enabled	+15	79h
3Ah	30.9	68.1	Enabled	+15	7Ah
3Bh	30.1	73.2	Enabled	+15	7Bh
3Ch	29.4	78.7	Enabled	+15	7Ch
3Dh	28.7	84.5	Enabled	+15	7Dh
3Eh	28	93.1	Enabled	+15	7Eh
3Fh	21.5	Open	Enabled	+15	7Fh
48h	102	52.3	Enabled	+5	40h
49h	97.6	53.6	Enabled	+5	41h
4Ah	93.1	56.2	Enabled	+5	42h
4Bh	88.7	57.6	Enabled	+5	43h
4Ch	84.5	60.4	Enabled	+5	44h
4Dh	80.6	61.9	Enabled	+5	45h
4Eh	76.8	63.4	Enabled	+5	46h
4Fh	73.2	66.5	Enabled	+5	47h
40h	Open	34.8	Enabled	+5	60h
41h	174	43.2	Enabled	+5	61h
42h	158	44.2	Enabled	+5	62h
43h	147	46.4	Enabled	+5	63h
44h	133	46.4	Enabled	+5	64h
45h	124	47.5	Enabled	+5	65h
46h	118	49.9	Enabled	+5	66h
47h	110	51.1	Enabled	+5	67h
50h	69.8	68.1	Enabled	+5	70h
51h	68.1	71.5	Enabled	+5	71h
52h	64.9	73.2	Enabled	+5	72h
53h	63.4	78.7	Enabled	+5	73h
54h	60.4	80.6	Enabled	+5	74h
55h	59	84.5	Enabled	+5	75h
56h	57.6	90.9	Enabled	+5	76h
57h	54.9	93.1	Enabled	+5	77h
58h	53.6	100	Enabled	+5	78h

Table 2. PROG 2 Resistor Reader (Continued)

PROG2 (DD)	R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Comp (°C)	PM_ADDR (7-Bit)
59h	52.3	105	Enabled	+5	79h
5Ah	49.9	110	Enabled	+5	7Ah
5Bh	48.7	118	Enabled	+5	7Bh
5Ch	47.5	127	Enabled	+5	7Ch
5Dh	46.4	137	Enabled	+5	7Dh
5Eh	45.3	150	Enabled	+5	7Eh
5Fh	34.8	Open	Enabled	+5	7Fh
68h	154	78.7	Enabled	Off	40h
69h	147	80.6	Enabled	Off	41h
6Ah	140	84.5	Enabled	Off	42h
6Bh	133	86.6	Enabled	Off	43h
6Ch	127	90.9	Enabled	Off	44h
6Dh	121	93.1	Enabled	Off	45h
6Eh	115	95.3	Enabled	Off	46h
6Fh	110	100	Enabled	Off	47h
60h	Open	52.3	Enabled	Off	60h
61h	261	64.9	Enabled	Off	61h
62h	237	66.5	Enabled	Off	62h
63h	221	69.8	Enabled	Off	63h
64h	200	69.8	Enabled	Off	64h
65h	187	71.5	Enabled	Off	65h
66h	178	75	Enabled	Off	66h
67h	165	76.8	Enabled	Off	67h
70h	105	102	Enabled	Off	70h
71h	102	107	Enabled	Off	71h
72h	97.6	110	Enabled	Off	72h
73h	95.3	118	Enabled	Off	73h
74h	90.9	121	Enabled	Off	74h
75h	88.7	127	Enabled	Off	75h
76h	86.6	137	Enabled	Off	76h
77h	82.5	140	Enabled	Off	77h
78h	80.6	150	Enabled	Off	78h
79h	78.7	162	Enabled	Off	79h
7Ah	75	165	Enabled	Off	7Ah
7Bh	73.2	178	Enabled	Off	7Bh
7Ch	71.5	191	Enabled	Off	7Ch
7Dh	69.8	205	Enabled	Off	7Dh
7Eh	68.1	226	Enabled	Off	7Eh
7Fh	52.3	Open	Enabled	Off	7Fh
88h	221	113	Disabled	+30	40h

Table 2. PROG 2 Resistor Reader (Continued)

PROG2 (DD)	R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Comp (°C)	PM_ADDR (7-Bit)
89h	210	115	Disabled	+30	41h
8Ah	200	121	Disabled	+30	42h
8Bh	191	124	Disabled	+30	43h
8Ch	182	130	Disabled	+30	44h
8Dh	174	133	Disabled	+30	45h
8Eh	165	137	Disabled	+30	46h
8Fh	158	143	Disabled	+30	47h
80h	Open	75	Disabled	+30	60h
81h	374	93.1	Disabled	+30	61h
82h	340	95.3	Disabled	+30	62h
83h	316	100	Disabled	+30	63h
84h	287	100	Disabled	+30	64h
85h	267	102	Disabled	+30	65h
86h	255	107	Disabled	+30	66h
87h	237	110	Disabled	+30	67h
90h	150	147	Disabled	+30	70h
91h	147	154	Disabled	+30	71h
92h	140	158	Disabled	+30	72h
93h	137	169	Disabled	+30	73h
94h	130	174	Disabled	+30	74h
95h	127	182	Disabled	+30	75h
96h	124	196	Disabled	+30	76h
97h	118	200	Disabled	+30	77h
98h	115	215	Disabled	+30	78h
99h	113	232	Disabled	+30	79h
9Ah	110	243	Disabled	+30	7Ah
9Bh	105	255	Disabled	+30	7Bh
9Ch	102	274	Disabled	+30	7Ch
9Dh	100	294	Disabled	+30	7Dh
9Eh	97.6	324	Disabled	+30	7Eh
9Fh	75	Open	Disabled	+30	7Fh
A8h	309	158	Disabled	+15	40h
A9h	294	162	Disabled	+15	41h
AAh	280	169	Disabled	+15	42h
ABh	267	174	Disabled	+15	43h
ACh	255	182	Disabled	+15	44h
ADh	243	187	Disabled	+15	45h
AEh	232	191	Disabled	+15	46h
AFh	221	200	Disabled	+15	47h
A0h	Open	105	Disabled	+15	60h

Table 2. PROG 2 Resistor Reader (Continued)

PROG2 (DD)	R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Comp (°C)	PM_ADDR (7-Bit)
A1h	523	130	Disabled	+15	61h
A2h	475	133	Disabled	+15	62h
A3h	442	140	Disabled	+15	63h
A4h	402	140	Disabled	+15	64h
A5h	374	143	Disabled	+15	65h
A6h	357	150	Disabled	+15	66h
A7h	332	154	Disabled	+15	67h
B0h	210	205	Disabled	+15	70h
B1h	205	215	Disabled	+15	71h
B2h	196	226	Disabled	+15	72h
B3h	191	237	Disabled	+15	73h
B4h	182	243	Disabled	+15	74h
B5h	178	255	Disabled	+15	75h
B6h	174	274	Disabled	+15	76h
B7h	165	280	Disabled	+15	77h
B8h	162	301	Disabled	+15	78h
B9h	158	324	Disabled	+15	79h
BAh	154	340	Disabled	+15	7Ah
BBh	147	357	Disabled	+15	7Bh
BCh	143	383	Disabled	+15	7Ch
BDh	140	412	Disabled	+15	7Dh
BEh	137	453	Disabled	+15	7Eh
BFh	105	Open	Disabled	+15	7Fh
C8h	432	221	Disabled	+5	40h
C9h	412	226	Disabled	+5	41h
CAh	392	237	Disabled	+5	42h
CBh	374	243	Disabled	+5	43h
CCh	357	255	Disabled	+5	44h
CDh	340	261	Disabled	+5	45h
CEh	324	267	Disabled	+5	46h
CFh	309	280	Disabled	+5	47h
C0h	Open	147	Disabled	+5	60h
C1h	732	182	Disabled	+5	61h
C2h	665	187	Disabled	+5	62h
C3h	619	196	Disabled	+5	63h
C4h	576	200	Disabled	+5	64h
C5h	523	200	Disabled	+5	65h
C6h	499	210	Disabled	+5	66h
C7h	464	215	Disabled	+5	67h
D0h	301	294	Disabled	+5	70h

Table 2. PROG 2 Resistor Reader (Continued)

PROG2 (DD)	R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Comp (°C)	PM_ADDR (7-Bit)
D1h	287	301	Disabled	+5	71h
D2h	274	309	Disabled	+5	72h
D3h	267	332	Disabled	+5	73h
D4h	255	340	Disabled	+5	74h
D5h	249	357	Disabled	+5	75h
D6h	243	383	Disabled	+5	76h
D7h	232	392	Disabled	+5	77h
D8h	226	422	Disabled	+5	78h
D9h	221	453	Disabled	+5	79h
DAh	215	475	Disabled	+5	7Ah
DBh	205	499	Disabled	+5	7Bh
DCh	200	536	Disabled	+5	7Ch
DDh	196	576	Disabled	+5	7Dh
DEh	191	634	Disabled	+5	7Eh
DFh	147	Open	Disabled	+5	7Fh
E8h	590	301	Disabled	Off	40h
E9h	562	309	Disabled	Off	41h
EAh	536	324	Disabled	Off	42h
EBh	511	332	Disabled	Off	43h
ECh	487	348	Disabled	Off	44h
EDh	464	357	Disabled	Off	45h
EEh	442	365	Disabled	Off	46h
EFh	422	383	Disabled	Off	47h
E0h	Open	499	Disabled	Off	60h
E1h	1000	249	Disabled	Off	61h
E2h	909	255	Disabled	Off	62h
E3h	845	267	Disabled	Off	63h
E4h	768	267	Disabled	Off	64h
E5h	715	274	Disabled	Off	65h
E6h	665	280	Disabled	Off	66h
E7h	634	294	Disabled	Off	67h
F0h	402	392	Disabled	Off	70h
F1h	392	412	Disabled	Off	71h
F2h	374	422	Disabled	Off	72h
F3h	365	453	Disabled	Off	73h
F4h	348	464	Disabled	Off	74h
F5h	340	487	Disabled	Off	75h
F6h	324	511	Disabled	Off	76h
F7h	316	536	Disabled	Off	77h
F8h	309	576	Disabled	Off	78h

Table 2. PROG 2 Resistor Reader (Continued)

PROG2 (DD)	R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Comp (°C)	PM_ADDR (7-Bit)
F9h	301	604	Disabled	Off	79h
FAh	287	634	Disabled	Off	7Ah
FBh	280	681	Disabled	Off	7Bh
FCh	274	732	Disabled	Off	7Ch
FDh	267	787	Disabled	Off	7Dh
FEh	261	866	Disabled	Off	7Eh
FFh	499	Open	Disabled	Off	7Fh

Table 3. PROG 3 Resistor Reader

PROG3 (DE)	R_{UP} (kΩ)	R_{DW} (kΩ)	Ultrasonic PFM	Fault Behavior	f_{SW} (kHz)	AV Gain	
						1x	2x
01h	49.9	12.4	Disabled	Retry	300	36.5	73
02h	45.3	12.7	Disabled	Retry	300	30.5	61
03h	42.2	13.3	Disabled	Retry	300	24.5	49
04h	38.3	13.3	Disabled	Retry	300	19	38
05h	35.7	13.7	Disabled	Retry	300	13	26
06h	34	14.3	Disabled	Retry	300	7	14
07h	31.6	14.7	Disabled	Retry	300	1	2
08h	29.4	15	Disabled	Retry	400	42	84
09h	28	15.4	Disabled	Retry	400	36.5	73
0Ah	26.7	16.2	Disabled	Retry	400	30.5	61
0Bh	25.5	16.5	Disabled	Retry	400	24.5	49
0Ch	24.3	17.4	Disabled	Retry	400	19	38
0Dh	23.2	17.8	Disabled	Retry	400	13	26
0Eh	22.1	18.2	Disabled	Retry	400	7	14
0Fh	21	19.1	Disabled	Retry	400	1	2
10h	20	19.6	Disabled	Retry	500	42	84
11h	19.6	20.5	Disabled	Retry	500	36.5	73
12h	18.7	21.5	Disabled	Retry	500	30.5	61
13h	18.2	22.6	Disabled	Retry	500	24.5	49
14h	17.4	23.2	Disabled	Retry	500	19	38
15h	16.9	24.3	Disabled	Retry	500	13	26
16h	16.5	26.1	Disabled	Retry	500	7	14
17h	15.8	26.7	Disabled	Retry	500	1	2
18h	15.4	28.7	Disabled	Retry	600	42	84
19h	15	30.1	Disabled	Retry	600	36.5	73
1Ah	14.7	32.4	Disabled	Retry	600	30.5	61
1Bh	14	34	Disabled	Retry	600	24.5	49
1Ch	13.7	36.5	Disabled	Retry	600	19	38
1Dh	13.3	39.2	Disabled	Retry	600	13	26

Table 3. PROG 3 Resistor Reader (Continued)

PROG3 (DE)	R_{UP} (kΩ)	R_{DW} (kΩ)	Ultrasonic PFM	Fault Behavior	f_{SW} (kHz)	AV Gain	
						1x	2x
1Eh	13	43.2	Disabled	Retry	600	7	14
1Fh	10	Open	Disabled	Retry	600	1	2
20h	Open	21.5	Disabled	Retry	700	42	84
21h	107	26.7	Disabled	Retry	700	36.5	73
22h	97.6	27.4	Disabled	Retry	700	30.5	61
23h	90.9	28.7	Disabled	Retry	700	24.5	49
24h	82.5	28.7	Disabled	Retry	700	19	38
25h	76.8	29.4	Disabled	Retry	700	13	26
26h	71.5	30.1	Disabled	Retry	700	7	14
27h	68.1	31.6	Disabled	Retry	700	1	2
28h	63.4	32.4	Disabled	Retry	850	42	84
29h	60.4	33.2	Disabled	Retry	850	36.5	73
2Ah	57.6	34.8	Disabled	Retry	850	30.5	61
2Bh	54.9	35.7	Disabled	Retry	850	24.5	49
2Ch	52.3	37.4	Disabled	Retry	850	19	38
2Dh	49.9	38.3	Disabled	Retry	850	13	26
2Eh	47.5	39.2	Disabled	Retry	850	7	14
2Fh	45.3	41.2	Disabled	Retry	850	1	2
30h	43.2	42.2	Disabled	Retry	1000	42	84
31h	42.2	44.2	Disabled	Retry	1000	36.5	73
32h	40.2	45.3	Disabled	Retry	1000	30.5	61
33h	39.2	48.7	Disabled	Retry	1000	24.5	49
34h	37.4	49.9	Disabled	Retry	1000	19	38
35h	36.5	52.3	Disabled	Retry	1000	13	26
36h	34.8	54.9	Disabled	Retry	1000	7	14
37h	34	57.6	Disabled	Retry	1000	1	2
40h	Open	34.8	Disabled	Latch	300	42	84
41h	174	43.2	Disabled	Latch	300	36.5	73
42h	158	44.2	Disabled	Latch	300	30.5	61
43h	147	46.4	Disabled	Latch	300	24.5	49
44h	133	46.4	Disabled	Latch	300	19	38
45h	124	47.5	Disabled	Latch	300	13	26
46h	118	49.9	Disabled	Latch	300	7	14
47h	110	51.1	Disabled	Latch	300	1	2
48h	102	52.3	Disabled	Latch	400	42	84
49h	97.6	53.6	Disabled	Latch	400	36.5	73
4Ah	93.1	56.2	Disabled	Latch	400	30.5	61

Table 3. PROG 3 Resistor Reader (Continued)

PROG3 (DE)	R_{UP} (kΩ)	R_{DW} (kΩ)	Ultrasonic PFM	Fault Behavior	f_{SW} (kHz)	AV Gain	
						1x	2x
4Bh	88.7	57.6	Disabled	Latch	400	24.5	49
4Ch	84.5	60.4	Disabled	Latch	400	19	38
4Dh	80.6	61.9	Disabled	Latch	400	13	26
4Eh	76.8	63.4	Disabled	Latch	400	7	14
4Fh	73.2	66.5	Disabled	Latch	400	1	2
50h	69.8	68.1	Disabled	Latch	500	42	84
51h	68.1	71.5	Disabled	Latch	500	36.5	73
52h	64.9	73.2	Disabled	Latch	500	30.5	61
53h	63.4	78.7	Disabled	Latch	500	24.5	49
54h	60.4	80.6	Disabled	Latch	500	19	38
55h	59	84.5	Disabled	Latch	500	13	26
56h	57.6	90.9	Disabled	Latch	500	7	14
57h	54.9	93.1	Disabled	Latch	500	1	2
58h	53.6	100	Disabled	Latch	600	42	84
59h	52.3	105	Disabled	Latch	600	36.5	73
5Ah	49.9	110	Disabled	Latch	600	30.5	61
5Bh	48.7	118	Disabled	Latch	600	24.5	49
5Ch	47.5	127	Disabled	Latch	600	19	38
5Dh	46.4	137	Disabled	Latch	600	13	26
5Eh	45.3	150	Disabled	Latch	600	7	14
5Fh	34.8	Open	Disabled	Latch	600	1	2
60h	Open	52.3	Disabled	Latch	700	42	84
61h	261	64.9	Disabled	Latch	700	36.5	73
62h	237	66.5	Disabled	Latch	700	30.5	61
63h	221	69.8	Disabled	Latch	700	24.5	49
64h	200	69.8	Disabled	Latch	700	19	38
65h	187	71.5	Disabled	Latch	700	13	26
66h	178	75	Disabled	Latch	700	7	14
67h	165	76.8	Disabled	Latch	700	1	2
68h	154	78.7	Disabled	Latch	850	42	84
69h	147	80.6	Disabled	Latch	850	36.5	73
6Ah	140	84.5	Disabled	Latch	850	30.5	61
6Bh	133	86.6	Disabled	Latch	850	24.5	49
6Ch	127	90.9	Disabled	Latch	850	19	38
6Dh	121	93.1	Disabled	Latch	850	13	26
6Eh	115	95.3	Disabled	Latch	850	7	14
6Fh	110	100	Disabled	Latch	850	1	2
70h	105	102	Disabled	Latch	1000	42	84
71h	102	107	Disabled	Latch	1000	36.5	73
72h	97.6	110	Disabled	Latch	1000	30.5	61

Table 3. PROG 3 Resistor Reader (Continued)

PROG3 (DE)	R_{UP} (kΩ)	R_{DW} (kΩ)	Ultrasonic PFM	Fault Behavior	f_{SW} (kHz)	AV Gain	
						1x	2x
73h	95.3	118	Disabled	Latch	1000	24.5	49
74h	90.9	121	Disabled	Latch	1000	19	38
75h	88.7	127	Disabled	Latch	1000	13	26
76h	86.6	137	Disabled	Latch	1000	7	14
77h	82.5	140	Disabled	Latch	1000	1	2

Table 4. PROG 4 Resistor Reader

PROG4 (DF)	R_{UP} (kΩ)	R_{DW} (kΩ)	SS Rate (mV/µs)	RR (kΩ)	AVMLTI
A0h	Open	105	0.157	200	1
A7h	332	154	0.157	200	2
A8h	309	158	0.157	400	1
AFh	221	200	0.157	400	2
B0h	210	205	0.157	600	1
B7h	165	280	0.157	600	2
B8h	162	301	0.157	800	1
BFh	105	Open	0.157	800	2
C0h	Open	147	0.315	200	1
C7h	464	215	0.315	200	2
C8h	432	221	0.315	400	1
CFh	309	280	0.315	400	2
D0h	301	294	0.315	600	1
D7h	232	392	0.315	600	2
D8h	226	422	0.315	800	1
DFh	147	Open	0.315	800	2
E0h	Open	499	0.625	200	1
E7h	634	294	0.625	200	2
E8h	590	301	0.625	400	1
EFh	422	383	0.625	400	2
F0h	402	392	0.625	600	1
F7h	316	536	0.625	600	2
F8h	309	576	0.625	800	1
FFh	499	Open	0.625	800	2
00h	Open	10	1.25	200	1
07h	31.6	14.7	1.25	200	2
08h	29.4	15	1.25	400	1
0Fh	21	19.1	1.25	400	2
10h	20	19.6	1.25	600	1
17h	15.8	26.7	1.25	600	2
18h	15.4	28.7	1.25	800	1
1Fh	10	Open	1.25	800	2

Table 4. PROG 4 Resistor Reader (Continued)

PROG4 (DF)	R_{UP} (kΩ)	R_{DW} (kΩ)	SS Rate (mV/µs)	RR (kΩ)	AVMLTI
20h	Open	21.5	2.5	200	1
27h	68.1	31.6	2.5	200	2
28h	63.4	32.4	2.5	400	1
2Fh	45.3	41.2	2.5	400	2
30h	43.2	42.2	2.5	600	1
37h	34	57.6	2.5	600	2
38h	33.2	61.9	2.5	800	1
3Fh	21.5	Open	2.5	800	2
40h	Open	34.8	5	200	1
47h	110	51.1	5	200	2
48h	102	52.3	5	400	1
4Fh	73.2	66.5	5	400	2
50h	69.8	68.1	5	600	1
57h	54.9	93.1	5	600	2
58h	53.6	100	5	800	1
5Fh	34.8	Open	5	800	2
60h	Open	52.3	10	200	1
67h	165	76.8	10	200	2
68h	154	78.7	10	400	1
6Fh	110	100	10	400	2
70h	105	102	10	600	1
77h	82.5	140	10	600	2
78h	80.6	150	10	800	1
7Fh	52.3	Open	10	800	2

3. PCB Layout Guidelines

The ISL8282MEVAL1Z is a 3x3.4 inch six-layer FR-4 board with 2oz. copper on all layers. This board can be used as a single 15A reference design. For board layout information, see Figures 7 through 14 starting on page page 27.

The ISL8282MEVAL1Z board layout is optimized for electrical performance, low loss, and good thermal performance. For similar performance in designs using the ISL8282M, use the following layout design tips.

3.1 Layout Considerations

(1) Renesas recommends using a six-layer PCB board. Use the top and bottom layer to route VIN and VOUT. Use a full ground plane in the internal layers (underneath the module) with shared SGND and PGND to simplify the layout design. Use another full ground plane directly above the bottom layer. Use the other internal layers to route the remote sense, PGOOD, SCL, SDA, and SALERT signals.

(2) Place the input capacitors and high frequency decoupling ceramic capacitors between VIN and PGND as close to the module as possible. The loop formed by the input capacitors, VIN, and PGND must be as small as possible to minimize high frequency noise. Place the output ceramic capacitors close to VOUT. Use a copper plane to connect the output ceramic capacitors to the load to avoid any parasitic inductances and resistances. See Figures 2 and 3 for example layouts.

(3) Use large copper planes for power paths (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress. Use multiple vias to connect the power planes in different layers.

(4) Do not oversize the copper planes for the PHASE planes. Because the PHASE planes are subjected to very high dv/dt, the parasitic capacitor formed between these planes and the surrounding circuitry tends to couple the switching noise. Ensure that none of the sensitive signal traces are routed close to the PHASE plane.

(5) Place the PVCC and VIN1 bypass capacitors underneath the PVCC and VIN1 pins and connect their grounds to the SGND. For the external pin-strap resistor dividers connected to PROG1, PROG2, PROG3, and PROG4, connect the low side dividers' ground to the SGND. If a local decoupling capacitor is used to bias these resistor dividers, place the decoupling capacitor close to the dividers and connect the capacitor's ground to the SGND. An example layout is illustrated in Figure 3.

(6) Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation. Route the remote sensing traces in parallel underneath the PGND layer and avoid routing the sensing trace near noisy planes such as PHASE. Place 2Ω resistors close to both VSEN and RGND to dampen the noise on the traces.

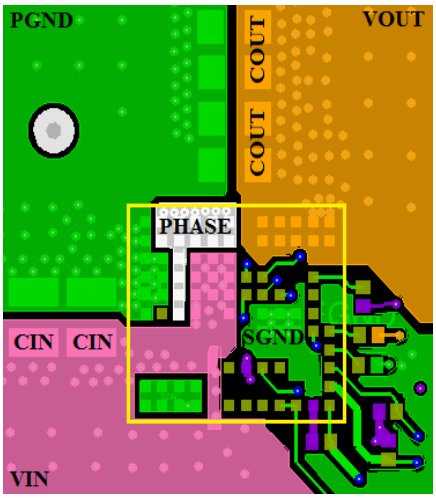

Figure 2. Layout Example - Top Layer

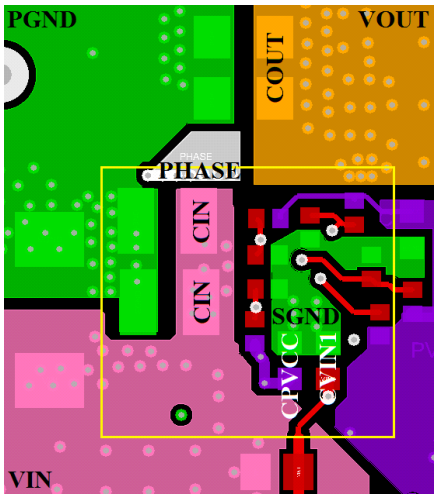

Figure 3. Layout Example - Bottom Layer

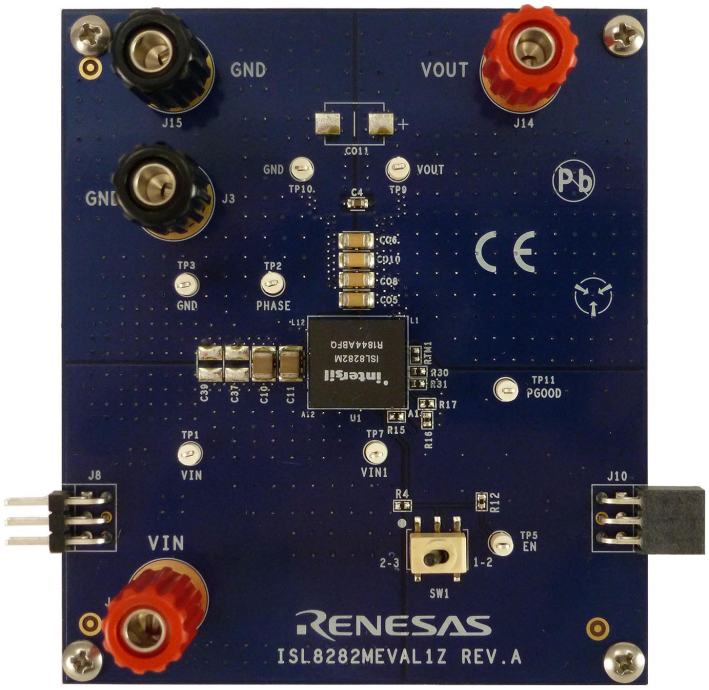

Figure 4. Top of Board

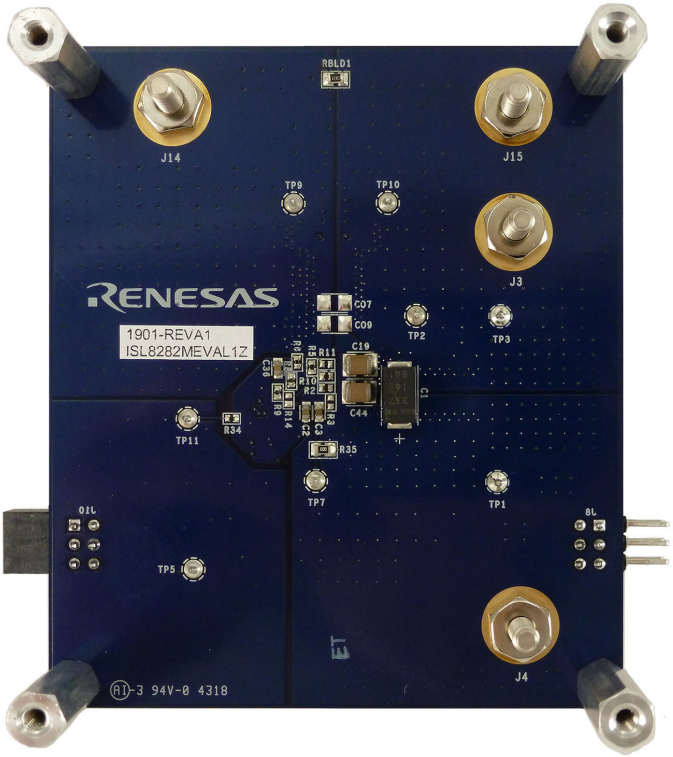

Figure 5. Bottom of Board

3.2 Schematic

RESISTOR READER

PROG1 BOOT VOLTAGE=1V, R3=OPEN; R2=75K OHMS

PROG2 PFM DISABLED, TCOMP=5C AND PMBUS ADDRESS 0X60, R11=OPEN; R10=147K OHMS

PROG3 RETRY,400KHZ,AV49 AND 25KHZ CLAMP DISABLED, R9= 25.5K OHMS; R8= 16.5K OHMS

PROG4 SS= 0.157MV/US, RR=200KOHM AND AVMULTI=2X, R6= 332K OHMS;R5=154K OHMS

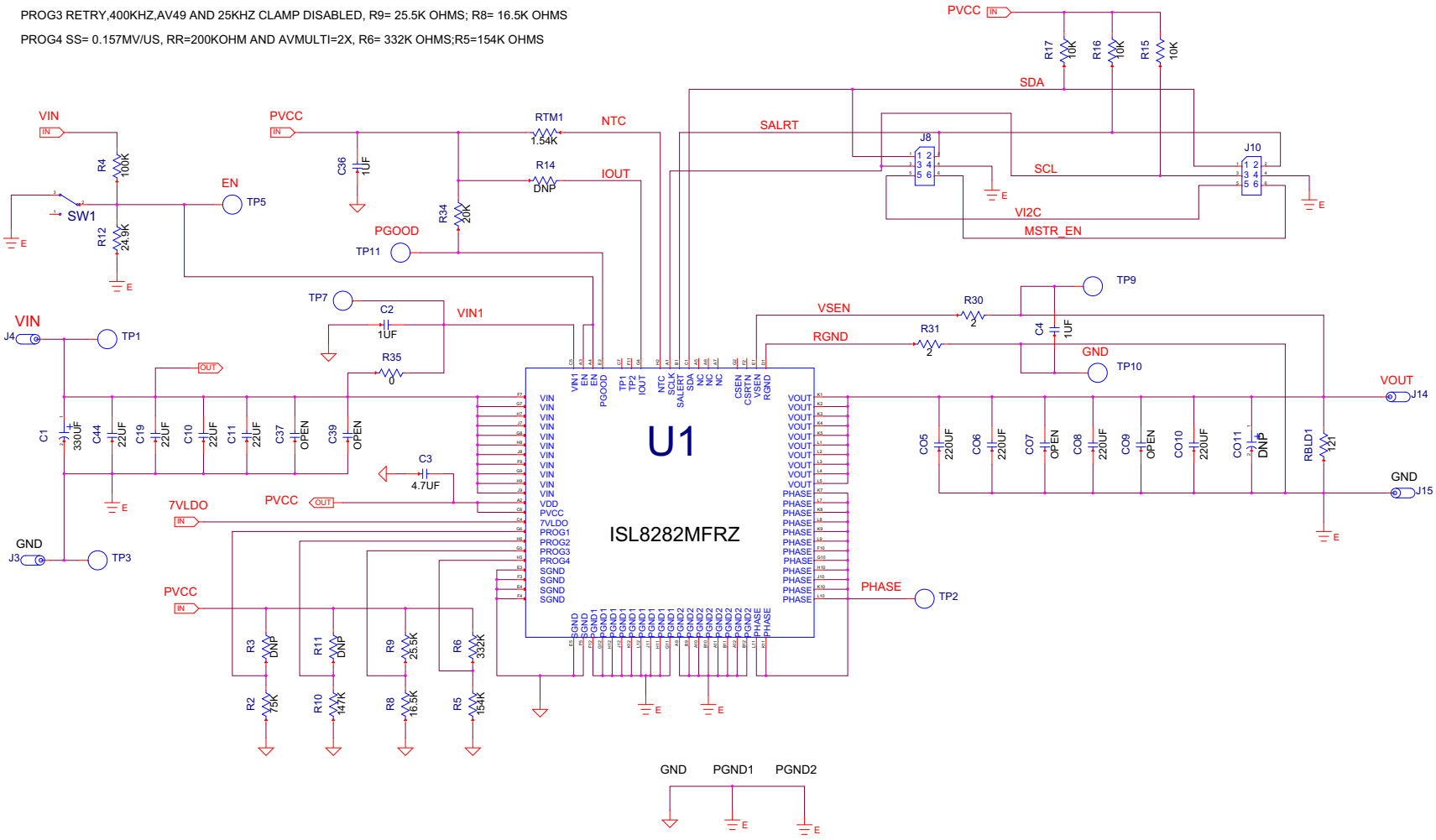

Figure 6. Schematic

3.3 Bill of Materials

Reference Designators	Qty	Value	Tol.	Voltage	Power	Package Type	Manufacturer	Part Number	Description
C1	1	330µF	±20%	16V		2917	Kemet	T521X337M016ATE025	POSCAP
C2, C36	2	1µF	±10%	25V		0603	Taiyo Yuden	TMK107BJ105KA-T	Ceramic Capacitor
C10, C11, C19, C44	4	22µF	±10%	25V		1210	Murata	GRM32ER71E226KE15L	Ceramic Capacitor
C3	1	4.7µF	±10%	10V		0603			Ceramic Capacitor
C4	1	1µF	±10%	16V		0603	TDK	C1608X7R1C105K	Ceramic Capacitor
CO5, CO6, CO8, C10	4	220µF	±20%	6.3V		1206	Murata	GRM31CR60J227ME11L	Ceramic Capacitor
C37, C39, CO7, CO9, CO11	5								DNP
J3, J15	2						Cinch Connectivity Solutions	111-0703-001	Binging Post (Black)
J4, J14,	2						Cinch Connectivity Solutions	111-0702-001	Binging Post (Red)
J8	1					Through Hole	Samtec	TSW-103-08-T-D-RA	6 Pin Male Right Angle Header 0.100” (2.54mm)
J10	1					Through Hole	Samtec	SSQ-103-02-T-D-RA	6 Pin Female Right Angle Header 0.100” (2.54mm)
RBLD1	1	121Ω	±1%		1/10W	0805			Thick Film Chip Resistor
RTM1	1	1.54kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R2	1	75kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R4	1	100kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R5	1	154kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R6	1	332kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R8	1	16.5kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R9	1	25.5kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R10	1	147kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R12	1	24.9kΩ	±1%		1/16W	0402			Thick Film Chip Resistor

Reference Designators	Qty	Value	Tol.	Voltage	Power	Package Type	Manufacturer	Part Number	Description
R15-R17	3	10kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R30, R31	2	2Ω	±1%		1/16W	0402	Vishay	CRCW04022R00FKED	Thick Film Chip Resistor
R34	1	20kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R35	1	0Ω	±1%		1/10W	0805			Thick Film Chip Resistor
R3, R11, R14	3								DNP
SW1	1						C&K	GT11MSCBE	Switch Toggle SPDT 0.4VA 20V
TP1-TP3, TP5, TP7, TP9-TP11	8					Through Hole	Keystone	5002	Miniature PC Test Point, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type
U1	1					12x11 HDA	Renesas	ISL8282MFRZ	15A Step-Down Power Module

3.4 Board Layout

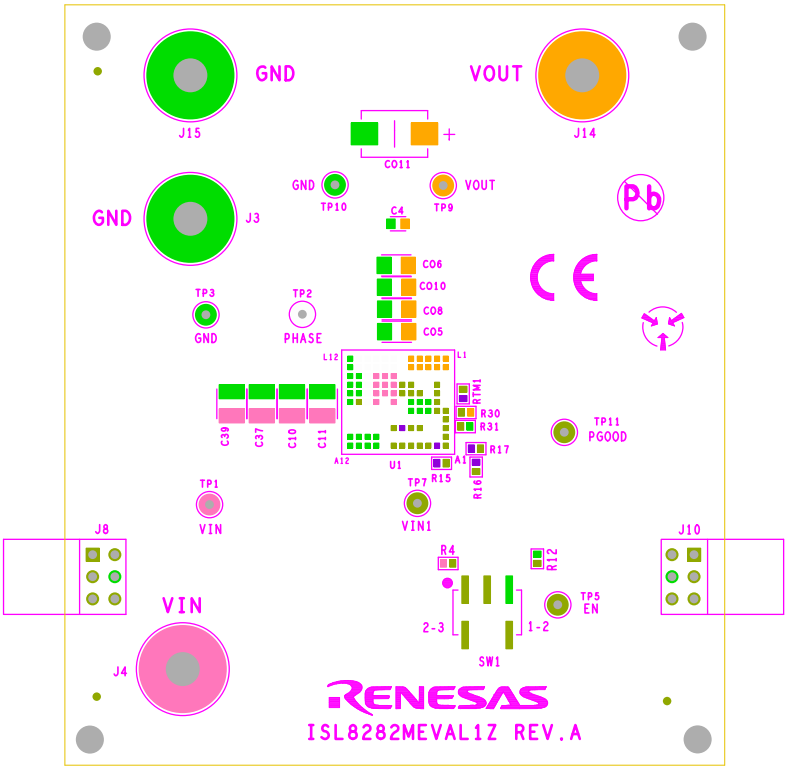

Figure 7. Silkscreen Top

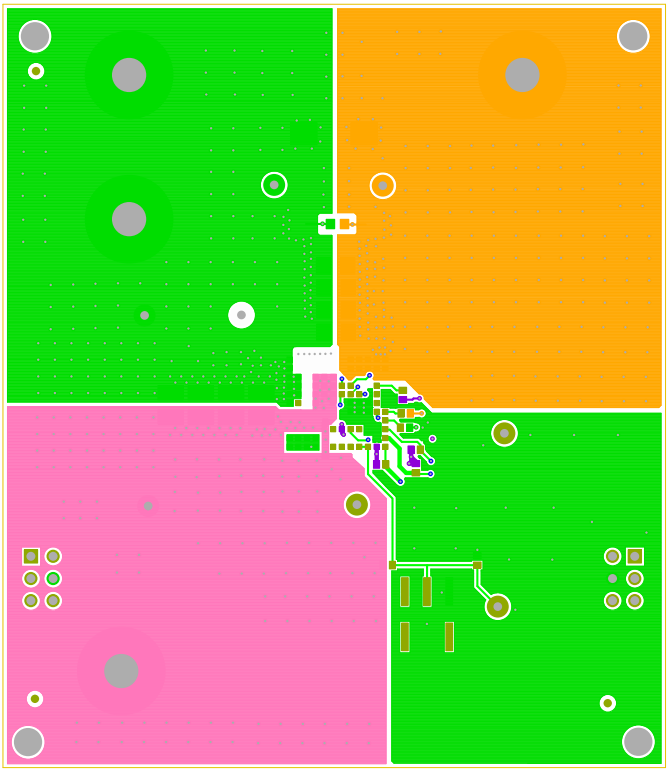

Figure 8. Top Layer Component Side

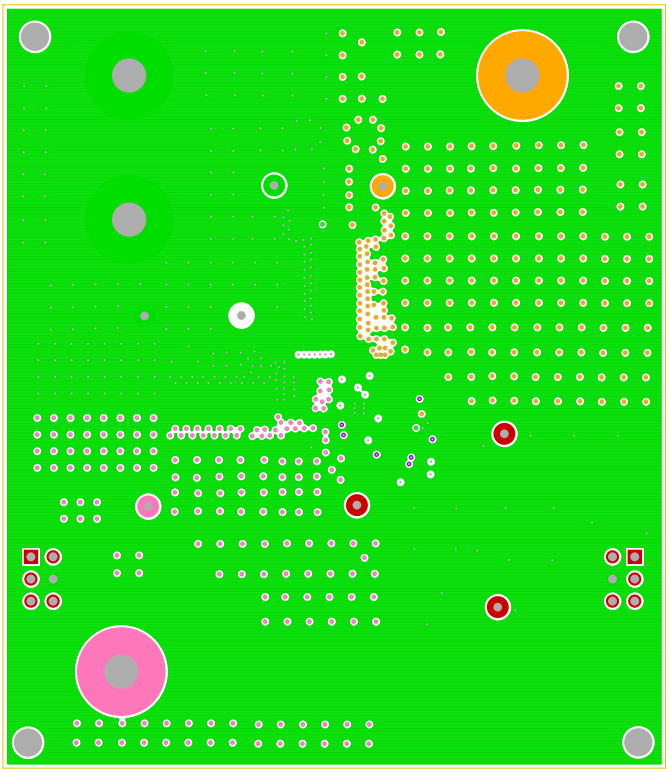

Figure 9. Inner Layer 2

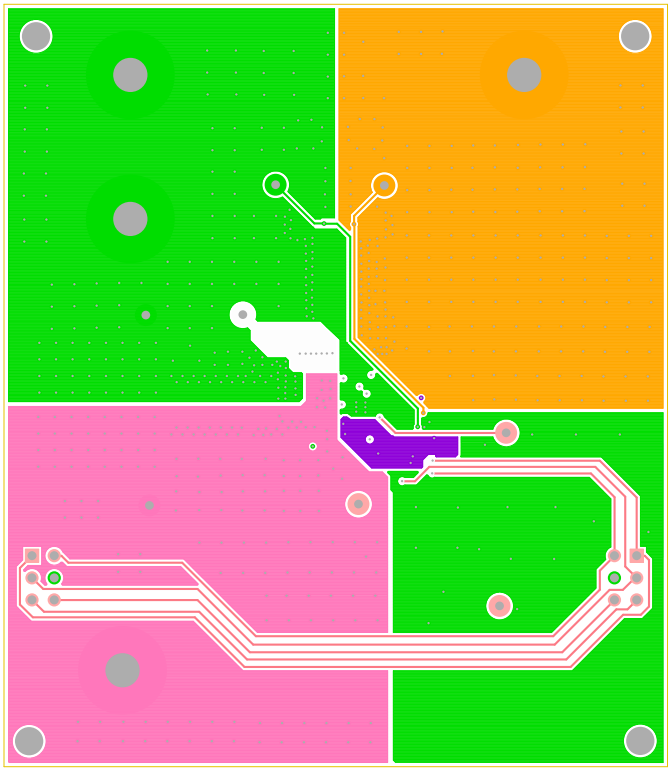

Figure 10. Inner Layer 3

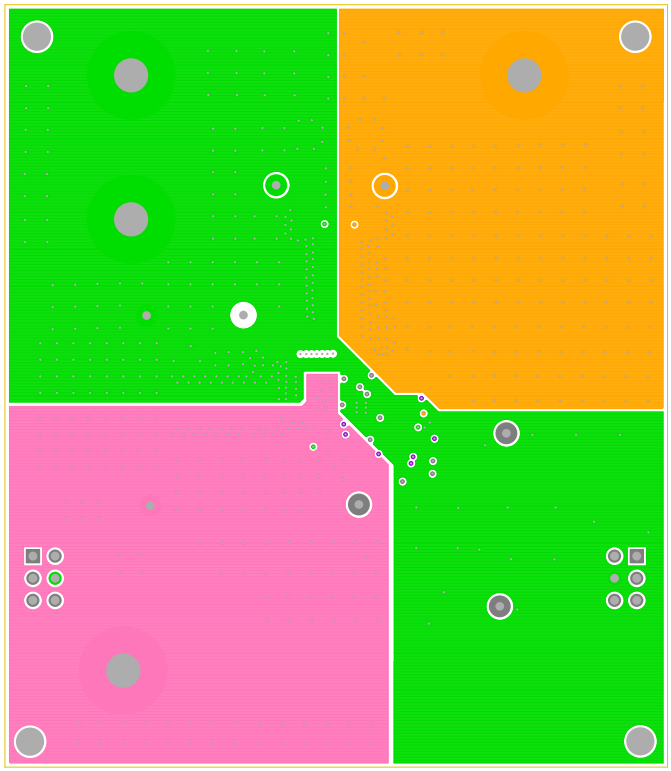

Figure 11. Inner Layer 4

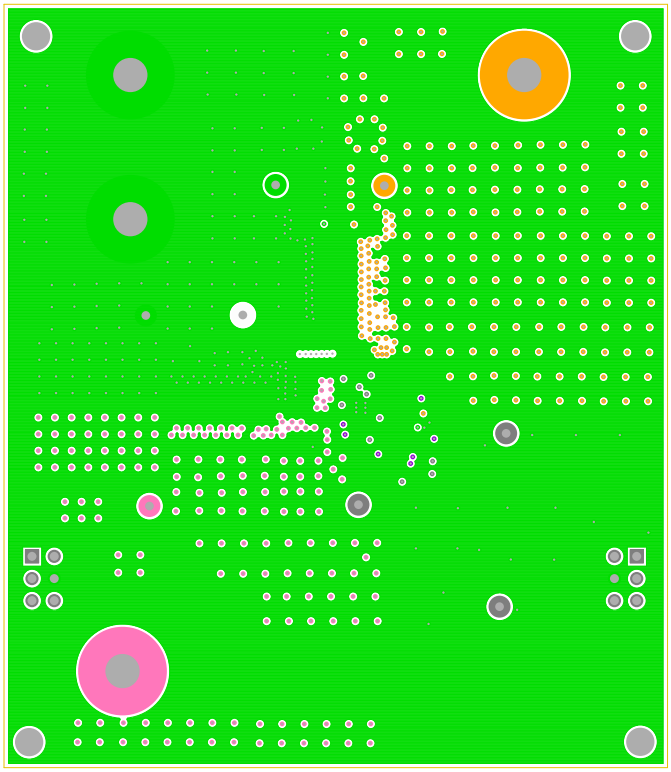

Figure 12. Inner Layer 5

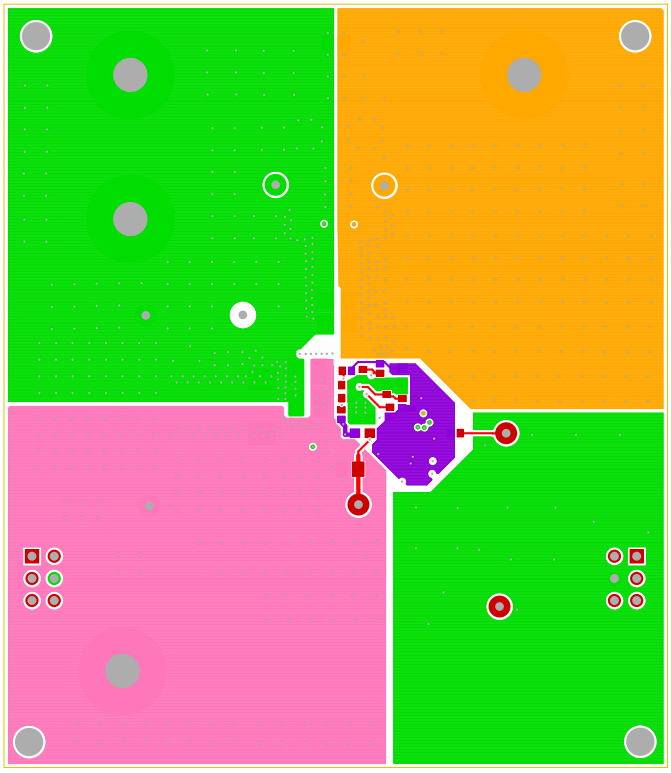

Figure 13. Bottom Layer Solder Side

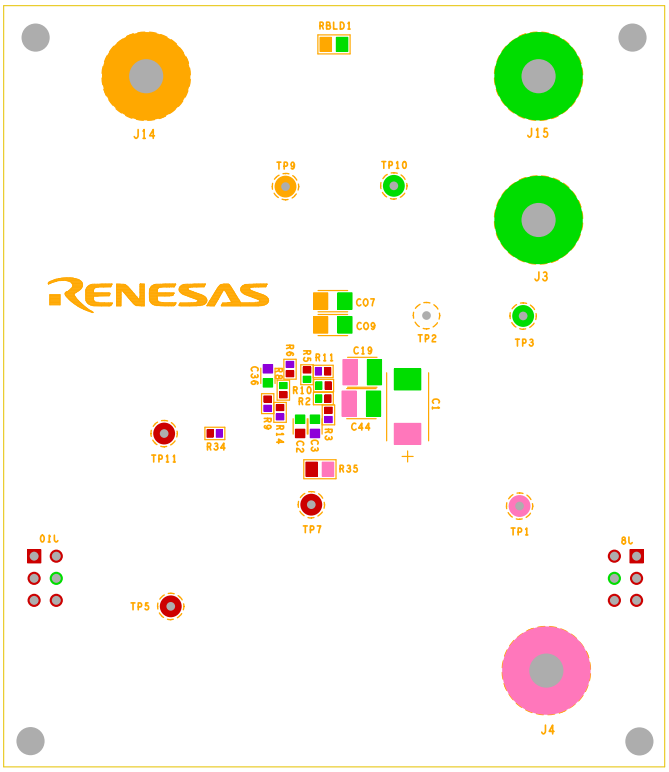

Figure 14. Silkscreen Bottom

4. Typical Performance Data

The following data was acquired using the ISL8282MEVAL1Z evaluation board at +25°C ambient temperature and free air 0LFM. See the "ISL8282M Design Guide Matrix of Typical Applications" table in the ISL8282M datasheet for recommended configurations of different output voltages.

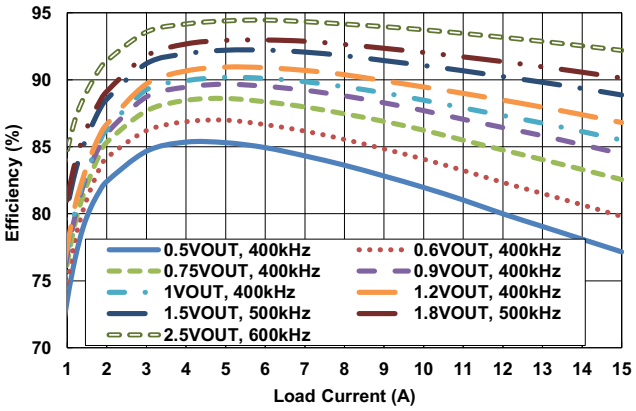

Figure 15. Efficiency vs Load Current at $5V_{IN}$ (PWM)

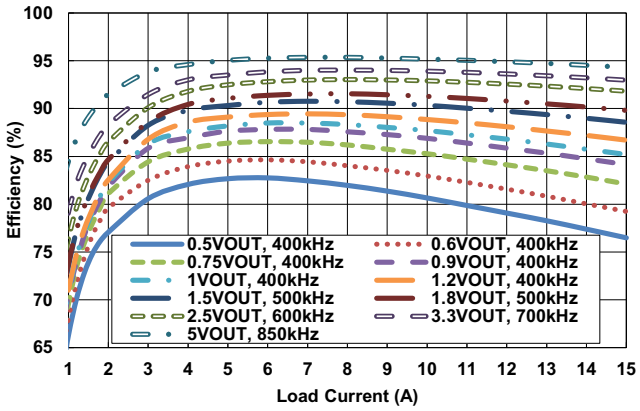

Figure 16. Efficiency vs Load Current at $8V_{IN}$ (PWM)

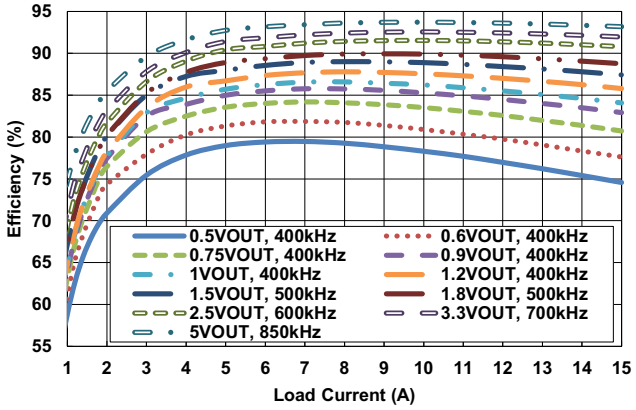

Figure 17. Efficiency vs Load Current at $12V_{IN}$ (PWM)

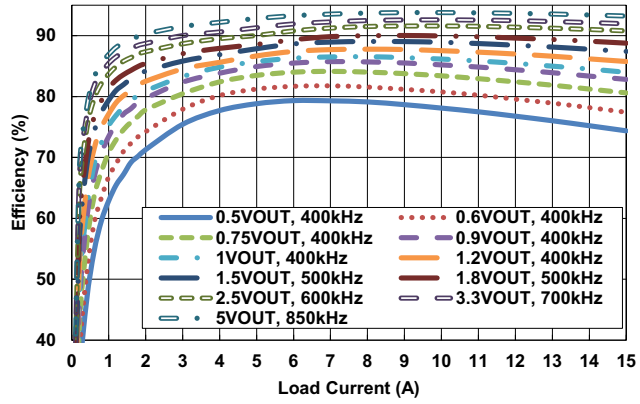

Figure 18. Efficiency vs Load Current at $12V_{IN}$ (PFM)

5. Typical Performance Curves

Operating conditions: V_{IN} = 12V, f_{SW} = 400kHz, AV gain = 49, RR = 200kΩ, C_{OUT} = 4 x 220µF Ceramic, PWM Mode, unless otherwise noted.

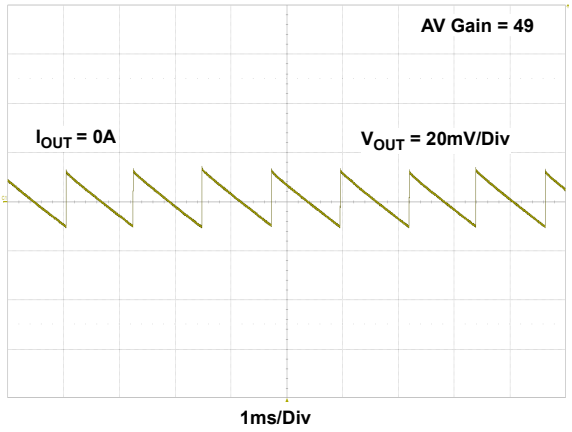

Figure 19. Output Ripple, V_{IN} = 12V, V_{OUT} = 1V, PFM Mode

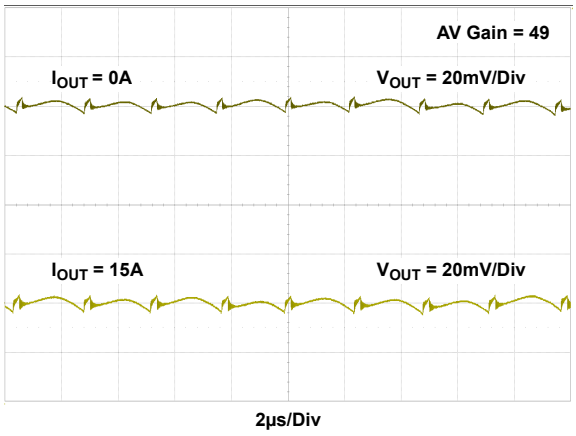

Figure 20. Output Ripple at $12V_{IN}$ and $1V_{OUT}$

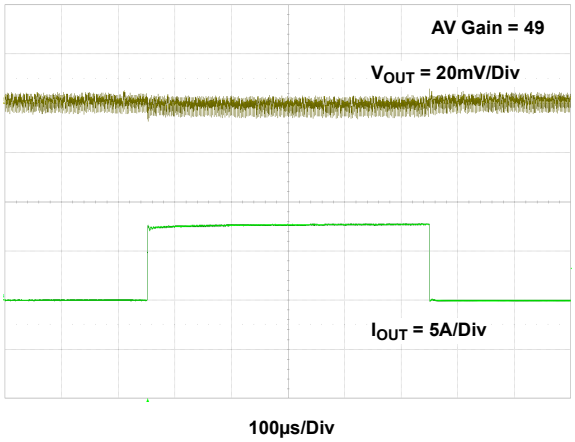

Figure 21. Transient Response, V_{OUT} = 1V, 0A to 7.5A, 7.5A/µs Step Load

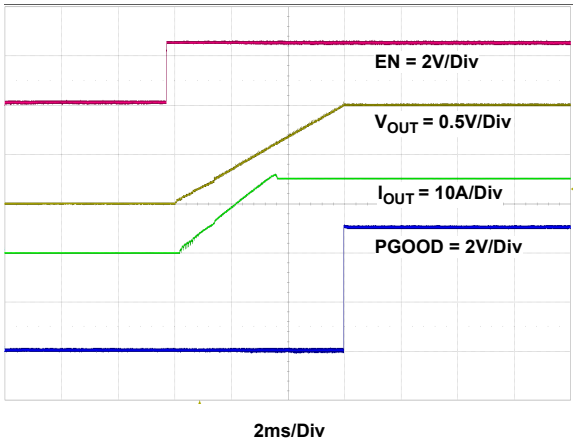

Figure 22. Startup Waveform at I_{OUT} = 15A

Operating conditions: V_{IN} = 12V, f_{SW} = 400kHz, AV gain = 49, RR = 200kΩ, C_{OUT} = 4 x 220µF Ceramic, PWM Mode, unless otherwise noted. **(Continued)**

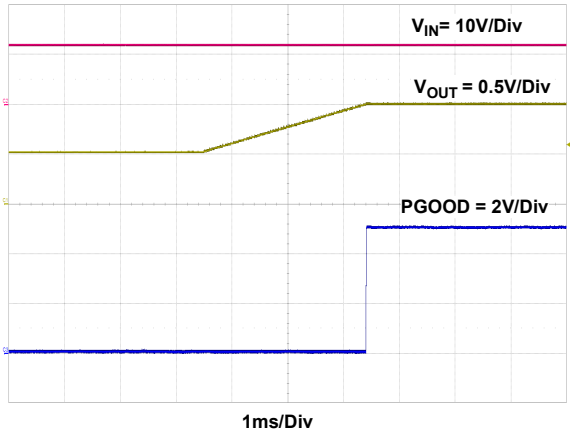

Figure 23. Prebiased Power-Up Waveform, Prebiased Voltage = 0.5V, V_{OUT} = 1V, I_{OUT} = No Load

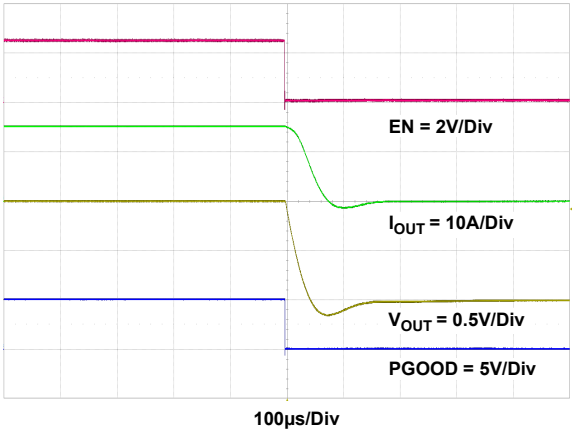

Figure 24. Shutdown Waveform at I_{OUT} = 15A

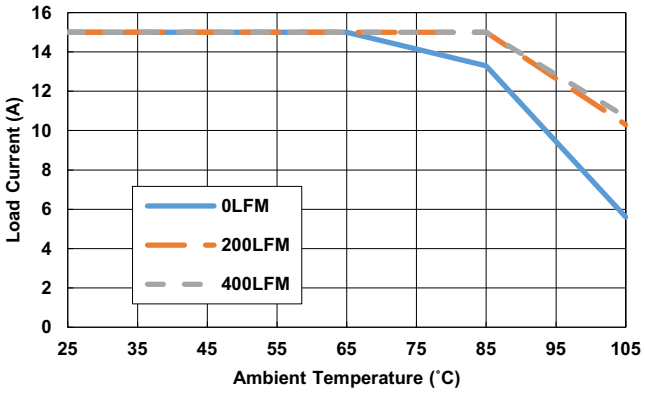

Figure 25. Derating Curve, V_{OUT} = 1V

6. Revision History

Rev.	Date	Description
1.00	Jan 31, 2019	Initial release

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