NEC

Preliminary User's Manual

IE-78K0-NS-P04
IE-1615-NS-EM4

I/O Board and Probe Board

Document No. U13359EE2V0UM00, 2-nd edition
Date Published November 1998

CE

This equipment complies with the EMC protection requirements.

Warning

This is a ´Class A´ (EN 55022: 1994) equipment. This equipment can cause radio frequency noise when used in the residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures under his responsibility.

Caution

This equipment should be handled like a CMOS semiconductor device. The user must take all precautions to avoid build-up of static electricity while working with this equipment. All test and measurement tools including the workbench must be grounded. The user/operator must be grounded using the wrist strap. The In-Circuit Emulator probe target connector plug and/or its adapter pins should not be touched with bare hands.

MS-DOS and MS-Windows are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries.
PC/AT and PC DOS are trademarks of IBM Corp.

The related documents in this publication may include preliminary versions. However, preliminary versions are not marked as such.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

M4 94.11

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 800-366-9782
Fax: 800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

NEC do Brasil S.A.
Sao Paulo-SP, Brasil
Tel: 011-889-1680
Fax: 011-889-1689

Preface

Product Outline

The IE-78K0-NS-P04 and IE-1615-NS-EM4, in combination with the IE-78001-R-A, is used for debugging the following target devices of the 78K/0 series 8-bit single-chip microcontrollers.

- µPD1615 subseries: µPD1615, µPD1616, µPD16F15

Intended Readership

This manual is intended for engineers who perform system debugging using the IE-78001-R-A in combination with the IR-78K0-NS-P04 and IR-1615-NS-RM4.

Engineers reading this manual are assumed to have sufficient knowledge regarding functions and use of the above target devices and the debugger.

Organization

There are four manuals relating to use of the IE-78001-R-A: This manual, supplied with the IE-1615-NS-EM4, the manual supplied with the IE-78001-R-A and the manual supplied with the integrated debugger (Introduction and reference volumes).

IE-78K0-NS-P04 and E-1615-NS-EM4 User's Manual	IE-78001-R-A User's Manual
(Supplied with IE-1615-NS-EM4) Function Outline IE-78K0-NS-P04 Connection Method IE-1615-NS-EM4 Connection Method Emulation Probe Connection Method	(Supplied with IE-78001-R-A) Basic specifications System Configuration External Interface Functions

ID78K0 Integrated Debugger User's Manual - Introduction	ID78K0 Integrated Debugger User's Manual - Reference
(Supplied with Integrated Debugger)	
Simple Method of Use of IE-78001-R-A	Function Outline Command Descriptions Menu Descriptions

Purpose

The purpose of this manual is to explain the basic functions and proper connection method of the IE-78K0-NS-P04 and IE-1615-NS-EM4.

How to Read This Manual

For an understanding of the basic specification

→ Read **Chapter 1 "General"**.

When connecting the IE-78K0-NS-P04 and IE-1615-NS-EM4

→ Read **Chapter 2 "Installation Procedure"** and **IE-78001-R-A User's Manual**.

When setting the clock

→ Read **Chapter 4 "Clock Setting".**

Terminology

Terminology used in this manual is explained in the table below.

Term	Meaning
Emulation device	Generic term for the device performing target device emulation in the emulator. Includes the emulation CPU.
Emulation CPU	CPU section executing the user-written program in the emulator.
Target device	The device which is the object of emulation (real chip).
Target program	The program which is the object of debugging (user-written program).
Target system	The system which is the object of debugging (user-created system). Includes the target program and user-created hardware. In a narrower sense, designates the hardware only.

Note: Explanation of an item marked with Note in the text.
Caution: **Information to be particularly noted.**
Remark: Supplementary information.
Procedure: Procedure for connection, setting, etc.

Related Documents

The documents referred to in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document Number	
		Japanese	English
IE-78001-R-A user's manual		Planned	Planned
IE-78001-R-BK user's manual		Planned	Planned
IE-78K0-NS-P04, IE-1615-NS-EM4 user's manual		—	This manual
IE-78K0-R-Ex1		SUD-T-3677	SUD-T-3677
EP-78230GC-R user's manual		TEMPU-0296	TEMPU-0296
Flashpro programmer user's manual		—	—
ID78K0 integrated debugger user's manual	Introduction	U11649J	—
PC-9800 series (MS-DOS™) base	Reference	U11151J	—
ID78K0 integrated debugger user's manual	Introduction	U11649J	U11649E
IBM PC/AT™ (PC DOS™) base	Reference	U11539J	U11539E

Caution: These documents are subject to change without notice. Be sure to use the latest documents when you design your system.

Contents

1. General 9
1.1 Features 9
1.2 IE-78K0-NS-P04 Components 9
1.3 IE-1615-NS-EM4 Components 9
1.4 External View and Part Names 12
1.5 Target Devices 14
1.6 Emulation Probes 15
1.7 Notes on Use of IE-78K0-NS-P04 and IE-1615-NS-EM4 15

2. Installation Procedure 17

3. Differences from Target Device 26
3.1 Differences in Port Functions 26
3.2 Differences in SFR-Registers 30
3.3 Target Interface Circuit 30

4. Clock Setting 32
4.1 Outline of Clock Setting 32
4.1.1 Main System Clock Selections 33
4.1.2 Subsystem Clock Selections 35
4.2 Main System Clock Setting 36
4.2.1 When Using Standard Clock offered by the Break Board 36
4.2.2 When using Clock mounted by User on the Emulation Board 37
4.2.3 When Using External Clock on the Target Hardware 43
4.2.4 Examples of Main System Clock Setting 45
4.3 Subsystem Clock Setting 46
4.3.1 When Using Standard Clock offered by the Break Board 46
4.3.2 When Using Clock Mounted by User on the Emulation Board 47
4.3.3 When Using External Clock on the Target Hardware 52
4.3.4 Examples of Subsystem Clock Setting 54

Appendix A IE-78K0-NS-P04, IE-1615-NS-EM4 Product Specifications 56

Appendix B Conversion Socket/Conversion Adapter Package Drawings and recommended Board Mounting Pattern 59

Appendix C Pin Correspondence Tables of Emulation Probe 62

1. General

The IE-78K0-NS-P04 is an emulation board for use with the IE-78001-R-A development system for 78K/0 series 8-bit single-chip microcontroller. Combination of this board with the separately available IE-78001-R-A and emulation probe allows efficient emulation of the subseries of µPD1615. The emulation probe with 80 pin GC package target adapter is connected to the probe board (IE-1615-NS-EM4), via the probe extender board (IE-78K0-R-EX1), which is connected to the emulation board (IE-78K0-NS-P04).

1.1 Features

Connecting the IE-78K0-NS-P04 and IE-1615-NS-EM4 to the IE-78001-R-A offers the following features:

(1) Target device peripheral functions (I/O ports, etc.) can be emulated.
(2) I/O port statuses during emulation can be traced.

1.2 IE-78K0-NS-P04 Components

The IE-78K0-NS-P04 comprises the following components. Please check that all these items are included in the package.

(1)	IE 78K0-NS-P04	x 1
(2)	Part holders (with cover)	x 2
(3)	Registration Card	x 1
(4)	Readme First	x 1
(5)	List of Contents	x 1

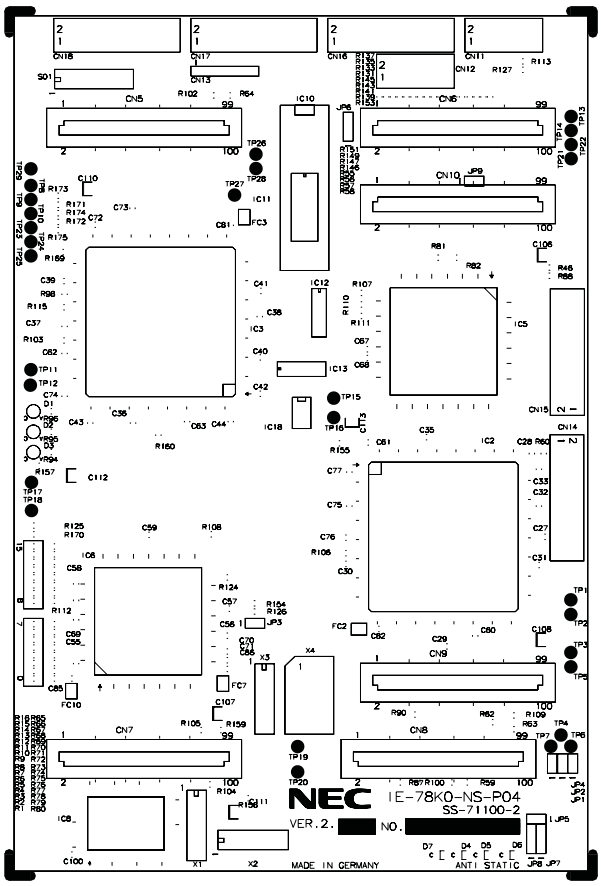
1.3 IE-1615-NS-EM4 Components

The IE-1615-NS-EM4 comprises the following components. Please check that all these items are included in the package.

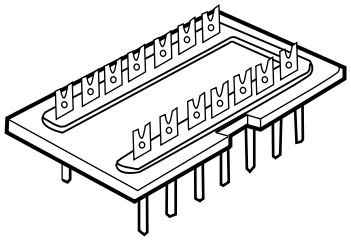
(1)	IE-1615-NS-EM4	x 1
(2)	Screws set	x 1
(3)	Registration Card	x 1
(4)	Readme First	x 1
(5)	List of Attachment	x 1
(6)	Floppy Disk with Device File and FPGA Data	x 1
(7)	User's Manual (this manual)	x 1

Figure 1-1: IE-78K0-NS-P04 Components

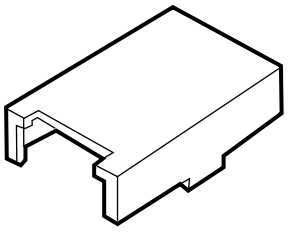
(1) IE-*78K0-NS-P04*



(2) Parts Holder[Note]



Parts Holder Cover



Note: The actual parts holder is supplied with the cover shown on the right fitted.

(3) Screw

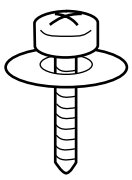
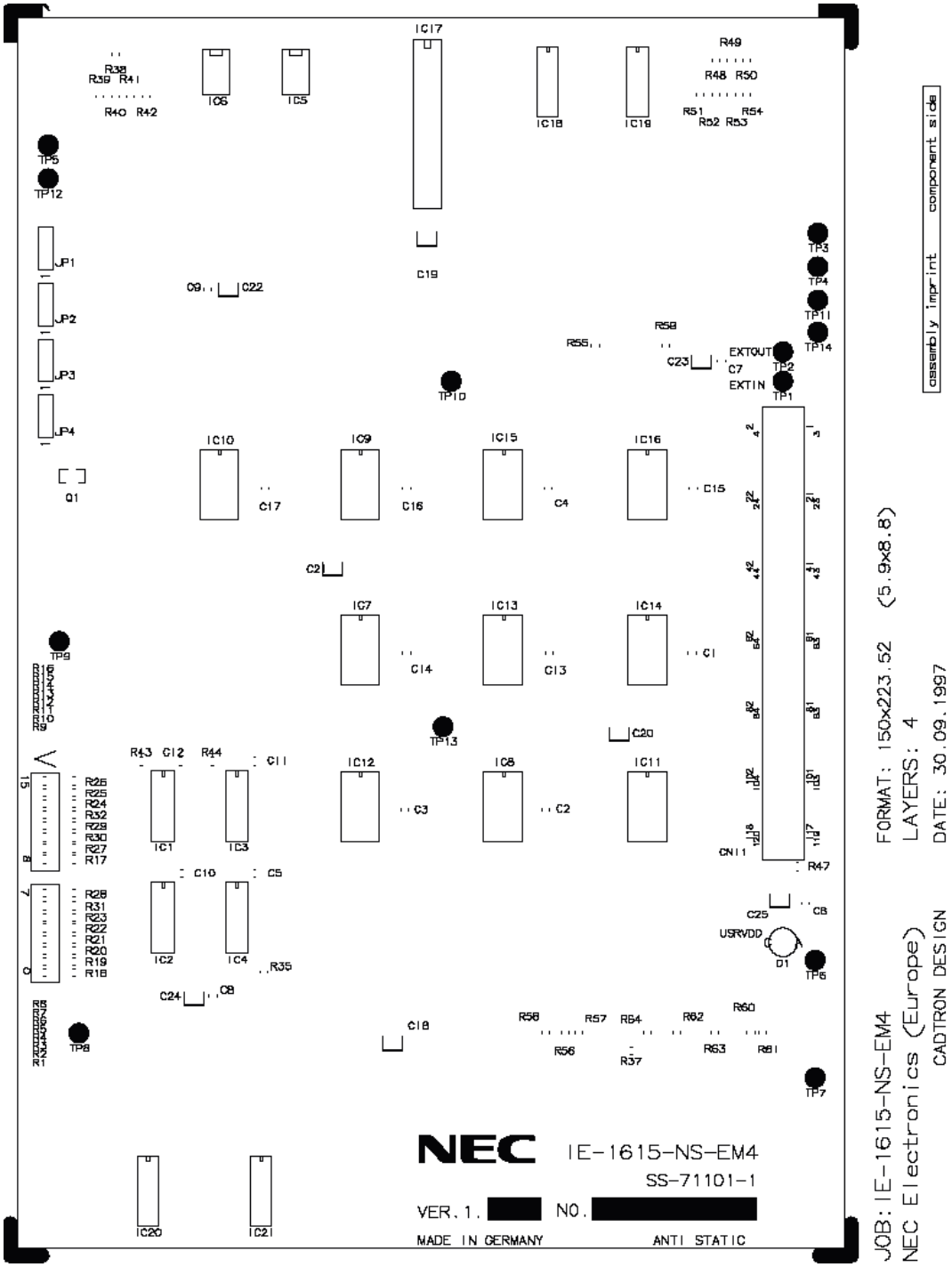
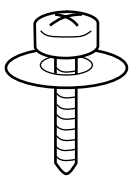


Figure 1-2: IE-1615-NS-EM4 Components

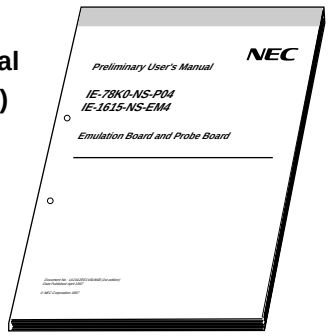
(1) IE-1615-NS-EM4



(2) Screw



(3) User's Manual (This Manual)



1.4 External View and Part Names

Figure 1-3: IE-78K0-NS-P04 External View and Part Names

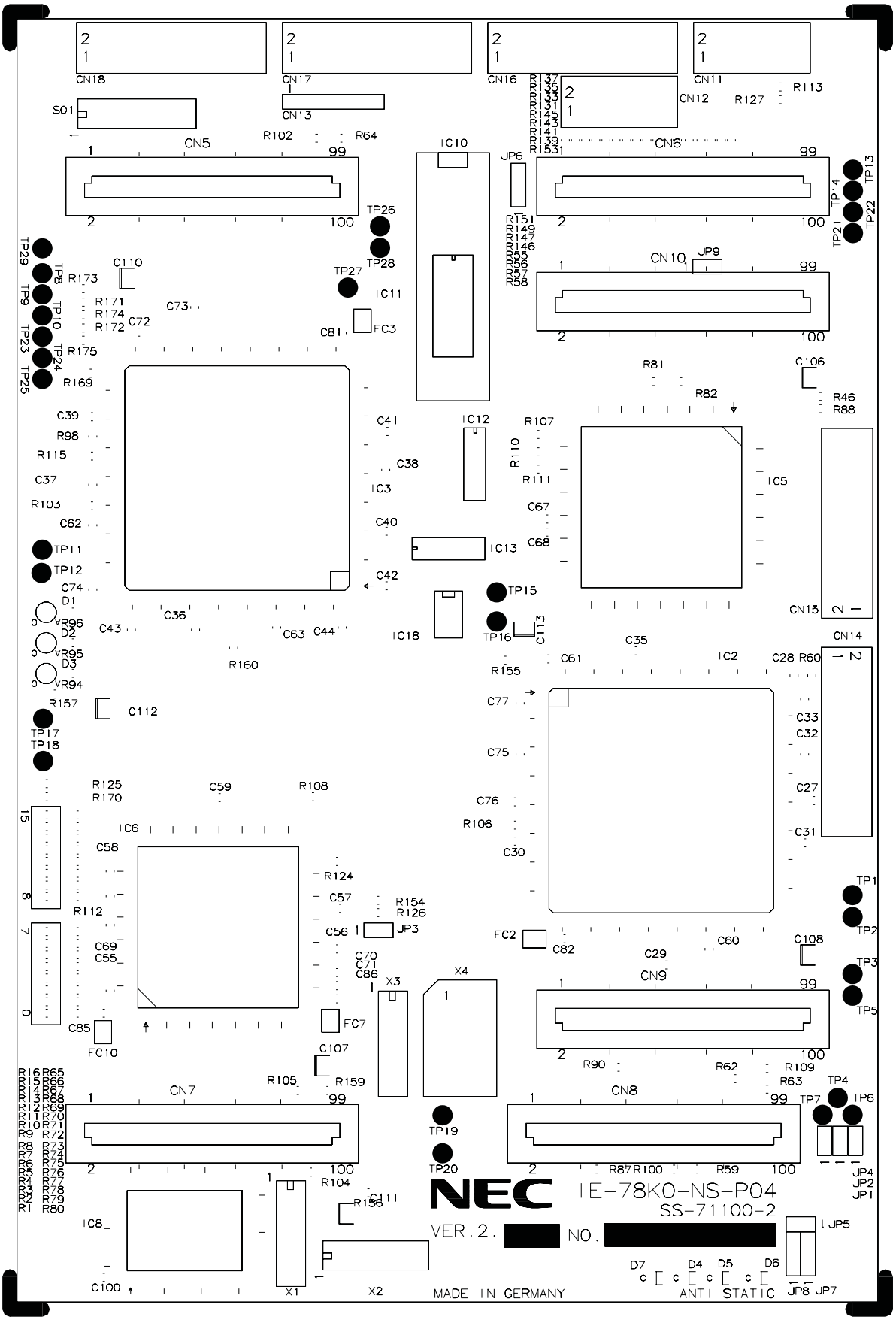


Figure 1-4: IE-1615-NS-EM4 External View and Part Names

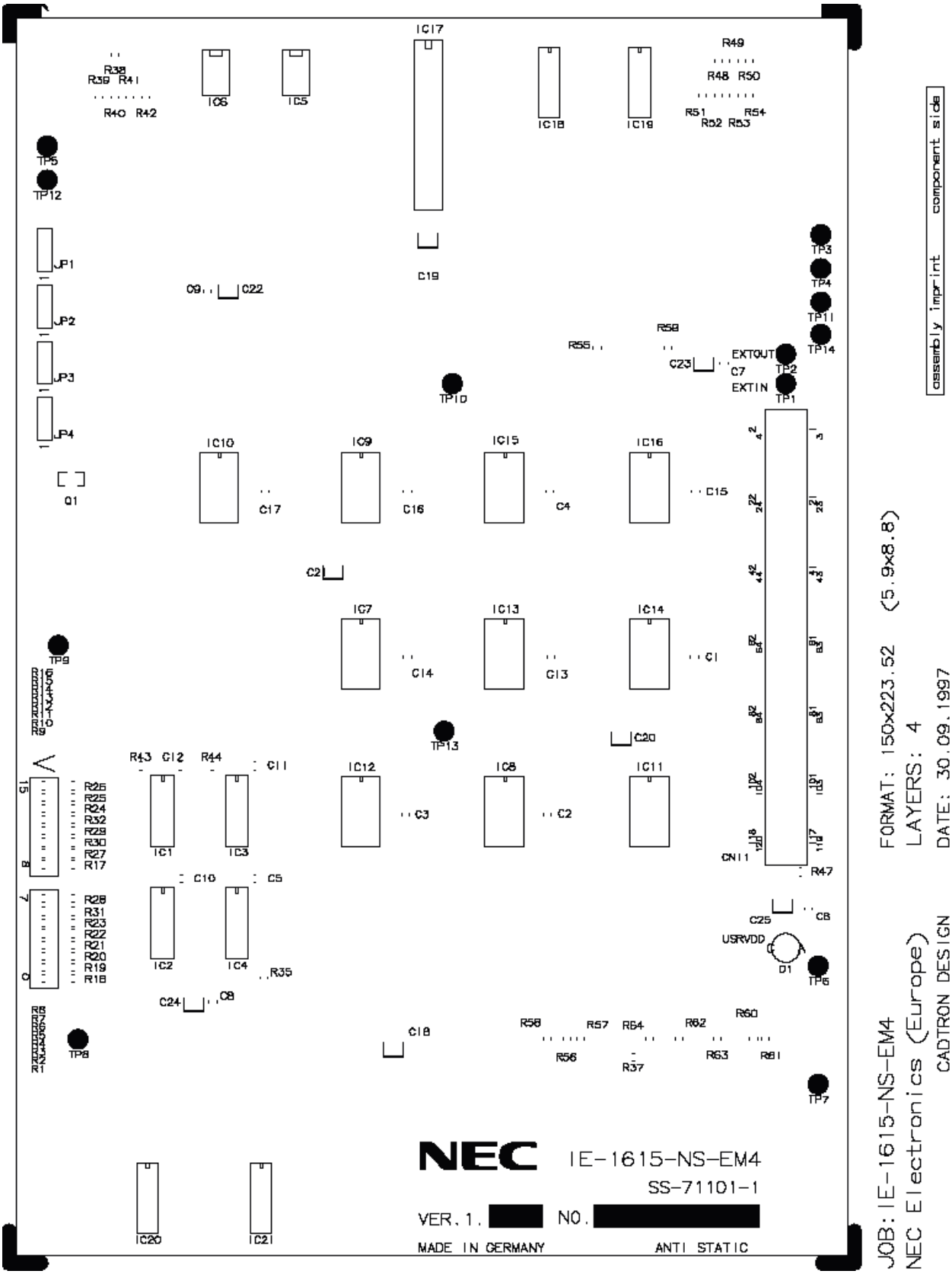


Table 1-1: Names of IE-78K0-NS-P04 and IE-1615-NS-EM4 Parts

Name	Description (IE-78K0-NS-P04)	Name	Description (IE-1615-NS-EM4)
CN1	Break board (IE-78001-R-BK) connectors	CN5	Emulation board connectors (IE-78K0-NS-P04)
CN2		CN6	
CN3		CN7	
CN4		CN8	
CN5	Probe board connectors (IE-1615-NS-EM4)	CN9	
CN6		CN10	
CN7		CN11	Probe connector (EP-78230GC-R)
CN8		JP1	VAN in/out buffer select
CN9		JP2	VAN in/out buffer select
CN10		JP3	VAN in/out buffer select
CN13	FPGA download cable connector (only for internal use by NEC)	JP4	VAN in/out buffer select
CN11	JTAG connector of FPGA (only for internal use by NEC)		
CN12			
CN14	Test connector (only for internal use by NEC)		
CN15			
CN16			
CN17			
CN18			
JP1	Analog Reference Voltage		
JP2	GND-pin of A/D Converter		
JP3	Reserved (only for internal use by NEC)		
JP4	JTAG mode selection (only for internal use by NEC)		
JP5	FPGA mode selection		
JP6	JTAG mode selection (only for internal use by NEC)		
JP7	$LV_{REF}1$		
JP8	$LV_{REF}0$		

1.5 Target Devices

Target devices for which emulation is possible using the IE-78001-R-A in conjunction with the IE-78K0-NS-P04 and the IE-1615-NS-EM4 are shown below. The names of the device files to be installed in development of each product and the names of the CPU series to be input when starting the integrated debugger (ID78K0) are also shown.

Table 1-2: Target Device

Target Device	Device File	CPU Series Name
µPD1615	DF1615.78K	1615
µPD16F15	DF16F15.78K	1615
µPD1616	DF1615.78K	1616

1.6 Emulation Probes

Emulation probes are sold separately.

The appropriate probe should be used for the target device package.

Table 1-3: Emulation Probes and Target Devices

Emulation Probe	Package	Target Device
EP-78230GC-R	80-pin plastic QFP (14 x 14 mm)	µPD1615 µPD16F15 µPD1616

1.7 Notes on Use of IE-78K0-NS-P04 and IE-1615-NS-EM4

(1) Ensure that the power supply for the IE-78001-R-A and the target system is OFF before connecting or disconnecting to/from the IE-78001-R-A and the target device, or changing switch settings, etc.

(2) When carrying out target device emulation using the IE-78K0-NS-P04 and IE-1615-NS-EM4 in conjunction with the IE-78001-R-A, there are certain differences from the operation of the actual device (see **Chapter 3 Differences from Target Device**).

(3) The emulation probe earth clip must be connected to the signal ground line of the target system (please refer to TEMPU-0296).

(4) The target system V_{DD} must be between 4.5 V and 5.5 V.

(5) Power on sequence:
   1. Power on IE-78001-R-A.
   2. Power on target hardware.
   3. Start debugger ID 78K0.

(6) Power off sequence:
   1. Exit from debugger ID 78K0.
   2. Power off target hardware.
   3. Power off IE-78001-R-A.

[Memo]

2. Installation Procedure

This chapter describes the procedure for connecting the following items to the IE-78K0-NS-P04 and IE-1615-NS-EM4 and setting up the 78K/0 series development system.

- The break board (IE-78001-R-BK) installed in the IE-78001-R-A
- The emulation board (IE-78K0-NS-P04) installed on the break board (IE-78001-R-BK)
- The probe board (IE-1615-NS-EM4) installed on the emulation board (IE-78K0-NS-P04)
- The emulation probe (EP-78230GC-R)

The power supply for the IE-78001-R-A and the target system must be OFF when connecting or disconnecting any item.

For the method of connecting the emulation probe and target system, see user's manuals for each emulation probe.

This chapter includes a description which jumper has to be set for using special clocks.

The connection of the IE-78K0-NS-P04 and IE-1615-NS-EM4, break board, IE-78001-R-A, is described below.

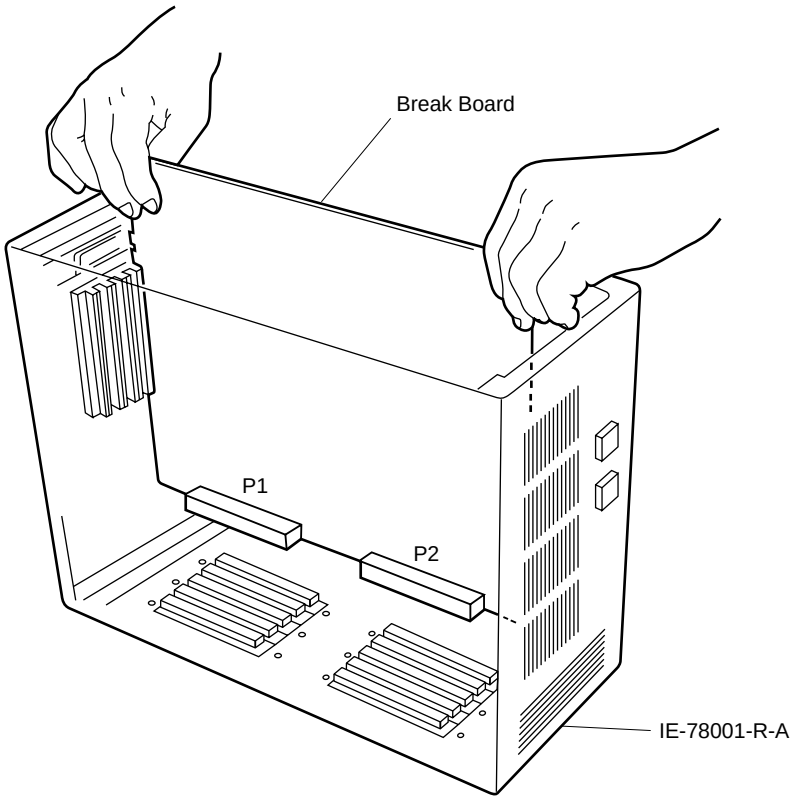
Procedure

<1> Remove the 6 screws in the top of the IE-78001-R-A and open the lid.

<2> Remove the J1 and J2 cables connecting the control/trace board (IE-78001-R-A) and the break board.

<3> Pull forward the card pullers on either side of the break board, and remove the break board from the slot.

Figure 2-1: Removal of Break Board



<4> Set up the break board.

It is necessary to set some jumper and switches on the **break board**. The following tables show the function of each jumper. An example for each jumper setting will be given in **Chapter 4 Clock Setting**.

Jumper JP2 Fixed Internal Main Oscillation Frequency

Table 2-1: Jumper JP2 Fixed Internal Main Oscillation Frequency

Jumper Position	Frequency	Function
(1-2)	20 MHz	Internal clock = 20 MHz
(3-4)	16.77 MHz	Internal clock = 16.77MHz
(5-6)	10 MHz	Internal clock = 10 MHz
(7-8)	8.38 MHz	Internal clock = 8.38 Mhz (**default**)
(9-10)	5 MHz	Internal clock = 5 MHz
(11-12)	4.19 MHz	Internal clock = 4.19 MHz
(13-14)	IOMCK	Fixed clock on IE-K0-NS-P04 board is used
(15-16)	FLASHCK	Fixed clock on real chip board is used

Jumper JP3

Table 2-2: Usage of Clock Doubler

Jumper Position	MCLK	Usage of clock doubler	Function
(1-2)	IF	Clock doubler of µPD780009 used	Selection of JP4 (**default**)
(3-4)	FPGA	Clock doubler of µPD780009 not used	Clock doubler in FPGA (based board)
(5-6)	FLASH		Clock doubler in real chip (realchip based board)

Jumper JP4 Main Clock Selection

Table 2-3: Main Clock Selection

Jumper Position	Main Clock	Function
(1-2)	AUTO	Clock is selected by software (**default**)
(3-4)	CLK I	Clock is selected by JP2
(5-6)	CLK U	User clock is used (from target **or** parts holder on emulation board ref.Chapter 4)

Jumper JP5 Subclock Selection

Table 2-4: Subclock Selection

Jumper Position	Subclock	Function
(1-2)	IOSCK	Internal subclock (IOSCK)
(3-4)	URSCK	User clock is used (from target **or** parts holder on emulation board ref.Chapter 4)
(5-6)	32 kHz	32 kHz subclock (break board) (**default**)

Jumper JP24 FPGA Load Mode

Table 2-5: Downloading Selection

Jumper Position	Function
SERIAL LOAD	Loading FPGA data via serial connector on the BK-board (**default**)
SVLOD	Loading FPGA data via device file

This jumper has to be set to SERIAL LOW independent of the download procedure.

Switch SW1 Voltage Selection

Table 2-6: Voltage Selection

Switch Position	Function
IE	Internal voltage from IE is used (only 5V from IE) (**default**)
USR	Target system power supply is used (variable voltage from target)

There are eight different ways to generate the main clock for the IE. The following table describes the settings of the BK board and the emulation board.

Table 2-7: Clock Selections

Main system clock frequency	Setting clock on ID configuration	IE-78001-R-BK	IE-780948-SL-EM1
4.19 Mhz: BK Board Clock	Internal	JP2: short11-12 JP3: short 1-2 JP4: short 1-2	Don't care
5 Mhz: BK Board Clock	Internal	JP2: short 9-10 JP3: short 1-2 JP4: short 1-2	Don't care
8.38 Mhz: BK Board Clock	Internal	JP2: short 7-8 JP3: short 1-2 JP4: short 1-2	Don't care
10 Mhz: BK Board Clock (not allowed)	Internal	JP2: short 5-6 JP3: short 1-2 JP4: short 1-2	Don't care
16.77 Mhz: BK Board Clock (not allowed)	Internal	JP2: short 3-4 JP3: short 1-2 JP4: short 1-2	Don't care
20 Mhz: BK Board Clock (not allowed)	Internal	JP2: short 1-2 JP3: short 1-2 JP4: short 1-2	Don't care
Clock on Emulation Board (parts holder)	External	JP2: don't care JP3: short 1-2 JP4: short 5-6	Please refer to chapter 4
Clock on Target Board (user hardware)	External	JP2: don't care JP3: short 1-2 JP4: short 5-6	Please refer to chapter 4

<5> When a user clock is used, mount the main system clock to the emulation board and the subsystem clock to the emulation board too, using a parts holder (See **Chapter 4 Clock Setting**).

<6> Setup **the I/O board**

It is necessary to set some jumper and switches on the I/O board. The following tables describe the function of each jumper.

Table 2-8: FPGA Mode Selection

Jumper JP5

Jumper Position	M-FSW	Function
close	GND	Reserved
open	Pull-up	Internal use **(default)**

Ground Voltage Pin of AD-Converter

Table 2-9: Ground Voltage Pin of AD-Converter

Jumper JP2

Jumper Position	AAVSS	Function
open	target	Connected to selected ground base **(default)**
closed	GND	Internal digital ground

VCC Voltage Pin of AD-Converter

Table 2-10: VCC Voltage Pin of AD-Converter

Jumper JP1

Jumper Position	AAVREF0	Function
open	target	Connected to selected voltage **(default)**
closed	VCC	Internal digital VCC

Voltage Setting

Table 2-11: Voltage Setting

Jumper JP8

Jumper Position		Function
(1 – 2)	V_{CC}	For internal testing
(2 – 3)	LV_{DD}	For internal testing **(default)**

Voltage Setting

Table 2-12: Voltage Setting

Jumper JP7

Jumper Position		Function
(1 – 2)	Vcc	For internal testing
(2 – 3)	LV_{DD}	For internal testing (**default**)

Table 2-13: LED Indicator D1, D2, D3

LED	Condition	Function
LED1 green	blinking	FPGA downloading ongoing
LED1 green	on	FPGA download complete
LED1 green	off	FPGA not programmed
LED2 yellow	blinking	not used
LED2 yellow	on	VCC on
LED2 yellow	off	VCC off
LED3 red	blinking	reserved
LED3 red	on	reserved
LED3 red	off	reserved

<7> Setup the probe board

It is necessary to set a jump on the **probe board**.The following table discribes the function each jump.

VAN serial in/out buffer type selection

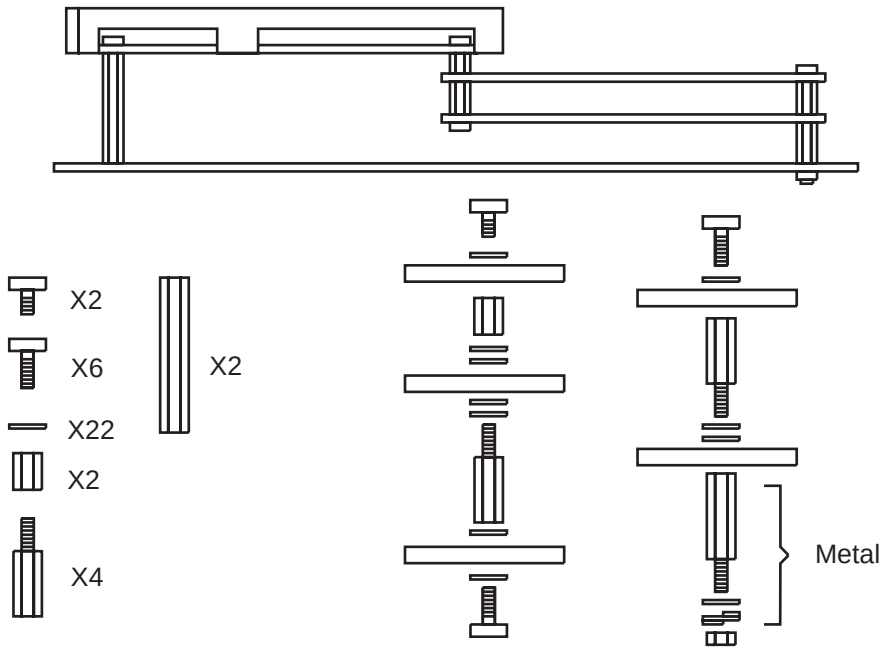
Table 2-14: **VAN serial in/out**

Jumper JP1 to JP4

Jumper Position		Function
(1 – 2)	Pin Emulator	Original buffer type (**default)**
(2 – 3)	FPGA	Buffer type different / timing optimized

<8> Connect all boards to the mother-board slots in the IE-78001-R-A housing (the break board in the 1-st slot from the right).

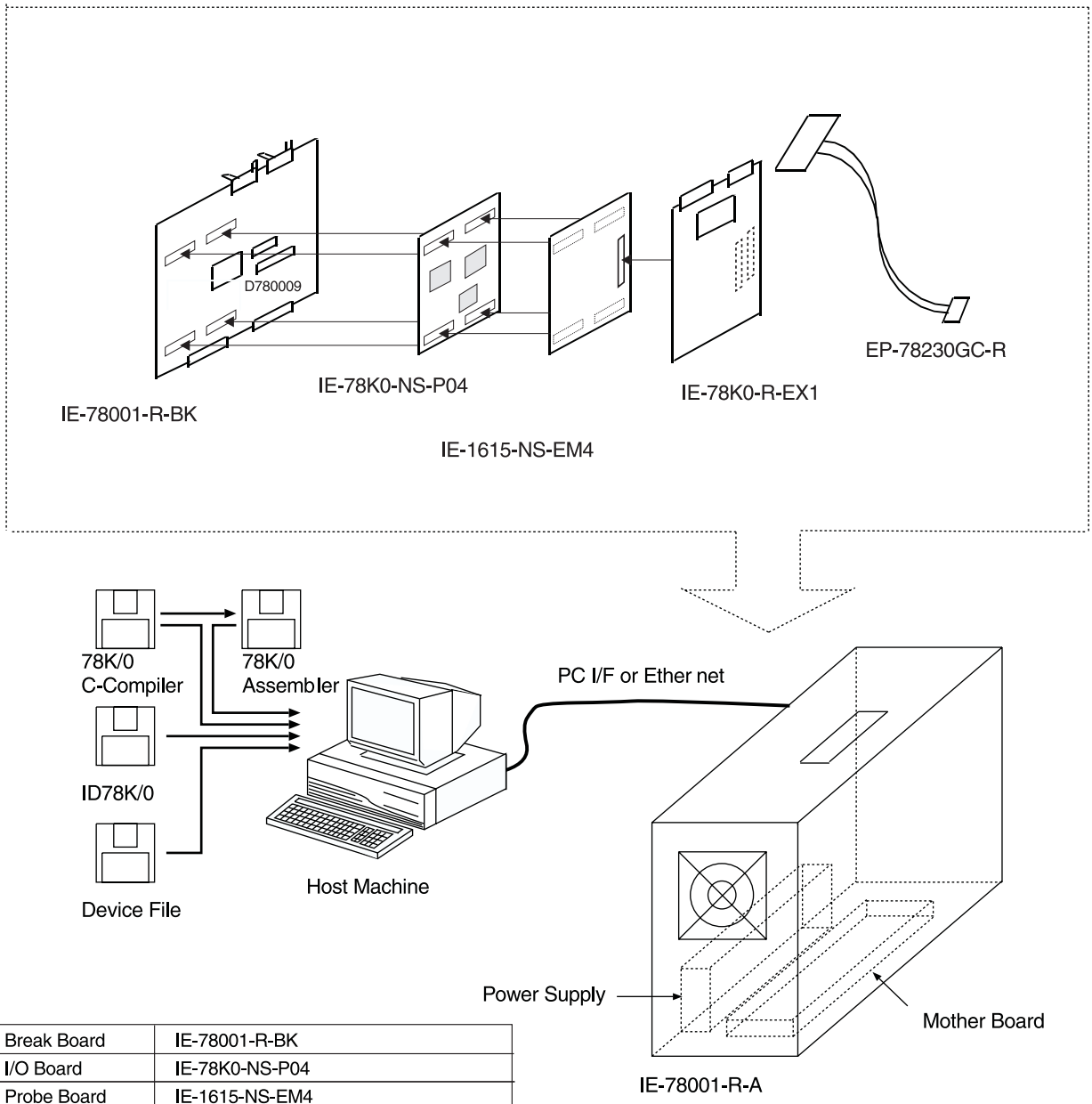
Figure 2-2: Emulation boad assembling with screw set



<9> Re-connect the J1 and J2 cables in their original positions.

<10>Check the position of the boards, then close the lid.

Figure 2-3: Connections of Boards



Break Board	IE-78001-R-BK
I/O Board	IE-78K0-NS-P04
Probe Board	IE-1615-NS-EM4
Extender Board	IE-78K0-R-EX1
Emulation Probe	EP-78230GC-R
Device File(s)	D16F15.78K / D1615.78K / D1615.78K

[Memo]

3. Differences from Target Device

When target device emulation is performed using the IE-78K0-NS-P04 and IE-1615-NS-EM4 in conjunction with the IE-78001-R-A, there are certain differences from the operation of the actual target device. These differences are described in this chapter.

3.1 Differences in Port Functions

(1) Port 4, 8, 9, 10, 11, 12.0, 12.4 and 12.6 of the device are a normal CMOS inputs with no hysteresis. The emulator has pins with hysteresis.

(2) The LCD-segment signals S0-S39 are in/out ports of type 17A/17B at the device. The emulator drives these signals by an analog switch.

3.1.1 Port related Signals

Figure 3-1: Port 0, Port 1 (digital), Port 2, Port 4 (without 4.7)

Figure 3-2: Port 4.7

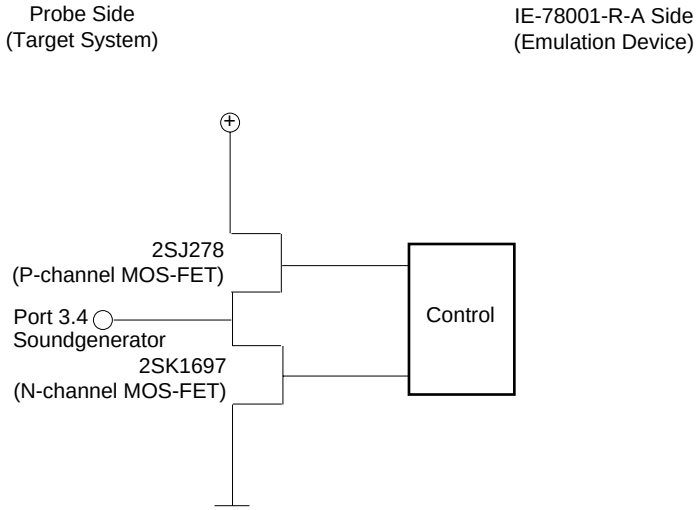
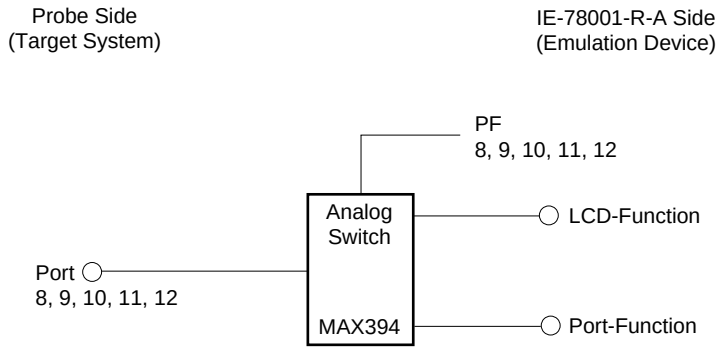
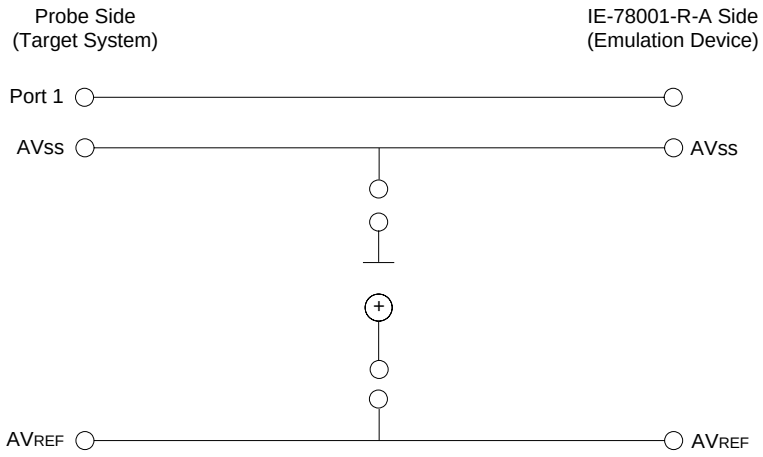


Figure 3-3: Port 8, 9, 10, 11, 12



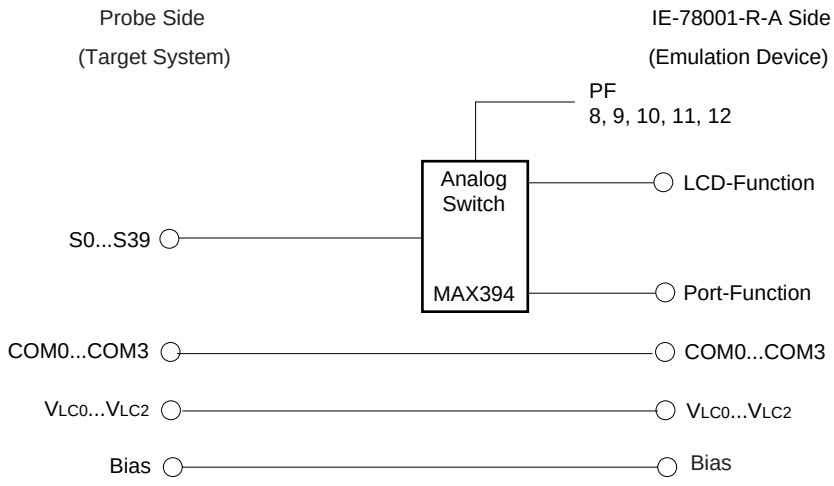
3.1.2 Analog related Signals

Figure 3-4: Analog related Signals



3.1.3 LCD related Signals

Figure 3-5: LCD related Signals

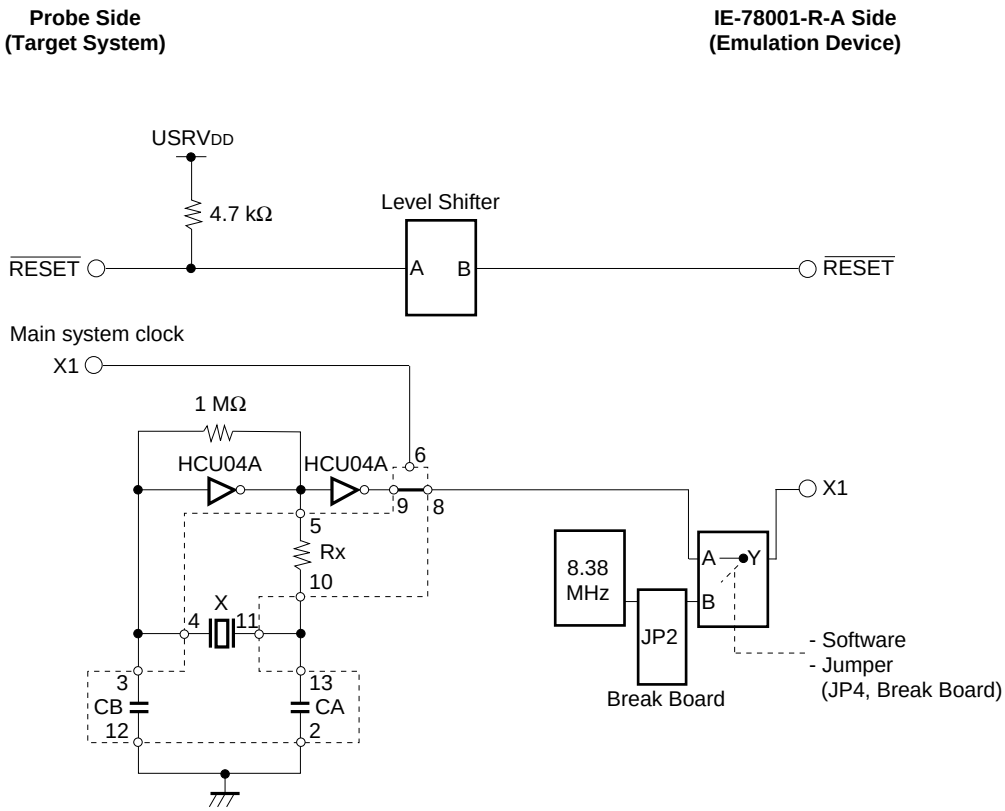


3.1.4 Circuits which input Signals to/from Emulation Device

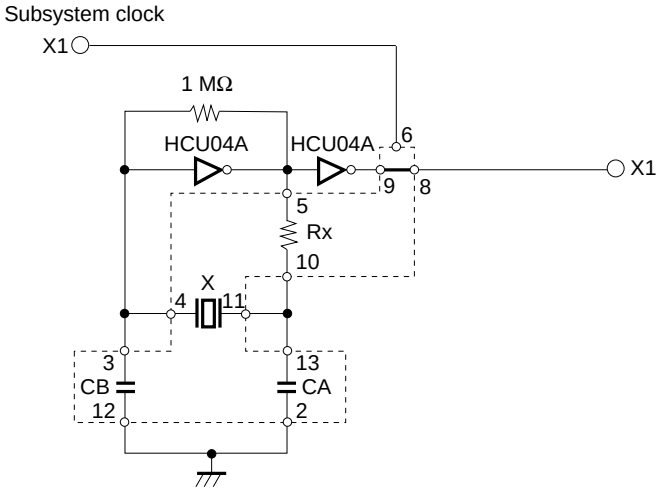
These circuits interface the following signals:

- $\overline{\text{RESET}}$ signal
- Clock input related signals

Figure 3-6: Emulation Circuit Equivalent Circuit Diagram



Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.



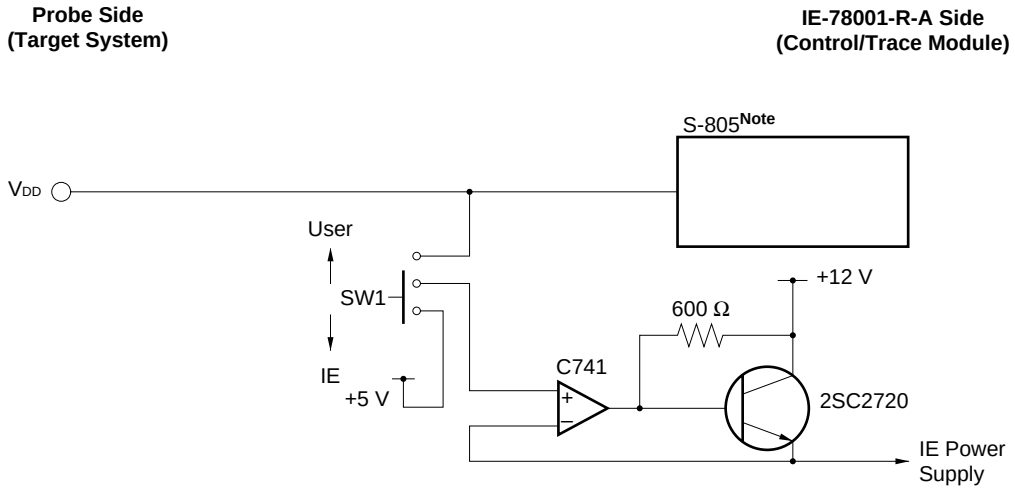
Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

3.1.5 Circuits which input Signals to Control/Trace Module

These circuit interfaces the following signals:

- V_{DD} signal

Figure 3-7: Emulation Circuit Equivalent Circuit Diagram



Note: The S-805 is an IC manufactured by Seiko Electronics Industries, Inc.

3.2 Differences in SFR-Registers

Caution: 1. The emulator has a register to emulate the powerfail detection which is not existing at the real chip. The name of the register is DAM0 (SFR-Adr: 0xFF9C). This register has to be set to the value 0x01 by the user-program.

2. The emulator has a register for the emulation of the LCD-function. The name of the register is LCDTM (SFR-Adr: 0xFF4A). This register has to be set to the value 0x02 by the user-program.

3.3 Target Interface Circuit

The purpose of the target interface circuit is to have the same operations as the target device performed in the IE-78001-R-A. It comprises the emulation device and various gates (CMOS, TTL and other ICs).

When debugging is performed with the target system connected to the IE-78001-R-A, the IE-78001-R-A target interface circuit performs emulation as though the actual target device were operating in the target system.

The target device has a CMOS LSI configuration. The target interface circuit emulation device also has a CMOS LSI configuration, and is virtually identical to the target device in terms of DC characteristics and AC characteristics (when operating on V_{DD} = 4.5 to 5.0 V).

However, where emulation device signal input/output is performed via gates in the target interface circuit, DC and AC characteristics differ from those of the target device.

In particular, regarding AC characteristics, there is a gate delay time (which differs from gate to gate) each time a gate is passed through.

The above points must be taken into consideration when designing the target system.

Caution: When the IE-78001-R-A and IE-78K0-NS-P04 and IE-1615-NS-EM4 are connected to the target system, 4.5 to 5.5 V must be supplied as the target system power supply (V_{DD}).

[Memo]

4. Clock Setting

This chapter describes the clock setting method.

4.1 Outline of Clock Setting

The main system clock for use in debugging can be selected from (1) to (3) below.
The subsystem clock can be selected from (1) to (3), too.

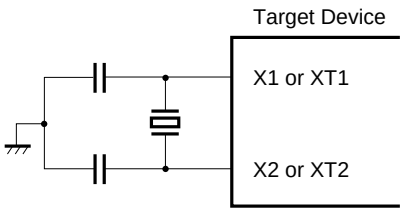
(1) Standard clock offered by the break board
(2) Clock mounted by the user on the emulation board
(3) External clock on the target hardware

If an internal clock is incorporated in the target system, (1) “Clock mounted on the break board” or (2) “Clock mounted by the user” should be selected. An internal clock means the use of an oscillator in the target device with a resonator connected to the target device. The external circuit is shown in Figure 4-1(a). The resonator mounted in the target system is not used during emulation. The clock mounted on the emulation board installed in the IE-78001-R-A is used.

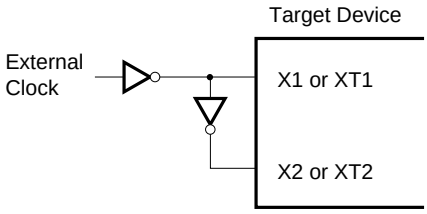
If an external clock is incorporated in the target system, (3) “External clock” should be selected. An external clock means supplying a clock from outside the target device, and the oscillator in the target device is not used. The external circuit is shown in Figure 4-1(b).

Figure 4-1: System Clock Oscillator External Circuit

(a) Internal Clock



(b) External Clock

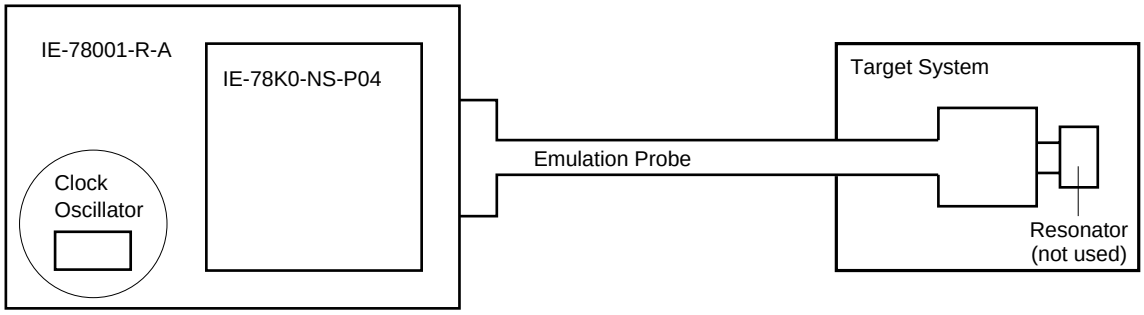


4.1.1 Main System Clock Selections

(1) Standard clock offered by the break board

A crystal oscillator is already mounted on the break board. The frequency is 8.38 MHz.

Figure 4-2: When Using Standard Clock Mounted on Break Board

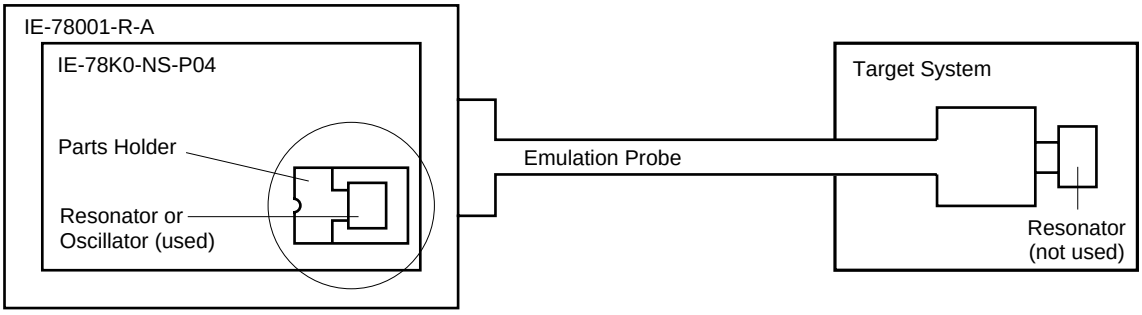


Remark: The clock supplied from the oscillator on the IE-78001-R-BK (circled) is used.

(2) Clock mounted by user on the emulation board

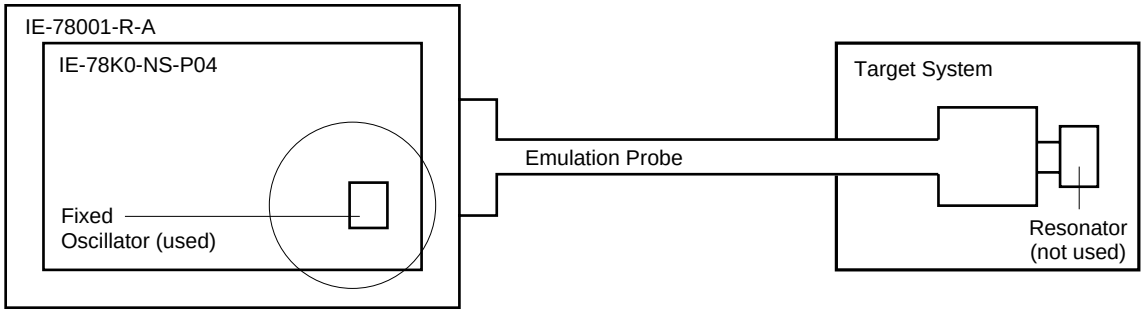
A clock that matches the specifications set by the user can be mounted on the IE-78K0-NS-P04. The resonator or oscillator to be used is mounted on a parts holder and that parts holder is installed on the IE-78K0-NS-P04. This is useful if you want to perform debugging at a different frequency from that of the clock mounted beforehand.

Figure 4-3: When Using Clock Mounted on the Emulation Board



Remark: The clock supplied from the resonator or oscillator on the IE-78K0-NS-P04 (circled) is used.

Figure 4-4: Using a fixed Clock mounted by the User on the Emulation Board

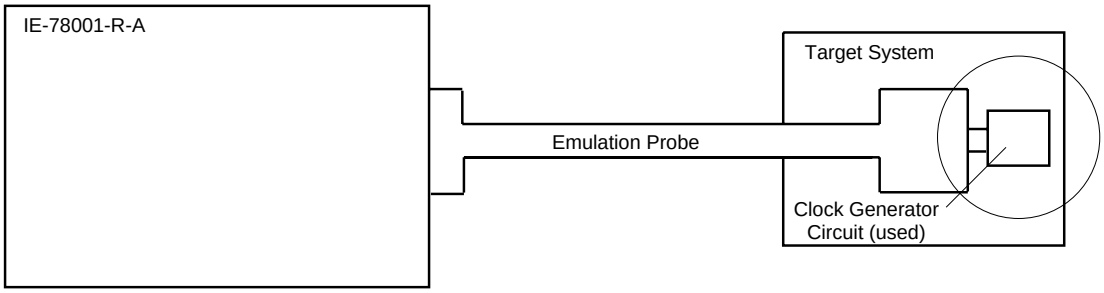


Remark: The clock supplied with the oscillator on the IE-78K0-NS-P04 (circled in the above figure) is used. The frequency is 8.00 MHz.

(3) External clock on the target hardware

The external clock on the target system can be used via an emulation probe.

Figure 4-5: Using an External Clock mounted on the Target Hardware



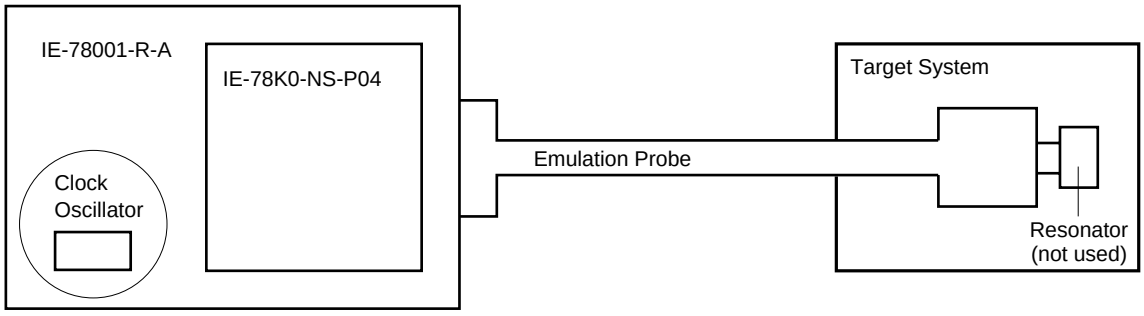
Remark: The clock supplied by the clock generator circuit (circled in the above figure) is used.

4.1.2 Subsystem Clock Selections

(1) Standard clock offered by the break board

A crystal oscillator is already mounted on the break board. The frequency is 32.768 kHz.

Figure 4-6: When Using Standard Clock Mounted on Break Board

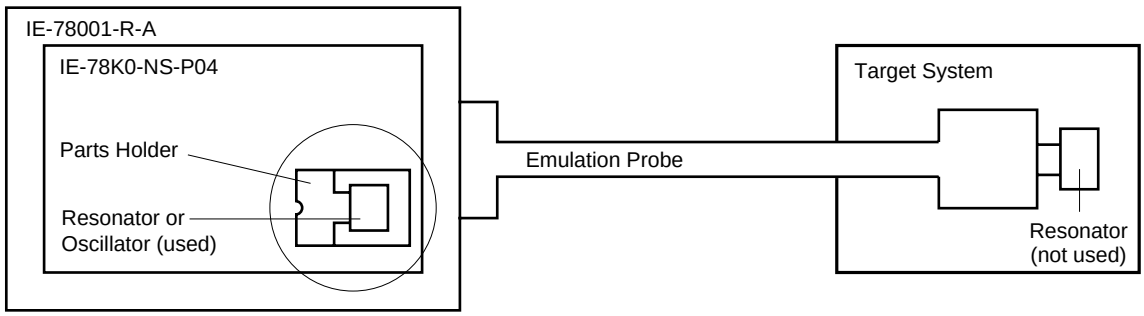


Remark: The clock supplied from the oscillator on the IE-78001-R-BK (circled) is used.

(2) Clock mounted by user on the emulation board

A clock that matches the specifications set by the user can be mounted on the IE-78K0-NS-P04. The resonator or oscillator to be used is mounted on a parts holder and that parts holder is installed on the IE-78K0-NS-P04. This is useful if you want to perform debugging at a different frequency from that of the clock mounted beforehand.

Figure 4-7: When Using Clock Mounted on the Emulation Board

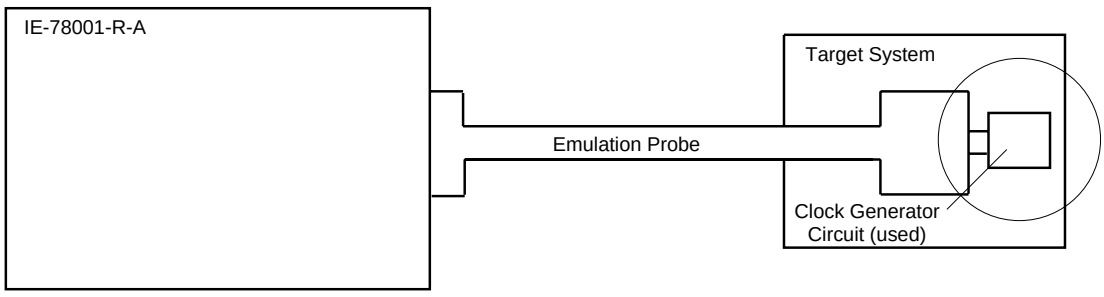


Remark: The clock supplied from the resonator or oscillator on the IE-78K0-NS-P04 (circled) is used.

(3) External clock on the target hardware

The external clock on the target system can be used via an emulation probe.

Figure 4-8: Using an External Clock mounted on the Target Hardware



Remark: The clock supplied by the clock generator circuit (circled in the above figure) is used.

4.2 Main System Clock Setting

It is not necessary to change the parts holder (IC29, X1 (MAIN)) on the breakboard IE-78001-R-BK.

4.2.1 When Using Standard Clock offered by the Break Board

A parts holder, wired as shown in Figure 4-9, is fitted in the X2 socket on the IE-78K0-NS-P04 when the product is shipped. If the parts holder state is the same as when the product was shipped, no particular hardware settings are necessary.

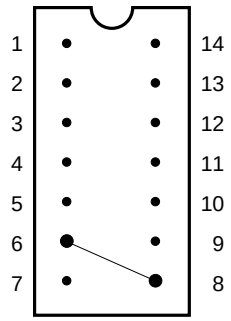
When the integrated debugger (ID78K0) is started, clock should be set to "INTERNAL" in the configuration window clock selection.

Items to be prepared

- Parts holder (IE-78K0-NS-P04 accessory)
- Lead wire
- Set of soldering tools

Procedure

Figure 4-9: Lead Wiring Diagram (When Clock mounted on Break Board is used as Main System Clock)



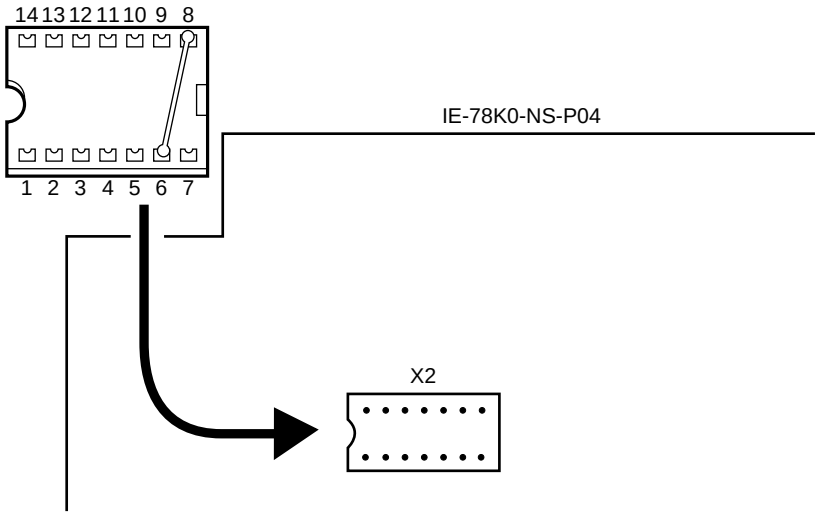
Parts Holder Inter-Pin Numbers
6-8

<1> Check the break board and the IE-78K0-NS-P04.

<2> Insert parts holder in the socket (marked "X2") on the IE-78K0-NS-P04. Ensure that the pin <1> mark is correctly oriented when inserting the parts holder.

<3> Confirm that the component mounted on the X1 (MAIN) socket on the break board is wired as shown in Figure 4-9.

Figure 4-10: Parts Holder Mounting Location (When Clock mounted on the Break Board is used as Main System Clock)



<5> Install the IE-78K0-NS-P04 and the other boards in the IE-78001-R-A.

4.2.2 When using Clock mounted by User on the Emulation Board

The settings shown in (1) or (2) below must be performed depending on the type of clock used. When the integrated debugger ID78K0 is started, clock should be selected to “INTERNAL” in the configuration window (clock selection).

(1) When ceramic resonator/crystal resonator is used

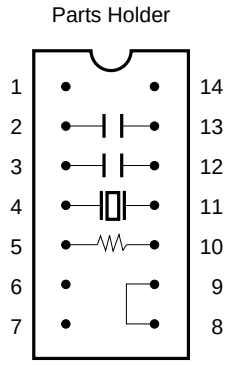
Items to be prepared

- Parts holder (IE-78K0-NS-P04 accessory)
- Ceramic resonator or crystal resonator
- Resistor Rx
- Capacitor CA
- Capacitor CB
- Set of soldering tools

Procedure

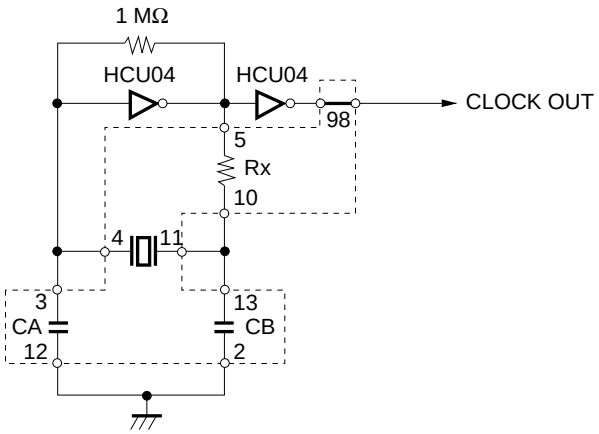
<1> Solder the ceramic resonator or crystal resonator to be used and resistor Rx, capacitor CA and capacitor CB appropriate to the oscillation frequency of the resonator to the parts holder provided as shown below.

Figure 4-11: Soldering of Parts to the Parts Holder



Pin No.	Connection
2-13	Capacitor CB
3-12	Capacitor CA
4-11	Ceramic resonator/crystal resonator
5-10	Resistor Rx
8-9	Shorted

Figure 4-12: Circuit Diagram



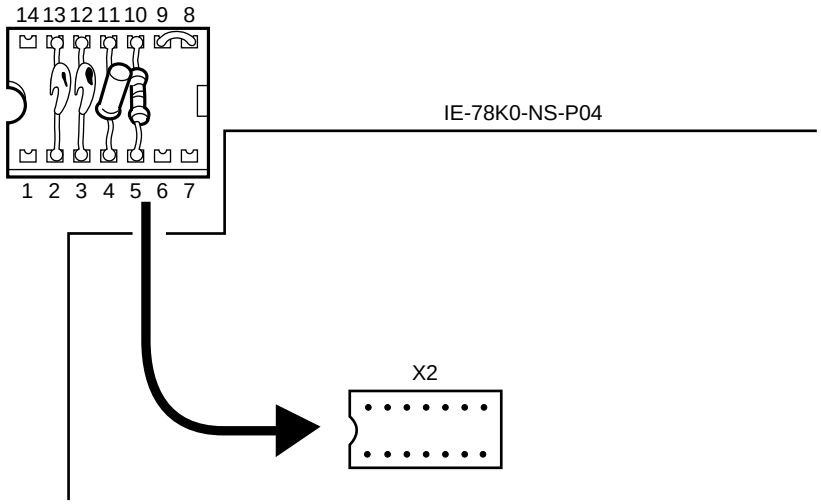
Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

<2> Prepare the break board (jumper settings) and the IE-78K0-NS-P04.

<3> Remove the external clock parts holder inserted in the socket (marked “X2”) on the IE-78K0-NS-P04.

<4> Insert parts holder <1> in the socket (X2) from which the external clock parts holder was removed in <3>. Ensure that the pin 1 mark is correctly oriented when inserting the parts holder.

Figure 4-13: Parts Holder Mounting Location (When Clock mounted by User on the Emulation Board is used as Main System Clock)

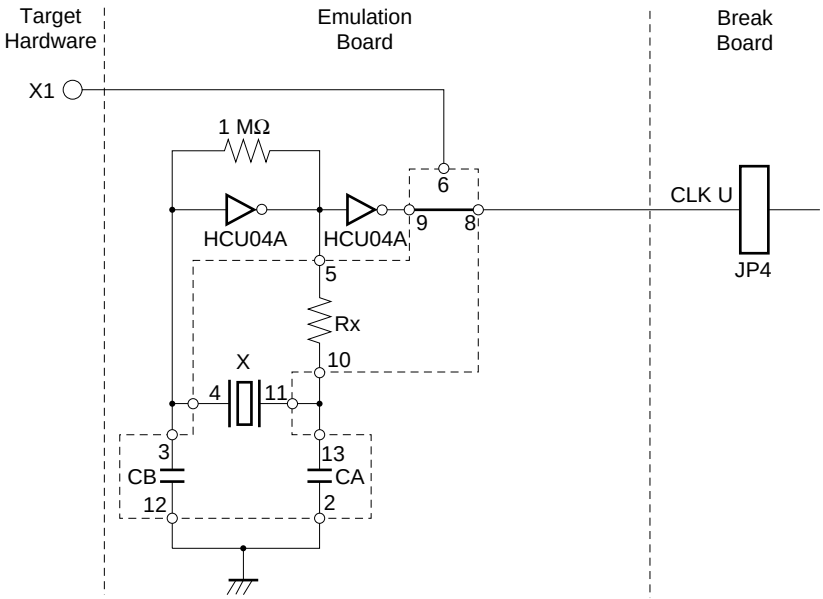


<5> Confirm that the component mounted on the X1 (MAIN) socket on the break board is wired as shown in Figure 4-5.

<6> Install the IE-78K0-NS-P04 and the other board in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock to be supplied to the emulation device from the mounted resonator.

Figure 4-14: Clock Enabling



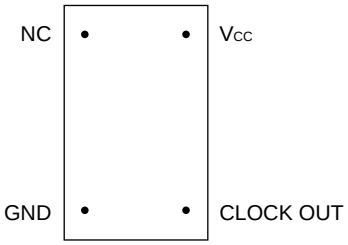
Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

(2) When crystal oscillator is used

Items to be prepared

- Crystal oscillator (with pins as shown in Figure 4-15)

Figure 4-15: Crystal Oscillator (When Clock mounted by User on the Emulation Board is used as Main System Clock)



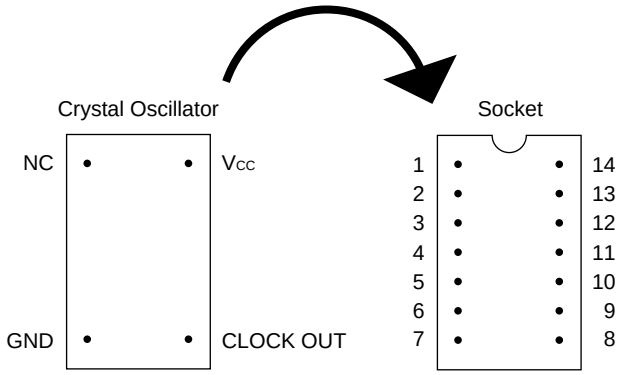
Procedure

<1> Prepare the break board (jumper settings) and the IE-78K0-NS-P04.

<2> Remove the external clock parts holder inserted in the socket (marked “X2”) on the IE-78K0-NS-P04.

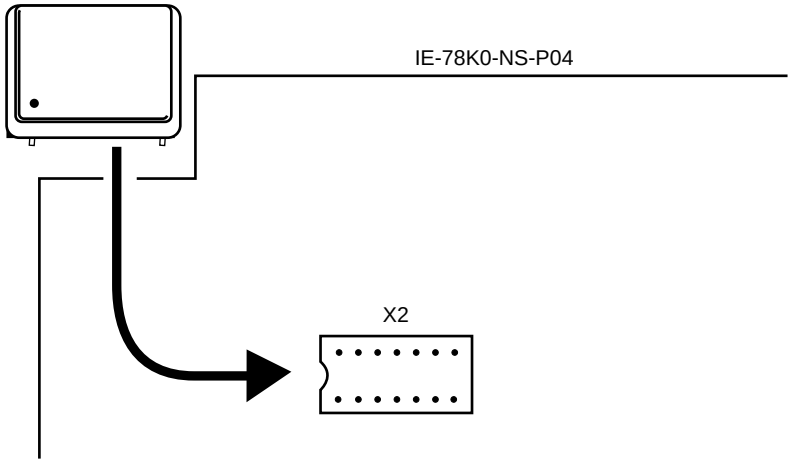
<3> Insert the crystal oscillator in the socket (marked "X2") from which the external clock parts holder was removed in <2>. The crystal oscillator pins should be inserted in the socket holes as shown in Figure 4-16.

Figure 4-16: Insertion of Crystal Oscillator in the Socket



Crystal Oscillator Pin	Socket Hole No.
NC	1
GND	7
CLOCK OUT	8
VCC	14

Figure 4-17: Crystal Oscillator Mounting Location (When Clock mounted by User on the Emulation Board is used as Main System Clock)

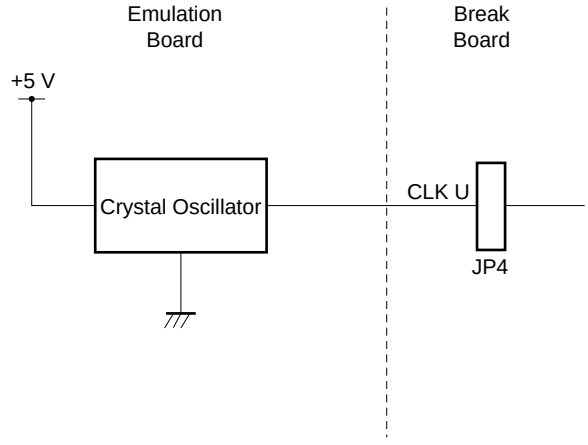


<4> Confirm that the component mounted on the X1 (MAIN) socket on the break board is wired as shown in Figure 4-5.

<5> Install the IE-78K0-NS-P04 and the other board in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock to be supplied to the emulation device from the mounted oscillator.

Figure 4-18: Clock Enabling



(3) When fixed oscillator on the emulation board is used

Procedure

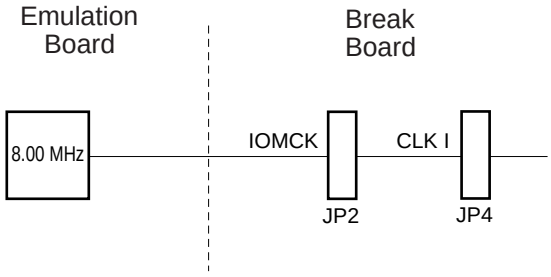
<1> Prepare the break board (jumper settings).

<2> Confirm that the component mounted on the X1 (main) socket on the break board is wired as shown in Figure 4-5.

<3> Install the IE-78K0-NS-P04 and the other board in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock to be supplied to the emulation device from the oscillator mounted fixed on the emulation board.

Figure 4-19: Fixed Oscillator



4.2.3 When Using External Clock on the Target Hardware

A parts holder, wired as shown in Figure 4-20, is fitted in the X2 socket on the IE-78K0-NS-P04 when the product is shipped. If the parts holder state is the same as when the product was shipped, no particular hardware settings are necessary.

When the integrated debugger ID78K0 is started, clock should be set to "EXTERNAL" in the configuration window (clock selection).

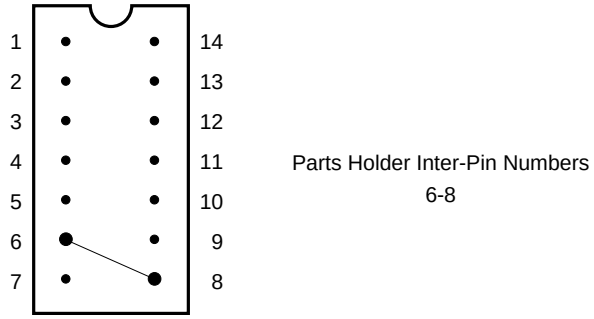
Items to be prepared

- Parts holder (IE-78K0-NS-P04 accessory)
- Lead wire
- Set of soldering tools

Procedure

<1> Solder and wire the parts holder provided with the lead wire.

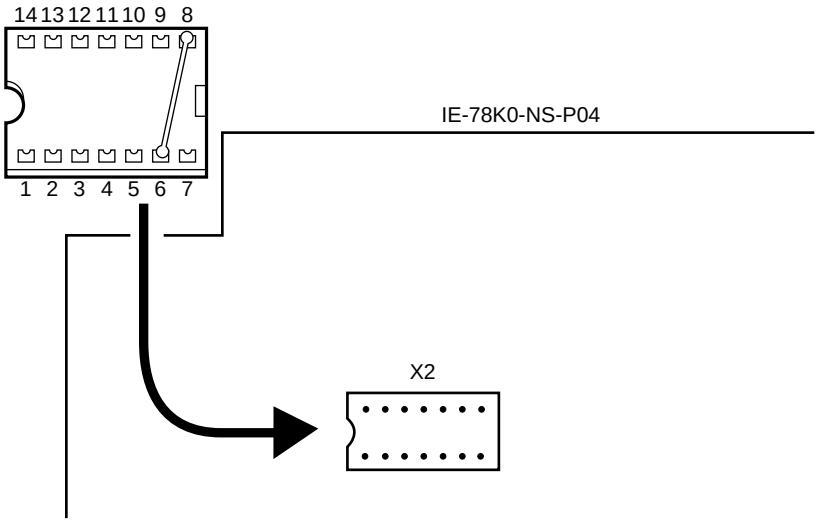
Figure 4-20: Lead Wiring Diagram (When External Clock on the Target Hardware is used as Main System Clock)



<2> Prepare the break board (jumper settings) and the IE-78K0-NS-P04.

<3> Insert parts holder <1> in the socket (marked “X2”) on the IE-78K0-NS-P04. Ensure that the pin 1 mark is correctly oriented when inserting the parts holder.

Figure 4-21: Parts Holder Mounting Location (When External Clock on the Target Hardware is used as Main System Clock)

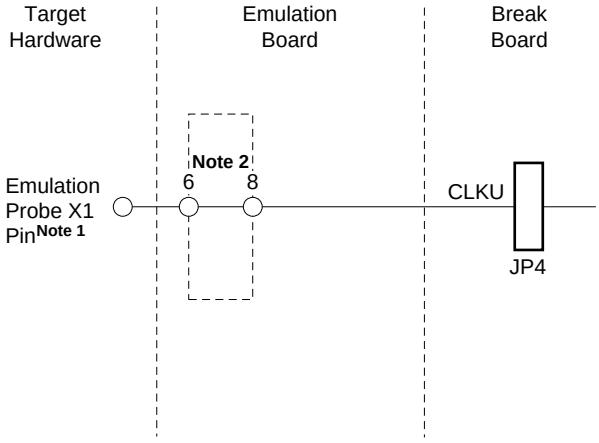


<4> Confirm that the component mounted on the X1 (MAIN) socket on the break board as well as the IE-78K0-NS-P04 are wired as shown in Figure 4-5.

<5> Install the IE-78K0-NS-P04 and the other boards in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock signal on the target system to be supplied to the emulation device.

Figure 4-22: Clock Enabling



Notes: **1.** Target device pin name
2. Parts holder pin numbers

Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

4.2.4 Examples of Main System Clock Setting

(1) Standard Clock offered by the Break Board

Break Board: JP2 - Frequency selection
JP4 - CLK I
Emulation Board: X2 with shortcut between 6 - 8
ID78K0: Internal

(2) Clock mounted by the User on the Emulation Board

- User related Clock
  Break Board: JP2 - don't care
  JP4 - CLK U
  Emulation Board: X2 with parts holder and crystal resonator, ceramic resonator or crystal oscillator
  ID78K0: External
- Fixed Clock
  Break Board: JP2 - IOMCK
  JP4 - CLK I
  Emulation Board: don't care
  ID78K0: Internal

(3) External Clock on the Target Hardware

Break Board: JP2 - don't care
JP4 - CLK U
Emulation Board: X2 with shortcut between 6 - 8
ID78K0: External

4.3 Subystem Clock Setting

It is not necessary to change the parts holder (IC30, X2 (SUB)) on the breakboard IE-78001-R-BK.

4.3.1 When Using Standard Clock offered by the Break Board

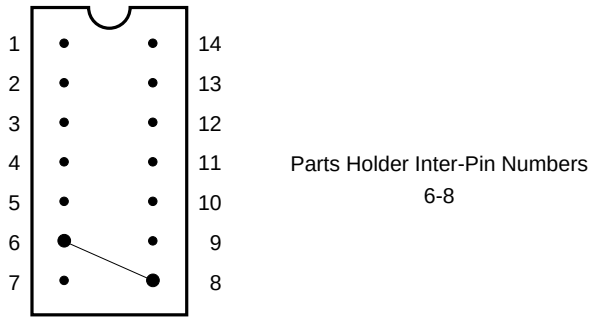
A parts holder, wired as shown in Figure 4-18, is fitted in the X1 (SUB) socket on the IE-78K0-NS-P04 when the product is shipped. If the parts holder state is the same as when the product was shipped, no particular hardware settings are necessary.

Items to be prepared

- Parts holder (IE-78K0-NS-P04 accessory)
- Lead wire
- Set of soldering tools

Procedure

Figure 4-23: Lead Wiring Diagram (When Clock mounted on Break Board is used as Subystem Clock)



<1> Check the break board and the IE-78K0-NS-P04.

<2> Insert parts holder in the socket (marked “X1”) on the IE-78K0-NS-P04. Ensure that the pin <1> mark is correctly oriented when inserting the parts holder.

<3> Confirm that the component mounted on the X2 (SUB) socket on the break board as well as the IE-78K0-NS-P04 are wired as shown in Figure 4-5.

4.3.2 When Using Clock Mounted by User on the Emulation Board

The settings shown in (1) or (2) below must be performed depending on the type of clock used.
No particular settings are required on the integrated debugger.

(1) When ceramic resonator/crystal resonator is used

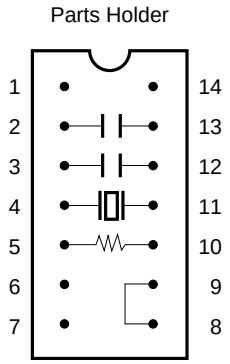
Items to be prepared

- Parts holder (IE-78K0-NS-P04 accessory)
- Ceramic resonator or crystal resonator
- Resistor Rx
- Capacitor CA
- Capacitor CB
- Set of soldering tools

Procedure

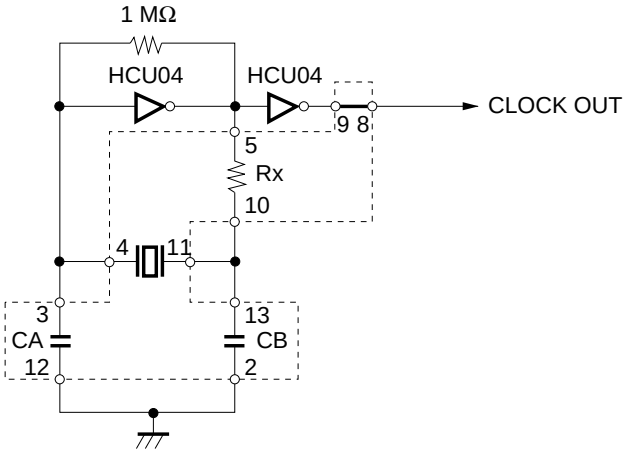
<1> Solder the ceramic resonator or crystal resonator to be used and resistor Rx, capacitor CA and capacitor CB appropriate to the oscillation frequency of the resonator to the parts holder provided as shown below.

Figure 4-24: Lead Wiring Diagram (When Clock mounted by User)



Pin No.	Connection
2-13	Capacitor CB
3-12	Capacitor CA
4-11	Ceramic resonator/crystal resonator
5-10	Resistor Rx
8-9	Shorted

Figure 4-25: Circuit Diagram

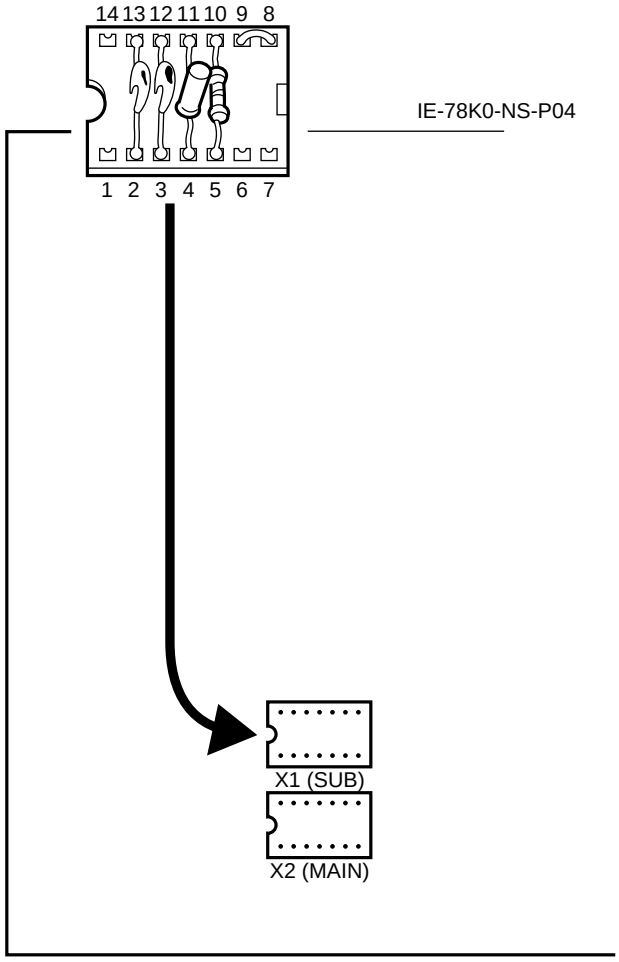


Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

<2> Prepare the break board (jumper settings) and the IE-78K0-NS-P04.

<3> Insert parts holder <1> in the socket X1 from which the external clock parts holder was removed in <3>. Ensure that the pin 1 mark is correctly oriented when inserting the parts holder.

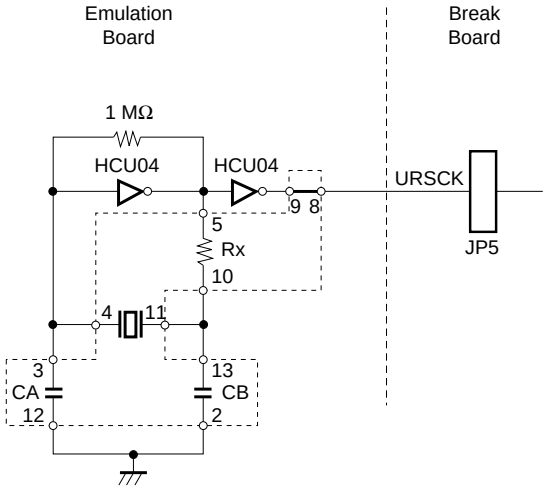
Figure 4-26: Parts Holder Mounting Location (When Clock mounted by User on the Emulation Board is used as Subsystem Clock)



<4> Install the IE-78K0-NS-P04 and the other boards in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock to be supplied to the emulation device from the mounted resonator.

Figure 4-27: Clock Enabling



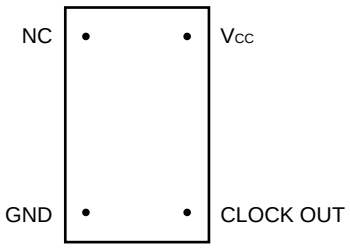
Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

(2) When crystal oscillator is used

Items to be prepared

- Crystal oscillator (with pins as shown in Figure 4-28)

Figure 4-28: Crystal Oscillator (When Clock mounted by User on the Emulation Board is used as Subsystem Clock)

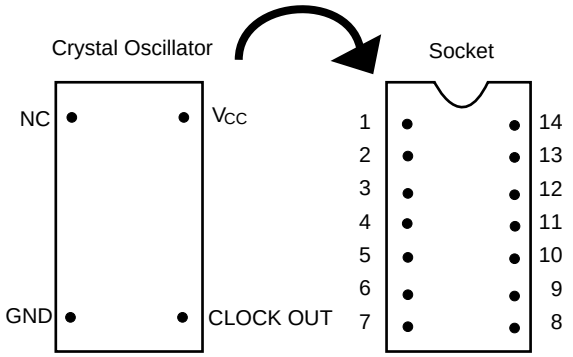


Procedure

<1> Prepare the break board (jumper setting) and the IE-78K0-NS-P04.

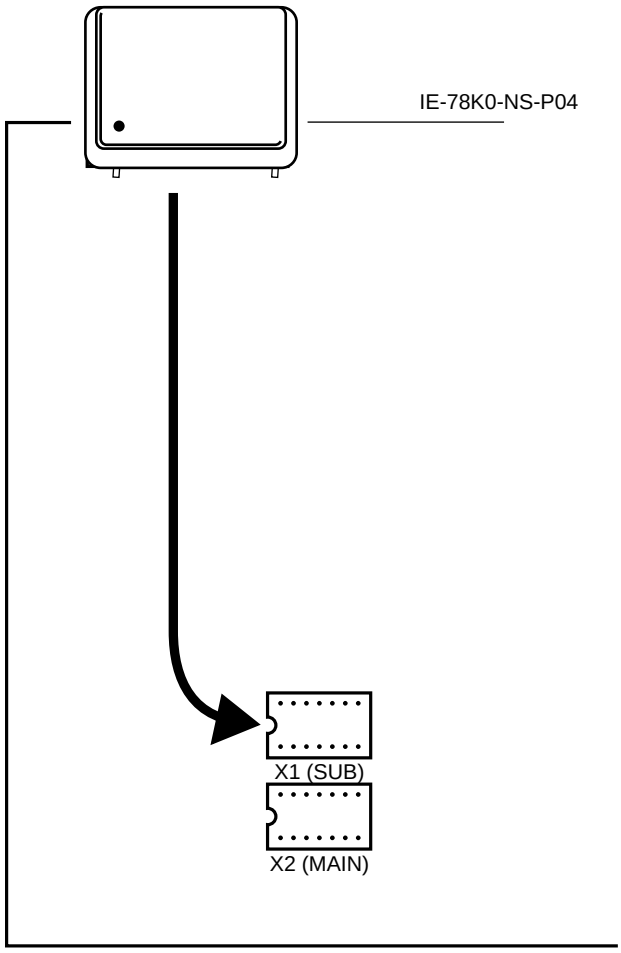
<2> Insert the crystal oscillator in the socket X1 from which the external clock parts holder was removed. The crystal oscillator pins should be inserted in the socket holes as shown in Figure 4-29.

Figure 4-29: Insertion of Crystal Oscillator in the Socket



Crystal Oscillator Pin	Socket Hole No.
NC	1
GND	7
CLOCK OUT	8
VCC	14

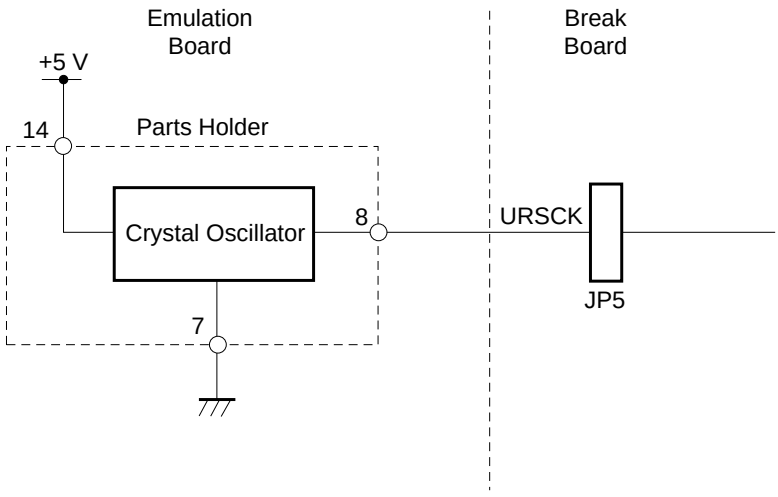
Figure 4-30: Crystal Oscillator Mounting Location (When Clock mounted by User on the Emulation Board is used as Subsystem Clock)



<4> Install the IE-78K0-NS-P04 and the other board in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock to be supplied to the emulation device from the mounted oscillator.

Figure 4-31: Clock Enabling



4.3.3 When Using External Clock on the Target Hardware

A parts holder, wired as shown in Figure 4-32, is fitted in the X1 socket on the IE-78K0-NS-P04 when the product is shipped. If the parts holder state is the same as when the product was shipped, no particular hardware settings are necessary.

No particular settings are required on the integrated debugger.

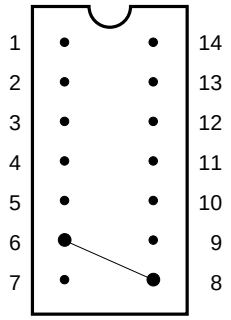
Items to be prepared

- Parts holder (IE-78K0-NS-P04 accessory)
- Lead wire
- Set of soldering tools

Procedure

<1> Solder and wire the parts holder provided with the lead wire.

Figure 4-32: Lead Wiring Diagram (When External Clock on the Target Hardware is used as Subsystem Clock)

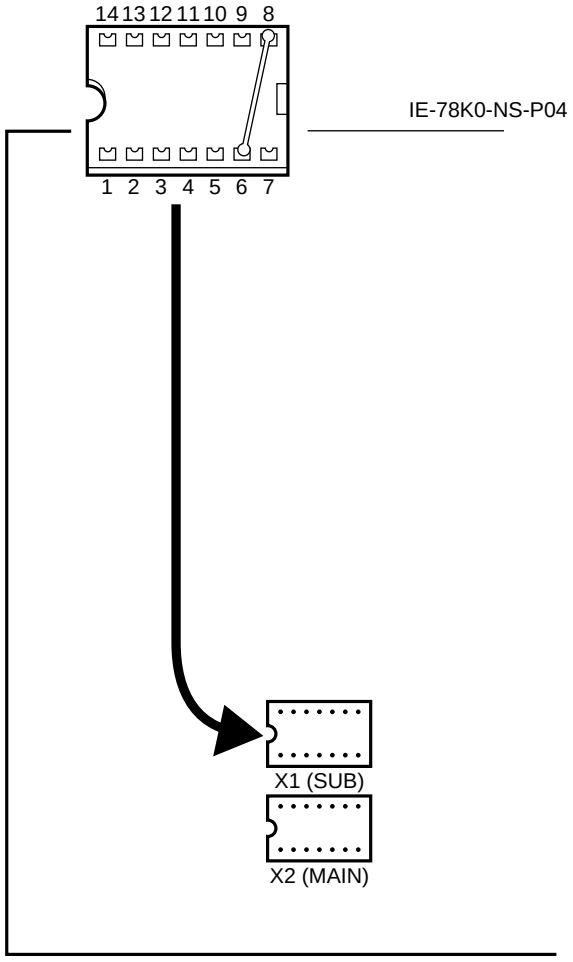


Parts Holder Inter-Pin Numbers
6-8

<2> Prepare the break board (jumper settings) and the IE-78K0-NS-P04.

<3> Insert parts holder <1> in the socket (marked “X1”) on the emulation board. Ensure that the pin 1 mark is correctly oriented when inserting the parts holder.

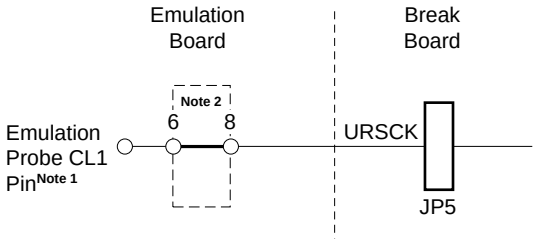
Figure 4-33: Parts Holder Mounting Location (When External Clock on the Target Hardware is used as Subsystem Clock)



<4> Install the IE-78K0-NS-P04 and the other board in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock signal on the target system to be supplied to the emulation device.

Figure 4-34: IE-78001-R-A Side (Emulation Device)



Notes: **1.** Target device pin name
2. Parts holder pin numbers

Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

4.3.4 Examples of Subsystem Clock Setting

(1) Standard Clock offered by the Break Board

Break Board: JP5 - 32kHz
Emulation Board: X1 with shortcut between 6 - 8

(2) Clock mounted by the User on the Emulation Board

Break Board: JP5 - URSCK
Emulation Board: X1 with parts holder and crystal resonator, ceramic resonator or crystal oscillator

(3) External Clock on the Target Hardware

Break Board: JP5 - URSCK
Emulation Board: X2 with shortcut between 6 - 8

[Memo]

Appendix A IE-78K0-NS-P04, IE-1615-NS-EM4 Product Specifications

Product name	: IE-78K0-NS-P04, IE-1615-NS-EM4
Peripheral emulation device	: μPD1615, 16F15, 1616.
Operating temperature	: 0 to 50 °C
Humidity	: 10 to 80% RH (no condensation)
Storage temperature	: –15 to +60 °C
Power supply	: Power supply capacity : DC 200mA (MAX.) 1.0 W +5 V

Table A-1: Connectors on IE-78K0-NS-P04 Board (Emulation Board) and IE-1615-NS-EM4 Board (Probe Board).

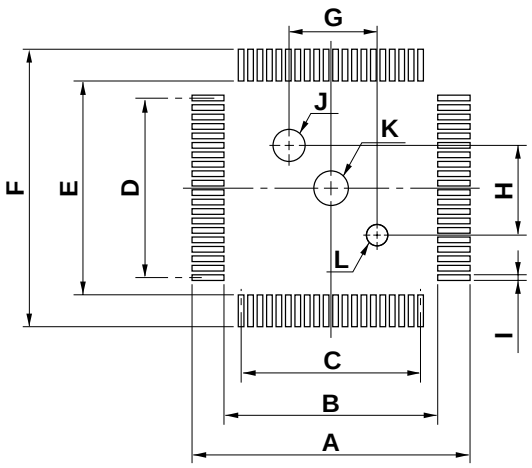
Name	Description (IE-78K0-NS-P04)	Name	Description (IE-1615-NS-EM4)
CN1	Break board (IE-78001-R-BK) connectors	CN5	Emulation board connectors (IE-78K0-NS-P04)
CN2		CN6	
CN3		CN7	
CN4		CN8	
CN5	Probe board connectors (IE-1615-NS-EM4)	CN9	
CN6		CN10	
CN7		CN11	Probe connector (EP-78230GC-R)
CN8		JP1	VAN in/out buffer select
CN9		JP2	VAN in/out buffer select
CN10		JP3	VAN in/out buffer select
CN13	FPGA download cable connector (only for internal use by NEC)	JP4	VAN in/out buffer select
CN11	JTAG connector of FPGA (only for internal use by NEC)		
CN12			
CN14	Test connector (only for internal use by NEC)		
CN15			
CN16			
CN17			
CN18			
JP1	Analog Reference Voltage		
JP2	GND-pin of A/D Converter		
JP3	Reserved (only for internal use by NEC)		
JP4	JTAG mode selection (only for internal use by NEC)		
JP5	FPGA mode selection		
JP6	JTAG mode selection (only for internal use by NEC)		
JP7	$LV_{REF}1$		
JP8	$LV_{REF}0$		

[Memo]

Appendix B Conversion Socket/Conversion Adapter Package Drawings and recommended Board Mounting Pattern

Figure B-1: EV9200GC-80 Recommended Board Mount Pattern (Reference)

Based on EV-9200GC-80
(2) Pad drawing (in mm)



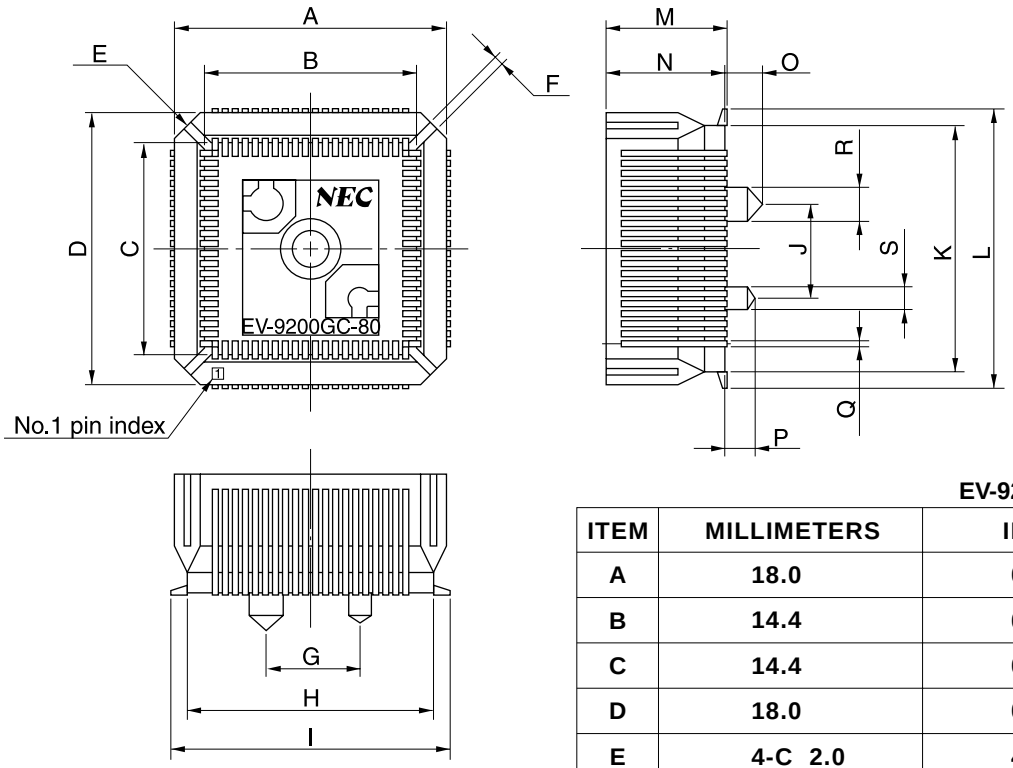
EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	0.65±0.02 x 19=12.35±0.05	$0.026^{+0.001}_{-0.002}$ x 0.748=0.486 $^{+0.003}_{-0.002}$
D	0.65±0.02 x 19=12.35±0.05	$0.026^{+0.001}_{-0.002}$ x 0.748=0.486 $^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0±0.05	$0.236^{+0.003}_{-0.002}$
H	6.0±0.05	$0.236^{+0.003}_{-0.002}$
I	0.35±0.02	$0.014^{+0.001}_{-0.001}$
J	Ø 2.36±0.03	Ø $0.093^{+0.001}_{-0.002}$
K	Ø 2.3	Ø 0.091
L	Ø 1.57±0.03	Ø $0.062^{+0.001}_{-0.002}$

Caution: Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "Semiconductor Device Mounting Technology Manual" (C10535E).

Figure B-2: EV9200GC-80 Package Drawings (Reference)

Based on EV-9200GC-80
(1) Package drawing (in mm)



EV-9200GC-80-G1E

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	Ø 2.3	Ø 0.091
S	Ø 1.5	Ø 0.059

[Memo]

Appendix C Pin Correspondence Tables of Emulation Probe

Table C-1: Connector CN11 to Emulation Probe (1/2)

No.	Real-chip	Pin Function
1		GND
3		NC
5		NC
7	Pin 42	P83/S36
9	Pin 20	Rx2VAN
11		GND
13	Pin 44	P85/S34
15	Pin 18	Rx0VAN
17	Pin 46	P87/S32
19	Pin 16	P06/TI50/TO50
21	Pin 48	P91/S30
23	Pin 14	P01/INTP1
25		GND
27	Pin 50	P93/S28
29	Pin 12	VDD0
31		NC
33		NC
35	Pin 40	P81/S38
37	Pin 21	TxVAN
39		GND
41	Pin 38	COM3
43	Pin 22	P47/SGO/SGOF
45	Pin 36	COM1
47	Pin 24	P45
49	Pin 34	VLC2
51	Pin 26	P43
53		GND
55	Pin 32	VLC0
57	Pin 28	P41
59	Pin 30	VSS1
61	Pin 70	P117/S8
63	Pin 68	P115/S10
65	Pin 72	P121/TIO0/TO0/S6
67		GND
69	Pin 66	P113/S12
71	Pin 74	RxD/S4
73	Pin 64	P111/S14
75	Pin 76	P125/SCK3/S2
77	Pin 62	P107/S16
79	Pin 78	SI3/S0
81		GND
83	Pin 61	P106/S17
85	Pin 80	P13/AN13
87		NC
89		NC
91	Pin 52	P95/S26
93	Pin 10	CL2
95		GND
97	Pin 54	P97/S24
99	Pin 08	IC/VPP
101	Pin 56	P101/S22
103	Pin 06	X1

No.	Real-chip	Pin Function
2		GND
4		NC
6		NC
8	Pin 41	P82/S37
10	Pin 19	Rx1VAN
12		GND
14	Pin 43	P84/S35
16	Pin 17	R07/TI51/TO51
18	Pin 45	P86/S33
20	Pin 15	P02/INTP2
22	Pin 47	P90/S31
24	Pin 13	P00/INTP0
26		GND
28	Pin 49	P92/S29
30	Pin 11	VSS0
32		NC
34		NC
36		NC
38		NC
40		GND
42	Pin 39	P807S39
44	Pin 23	P46/SGOA
46	Pin 37	COM2
48	Pin 25	P44
50	Pin 35	COM0
52	Pin 27	P42
54		GND
56	Pin 33	VLC1
58	Pin 29	P40
60	Pin 31	VDD1
62	Pin 71	PCL/S7
64	Pin 69	P119/S9
66	Pin 73	TIO1/S5
68		GND
70	Pin 67	P114/S11
72	Pin 75	TxD/S3
74	Pin 65	P112/S13
76	Pin 77	SO3/S1
78	Pin 63	P110/S15
80	Pin 79	AVss
82		GND
84		NC
86		NC
88		NC
90		NC
92	Pin 51	P94/S27
94	Pin 09	CL1
96		GND
98	Pin 53	P96/S25
100	Pin 07	X2
102	Pin 55	P100/S23
104	Pin 05	RESET

Table C-2: Connector CN11 to Emulation Probe (2/2)

105	Pin 58	P103/S20
107	Pin 04	Avref
109		GND
111	Pin 60	P105/S18
113	Pin 02	P11/ANI1
115		NC
117		NC
119		GND

106	Pin 57	P102/S21
108	Pin 03	P10/ANI0
110		GND
112	Pin 59	P104/S19
114	Pin 01	P12/ANI2
116		NC
118		NC
120		GND

Remark: The meaning of the symbols and figures in the Emulation Probe column is as follows:
GND: Ground clip, NC: Not connected
1–120: Emulation probe tip pin numbers

[Memo]

NEC

Facsimile Message

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

From:

Name

Company

Tel. FAX

Address

Thank you for your kind support.

North America
NEC Electronics Inc.
Corporate Communications Dept.
Fax: 1-800-729-9288

Hong Kong, Philippines, Oceania
NEC Electronics Hong Kong Ltd.
Fax: +852-2886-9022/9044

Asian Nations except Philippines
NEC Electronics Singapore Pte. Ltd.
Fax: +65-250-3583

Europe
NEC Electronics (Europe) GmbH
Technical Documentation Dept.
Fax: +49-211-6503-274

Korea
NEC Electronics Hong Kong Ltd.
Seoul Branch
Fax: 02-551-0451

Japan
NEC Corporation
Semiconductor Solution Engineering Division
Technical Information Support Dept.
Fax: 044-548-7900

South America
NEC do Brasil S.A.
Fax: +55-11-889-1689

Taiwan
NEC Electronics Taiwan Ltd.
Fax: 02-719-5951

I would like to report the following error/make the following suggestion:

Document title: _____

Document number: _____ Page number: _____

If possible, please fax the referenced page or drawing.

Document Rating	Excellent	Good	Acceptable	Poor
Clarity	❑	❑	❑	❑
Technical Accuracy	❑	❑	❑	❑
Organization	❑	❑	❑	❑

CS 95.12