QCIOT-SLG46826POCZ

The QCIOT-SLG46826POCZ board enables quick prototyping of the SLG46826V. The SLG46826V provides a small, low-power component for commonly used Mixed-Signal functions. The user creates the circuit design by programming the multiple-time non-volatile memory (NVM) to configure the interconnect logic, the IOs, and the macrocells of the SLG46826. Also, a dual power supply allows for the interfacing of two independent voltage domains. This highly versatile device features a wide variety of mixed-signal functions to be designed within a small, low-power single integrated circuit.

The board provides a Pmod™ connection for the on-board sensor to plug into any required MCU evaluation kit with a matching connector. The QCIOT-SLG46826POCZ board features Pmod connectors on both sides of the board to allow additional Pmod boards to connect in a daisy-chained solution with multiple devices on the same MCU Pmod connector.

The software support that is included with the Go Configure™ Software Hub provides code generation to connect the device and the MCU so that development time is significantly reduced. With its standard connector and software support, the QCIOT-SLG46826POCZ board is ideal for the Renesas Quick-Connect IoT to rapidly create an IoT system.

Features

- Multi-time programmable (MTP) GreenPAK that supports I^2C
- Uses GUI to program the GreenPAK
- Compatible with the QCIOT system
- 3.3V/1.8V power operated
- Two high-speed general-purpose rail-to-rail analog comparators (ACMPxH)
- Two low-power general purpose rail-to-rail analog comparators (ACMPxL)
- Three oscillators
  - 2.048kHz
  - 2.048MHz
  - 25MHz
- 2-kbit (256 × 8) I^2C-compatible (2-wire) serial EEPROM emulation with software write protection

Board Contents

- QCIOT-SLG46826POCZ Board

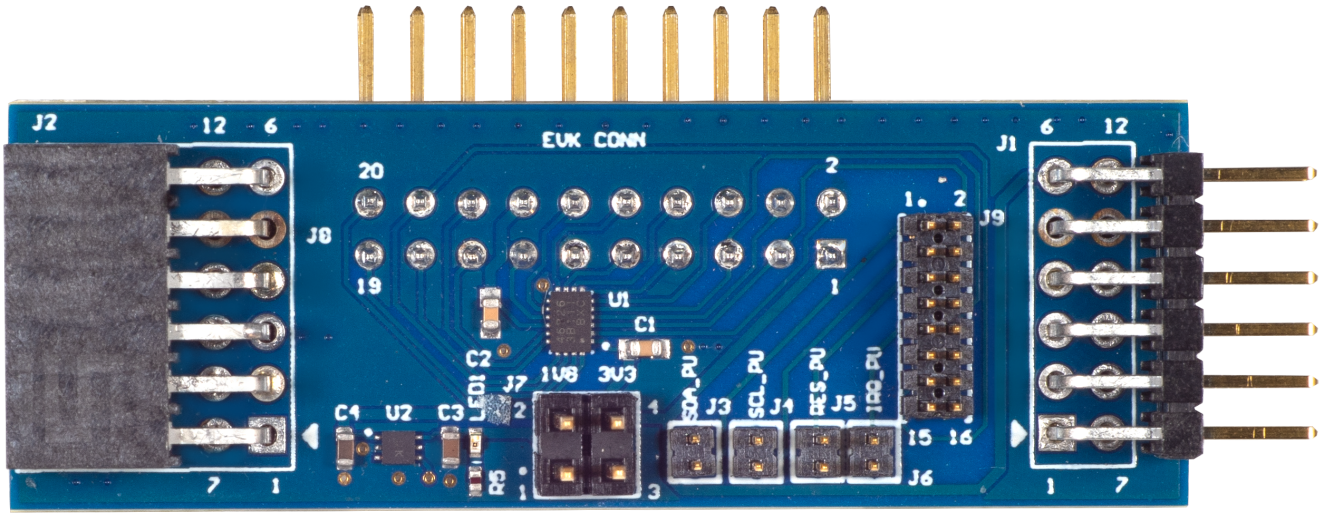

Figure 1. QCIOT-SLG46826POCZ Board

Contents

1. Functional Description

The QCIOT-SLG46826POCZ board is intended as a quick connect prototyping solution for routing the connections from one Pmod to a second Pmod. This board enables the designer to quickly evaluate applications where a Pmod on the MCU side is different from the peripheral module. Use the QCIOT-SLG46826POCZ board to eliminate the problem of different pin configurations on the Pmod. Also, use it to level-shift the signals from 3.3V to 1.8V and for prototyping SLG46826V.

The block diagram highlights the main parts of the system:

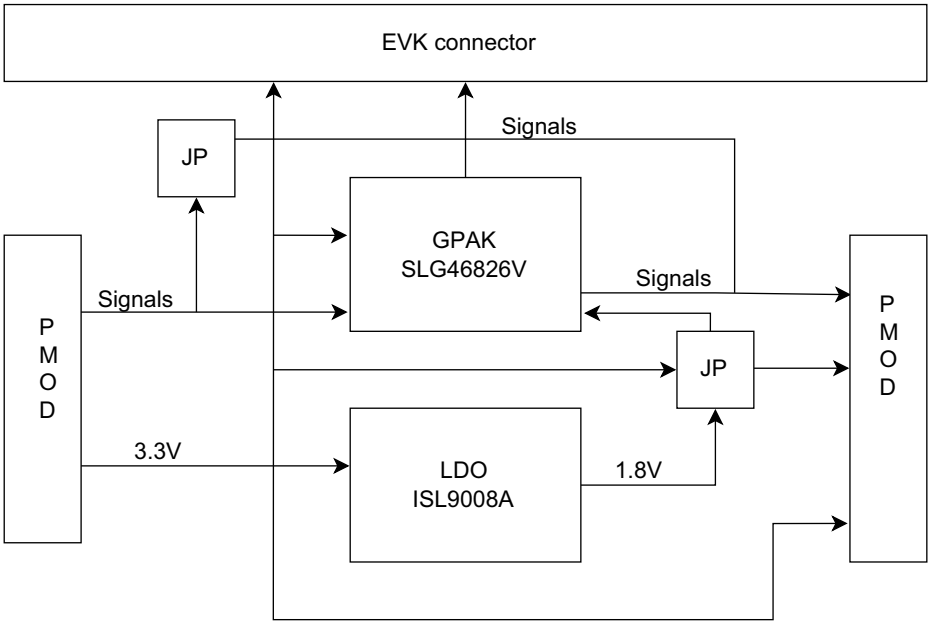

Figure 2. QCIOT-SLG46826POCZ Board Block Diagram

The building blocks of the QCIOT-SLG46826POCZ board and their functionality are as listed:

GPAK SLG46826V – The *Go Configure Software Hub* is used to create the circuit design by programming the multiple-time non-volatile memory (NVM) to configure the interconnect logic, the IOs, and the macrocells of the SLG46826. A dual power supply allows for interfacing two independent voltage domains. SLG46826V has two power supplies, VDD1 and VDD2. VDD1 is connected to the MCU Pmod output source (3.3V or 5V), and VDD2 is 3.3V or 1.8V depending on Jumper (J7) connection.

LDO ISL9008A – SL9008A is a high-performance, single low-noise high PSRR LDO that delivers a continuous 150mA load current. This LDO provides a fixed output voltage of 1.8V to the VDD2 of SLG46826V and to the opposite-side Pmod.

1.1 Setup and Configuration

1.1.1 Software Installation and Usage

The Renesas *Go Configure Software Hub* development software enables a complete graphical design process that requires no programming language or compiler, allowing a designer to configure, program, and test custom GreenPAK samples in minutes. Renesas Go Configure provides the following features:

- Schematic capture-like design and routing
- Entire component library showing available resources for each device
- Easy component configuration

- Example projects and support documentation
- Simulation capability with external components

Visit the Renesas Go Configure Software Hub for more information about creating your customized system solution.

1.1.2 Kit Hardware Connections

Follow these procedures to set up the kit.

1. Connect the QCIOT-SLG46826POCZ board to the GreenPAK Advanced Development Board.

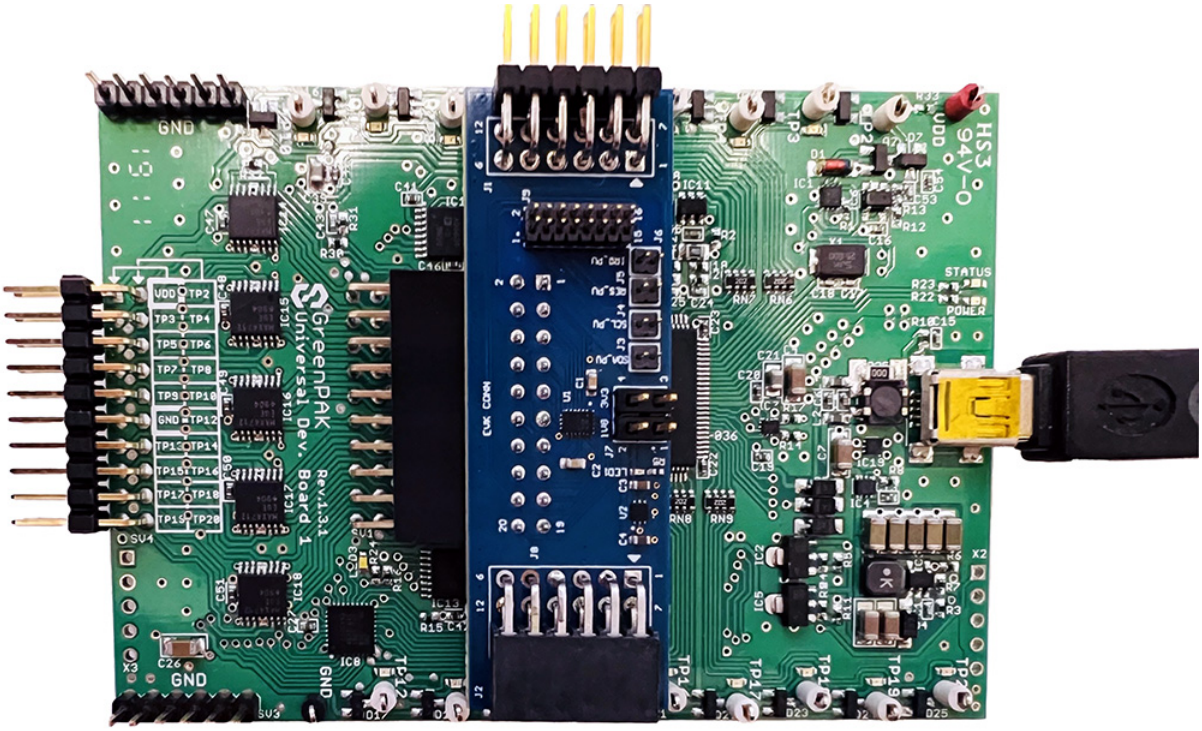

Figure 3. Hardware Connection

2. Using the *Go Configure Software Hub*, program GreenPAK as per the system requirement.
3. Unplug the QCIOT-SLG46826POCZ board from the GreenPAK Development Board.
4. The left-side Pmod must be configured to the voltage level 1.8V or 3.3V. Depending on the requirement, connect the J7 pins using the jumper.

J7 Pins	Voltage
Pin 1 and Pin 2	1.8V
Pin 3 and Pin 4	3.3V

5. The J9 connector connects the right-side Pmod to left-side Pmod. Depending on the application, connect the J9 connector pins (Figure 4).

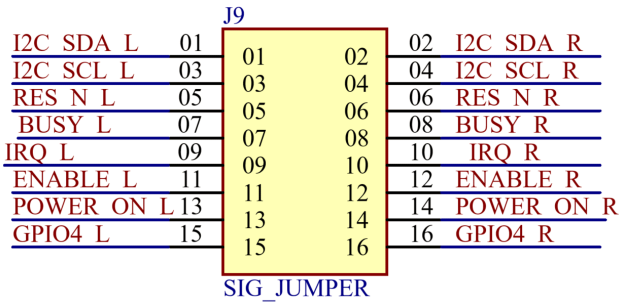

Figure 4. J9 Jumper Connector

6. If required connect the J3, J4, J5, and J6 jumpers to place 4.7kΩ pull-up resistors on the SDA, SCL, RES, and IRQ lines.
7. The QCIOT-SLG46826POCZ board is now programmed and configured to be used in the system.

2. Board Design

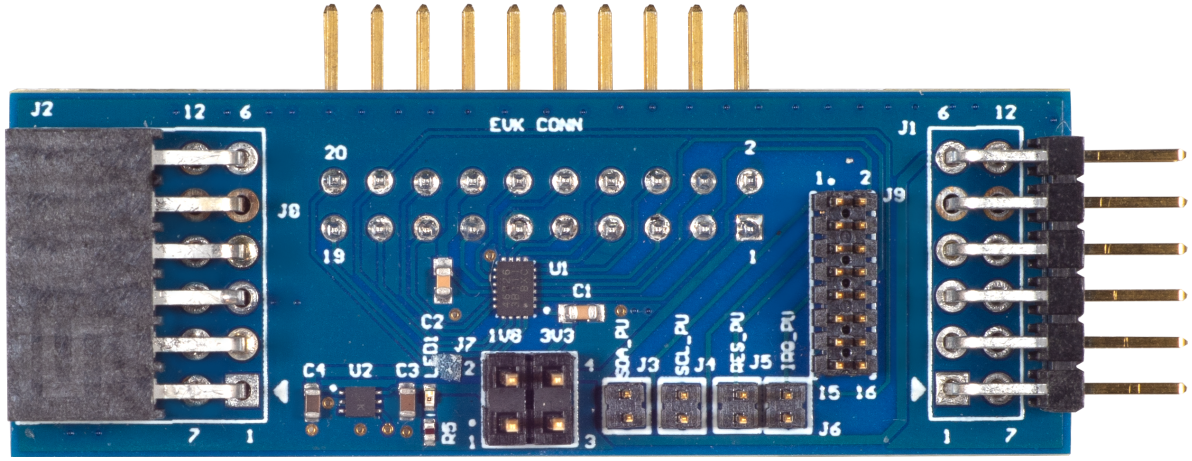

Figure 5. QCIOT-SLG46826POCZ Board (Top)

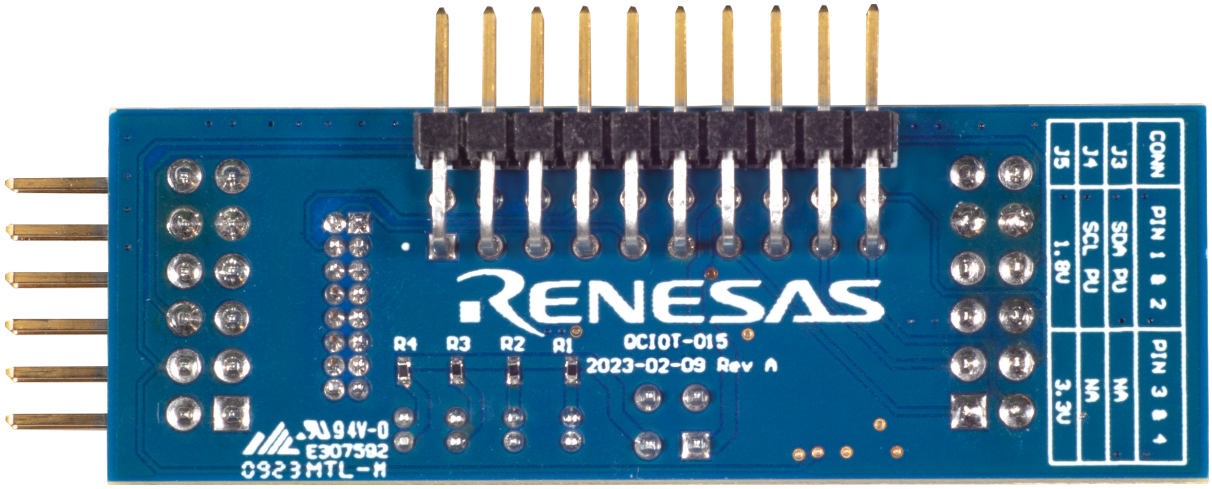

Figure 6. QCIOT-SLG46826POCZ Board (Bottom)

2.1 Schematic Diagrams

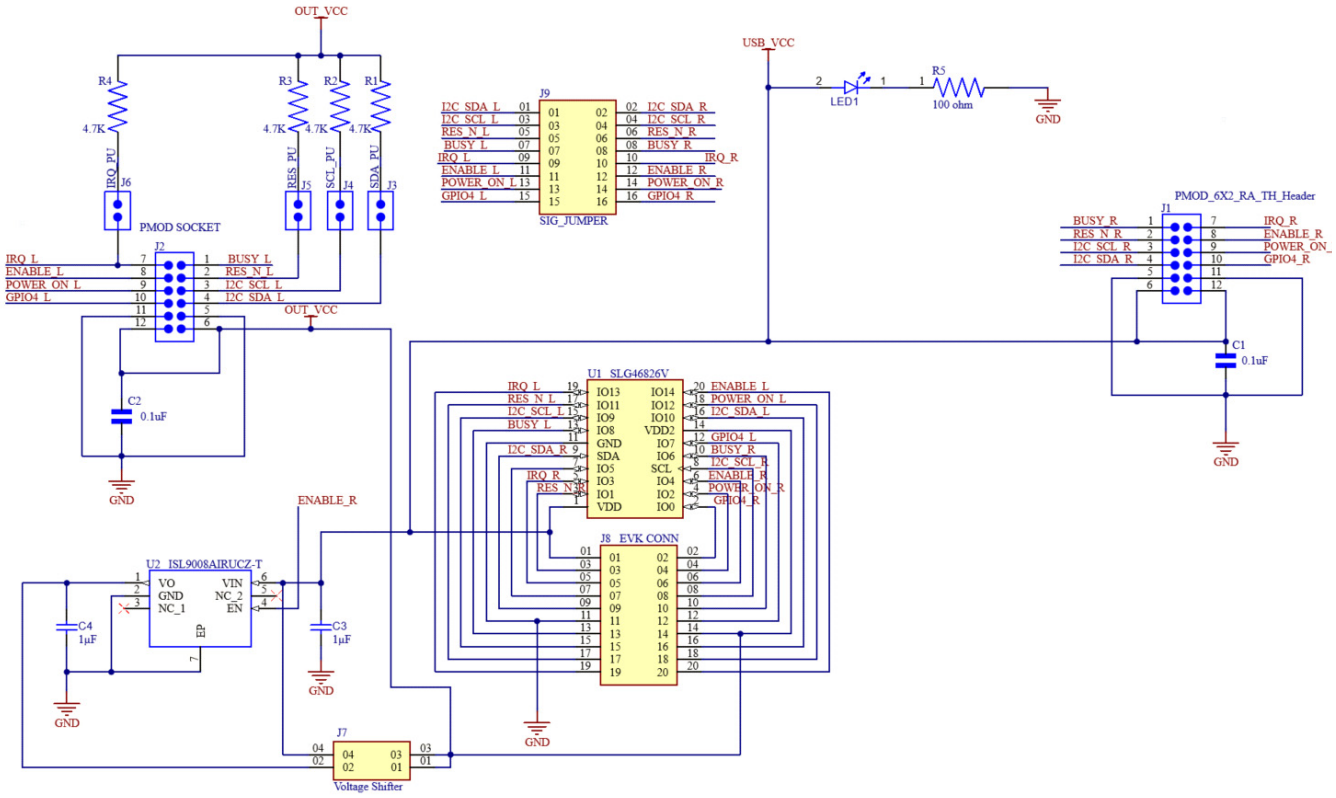

Figure 7. QCIOT-SLG46826POCZ Board Schematic

2.2 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Part Number
2	C1, C2	0.1µF ±10% 10V Ceramic Capacitor X7R 0603 (1608 Metric)	KYOCERA AVX	0603ZC104KAT2A
2	C3, C4	1µF ±20% 10V Ceramic Capacitor X7R 0603 (1608 Metric)	KYOCERA AVX	0603ZC105MAT2A
4	J3, J4, J5, J6	Connector Header Through Hole 2 position 0.050" (1.27mm)	Samtec Inc.	FTS-102-01-L-S
1	J1	Connector Header Through Hole, Right Angle 12 position 0.100" (2.54mm)	Harwin Inc.	M20-9950645
1	J2	12 Position Receptacle Connector 0.100" (2.54mm) Through Hole, Right Angle Gold	Samtec Inc.	SSW-106-02-F-D-RA
1	J8	Connector Header Through Hole, Right Angle 20 position 0.100" (2.54mm)	Samtec Inc.	TSW-110-08-L-D-RA
1	J7	Connector Header Through Hole 4 position 0.100" (2.54mm)	Samtec Inc.	TSW-102-23-S-D
1	LED1	Red 620nm LED Indication - Discrete 2.1V 0402 (1005 Metric)	QT Brightek (QTB)	QBLP595-R-2897
4	R1, R2, R3, R4	4.7kΩ ±1% 0.063W, 1/16W Chip Resistor 0402 (1005 Metric) Thick Film	Bourns Inc.	CR0402-FX-4701GLF
1	R5	100Ω ±5% 0.063W, 1/16W Chip Resistor 0402 (1005 Metric) Anti-Sulfur, Automotive AEC-Q200 Thick Film	Rohm Semiconductor	SFR01MZPJ101
1	U1	Linear Voltage Regulator IC Positive Fixed 1 Output 150mA 6-UTDFN (1.6×1.6)	Renesas Electronics America Inc	ISL9008AIRUCZ-T
1	J9	Connector Header Through Hole 16 position 0.050" (1.27mm)	Samtec Inc.	FTSH-108-01-L-D
1	U2	GPAK MIXED SIGNAL MATRIX	Dialog Semiconductor GmbH	SLG46826V

2.3 Board Layout

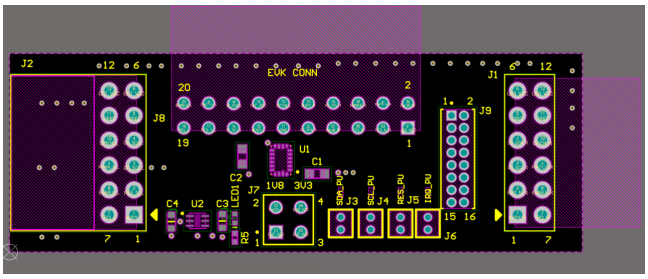

Figure 8. Top Overlay

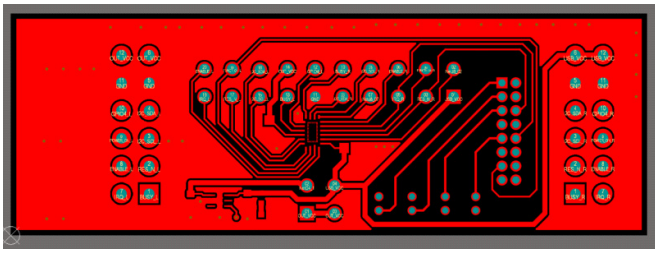

Figure 9. Top Layer

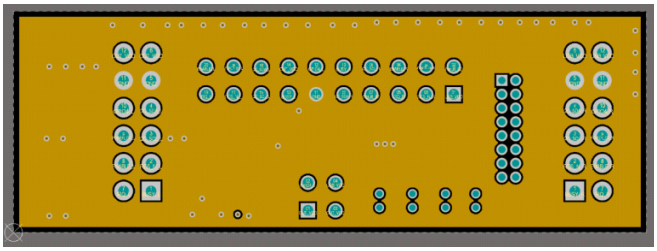

Figure 10. Layer 2(GND)

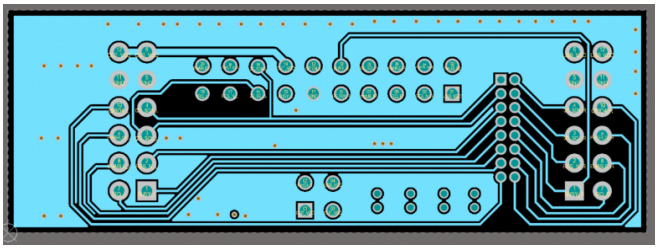

Figure 11. Layer 3(Signal)

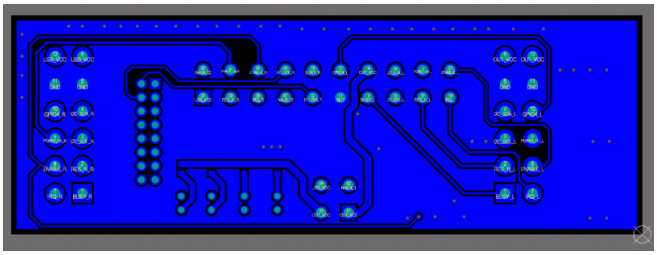

Figure 12. Bottom Layer

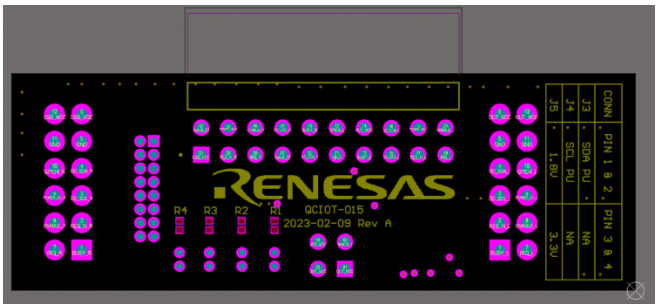

Figure 13. Bottom Overlay

3. Software and Hardware Configuration

The section provides an example for configuring the GreenPAK with the *Go Configure Software Hub* and hardware connections.

3.1 Example 1: Re-route GPIO Pins

3.1.1 Step 1: Configure the GreenPAK using the Go Configure Software Hub

As an example, with a Quick Connect Board that has the following pin configuration:

Pin 1 → BUSY	Pin 7 → IRQ
Pin 2 → RES	Pin 8 → EN
Pin 3 → SCL	Pin 9 → PWR_ON
Pin 4 → SDA	Pin 10 → GPIO
Pin 5 → GND	Pin 11 → GND
Pin 6 → VCC	Pin 12 → VCC

The Renesas MCU board provides the following configuration:

Pin 1 → BUSY	Pin 7 → RES
Pin 2 → IRQ	Pin 8 → PWR_ON
Pin 3 → SCL	Pin 9 → EN
Pin 4 → SDA	Pin 10 → GPIO
Pin 5 → GND	Pin 11 → GND
Pin 6 → VCC	Pin 12 → VCC

Because the RES, IRQ, EN, and PWR_ON pins do not match with the Renesas MCU board, the GreenPAK requires configuration to match the pin configuration of the MCU board:

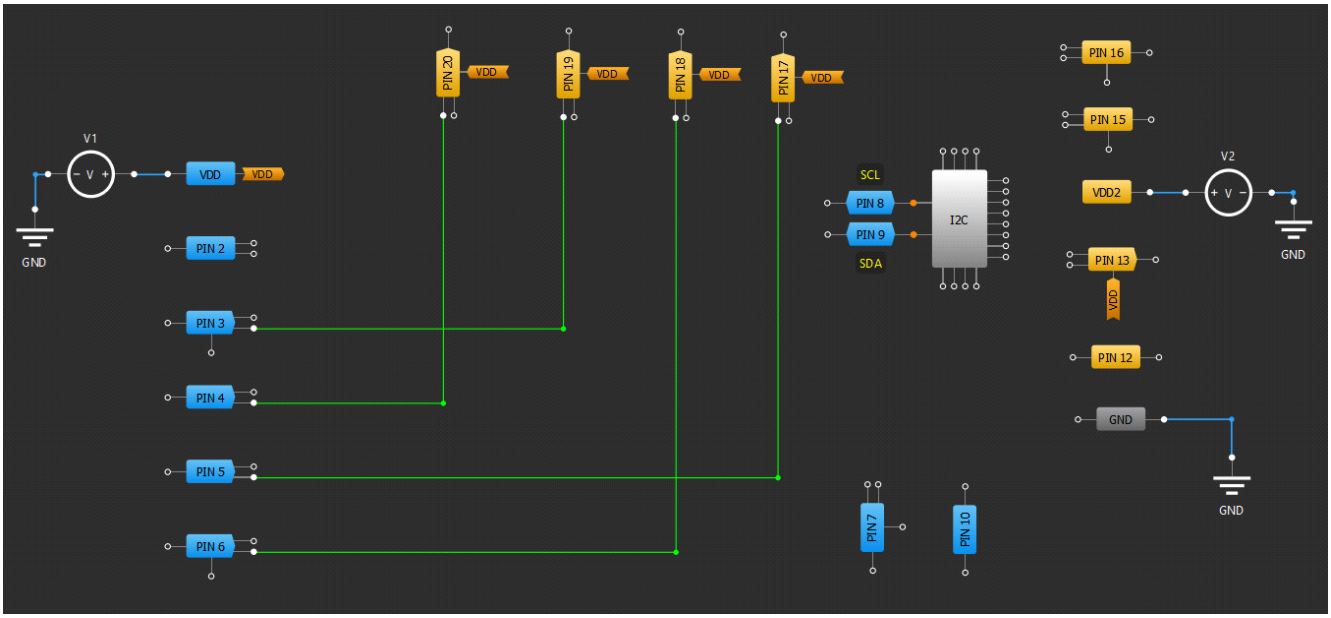

Figure 14. Go Configure Schematics

Key Notes:

- I/Os within GreenPAK are flexible. The I/O capabilities vary from pin-to-pin and part-to-part, so a design should be mapped to the necessary pin configuration before choosing a specific GreenPAK.
- Outputs can be configured as push-pull or open-drain in either a NMOS or PMOS configuration. A scaling factor, such as 2x, indicates that the output strength is doubled.
- Additionally, pull-up and pull-down resistor options of 10kΩ, 100kΩ, and 1MΩ are available on output pins.
- Multiple input options are available, such as Digital-In, Digital-In with Schmitt Trigger, Low Voltage Digital-In, and Analog-In, which is used as an input to an ACMP.

For more details on the configuration settings, refer to the GreenPAK CookBook.

3.1.2 Step 2: Configure the J9 Connector

As the BUSY, SCL, SDA, and GPIO pins were unchanged and not configured, you must connect the unchanged right-side Pmod lines to the left-side Pmod lines using the J9 connector.

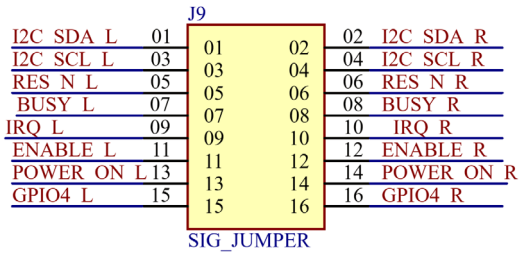

Figure 15. J9 Jumper Connector

For this specific application you must connect the J9 connector as follows:

Pin Number	Pin Number	Connection	Line
1	2	Close	SDA
3	4	Close	SCL
5	6	Open	RES
7	8	Close	BUSY
9	10	Open	IRQ
11	12	Open	EN
13	14	Open	PWR_ON
15	16	Close	GPIO

3.1.3 Step 3: Configure Voltage Level using the J7 Connector

Depending on the application, the left-side Pmod (J2) can be configured to either 1.8V or 3.3V.

J7 Pins	Voltage
Pin 1 and Pin 2	1.8V
Pin 3 and Pin 4	3.3V

3.1.4 Step 4: Connect the Pull-Up Resistors

If required, connect the J3, J4, J5, and J6 jumpers to place 4.7kΩ pull-up resistors on the SDA, SCL, RES, and IRQ lines.

Jumper Connector	Line
J3	SDA
J4	SCL
J5	RES
J6	IRQ

The QCIOT-SLG46826POCZ board configuration is now complete and ready to use in the system.

Note: Ensure the unused I/O pins are made High-impedance.

3.2 Example 2: Window Comparator

By default, the QCIOT-SLG46826POCZ board is programmed to work as a Window Comparator. For more details on the window comparator functions, refer to the GreenPAK CookBook.

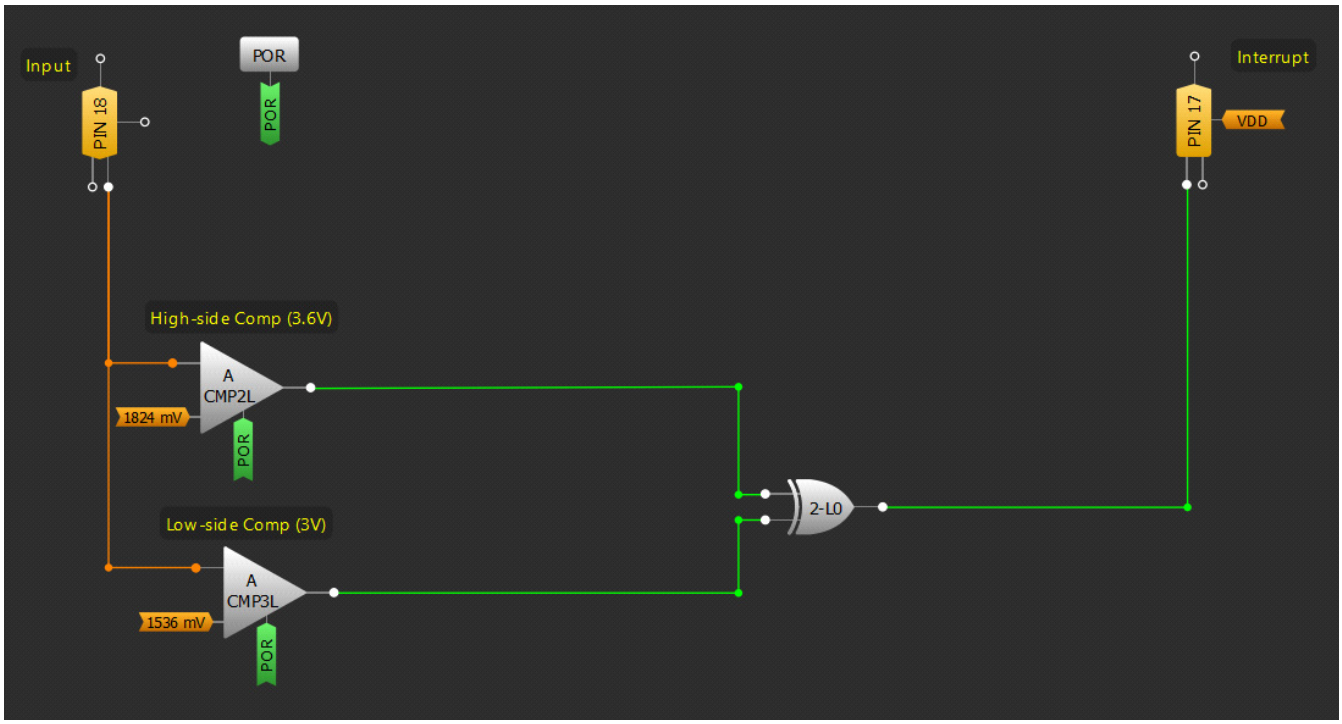

Figure 16. Window Comparator Schematic

Figure 16 shows the schematic of the window comparator. Input is connected to Pin 18 whereas output is connected to Pin 17 on GreenPAK GPIO IC. Input is connected to two comparators, and depending on the voltage level selected for each comparator, the comparator will trigger the output pin 17 (Interrupt pin).

For this specific window comparator code, the comparators are set to High-side Comp as 3.6V and Low-side Comp as 3V. If the input voltage range is between 3V to 3.6V, the output interrupt pin is high whereas if the input voltage is out of this range, then the output pin is low.

Notes:

- Pmod board connector J2 pin 9 is the input pin connected to Pin 18 on the GreenPAK GPIO IC.
- Pmod board connector J2 pin 2 is the output pin connected to Pin 17 on the GreenPAK GPIO IC.

4. Ordering Information

Part Number	Description
QCIOT-SLG46826POCZ	QCIOT-SLG46826POCZ Board

5. Revision History

Revision	Date	Description
1.04	Apr 16, 2024	▪ Added section Example 1: Re-route GPIO Pins and renumbered relative sub-sections. ▪ Added section Example 2: Window Comparator.
1.03	Feb 21, 2024	Changed part number to QCIOT-SLG46826POCZ from GPK46826VPOCZ.
1.02	Feb 9, 2024	Removed references to QCIOT-015 on page 1.
1.01	Jan 19, 2024	▪ Changed QCIOT-015 to GPK46826VPOCZ throughout the document. ▪ Updated Functional Description text. ▪ Added notes at the end of Step 4: Connect the Pull-Up Resistors.
1.00	Sep 8, 2023	Initial release