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Renesas Electronics Corporation

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User's Manual

R0P7780TH001TRKE

General Information Manual

SH7780 T-Engine Development Kit

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Rev.2.00 2008.06

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Precautions for Safety

Definitions of Signal Words

In both the user's manual and on the product itself, several icons are used to insure proper handling of this product and also to prevent injuries to you or other persons, or damage to your properties.
This chapter describes the precautions which should be taken in order to use this product safely and properly. Be sure to read this chapter before using this product.

⚠	This symbol represents a warning about safety. It is used to arouse caution about a potential danger that will possibly inflict an injury on persons. To avoid a possible injury or death, please be sure to observe the safety message that follows this symbol.
⚠ **DANGER**	**DANGER** indicates an imminently dangerous situation that will cause death or heavy wound unless it is avoided. However, there are no instances of such danger for the product presented in this manual.
⚠ **WARNING**	**WARNING** indicates a potentially dangerous situation that will cause death or heavy wound unless it is avoided.
⚠ **CAUTION**	**CAUTION** indicates a potentially dangerous situation that will cause a slight injury or a medium-degree injury unless it is avoided.
CAUTION	**CAUTION** with no safety warning symbols attached indicates a potentially dangerous situation that will cause property damage unless it is avoided.
IMPORTANT	This is used in operation procedures or explanatory descriptions to convey exceptional conditions or cautions to the user.

In addition to the five above, the following are also used as appropriate.

△means WARNING or CAUTION.
Example:  CAUTION AGAINST AN ELECTRIC SHOCK

⃠means PROHIBITION.
Example:  DISASSEMBLY PROHIBITED

●means A FORCIBLE ACTION.
Example:  UNPLUG THE POWER CABLE FROM THE RECEPTACLE.

⚠ WARNING

Warnings for AC Power Supply:

- If the attached AC power cable does not fit the receptacle, do not alter the AC power cable and do not plug it forcibly. Failure to comply may cause electric shock and/or fire.
- Do not touch the plug of the AC power cable when your hands are wet. This may cause electric shock.
- This product is connected signal ground with frame ground. If your developing product is transformless (not having isolation transformer of AC power), this may cause electric shock. Also, this may give an unrepairable damage to this product and your developing one.
  While developing, connect AC power of the product to commercial power through isolation transformer in order to avoid these dangers.
- If other equipment is connected to the same branch circuit, care should be taken not to overload the circuit.

- When installing this equipment, insure that a reliable ground connection is maintained.

- If you smell a strange odor, hear an unusual sound, or see smoke coming from this product, then disconnect power immediately by unplugging the AC power cable from the outlet.
  Do not use this as it is because of the danger of electric shock and/or fire. In this case, contact your local distributor.
- Before setting up this product and connecting it to other devices, turn off power or remove a power cable to prevent injury or product damage.

Warnings to Be Taken for This Product:

- Do not disassemble or modify this product. Personal injury due to electric shock may occur if this product is disassembled and modified. Disassembling and modifying the product will void your warranty.
- Make sure nothing falls into the cooling fan on the top panel, especially liquids, metal objects, or anything combustible.

Warning for Installation:

- Do not set this product in water or areas of high humidity. Make sure that the product does not get wet. Spilling water or some other liquid into the product may cause unrepairable damage.

Warning for Use Environment:

- This equipment is to be used in an environment with a maximum ambient temperature of 35°C. Care should be taken that this temperature is not exceeded.

⚠ CAUTION

Note on Connecting the Power Supply:

- Do not use any power cable other than the one that is included with the product.
- The power cable included with the product has its positive and negative poles color-coded by red and black, respectively.
- Pay attention to the polarities of the power supply. If its positive and negative poles are connected in reverse, the internal circuit may be broken.
- Do not apply any voltages exceeding the product's rated power supply voltage (5.0 V ±5%). Extreme voltages may cause a burn due to abnormal heat or cause the internal circuit to break down.

Cautions to Be Taken for Handling This Product:

- Use caution when handling the main unit. Be careful not to apply a mechanical shock.
- Do not touch the connector pins of the product main unit and the target MCU connector pins directly. Static electricity may damage the internal circuits.
- Excessive flexing or force of the flexible cable for connecting this product to the emulation probe may break connector.

Cautions to Be Taken for System Malfunctions:

- If the product malfunctions because of interference like external noise, do the following to remedy the trouble.
  (1) Press the RESET button on the board.
  (2) If normal operation is not restored after step (1), shut OFF the product once and then reactivate it.

Content

1. Outline

This chapter describes the package components, the system configuration and the preparation for using this product for the first time.

1.1 Package Components

The R0P7780TH001TRK package consists of the following items.

Table 1.1 Package components

Item	Quantity
T-Engine Board	1
ACadapter	1
RS-232C cable	1
CD-ROM - T-Engine Board User's Manual (This Manual) - Software setup Manual and sample software	2

1.2 System Configuration

1.2.1 T-Engine Features

The following summarizes the main features of T-Engine.

(1) The manual covers all information about T-Engine, including the circuit diagrams, connector specifications, and internal logic of FPGA employed on this board.

(2) The peripheral LSI chips (PCMCIA controller and sound generator chips) are commercially available.

(3) This board contains the PCMCIA controller, sound generator chip, eTRON card connector, etc., so that application systems can be developed taking advantage of them.

(4) This board contains two SH7780 buses (address bus and data bus) and one expansion slot subject to control signal output so that users can connect user-specific hardware.

1.2.2 T-Engine Configuration

Figure 1.1 shows a T-Engine Board system configuration and Figure 1.2 shows a T-Engine block diagram. Users must prepare any user-specific devices as needed, in addition to preparing the T-Engine and its accessories.

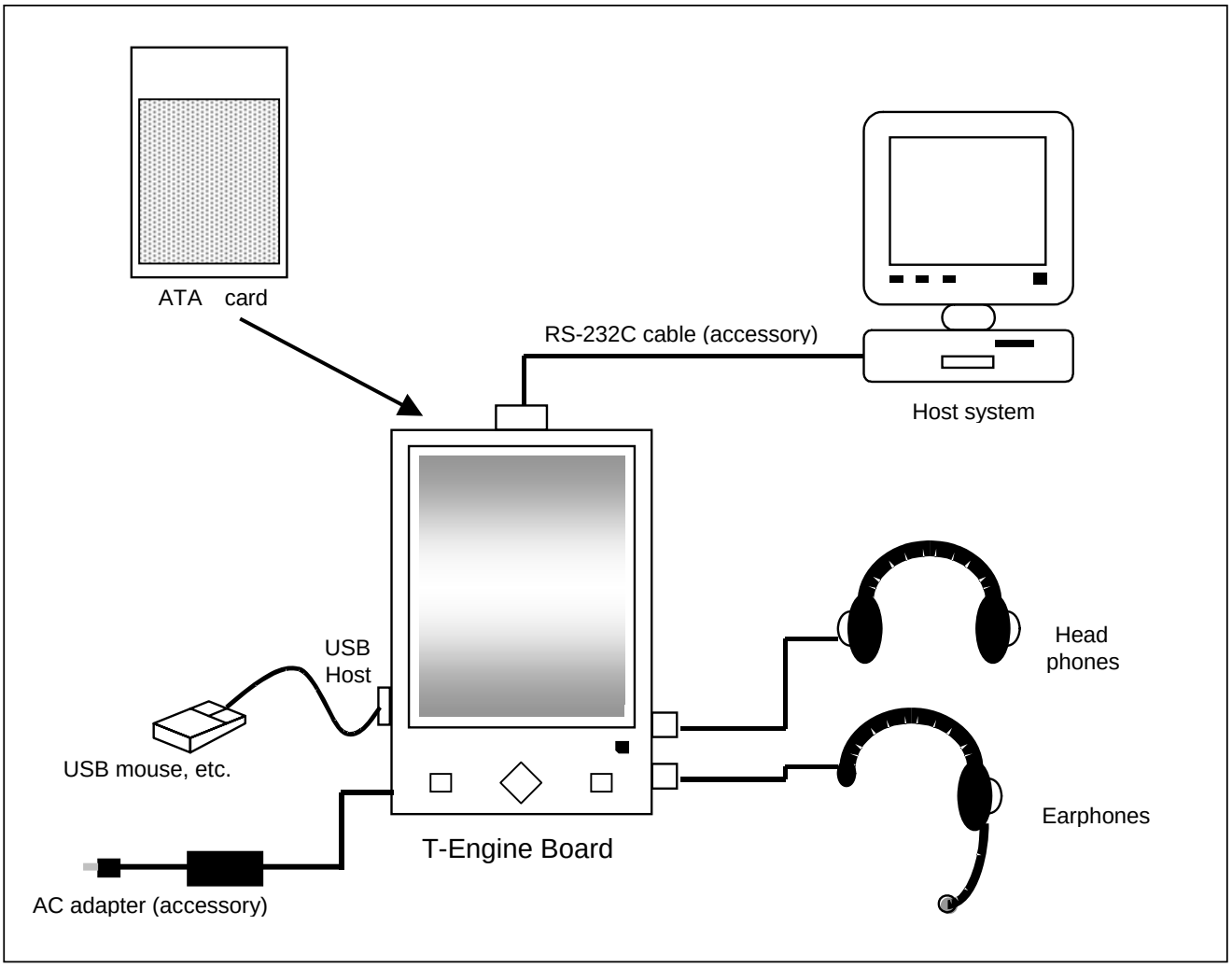


Figure 1.1 System configuration

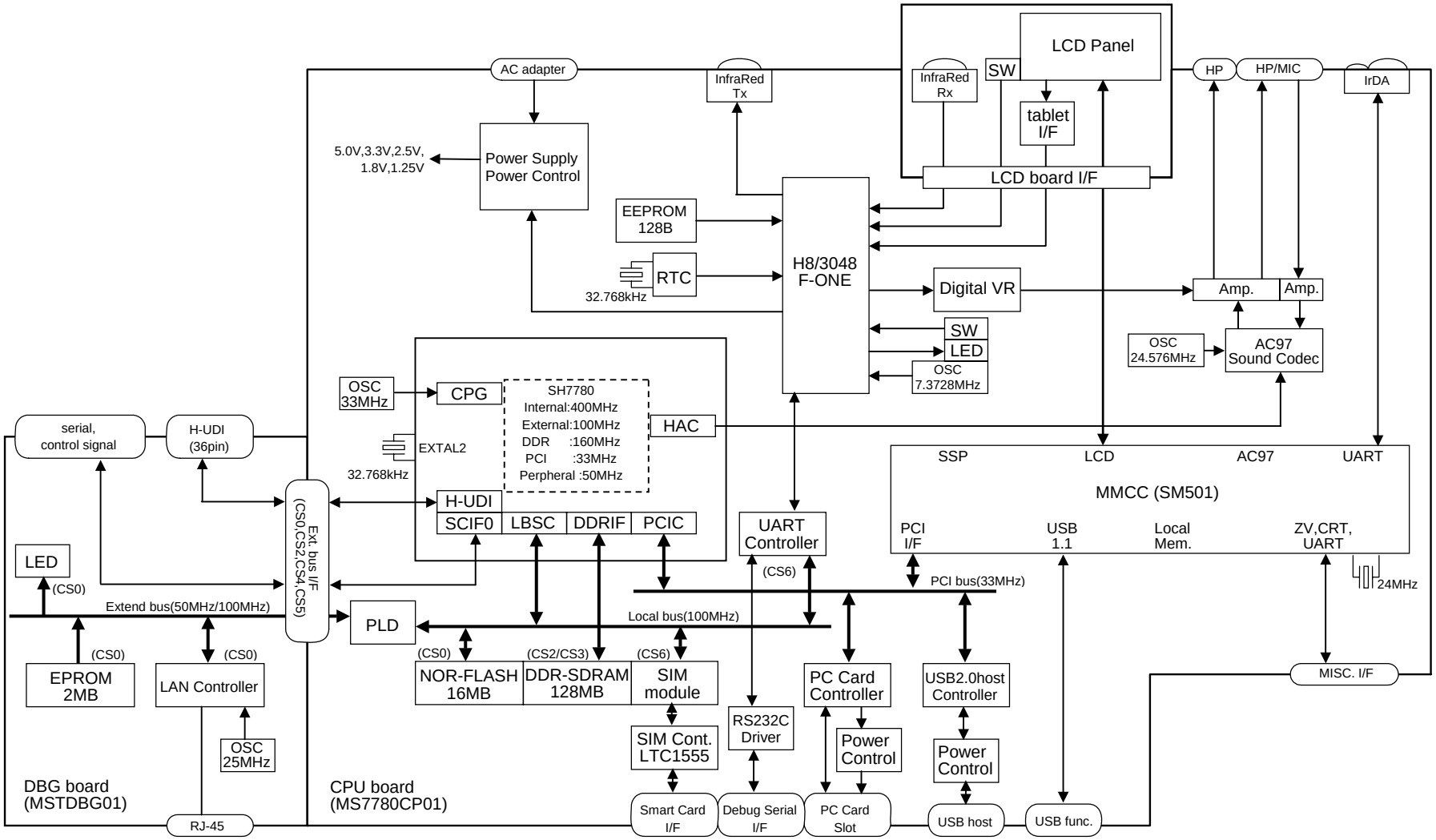


Figure 1.2 T-Engine Block Diagram

1.3 T-Engine Appearance

T-Engine Board consists of three boards: CPU, LCD and debug. Figure 1.3 is an external view of the T-Engine. Figures 1.4 to 1.6 show the appearances of the respective boards (LCD, CPU and debug).

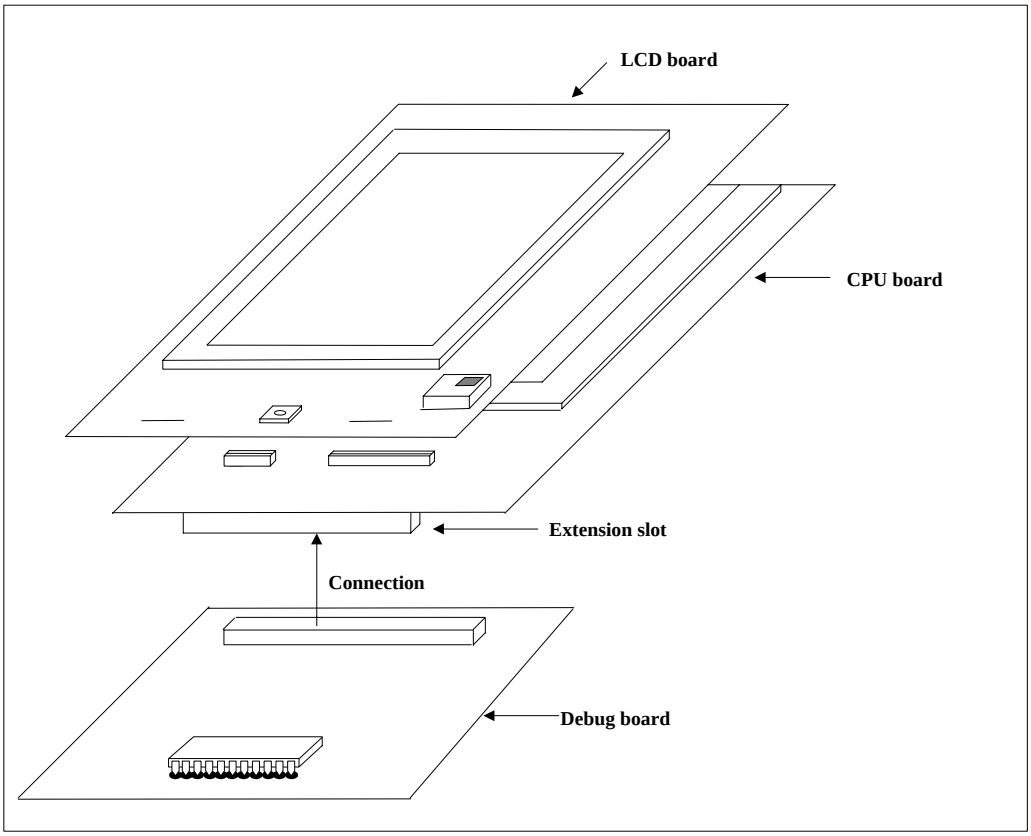


Figure 1.3 T-Engine - External View

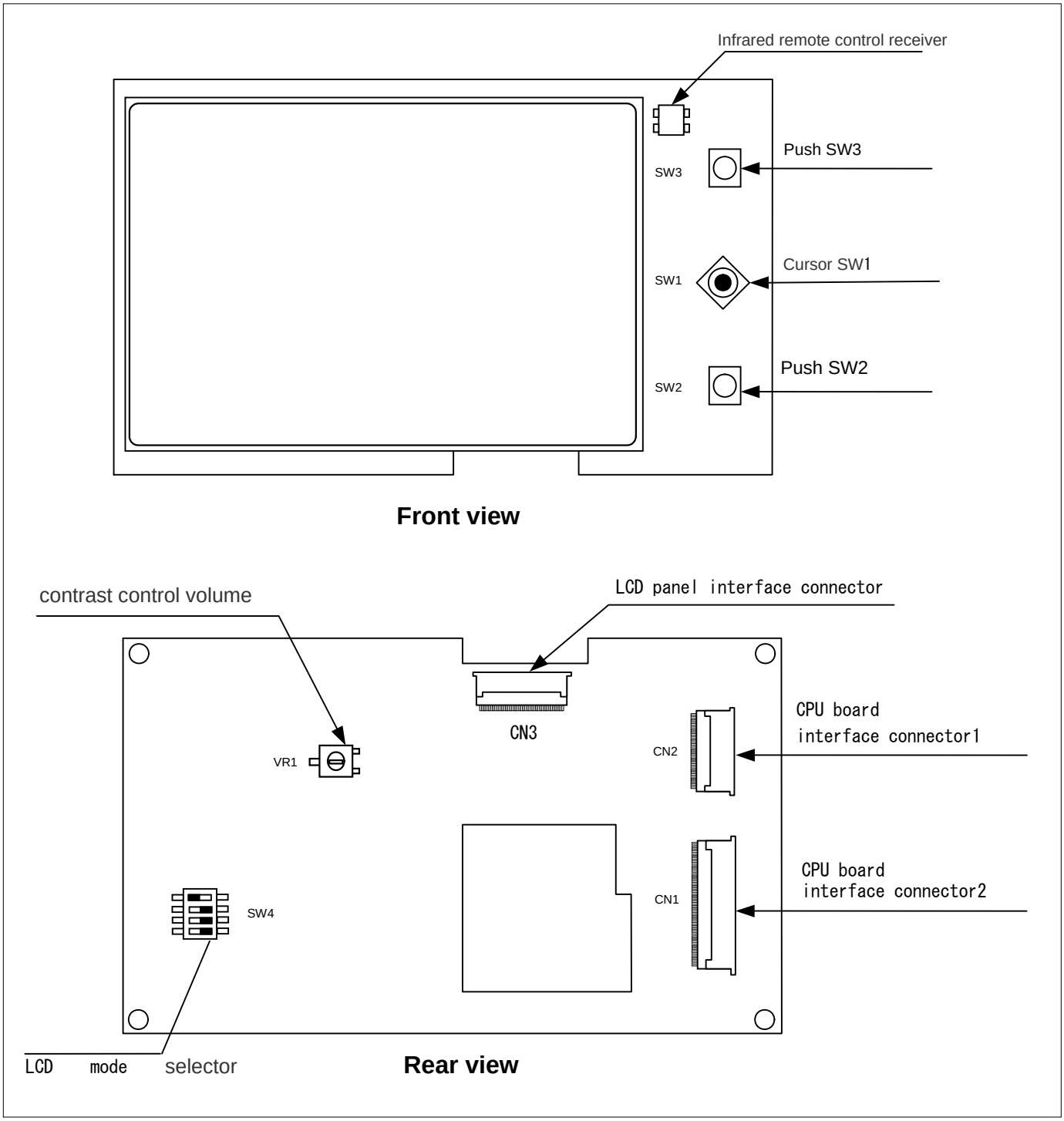
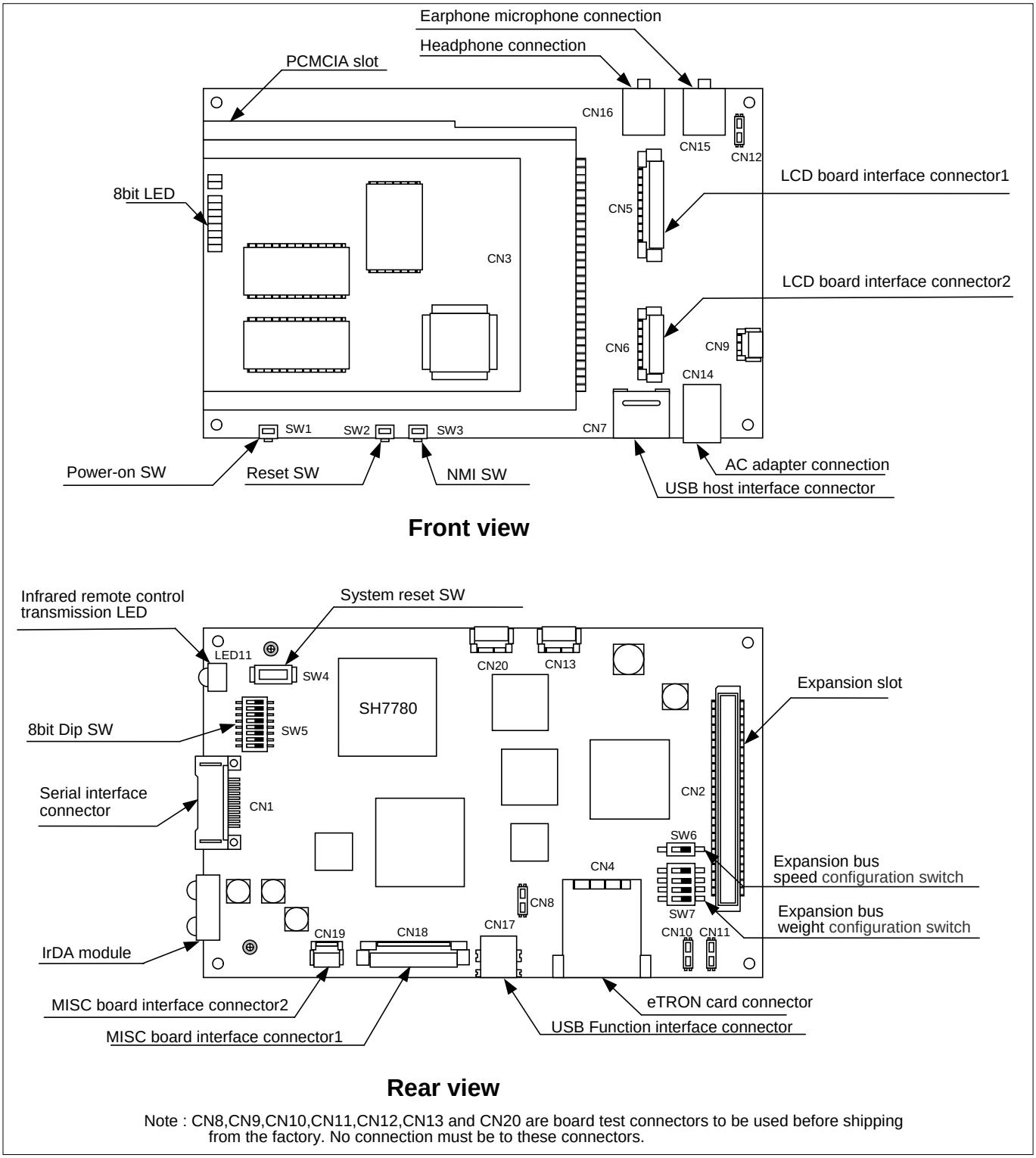


Figure 1.4 LCD Board - External View



Note : CN8,CN9,CN10,CN11,CN12,CN13 and CN20 are board test connectors to be used before shipping from the factory. No connection must be to these connectors.

Figure 1.5 CPU Board - External View

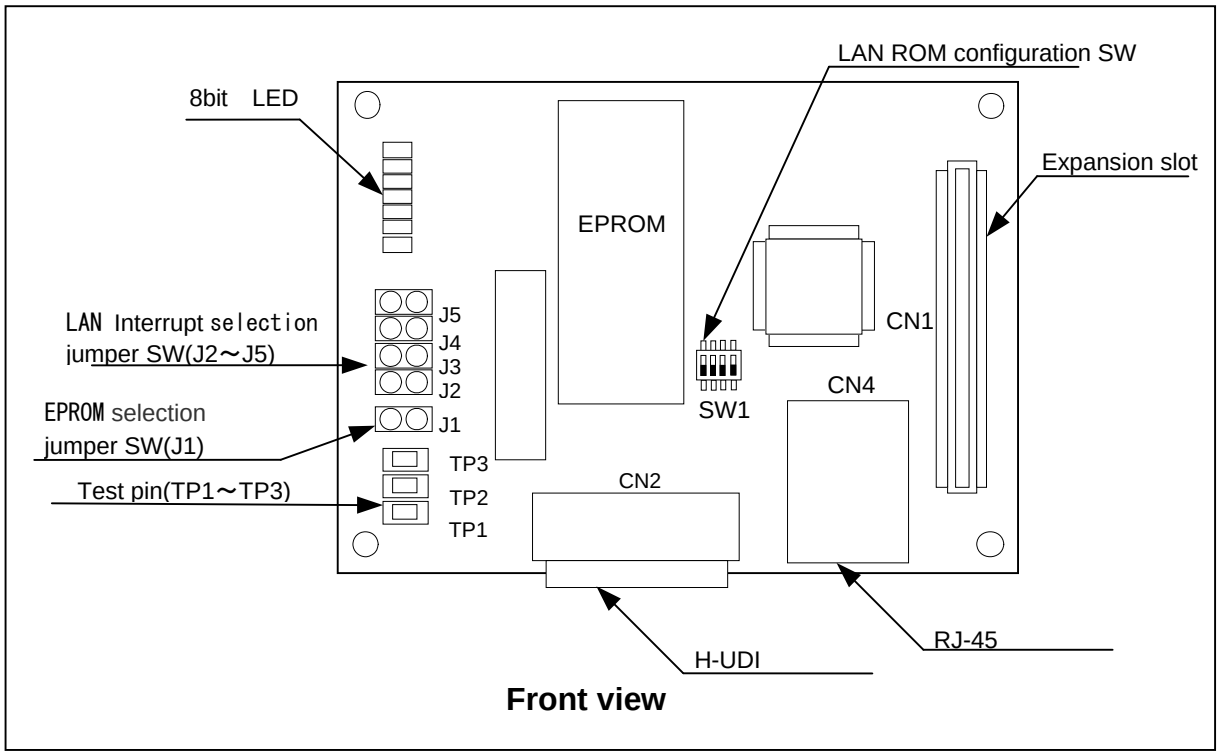


Figure 1.6 Debug Board - External View

1.4 T-Engine Specifications

Table 1.2 summarizes the T-Engine function specifications. and Table 1.3 the power supply, dimensions, and environmental specifications.

Table 1.2 T-Engine Function Specifications

Item	Specifications	Remarks
CPU	SH7780(SH-4A) Model name : R8A77800ANBGV(RENESAS) Input clock : 33MHz Internal clock(Ick) : 400MHz(× 12) Peripheral (Pck) : 33MHz(× 1) DDR clock(DDRck) : 133MHz(× 4) Bus clock(Bck) : 66MHz(× 2) PCI clock : 33MHz	Clock mode = 12 MODE[7,2,1,0] = 1100
NOR-FLASH	Capacity: 16MB Model name : S29GL128N10TFI010(SPANSION) × 1	To be connected via the LBSC Bit wide : 16bit
DDR-SDRAM	Capacity: 128MB Model name : MT46V32M16P-6T(MICRON) × 2	To be connected via the DDRIF Bit wide : 32bit
PCMCIA I/F (SHPC)	1 slot Controller : PCI1510ZGU(TI)	To be connected via the PCIC
Serial I/F	2ch Controller : XR16L2550IM-F(EXAR)	chA : H8/3048F-ONE I/F chB : Monitor for debugging
Mobile multimedia companion chip (MMCC)	Model name :SM501GX08LF01-AB(SiliconMotion) built-in RAM : 8MB	To be connected via the PCIC
TFT color LCD module	Model name :LS037V7DW01(SHARP) Display color: 262,144 colors Display area: 240(H) x 320(V)pixels 480(H) x 640(V)pixels Display controller : built-in MMCC LCD controller Touch panel controller : ADS7843E(TI)	with Touch panel
USB Host I/F	1ch Controller : uPD720101F1-EA8-A (NEC) conform to USB Specification Rev2.0	To be connected via the PCIC Connector : TypeA
USB Function I/F	1ch Controller : built-in MMCC USB controller conform to USB Specification Rev1.1	Connector : Type miniB
Sound I/F	Stereo headphone output : 2ch(Lch/Rch) Earphone microphone : Output 1ch(Rch)/Input 1ch Controller : STAC9751T(SIGMATEL)	To be connected via the HAC (built-in SH7780)
eTRON Card I/F	SIM Power Controller Model name : LTC1555LEGN-1.8#PBF(LTC)	To be connected via the LBSC
LAN I/F	1ch Controller : LAN91C111-NU(SMSC)	To be connected via the LBSC
IrDA I/F	1ch Controller : IrDA controller with a built-in MMCC conform to IrDA Specification Rev1.1 (SIR mode only)	
Power controller	H8/3048F-ONE Model name : HD64F3048BVTE25V(RENESAS) Operating frequency : 7.3728MHz	The control SH7780 working must be interfaced via the serial chA.
RTC	1ch Model name : RV5C348B-F(RICOH)	via H8/3048
Serial EEPROM	Capacity: 128B Model name : BR93L46FJ-W(ROHM)	
Infrared remote control	Transmission Model name : GL390(SHARP) Reception Model name :GP1US301XP(SHARP) Reception carrier: 38kHz	

1.5 Use environmental condition

Table 1.3 lists the environment conditions under which the T-Engine board can be used. Table 1.4 shows the permissible current that each power supply of the board can supply to external devices.

Table 1.3 Power supply, Dimensions, and Environmental Specifications of the T-Engine Board

Item	Specifications
Environment	Operating conditions - Temperature: 10-35ºC - Humidity: 30 to 85% RH (no dew condensation occurs) Ambient gas: no corrosive gas
Operating voltage	DC 5.6VDC
Dissipation current	600mA
Dimensions	CPU board: 120mm x 75mm LCD board: 120mm x 75mm Debug board: 101mm x 75mm

Table 1.4 Permissible Current Supplied Externally by T-Engine Supply Voltage

Supply voltage	Permissible current	Locations subject to current supply
5V	250mA	• PCMCIA card power supply • USB bus power • Expansion slot
3.3V	250mA	• PCMCIA card power supply • Expansion slot

⚠ CAUTION

- Table 1.3 shows the maximum dissipation current of T-Engine (comprising only the CPU board, LCD board, and debug board) without external devices.
- Table 1.4 shows the sum of permissible current in all the powered devices on T-Engine. Accordingly, when a current of 100mA is used for the PCMCIA card supply voltage (5V), the currents of the USB bus power or expansion slot is 150mA (250mA to 100mA). This is true for the supply voltage 3.3V.
- When the PCMCIA card, etc. is powered from the internal power supply of T-Engine, the current must not exceed the permissible current of each power supply shown in Table 1.4. Otherwise, there is a risk of electric shock, heat, or fire.

2. Installation

2.1 Host System Connection

To communicate the host system, connect the serial interface connector (CN1) of the T-Engine board with an RS-232C interface cable (accessory). Figure 2.1 shows the host system connection method. Figure 2.2 shows the pins of the serial interface connector. Table 2.1 shows the signals of the serial interface connector.

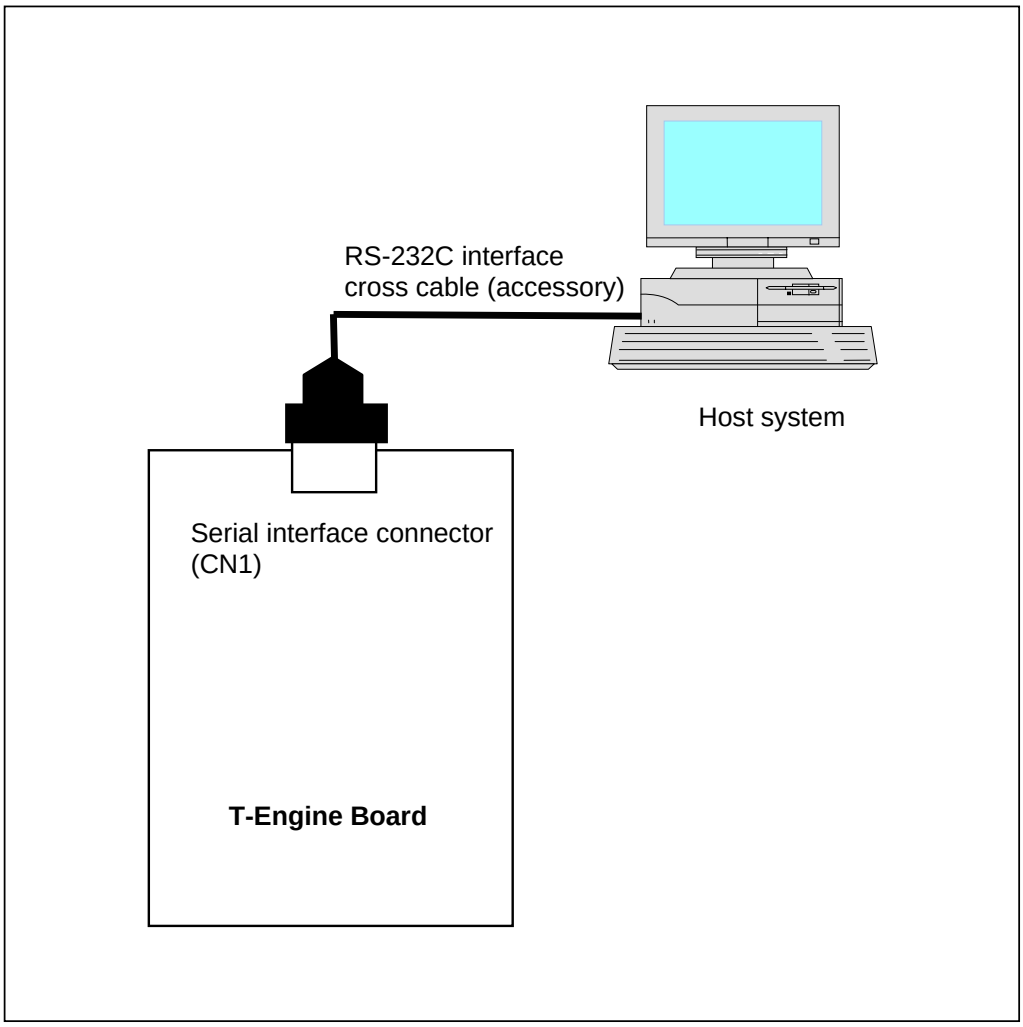


Figure 2.1 Host System Connection

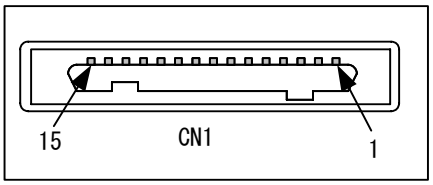


Figure 2.2 Serial Interface Connector Pins

Table 2.1 Serial Interface Connector Signals

Pin No.	Signal name	I/O	Remarks
1	GND	-	
2	TxD	Output	TXB(UART)
3	RxD	I	RXB(UART)
4	GND	-	
5	RTS	O	RTSB(UART)
6	CTS	I	CTSB(UART)
7	GND	-	
8	Reserved	-	ISP TCK(*)
9	Reserved	-	GND(*)
10	Reserved	-	ISP TMS(*)
11	Reserved	-	ISP Plug(*)
12	Reserved	-	ISP BScan(*)
13	Reserved	-	ISP TDI(*)
14	Reserved	-	ISP TDO(*)
15	Reserved	-	Vcc(3.3V) (*)

*: These pins are used only to test the board when it is shipped from the factory.

Don’t use these pins for any other purpose.

2.2 AC Adapter Connection

Figure 2.3 shows an AC adapter connection method. As shown in Figure 2.3, connect the plug to the AC adapter connector of the T-Engine board (1), then connect the adapter cord to the receptacle (2).

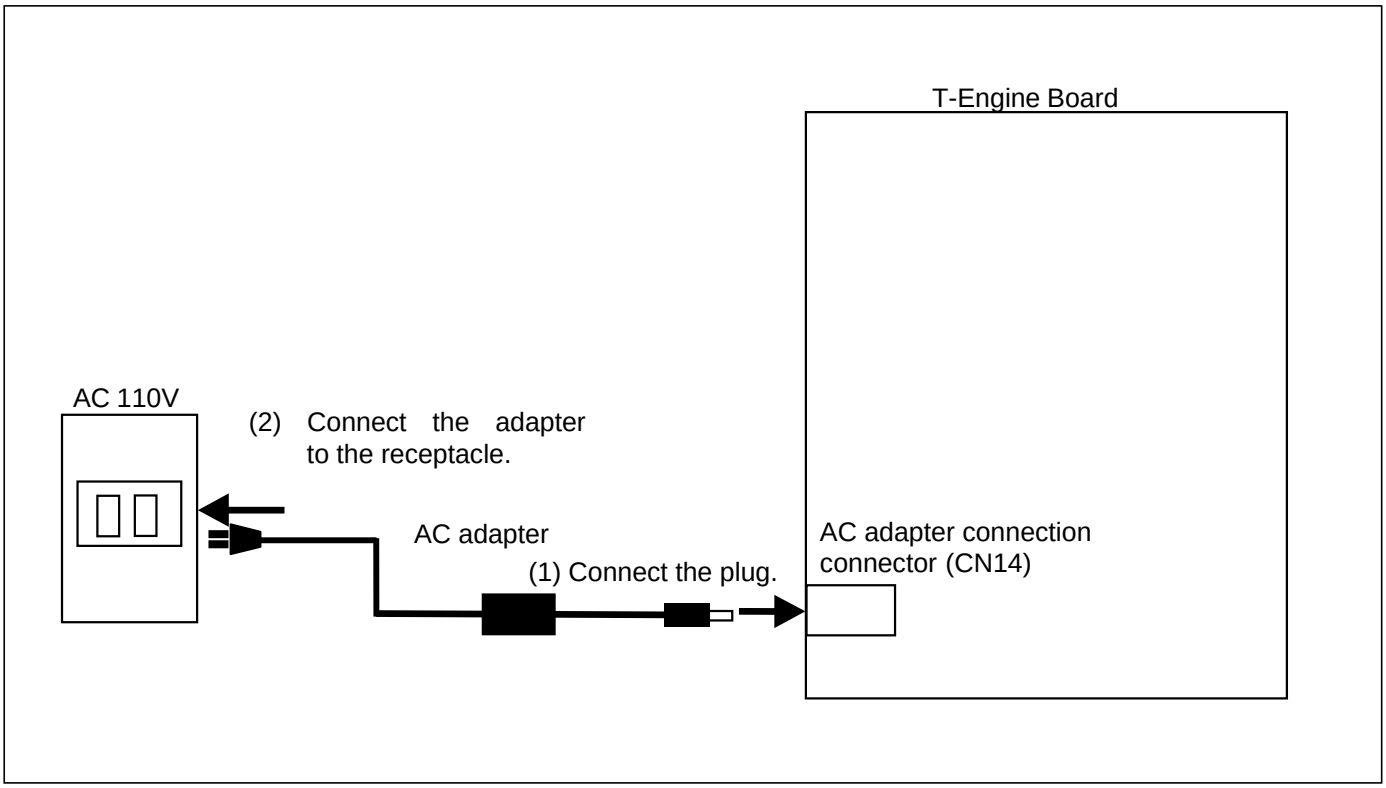


Figure 2.3 AC Adapter Connection Cord

⚠ CAUTION

- Don't put heavy things on the AC adapter cord. To avoid the risk of electric leakage, fire, or electric shock, don't damage or modify the AC adapter cord.
- To avoid the risk of electric shock, don't unplug the AC adapter cord with wet hands. To avoid the risk of cord damage, electric shock, or fire, don't pull on the AC adapter cord; rather, grasp and pull the plug to disconnect the AC adapter cord.
- When connecting the AC adapter to the receptacle, check the polarity and connection beforehand to avoid the risk of electric shock, fire, or fault.

2.3 Turning ON or OFF the T-Engine Board

To turn the T-Engine board ON or OFF, press the power-on switch (SW1) on the CPU board. To turn ON the T-Engine board, press and hold the switch for 0.5 seconds or more. To turn it OFF, press and hold this switch for 2 seconds or more while the T-Engine board is powered.

2.4 Using the Debug Board

2.4.1 Debug Board Function

When the debug board has been connected to the T-Engine, the following functions can be implemented:

(1) Run the program stored in the EPROM on the debug board to refresh the flash memory on the T-Engine board. The H8/3048F-One firmware can be refreshed. For details on flash memory refresh, refer to 10. “Flash Memory Refresh.”

(2) All 8-bit LEDs on the debug board can be turned on or off from the SH7780. The software execution state can be monitored by controlling the ON/OFF state of these LEDs.

(3) The H-UDI debugger (to be connected to the H-UDI and AUD pins of the SH7780) can be used.

2.4.2 Debug Board Connection

Figure 2.4 shows a debug board connection method. Connect the debug board to the expansion slot (CN2) on the T-Engine board.

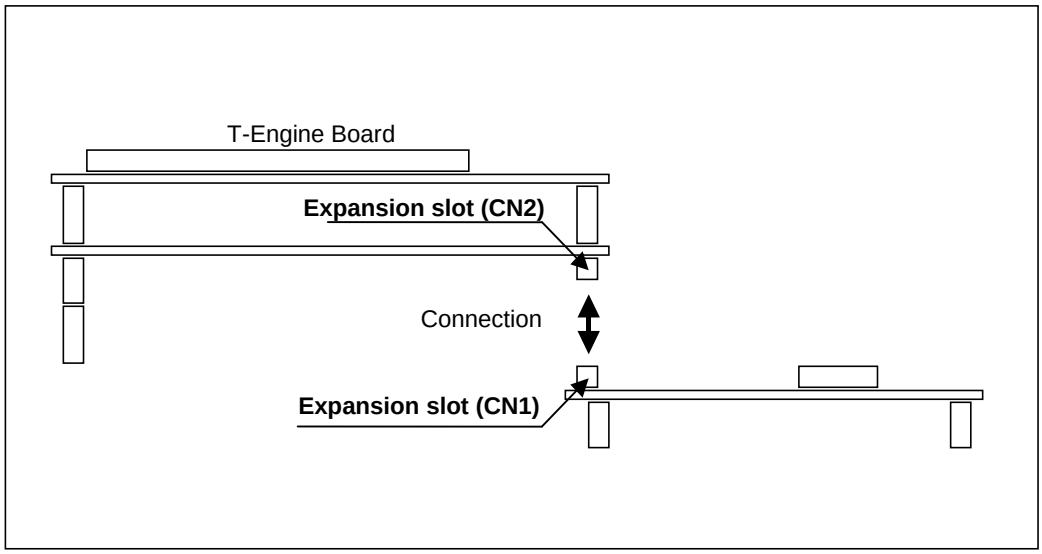


Figure 2.4 Debug Board Connection

⚠ CAUTION

Turn off the T-Engine before connecting the debug board or detaching the EPROM.
When reattaching the EPROM, check the connecting direction as shown in Figure 2.5.

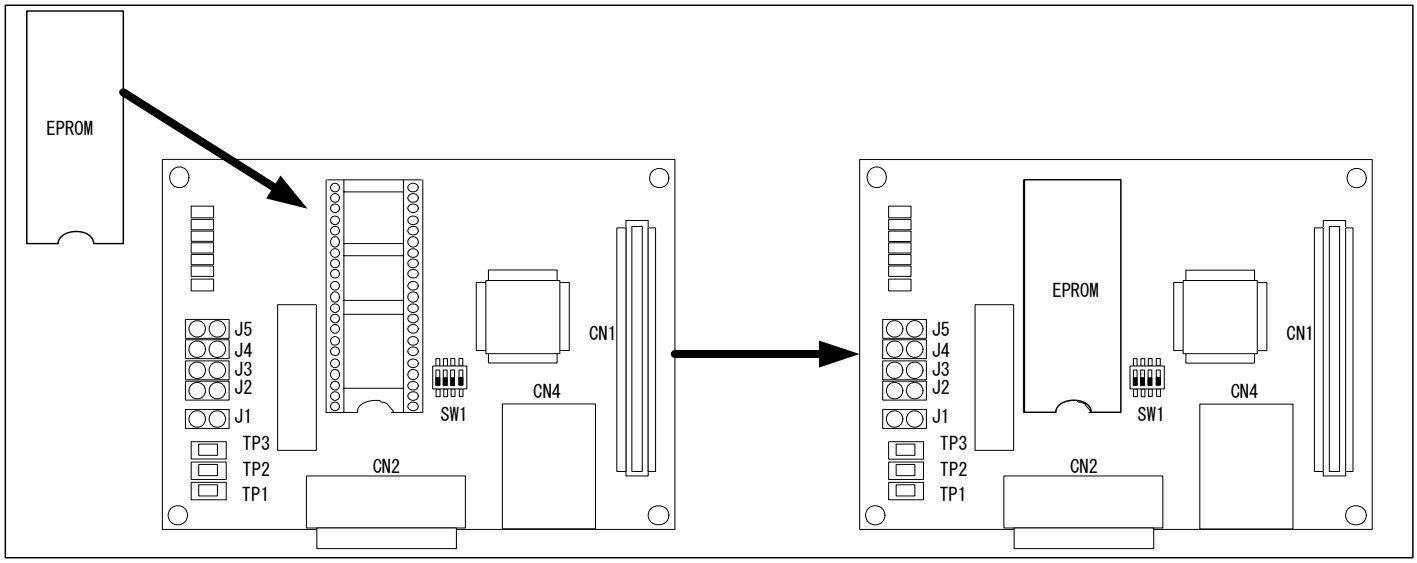


Figure 2.5 EPROM Connection

2.4.3 Debug Board Jumper Switches

Table 2.2 describes a method for setting the EPROM selection jumper switch (J1) on the debugger board.

Table 2.3 describes the method for configuring the LAN interrupt source via jumper switch (J2,J3,J4,J5) on the debugger board. For details of a memory map during debug board connection, refer to 4. “Memory Map.”

Table 2.2 Setting the EPROM Selection Jumper Switch (J1)

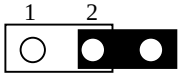
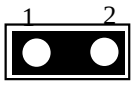
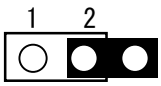
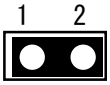
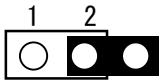
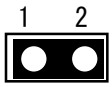
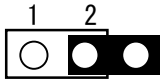
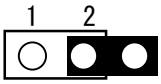
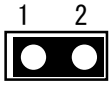
Jumper switch	Setting	Description
J1	 Pins 1 and 2 must be open	Debug board resources are assigned to area 0 on the SH7780 board as shown below. (Factory setting) - The flash memory on the T-Engine board is assigned to an address range from h'00000000 to h'00FFFFFF. - The EPROM mounted on the debug board is assigned to an address range from h'01000000 to h'0103FFFF. - The LAN controller mounted on the debug board is assigned to an address range from h'01400000 to h'017FFFFF. - The 8-bit LEDs mounted on the debug board are assigned to an address range from h'01800000 to h'01BFFFFF.
	 Pins 1 and 2 must be short-circuited.	Debug board resources are assigned to area 0 on the SH7780 board as shown below. - The EPROM mounted on the debug board is assigned to an address range from h'00000000 to h'003FFFFF. - The LAN controller mounted on the debug board is assigned to an address range from h'00400000 to h'007FFFFF. - The 8-bit LEDs mounted on the debug board are assigned to an address range from h'00800000 to h'00BFFFFF. - The flash memory on the T-Engine board is assigned to an address range from h'01000000 to h'01FFFFFF.

Table 2.3 Setting the LAN interrupt configuration jumper switch(J2,J3,J4,J5)

Jumper SW	Setting	Description
J2	 1−2 open	LAN controller's interrupt is not connected with external interrupt 0.
	 1-2 short-circuit	LAN controller's interrupt is connected with external interrupt 0. (Factory setting)
J3	 1−2 open	LAN controller's interrupt is not connected with external interrupt 1. (Factory setting)
	 1-2 short-circuit	LAN controller's interrupt is connected with external interrupt 1.
J4	 1−2 open	LAN controller's interrupt is not connected with external interrupt 2. (Factory setting)
	 1-2 short-circuit	LAN controller's interrupt is connected with external interrupt 2.
J5	 1−2 open	LAN controller's interrupt is not connected with external interrupt 3. (Factory setting)
	 1-2 short-circuit	LAN controller's interrupt is connected with external interrupt 3.

2.4.4 8-bit LEDs on the Debug Board

The low-order 8 bits (D7 to D0) of the SH7780 data bus are connected to the 8-bit LEDs placed on the debug board. The 8-bit LEDs can be turned on or off by writing data to an area assigned for the LEDs through D7 to D0. When a value of 1 is written to a bit, the corresponding LED is turned off. When a value of 0 is written to the bit, it is turned on. The 8-bit LED area is common to the EPROM area. When writing takes place, LED access takes place. When reading takes place for this area, EPROM access takes place. Note that LED access must take place in words to enable the lower 8 bits (D7 to D0).

2.4.5 H-UDI Debugger Connection

The debug board allows the H-UDI debugger to be connected to the pin 36 (CN2) of the H-UDI (User Debugging Interface) connector. Connect the H-UDI and AUD pins of the SH7780 board to the H-UDI connector. Figure 2.6 shows a method for connecting the H-UDI debugger. Connect an H-UDI debugger cable to the H-UDI connector (CN2) of the debug board. Note that the following H-UDI debugger can be connected to T-Engine. For details on the H-UDI debugger connection/setup procedure, refer to the pertinent manual of the product.

- Renesas Technology Corporation

  E10A-USB Emulator Model name: HS0005KCU02H (AUD)

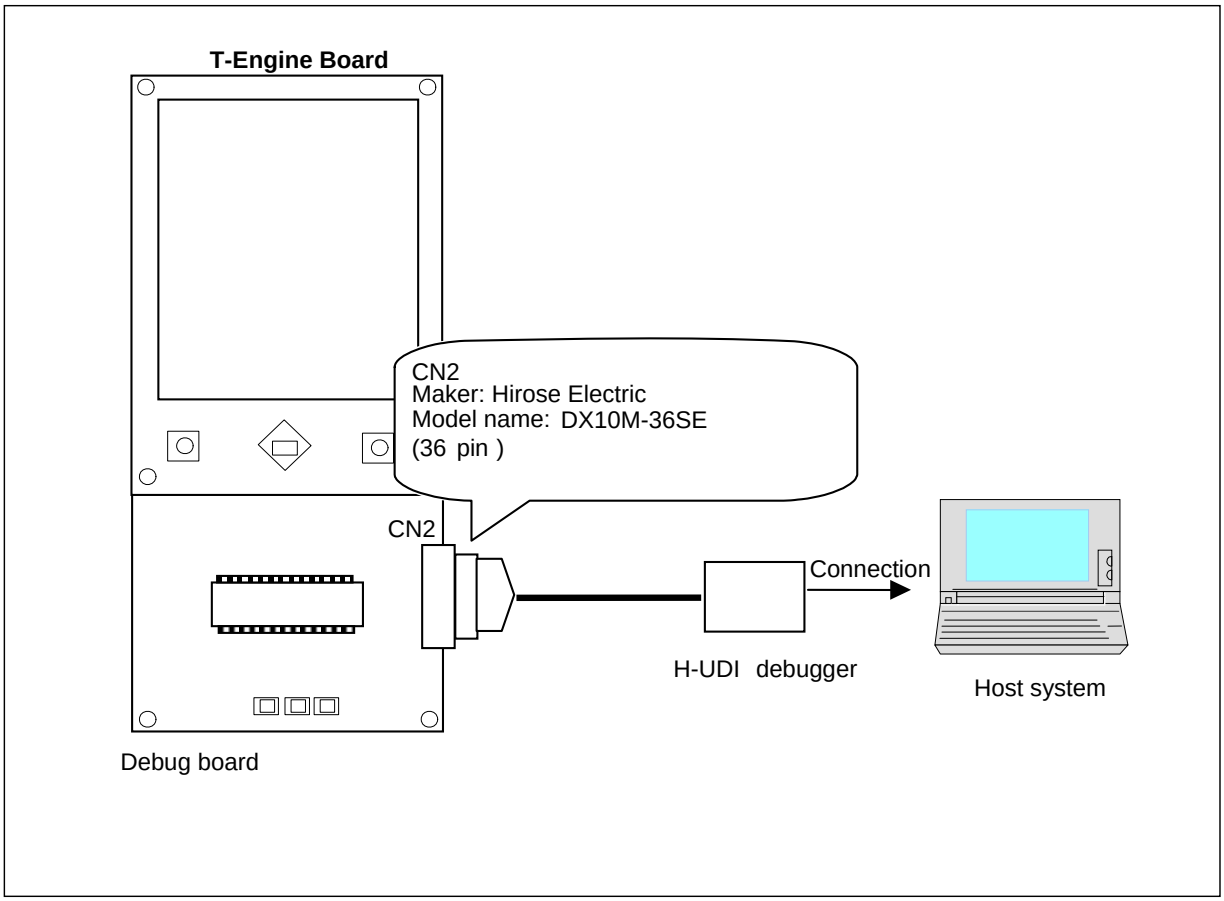


Figure 2.6 H-UDI Debugger Connection

3. Switches

3.1 CPU Board Switches

Figure 3.1 shows the location of the switches (SW1 to SW7) on the CPU board. In addition, this section gives a brief description of each switch in (1) to (7).

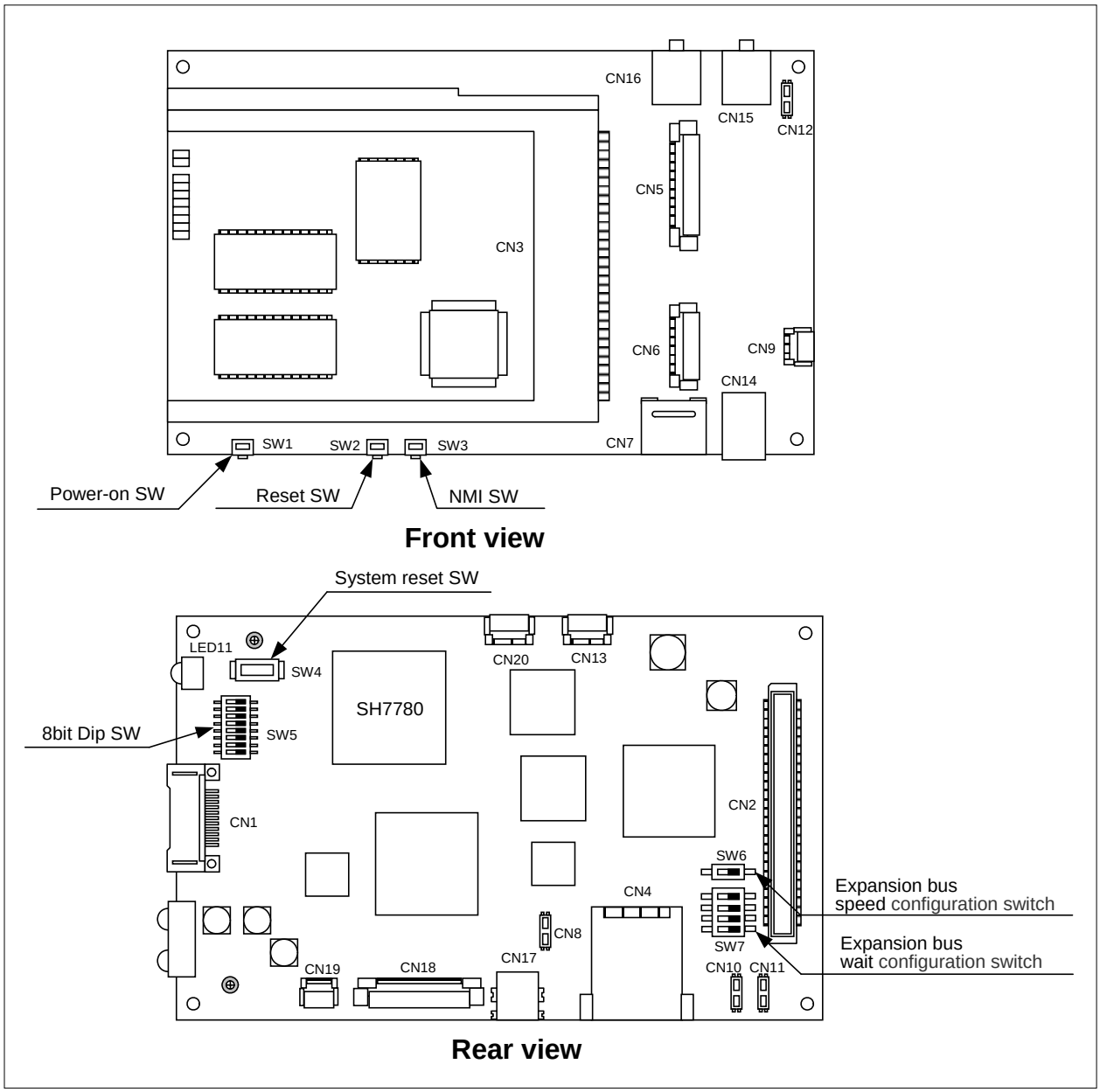


Figure 3.1 CPU Board Switches (SW1 to SW7)

(1) Power on Switch (SW1)

This switch turns on or off T-Engine. To turn on T-Engine, press and hold down this switch for 0.5 seconds or more. To turn it off, press and hold down this switch for 2 seconds or more when T-Engine is being powered.

(2) Reset Switch (SW2)

This switch resets T-Engine. To reset devices other than the H8/3048-ONE, press this switch. To reset and restart T-Engine, release this switch. In this case, the values of H8/3048-ONE internal registers are not initialized. Among the control registers, the values of those that can be accessed by SH7780 are initialized but the others are not (i.e., their values are retained). For more details, refer to 6.13 “Initial Values of the Power Supply Controller Register.”

(3) NMI Switch (SW3)

This switch controls the SH7780 NMI pin. Press this switch and the SH7780 NMI pin will go “Low.” Release this switch, and the NMI pin will go “High.”

(4) System Reset Switch（SW4）

The system reset switch controls the hardware reset for T-Engine. All devices on T-Engine are reset while this system reset switch is pressed and held down. T-Engine is turned off when this switch is released. It is turned on and activated when the power-on switch is pressed. However, the T-Engine is turned on automatically and activated when this switch is released if SW5-7 switch is set ON.

(5) 8-bit DIP Switch (SW5)

Figure 3.2 shows the setting of an 8-bit DIP switch. This DIP switch is connected to SH7780’s pins PTH7, PTH5, PTK6, PTK3, PTK2, PTE3 and MD5 of the terminal. Be sure to turn off the power-on switch before setting the DIP switch.

(a) Switches SW5-1 to SW5-6 are connected to SH7780’s pins PTH7, PTH5, PTK3, PTK2, PTE3, PTK6 (input pins).

SW No.	connecting pin name	SW No.	connecting pin name
SW5-1	PTK6	SW5-4	PTK3
SW5-2	PTE3	SW5-5	PTH5
SW5-3	PTK2	SW5-6	PTH7

ON: The input pin goes “Low.”

OFF: The input pin goes “High.” (Factory setting)

(b) The SW5-7 switch is used to set the power-on condition of T-Engine.

ON: T-Engine is powered when power supply takes place through the AC adapter.

OFF: T-Engine is powered when the power-on switch is pressed. (Factory setting)

(c) The SW5-8 switch is connected to SH7780's pin MD5. The SW5-8 switch is used to set the type of endian for SH7780 operation.

ON: The MD5 pin goes “Low” to set the big endian for SH7780 operation.

OFF: The MD5 pin goes “High” to set the little endian for SH7780 operation. (Factory setting)

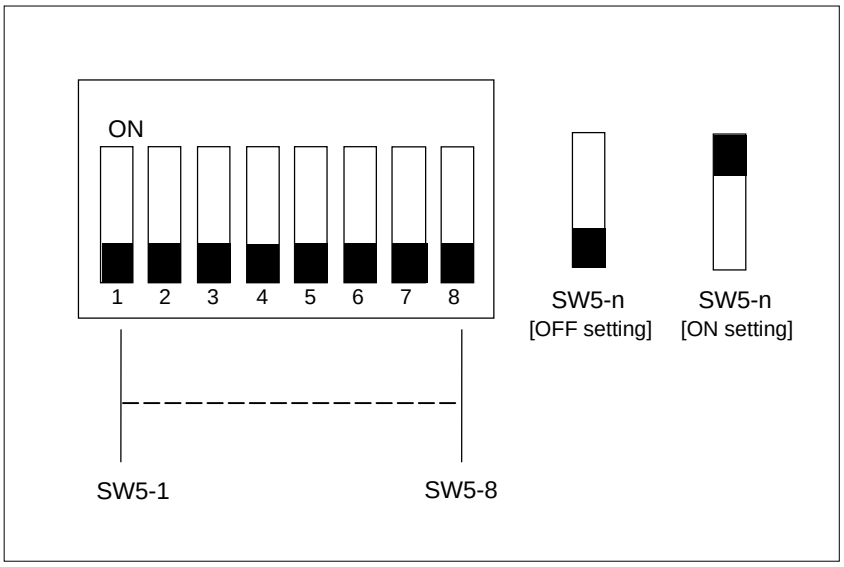


Figure 3.2 Setting the 8-bit DIP Switch

(6) Expansion bus speed configuration Switch (SW6)

Figure 3.3 shows how to set the expansion bus speed configuration switch.

The operating clock frequency of the expansion bus changes depending on how this switch is set.

ON : Low expansion bus speed. The operating clock frequency of the expansion bus is half that of CKIO.

OFF : Normal expansion bus speed. The operating clock frequency of the expansion bus is the same as that of CKIO. (Factory settings)

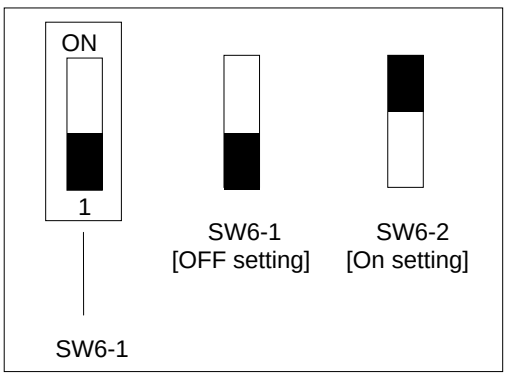


Figure 3.3 Setting the Expansion bus speed configuration switch

(7) Expansion bus Wait-cycle configuration Switch (SW7)

Figure 3.4 shows how to set the expansion bus wait-cycle configuration switch.

This switch sets the number of cycles automatically inserted in expansion bus access cycles. The user can configure to set 1 to 4 wait cycles to be inserted. However, if more tan one bit is set to ON position, one wait cycle is assumed. Note, however, that settings of this switch are effective only when the expansion bus speed is set to low speed by the expansion bus speed configuration switch.

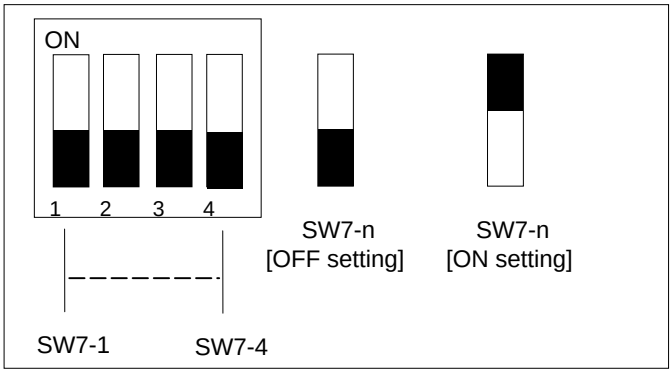


Figure 3.4 Setting the Expansion bus Wait-cycle configuration Switch

3.2 LCD Board Switch

3.2.1 Application Switch

The states of the cursor switch (SW1) and push-button switches (SW2 and SW3) are signaled to the SH7780 through the power supply controller. For details, refer to 6. “Power Supply Controller.”

3.2.2 LCD configuration switch

Figure 3.5 shows the setting of an 4-bit DIP switch.

(1) SW4-1 : The setting of “Display Mode”.

SW4-1 : ON The Display Mode is VGA(480X640)

SW4-1 : OFF The Display Mode is QVGA(240X320) (Factory setting)

(2) SW4-2 : The setting of “Vertical scan of the LCD display”

SW4-2 : ON Scan direction is from (X,Y) toward (X,1)

SW4-2 : OFF Scan direction is from (X,1) toward (X,Y) (Factory setting)

(3) SW4-3 : The setting of “Horizontal scan of the LCD display”

SW4-3 : ON Scan direction is from (X,Y) toward (1,Y)

SW4-3 : OFF Scan direction is from (1,Y) toward (X,Y) (Factory setting)

(4) SW4-4 : TBD

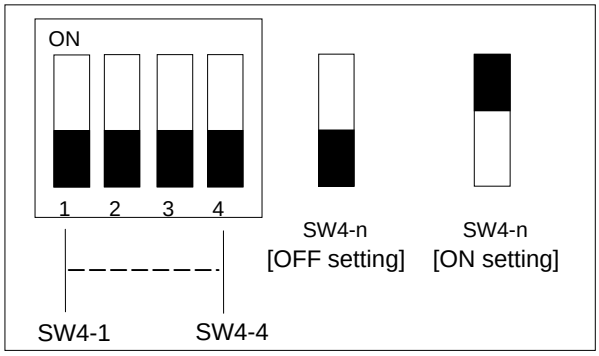


Figure 3.5 Setting the 4-bit DIP Switch

3.3 Debug board switch

3.3.1 LAN_ROM configuration Switch (SW1)

Figure 3.6 shows the setting of an LAN_ROM configuration switch.

This switch is EEPROM setting switch.

SW No.	connecting pin name (LAN controller)	function
SW1-1	ENEEP	This switch is EEPROM access control of LAN controller. ON: Impossible to access to EEPROM OFF: Possible to access to EEPROM (Factory setting)
SW1-2	IOS2	These switches specify offset when LAN controller read setup information from EEPROM. Factory setting : All OFF
SW1-3	IOS1	
SW1-4	IOS0	

For details, refer to data sheet of LAN controller.

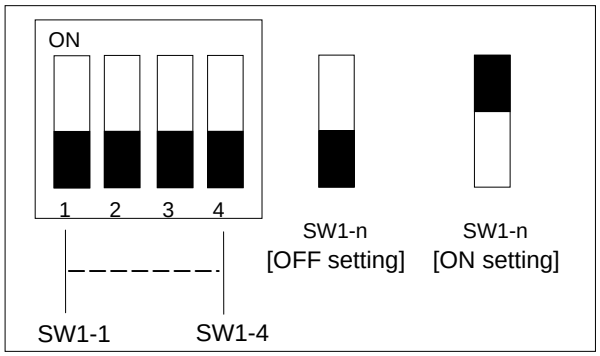


Figure 3.6 Setting the LAN_ROM setting Switch

4. Memory Map

4.1 Memory Map for the T-Engine Board

Table 4.1 shows an SH7780 memory map for the T-Engine board without expansion board.

Table 4.1 SH7780 Memory Map for T-Engine without Expansion Board

Area No.	Bus Width	Space	Space name	Device	Remarks
Area0	16bit	h'00000000 ～ h'00FFFFFF	Frash Memory area	Capacity：16MB S29GL128N10TFI010(SPANSION)×1	—
		h'01000000 ～ h'03FFFFFF	Unused area	—	—
Area1	8/16/ 32bit	h'04000000 ～ h'07FFFFFF	Expansion area	User's expansion space	assert ~CS2 of expansion bus I/F
Area2/ Area3	32bit	h'08000000 ～ h'0FFFFFFF	DDR-SDRAM area	Capacity：128MB MT46V32M16P-6T(MICRON)×2	
Area4	8/16/ 32bit	h'10000000 ～ h'13FFFFFF	Expansion area	User's expansion space	assert ~CS4 of expansion bus I/F
Area5	8/16/ 32bit	h'14000000 ～ h'17FFFFFF	Expansion area	User's expansion space	assert ~CS5 of expansion bus I/F
Area6	16bit	h'18000000 ～ h'18FFFFFF	SIM area	SmartCard I/F area	eTRON control
		h'19000000 ～ h'19FFFFFF	PLD register area	PLD built-in register	USB control Interrupt control etc.
		h'1A000000 ～ h'1AFFFFFF	UART-ChA area	UART XR16L2550IM-F(EXAR)×1	uses for I/F with H8/3048F-ONE
		h'1B000000 ～ h'1BFFFFFF	UART-ChB area		outputs to the connector for communications with the host system
Area7	—	h'1C000000 ～ h'1FFFFFFF	Reserve area	—	—

4.2 Memory Map during Debug Board Connection

Table 4.2 shows a memory map for the SH7780 when the debug board is connected to the T-Engine board and the jumper switch (J1) on the debug board is open. Table 4.3 also shows a memory map for the SH7780 when the debug board is connected to the T-Engine board and the jumper switch (J1) on the debug board is open. The areas other than area 0 are similar to Table 4.1.

Table 4.2 Memory Map during Debug Board Connection (J1: Open)

Area No.	Bus Width	Space	Space name	Device	Remarks
Area0	16bit	h'00000000 ～ h'00FFFFFF	Flash memory area	Capacity：16MB S29GL128N10TFI010(SPANSION)×1	－
		h'01000000 ～ h'013FFFFF	EPROM area	Capacity：2MB M27C160-100F1 (STMicroelectronics)×1	Resource on Debug board assert ~ EPROMCE of expansion bus I/F
		h'01400000 ～ h'017FFFFF	LAN area	LAN91C111-NU(SMSC)	
		h'01800000 ～ h'01BFFFFF	LED area	8bit LED	
		h'01C00000 ～ h'03FFFFFF	Unused area	－	－

Table 4.3 Memory Map during Debug Board Connection (J1: short-circuited)

Area No.	Bus Width	Space	Space name	Device	Remarks
Area0	16bit	h'00000000 ～ h'00FFFFFF	EPROM area	Capacity：2MB M27C160-100F1 (STMicroelectronics)×1	Resource on Debug board assert ~ EPROMCE of expansion bus I/F
		h'00400000 ～ h'007FFFFF	LAN area	LAN91C111-NU(SMSC)	
		h'00800000 ～ h'00BFFFFF	LED area	8bit LED	
		h'00C00000 ～ h'00FFFFFF	Unused area	－	－
		h'01000000 ～ h'01FFFFFF	Flash mamory area	Capacity：16MB S29GL128N10TFI010(SPANSION)×1	－
		h'02000000 ～ h'03FFFFFF	Unused area	－	－

5. Functional Blocks

5.1 PCMCIA

5.1.1 Block Description

Figure 5.1 shows the PCMCIA control block. As shown in Figure 5.1, the PCMCIA control block contains a controller (PCI1510ZGU from TI), a 68-pin PC card interface connector (CN3) and a power supply controller IC (TPS2211DB from TI). This controller interfaces with the card(s) conforming to the PC Card Standard 97.

Interrupts from the controller are connected to the SH7780's PCI interrupts (INTA/INTB/INTC selectable) and IRL interrupts via the PLD.

For details, refer toTI's PCI1510ZGU Manual.

TI Homepage: http://focus.ti.com/docs/prod/folders/print/pci1510.html

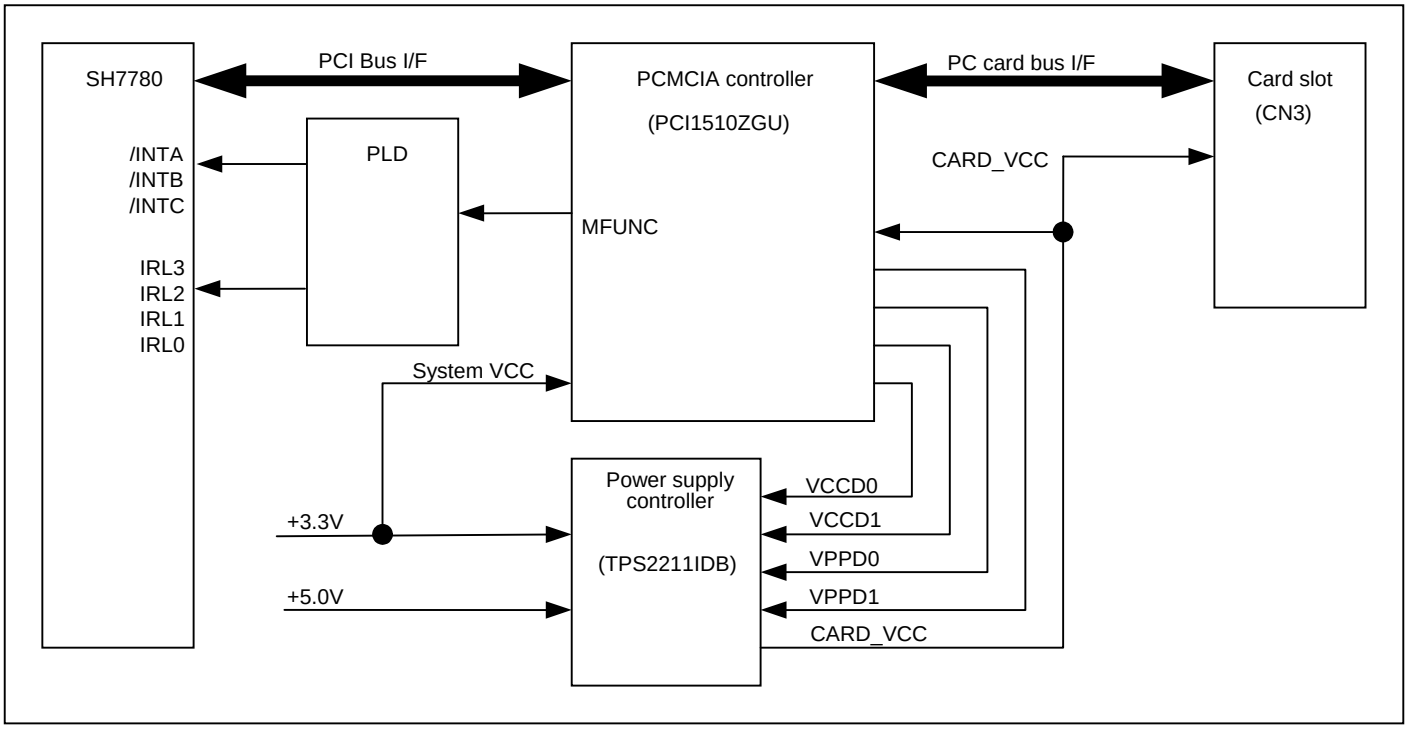


Figure 5.1 PCMCIA Control Block

5.1.2 Connector Pins

Table 5.1(1) and Table5.1(2) summarize the pins of a 68-pin PC card interface connector (CN3).

Table 5.1(1) PC Card Interface Connector Signal Pins

Pin	Memory card			I/O card		
	Signal name	I/O	Function	Signal name	I/O	Function
1	GND	-	Ground	GND	-	Ground
2	D3	I/O	Data bit 3	D3	I/O	Data bit 3
3	D4	I/O	Data bit 4	D4	I/O	Data bit 4
4	D5	I/O	Data bit 5	D5	I/O	Data bit 5
5	D6	I/O	Data bit 6	D6	I/O	Data bit 6
6	D7	I/O	Data bit 7	D7	I/O	Data bit 7
7	CE1#	I	Card enable	CE1#	I	Card enable
8	A10	I	Address bit 10	A10	I	Address bit 10
9	OE#	I	Output enable	OE#	I	Output enable
10	A11	I	Address bit 11	A11	I	Address b it 11
11	A9	I	Address bit 9	A9	I	Address bit 9
12	A8	I	Address bit 8	A8	I	Address bit 8
13	A13	I	Address bit 13	A13	I	Address bit 13
14	A14	I	Address bit 14	A14	I	Address bit 14
15	WE#	I	Write enable	WE#	I	Write enable
16	READY	O	Ready	IREQ#	O	Interrupt request
17	Vcc	-	Supply voltage	Vcc	-	Supply voltage
18	VPP1	-	Programmed supply voltage	VPP1	-	Programmed supply voltage
19	A16	I	Address bit 16	A16	I	Address bit 16
20	A15	I	Address bit 15	A15	I	Address bit 15
21	A12	I	Address bit 12	A12	I	Address bit 12
22	A7	I	Address bit 7	A7	I	Address bit 7
23	A6	I	Address bit 6	A6	I	Address bit 6
24	A5	I	Address bit 5	A5	I	Address bit 5
25	A4	I	Address bit 4	A4	I	Address bit 4
26	A3	I	Address bit 3	A3	I	Address bit 3
27	A2	I	Address bit 2	A2	I	Address bit 2
28	A1	I	Address bit 1	A1	I	Address bit 1
29	A0	I	Address bit 0	A0	I	Address bit 0
30	D0	I/O	Data bit 0	D0	I/O	Data bit 0
31	D1	I/O	Data bit 1	D1	I/O	Data bit 1
32	D2	I/O	Data bit 2	D2	I/O	Data bit 2
33	WP	O	Write Protect	IOIS16#	O	16bit I/O port
34	GND	-	Ground	GND	-	Ground

Table 5.1(2) PC Card Interface Connector Signal Pins

Pin	Memory card			I/O card		
	Signal name	I/O	Function	Signal name	I/O	Function
35	GND	-	Ground	GND	-	Ground
36	CD1#	O	Card detection	CD1#	O	Card detection
37	D11	I/O	Data bit 11	D11	I/O	Data bit 11
38	D12	I/O	Data bit 12	D12	I/O	Data bit 12
39	D13	I/O	Data bit 13	D13	I/O	Data bit 13
40	D14	I/O	Data bit 14	D14	I/O	Data bit 14
41	D15	I/O	Data bit 15	D15	I/O	Data bit 15
42	CE2#	I	Card enable	CE2#	I	Card enable
43	VS1#	O	Voltage sense	VS1#	O	Voltage sense
44	RFU	-	Reserved	IORD#	I	I/O read
45	RFU	-	Reserved	IOWR#	I	I/O write
46	A17	I	Address bit 17	A17	I	Address bit 17
47	A18	I	Address bit 18	A18	I	Address bit 18
48	A19	I	Address bit 19	A19	I	Address bit 19
49	A20	I	Address bit 20	A20	I	Address bit 20
50	A21	I	Address bit 21	A21	I	Address bit 21
51	Vcc	-	Supply voltage	Vcc	-	Supply voltage
52	VPP2	-	Programmed supply voltage	VPP2	-	Programmed supply voltage
53	A22	I	Address bit 22	A22	I	Address bit 22
54	A23	I	Address bit 23	A23	I	Address bit 23
55	A24	I	Address bit 24	A24	I	Address bit 24
56	A25	I	Address bit 25	A25	I	Address bit 25
57	VS2#	O	Voltage sense	VS2#	O	Voltage sense
58	RESET	I	Card reset	RESET	I	Card reset
59	WAIT#	O	Bus cycle expansion	WAIT#	O	Bus cycle expansion
60	RFU	-	Reserved	INPACK#	O	I/O port response
61	REG#	I	Register selection	REG#	I	Register selection
62	BVD2	O	Battery voltage detection	SPKR#	O	Audio digital waveform
63	BVD1	O	Battery voltage detection	STSCHG#	O	Card status change
64	D8	I/O	Data bit 8	D8	I/O	Data bit 8
65	D9	I/O	Data bit 9	D9	I/O	Data bit 9
66	D10	I/O	Data bit 10	D10	I/O	Data bit 10
67	CD2#	O	Card detection	CD2#	O	Card detection
68	GND	-	Ground	GND	-	Ground

5.1.3 Register Map

Table 5.2 shows a map for the PCMCIA controller registers.

Table 5.2(1) PCMCIA Control Registers Map ExCA Register Map

PCI Memory Address Offset	ExCA Register Name
h'800	Identification and revision
h'801	Interface status
h'802	Power control
h'803	Interrupt and general control
h'804	Card status change
h'805	Card status-change interrupt configuration
h'806	Address window enable
h'807	I/O window control
h'808	I/O window 0 start-address low byte
h'809	I/O window 0 start-address high byte
h'80A	I/O window 0 end-address low byte
h'80B	I/O window 0 end-address high byte
h'80C	I/O window 1 start-address low byte
h'80D	I/O window 1 start-address high byte
h'80E	I/O window 1 end-address low byte
h'80F	I/O window 1 end-address high byte
h'810	Memory window 0 start-address low byte
h'811	Memory window 0 start-address high byte
h'812	Memory window 0 end-address low byte
h'813	Memory window 0 end-address high byte
h'814	Memory window 0 offset-address low byte
h'815	Memory window 0 offset-address high byte
h'816	Card detect and general control
h'817	Reserved
h'818	Memory window 1 start-address low byte
h'819	Memory window 1 start-address high byte
h'81A	Memory window 1 end-address low byte
h'81B	Memory window 1 end-address high byte
h'81C	Memory window 1 offset-address low byte
h'81D	Memory window 1 offset-address high byte
h'81E	Global control
h'81F	Reserved
h'820	Memory window 2 start-address low byte
h'821	Memory window 2 start-address high byte
h'822	Memory window 2 end-address low byte
h'823	Memory window 2 end-address high byte
h'824	Memory window 2 offset-address low byte
h'825	Memory window 2 offset-address high byte
h'826	Reserved
h'827	Reserved
h'828	Memory window 3 start-address low byte
h'829	Memory window 3 start-address high byte
h'82A	Memory window 3 end-address low byte
h'82B	Memory window 3 end-address high byte
h'82C	Memory window 3 offset-address low byte
h'82D	Memory window 3 offset-address high byte
h'82E	Reserved
h'82F	Reserved

Table 5.2(2) PCMCIA Control Registers Map ExCA Register Map

PCI Memory Address Offset	ExCA Register Name
h'830	Memory window 4 start-address low byte
h'831	Memory window 4 start-address high byte
h'832	Memory window 4 end-address low byte
h'833	Memory window 4 end-address high byte
h'834	Memory window 4 offset-address low byte
h'835	Memory window 4 offset-address high byte
h'836	I/O window 0 offset-address low byte
h'837	I/O window 0 offset-address high byte
h'838	I/O window 1 offset-address low byte
h'839	I/O window 1 offset-address high byte
h'83A	Reserved
h'83B	Reserved
h'83C	Reserved
h'83D	Reserved
h'83E	Reserved
h'83F	Reserved
h'840	Memory window page 0
h'841	Memory window page 1
h'842	Memory window page 2
h'843	Memory window page 3
h'844	Memory window page 4

5.2 USB Host

5.2.1 Block Description

Figure 5.2 shows the USB host control block. As shown in Figure 5.2, the USB Host control block contains a controller (uPD720101F1-EA8-A from NEC Electronic), a USB Power control IC (LM3526M-H from National Semiconductor) and a connector of TypeA(CN7). This internal controller supports USB Versions 2.0 and 1.1.

Note that this controller and the SH7780 are connected with PCI bus (32-bit, 33 MHz).

Interrupts from the USB controller are connected to the SH7780's PCI interrupts (INTA/INTB/INTC selectable) and IRL interrupts via the PLD.

For details, refer to the pertinent uPD720101F1-EA8-A Hardware Manual.

NEC Electronics Corporation Homepage: http://www.necel.com

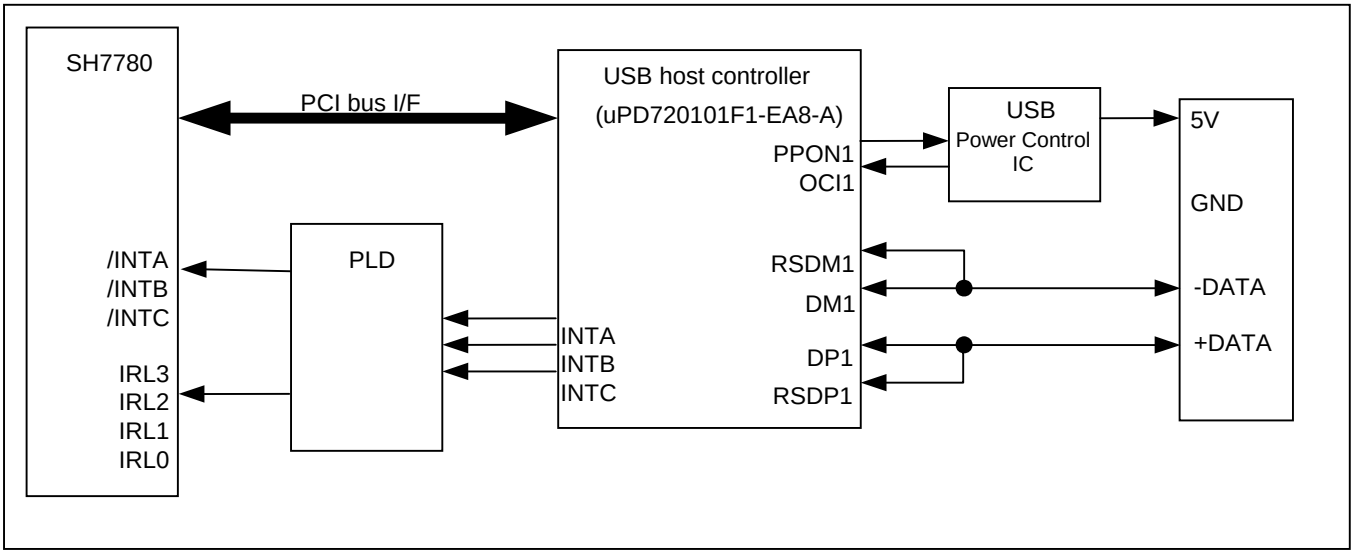
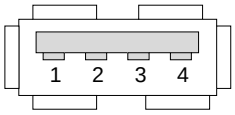


Figure 5.2 USB Host Control Block

5.2.2 Connector Pins

Figure 5.3 shows the pins of the USB host connector (CN7).



CN7 USB host connector (TypeA)
Model name: 24-5041-0041-10-834S
Maker: Kyocera Elco

Pin No	Signal name
1	VBUS
2	-DATA
3	+DATA
4	GND

Figure 5.3 USB Host Connector (CN7) Pins

5.2.3 Register Map

Table 5.3 shows a register map for the USB host controller.

For the register maps of the OHCI host controller #2 and EHCI host controller, refer to the uPD720101F1-EA8-A user's manual.

Table5.3 USB Host Controller Register

Offset address	Default value	Register name
H'00	H'00000010	HcRevision Register
H'04	H'00000000	HcControl Register
H'08	H'00000000	HcCommandStatus Register
H'0C	H'00000000	HcInterruptStatus Register
H'10	H'00000000	HcInterruptEnable Register
H'14	H'00000000	HcInterruptDisable Register
H'18	H'00000000	HcHCCA Register
H'1C	H'00000000	HcPeriodCurrentED Register
H'20	H'00000000	HcControlHeadED Register
H'24	H'00000000	HcControlCurrentED Register
H'28	H'00000000	HcBulkHeadED Register
H'2C	H'00000000	HcBulkCurrentED Register
H'30	H'00000000	HcDonrHeadED Register
H'34	H'00002EDF	HcFmInterval Register
H'38	H'00002EDF	HcFrameRemaining Register
H'3C	H'00000000	HcFmNumber Register
H'40	H'00000000	HcPeriodicStart Register
H'44	H'00000628	HcLSThreshold Register
H'48	H'0F000901	HcRhDescriptorA Register
H'4C	H'00020000	HcRhDescriptorB Register
H'50	H'00000000	HcRhStatus Register
H'54	H'00000000	HcRhPortStatus1 Register
H'58	H'FFFFFFFF	HcRhPortStatus2 Register
H'5C	H'FFFFFFFF	HcRhPortStatus3 Register

5.3 USB Function

5.3.1 Block Description

Figure 5.4 shows the USB function control block. As shown in Figure 5.4, the SM501GX08LF01-AB contains the internal USB function controller, a connector of TypeB (CN17). This internal controller supports USB Versions 1.1.

Note that this controller and the SH7780 are connected with PCI bus (32-bit, 33 MHz).

VBUS (cable connect) detection signals are connected to the IRL interrupts via the PLD.

For details, refer to the pertinent SM501GX08LF01-AB Hardware Manual.

SiliconMotion Homepage：http://www.siliconmotion.com.tw/en/en2/products4.htm

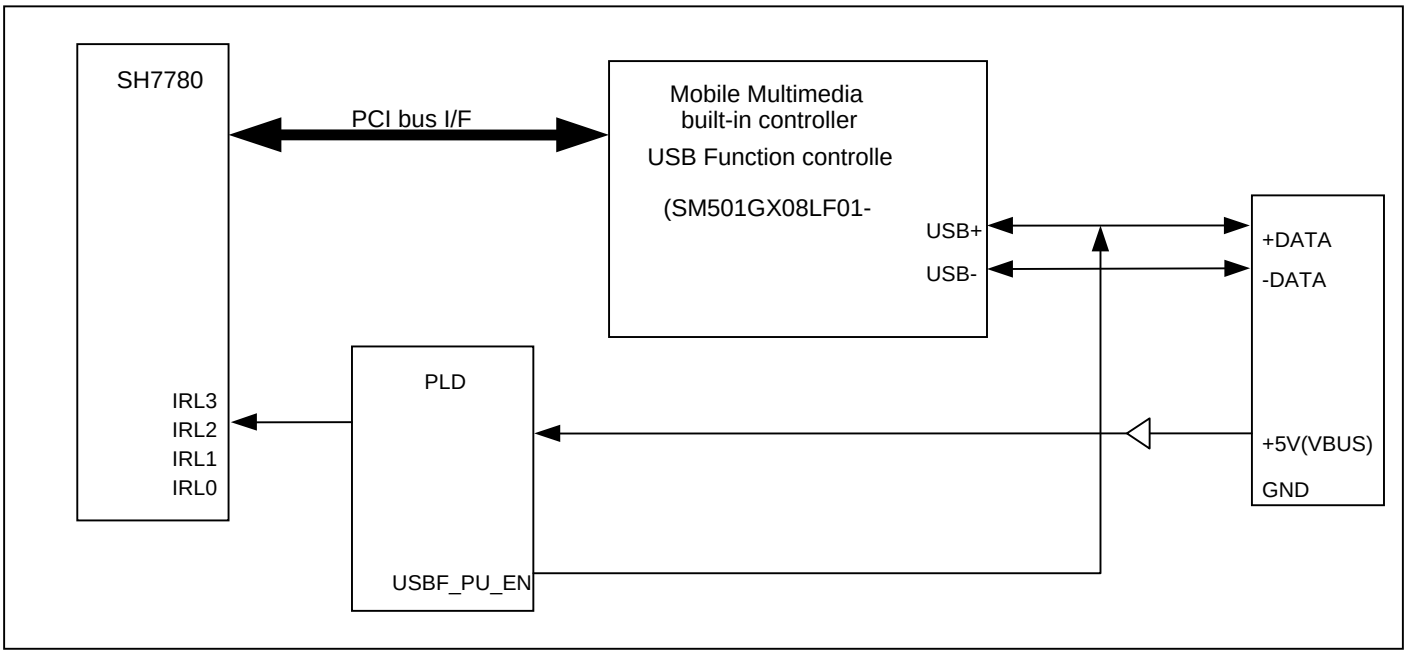
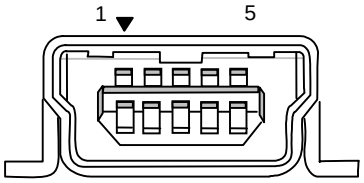


Figure 5.4 USB function control block

5.3.2 Connector Pins

Figure 5.5 shows the pins of the USB function connector (CN17).



CN17: USB function connector (miniB)
Model name: 24-5141-005-000-863+
Maker: Kyocera Elco

Pin No.	Signal name
1	VBUS
2	D-
3	D+
4	NC
5	GND

Figure 5.5 USB function connector (CN17) Pins

5.3.3 Register Map

The following shows the internal USB function control register of the PLD. For the USB function I/F register incorporated in the SM501, refer to its data sheet.

名称：USB Control Register(USBCR)

Address：H'19000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	FUNC VBUS	DPUP EN
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

bit15～2： Reserved

When read, these bits read as 0.

Writing data to these bits has no effect.

bit1：USB function VBUS detection flag (FUNCVBUS)

0: VBUS of USB function was not detected. (Initial value)

1: VBUS of USB function was detected.

Only writing 0 is accepted. Writing 1 has no effect.

bit0：USB function D+ pull-up enable (DPUPEN)

0：USB function D+ pull-up disable（Initial value）

1：USB function D+ pull-up enable

5.4 UART

5.4.1 Block Description

Figure 5.6 shows the UART control block. As shown in Figure 5.6, the UART control block contains the controller (XR16L2550IM-F from EXAR), RS232C interface driver, and 15-pin connector (CN1). This controller uses the clock pulses (7.3728MHz) supplied from the power supply controller (H8/3048F-ONE) for operations, and determines a baud rate (transfer rate) using these pulses as reference.

This controller has been provided with a 2-channel UART device. Channel A is used to communicate with the power supply controller (H8/3048F-ONE). Because channel B is connected to a 15-pin RS-232C connector (CN1), it can be used as a debug interface if it is connected to a PC.

For details, refer to the EXAR XR16L2550IM-F Manual.

EXAR Homepage: http://www.exar.com

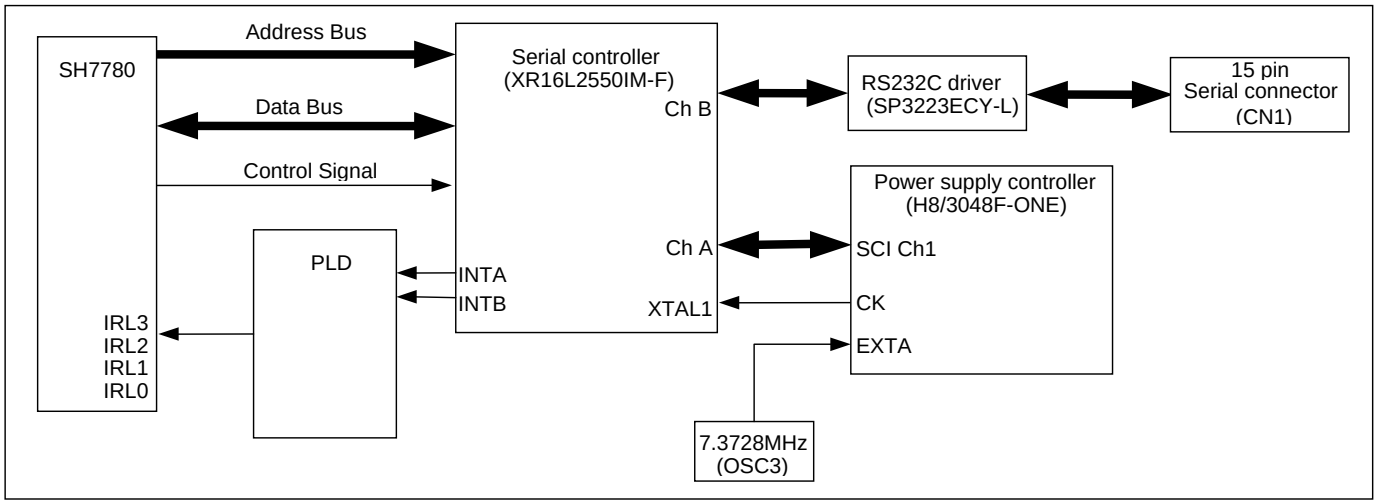
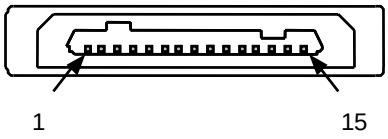


Figure 5.6 Serial Interface Block

5.4.2 Connector Pins

Figure 5.7 shows the pins of a 15-pin serial interface connector (CN1).



CN1: 15-pin serial connector
Model name: RMC-EA15MY-OM15-MC1
Maker: Honda Tsushin kogyo

Pin No	Signal name
1	GND
2	TxD
3	RxD
4	GND
5	RTS
6	CTS
7	GND
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

Figure 5.7 15-pin Serial Interface Connector Pins (CN1)

5.4.3 Register Map

Tables 5.4 and 5.5 show register maps for the serial interface controller registers.

Be sure all registers are accessed wordwise.

If access takes place in words, data in the low order 8 bits (D7 to D0) will become effective.

Table 5.4 Serial Interface Controller Register Map (Channel A)

Address	Initial value	Register name (at read)	Register name (at write)	Remarks
H'BA000000	—	RHR(ReceiveHoldingRegister)	THR(TransferHoldingRegister)	LCR bit7=0
H'BA000002	H'00	IER(InterruptEnableRegister)	IER(InterruptEnableRegister)	
H'BA000004	H'01	ISR(InterruptStatusRegister)	FCR(FIFOControlRegister)	LCR ≠ H'BF
H'BA000006	H'00	LCR(LineControlRegister)	LCR(LineControlRegister)	
H'BA000008	H'00	MCR(ModemControlRegister)	MCR(ModemControlRegister)	LCR ≠H'BF
H'BA00000A	H'60	LSR(LineStatusRegister)	N.A	
H'BA00000C	H'X0	MSR(ModemStatusRegister)	N.A	
H'BA00000E	H'FF	SPR(ScratchpadRegister)	SPR(ScratchpadRegister)	
H'BA000000	—	DLL(LSB of Divisor Latch)	DLL(LSB of Divisor Latch)	LCR bit7=1
H'BA000002	—	DLM(MSB of Divisor Latch)	DLM(MSB of Divisor Latch)	LCR ≠H'BF
H'BA000000	H'01	DREV(Device Revision)	—	LCR bit7=1
H'BA000002	H'02	DVID(Device ID)	—	LCR ≠H'BF DLL = H'00 DLM = H'00
H'BA000004		EFR(Enhanced Function Register)	EFR(Enhanced Function Register)	LCR = H'BF
H'BA000008		Xon-1(Xon Character 1)	Xon-1(Xon Character 1)	
H'BA00000A		Xon-2(Xon Character 2)	Xon-2(Xon Character 2)	
H'BA00000C		Xoff-1(Xoff Character 1)	Xoff-1(Xoff Character 1)	
H'BA00000E		Xoff-2(Xoff Character 2)	Xoff-2(Xoff Character 2)	

Table 5.5 Serial Interface Controller Register Map (Channel B)

Address	Initial value	Register name (at read)	Register (at write)	Remarks
H'BB000000	—	RHR(ReceiveHoldingRegister)	THR(TransferHoldingRegister)	LCR bit7=0
H'BB000002	H'00	IER(InterruptEnableRegister)	IER(InterruptEnableRegister)	
H'BB000004	H'01	ISR(InterruptStatusRegister)	FCR(FIFOControlRegister)	LCR ≠ H'BF
H'BB000006	H'00	LCR(LineControlRegister)	LCR(LineControlRegister)	
H'BB000008	H'00	MCR(ModemControlRegister)	MCR(ModemControlRegister)	LCR ≠H'BF
H'BB00000A	H'60	LSR(LineStatusRegister)	N.A	
H'BB00000C	H'X0	MSR(ModemStatusRegister)	N.A	
H'BB00000E	H'FF	SPR(ScratchpadRegister)	SPR(ScratchpadRegister)	
H'BB000000	—	DLL(LSB of Divisor Latch)	DLL(LSB of Divisor Latch)	LCR bit7=1
H'BB000002	—	DLM(MSB of Divisor Latch)	DLM(MSB of Divisor Latch)	LCR ≠H'BF
H'BB000000	H'01	DREV(Device Revision)	—	LCR bit7=1
H'BB000002	H'02	DVID(Device ID)	—	LCR ≠H'BF DLL = H'00 DLM = H'00
H'BB000004		EFR (Enhanced Function Register)	EFR(Enhanced Function Register)	LCR = H'BF
H'BB000008		Xon-1(Xon Character 1)	Xon-1(Xon Character 1)	
H'BB00000A		Xon-2(Xon Character 2)	Xon-2(Xon Character 2)	
H'BB00000C		Xoff-1(Xoff Character 1)	Xoff-1(Xoff Character 1)	
H'BB00000E		Xoff-2(Xoff Character 2)	Xoff-2(Xoff Character 2)	

5.5 LCD

5.5.1 Block Description

Figure 5.8 shows the LCD control block. As shown in Figure 5.8, the SM501GX08LF01-AB contains the LCD control and an LCD panel (TFT liquid crystal panel) mounted on the LCD board that can display 16-bit RGB data with a resolution of QVGA (240 x 320).

The VideoRam used for LCD display here is the local SDRAM incorporated in the SM501GX08LF01-AB.

The display data is stored in the internal local SDRAM of the SM501GX08LF01-AB beginning with the start address in order of coordinates (0,0), (1,0), and (239, 319). Display positions on the LCD panel are such that the data for the origin (0,0) is displayed at the upper left corner of the LCD panel and the data for coordinate (239, 319) is displayed at the lower right corner. Note that the display positions on LCD can be reversed top to bottom and left to right by changing settings of the LCD setup switch of the LCD board. The front light of the LCD panel can be turned on or off by the power supply controller.

For details about control of the front light, refer to Chapter 6, “Power Supply Controller.”

For details, refer to the pertinent SM501GX08LF01-AB Hardware Manual.

SiliconMotion Homepage：http://www.siliconmotion.com.tw/en/en2/products4.htm

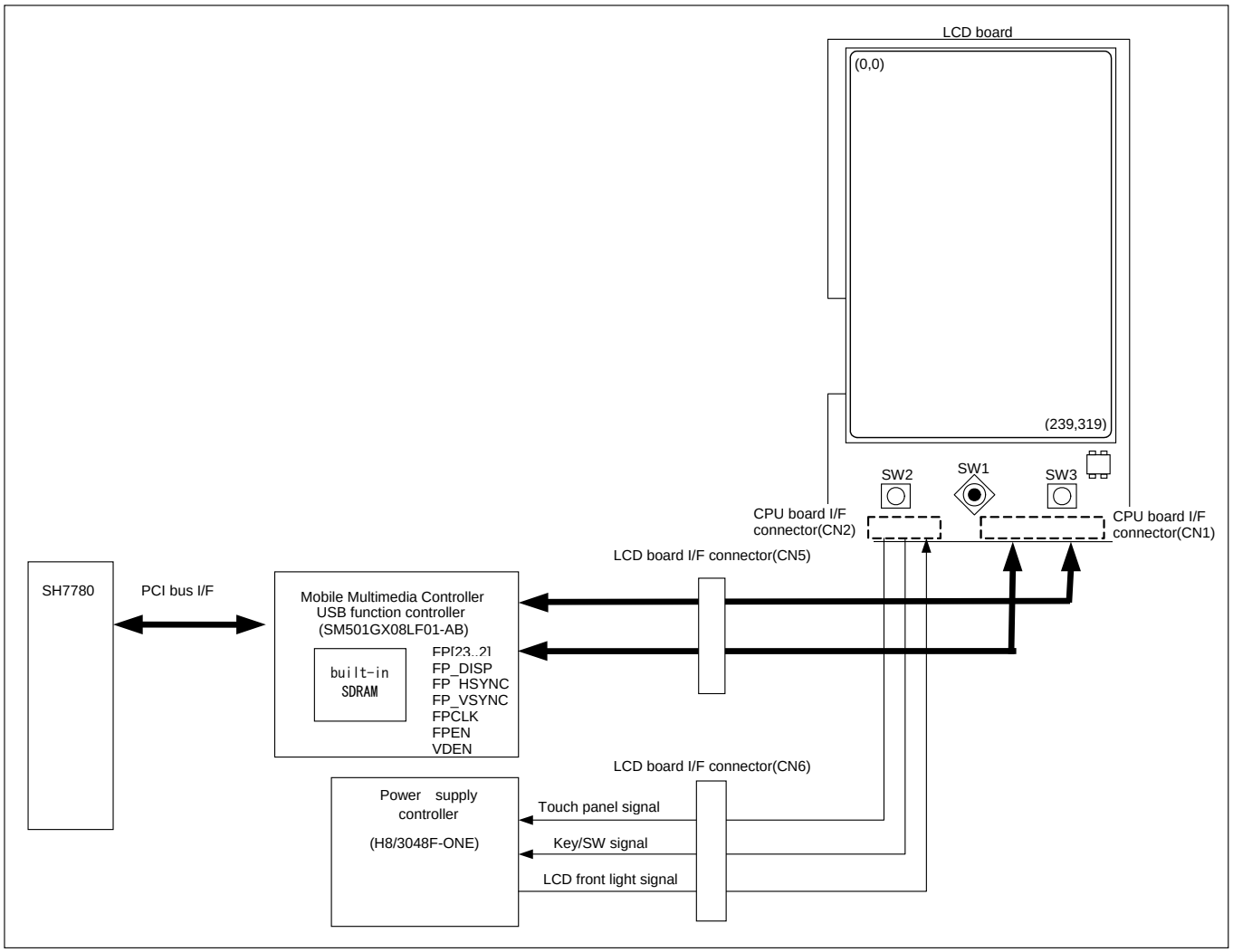
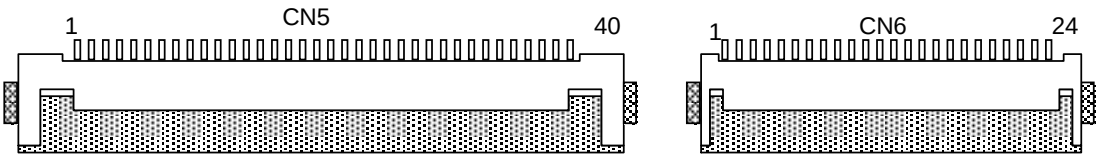


Figure 5.8 LCD Control Block

5.5.2 Connector Pins

Figure 5.9 shows the pins of the LCD interface connectors (CN5 and CN6). Tables 5.6 and 5.7 summarize the signals of these interface connectors.



CN5: LCD interface connector
Model name: FH12-40S-0.5SH
Maker: Hirose Electric Co., LTD.

CN6: LCD interface connector
Model name: FH12-24S-0.5SH
Maker: Hirose Electric Co., LTD.

Figure 5.9 LCD Interface Connector (CN5/CN6) Pins

Table 5.6 LCD Interface Connector (CN5) Signals

Pin No.	Signal name	I/O	Remarks	Pin No.	Signal name	I/O	Remarks
1	VBAT	-	Power supply	21	LCD13	OUT	LCDC
2	VBAT	-	Power supply	22	LCD14	OUT	LCDC
3	VBAT	-	Power supply	23	LCD15	OUT	LCDC
4	VBAT	-	Power supply	24	GND	-	Power supply
5	N.C	-	Unused	25	GND	-	Power supply
6	LCD0	OUT	LCDC	26	CL1	OUT	LCDC
7	LCD1	OUT	LCDC	27	CL2	OUT	LCDC
8	LCD2	OUT	LCDC	28	DON	OUT	LCDC
9	LCD3	OUT	LCDC	29	M_DISP	OUT	LCDC
10	LCD4	OUT	LCDC	30	FLM	OUT	LCDC
11	LCD5	OUT	LCDC	31	VEPWC	OUT	LCDC
12	LCD6	OUT	LCDC	32	VCPWC	OUT	LCDC
13	LCD7	OUT	LCDC	33	NC	-	Unused
14	GND	-	Power supply	34	GND	-	Power supply
15	GND	-	Power supply	35	GND	-	Power supply
16	LCD8	OUT	LCDC	36	IR_IN	IN	Remote control
17	LCD9	OUT	LCDC	37	3.3V	-	Power supply
18	LCD10	OUT	LCDC	38	3.3V	-	Power supply
19	LCD11	OUT	LCDC	39	3.3V	-	Power supply
20	LCD12	OUT	LCDC	40	3.3V	-	Power supply

Table5.7 LCD Interface Connector (CN6) Signals

Pin No.	Signal name	I/O	Remarks	Pin No.	Signal name	I/O	Remarks
1	GND	-	Power supply	13	~PAD_CS	OUT	PAD I/F
2	GND	-	Power supply	14	~PAD_IRQ	IN	PAD_I/F
3	KEY_IN0	IN	KEY_I/F	15	PAD_DIN	OUT	PAD_I/F
4	KEY_IN1	IN	KEY_I/F	16	PAD_DOUT	IN	PAD_I/F
5	KEY_IN2	IN	KEY_I/F	17	PAD_DCLK	OUT	PAD_I/F
6	KEY_IN3	IN	KEY_I/F	18	~RESET	OUT	Reset
7	KEY_IN4	IN	KEY_I/F	19	~LCD_FLON	OUT	LCD power supply
8	KEY_OUT0	OUT	KEY_I/F	20	~LCD_PWRDY	IN	LCD power supply
9	KEY_OUT1	OUT	KEY_I/F	21	GND	-	Power supply
10	KEY_OUT2	OUT	KEY_I/F	22	GND	-	Power supply
11	GND	-	Power supply	23	3.3VSB	-	Power supply
12	GND	-	Power supply	24	3.3VSB	-	Power supply

5.6 Sound Generator

5.6.1 Block Description

Figure 5.10 shows the sound generator control block. As shown in Figure 5.10, the SH7780 contains the internal Audio Codec I/F (HAC), and an Audio codec (STAC9751T from SIGMATEL) so that sound can be output to headphones connected to an output mini-jack (CN16) or it can be input to earphones connected to an I/O mini-jack (CN15). In addition, headphone output takes place with the quality of stereo output while earphone I/O takes place with the quality of monaural I/O that uses only the Rch.

This control block is connected to an electronic volume so that sound output volume can be controlled. This electronic volume is controlled through the power supply controller. For details, refer to 6. “Power Supply Controller.”

For more details, refer to the pertinent SIGMATEL STAC9751T Manual.

SIGMATEL Homepage: http://www.idt.com/?genID=STAC9751&source=products_genericPart_STAC9751

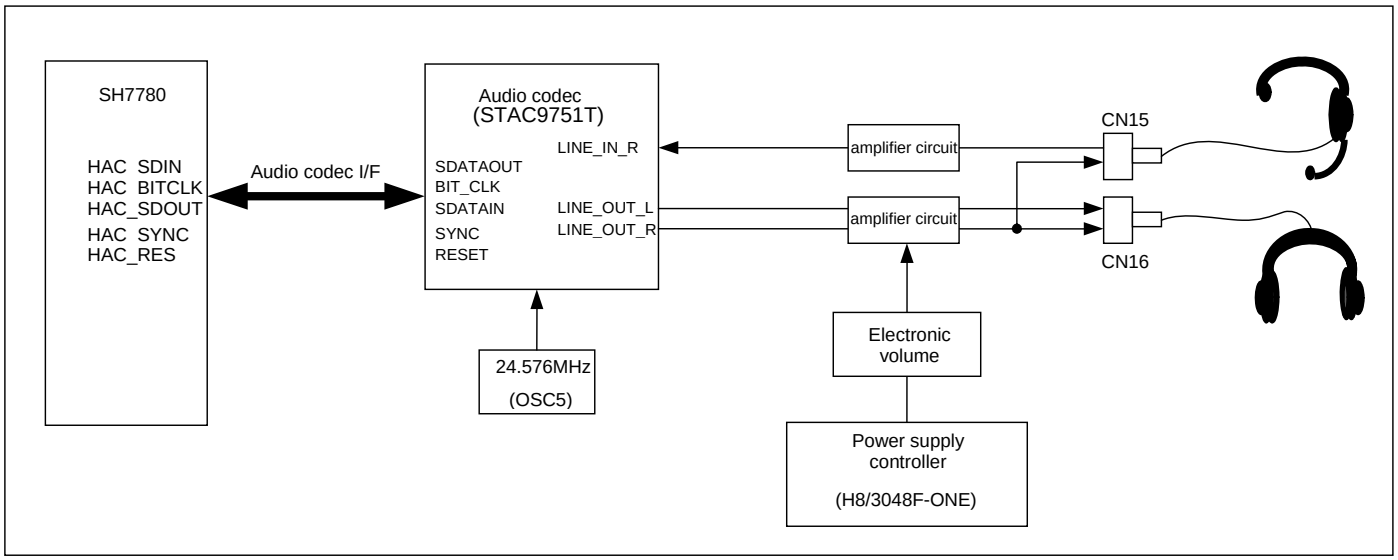


Figure 5.10 Sound Generator Control Block

5.6.2 Connector Pins

Figure 5.11 shows the pins of the sound generator I/O mini-jack (CN15, CN16). Tables 5.8 and 5.9 list the signals of the sound generator I/O mini-jack (CN15, CN16).

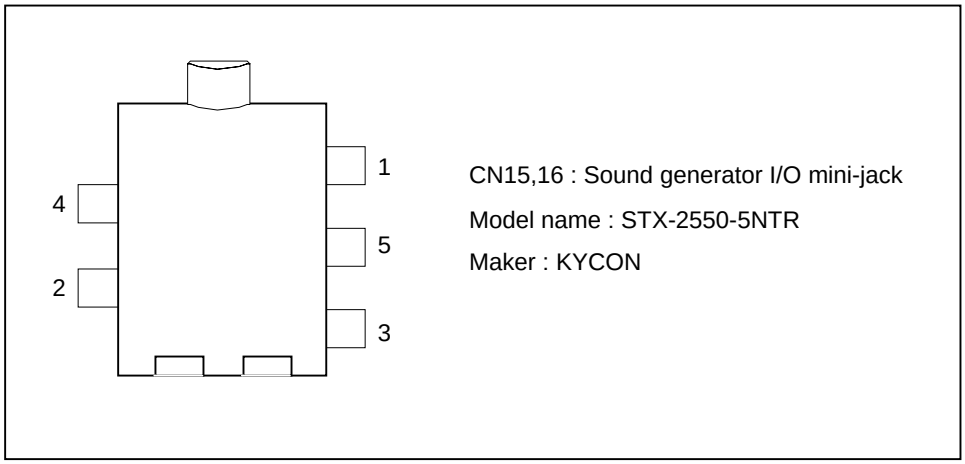


Figure 5.11 Sound Generator I/O Mini-jack (CN15, CN16) Pins

Table 5.8 Sound Generator I/O Mini-jack (CN15) Signals

Pin No	Signal Name
1	GND
2	R-IN
3	R-OUT
4	MIC-IN
5	HP_SENSE

Table 5.9 Sound Generator I/O Mini-jack (CN16) Signals

Pin No	Signal Name
1	GND
2	L-OUT
3	R-OUT
4	HP_SENSE
5	NC

5.6.3 Register Map

Table 5.10 shows a register map for the SH7780 HAC registers.

Table 5.10 HAC Controller Register

Address	Initial value	Register name
H’FFE40008	H’00000200	Control and status register
H’FFE40020	H’00000000	Command/status address register
H’FFE40024	H’00000000	Command/status data register
H’FFE40028	H’00000000	PCM left chann registerel
H’FFE4002C	H’00000000	PCM right channel register
H’FFE40050	H’00000000	TX interrupt enable register
H’FFE40054	H’F0000000	TX status register
H’FFE40058	H’00000000	RX interrupt enable register
H’FFE4005C	H’00000000	RX status register
H’FFE40060	H’84000000	HAC control register

5.7 eTRON Interface

5.7.1 Block Description

Figure 5.12 shows the eTRON interface control block. As shown in Figure 5.12, this block incorporates a smart card interface controller, allowing it to communicate with the eTRON card inserted into the eTRON interface connector (CN4). Resetting the eTRON card can be controlled by controlling the port (PE6) of the SH7780. The control method is described below.

Low output from PE6: Pulls the reset pin of the eTRON card low (reset state)

High output from PE6: Holds the reset pin of the eTRON card high (normal state)

The power supply to the eTRON card is controlled by the power supply controller (H8/3048F-ONE), but when the T-Engine board remains powered on, the eTRON card is always supplied with power. Always be sure to check that the power for the T-Engine board is turned off before inserting or removing the eTRON card.

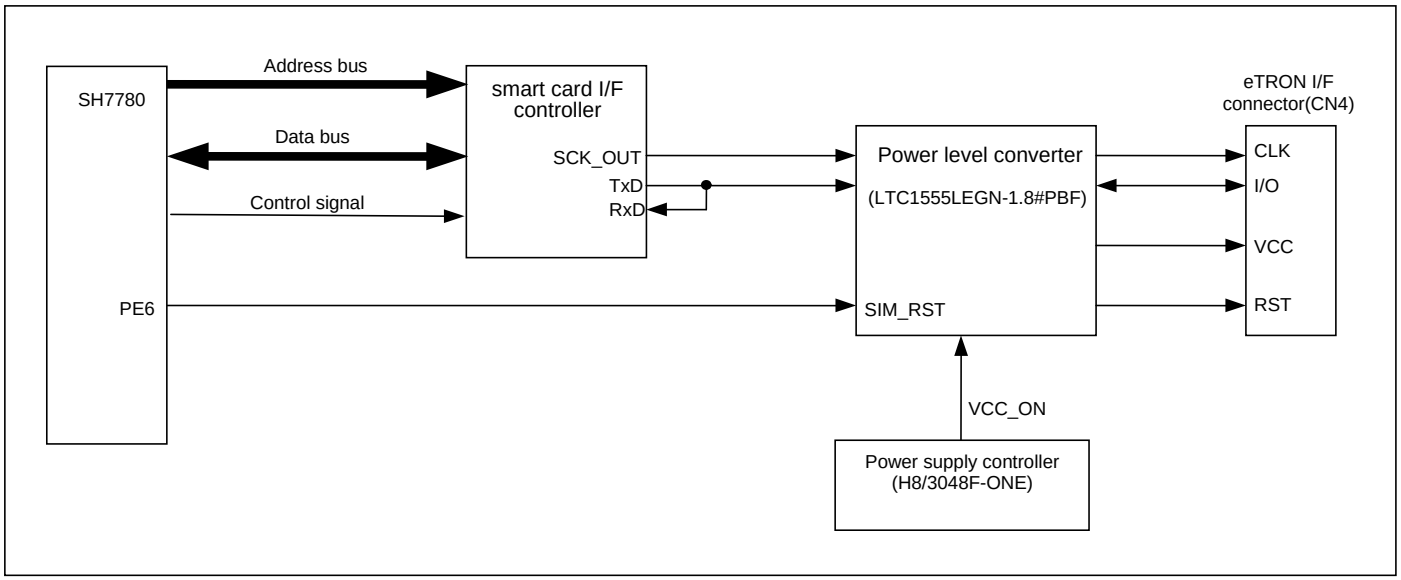


Figure 5.12 eTRON Interface Control Block

5.7.2 Connector Pins

Figure 5.13 shows the pins of the eTRON interface connector (CN4). Table 5.11 summarizes the signals of the eTRON interface connector (CN4).

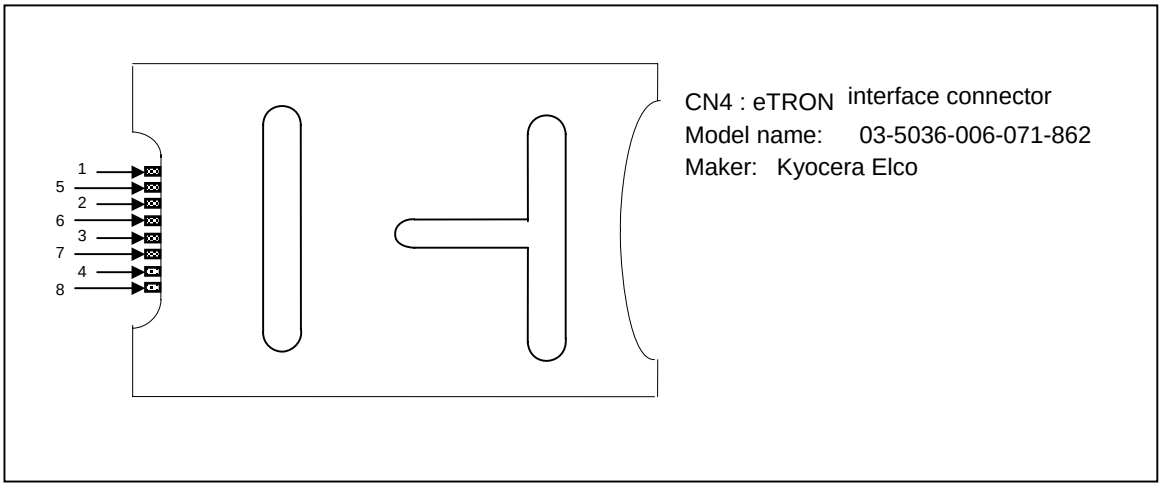


Figure 5.13 eTRON Interface Connector (CN4) Pins

Table 5.11 eTRON Interface Connector (CN4) Signals

Pin No	Signal Name
1	C1:VCC
2	C2:RST
3	C3:CLK
4	C4:*1
5	C5:GND
6	C6:VPP
7	C7:I/O
8	C8: *1

*1: Pins 4 and 8 are connected to the connector (CN8) for board test. Don't use this connector for the other purpose.

5.7.3 Register Map

Table 5.12 shows a register map for the SH7780 internal smart card interface (SCI) controller, including the SIMCRT registers within the FPGA.

Table 5.12 SIM Card Module Register Map

Address	Initial value	Register name
H'B8000000	H'00	Srial mode register
H' B8000002	H'FF	Bit rate register
H' B8000004	H'00	Serial control register
H' B8000006	H'FF	Transmit data register
H' B8000008	H'84	Serial status register
H' B800000A	H'00	Receive data register
H' B800000C	H'00	Smart card mode register

Register name : Srial mode register (SCSMR)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	GM	-	-	O_NE	-	-	CKS1	CKS0
initial value	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R	R	R/W	R/W

bit15～8,6,5,3,2 : Reserved

When read, these bits read as 0 (however, bits 5 and 3 = 1).

Writing data to these bits has no effect.

bit7 : GSM mode(GM)

This bit sets operation mode of the smart card interface.

0: The smart card interface operates in normal mode. (Initial value)

The TEND flag is set 12.5 etu after the beginning of the start bit.

Clock output is controlled only for ON/OFF.

1: The smart card interface operates in GSM mode.

The TEND flag is set 11.0 etu after the beginning of the start bit.

Clock output is controlled for ON/OFF, as well as controlled for fixed High/Low.

bit4 : Parity mode (O_NE)

This bit selects even or odd parity for parity addition/parity check.

0: Selects even parity. (Initial value)

1: Selects odd parity.

bit2,1 : Clock select (CKS[1:0])

These bits select the clock source for the internal baud rate generator.

CKS[1:0] = 00: System clock. (Initial value)

CKS[1:0] = 01: System clock divided by 4.

CKS[1:0] = 10: System clock divided by 16.

CKS[1:0] = 11: System clock divided by 64.

Register name : Bit rate register (SCBRR)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0
Initial value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit15～8 : Reserved

When read, these bits read as 0.
Writing data to these bits has no effect.

bit7～0 : bit rate set (BRR[7:0])

These bits set the bit rate of serial transmission/reception.

Register name : Serial control register (SCSCR)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	TIE	RIE	TE	RE	-	-	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bit15～8,3,2 : Reserved

When read, these bits read as 0.
Writing data to these bits has no effect.

bit7 : Transmit interrupt enable (TIE)

This bit enables or disables generation of transmit interrupt (TXI) requests when the TEND flag of SCSSSR1 is set to 1 after completion of transmission.

0: Interrupt requests disabled. (Initial value)
Transmit interrupt (TXI) requests are disabled. TXI is cleared.

1: Interrupt requests enabled.
Transmit interrupt (TXI) requests are enabled. Negation of TXI is also possible by clearing the TDRE flag from 1 to 0.

bit6 : Receive interrupt enable (RIE)

This bit enables or disables generation of received data full interrupt (RXI) and error interrupt (ERI) requests when the RDRF flag of SCSSSR1 is set to 1 after completion of reception.

0: Interrupt requests disabled. (Initial value)
Received data full interrupt (RXI) and error interrupt (ERI) requests are disabled. RXI and ERI are cleared.

1: Interrupt requests enabled.
Received data full interrupt (RXI) and error interrupt (ERI) requests are enabled. Negation of RXI and ERI is also possible by clearing the RDRF flag or the ERS, PER and ORER flags from 1 to 0.

bit5 : Transmit enable (TE)

This bit enables or disables commencement of serial transmit operation.

0: Transmit operation disabled. (Initial value)
The TDRE flag is fixed to 1.

1: Transmit operation enabled.
Always be sure to set up the serial mode register (SCSMR1) to determine the transmit format before setting the TE bit to 1.

bit4 : Receive enable (RE)

This bit enables or disables commencement of serial receive operation.

0: Receive operation disabled. (Initial value)

Even when the RE bit is cleared, the RDRF, FER, PER and ORER flags each are unaffected and retain their state.

1: Receive operation enabled.

Always be sure to set up the SCSMR1 register to determine the receive format before setting the RE bit to 1.

bit2,1 : Clock enable (CKE[1:0])

These bits select the function of the SCK pin.

In addition to disabling or enabling normal clock output by setting the GM bits of CKE0, CKE1 and SCSMR1 and the SPBOIO bit of SCSPTR1, it is possible to specify that clock output be fixed high or fixed low.

Register name : Transmit data register (SCTDR)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
Initial value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit15～8 : Reserved

When read, these bits read as 0.

Writing data to these bits has no effect.

bit7～0 : Transmit data (TDR[7:0])

These bits comprise an 8-bit register in which serial transmit data is stored.

While the transmit shift register (SCTSR) that cannot be read or written from the CPU is empty, data may be written to the SCTDR, so that the data is transferred from that register to the SCTSR to start serial transmission.

Furthermore, while serial data is transferred from the SCTSR, the next transmit data may be written to the SCTDR. That way, serial transmission can be performed successively.

Register name : Transmit shift register (SCTSR)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	TSR7	TSR7	TSR7	TSR7	TSR7	TSR7	TSR7	TSR7
Initial value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

bit7～0 : Transmit shift data (TSR[7:0])

This register cannot be read or written directly from the CPU.

The data transferred from the SCTDR to this register is sequentially shifted out to the TxD pin beginning with the LSB (bit 0) to perform serial data transmission.

When 1 byte of data has all be transmitted, the next data is automatically transferred from the SCTDR to start transmission. However, if the TDRE flag of the serial status register (SCSSR) is set to 1, no data is transferred from the SCTDR.

Register name : Serial status Register (SCSSR)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	TDRE	RDRF	ORER	ERS	PER	TEND	-	-
Initial value	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

bit15～8,1,0 : Reserved

When read, these bits read as 0.
Writing data to these bits has no effect.

bit7 : Transmit data register empty (TDRE)

This bit indicates that no data exists in the SCTDR.
Only writing 0 is accepted. However, if TE = 0, no data can be written to this bit.
0: Denotes that valid transmit data has been written to the SCTDR.

Clear conditions
(1) Cleared by writing 0 after reading TDRE = 1
(2) Cleared when data is written to the SCTDR

1: Denotes that no valid transmit data exists in the SCTDR. (Initial value)

Set conditions
(1) Set when the register is reset
(2) Set when the TE bit of the SCSCR = 0
(3) Set when data is written to the SCTDR after data was transferred from the SCTDR to the SCTSR
When the TDRE bit is cleared from 1 to 0, the transmit interrupt (TXI) is cleared.

bit6 : Receive data register full (RDRF)

This bit indicates that receive data is stored in the SCRDR.
Only writing 0 is accepted.
0: Denotes that valid receive data is not stored in the SCRDR. (Initial value)
Clear conditions
(1) Cleared when the register is reset
(2) Cleared by writing 0 after reading RDRE = 1
(3) Cleared when data is read out from the SCRDR
1: Denotes that valid receive data is stored in the SCRDR.
Set conditions
Set when receive data has been transferred from the SCRSR to the SCRDR after serial reception terminated normally. Even when an error is detected during reception or the RE bit of the SCSCR is cleared to 0, the SCRDR and the RDRF flag are unaffected and retain their previous state.

When the RDRF bit is cleared from 1 to 0, the receive interrupt (RXI) is cleared.
If while the RDRF flag remains set to 1 the next data has all been received, an overrun error occurs, in which case the received data is lost.

bit5 : Overrun error (ORER)

This bit indicates that an overrun error occurred during reception and the receive operation terminated abnormally.
Only writing 0 is accepted.
0: Denotes that data has been normally received, with no errors signaled. (Initial value)
Clear conditions
(1) Cleared when the register is reset
(2) Cleared by writing 0 after reading ORER = 1
1: Denotes that an overrun error occurred during reception.
Set conditions
(1) Set when an error signal is sampled low
Even when the RE bit is cleared to 0, the ORER flag is unaffected and retains its previous state.
The data received in the SCRDR before an overrun error occurred is retained in it and the data received after that is lost.
Once ORER = 1 is set, subsequent serial reception cannot be continued.
When the ORER bit is cleared from 1 to 0, the error interrupt (ERI) is cleared.

bit4 : Error signal status (ERS)

This bit indicates that an error signal has been sent from the receive side during transmission.
Only writing 0 is accepted.
0: Denotes that data has been received normally, with no errors signaled. (Initial value)
Clear conditions
(1) Cleared when the register is reset
(2) Cleared by writing 0 after reading ERS = 1
1: Denotes that an error signal indicating detected parity error has been sent out from the received side.
Set conditions
(1) Set when an error signal is sampled low
Even when the TE bit is cleared to 0, the ERS flag is unaffected and retains its previous state.
When the ERS bit is cleared from 1 to 0, the error interrupt (ERI) is cleared.
While ERS = 1, new data transmissions cannot be performed.

bit3 : Parity Error (PER)

This bit indicates that a parity error occurred during receiving and the receive operation terminated abnormally.
Only writing 0 is accepted.
0: Denotes that data is being received or data has all be received normally. (Initial value)
Clear conditions
(1) Cleared when the register is reset
(2) Cleared by writing 0 after reading PER = 1
1: Denotes that a parity error occurred during reception.
Set conditions
(1) Set when during parity check of received data, the even/odd parity set in it did not match the one specified by the O_NE bit of the SCSMR
Even when the RE bit is cleared to 0, the PER flag is unaffected and retains its previous state.
Although the receive data in which a parity error occurred is transferred to the SCRDR, the RDRF flag is not set.
Note that once the PER flag is set to 1, subsequent data reception cannot be continued.
When the PER bit is cleared from 1 to 0, the error interrupt (ERI) is cleared.

bit2 : Transmit end (TEND)

This bit indicates transmit state.
This bit is read-only, and writing data has no effect.
0: Denotes that transmission is under way.
Clear conditions
(1) Cleared by writing 0 to the TDRE flag after reading TDRE = 1
(2) Cleared when data is written to the SCTDR
1: Denotes that transmission is completed. (Initial value)
Set conditions
(1) Set when the register is reset
(2) Set when TE bit of SCSCR = 0 and ERS bit = 0
(3) Set when TDRE = 1 and ERS = 0 (transmitted normally) 2.5 etu after 1 byte of character was transmitted while GM bit of SCSMR = 0
(4) Set when TDRE = 1 and ERS = 0 (transmitted normally) 1.0 etu after 1 byte of character was transmitted while GM bit of SCSMR = 1

Register name : Receive data register (SCRDR)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit15～8 : Reserved

When read, these bits read as 0.
Writing data to these bits has no effect.

bit7～0 : Receive data (RDR[7:0])

The received serial data is stored in these bits.
When one byte of data has all been received, the received data is transferred from the SCRSR to the SCRDR and stored in it to terminate the receive operation. After receive operation is completed, the SCRSR becomes ready to receive again.
Since the SCRSR and SCRDR are configured as dual buffers, successive receive operations are possible.
The SCRDR is read-only, and writing data from the CPU has no effect.

Register name : Receive data register (SCRSR)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
Initial value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

bit7～0 : Receive shift data (RSR[7:0])

These bits are used to receive serial data.
The serial data input from the RxD pin is set in these bits and converted to parallel data in the order the data is received beginning with the LSB (bit 0). When one byte of data has all been received, the data is automatically transferred to the SCRDR.
This register cannot be accessed directly from the CPU.

Register name : Smart card mode register (SCSCMDR)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	SDIR	SINV	-	SMIF
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W

bit15～4,1 : Reserved

When read, these bits read as 0.

Writing data to these bits has no effect.

bit3 : Smart card data transfer direction (SDIR)

This bit sets the data format of serial/parallel conversion.

0: The content of the SCTDR is transmitted the LSB first, and the received data is stored in the SCRDR the LSB first. (Initial value)

1: The content of the SCTDR is transmitted the MSB first, and the received data is stored in the SCRDR the MSB first.

bit2 : Smart card data invert (SINV)

This bit specifies that the logic level of data is inverted.

This function is used in combination with the function of bit 3 for transmission/reception with inverse convention cards.

SINV does not affect the logic level of parity bits.

0: The content of the SCTDR is transmitted directly as is, and the received data is stored in the SCRDR directly as is. (Initial value)

1: The content of the SCTDR is inverted before being transmitted, and the received data is inverted before being stored in the SCRDR.

bit0 : Smart card interface mode select (SMIF)

This bit enables the smart card interface function.

0: Smart card interface function is disabled (standby mode). (Initial value)

In this case, all register bits but SMIF come inaccessible. Furthermore, the TxD and SCK pins are fixed in the high-impedance state, and data input from the RxD pin cannot be received. During standby, however, all register values are retained.

1: Smart card interface function is enabled (normal mode).

Do not clear the SMIF bit to 0 during transmission/reception. Unless this caution is observed, device operation cannot be guaranteed.

Register name : Serial Port Register (SCSPTR)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	EIO	-	-	-	SPB1IO	SPB1DT	SPB0IO	SPB0DT
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	X	0	X
R/W	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W

bit15～8,6～4 : Reserved

When read, these bits read as 0.
Writing data to these bits has no effect.

bit7 : Error interrupt only (EIO)

Even when the RIE bit is set to 1 while EIO bit = 1, no RXI interrupt requests are sent to the CPU.
This bit enables or disables RXI interrupt.
0: When RIE bit = 1, RXI and ERI interrupts are enabled. (Initial value)
1: When RIE bit = 1, only ERI interrupt is enabled.

bit3 : Serial port clock port I/O (SPB1IO)

This bit specifies that the serial port SCK pin is set for input or output.
For the value set by the SPB1DT bit to be actually output after setting the SCK pin for output,
be sure the C/A bit of the SCSMR and the CKE1 and CKE0 bits of the SCSCR are set to 0.
0: Denotes that the value of the SPB1DT bit is not output to the SCK pin. (Initial value)
1: Denotes that the value of the SPB1DT bit is output to the SCK pin.

bit2 : Serial port clock port data (SPB1DT)

This bit specifies the input/output data on serial port SCK pin.
Whether the port is set for input or output is specified by the SPB1IO bit.
When set for output, the value of the SPB1DT bit is output to the SCK pin.
No matter how the SPB1IO bit is set, the value of the SCK pin is always read out from
the SPB1DT bit. The initial value after reset is indeterminate.
0: Denotes that the input/output data at the port is low-level data.
1: Denotes that the input/output data at the port is high-level data.

bit1 : Serial port break I/O (SPB0IO)

This bit specifies output conditions for the serial port TxD pin.
For the value set by the SPB0DT bit to be actually output after setting the TxD pin for output, be sure
the TE and RE bits of the SCSCR are set to 0.
0: Denotes that the value of the SPB0DT bit is not output to the TxD pin. (Initial value)
1: Denotes that the value of the SPB0DT bit is output to the TxD pin.

bit0 : Serial port break data (SPB0DT)

This bit specifies the input data on serial port RxD pin and the output data on TxD pin.
The output condition for the TxD pin is specified by the SPB0IO bit.
If the TxD pin is set for output, the value of the SPB0DT bit is output to the TxD pin.
No matter how the SPB0IO bit is set, the value of the RxD pin is always read out from the SPB0DT bit.
The initial value after reset is indeterminate.
0: Denotes that the input/output data at the port is low-level data.
1: Denotes that the input/output data at the port is high-level data.

5.8 Ethernet Controller

5.8.1 Block Description

This block has the Ethernet controller (LAN91C111-NU made by SMSC) and RJ-45 connector (CN4) mounted on the debug board of the T-Engine board, allowing 10BASE-T/100BASE-T Ethernet communications to be performed.

Table 5.13 shows the modes in which the Ethernet controller is used.

A 25 MHz clock is used for operation of the controller, and the controller operates synchronously with this clock. Interrupts from the controller are connected to the expansion slots IRQ3–IRQ0 of the T-Engine board. The expansion slots IRQ3–IRQ0 to which interrupts are connected can be selected by setting the J2–J5 on the debug board, as shown below.

J2 shorted: Expansion slot IRQ0 is selected.

J3 shorted: Expansion slot IRQ1 is selected.

J4 shorted: Expansion slot IRQ2 is selected.

J5 shorted: Expansion slot IRQ3 is selected.

CAUTION

Always be sure that only one of J2–J5 is shorted at a time, with the others left open.

For other details, refer to the LAN91C111-NU user's manual.

SMSC Home Page: http://www.smsc.com/main/catalog/lan91c111.html

Table5.13 Ethernet Controller Operation Modes

Item	Content
Bus type	16-bit bus mode
Bus width	16 bits
WAIT	ARDY signal used (NO WAIT bit of Configuration Register = 0)
Interrupt pin	INTRO used (INT SEL0 and SEL1 bits of Configuration Register = 00)

5.8.2 Connector Pins

Figure 5.14 shows the pins of the Ethernet interface connector (CN4). Table 5.14 summarizes the signals of the Ethernet interface connector (CN4).

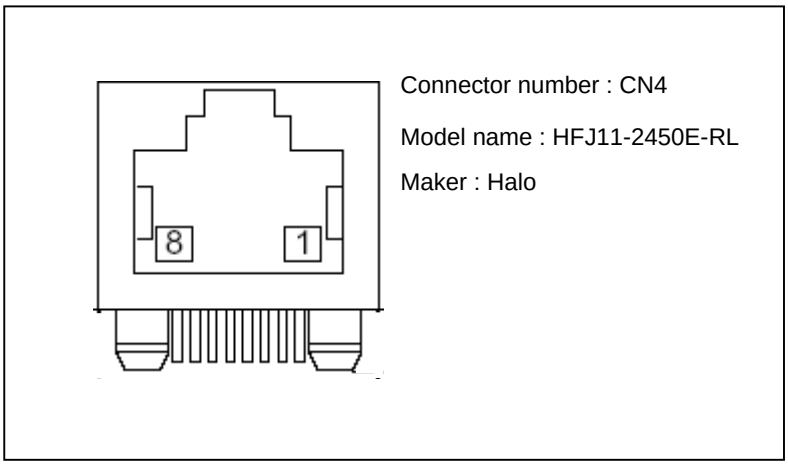


Figure5.14 Ethernet interface connector (CN4) Pins

Table 5.14 Ethernet Interface Connector (CN4) Signals

Pin No.	Signal name	I/O	Remarks
1	TX+	OUT	
2	TX-	OUT	
3	RX+	IN	
4	―	―	
5	―	―	
6	RX-	IN	
7	―	―	
8	―	―	
9	GND	―	
10	GND	―	

5.8.3 Register Map

Table 5.15 shows a register map for the Ethernet controller.

Table5.15 Ethernet controller Register Map

Register Address	BANK0	BANK1	BANK2	BANK3
H'A0400000	TCR	CONFIG	MMU COMMAND	MT0-1
H'A0400002	EPH STATUS	BASE	PNR	MT2-3
H'A0400004	RCR	IA0-1	FIFO PORTS	MT4-5
H'A0400006	COUNTER	IA2-3	POINTER	MT6-7
H'A0400008	MIR	IA4-5	DATAMGMT	MGMT
H'A040000A	RPCR	GENERAL	DATA	REVISION
H'A040000C	RESERVED	CONTOROL	INTERRUPT	ERCV
H'A040000E	BANK SELECT			

5.9 IrDA

5.9.1 Block Description

Figure 5.15 shows the infrared communication module control block. As shown in Figure 5.15, the mobile multimedia controller (SM501GX08LF01-AB made by SiliconMotion) incorporates a serial/IrDA controller, use of which makes IrDA1.0-compliant infrared communication possible.

For details, refer to the pertinent SM501GX08LF01-AB Hardware Manual.

SiliconMotion Homepage：http://www.siliconmotion.com.tw/en/en2/products4.htm

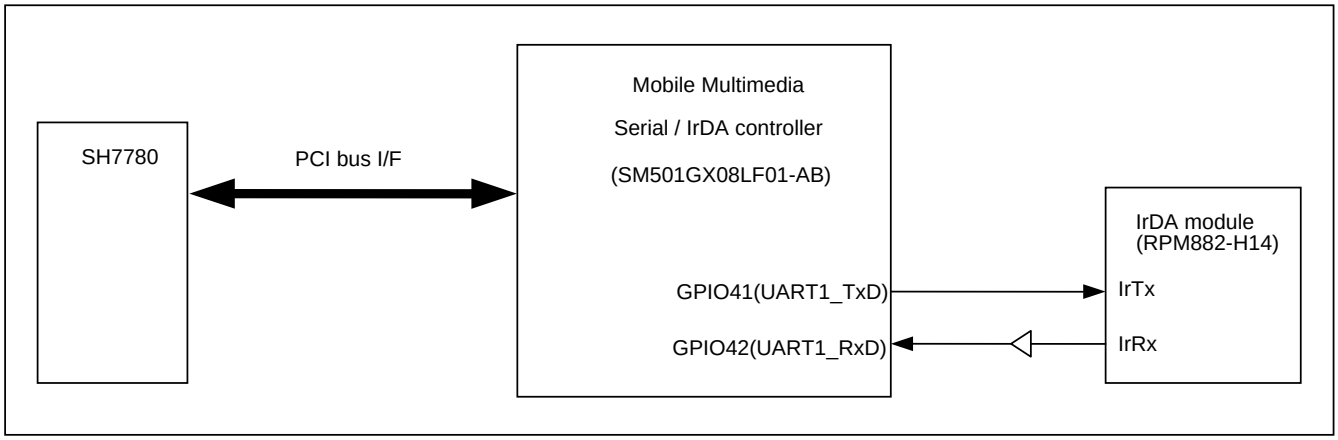


Figure5.15 Infrared Communication Module Control Block

6. Power Supply Controller

6.1. Power Supply Controller Functions

The H8/3048F-ONE power supply controller (simply called the power supply controller) provides the following control functions with firmware stored in the internal memory. The following functions can be controlled through the UART ChA from the SH7780. Figure 6.1 shows a power supply controller block diagram.

(1) RTC (real-time clock) function
(2) System power supply (3.3V/5/0V) ON/OFF control function
(3) Touch panel coordinate position read function
(4) Key switch input function
(5) 8 bit LED lighting/extinction function
(6) Infrared remote control transmission/reception function
(7) Electronic volume
(8) Serial EPROM read/write function

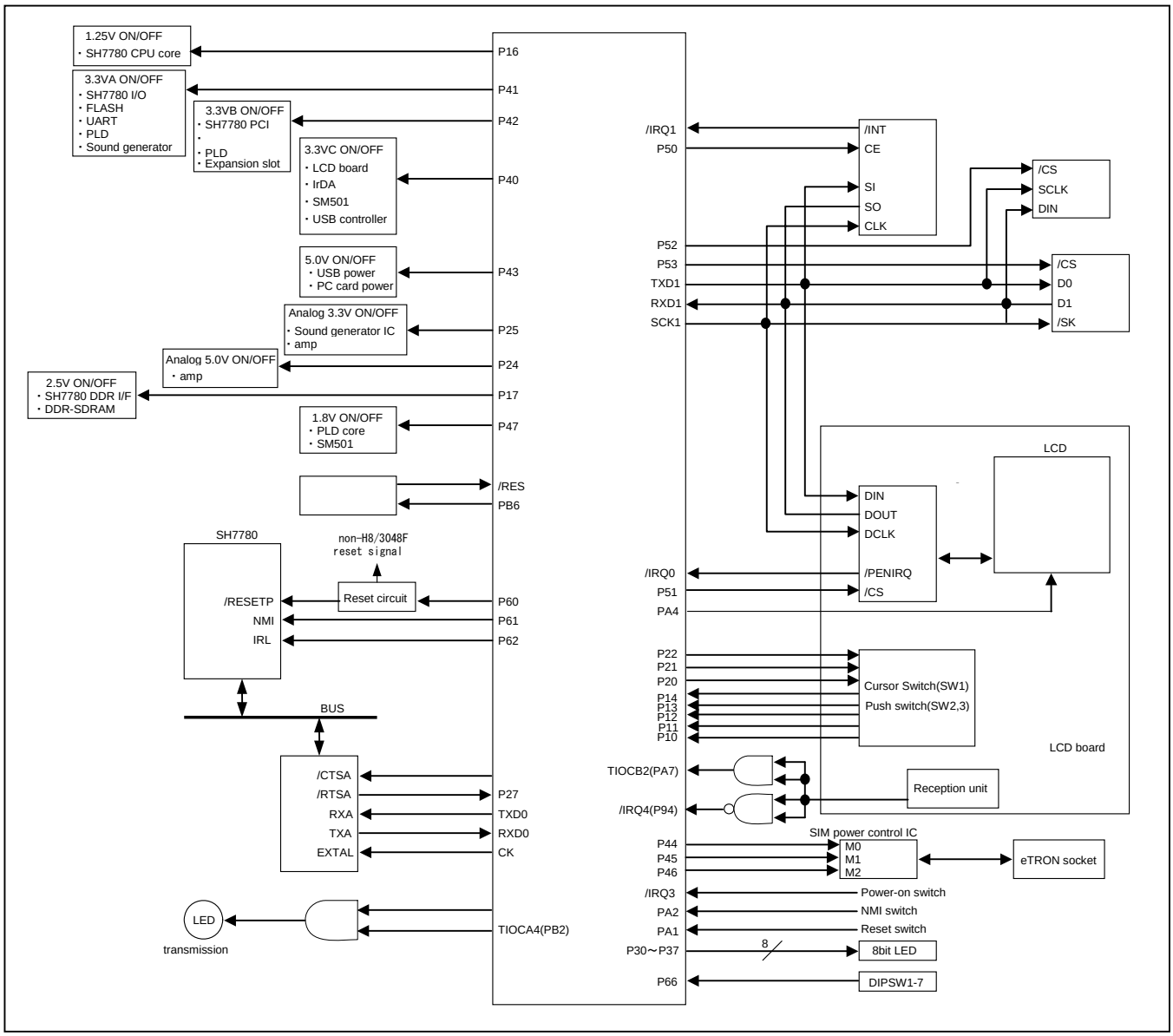


Figure 6.1 Power Supply Control Block Diagram

⚠ CAUTION

Though the power supply controller's I/O port is connected to the /RTSA and /CTSA pins of the UART controller (XR16L2550IM-F) through the circuit, the power supply controller does not execute hardware control during communications with SH7780. For details of communications between SH7780 and the power supply controller, refer to 6.2 “Serial Communications between SH7780 and the Power Supply Controller.”

6.2 Serial Communications between SH7780 and the Power Supply Controller

This section describes how serial communications take place between SH7780 and the power supply controller.

6.2.1 Serial Format

This subsection describes a format for serial communications between SH7780 and the power supply controller.

(1) Mode: asynchronous communication

(2) Baud rate: 38400 bits/second

(3) Stop bit: 1 bit

(4) Start bit: 1 bit

(5) Parity bit: None

(6) LSB first

6.2.2 Power Supply Control Register Read Procedure

This subsection describes a procedure for reading the power supply control registers.

(1) SH7780 issues a read command to a power supply controller.

(2) The power supply controller returns a response to SH7780.

⚠ CAUTION

Don’t issue multiple commands continually from SH7780. Note that the next command must be issued after a response to the preceding command has been returned from the power supply controller.

6.2.3 Read Command

Figure 6.2 shows a read command format. SH7780 sends a start code, a function code and a register address, in this order, as a read command.

(1) Start code (1 byte)	(2) Function code (1 byte or 2 bytes)	(3) Register address (2 bytes)

Figure6.2 Read Command

(1) Start code

The code is fixed at 0 x 02.

(2) Function code

- A 1-byte function code specifies the size of data to be read in the lower 4 bits when the upper 4 bits of a function code are 1000. Figure 6.3 shows a function command where the upper 4 bits are 1000.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	Size of data			

Figure6.3 Function Command (1 Byte)

- A 2-byte function code specifies the size of data to be read in the lower 12 bits when the upper 4 bits of a function code are 1001. Figure 6.4 shows a function command where the upper 4 bits are 1001.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	Size of data											

Figure6.4 Function Command (2 Bytes)

(3) Register Address

The register address specifies the address of the register to be read.

6.2.4 Normal Response during a Read Operation

Figure 6.5 shows the response format for the read command. The power supply controller returns an ACK code, a function code, a register address and target data, in this order, as a response.

(1) ACK code(1 byte)	(2) Function code (1 byte or 2 bytes)	(3) Register address (2 bytes)	(4) Data (N byte)

Figure 6.5 Normal Response during a Read Operation

(1) ACK code

The code is fixed at ACK (0x06).

(2) Function code

The same function code as for the read command returns.

(3) Register address

The address of a register subject to a read operation returns.

(4) Data

Read data returns. The size of this data is equal to the value specified in the function code.

6.2.5 Error Response during a read Operation

Figure 6.6 shows the error response format for the read command. The power supply controller returns a NAK code and an error code in this order as a response at error occurrence.

Figure 6.6 Error Response during a Read Operation

(1) NAK code

This code is fixed at NAK (0x15).

(2) Error code

Table 6.1 summarizes the error codes.

Table 6.1 Error Codes

Error No	Error type
0x01	Communications error
0x02	Invalid function code
0x03	Invalid register number
0x04	Register size error
0x05	Data size error

6.2.6 Power Supply Control Register Write Procedure

This subsection describes the procedure for writing to a controller control of the power supply controller from SH7780.

(1) SH7780 issues a write command to the power supply controller.

(2) The power supply controller returns a response the SH7780.

⚠ CAUTION

Don't issue multiple commands continually from SH7780. Note that the next command must be issued after a response to the preceding command has been returned from the power supply controller.

6.2.7 Write Command

Figure 6.7 shows the write command format. SH7780 sends a start code, a function code, a register address and data, in this order, as a write command.

(1) Start code (1 byte)	(2) Function code (1 byte or 2 byte)	(3) Register address (2 byte)	(4) Register address (N byte)

Figure 6.7 Read Command

(1) Start code

This code is fixed at 0x02.

(2) Function code

• A 1-byte function code specifies the size of data to be written in the lower 4 bits when the upper 4 bits of a function code are 1100. Figure 6.8 shows a function command where the upper 4 bits are 1100.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	Size of data			

Figure 6.8 Function Command (1 Byte)

• A 2-byte function code specifies the size of data to be written in the lower 12 bits when the upper 4 bits of a function code are 1101. Figure 6.9 shows a function command where the upper 4 bits are 1101.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	Size of data											

Figure 6.9 Function Command (2 Bytes)

(3) Register Address

The register address specifies the address of the register to be written.

(4) Data

This field specifies the size of data to be written. This data size is equal to that specified in the function code.

6.2.8 Normal Response during a Write Operation

Figure 6.10 shows the response format for the write command. The power supply controller returns an ACK code, a function code, a register address and target data, in this order, as a response for the write command.

(1) ACK code (1 byte)	(2) Function code (1 byte or 2 byte)	(3) Register address (2 byte)	(4) Data (N byte)

Figure 6.10 Normal Response during a Write Operation

(1) ACK code

This code is fixed at ACK (0x06).

(2) Function code

The same code as for the write command returns.

(3) Register address

The address of a register subject to a write operation returns.

(4) Data

Write data returns. The size of this data is equal to the value specified in the function code. However, note that no data returns for IRRSFDR subject to infrared remote control and EEPDR subject to serial EEPROM control.

6.2.9 Error Response during a Write Operation

Figure 6.11 shows an error response format for the write command at error occurrence. The power supply controller returns a NAK code and an error code in this order as an error response.

(1) NAK code (1 byte)	(2) Error code (1 byte)

Figure 6.11 Error Response during a Write Operation

(1) NAK code

This code is fixed at NAK (0x15).

(2) Error code

Table 6.2 summarizes the error codes.

Table 6.2 Error Codes

Error No.	Error type
0x01	Communications error
0x02	Invalid function code
0x03	Invalid register number
0x04	Register size error
0x05	Data size error

6.3 RTC (Real-time Clock) Functions

This section describes the RTC functions. Table 6.1 summarizes the RTC registers. For a detailed description of each register, refer to 6.3.1 to 6.3.17.

(1) Function for counting the seconds, minutes, hours, day of the week, month, and year (BCD code)

(2) RTC start/stop function

(3) Alarm interrupt function

(4) 1sec/0.5sec cyclic interrupt function

(5) Automatic correction function for leap years

(6) Effective range of operation from January 1, 2000 to December 31, 2099

Table 6.3 RTC Registers

Register	Abbreviation	Address	R/W	Size	Remarks
RTC control register	RTCCR	0x0000	R/W	1 byte	
RTC status register	RTCSR	0x0001	R/W	1 byte	
Second counter	SECCNT	0x0002	R/W	1 byte	
Minute counter	MINCNT	0x0003	R/W	1 byte	
Hour counter	HRCNT	0x0004	R/W	1 byte	
Day-of-the-week counter	WKCNT	0x0005	R/W	1 byte	
Day counter	DAYCNT	0x0006	R/W	1 byte	
Month counter	MONCNT	0x0007	R/W	1 byte	
Year counter	YRCNT	0x0008	R/W	1 byte	
Second alarm counter	SECAR	0x0009	R/W	1 byte	
Minute alarm counter	MINAR	0x000A	R/W	1 byte	
Hour alarm counter	HRAR	0x000B	R/W	1 byte	
Day-of-the-week alarm counter	WKAR	0x000C	R/W	1 byte	
Day alarm counter	DAYAR	0x000D	R/W	1 byte	
Month alarm counter	MONAR	0x000E	R/W	1 byte	
RTC/Touch panel/Key input/Power supply status register	RTKISR	0x0090	R/W	1 byte	

6.3.1 RTC Control Register (RTCCR)

Address: 0x000 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	CNTS	SECCAF	0.5secI	1secI	ARI	START
R	R	R/W	R/W	R/W	R/W	R/W	R/W

(1) START

START bit	Setting
0	RTC start (Initial value)
1	RTC stop

⚠ CAUTION

Don't write to any counter while the START bit is set to "0." Rewrite each counter after setting the START bit to "1."

(2) ARI

ARI bit	Setting
0	No alarm interrupt is generated (Initial value)
1	An alarm interrupt is generated

(3) 1secI

1secI bit	Setting
0	No interrupt is generated at intervals of 1 second. (Initial value)
1	An interrupt is generated at intervals of 1 second.

(4) 0.5secI

0.5secI bit	Setting
0	No interrupt is generated at intervals of 0.5 second. (Initial value)
1	An interrupt is generated at intervals of 0.5 second.

(5) SECCAF

SECCAF bit	Setting
0	No carry has been generated in the second counter (SECCNT). (Initial value)
1	A carry has been generated in the second counter (SECCNT). [Zero-clear condition] The SECCAF bit is set to "1.''

(6) CNTS

CNTS bit	Setting
0	The setting (value) of each counter is not updated. (Initial value)
1	The setting (value) of each counter is updated. [Zero-clear condition] Counter update is completed. This clear operation is automatically performed.

⚠ CAUTION

Don't write to any counter while the START bit is set to "0." Set the CNTS bit to "1" after updating the value of each counter with the START bit set to "1."

6.3.2 RTC Status Register (RTCSR)

Address: 0x001 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0.5 secF	1 secF	ARF	0
R	R	R	R	R/W	R/W	R/W	R

(1) ARF

ARF bit	Setting
0	The setting of each alarm register with the AR bit set is not the same as that of each counter register (Initial value)
1	The setting of each alarm register with the AR bit set is identical to that of each counter register. At this time, an interrupt occurs if the ARI bit is set to "1.'' [Clear condition] "0'' is written with the ARF bit set to "1.''

(2) 1secF

1secF bit	Setting
0	A second has not elapsed yet (Initial value)
1	A second has elapsed. [Clear condition] "0'' is written with the 1secF bit set to "1.''

(3) 0.5secF

0.5secF bit	Setting
0	A half second has not elapsed yet. (Initial value)
1	A half second has elapsed yet. [Clear condition] "0'' is written with the 0.5secF bit set to "1.''

6.3.3 Second Counter (SECCNT)

Address: 0x002 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 second			1 second			
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 00 to 59. When the value changes from 59 to 00, a carry is generated in the minute counter.

6.3.4 Minute Counter (MINCNT)

Address: 0x0003 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	10 minutes			1 minutes			
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 00 to 59. When the value changes from 59 to 00, a carry is generated in the hour counter.

6.3.5 Hour Counter (HRCNT)

Address: 0x0004 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 hours		1 hours			
R	R	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 00 to 23. When the value changes from 23 to 00, a carry is generated in the day counter and the day-of-the-week counter.

6.3.6 Day-of-the-Week Counter (WKCNT)

Address: 0x0005 Initial Value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Septinary incremental counter		
R	R	R	R	R	R/W	R/W	R/W

Counting takes place within a range from 0x00 to 0x06.

The following shows the correspondence between the day of the week and the value of the septinary incremental counter.

(D2.D1.D0) = (0.0.0) →Sunday

(D2.D1.D0) = (0.0.1) →Monday

(D2.D1.D0) = (0.1.0) →Tuesday

(D2.D1.D0) = (0.1.1) →Wednesday

(D2.D1.D0) = (1.0.0) →Thursday

(D2.D1.D0) = (1.0.1) →Friday

(D2.D1.D0) = (1.1.0) →Saturday

6.3.7 Day Counter (DAYCNT)

Address: 0x0006 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 days		1 day			
R	R	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 1 to 31 (January, March, July, August, October and December), 1 to 30 (April, June, September and November), 1 to 28 (February in normal year) or 1 to 29 (February in leap year).

6.3.8 Month Counter (MONCNT)

Address: 0x0007 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	October	January			
R	R	R	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 1 to 12. When the counter value changes from 12 to 1, a carry is generated in the year counter.

6.3.9 Year Counter (YRCNT)

Address: 0x0008 Initial value: 0xXX (Not defined)

D7	D6	D5	D4	D3	D2	D1	D0
10 years				1 year			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The counter value is a BCD (Binary Coded Decimal) value. Counting takes place within a range from 0 to 99.

In this range, 00, 04, ..., 92 and 96 are leap years.

6.3.10 Alarm Register

Each alarm register corresponds to the relevant counter as shown below.

If the AR bit (D7) of each alarm is set to “1,” counters will be compared with alarm registers. This comparison is performed only for alarm registers with the AR bit (D7) set to “1” and an alarm interrupt is generated only at correct correspondence.

• Correspondence between the alarm registers and counters

Second alarm register (BCD code): second counter

Minute alarm register (BCD code): minute counter

Hour alarm register (BCD code): Hour counter

Day-of-the-week alarm register (0x00 to 0x07): Day-of-the-week counter

Day alarm register (BCD code): Day counter

Month alarm register (BCD code): Month counter

6.3.11 Second Alarm Register (SECAR)

Address: 0x0009 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	10 seconds			1 second			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 00 and 59.

6.3.12 Minute Alarm Register (MINAR)

Address: 0x000A Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	10 minutes			1 minute			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 00 and 59.

6.3.13 Hour Alarm Register (HRAR)

Address: 0x000B Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	10 hours		1 hour			
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 00 and 23.

6.3.14 Day-of-the-Week Alarm Register (WKAR)

Address: 0x000C Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	0	0	0	Septinary counter value		
R/W	R	R	R	R	R/W	R/W	R/W

The alarm value must be set within a range from 0x00 to 0x06.

• Day of the week and septinary counter value

(D2.D1.D0) = (0.0.0) → Sunday

(D2.D1.D0) = (0.0.1) → Monday

(D2.D1.D0) = (0.1.0) → Tuesday

(D2.D1.D0) = (0.1.1) → Wednesdady

(D2.D1.D0) = (1.0.0) → Thursday

(D2.D1.D0) = (1.0.1) → Friday

(D2.D1.D0) = (1.1.0) → Saturday

6.3.15 Day Alarm Register (DAYAR)

Address: 0x000D Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	10 days		1 day			
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 1 and 31 (January, March, May, July, August, October and December), between 1 and 30 (April, June, September and November), between 1 and 28 (February in normal year) or between 1 and 29 (February in leap year).

6.3.16 Month Alarm Register (MONAR)

Address: 0x000E Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
AR	0	0	October	January			
R/W	R	R	R/W	R/W	R/W	R/W	R/W

The alarm value must be a BCD (Binary Coded Decimal) code between 01 and 12.

6.3.17 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel or key input status. The following is a brief description of RTC-related status bits.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) RTCIF

RTCIF bit	Setting
0	The ARF, 1secF ad 0.5secF bits of the RTC register are all set to “0.’’ (Initial value)
1	One of the ARF, 1secF ad 0.5 secF bits of the RTC register is set to “1.’’ [Clear condition] “0’’ is written with the RTCIF bit set to ‘‘1.’’

6.4 Touch Panel Functions

This section describes the touch panel functions. In addition, Table 6.4 summarizes the touch panel registers. For details of each register, refer to 6.4.1 to 6.4.32.

(1) The A/D conversion value of the X or Y position sensed by pen touch is output.

(2) Pen touch ON/OFF interrupt function

Sampling takes place at intervals of 20msec to 100msec. When the results (A/D conversion value of the X or Y position) obtained three times from sampling are approximate to each other, a pen touch ON interrupt is generated for SH7780. In addition, when the touch panel is turned off, a pen touch OFF interrupt is generated.

(3) To keep the pen touch “ON,” sampling is performed at intervals of 20msec to 100msec and a pen touch ON interrupt is generated if the results obtained from sampling are approximate to each other.

(4) Calibration function

Calibration is performed when two points on the touch panel are touched with the pen. After completion of calibration, the X and Y positions are converted into the LCD drawing dot positions for output.

Table 6.4 Touch Panel Registers

Register	Abbreviation	Address	R/W	Size	Remarks
Touch panel control register	TPLCR	0x0020	R/W	1 byte	
Touch panel status register	TPLSR	0x0021	R/W	1 byte	
Touch panel sampling control register	TPLSCR	0x0022	R/W	1 byte	
X position A/D register	XPAR	0x0024	R	2 bytes	
Y position A/D register	YPAR	0x0026	R	2 bytes	
X position dot register	XPDR	0x0028	R	2 bytes	
Y position dot register	YPDR	0x002A	R	2 bytes	
XA position dot register	XAPDR	0x002C	R/W	2 bytes	
YA position dot register	YAPDR	0x002E	R/W	2 bytes	
XB position dot register	XBPDR	0x0030	R/W	2 bytes	
YB position dot register	YBPDR	0x0032	R/W	2 bytes	
XC position dot register	XCPDR	0x0034	R/W	2 bytes	
YC position dot register	YCPDR	0x0036	R/W	2 bytes	
XA position A/D register	XAPAR	0x0038	R/W	2 bytes	
YA position A/D register	YAPAR	0x003A	R/W	2 bytes	
XB position A/D register	XBPAR	0x003C	R/W	2 bytes	
YB position A/D register	YBPAR	0x003E	R/W	2 bytes	
XC position A/D register	XCPAR	0x0040	R/W	2 bytes	
YC position A/D register	YCPAR	0x0042	R/W	2 bytes	
DX dot register	DXDR	0x0044	R/W	2 bytes	
DY dot register	DYDR	0x0046	R/W	2 bytes	
X position dot calculation A/D value	XPARDOT	0x0048	R/W	2 bytes	
X position A/D value 1	XPARDOT1	0x004A	R/W	2 bytes	
X position A/D value 2	XPARDOT2	0x004C	R/W	2 bytes	
X position A/D value 3	XPARDOT3	0x004E	R/W	2 bytes	
X position A/D value 4	XPARDOT4	0x0050	R/W	2 bytes	
Y position dot calculation A/D value	YPARDOT	0x0052	R/W	2 bytes	
Y position A/D value 1	YPARDOT1	0x0054	R/W	2 bytes	
Y position A/D value 2	YPARDOT2	0x0056	R/W	2 bytes	
Y position A/D value 3	YPARDOT3	0x0058	R/W	2 bytes	
Y position A/D value 4	YPARDOT4	0x005A	R/W	2 bytes	
RTC/Touch Panel/Key Input/Power Supply Status Register	RTKISR	0x0090	R/W	1 byte	

6.4.1 Touch Panel Control Register (TPLCR)

Address: 0x0020 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PEN_ONRE	PEN_OFFI	PEN_ONI	TP_STR
R	R	R	R	R/W	R/W	R/W	R/W

(1) TP_STR

TP_STR bit	Setting
0	The touch panel is disabled. (Initial value)
1	The touch panel is enabled.

(2) PEN_ONI

PEN_ONI bit	Setting
0	A pen touch ON interrupt is not generated. (Initial value)
1	A pen touch ON interrupt is generated.

(3) PEN_OFFI

PEN_OFFI bit	Setting
0	A pen touch OFF interrupt is not generated. (Initial value)
1	A pen touch OFF interrupt is generated.

(4) PEN_ONRE

PEN_ ONRE bit	Setting
0	A pen touch ON interrupt is not generated when pen touch continues. (Initial value)
1	A pen touch ON interrupt is generated when pen touch continues.

6.4.2 Touch Panel Status Register (TPLSR)

Address: 0x0021 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	PEN_OFFIF	PEN_ONIF	0
R	R	R	R	R	R/W	R/W	R

(1) PEN_ONIF

PEN_ONIF bit	Setting
0	The touch panel has not been pen-touched. (pen touch OFF) (Initial value)
1	The pen-touch state on the touch panel has been changed from OFF to ON. The touched positions on the touch panel are output to the X position A/D register, Y position A/D register, X position dot register and Y position dot register. At this time, a pen touch ON interrupt is generated if the PEN_ONI bit is set to “1.’’ [Clear condition] “0’’ is written with the PEN_ONIF bit set to ‘’1.’’

(2) PEN_OFFIF

PEN_OFFIF bit	Setting
0	The touch panel has not been pen-touched. (pen touch OFF) (Initial value)
1	The pen-touch state on the touch panel has been changed from ON to OFF. At this time, a pen touch OFF interrupt is generated if the PEN_OFFI bit is set to “1.’’ [Clear condition] “0’’ is written with the PEN_OFFIF bit set to ‘’1.’’

6.4.3 Touch panel Sampling Control Register (TPLSCR)

The touch panel sampling control register sets a sampling interval for the touch panel.

Address: 0x0022 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
160msec	140msec	120msec	100msec	80msec	60msec	40msec	20msec
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

A sampling interval for the touch panel can be set within a range from 20msec to 160msec (unit: 20msec). When a bit is set to “1,” the corresponding sampling interval from 20msec to 160msec is set. Note that only the following values can be specified.

• Correspondence between the setting values and sampling intervals

0x01: 20msec

0x02: 40msec

0x04: 60msec

0x08: 80msec

0x10: 100msec

0x20: 120msec

0x40: 140msec

0x80: 160msec

6.4.4 X Position A/D Register (XPAR)

Address: 0x0024 Initial value: 0x000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XA_D11	XA_D10	XA_D9	XA_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
XA_D7	XA_D6	XA_D5	XA_D4	XA_D3	XA_D2	XA_D1	XA_D0
R	R	R	R	R	R	R	R

The X position A/D register indicates the A/D conversion result of a pen-touched X position on the touch panel.

6.4.5 Y Position A/D Register (YPAR)

Address: 0x0026 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YA_D11	YA_D10	YA_D9	YA_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
YA_D7	YA_D6	YA_D5	YA_D4	YA_D3	YA_D2	YA_D1	YA_D0
R	R	R	R	R	R	R	R

The Y position A/D register indicates the A/D conversion result of a pen-touched Y position on the touch panel.

6.4.6 X Position Dot Register (XPDR)

Address: 0x0028 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XD_D15	XD_D14	XD_D13	XD_D12	XD_D11	XD_D10	XD_D9	XD_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
XD_D7	XD_D6	XD_D5	XD_D4	XD_D3	XD_D2	XD_D1	XD_D0
R	R	R	R	R	R	R	R

The X position dot register indicates the dot position of a pen-touched X position on the touch panel. Use the output value of this register after calibration. The output value is not settled without calibration.

6.4.7 Y Position Dot Register (YPDR)

Address: 0x002A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YD_D15	YD_D14	YD_D13	YD_D12	YD_D11	YD_D10	YD_D9	YD_D8
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
YD_D7	YD_D6	YD_D5	YD_D4	YD_D3	YD_D2	YD_D1	YD_D0
R	R	R	R	R	R	R	R

The Y position dot register indicates the dot position of a pen-touched Y position on the touch panel. Use the output value of this register after calibration. The output value is not settled without calibration.

6.4.8 XA Position Dot Register (XAPDR)

Address: 0x002C Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XAD_D15	XAD_D14	XAD_D13	XAD_D12	XAD_D11	XAD_D10	XAD_D9	XAD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XAD_D7	XAD_D6	XAD_D5	XAD_D4	XAD_D3	XAD_D2	XAD_D1	XAD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XA position dot register indicates the X dot position of point A when calibration takes place.

6.4.9 YA Position Dot Register (YAPDR)

Address: 0x002E Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YAD_D15	YAD_D14	YAD_D13	YAD_D12	YAD_D11	YAD_D10	YAD_D9	YAD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YAD_D7	YAD_D6	YAD_D5	YAD_D4	YAD_D3	YAD_D2	YAD_D1	YAD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YA position dot register indicates the Y dot position of point A when calibration takes place.

6.4.10 XB Position Dot Register (XBPDR)

Address: 0x0030 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XBD_D15	XBD_D14	XBD_D13	XBD_D12	XBD_D11	XBD_D10	XBD_D9	XBD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XBD_D7	XBD_D6	XBD_D5	XBD_D4	XBD_D3	XBD_D2	XBD_D1	XBD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XB position dot register indicates the X dot position of point B when calibration takes place.

6.4.11 YB Position Dot Register (YBPDR)

Address: 0x0032 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YBD_D15	YBD_D14	YBD_D13	YBD_D12	YBD_D11	YBD_D10	YBD_D9	YBD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YBD_D7	YBD_D6	YBD_D5	YBD_D4	YBD_D3	YBD_D2	YBD_D1	YBD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YB position dot register indicates the Y dot position of point B when calibration takes place.

6.4.12 XC Position Dot Register (XCPDR)

Address: 0x0034 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
XCD_D15	XCD_D14	XCD_D13	XCD_D12	XCD_D11	XCD_D10	XCD_D9	XCD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XCD_D7	XCD_D6	XCD_D5	XCD_D4	XCD_D3	XCD_D2	XCD_D1	XCD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XC position dot register indicates the X dot position of point C when calibration takes place. This register will be functionally enhanced in future. Don't access this register.

6.4.13 YC Position Dot Register (YCPDR)

Address: 0x0036 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
YCD_D15	YCD_D14	YCD_D13	YCD_D12	YCD_D11	YCD_D10	YCD_D9	YCD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YCD_D7	YCD_D6	YCD_D5	YCD_D4	YCD_D3	YCD_D2	YCD_D1	YCD_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YC position dot register indicates the Y dot position of point C where calibration takes place. This register will be functionally enhanced in future. Don't access this register.

6.4.14 XA Position A/D Register (XAPAR)

Address: 0x0038 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XAA_D11	XAA_D10	XAA_D9	XAA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XAA_D7	XAA_D6	XAA_D5	XAA_D4	XAA_D3	XAA_D2	XAA_D1	XAA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XA position A/D register indicates the X position A/D conversion result of point A subject to calibration.

6.4.15 YA Position A/D Register (YAPAR)

Address: 0x003A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YAA_D11	YAA_D10	YAA_D9	YAA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YAA_D7	YAA_D6	YAA_D5	YAA_D4	YAA_D3	YAA_D2	YAA_D1	YAA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YA position A/D register indicates the Y position A/D conversion result of point A subject to calibration.

6.4.16 XB Position A/D Register (XBPAR)

Address: 0x003C Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XBA_D11	XBA_D10	XBA_D9	XBA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XBA_D7	XBA_D6	XBA_D5	XBA_D4	XBA_D3	XBA_D2	XBA_D1	XBA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XB position A/D register indicates the X position A/D conversion result of point B subject to calibration.

6.4.17 YB Position A/D Register (YBPAR)

Address: 0x003E Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YBA_D11	YBA_D10	YBA_D9	YBA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YBA_D7	YBA_D6	YBA_D5	YBA_D4	YBA_D3	YBA_D2	YBA_D1	YBA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YB position A/D register indicates the Y position A/D conversion result of point B subject to calibration.

6.4.18 XC Position A/D Register (XCPAR)

Address: 0x0040 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	XCA_D11	XCA_D10	XCA_D9	XCA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XCA_D7	XCA_D6	XCA_D5	XCA_D4	XCA_D3	XCA_D2	XCA_D1	XCA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The XC position A/D register indicates the X position A/D conversion result of point C subject to calibration. This register will be functionally enhanced in future. Don't access this register.

6.4.19 YC Position A/D Register (YCPAR)

Address: 0x0042 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	YCA_D11	YCA_D10	YCA_D9	YCA_D8
R	R	R	R	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YCA_D7	YCA_D6	YCA_D5	YCA_D4	YCA_D3	YCA_D2	YCA_D1	YCA_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The YC position A/D register indicates the Y position A/D conversion result of point C subject to calibration.
This register will be functionally enhanced in future. Don't access this register.

6.4.20 DX Dot Register (DXDR)

Address: 0x0044 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
DX1_D15	DX1_D14	DX1_D13	DX1_D12	DX1_D11	DX1_D10	DX1_D9	DX1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
DX1_D7	DX1_D6	DX1_D5	DX1_D4	DX1_D3	DX1_D2	DX1_D1	DX1_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DX dot register holds a value obtained by multiplying the number of dots per data (X position A/D conversion result at calibration) by 1,000. The power supply controller outputs a dot position of the X position to be stored in the X position dot register (XPDR) from the values set in the DX dot register (DXDR), XA position dot register (XAPDR) and XA position A/D register (XAPAR). When the DX dot register (DXDR) has been set to “0,” the dot position is not calculated.

6.4.21 DY Dot Register (DYDR)

Address: 0x0046 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
DY1_D15	DY1_D14	DY1_D13	DY1_D12	DY1_D11	DY1_D10	DY1_D9	DY1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
DY1_D7	DY1_D6	DY1_D5	DY1_D4	DY1_D3	DY1_D2	DY1_D1	DY1_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DY dot register (DY1DR) holds a value obtained by multiplying the number of dots per data (Y position A/D conversion result at calibration) by 1,000. The power supply controller outputs a dot position of the Y position to be stored in the Y position dot register (YPDR) from the values set in the DY dot register (DYDR), YA position dot register (YAPDR) and YA position A/D register (YAPAR). When the DY dot register (DY1DR) has been set to “0,” the dot position is not calculated.

6.4.22 X Position Dot Calculation A/D Value (XPARDOT)

Address: 0X0048 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD_D9	XD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD_D7	XD_D6	XD_D5	XD_D4	XD_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value register (XPARDOT) holds an AD value of X position dot calculation. This A/D value is obtained by calculating the mean of the previous four XPARDOT values and clearing the low order 3 bits with zeros.

6.4.23 X Position Dot Calculation A/D Value 1 (XPARDOT1)

Address: 0x004A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD1_D9	XD1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD1_D7	XD1_D6	XD1_D5	XD1_D4	XD1_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 1 register (XPARDOT1) holds an XPARDOT value before sampling.

6.4.24 X Position Dot Calculation A/D Value 2 (XPARDOT2)

Address: 0x004C Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD2_D9	XD2_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD2_D7	XD2_D6	XD2_D5	XD2_D4	XD2_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 2 register (XPARDOT2) holds an XPARDOT value before sampling.

6.4.25 X Position Dot Calculation A/D Value 3 (XPARDOT3)

Address: 0x004E Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD3_D9	XD3_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD3_D7	XD3_D6	XD3_D5	XD3_D4	XD3_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 3 register (XPARDOT3) holds an XPARDOT value before sampling.

6.4.26 X Position Dot Calculation A/D value 4 (XPARDOT4)

Address: 0x0050 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	XD4_D9	XD4_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
XD4_D7	XD4_D6	XD4_D5	XD4_D4	XD4_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The X position dot calculation A/D value 4 register (XPARDOT4) holds an XPARDOT value before sampling.

6.4.27 Y Position Dot Calculation A/D Value (YPARDOT)

Address: 0x0052 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD_D9	YD_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD_D7	YD_D6	YD_D5	YD_D4	YD_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value register (YPARDOT) holds an A/D value of Y position dot calculation. This A/D value is obtained by calculating the mean of the previous four YPARDOT values and clearing the following 3 bits with zeros.

6.4.28 Y Position Dot Calculation A/D Value 1 (YPARDOT1)

Address: 0 x0054 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD1_D9	YD1_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD1_D7	YD1_D6	YD1_D5	YD1_D4	YD1_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 1 register (YPARDOT1) holds a YPARDOT value before sampling.

6.4.29 Y Position Dot Calculation A/D Value 2 (YPARDOT2)

Address: 0x0056 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD2_D9	YD2_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD2_D7	YD2_D6	YD2_D5	YD2_D4	YD2_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 2 register (YPARDOT2) holds a YPARDOT value before sampling.

6.4.30 Y Position Dot Calculation A/D Value 3 (YPARDOT3)

Address: 0x0058 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD3_D9	YD3_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD3_D7	YD3_D6	YD3_D5	YD3_D4	YD3_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 3 register (YPARDOT3) holds a YPARDOT value before sampling.

6.4.31 Y Position Dot Calculation A/D Value 4 (YPARDOT4)

Address: 0x005A Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	YD4_D9	YD4_D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
YD4_D7	YD4_D6	YD4_D5	YD4_D4	YD4_D3	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Y position dot calculation A/D value 4 register (YPARDOT4) holds a YPARDOT value before sampling.

6.4.32 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits related to the touch panel.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) TPIF

TPIF bit	Setting
0	The PEN_ONIF, PEN_OFFIF, CAIF and CAEF bits of the touch panel status registered are all set to “0.’’ (Initial value)
1	One of the PEN_ONIF, PEN_OFFIF, CAIF and CAEF bits of the touch panel status register is set to “1.’’ [Clear condition] “0’’ is written with the TPIF bit set to “1.’’

6.4.33 Touch Panel Calibration Method (2-point System)

The power supply controller supports 2-point touch panel calibration. Figure 6.12 shows the points of the drawing coordinates and A/D conversion coordinates that are necessary for calibration.

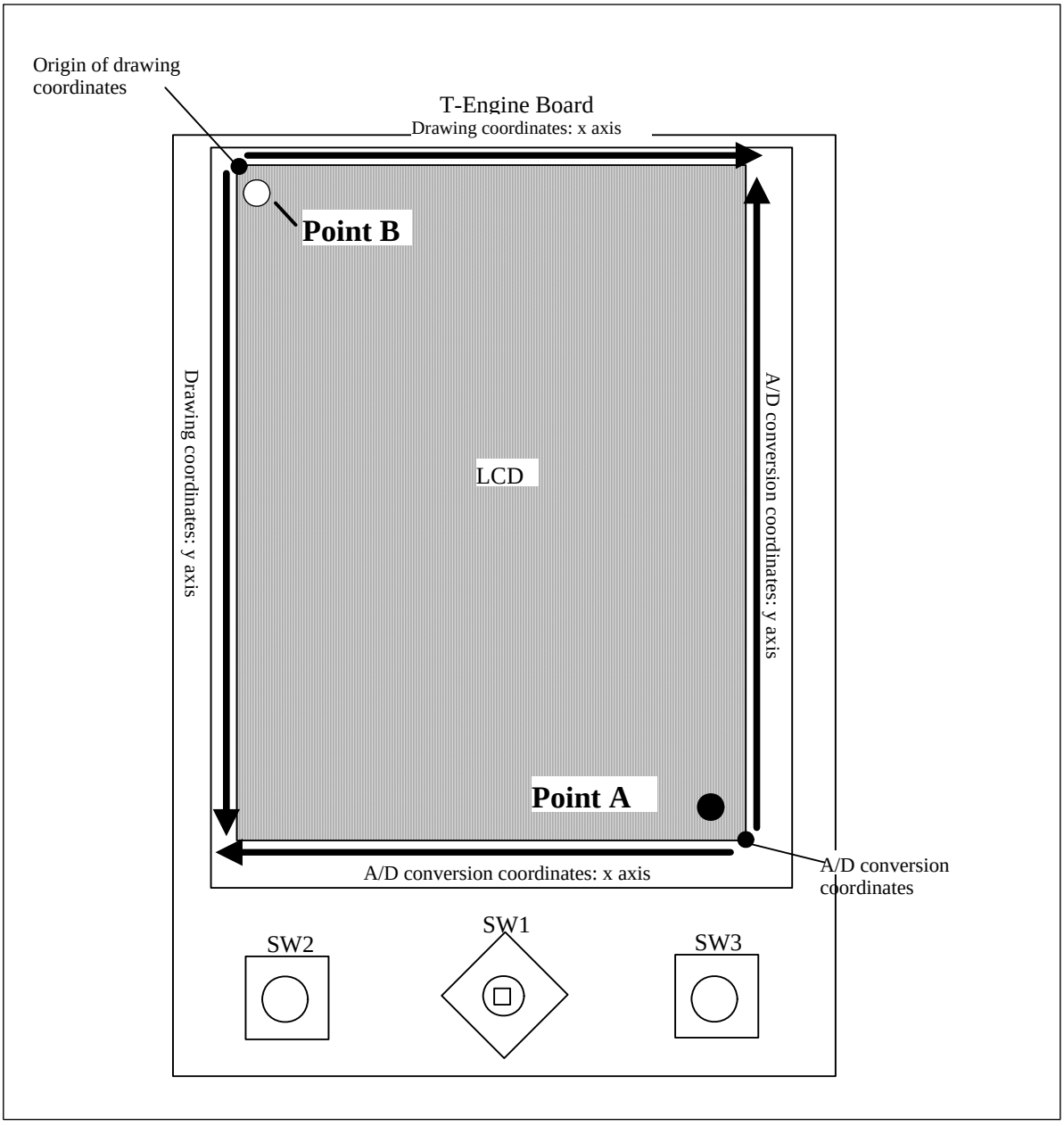


Figure 6.12 Points of the Drawing Coordinates and A/D Conversion Coordinates

[Calibration Method]

(1) The SH7780 writes the dot points of points A and B to the registers XAPDR, YAPDR, XBPDR, and YBPDR.

(2) When point A is pen-touched, it is signaled by a pen touch interrupt. The A/D conversion result of the pen-touched point A is written to the registers XAPAR and YAPAR.

(3) Next, when point B is pen-touched, it is signaled by a pen touch interrupt. The A/D conversion result of the pen-touched point B is written to the registers XBPAR and YBPAR.

(4) Calibration takes place according to data in the above steps (1) to (3). Using the following expression, the SH7780 calculates the number of dots per data of the X position A/D conversion result and that of the Y position A/D conversion result.

Number of dots per data of the X position A/D conversion result (DX)

DX = (DXA – DXB) / (TXB – TXA) Where TXA < TXB, DXA > DXB

Number of dots per data of the Y position A/D conversion result (DY)

DY = (DYA – DYB) / (TYB- TYA) Where TYA < TYB, DYA > DYB

DXA: X position drawing dot point of point A (XAPDR)
DXB: X position drawing dot point of point B (XBPDR)
TXA: X position A/D conversion result of point A (XAPAR)
TXB: X position A/D conversion result of point B (XBPAR)
DYA: Y position drawing dot point of point A (YAPDR)
DYB: Y position drawing dot point of point B (YBPDR)
TXA: Y position A/D conversion result of point A (YAPAR)
TXB: Y position A/D conversion result of point B (YBPAR)

（5） The above calculation results are multiplied by 1,000, their decimal places are rounded, and the resulting integers are written to the registers DXDR and DYDR.

DX dot register (DXDR) = DX x 1,000 (rounding the decimal places)

DY dot register (DYDR) = DY x 1,000 (rounding the decimal places)

（6） The power supply controller uses data stored in the registers DXDR, DYDR, XAPDR, YAPDR, XAPAR, and YAPAR to calculate dot position data (XPDR, YPDR) of the pen-touched point on the LCD. The power supply controller uses the following expression to calculate dot position data.

X position dot register (XPDR)

XPDR = (DXA – (DX x (TXD – TXA)) / 1,000

Y position dot register (YPDR)

YPDR = (DYA – (DY x (TYD – TYA)) / 1,000

DXA: XA position dot register (XAPDR) data
DX: DX1 dot register (DXDR) data
TXA: XA position A/D register (XAPAR) data
TXD: X position A/D register (XPAR) data
DYA: YA position dot register (YAPDR) data
DY: DY dot register (DYDR) data
TYA: YA position A/D register (YAPAR) data
TYD: X position A/D register (YPAR) data

The power supply controller outputs data stored in the X position A/D register (XPAR) and Y position A/D register (YPAR). When the values stored in the DX dot register (DXDR) and DY dot register (DYDR) are not 0, the power supply controller outputs the data derived from the above expressions to the X position dot register (XPDR) and Y position dot register (YPDR). When either value is 0, it does not use the above expression for calculation and outputs only XPAR and YPAR data.

6.5 Key Switch Control

Figure 6.13 shows the T-Engine switches under control by the power supply controller. The power supply controller controls the switches SW1 to SW3 on the CPU board and the switches SW1to SW3 on the LCD board.

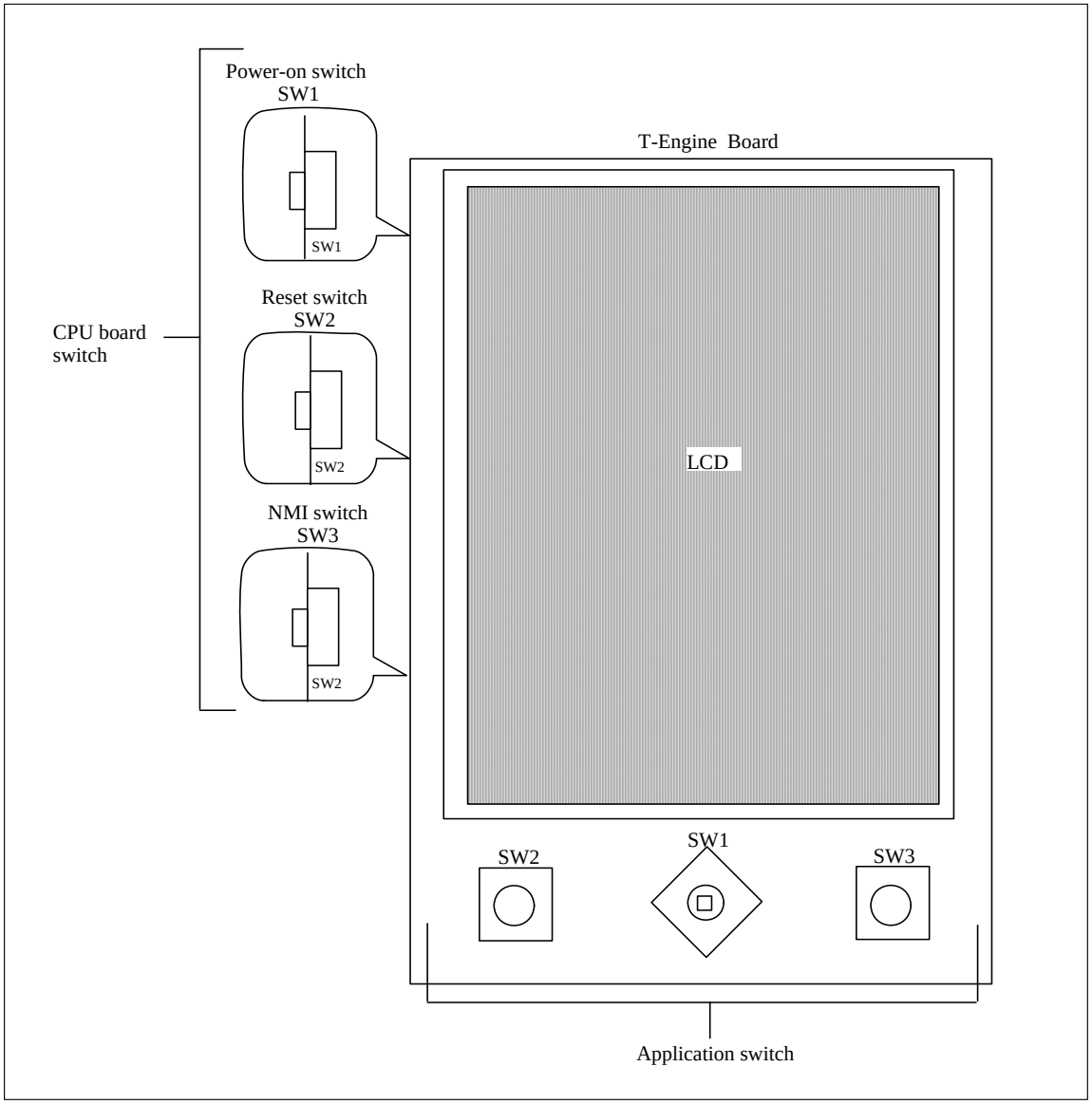


Figure 6.13 T-Engine Switch

6.5.1 CPU Board Switch Control

(1) Power-on switch (SW1)

- When T-Engine is OFF, it is turned ON if the power-on switch is pressed and held for 0.5 seconds or more.
- When T-Engine is ON, it is turned OFF if the power-on switch is pressed and held for 2 seconds or more.

(2) Reset switch (SW2)

T-Engine is turned OFF when the reset switch is pressed.

(3) NMI switch (SW3)

An NMI interrupt occurs for the SH7780 when the NMI switch is pressed.

6.5.2 LCD Board Switch Control (Application Switch)

(1) Cursor switch (SW1) and push-button switches (SW2 and SW3) on the LCD board

- The cursor switch and push-button switches are subject to sampling at intervals of 10msec. When consecutive three samplings indicate that the same key is being pressed, key bit pattern data of the cursor switch and push-button switches are output.
- If the switch is turned ON, a key ON interrupt occurs. If the switch is turned OFF, a key OFF interrupt occurs.
- When the same switch is pressed and held, an auto repeat interrupt occurs at intervals of 100 to 450msec (unit: 50msec).

6.5.3 Key Switch Registers

Table 6.5 summarizes the key switch registers. For details of each register, refer to 6.5.4 to 6.5.8.

Table 6.5 Key Switch Registers

Register	Abbreviation	Address	R/W	Size	Remarks
Key control register	KEYCR	0x0060	R/W	1 byte	
Key auto repeat time register	KATIMER	0x0061	R/W	1 byte	
Key bit pattern register	KBITPR	0x0064	R/W	2 bytes	
Key input status register	KEYSR	0x0062	R/W	1 byte	
RTC/Touch panel/key input/Power supply status register	RTKISR	0x0090	R/W	1 byte	

6.5.4 Key Control Register (KEYCR)

Address: 0x0060 Initial value: 0x20

D7	D6	D5	D4	D3	D2	D1	D0
0	0	NMIE	PONSWI	ARKEYI	KEY_OFFI	KEY_ONI	KEY_STR
R	R	R/W	R/W	R/W	R/W	R/W	R/W

(1) KEY_STR

KEY_STR bit	Setting
0	An application switch key input is disabled. (Initial value)
1	An application switch key input is enabled.

(2) KEY_ONI

KEY_ONI bit	Setting
0	An application switch ON interrupt is disabled. (Initial value)
1	An application switch key ON interrupt is enabled.

(3) KEY_OFFI

KEY_OFFI bit	Setting
0	An application switch OFF interrupt is disabled. (Initial value)
1	An application switch key OFF interrupt is enabled.

(4) ARKEYI

ARKEYI bit	Setting
0	An application switch auto repeat interrupt is disabled. (Initial value)
1	An application switch auto repeat interrupt is enabled.

(5) PONSWI

PONSWI bit	Setting
0	A power-on switch interrupt is disabled. (Initial value)
1	A power-on switch interrupt is enabled.

(6) NMIE

NMIE bit	Setting
0	An NMI interrupt is disabled for the SH7780 even when the NMI switch is pressed.
1	An NMI interrupt is disabled for the SH7780 when the NMI switch is pressed. (Initial value)

6.5.5 Key Auto Repeat Time Register (KATIMER)

Address: 0x0061 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
450msec	400msec	350msec	300msec	250msec	200msec	150msec	100msec
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register sets the auto repeat interrupt generation time. The auto repeat interrupt generation time is set at intervals of 100msec to 450msec (unit: 50msec). When one of the bits (100msec to 450msec) is set, the corresponding auto repeat interrupt generation time is set.

6.5.6 Key Bit Pattern Register (KBIPR)

Address: 0x0064 Initial value: 0x0000

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	SW3	0	SW2
R	R	R	R	R	R	R	R

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	SW1-5 (Decided)	SW1-4 (↓)	SW1-3 (↑)	SW1-2 (←)	SW1-1 (→)
R	R	R	R	R	R	R	R

This register stores the bit pattern of the application switch (SW1 to SW3) key input status.

(1) SWn

SWn bit	Setting
0	Application switch key input: OFF (Initial value)
1	Application switch key input: ON

6.5.7 Key Input Status Register (KEYSR)

Address: 0x0062 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	PONSWF	ARKEYF	KEY_OFFF	KEY_ONF	0
R	R	R	R/W	R/W	R/W	R/W	R

(1) KEY_ONF

KEY_ONF bit	Setting
0	An application switch key has not been turned on (Initial value)
1	An application switch key has been turned on. At this time, if the KEY_ONI bit is set to ‘‘1,’’ a key ON interrupt occurs. [Clear condition] “0’’ is written with the KEY_ONF bit set to ‘‘1.’’

(2) KEY_OFFF

KEY_OFFF bit	Setting
0	An application switch key is ON or OFF. (Initial value)
1	An application switch key has changed from ON to OFF. (Initial value) At time, if the KEY_OFFI bit is set to “1,’’ a key OFF interrupt occurs. [Clear condition] “0’’ is written with the KEY_OFFI bit set to ‘‘1.’’

(3) ARKEYF

ARKEYF bit	Setting
0	The same application switch key is not ON for the time specified in the key auto repeat time register (Initial value)
1	The same application switch key is not ON for the time specified in the key auto repeat time register. At this time, if the ARKEYI bit is set to ‘‘1,’’ repeat interrupt occurs. [Clear condition] ‘‘0’’ is written with the ARKEYF bit set to “1.’’

(4) PONSWF

PONSWF bit	Setting
0	The power-on switch has not been turned on for 2sec or more.
1	The power-on switch has been turned on for 2 sec or more. At this time, if the PONSWI bit is set to “1,” a power-on interrupt occurs. [Clear condition] “0” is written to the PONSWF bit set to “1.”

[Supplementary description on application switch key input]

(1) When multiple keys are pressed at the same time, the corresponding bits are all set to “1,” and a KEY_ONF interrupt occurs so long as it is enabled.

(2) If data in the key bit pattern register changes when multiple keys are pressed at the same time, a KEY_ONF interrupt occurs so long as it is enabled.

- Example -

This KEY_ONF interrupt occurs when the state with switches SW1 and SW2 pressed simultaneously changes to one with switches SW1 and SW3 pressed simultaneously.

(3) When multiple keys are released in the state with the keys pressed and held, a KEY_OFFI interrupt occurs so long as it is enabled.

(4) When multiple keys are released, the key states immediately before key release are retained in the key bit pattern register.

6.5.8 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits for key input.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) KEYIF

KEYIF bit	Setting
0	The PONSWF, ARKEYF, KEY_OFFF, and KEY_ONF bits of the key input status register are all set to “0.” (Initial value)
1	One of the PONSWF, ARKEYF, KEY_OFFF, or KEY_ONF bits of the key input status register is set to “1.” [Clear condition] “0” is written with the KEYIF bit set to “1.”

6.6 Power Supply Control

This section describes the power supply control functions. Table 6.6 summarizes the power supply control registers. In addition, refer to 6.6.1 to 6.6.3 for details of each register.

(1) T-Engine is turned ON or OFF.

(2) When T-Engine is OFF, it is turned ON if the power-on switch is pressed for 2 seconds or more.

(3) T-Engine can be turned OFF from the SH7780.

(4) If the DIP switch (SW7) is set to ON, T-Engine is also turned ON at the same time the power supply controller is turned ON.

Table 6.6 Power Control Registers

Register	Abbreviation	Address	R/W	Size	Remarks
System power control register 1	SPOWCR1	0x0070	R/W	1 byte	
System power control register 2	SPOWCR2	0x0071	R/W	1 byte	

6.6.1 System Power Control Register 1 (SPOWCR1)

Address: 0x0070 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	SPOWER
R	R	R	R	R	R	R	R/W

(1) SPOWER

SPOWER bit	Setting
0	System power supply: OFF
1	System power supply: ON (Initial value)

6.6.2 System Power Control Register 2 (SPOWCR2)

Address: 0x0071 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	SFPOWER
R	R	R	R	R	R	R	R/W

(1) SFPOWER

SFPOWER	Setting
0	T-Engine is turned OFF by SH7780 control.
1	T-Engine is turned OFF by pressing the power-on switch. (Initial value)

6.6.3 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits for power control.

Address: 0x0090 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) POWERIF

This bit will be functionally enhanced in the future. Don’t access this register. When read, this bit is always 0.”

6.7 LCD Front Light Control

This section describes the LCD light control functions. In addition, Table 6.7 summarizes the front light control registers.

(1) Controlling the ON/OFF state of the LCD front light

Table 6.7 LCD front light register

Register	Abbreviation	Address	R/W	Size	Remarks
LCD front light register	LCDR	0x00A1	R/W	1 byte	

6.7.1 LCD Front Light Register (LCDR)

Address: 0x00A1 Initial value: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	FRONTL
R	R	R	R	R	R	R	R/W

(1) FRONTL

FRONTL bit	Setting
0	The LCD front light is turned ON.
1	The LCD front light is turned OFF. (Initial value)

6.8 Reset Control

This section describes the reset control functions. Table 6.8 summarizes the reset control registers.

(1) T-Engine reset is controlled.

Table 6.8 Reset Registers

Register	Abbreviation	Address	R/W	Size	Remarks
Reset control register	RESTCR	0x00A2	R/W	1byte	

6.8.1 Reset Control Register (RESTCR)

Address: 0x00A2 Initial value: 0x02

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	SWRES	SORES
R	R	R	R	R	R	R/W	R/W

(1) SORES

SORES bit	Setting
0	T-Engine is not restarted by reset. (Initial value)
1	T-Engine is restarted by reset.

If this bit is set to “1,” T-Engine is restarted.

(2) SWRES

SWRES bit	Setting
0	Devices other than the power supply controller are reset with the reset switch (SW2).
1	All the devices covering the power supply controller are reset with the reset switch (SW2). (Initial value)

6.9 Infrared Remote Control

This section describes the infrared remote control functions. Table 6.9 summarizes the infrared remote control functions. For details of each register, refer to 6.9.1 to 6.9.8.

(1) Support of formats for two kinds of infrared remote control signal

- Supported format: NEC format and Home Appliance Manufacturer's Association format

(2) Function for receiving infrared remote control signals

- A maximum of 255 bytes of the infrared remote control signal can be stored. Receive data can be read from the receiving FIFO data register (IRRRFDR).
- Infrared remote control signals of a specified format can be received.
- When a frame signal has been received, a receiving interrupt may be generated.

(3) Function for transmitting infrared remote control signals

- A maximum of 255 bytes of the infrared remote control signal can be transmitted.
- Transmit data can be written to the transmitting FIFO data register (IRRSFDR).
- Infrared remote control signals of the specified format are transmitted.

Table 6.9 Infrared Remote Control Registers

Register	Abbreviation	Address	R/W	Size
Infrared remote control register	IRRCR	0x00B0	R/W	1 byte
Infrared remote status register	IRRSR	0x00B1	R/W	1 byte
Receive data count register for infrared remote control signals	IRRRDNR	0x00B2	R	1 byte
Transmit data count register for infrared remote control signals	IRRSDNR	0x00B3	R	1 byte
Receive FIFO data register for infrared remote control signals	IRRRFDR	0x00B4	R	1 byte
Transmit FIFO data register for infrared remote control signals	IRRSFDR	0x00B5	W	1 byte

6.9.1 Infrared Remote Control Register (IRRCR)

Address; 0x00B0 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	TDIE	RDIE	FORMAT	START
R	R	R	R	R/W	R/W	R/W	R/W

(1) START

START bit	Setting
0	ontrol is disabled. (Initial value)
1	Infrared remote control is enabled to start data transmission/reception.

(2) FORMAT

FORMAT bit	Setting
0	The NEC format is set. (Initial value)
1	The Home Appliance Manufacturer's Association format is set.

(3) RDIE

RDIE bit	Setting
0	An interrupt is disabled upon completion of receiving a frame of infrared remote control signal. (Initial value)
1	An interrupt is enabled upon completion of receiving a frame of infrared remote control signal.

(4) TDIE

TDIE bit	Setting
0	An interrupt is disabled upon completion of transmitting a frame of infrared remote control signal. (Initial value)
1	An interrupt is enabled upon completion of transmitting a frame of infrared remote control signal.

6.9.2 Infrared Remote Control Status Register (IRRSR)

Address: 0x00B1 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	TDI	RDI	0	RDBFER
R	R	R	R	R/W	R/W	R	R/W

(1) RDBFER

RDBFER bit	Setting
0	A buffer full error has not occurred during a receive operation. (Initial value)
1	A buffer full error has occurred during a receive operation.

(2) RDI

RDI bit	Setting
0	A frame of data has not been received. (Initial value)
1	A frame of data has been received. [Clear condition] “0” is written with the RDI bit set to “1.”

(3) TDI

TDI bit	Setting
0	A frame of data has not been transmitted. (Initial value)
1	A frame of data has been transmitted. [Clear condition] “0” is written with the TDI bit set to “1.”

6.9.3 Receive Data Count Register for Infrared Remote Control Signals (IRRRDNR)

Address: 0x00B2 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRRD_D7	IRRRD_D6	IRRRD_D5	IRRRD_D4	IRRRD_D3	IRRRD_D2	IRRRD_D1	IRRRD_D0
R	R	R	R	R	R	R	R

This register indicates the number of received data items (infrared remote control signals) stored in the receive FIFO register. When this register is “0x00,” it indicates that there is no data. When the value of this register is “0xFF,” it indicates that the receive FIFO register is full of data.

6.9.4 Transmit Data Count Register for Infrared Remote Control Signals (IRRSDNR)

Address: 0x00B3 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRSD_D7	IRRSD_D6	IRRSD_D5	IRRSD_D4	IRRSD_D3	IRRSD_D2	IRRSD_D1	IRRSD_D0
R	R	R	R	R	R	R	R

This register indicates the number of data items not transmitted (infrared remote control signals) stored in the transmit FIFO register. When the value of this register is “0x00,” it indicates that there is no data. When the value of this register is “0xFF,” it indicates that the transmit FIFO buffer is full of data.

6.9.5 Receive FIFO Data Register for Infrared Remote Control Signals (IRRRFDR)

Address: 0x00B4 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRRDR_D7	IRRRDR_D6	IRRRDR_D5	IRRRDR_D4	IRRRDR_D3	IRRRDR_D2	IRRRDR_D1	IRRRDR_D0
R	R	R	R	R	R	R	R

This register is an 8-bit FIFO register for storing received data. All the received data can be obtained from this register until it is emptied. For details, refer to 6.10.8, “Infrared Remote Control Data Structure.”

6.9.6 Transmit FIFO Data Register for Infrared Remote Control Signals (IRRSFDR)

Address: 0x00B5 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
IRRSDR_D7	IRRSDR_D6	IRRSDR_D5	IRRSDR_D4	IRRSDR_D3	IRRSDR_D2	IRRSDR_D1	IRRSDR_D0
W	W	W	W	W	W	W	W

This register is an 8-bit FIFO register that stores transmission data. Transmission data can be stored until this register is filled with data. For details, refer to 6.10.8, “Infrared Remote Control Data Structure.”

6.9.7 RTC/Touch Panel/Key Input/Power Supply Status Register (RTKISR)

This status register indicates the RTC, touch panel, or key input status. Below is a brief description of the status bits for infrared remote control signals.

Address: 0x0090 Initial value: 0x00

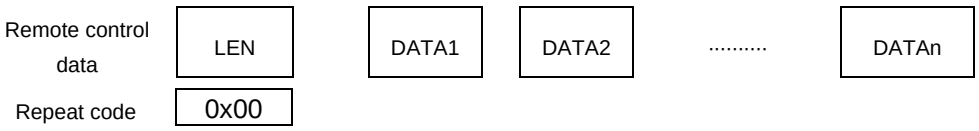
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	IRRIF	POWERIF	KEYIF	TPIF	RTCIF
R	R	R	R/W	R/W	R/W	R/W	R/W

(1) IRRIF

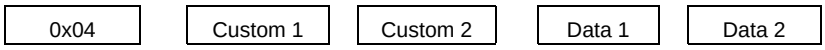
IRRIF bit	Setting
0	A frame of data has not been transmitted or received. (Initial value)
1	A frame of data has been transmitted or received. [Clear condition] "0" is written with the IRRIF bit set to "1."

6.9.8 Infrared Remote Control Data Structure

The following shows the relation between the infrared remote control data and repeat codes. In addition, it shows a structure of remote control data in the NEC format.



Example) NEC format remote control data



[Infrared Remote Control Operation Procedure]

[Initial setting]

(1) Two kinds of formats are set by selecting the FORMAT bit of the IRRCR register.
(2) The START bit of the IRRCR register is set to "1" to start infrared remote control and infrared signal reception
(3) To enable an interrupt at the time of receiving a frame of the signal, the RDIE bit is set to "1."
(4) To enable an interrupt at the time of transmitting a frame of the signal, the TDIE bit is set to "1."

[For infrared signal reception]

(1) When a frame of data has been received (RDI=1), the IRRIF bit of the RTKISR register is set to "1."
(2) When an interrupt at completion of signal reception has been enabled (RDIE=1), an interrupt occurs when a frame of data is stored in the IRRRFDE register.
(3) To obtain the received data, the receiving FIFO data register (IRRRFDR) is read. The IRRRFDR register contains a data count (that indicates the number of items of one frame of data received) and the received data itself. If this register is read, the data count and data itself are output in this order.
(4) The size of received data is set in the received data count register (IRRRDNR). When two frames have been received, the total data count and the two frames of data are set in the received data count register (IRRRDNR).

[For infrared signal transmission]

(1) When transmission data is transmitted, it is written to the transmitting FIFO data register. The data count for one frame of transmission data and the data itself are written to this data register. In addition, this transmission data count is not counted as transmission data.
(2) The count for data not transmitted is set in the transmission data count register (IRRSDNR).
(3) Data can be written to the transmission data IRRSFDR until the count for data not transmitted (IRRSDNR) reaches 255.
(4) When a frame of data has been transmitted (TDI=1), the IRRIF bit of the RTKISR register is set to “1.” An interrupt for transmission completion occurs so long as it is enabled.

⚠ CAUTION

- To change the type of format, the FORMAT value of the same register must be set before the START bit of the IRRCR register is set to “1.”
- When the START bit of the IRRCR register is “0,” transmission/reception is not guaranteed.
- When the specified size is larger than the IRRRDNR value during a read operation, “FF” is set for excessive read data.
- Only the custom code and data code are specified for transmission data, and the leader, stop bit, frame space, and trailer are automatically added.
- When the number of write data items is larger than that of the remaining transmission data (255–byte transmission data count register IRRSDNR), a data length error occurs.
- When the IRRRFDR register has become full during a read operation, the buffer full error bit is set to “1,” and the data received later is discarded.
- The IRRIF bit of the RTKISR register is cleared when “0” is written with the IRRIF bit set to “1.”

6.10 Serial EEPROM Control

This section describes the EEPROM control functions. Table 6.10 summarizes the serial EEPROM control registers. For details of each register, refer to 6.10.1 to 6.10.3.

(1) Serial EEPROM (128 bytes) can be read and written.

Table 6.10 Serial EEPROM Control Registers

Register	Abbreviation	Address	R/W	Size
EEPROM control register	EEPCR	0x00C0	R/W	1 byte
EEPROM data register	EEPDR	0x0100~0x02FF	R/W	1 byte x 128

6.10.1 EEPROM Control Register (EEPCR)

Address: 0x00C0 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	START
R	R	R	R	R	R	R	R/W

(1) START

START bit	Setting
0	The serial EEPROM is disabled. (Initial value)
1	The serial EEPROM is enabled.

6.10.2 EEPROM Data Register (EEPDR)

Address: 0x0100 to 0x017F Initial value: Not defined

D7	D6	D5	D4	D3	D2	D1	D0
EEPDR_D7	EEPDR_D6	EEPDR_D5	EEPDR_D4	EEPDR_D3	EEPDR_D2	EEPDR_D1	EEPDR_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register consists of 512 8-bit data in the above format.

EEPDR address	
0x0100	8 bit
0x0101	8 bit
	-
	-
	-
0x02FE	8 bit
0x02FF	8 bit

An EEPROM address corresponds to an EEPDR address. When a read/write operation is performed on the EEPROM, the EEPDR address must be specified for the operation.

6.10.3 Serial EEPROM Operation Procedure

[Initial Setting]

(1) The START bit of the EEPCR register is set to “1.”

[For a read/write operation to the serial EEPROM]

(1) An EEPDR address corresponding to an EEPROM address must be specified for a read/write operation.

⚠ CAUTION

When the START bit of the EEPCR register is “0,” read/write data is not guaranteed.

6.11 Electronic Volume Control

This section describes the electronic volume control functions. Table 6.11 summarizes the electronic volume control registers. For details of each register, refer to 6.11.1 and 6.11.2.

(1) An electronic volume value can be set.

An electronic volume value can be set within a range from 0x00 (minimum sound volume) to 0xFF (maximum sound volume).

(2) Two electronic volume values can be set.

An electronic volume value can be set for the right or left speaker.

Table 6.11 Electronic Volume Control Registers

Register	Abbreviation	Address	R/W	Size
Electronic volume data register for the right speaker	EVRDR	0x00D0	R/W	1 byte
Electronic volume data resister for the left speaker	EVLDR	0x00D1	R/W	1 byte

6.11.1 Electronic Volume Data Register for the Right Speaker (EVRDR)

Address: 0x00D0 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
EVRDR_D7	EVRDR_D6	EVRDR_D5	EVRDR_D4	EVRDR_D3	EVRDR_D2	EVRDR_D1	EVRDR_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Values from 0x00 to 0xFF can be set.

6.11.2 Electronic Volume Data Register for the Left Speaker (EVLDR)

Address: 0x00D1 Initial value: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
EVLRD_D7	EVLRD_D6	EVLDR_D5	EVLDR_D4	EVLDR_D3	EVLDR_D2	EVLDR_D1	EVLDR_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Values from 0x00 to 0xFF can be set.

6.12 LED Control

This section describes the LED control functions. Table 6.12 summarizes the LED control register.

Controlling the ON/OFF State of LEDs (LED1 to LED8) on the CPU board

Table 6.12 LED control register

Register	Abbreviation	Address	R/W	Size	Remarks
LED register	LEDR	0x00A0	R/W	1 byte	

6.12.1 LED Register (LEDR)

Address: 0x00A0 Initial value: 0xXX

D7	D6	D5	D4	D3	D2	D1	D0
LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEDn

LEDn	Setting
0	LEDn is turned OFF.
1	LEDn is turned ON.

6.13 Power Supply Controller Initial Values

The register values for the power supply controller vary depending on the following conditions. Under condition A, all the power supply controller registers are initialized. The initial value of each register is given in the description of each register in this manual.

For register values under conditions A to D, refer to the following table of RTC registers.

[Condition]

Condition A: The power is turned ON.

The hard reset switch (SW4) is pressed.

Condition B: The power is turned ON.

The RESTCR SORES bit has been set to “1.”

The RESTCR SWRES bit has been set to “1,” and the reset switch (SW2) has been pressed.

Condition C: The RESTCR SWES bit has been cleared to zero and the reset switch (SW2) has been pressed.

Condition D: The SPOWCR1 SPOWER bit has been set to “0.”

Table 6.13 Values under RTC Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
RTC control register	RTCCR	Initial value	Initial value	Hold	Initial value
RTC status register	RTCSR	Initial value	Hold	Hold	Hold
Second counter	SECCNT	Initial value	Operation	Operation	Operation
Minute counter	MINCNT	Initial value	Operation	Operation	Operation
Hour counter	HRCNT	Initial value	Operation	Operation	Operation
Day-of-the-week counter	WKCNT	Initial value	Operation	Operation	Operation
Day counter	DAYCNT	Initial value	Operation	Operation	Operation
Month counter	MONCNT	Initial value	Operation	Operation	Operation
Year counter	YRCNT	Initial value	Operation	Operation	Operation
Second alarm counter	SECAR	Initial value	Hold	Hold	Hold
Minute alarm counter	MINAR	Initial value	Hold	Hold	Hold
Hour alarm counter	HRAR	Initial value	Hold	Hold	Hold
Day-of-the-week alarm counter	WKAR	Initial value	Hold	Hold	Hold
Day alarm counter	DAYAR	Initial value	Hold	Hold	Hold
Month alarm counter	MONAR	Initial value	Hold	Hold	Hold
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Figure 6.14 Values under Touch Panel Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Touch panel control register	TPLCR	Initial value	Initial value	Hold	Initial value
Touch panel status register	TPLSR	Initial value	Initial value	Hold	Initial value
Touch panel sampling control register	TPLSCR	Initial value	Initial value	Hold	Initial value
X position A/D register	XPAR	Initial value	Initial value	Hold	Initial value
Y position A/D register	YPAR	Initial value	Initial value	Hold	Initial value
X position dot register	XPDR	Initial value	Initial value	Hold	Initial value
Y position dot register	YPDR	Initial value	Initial value	Hold	Initial value
XA position dot register	XAPDR	Initial value	Hold	Hold	Hold
YA position dot register	YAPDR	Initial value	Hold	Hold	Hold
XB position dot register	XBPDR	Initial value	Hold	Hold	Hold
YB position dot register	YBPDR	Initial value	Hold	Hold	Hold
XC position dot register	XCPDR	Initial value	Hold	Hold	Hold
YC position dot register	YCPDR	Initial value	Hold	Hold	Hold
XA position A/D register	XAPAR	Initial value	Hold	Hold	Hold
YA position A/D register	YAPAR	Initial value	Hold	Hold	Hold
XB position A/D register	XBPAR	Initial value	Hold	Hold	Hold
YB position A/D register	YBPAR	Initial value	Hold	Hold	Hold
XC position A/D register	XCPAR	Initial value	Hold	Hold	Hold
YC position A/D register	YCPAR	Initial value	Hold	Hold	Hold
DX dot register	DXDR	Initial value	Hold	Hold	Hold
DY dot register	DYDR	Initial value	Hold	Hold	Hold
X position dot calculation A/D value	XPARDOT	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 1	XPARDOT1	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 2	XPARDOT2	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 3	XPARDOT3	Initial value	Hold	Hold	Hold
X position dot calculation A/D value 4	XPARDOT4	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value	YPARDOT	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 1	YPARDOT1	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 2	YPARDOT2	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 3	YPARDOT3	Initial value	Hold	Hold	Hold
Y position dot calculation A/D value 4	YPARDOT4	Initial value	Hold	Hold	Hold
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Table 6.15 Values under Switch Input Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Key control register	KEYCR	Initial value	Initial value	Hold	Initial value
Key auto repeat time register	KATIMER	Initial value	Initial value	Hold	Initial value
Key input status register	KEYSR	Initial value	Initial value	Hold	Initial value
Key bit pattern register	KBITPR	Initial value	Initial value	Hold	Initial value
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Table 6.16 Values under Power Supply Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
System power control register 1	SPOWCR1	Initial value	Initial value	Hold	0x00
System power snort register 2	SPOWCR2	Initial value	Initial value	Hold	Initial value
RTC/Touch Panel/Key Input/Power Supply status register	RTKISR	Initial value	Initial value	Hold	Initial value

Table 6.17 Values under LED Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
LED register	LEDR	Initial value	Initial value	Hold	0x00

Table 6.18 Values under LCD Front Light Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
LCD front light register	LCDR	Initial value	Initial value	Hold	0x00

Table 6.19 Values under Reset Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Reset control register	RESTCR	Initial value	Initial value	Hold	Initial value

Table 6.20 Values under Infrared Remote Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Infrared remote control register	IRRCR	Initial value	Initial value	Hold	Initial value
Infrared remote control status register	IRRSR	Initial value	Initial value	Hold	Initial value
Receive data count register for infrared remote control signals	IRRRDNR	Initial value	Initial value	Hold	Initial value
Transmit data count register for infrared remote control signals	IRRSDNR	Initial value	Initial value	Hold	Initial value
Receiving FIFO data register for infrared remote control signals	IRRRFDR	Initial value	Initial value	Hold	Initial value
Transmitting FIFO data register for infrared remote control signals	IRRSFDR	Initial value	Initial value	Hold	Initial value

Table 6.21 Values under Serial EEPROM Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
EEPROM control register	EEPCR	Initial value	Initial value	Hold	Initial value
EEPROM status register	EEPSR	Initial value	Initial value	Hold	Initial value
EEPROM data register	EEPDR	Initial value	Initial value	Hold	Initial value

Table 6.22 Values under Electronic Volume Control Register Conditions

Register	Abbreviation	Condition A	Condition B	Condition C	Condition D
Electronic volume data register for the right speaker	EVRDR	Initial value	Initial value	Hold	Initial value
Electronic volume data register from the left speaker	EVLDR	Initial value	Initial value	Hold	Initial value

7. External Interrupts

7.1 SH7780 External Interrupts

Figure 7.1 shows a mechanism for the SH7780 interrupt signal.

Table 7.1 shows the levels for respective interrupt signals.

As shown in Figure 7.1, interrupt signals from each device on the T-Engine board are converted by the PLD before being output to IRL[3:0] of the SH7780. Note, however, that interrupt signals from the USB Host controller, PCMCIA controller, and mobile multimedia controller that are connected via PCI are output to PCI_INT[A,B,C].

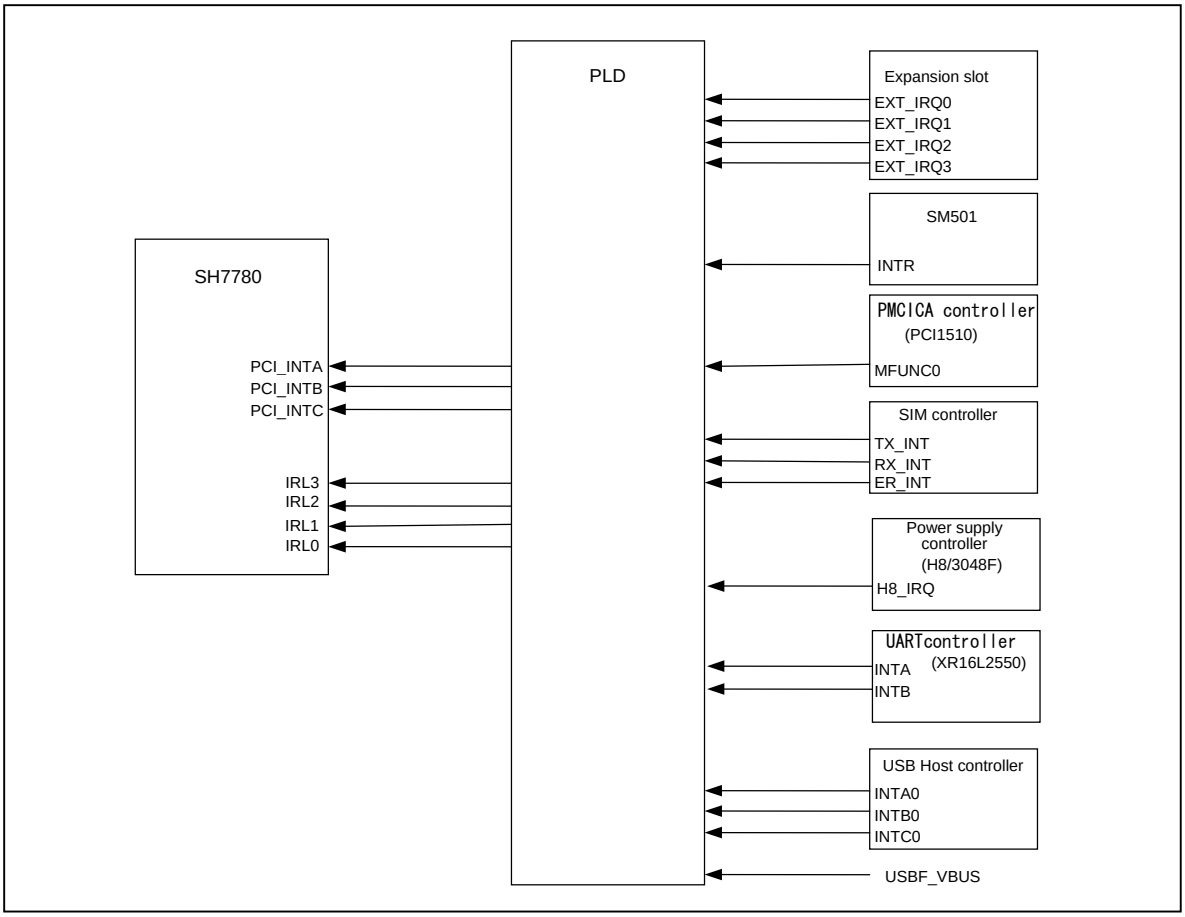


Figure 7.1 Interrupt Signal Mechanism

Table 7.1 Interrupt Levels for Interrupt Signals

No.	Interrupt request source	Signal name	/IRL[3:0]	Interrupt signal level	Remarks
1	Expansion slot/IRQ3	/EX_IRQ[3]	0001	14	Active Low
2	SIM error interrupt	/SIMER_INT	0010	13	
3	UART controller chA	UART_INTA	0011	12	Contact with H8/3048
4	H8/3048F-ONE	/H8_IRQ	0100	11	
5	Expansion slot /IRQ2	/EX_IRQ[2]	0101	10	Active Low
6	PCMCIA controller	/PCM_INT	0110	9	Output PCI_INT(A,B,C)
7	UART controller chB	UART_INTB	0111	8	Contact with T-Monitor
8	Mobile Multimedia controller	/MMCC_INT	1000	7	Output PCI_INT(A,B,C)
9	Expansion slot /IRQ1	/EX_IRQ[1]	1001	6	
10	SIM transmission Interrupt	/SIMTX_INT	1010	5	
11	SIM reception Interrupt	/SIMRX_INT	1011	4	
12	USB-Function	VBUS	1100	3	
13	Expansion slot /IRQ0	/EX_IRQ[0]	1101	2	Active Low
14	USB-Host	/USBH_INT	1110	1	Output PCI_INT(A,B,C)

*1: Be sure the interrupts from expansion slots are input as active low.

The PLD internally contains a register to indicate the status of interrupts from peripheral devices and a register to mask the PCI and IRL interrupts. The internal registers of the PLD are described below.

Register name : Interrupt status register (INTSTR)
Address : H'B9000002

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	SIMERINTS	SIMRXINTS	SIMTXINTS	-	USBHINTS	PCICINTS	MMCCINTS	EX3INTS	EX2INTS	EX1INTS	EX0INTS	USBFINTS	H8INTS	URTBINTS	URTAINTS
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit15,11 : Reserved
When read, these bits read as 0.
Writing data to these bits has no effect.

bit14 : SIM error interrupt status(SIMERINTS)
0: Error interrupt from the SIM controller was not detected. (Initial value)
1: Error interrupt from the SIM controller was detected.
The interrupt source must be cleared by the SIM controller.

bit13 : SIM reception interrupt atatus (SIMRXINTS)
0: Reception interrupt from the SIM controller was not detected. (Initial value)
1: Reception interrupt from the SIM controller was detected.
The interrupt source must be cleared by the SIM controller.

bit12 : SIM transmission interrupt status(SIMTXINTS)
0: Transmission interrupt from the SIM controller was not detected. (Initial value)
1: Transmission interrupt from the SIM controller was detected.
The interrupt source must be cleared by the SIM controller.

bit10 : USB host interrupt status (USBHINTS)
0: Interrupt from the USB host controller was not detected. (Initial value)
1: Interrupt from the USB host controller was detected.
The interrupt source must be cleared by the USB host controller.

bit9 : PCMCIA interrupt status (PCICINTS)
0: Interrupt from the PCMCIA controller was not detected. (Initial value)
1: Interrupt from the PCMCIA controller was detected.
The interrupt source must be cleared by the PCMCIA controller.

bit8 : MMCC interrupt status (MMCCINTS)
0: Interrupt from the graphic controller was not detected. (Initial value)
1: Interrupt from the graphic controller was detected.
The interrupt source must be cleared by the graphic controller.

bit7 : Expansion bus interrupt3 status(EX3INTS)
0: Interrupt 3 from the expansion bus was not detected. (Initial value)
1: Interrupt 3 from the expansion bus was detected.
The interrupt source must be cleared by the expansion board.

bit6 : Expansion bus interrupt2 status (EX2INTS)
0: Interrupt 2 from the expansion bus was not detected. (Initial value)
1: Interrupt 2 from the expansion bus was detected.
The interrupt source must be cleared by the expansion board.

bit5 : Expansion bus interrupt1 status (EX1INTS)
0: Interrupt 1 from the expansion bus was not detected. (Initial value)
1: Interrupt 1 from the expansion bus was detected.
The interrupt source must be cleared by the expansion board.

bit4 : Expansion bus interrupt0 status (EX0INTS)
0: Interrupt 0 from the expansion bus was not detected. (Initial value)
1: Interrupt 0 from the expansion bus was detected.
The interrupt source must be cleared by the expansion board.

bit3 : USB function interrupt status (USBFINTS)
0: USB host OCRNT interrupt was not detected. (Initial value)
1: USB host OCRNT interrupt was detected.
The interrupt source must be cleared by the USB control register (USBCR).

bit2 : H8 interrupt status (H8INTS)
0: Interrupt from the H8 was not detected. (Initial value)
1: Interrupt from the H8 was detected.
The interrupt source must be cleared by the H8.

bit1 : UARTB interrupt status (URTBINTS)

0: Interrupt from the UART channel B was not detected. (Initial value)

1: Interrupt from the UART channel B was detected.

The interrupt source must be cleared by the UART.

bit0 : UARTA interrupt status (URTAINTS)

0: Interrupt from the UART channel A was not detected. (Initial value)

1: Interrupt from the UART channel A was detected.

The interrupt source must be cleared by the UART.

Register name : PCI interrupt set register (PINTR)

Address : H'B9000004

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	USBH INTM	PCIC INTM	MMCC INTM	-	-	-	-	-	PCII SEL2	PCII SEL1	PCII SEL0
initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

bit15～bit11,bit7～bit3 : Reserved

When read, these bits read as 0.

Writing data to these bits has no effect.

bit10 : USB host controller interrupt mask (USBHINTM)

0: PCI interrupts of the USB host controller are not masked. (Initial value)

1: PCI interrupts of the USB host controller are masked.

bit9 : PCMCIA interrupt mask (PCICINTM)

0: PCI interrupts of the PCMCIA controller are not masked. (Initial value)

1: PCI interrupts of the PCMCIA controller are masked.

bit8 : Graphic controller interrupt mask (MMCCINTM)

0: PCI interrupts of the graphic controller are not masked. (Initial value)

1: PCI interrupts of the graphic controller are masked.

bit2～bit0 : PCI interrupt selection (PCIISEL)

These bits assign interrupts to INTA/B/C as shown below.

3'b000 : /INTA=PCMCIA , /INTB=MMCC , /INTC=USBH (Initial value)

3'b001 : /INTA=PCMCIA , /INTC=MMCC , /INTB=USBH

3'b010 : /INTB=PCMCIA , /INTA=MMCC , /INTC=USBH

3'b011 : /INTB=PCMCIA , /INTC=MMCC , /INTA=USBH

3'b100 : /INTC=PCMCIA , /INTA=MMCC , /INTB=USBH

3'b101 : /INTC=PCMCIA , /INTB=MMCC , /INTA=USBH

Others : Interrupts are not output to INTA/B/C.

Register name : IRL mask register0(IRLMR)
Address : H'B9000006

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	SIMERINTM	SIMRXINTM	SIMTXINTM	-	USBHINTM	PCICINTM	MMCCINTM	EX3INTM	EX2INTM	EX1INTM	EX0INTM	USBFINTM	H8INTM	URTBINTM	URTAINTM
Initial value	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: If an interrupt from any device is generated while interrupts are masked by setting this register, the interrupt is not notified to the SH7780, but the status of that interrupt is flagged in the interrupt status register.

bit15,bit11 : Reserved
When read, these bits read as 0.
Writing data to these bits has no effect.

bt14 : SIM module error interrupt mask set（SIMERINTM）
0: Error interrupts from the SIM controller are not masked.
1: Error interrupts from the SIM controller are masked. (Initial value)

bit13 : SIM reception interrupt mask set (SIMRXINTM)
0: Reception interrupts from the SIM controller are not masked.
1: Reception interrupts from the SIM controller are masked. (Initial value)

bit12 : SIM transmission interrupt mask set (SIMTXINTM)
0: Transmission interrupts from the SIM controller are not masked.
1: Transmission interrupts from the SIM controller are masked. (Initial value)

bit10 : USB host interrupt mask set (USBHINTM)
0: Interrupts from the USB host controller are not masked.
1: Interrupts from the USB host controller are masked. (Initial value)

bit9 : PCMCIA interrupt mask set (PCICINTM)
0: Interrupts from the PCMCIA controller are not masked.
1: Interrupts from the PCMCIA controller are masked. (Initial value)

bit8 : MMCC interrupt mask set (MMCCINTM)
0: Interrupts from the graphic controller are not masked.
1: Interrupts from the graphic controller are masked. (Initial value)

bit7 : Expansion bus interrupt3 mask set (EX3INTM)
0: Interrupt 3 from the expansion bus is not masked.
1: Interrupt 3 from the expansion bus is masked. (Initial value)

bit6 : Expansion bus interrupt2 mask set (EX2INTM)
0: Interrupt 2 from the expansion bus is not masked.
1: Interrupt 2 from the expansion bus is masked. (Initial value)

bit5 : Expansion bus interrupt1 mask set (EX1INTM)

0: Interrupt 1 from the expansion bus is not masked.

1: Interrupt 1 from the expansion bus is masked. (Initial value)

bit4 : Expansion bus interrupt0 mask set (EX0INTM)

0: Interrupt 0 from the expansion bus is not masked.

1: Interrupt 0 from the expansion bus is masked. (Initial value)

bit3 : USB function interrupt mask set (USBFINTM)

0: USB host OCRNT interrupt is not masked.

1: USB host OCRNT interrupt is masked. (Initial value)

bit2 : H8 interrupt mask set (H8INTM)

0: Interrupts from the H8 are not masked.

1: Interrupts from the H8 are masked. (Initial value)

bit1 : UARTB interrupt mask set (URTBINTM)

0: Interrupts from the UART channel B are not masked.

1: Interrupts from the UART channel B are masked. (Initial value)

bit0 : UARTA interrupt mask set (URTAINTM)

0: Interrupts from the UART channel A are not masked.

1: Interrupts from the UART channel A are masked. (Initial value)

8. T-Engine Expansion Slot

8.1 Expansion Slot Specifications

Connector number: CN2

T-Engine connector model: 24-5603-14-0401-861 (Kyocera Elco)

Adaptable connector model: 14-5603-14-0401-861 (Kyocera Elco)

Figure 8.1 shows the location of an expansion slot.

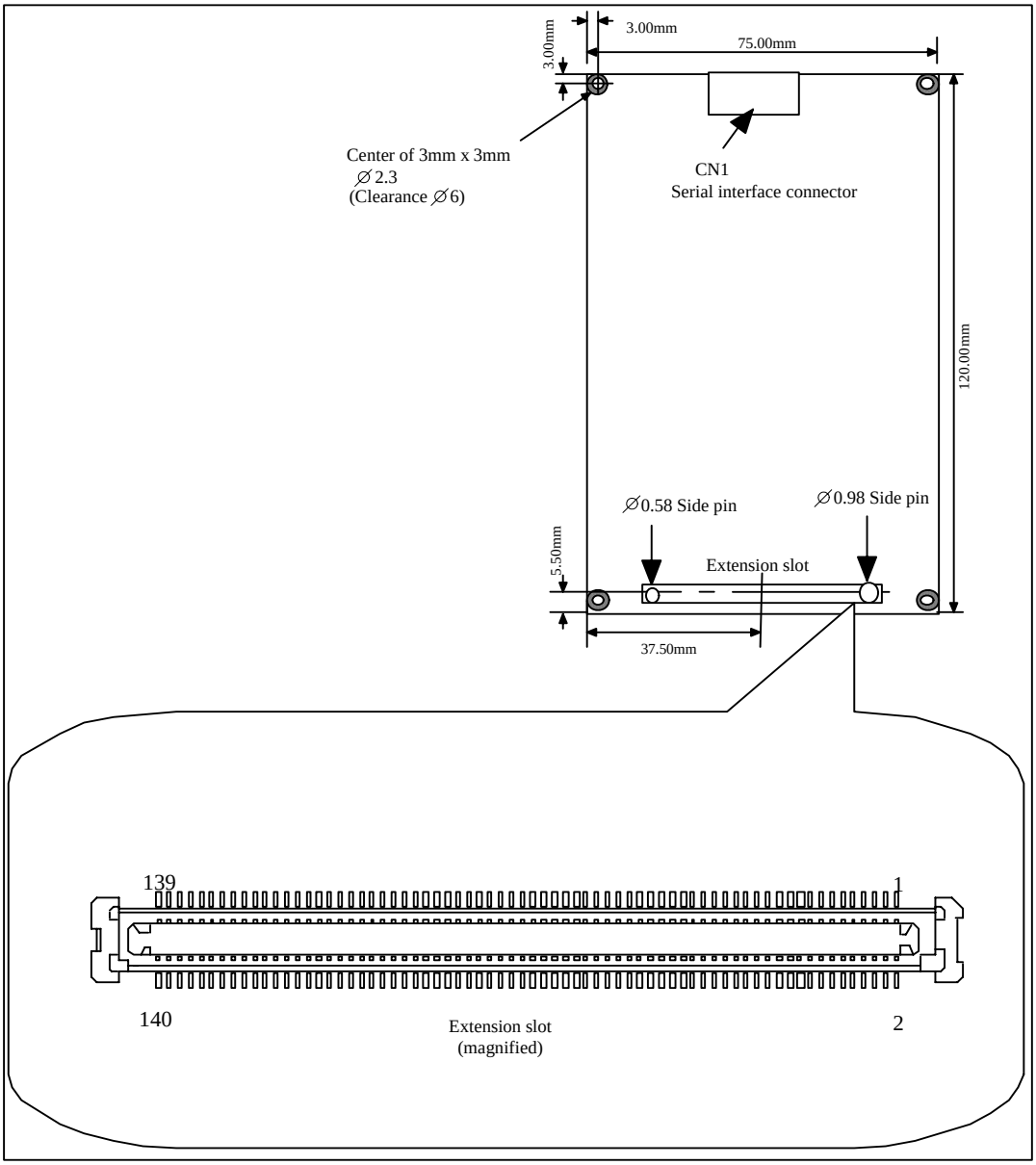


Figure 8.1 Expansion Slot Position

8.2 Expansion Slot Signal Assignment

Table 8.1 shows the assignment of expansion slot signals.

Table 8.1 Expansion Slot Signals

Pin No.	Signal name	I/O	Pin No.	Signal name	I/O	Pin No.	Signal name	I/O	Pin No.	Signal name	I/O
1	5.0V	–	36	D29	I/O	71	A24	O	106	/CTS	I
2	5.0V	–	37	D30	I/O	72	A25	O	107	–	–
3	5.0V	–	38	D31	I/O	73	/EPROMCE	O	108	ASEMD0	I
4	5.0V	–	39	GND	–	74	/CS2	O	109	GND	–
5	D0	I/O	40	GND	–	75	/CS4	O	110	GND	–
6	D1	I/O	41	CKIO	O	76	/CS5	O	111	TCK	I
7	D2	I/O	42	GND	–	77	RDWR	O	112	TMS	I
8	D3	I/O	43	GND	–	78	/BS	O	113	/TRST	I
9	D4	I/O	44	GND	–	79	GND	–	114	TDI	I
10	D5	I/O	45	A0	O	80	GND	–	115	TDO	O
11	D6	I/O	46	A1	O	81	/RD	O	116	/ASEBRKAK	O
12	D7	I/O	47	A2	O	82	/WAIT	I	117	3.3VSB	–
13	D8	I/O	48	A3	O	83	/WE0	O	118	3.3VSB	–
14	D9	I/O	49	A4	O	84	/WE1	O	119	3.3VSB	–
15	D10	I/O	50	A5	O	85	/WE2	O	120	3.3VSB	–
16	D11	I/O	51	A6	O	86	/WE3	O	121	AUDATA0	I/O
17	D12	I/O	52	A7	O	87	GND	–	122	AUDATA1	I/O
18	D13	I/O	53	A8	O	88	GND	–	123	AUDATA2	I/O
19	D14	I/O	54	A9	O	89	/IRQ0	I	124	AUDATA3	I/O
20	D15	I/O	55	A10	O	90	/IRQ1	I	125	/AUDSYNC	O
21	GND	–	56	A11	O	91	/IRQ2	I	126	AUDCK	I
22	GND	–	57	A12	O	92	/IRQ3	I	127	3.3V	–
23	D16	I/O	58	A13	O	93	NMI_IN	I	128	3.3V	–
24	D17	I/O	59	A14	O	94	/RST_IN	I	129	3.3V	–
25	D18	I/O	60	A15	O	95	/RST_OUT	O	130	3.3V	–
26	D19	I/O	61	GND	–	96	/DREQ	I	131	3.3V	–
27	D20	I/O	62	GND	–	97	/DRAK	O	132	3.3V	–
28	D21	I/O	63	A16	O	98	/DACK	O	133	VBAT_IN	–
29	D22	I/O	64	A17	O	99	ROMSEL	I	134	VBAT_IN	–
30	D23	I/O	65	A18	O	100	/BASE	I	135	VBAT_IN	–
31	D24	I/O	66	A19	O	101	GND	–	136	VBAT_IN	–
32	D25	I/O	67	A20	O	102	GND	–	137	GND	–
33	D26	I/O	68	A21	O	103	TxD	O	138	GND	–
34	D27	I/O	69	A22	O	104	RxD	I	139	GND	–
35	D28	I/O	70	A23	O	105	/RTS	O	140	GND	–

⚠ CAUTION

- The VBAT pin may be used to supply the power for the T-Engine board via an expansion slot. Be sure the power supply voltage applied to the board is in the range 5.0 V to 5.6 V.
- The /CS2 pin has /CS1 of the SH7780 output from it.
- The /BASE pin, when pulled low on the expansion board side, directs outputs of the SH7780 expansion bus to expansion slots.
- The 3.3VSB pin supplies 3.3 V (typ) power whenever an AC adapter is connected.

8.3 Extension Slot AC Timing

As shown in Figure 8.2, the SH7780 bus signals are routed through the bus buffer (PLD) when they are output to the expansion slot.

Furthermore, the operating clock frequency (CKIO) of the expansion bus can be set to 1/2 by setting SW6 to the ON position. In this case, wait states can be automatically inserted in bus cycles by setting SW7. For details on how to set these switches, refer to Section 3.1, “CPU Board Switches.”

Figures 8.3 and 8.4 show the AC timing of the expansion slot in cases when SW6 is set to the OFF position (normal mode) and set to the ON position (low speed mode), respectively.

For details about the bus timing of the SH7780, refer to the SH7780 hardware manual.

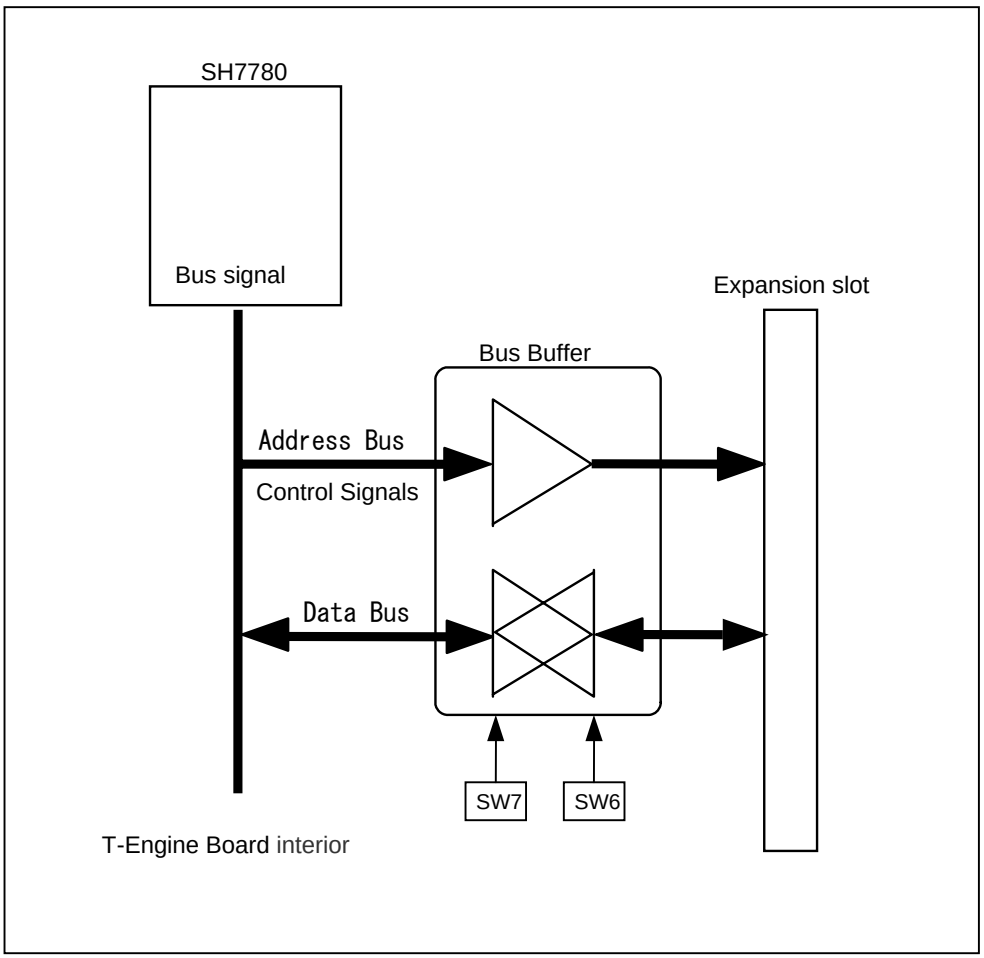


Figure8.2 Extension Slot Bus Buffer Structure

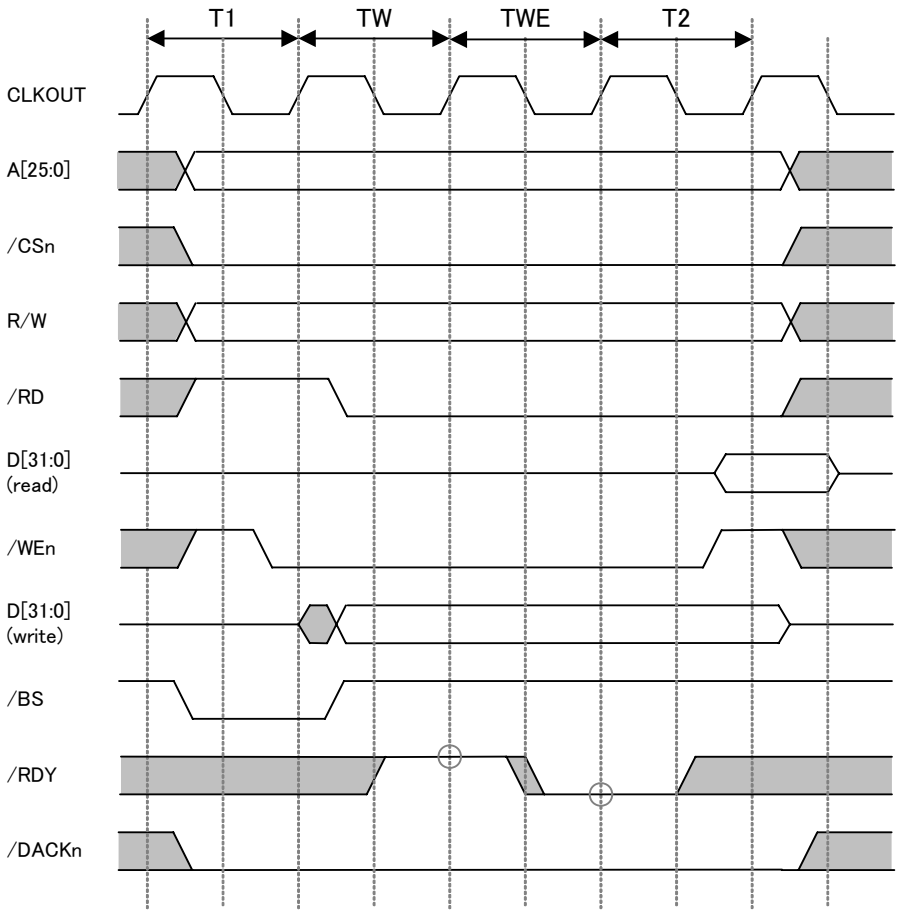


Figure8.3 SH7780 base AC timing (SW6:OFF(at Normal mode))

図8.4

9. Flash Memory Refresh

When refreshing the contents of the flash memory on T-Engine or the internal flash memory of the power supply controller (H8/3048F-ONE), connect the debug board to the expansion slot of T-Engine and run the program stored in the EPROM on the debug board.

9.1 Preparation for Flash Memory Refresh

Connect the debug board to the expansion slot (CN2) of T-Engine. In addition, make the following settings for the jumper switch.

For details, refer to 2.4.2 “Debug Board Connection” and 2.4.3 “Debug Board Jumper switch.”

Debug board jumper switch (J1): Pins 1 and 2 must be short-circuited (EPROM allocation to an address range from h’00000000 to h’0001FFFF).

Connect the serial interface connector (CN1) of T-Engine and the host system with an RS-232C interface cable (accessory). Start communication software on the host system and make the following settings.

Baud rate: 115200bps
Data length: 8 bits
Parity bit: None
Stop bit: 1 bit
Flow control: Xon/Xoff

After making the above settings, turn on the power of T-Engine, and the title screen --- screen indicating the execution status of the program stored in the EPROM --- will be displayed on the communication software as shown below.

[Display Screen]

```
================================================

        T-Engine (MS7780CP01) DownLoader VerX.XL

------------------------------------------------------------------------------
================================================

                        H[elp] for help messages...
Ready>
```

9.2 T-Engine Flash Memory

9.2.1 Refresh Method

Figure 9.1 shows how the T-Engine flash memory is refreshed. As shown in Figure 9.1, the T-Engine flash memory is refreshed in such a way that flash memory data is copied to DD-SDRAM and the data transferred from the host system is written to the flash memory.

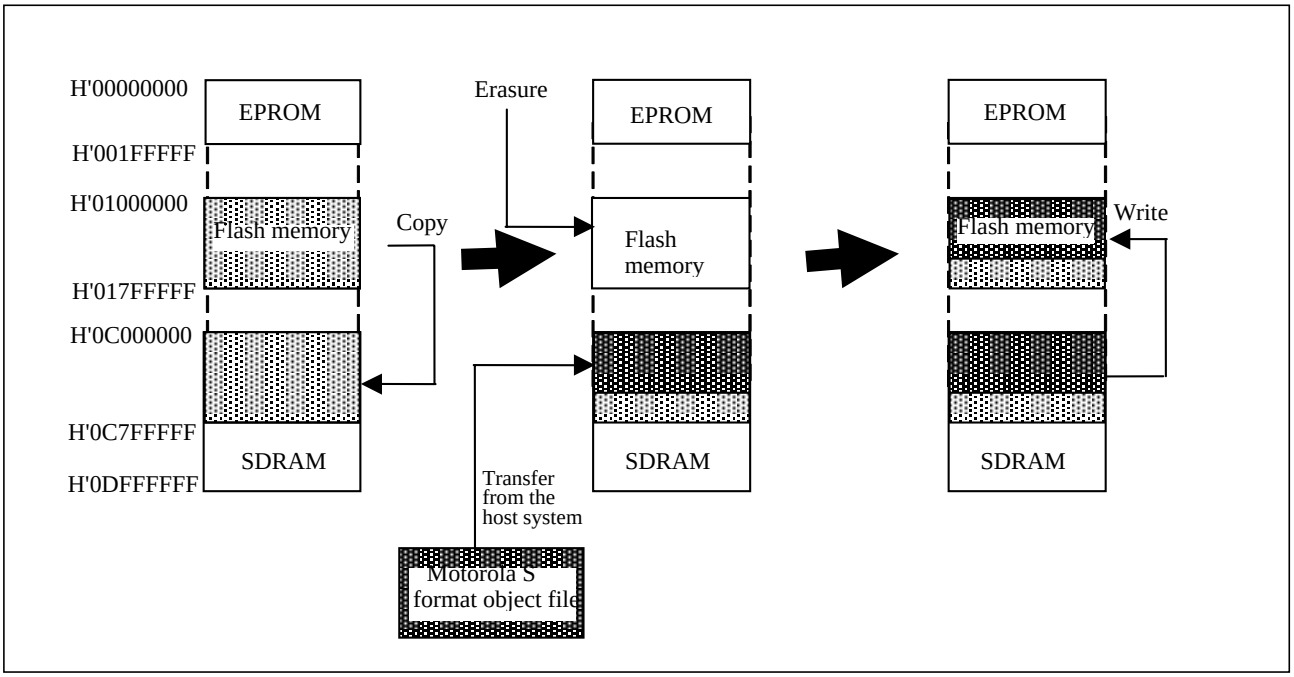


Figure 9.1 Flash Memory Refresh

Below is a description of the T-Engine flash memory refresh method.

(1) As shown on the following screen, type “FL 0” and hit the Enter key after the title screen appears on the communication software.

[Display Screen]

```
================================================

        T-Engine(MS7780CP01) DownLoader VerX.XL

------------------------------------------------------------------------------
================================================
                    H[elp] for help messages...
Ready>fl 0
```

(2) As shown on the following screen, transfer the Motorola S format object file after the transfer request message “Please Send A S-format Record” appears on the screen.

[Display Screen]

```
Ready>fl 0

SH7780 Flash Memory Change Value!
Flash Memory data copy to RAM
Please Send A S-format Record
```

(3) Flash memory refresh normally terminates when the messages (“flash memory chip erase: complete” and “flash write complete”) sequentially appear on the screen after the Motorola S format object file has been transferred.

[Display Screen]

```
Ready>fl 0

SH7780 Flash Memory Change Value!
Flash Memory data copy to RAM
Please Send A S-format Record

Start Addrs = 00000000
End Addrs = 000104D7

Transfer complete
flash chip erase: complete
flash chip erase verified: .....complete
Program :complete
flash write data verified: .....complete
Flash write complete
Ready>
```

9.3 Power Supply Controller's Internal Flash Memory

9.3.1 Refresh Method

Figure 9.2 shows how the flash memory of the power supply controller is refreshed. As shown in Figure 9.2, data transferred from the host system is saved in the SDRAM when power supply controller's flash memory is refreshed. The saved data is transferred to the power supply controller and written to the flash memory by the power supply controller firmware. Though the flash memory of the power supply controller has been divided into 8 blocks, the upper 4 blocks are occupied by the firmware for refreshing the flash memory and only the remaining 4 blocks (BLK4 to BLK7) are rewritten.

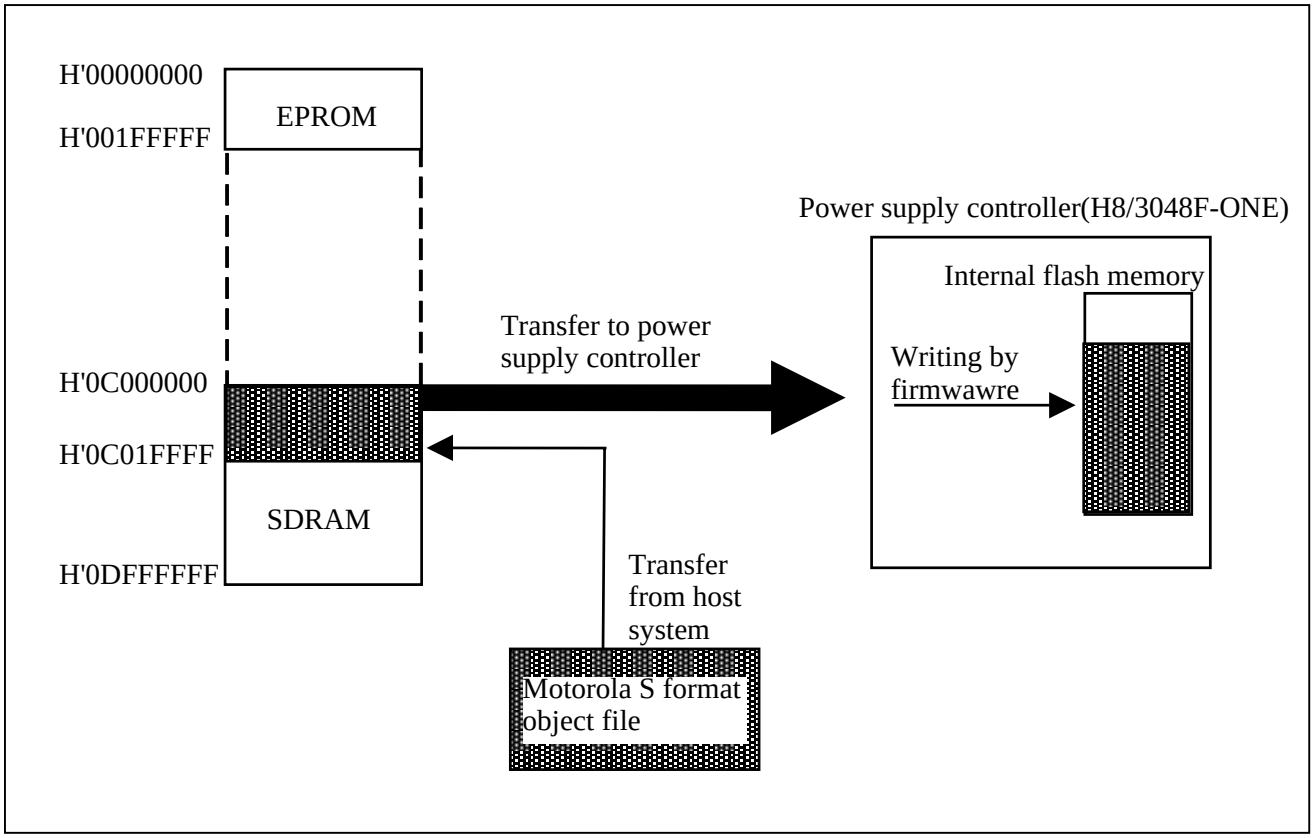


Figure 9.2 Refreshing the Flash Memory of the Power Supply Controller

Below is a description of the method for refreshing the flash memory of the power supply controller.

(1) As shown on the following screen, type “FL 1” and hit the Enter key after the title screen appears on the communication software.

[Display Screen]

```
================================================

        T-Engine (MS7780CP01) DownLoader VerX.XL

------------------------------------------------------------------------------------------
================================================

                        H[elp] for help messages...
Ready>fl 1
```

(2) As shown on the following screen, transfer the Motorola S format object file after the transfer request message “Please Send A S-format Record” appears on the screen.

⚠ CAUTION

After data is transferred, its program ID is checked to determine whether the transferred data is correct. When the program ID is not correct, the message “Wrong Data!!” appears and memory refresh terminates.

[Display Screen]

```
Ready>fl 1

H8/3048Fone Flash Memory Change Value!
Clear data buffer (all 0xFF)
Please Send A S-format Record
```

(3) Refreshing the flash memory of the power supply controller normally completes when the messages (“H8 flash erase: complete” and “flash write complete”) sequentially appear on the screen after the Motorola S format object file has been transferred.

⚠ CAUTION

When the flash memory of the power supply controller is being refreshed, never power OFF T-Engine. If ignored, refreshing may terminate in error or the flash memory may be damaged.

[Display Screen]

```
Ready>fl 1
H8/3048Fone Flash Memory Change Value!
Clear data buffer (all 0xFF)
Please Send A S-format Record
Start Addrs = 00001000
End Addrs = 00003D20
Transfer complete
H8 Flash erase: complete
Program :…… complete
Flash write complete
Ready>
```

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