RH4Z2501-PMOD

HW revision 1.1

This document explains the hardware design of the RH4Z2501-PMOD, its main features and the necessary hardware setup to implement an IO-Link device.

Target device: RH4Z2501 single channel IO-Link physical layer transceiver with integrated protection

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1. Overview

1.1 RH4Z2501 Features

The RH4Z2501-PMOD is a PMOD module for the RH4Z2501 Renesas silicon solution. The purpose of the module is to be used with a standard MCU evaluation board with a PMOD interface to implement an IO-Link Device.

The RH4Z2501 offers the following features:

- Voltage range from 9V to 36V
- Over voltage peak robustness of ±60V
- Configurable driver output current 50mA DC to 600mA DC
- R$_{DSON}$ of less than 2.5Ω
- Adjustable driver slew rate
- Integrated wake-up detection
- MCU assisted Wake-up generation (typically 600mA)
- OWI digital communication and calibration interface
- Integrated linear voltage regulators: 3.3V and 5V
- Ambient temperature range -40°C to 125°C
- Glitch filter for receiver
- Integrated Protection
  - ±1.25kV/2.5A (peak) surge protection for VDD, CQ, GND (8/20 µs pulse according to IEC 61000-4-5)
- Reverse polarity protection for L+, CQ, GND/L-
- On-chip diagnostics:
  - Over-temperature detection
  - Supply voltage monitor
  - Broken chip detection

For more information, refer to the *RH4Z2501 Datasheet* document.

1.2 RH4Z2501-PMOD Capabilities

The RH4Z2501-PMOD integrates an IO-Link PHY to equipe MCU Evaluation Boards containing PMOD with the IO-Link interface.
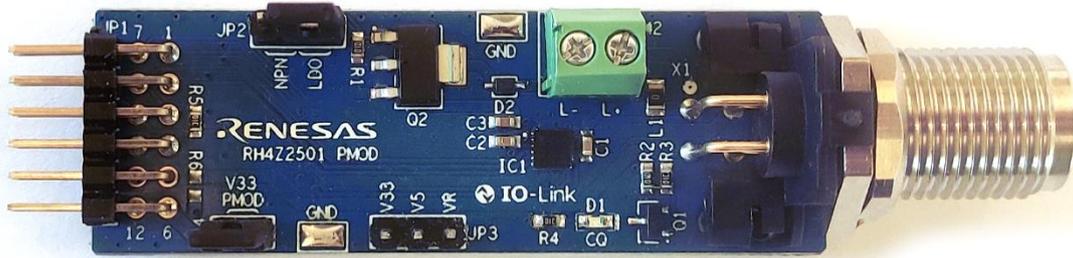
Figure 1. RH4Z2501-PMOD (Default Jumper Setting)

Note: Do NOT adjust any jumper settings on the RH4Z2501-PMOD during powered operation!

2. Getting Started

2.1 System Block Diagram

Figure 2 shows the system overview for the RH4Z2501-PMOD.
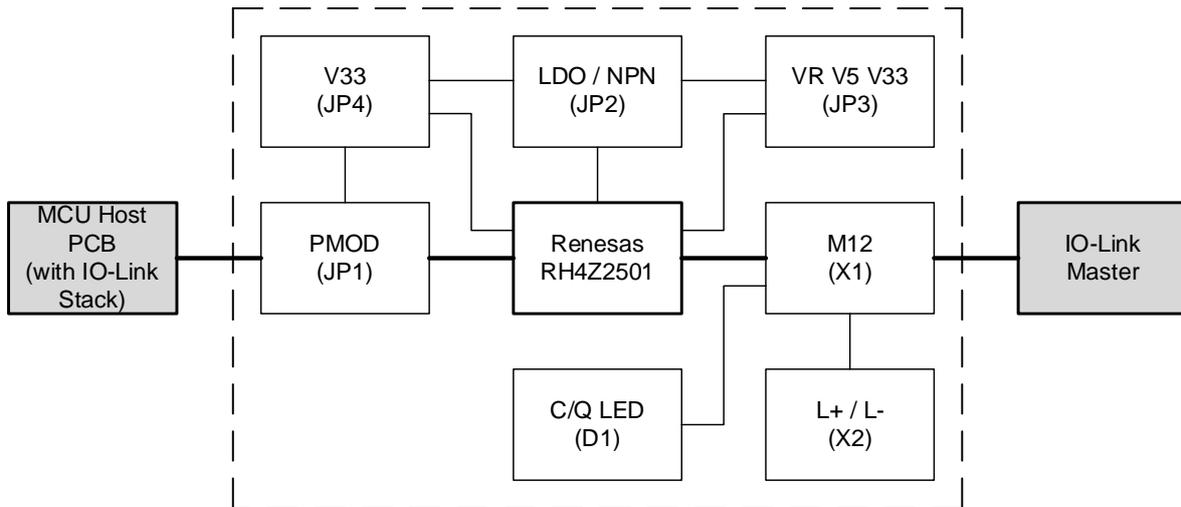
Figure 2. System Block Diagram

2.2 Default Board Configuration

Table 1 lists the default configuration for the RH4Z2501-PMOD.

Table 1. Default Board Configuration

Jumper/Switch	Default Position
JP2	LDO
JP3	Open
JP4	Closed

3. RH4Z2501-PMOD Components

3.1 X1: M12 Connector

X1 is a male 4-pin M12-A-coded connector. It enables an easy connection between the RH4Z2501-PMOD and an IO-Link Master. IO-Link is a serial, bidirectional point-to-point connection for signal transmission and power supply to sensors and actuators. The RH4Z2501-PMOD features a 4 pin Class A device port with the pin assignment as in Figure 3 and Table 2. For usage of Pin 2, populate R6 with a 0 Ohm resistor.

Table 2. X1: Pin Assignment

Pin	Signal	Designation
1	L+	Power Supply (+), 24V
2	I/Q	NC/DI(OSSDe)/DO/ AI/AO, Routed to pin 8 of JP1
3	L-	Power Supply (-), 0V / GND
4	C/Q	SIO(OSSDe)/SDCI, SIO (DI/DO) or SDCI (IO-Link coded data)
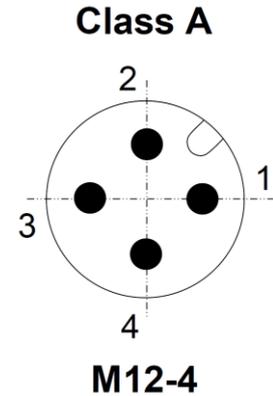
Figure 3. X1: Pin Numbering (Front View)

3.2 X2: Block Terminal

X2 offers direct access to L+ and L- from the M12 connector.

3.3 JP1: PMOD Connector

The RH4Z2501-PMOD is connected to Host MCU PCB (with IO-Link device stack) via JP1 carrying a PMOD interface.

Table 3. JP1: Pin Assignment

Pin	Function
1	OWI/DIAG
2	TxD
3	RxD
4	NC
5	GND
6	3V3
7	/WU
8	I/Q (connected to X1 pin 2)
9	TxEN
10	NC
11	GND
12	3V3
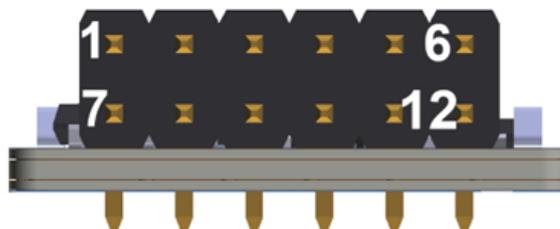
Figure 4. JP1: Pin Numbering (Front View)

3.4 JP2: Voltage Regulation Options (Onboard)

The RH4Z2501-PMOD enables the following methods to regulate the voltage supplied from the IO-Link Master:

▪ Set jumper to position LDO to use the internal LDO to regulate the voltage (maximum 50mA).

▪ Set jumper to position NPN to use the external NPN transistor (Q2) to regulate the voltage. The heat from voltage drop between 24V and 5V is generated in the external transistor and not in the RH4Z2501 IC. Current is limited by maximum supply current from Master and PCB thermal limits.

3.5 JP3: Voltage Regulation Options (External)

All voltage regulation pins are accessible on JP3 to implement external power options, for example, an external transistor or DC-DC converter. For more information, refer to the *RH4Z2501 Datasheet* document.

3.6 JP4: 3.3V PMOD Interface

When JP4 is closed, 3.3V power supply on PMOD interface is enabled (maximum 50mA if internal LDO is used).

3.7 D1: C/Q-LED

The RH4Z2501-PMOD has an LED that indicates the status of the C/Q line (IO-Link communication status). Its signal is regulated by NPN transistor Q1 and its voltage divider.

4. Glossary

Term	Description
C/Q	C/Q line of IO-Link interface. Connection for communication (C) or switching (Q) signal.
DC	Direct Current
DC-DC	Direct Current - Direct Current
GND	Ground
IC	Integrated Circuit
IO	Input Output
LDO	Low Drop Out
LED	Light Emitting Diode
MCU	Microcontroller
NPN	Negative-Positive-Negative
OWI	One Wire Interface
PCB	Printed Circuit Board
PHY	Physical Layer
PMOD	Digilent Pmod™ Connector

5. Revision History

Revision	Date	Description
1.0	Apr.15.24	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,

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