User Manual

32

RH850 Evaluation Platform

RH850/E2x-468BGA PiggyBack board T1

Y-RH850-E2X-468PIN-PB-T1-V1

Renesas Electronics
www.renesas.com

R20UT4287ED0100, Rev. 1.0
2018-03-12

Table of Contents

Chapter 1 Introduction

The RH850/E2x Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/E2x microcontrollers in a BGA-468 package. The PiggyBack board (Y-RH850-E2X-468PIN-PB-T1-V1) can be used as a standalone board, or can be mated with a mainboard (Y-RH850-X1X-MB-Tx-Vx) for extended functionality.

Main features:

- Socket for mounting of device
- Standalone operation of the board
- Direct supply of device voltage (typ. 5V, 3.3V and 1.09V) as well as the generation of the core voltage (typ. 1.09V) from an on-board voltage regulator
- Device programming capability
- Device debugging capability
- Pin headers for direct access to the functional device pins
- Reset switch
- MainOSC circuitry
- Connectors to Mainboard
- Operating temperature from 0°C to +40°C

This document describes the functionality provided by the PiggyBack board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the corresponding User's Manual.

Chapter 2 Overview

2.1 Overview of Y-RH850-E2X-468PIN-PB-T1-V1

Figures 1 and 2 provide a schematic view of the Y-RH850-E2X-468PIN-PB-T1-V1 PiggyBack board.

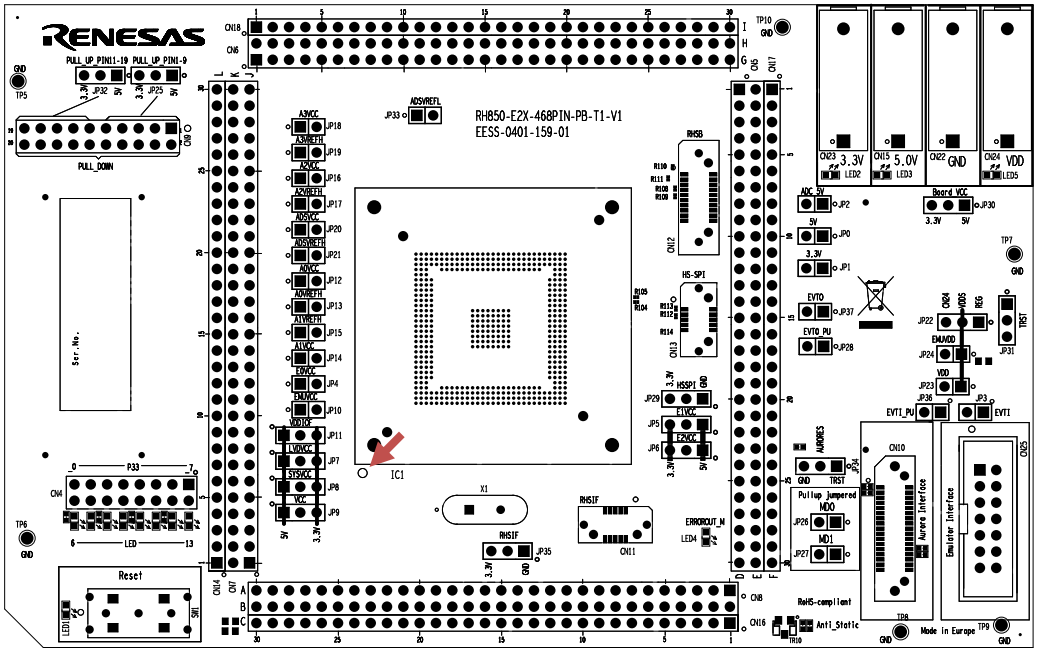


Figure 1 PiggyBack Board Top View

The red arrow denotes the position of socket pin #1.

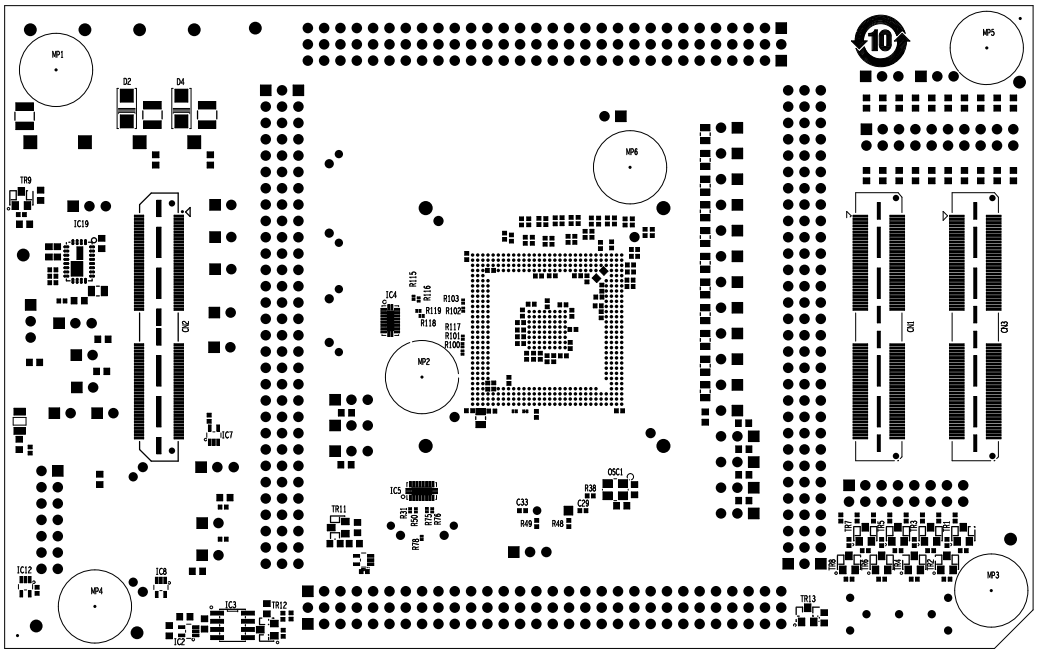


Figure 2 PiggyBack Board Bottom View

2.2 Mounting of the Device

The Y-RH850-E2X-468PIN-PB-T1-V1 PiggyBack board features a socket for mounting of the device. All E2x in BGA-468 package do fit into the available Enplas OTB-468(961RS)-0.8-048S-00 socket:

- RH850/E2H
- RH850/E2UH
- RH850/E2x-FCC2 for E2H
- RH850/E2x-FCC2 for E2UH

The device must be placed inside the socket IC1. To insert the device align the device package #1pin with the #1pin of the socket. The #1pin of the socket is marked with a circle near to the “IC1” label (see also red arrow in **Figure 1**). The #1pin of the device is marked by a white triangle on the package (see white circle in **Figure 3**).

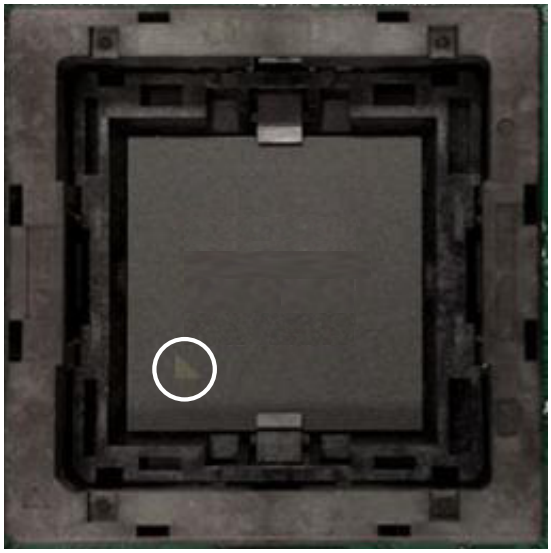


Figure 3 Enplas OTP-468(961RS)-0.8-048S-00 Socket with Mounted Device

CAUTION: *Please be careful with the placement to not damage the device.*

Chapter 3 Power Supply

3.1 Board Power Connection

For operation of the device, a supply voltage must be connected to the board. There are several possibilities to power the device.

Within this document the following voltages are considered as 'typical' values:

Voltage1 = 5V

Voltage2 = 3.3V

Voltage3 = 1.09V

Direct voltage supply

Three different voltages can be supplied to the board.

The following connectors are available to supply those voltages directly:

- Four 4mm 'banana-type' connectors:
  - Three red connectors for voltages 5V (CN15), 3.3V (CN23) and 1.09V (CN24).
  - A black connector for ground (GND) connection (CN22).
  Note: The four connectors are supplied with the board but not assembled.

For details about voltage distribution, refer to **Chapter 3.2 'Voltage Distribution'**.

Supply by Mainboard

In case the PiggyBack board is mounted on a Mainboard, the 5V and 3.3V is supplied by the on-board regulators of the Mainboard.

CAUTION: *Do not supply 5V or 3.3V directly to the PiggyBack board in case it is mounted on the Mainboard.*

For each of the voltages, 5V, 3.3V and 1.09V a green LED (LED3, LED2 and LED5, respectively) is available to signal that the related voltage is available on the PiggyBack board. The corresponding LEDs are placed directly beneath the connectors of the related voltage.

3.2 Voltage Distribution

The table shows the required device power supply pins. For detailed explanation of their function and specification, please refer to the user documentation of the corresponding device:

Table 1 Available Power Domains for MCU

Device Supply Pin
SYSVCC
VCC
EnVCC (n = 0-2)
LVDVCC
EMUVCC
AnVCC (n = 0-3)
AnVREFH (n = 0-3)
ADSVCC
ADSVREFH
EMUVDD
VDD

Additional power supply for the Mainboard and the operation of the PiggyBack board can be selected:

Table 2 Available Power Domains for Board Operation

Supply voltage	Function
VDDIOF	IO supply voltage for components located on a connected mainboard.
Board_VCC	Source for all devices (e.g. voltage regulator) on the PiggyBack board

The following figure shows the configurable voltage distribution on the PiggyBack board.

- Jumpers can interrupt all power supply lines. This provides the possibility to measure the current consumption of each individual power domain of the device (JP4 – 10, JP12 – 21 and JP23 – 24).
- The IO supply voltage for the Mainboard (VDDIOF) can be connected via jumper JP11 to 5V or 3.3V, if the PiggyBack board is mounted on a Mainboard.
- VDD and EMUVDD can be powered either directly from the ‘banana-type’ connector (CN24) or by an on-board voltage regulator.
- The source for the on-board voltage regulator, as well as the source for all on-board devices (Board_VCC) needs to be configured via jumper JP30 to either 5V or 3.3V.
- The source for VDD is selectable by the jumper JP22. The jumper JP23 and JP24 connect the voltage, configured by JP22 with the VDD and EMUVDD pins.

Note: Although typically 1.09V is specified as the input voltage to VDD and EMUDVV the output of the voltage regulator IC19 is slightly increased to 1.12V (see **Chapter 11 'Schematic'**). With this sufficient high voltage is applied, even in case of any possible voltage drops.

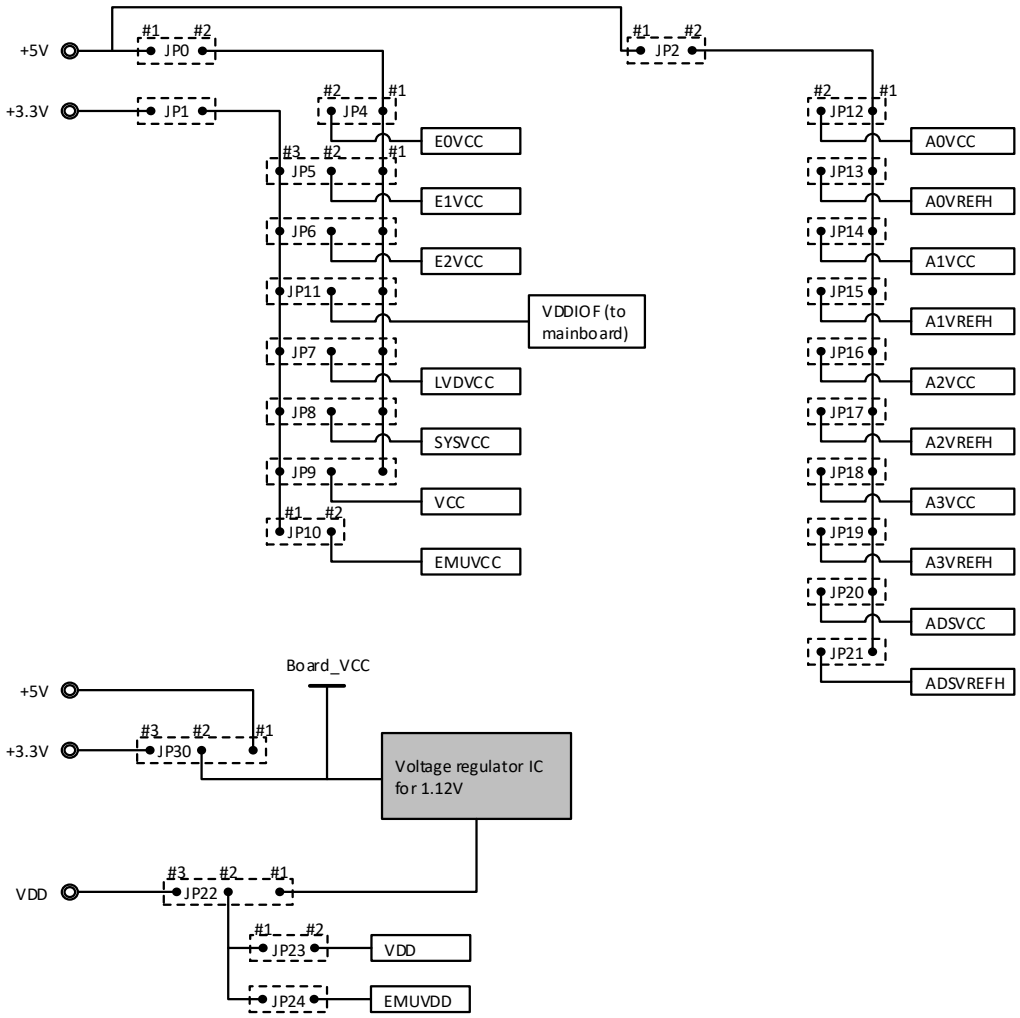


Figure 4 Voltage Distribution on the PiggyBack Board

For more details, please refer to **Chapter 11 'Schematic'**. For typical configuration of the jumpers, please refer to **Chapter 8 'Jumper Configuration'**.

Chapter 4 Clock Sources

External crystal oscillators for the device clock supply are provided with the board.

4.1.1 MainOSC

A crystal or ceramic resonator can be mounted on socket X1.

A 20 MHz and 40MHz oscillator are supplied with the board.

The signals X1 and X2 are by default not connected to a pin header in order to minimize disturbance on the resonator signal. If needed the signals can be connected to CN8 (pins #29 and 30) via connecting with 0Ohm resistances R48 and R49. For details, please refer to **Chapter 11 'Schematic'**.

4.1.2 Programmable Oscillator

It is possible to mount a programmable crystal oscillator on the PiggyBack board at OSC1. The available footprint and circuitry is designed for a SG-8002CE programmable crystal oscillator from Epson Toyocom. The output from this oscillator can be connected to port X1 via resistor R38. The SG-8002CE is neither mounted nor provided with the board. For details about the available circuitry, refer to **Chapter 11 'Schematic'**. A resonator mounted on socket X1 must not be used in parallel to another clock source.

Chapter 5 Debug and Programming Interface

The signal ‘EVTO’ from below connectors can be pulled up to ‘E0VCC’ via JP28. Please refer to the documentation of the used tool, whether this is needed.

The signal ‘TRST’ from below connectors can be pulled up to ‘SYSVCC’ or to the ‘TRST’ line of the used tool via jumper JP31.

For typical configuration of the jumpers, please refer to **Chapter 8 ‘Jumper Configuration’**.

5.1 14 Pin Debug Connector

For connection of the microcontroller to debug and flash programming tools, the connector CN25 with fourteen pins is available.

The signal connection of the connector CN25 is shown in the table below:

Table 3 Pin Assignment of CN25

CN25 Pin	Function
1	TCK
2	GND
3	JP31 #3 (TRST)*1)
4	MD0
5	TDO
6	-
7	TDI
8	VCC
9	TMS
10	EVTO (P33_9)*2)
11	DRDY
12	GND
13	RES_IN
14	GND

Note 1): For connecting CN25 pin #3 with the TRST pin of the MCU JP31 pins #2 and #3 needs to be closed.

Note 2): For connecting CN25 pin #10 with the pin P33_9 of the MCU JP37 needs to be closed. Please note that additionally P33_9 port function needs to be assigned to EVTO.

For more details, please refer to **Chapter 11 ‘Schematic’**. For typical configuration of the jumpers, please refer to **Chapter 8 ‘Jumper Configuration’**.

5.2 34 Pin Aurora Connector

For connection of the microcontroller to a trace tool CN10 is available.

The signal connection of the connector CN10 is shown in the table below:

Table 4 Pin Assignment of CN10

CN10 Pin	Function		CN10 Pin	Function
1	TODP0		2	VCC
3	TODN0		4	TCK
5	GND		6	TMS
7	Reserved (NC)		8	TDI
9	Reserved (NC)		10	TDO
11	GND		12	TRST
13	Reserved (NC)		14	MD0
15	Reserved (NC)		16	EVTI (P33_8)*1)
17	GND		18	EVTO (P33_9)*2)
19	Reserved (NC)		20	MD1
21	Reserved (NC)		22	RES_IN
23	GND		24	GND
25	Reserved (NC)		26	CICREFP
27	WDTDIS (NC)		28	CICREFN
29	GND		30	GND
31	ETK-BREQ (NC)		32	DRDY
33	ETK-BGNT (NC)		34	RES_OUT

Note 1): For connecting CN10 pin #16 with the pin P33_8 of the MCU JP3 needs to be closed. Please note that additionally P33_8 port function needs to be assigned to EVTI.

Note 2): For connecting CN10 pin #18 with the pin P33_9 of the MCU JP37 needs to be closed. Please note that additionally P33_9 port function needs to be assigned to EVTO.

Access to the signal AURORES is possible via JP34. With this jumper AURORES can also be connected to TRST or pulled-down to GND

For more details, please refer to **Chapter 11 'Schematic'**. For typical configuration of the jumpers, please refer to **Chapter 8 'Jumper Configuration'**.

Chapter 6 Connectors for Ports of Device

6.1 Pin Header for Device Pins

Connection to most functional pins of the devices is possible via the connectors CN5 to CN8, CN14 and CN16 to CN18.
Some functions might not be available on the pin headers, e.g. high frequency signals, as this would disturb the integrity of such signals. The actual voltage levels of the various voltage domains can be measured at the individual jumpers. For more details, please refer to **sec. 3.2 'Voltage Distribution'** and **Chapter 11 'Schematic'.**

CAUTION: *The pin headers are directly connected to the pins of the device, therefore special care must be taken to avoid any electrostatic or other damage to the device.*

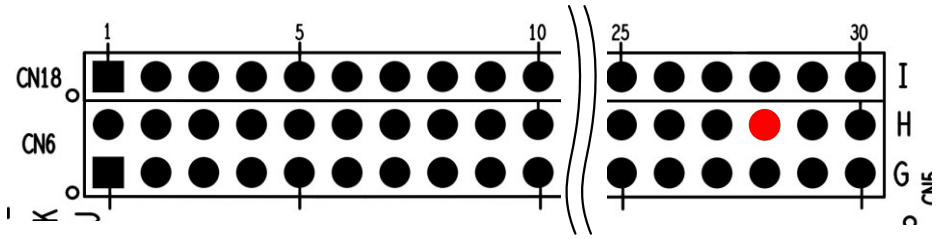


Figure 5 Pin Header CN6 and CN18 with Corresponding Label

Above picture **Figure *8*** shows a schematic overview of CN6 and CN18 (upper side of the board). The rectangular representation of the pin in the overview picture in sec. 2.1 identifies the #1 pin of both connectors. Thus, the assignment of the device pins to the individual connector pins can be checked in **Chapter 11 'Schematic'**.

However, for user's convenience the rows and columns of the connectors are additionally labeled with numbers and letters. This enables easier identification of the pin. As an example, the red highlighted dot in **Figure 8** has the coordinates H28. Additionally, the coordinates are also shown in **Chapter 11 'Schematic'**.

The assignment of the connectors is shown in the following tables.

Table 5 Pin Assignment of CN8 and CN16

Row	Column A	Column B	Column C
1	GND	GND	GND
2	P20_7	P20_6	P20_5
3	P20_2	P20_3	P20_4
4	P20_1	P20_0*1)	ERROROUT_M
5	P24_9	RES_IN	RES_OUT
6	P24_8	P24_7	P24_6
7	P24_3	P24_4	P24_5
8	P24_2	P24_1	P24_0
9	P21_3*1)	P21_4*1)	P21_5*1)
10	P21_2*1)	P22_13	P22_12
11	P22_9	P22_10	P22_11

Row	Column A	Column B	Column C
12	P22_8	P22_7	P22_6
13	P22_3	P22_4	P22_5
14	P22_2	P22_1	P22_0
15	X2[*1)]	X1[*1)]	NMI
16	AURORES	GND	GND
17	P23_5	P23_6	P23_7
18	P23_4	P23_3	P23_2
19	P25_0	P23_0	P23_1
20	P25_1	P25_2	P25_3
21	P25_6	P25_5	P25_4
22	P25_7	P25_8	P25_9
23	P25_12	P25_11	P25_10
24	P25_13	P25_14	P25_15
25	P26_0	P26_1	P31_15
26	P31_12	P31_13	P31_14
27	P31_11	P31_10	P31_9
28	P31_6	P31_7	P31_8
29	P31_5	P31_4	P31_3
30	P31_0	P31_1	P31_2

Table 6 Pin Assignment of CN5 and CN17

Row	Column D	Column E	Column F
1	GND	GND	GND
2	P02_7	P02_6	P02_5
3	P02_2	P02_3	P02_4
4	P10_14	P02_0	P02_1
5	P10_13	P10_12	P10_11
6	P10_8	P10_9	P10_10
7	P10_7	P10_6	P10_5
8	P10_2[*1)]	P10_3[*1)]	P10_4
9	P10_1[*1)]	P10_0[*1)]	P13_14
10	P13_11	P13_12	P13_13
11	P13_10	P13_9	P13_8

Row	Column D	Column E	Column F
12	P13_5	P13_6	P13_7
13	P13_4	P13_3[*1)]	P13_2[*1)]
14	P13_1[*1)]	P13_0[*1)]	P11_10
15	P11_7	P11_8	P11_9
16	P11_6	P11_5	P11_4
17	P11_1	P11_2	P11_3
18	P12_8	P12_9	P11_0
19	P12_5	P12_6	P12_7
20	P12_2	P12_3	P12_4
21	P14_12	P12_0	P12_1
22	P14_9	P14_10	P14_11
23	P14_8	P14_7	P14_6
24	P14_3	P14_4[*1)]	P14_5[*1)]
25	P14_2	P14_1	P14_0
26	P15_6	P15_7	P15_8
27	P15_5	P15_4	P15_3
28	P15_2	P15_1	P15_0
29	P24_13	P24_14	P24_15
30	P24_10	P24_11	P24_12

Table 7 Pin Assignment of CN6 and CN18

Row	Column G	Column H	Column I
1	GND	GND	AN210[*2)]
2	AN213[*2)]	AN212[*2)]	AN211[*2)]
3	AN200[*2)]	AN201[*2)]	AN202[*2)]
4	AN240	AN241	AN203[*2)]
5	AN220[*2)]	AN242	AN243
6	AN221	AN222[*2)]	AN223[*2)]
7	AN230	AN231	AN232[*2)]
8	AN250	AN251	AN233
9	AN260	AN252	AN253
10	AN261	AN262	AN263
11	AN270	AN271	AN272

Row	Column G	Column H	Column I
12	AN350	AN351	AN273
13	AN360	AN352	AN353
14	AN361	AN362	AN363
15	AN320	AN321	AN322
16	AN310	AN311	AN323
17	AN300	AN312	AN313
18	AN301	AN302	AN303
19	AN370	AN371	AN372
20	P00_11	P00_10	AN373
21	P00_9	P00_8	P00_7
22	P00_6	P00_5	P00_4
23	P00_3	P00_2	P00_1
24	P01_3	P01_4	P00_0
25	P01_7	P01_6	P01_5
26	P01_8	P01_9	P01_10
27	P01_13	P01_12	P01_11
28	P01_14	P01_15	P02_11
29	P02_8	P02_9	P02_10
30	GND	GND	GND

Table 8 Pin Assignment of CN7 and CN14

Row	Column J	Column K	Column L
1	GND	GND	GND
2	P30_15	P30_14	P30_13
3	P30_10	P30_11	P30_12
4	P30_9	P30_8	P30_7
5	P30_4	P30_5	P30_6
6	P30_3	P30_2	P30_1
7	P32_6	P32_5	P30_0
8	P32_2	P32_3	P32_4
9	P32_1	P32_0	P33_13
10	P33_10	P33_11	P33_12
11	P33_9	P33_8	P33_7

Row	Column J	Column K	Column L
12	P33_4	P33_5	P33_6
13	P33_3	P33_2	P33_3
14	P34_4	GND	P33_0
15	P34_3	P34_2	P34_1
16	AN100	AN101	P34_0
17	AN110	AN102	AN103
18	AN111	AN112	AN113
19	AN120	AN121	AN122
20	AN060	AN061	AN123
21	AN050	AN062	AN063
22	AN051	AN053	AN052
23	AN040	AN041	AN042
24	AN020	ADSVCL	AN043
25	AN021	AN022	AN023
26	AN000*2)	AN001*2)	AN002*2)
27	AN010	AN011	AN003*2)
28	AN030	AN012	AN013
29	AN031	AN032	AN033
30	GND	GND	GND

Note 1): This signals are by default not connected to the pin header. For connecting these pins the corresponding 0Ohm resistance needs to be soldered. For details, please refer to **Chapter 11 'Schematic'**.

Note 2): This signals are equipped with a filter structure in front of the analogue input pins. For details, please refer to **Chapter 11 'Schematic'**.

6.2 Toggle Switch for RESET

In order to issue a RESET to the device, the toggle switch SW1 is available.

The switch is a Nidec Copal Electronics Miniature Toggle Switch 'BT1H-2M4-Z' with two positions to issue a RESET.

The switching function is depicted in **Figure 6**. In order to issue a RESET to the device the switch needs to be toggled either to the left or to the right side. To the right side – 'ON' – a static RESET can be applied, while on the left side – '(ON)' – a momentary RESET is applied and the switch will return into the 'OFF' position again. Please note that the position of the switch is defined from the side of the part number marking, which is highlighted with a red arrow.

Switching function / Part No.	Viewed from part No. marking side		
			
★BT1H-2M4-Z	(ON)	OFF	ON
Connecting terminals	2−1	−	2−3

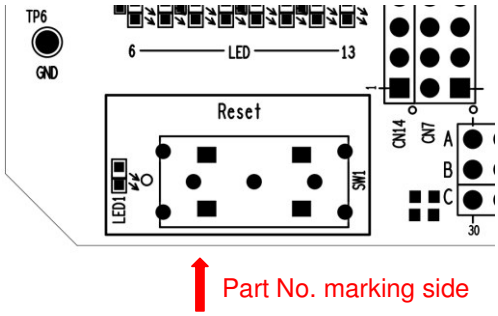


Figure 6 RESET Switching Function

LED1 is indicating the function of the switch, i.e. LED1 illuminates when the RESET is asserted by the switch. Please note that LED1 cannot indicate a RESET by another source e.g. a connected tool.

6.3 Mode Selection

The PiggyBack Board gives the possibility to configure the following mode pins

- MD0 via jumper JP26
- MD1 via jumper JP27

To apply “High” to the mode pins, the corresponding jumpers can be set.

CAUTION: *Be careful in configuration of mode related pins, as wrong configuration can cause irregular behavior of the devices. Be sure to check the corresponding User’s Manual for details, which modes can be selected for the used device.*

6.4 Connectors to Mainboard

Three connectors (CN1, CN2 and CN3) are available to connect the PiggyBack board to a Mainboard. Regarding the function on the Mainboard, please refer to the UM of any supported Mainboard (Y-RH850-X1X-MB-Tx-Vx).

For details about the signal assignment to the connectors, please refer to **Chapter 11 ’Schematic’**.

6.4.1 Assignment of CAN Pins

The available Mainboards (Y-RH850-X1X-MB-Tx-Vx) provide connectors for CAN communication. The channel number of the Mainboards does not necessarily match the channel number of RH850/E2x devices.

The following table shows the assignment.

Table 9 CAN Function Assignment

Mainboard	PiggyBack Board (MCU)	
	Port Pin	CAN Alternative Function
CAN0TX	P32_1	CTX2
CAN0RX	P32_0	CRX2
CAN1TX	P15_2	CTX1
CAN1RX	P15_1	CRX1
CAN2TX	P02_0	CTX0
CAN2RX	P02_2	CRX0
CAN3TX	P32_6	CTX3
CAN3RX	P32_4	CRX3
CAN4TX	P15_7	CTX4
CAN4RX	P15_8	CRX4
CAN5TX	P15_5	CTX5
CAN5RX	P15_3	CRX5
CAN6TX	P00_11	CTX6
CAN6RX	P00_10	CRX6
CAN7TX	P31_14	CTX7
CAN7RX	P31_15	CRX7
CAN8TX	P25_8	CTX8
CAN8RX	P25_9	CRX8
CAN9TX	P31_10	CTX9
CAN9RX	P31_11	CRX9

6.5 RHSIF I/F

CN11 is available to connect to the RHSIF I/F signals of the device. The connector is a Samtec ‘ERF8-005-05.0-L-DV-L-TR’ type connector and the following table shows the signal assignment.

Table 10 RHSIF I/F Pin Assignment

CN11 Pin	Function*1	Device Pin*1	Function*2	Device Pin*2		CN11 Pin	Function	Device Pin
1	HSIF0_TXDP	P21_5	HSIF0_RXDP	P21_3		2	GND	-
3	HSIF0_TXDN	P21_4	HSIF0_RXDN	P21_2		4	GND	-
5	GND	-	GND	-		6	HSIF0_REFCLK	P20_0

CN11 Pin	Function*1	Device Pin*1	Function*2	Device Pin*2		CN11 Pin	Function	Device Pin
7	HSIF0_RXDP	P21_3	HSIF0_TXDP	P21_5		8	GND	-
9	HSIF0_RXDN	P21_2	HSIF0_TXDN	P21_4		10	GND	-

Note 1 & 2: The function of CN11 pins 1, 3, 7 and 9 depend on the configuration of JP35

- JP35 pins 1 and 2 connected: Function *1 is effective
- JP35 pins 2 and 3 connected: Function *2 is effective

All signals are by default not connected to a pin header in order to minimize disturbance on the signal. If needed the signals can be connected to CN8 (pins #8 and 17 – 19) and CN16 (pin #9) via connecting with 0Ohm resistances R31, R50, R75, R76 and R78. For details, please refer to **Chapter 11 'Schematic'**.

6.6 HS-SPI I/F

CN13 is available to connect to the HS-SPI I/F signals of the device. The connector is a Samtec 'ERF8-005-05.0-L-DV-L-TR' type connector and the following table shows the signal assignment.

Table 11 HS-SPI I/F Pin Assignment

CN13 Pin	Function	Device Pin		CN13 Pin	Function*1	Device Pin*1	Function*2	Device Pin*2
1	CLKP	P13_1		2	TXDP	P13_3	RXDP	P14_4
3	CLKN	P13_0		4	TXDN	P13_2	RXDN	P14_5
5	GND	-		6	GND	-	GND	-
7	GND	-		8	RXDP	P14_4	TXDP	P13_3
9	SSL/SSLI*3	P14_2		10	RXDN	P14_5	TXDN	P13_2

Note 1 & 2: The function of CN13 pins 2, 4, 8 and 10 depend on the configuration of JP29

- JP29 pins 1 and 2 connected: Function *1 is effective
- JP29 pins 2 and 3 connected: Function *2 is effective

Note 3: The function of the pin P14_2 can be configured in the used MCU device. For details, please refer to the HW user's manual of the used device.

All signals (except SSL/SSLI on CN13 #9) are by default not connected to a pin header in order to minimize disturbance on the signal. If needed the signals can be connected to CN5 (pins #26 – 28 and 48) and CN17 (pins #13 and 24) via connecting with 0Ohm resistances R112, R113, R115, R116, R118 and R119. For details, please refer to **Chapter 11 'Schematic'**.

6.7 RHSB I/F

CN12 is available to connect to the HS-SPI I/F signals of the device. The connector is a Samtec 'ERF8-010-05.0-L-DV-L-TR' type connector and the following table shows the signal assignment

Table 12 RHSB I/F Pin Assignment

CN12 Pin	Function	Device Pin	CN12 Pin	Function	Device Pin
1	RHSB1FCLN	P10_1	2	RHSB1CSD0	P10_7
3	RHSB1FCLP	P10_0	4	RHSB1EMRG	P12_0
5	GND	-	6	RHSB1SI0	P12_2
7	RHSB1SON	P10_3	8	RHSB1SI1	P12_4
9	RHSB1SOP	P10_2	10	RHSB1CSD1	P10_6
11	RHSB0FCLN	P13_0	12	RHSB0CSD0	P14_7
13	RHSB0FCLP	P13_1	14	RHSB0EMRG	P12_7
15	GND	-	16	RHSB0SI0	P12_3
17	RHSB0SON	P13_2*1	18	RHSB0SI1	P12_1
19	RHSB0SOP	P13_3*1	20	RHSB0CSD1	P12_5

Note 1: By default, these signals are not directly connected to the corresponding device pins. In order to use these signals for the RHSB I/F CN12 pins #17 and #19 must be connected to the device via 0Ohm resistances R104 and R105. In case of using the HS-SPI I/F (refer to section **6.6**), it is recommended to not apply the latter resistances. This it to minimize signal disturbance. For details, please refer to **Chapter 11 'Schematic'**.

The signals assigned to CN12 pins #1, 3, 7, 9, 17 and 19 are by default not connected to a pin header in order to minimize disturbance on the signal. If needed the signals can be connected to CN5 (pins #15 – 18 and 26) and CN17 (pin #13) via connecting with 0Ohm resistances R108 – R111 and R115 and R116. Please also consider above note 1. For details, please refer to **Chapter 11 'Schematic'**.

Chapter 7 Other Circuitry

7.1 Signaling for ERROROUT_M

A red LED (LED4) is available two indicate a “low” output signal from ERROROUT_M.

7.2 Pin Headers for Pull-Down and Pull-Up

A connector CN9 is available to enable easy connection to 3.3V / 5V or GND via pull-up or pull-down resistances, respectively.

Hereby uneven pins from 1 to 19 (in total ten) are configured as pull-up pin headers, while the even numbers from 2 to 20 (in total ten) can be used for pull-down. JP25 and JP32 configure the voltage connected to the uneven pins to 3.3V or 5V. JP25 configures uneven pins 1 – 9 and JP32 configures uneven pins 11 – 19.

By connecting device port pins from CN5 – 8 to CN9 it is therefore possible to pull a desired port pin to “Low” or “High”.

7.3 Signaling LEDs

Eight LEDs are provided to allow visual observation of the output state of device pins. Device pins P33_0 to P33_7 are connected to the uneven pins 15 to 1 of the pin header CN4, while the LEDs 6 to 13 are connected to the even pins 16 to 2, respectively. Thus, the LEDs can be connected to the device port pins P33_0 to P33_7 via jumper or to any device port pin by connecting directly to the even pin headers of CN4.

Chapter 8 Jumper Configuration

Jumper are available to configure the function of the board. This chapter describes the standard configuration, i.e. jumper setting for the intended devices, to enable basic operation. For a detailed explanation of the supported function of the used device, please refer to the corresponding HW user's manual.

Table 13 Recommended Jumper Settings

Purpose	Jumper #	Device	
		RH850/E2M in BGA468	
		FCC2 for E2UH/E2H	E2UH/E2H
5.0V Main	0	o	o
3.3V Main*1)	1	o (opt)	- (opt)
5.0V Analog Main	2	o	o
EVTI Connect*2)	3	- (opt)	- (opt)
E0VCC	4	o	o
E1VCC Config	5	#1-#2	#1-#2
E2VCC Config	6	#1-#2	#1-#2
LVDVCC Config	7	#1-#2	#1-#2
SYSVCC Config	8	#1-#2	#1-#2
VCC Config	9	#1-#2	#1-#2
EMUVCC*1)	10	o (opt)	-
VDDIOF	11	#1-#2	#1-#2
A0VCC	12	o	o
A0VREFH	13	o	o
A1VCC	14	o	o
A1VREFH	15	o	o
A2VCC	16	o	o
A2VREFH	17	o	o
A3VCC	18	o	o
A3VREFH	19	o	o
ADSVCC	20	o	o
ADSVREFH	21	o	o
1.25V Source	22	#1-#2	#1-#2
VDD	23	o	o
EMUVDD*1)	24	o (opt)	-
CN9 Pull-Up 1-9	25	- (opt)	- (opt)
MD0 Pull-Up	26	- (opt)	- (opt)
MD1 Pull-Up	27	- (opt)	- (opt)
EVTO Pull-Up*2)	28	- (opt)	- (opt)
HS-SPI IC4 Config	29	- (opt)	- (opt)
Board_VCC Config	30	#1-#2	#1-#2
TRST Config	31	#2-#3	#2-#3
CN9 Pull-Up 11-19	32	- (opt)	- (opt)
ADSVREFL Pull-Down	33	o	o
AURORES Config*3)	34	#1-#2 (opt)	#2-#3 only
RHSIF IC5 Config	35	- (opt)	- (opt)
EVTI Pull-Up*2)	36	- (opt)	- (opt)
EVTO Connect*2)	37	- (opt)	- (opt)

Note 1): Optionally for the FCC1 device only. If any of the FCC1 specific features are used (e.g. ERAM, Aurora Trace …) these jumpers needs to be set.

Note 2): Whether EVTO and/or EVTI signals are supported and need to be pulled up depends on the used tool. Please clarify with your tool vendor about the specification.

Note 3): Optionally for the FCC1 device only, if Aurora Trace is used. Please refer to the user's documentation of the used tool for dedicated requirement.

The table has the following meaning:

- o: Jumper must be connected.
- o (opt): Recommended to be connected. Can be left open if not necessary for use case
- -: Jumper must be left open
- - (opt): Not mandatory to connect. Can be connected if necessary for use case
- #x-#y: Connect the pins #x and #y for the standard configuration. Possible to configure depending on the use case and on the allowed specification of the used device.

A small circle near the jumper on the board and a rectangular representation of the pin in the overview picture in sec. **2.1** identifies the #1 pin of the jumper.

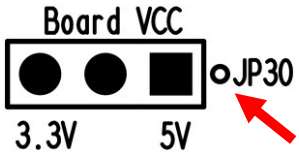


Figure 7 Identifying the Pin #1 at a Jumper

In this example (JP30), the pin #1 is on the right side. The red arrow highlights the marking circle.

Chapter 9 Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied, when the power supplied to the board is turned off.

Please follow below sequence:

1. At first assert a RESET via SW1 and keep the Reset asserted.
2. Turn off the board power supply.
3. After power supply is shut down, put the SW1 to 'OFF' position.

For details how to apply a RESET, please refer to **6.2 'Toggle Switch for RESET'**.

9.2 Pin Function Assignment of HS-SPI Pins

In order to enable HS-SPI communication between two PiggyBack boards some of the signals need to be switched. Thus, the device pins P13_2, P13_3, P14_4 and P14_5 are connected to a differential multiplexer IC (IC4). The inputs of this device are only 3.3V tolerant.

It is therefore not allowed to configure above mentioned pins to GPIO or any alternative functions other than the LVDS functions used on this board.

For details, please refer to section **6.6** and **Chapter 11 'Schematic'**, as well as the corresponding User's Manual of the used device.

Chapter 10 Mechanical Dimensions

All dimensions given in mm.

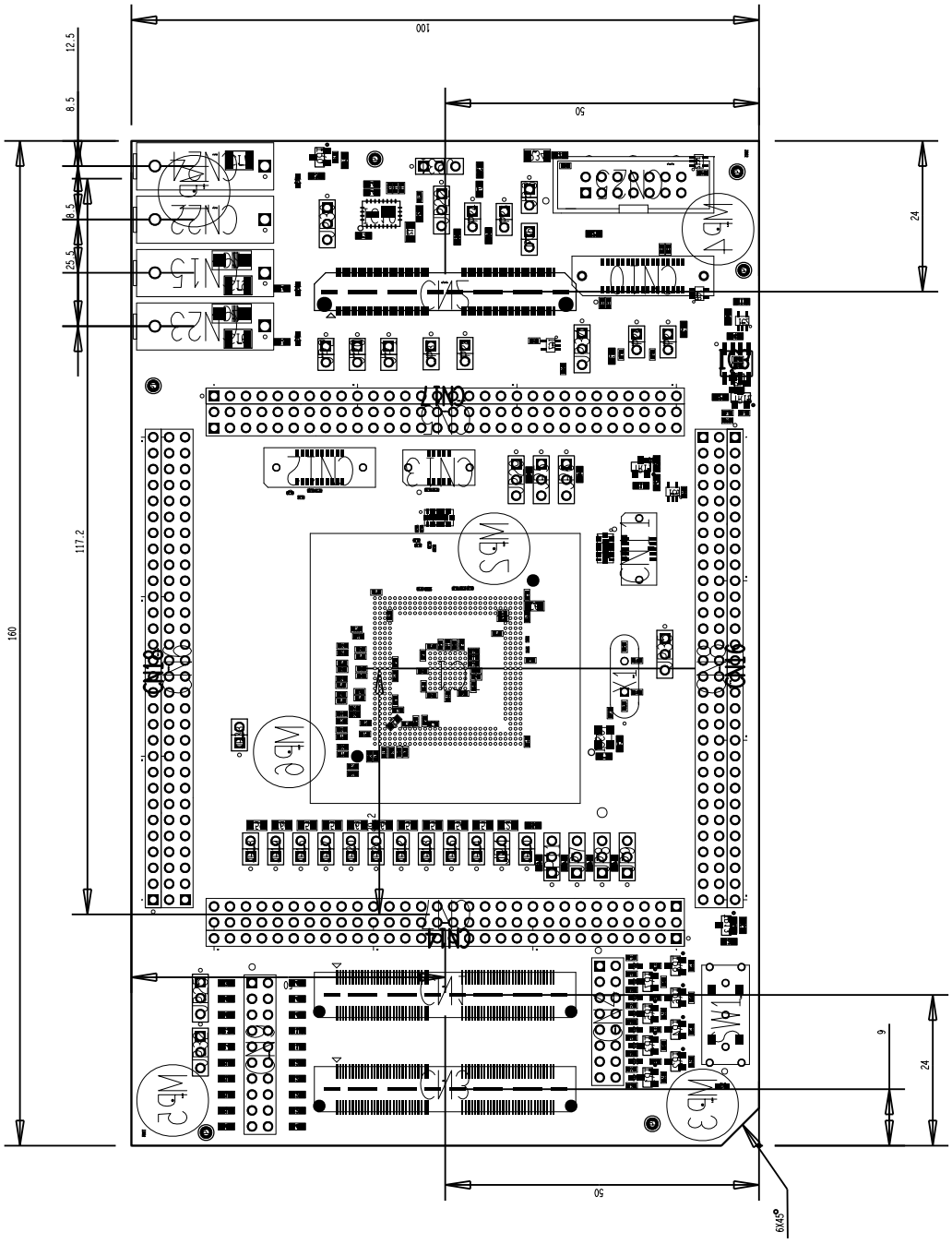


Figure 8 Dimensions of the PiggyBack Board

Chapter 11 Schematic

CAUTION: *The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.*

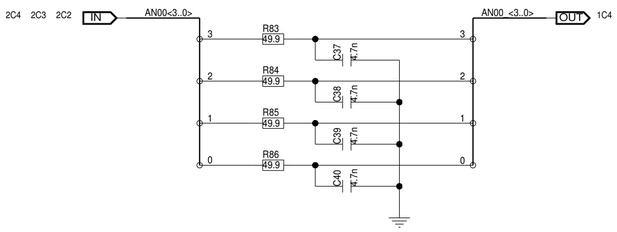
The following components described in the schematic are not provided with the board:

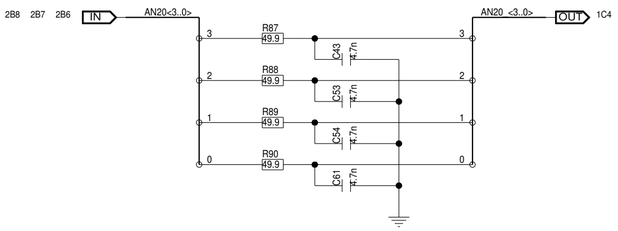
- Oscillator OSC1
- Capacitors C29 and C33
- Resistances
    - R48 and R49
    - R79 and R101
    - R31, R50, R75, R76, R78, R108 – R113, R115, R116, R118 and R119

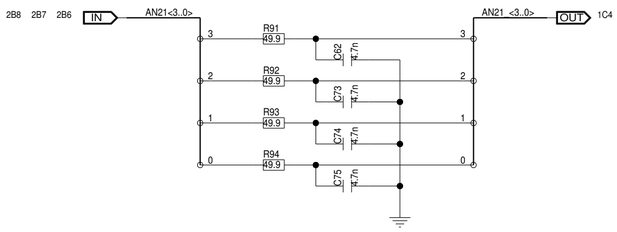
The following components described in the schematic are provided with but not mounted on the board:

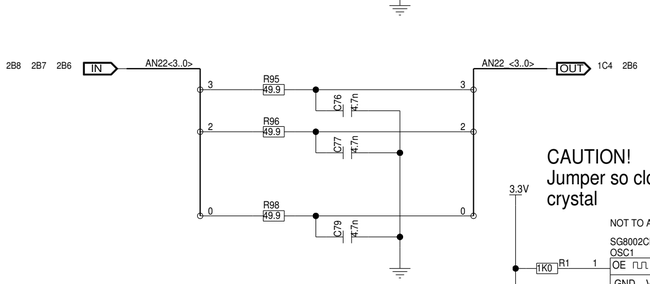
- Standard 4mm power lab sockets
    - CN22
    - CN15, CN23 and CN24

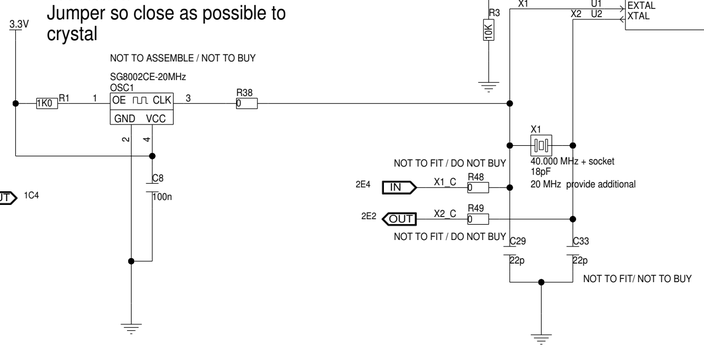
REV	COMMENT	DATE	DRAWN BY
1.00	Release	13.12.2017	W.Rauser

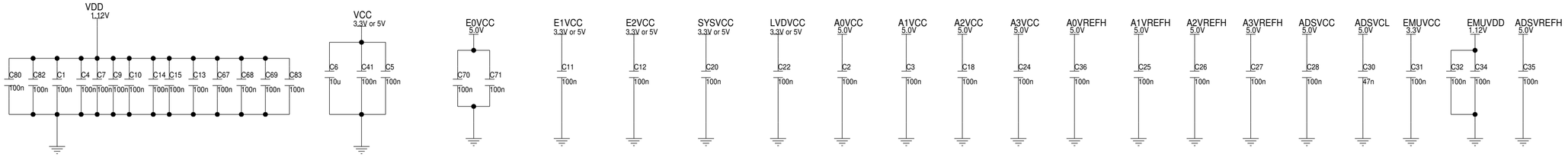










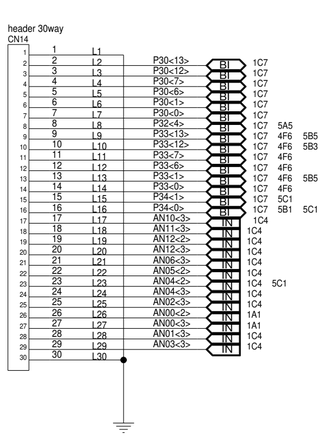


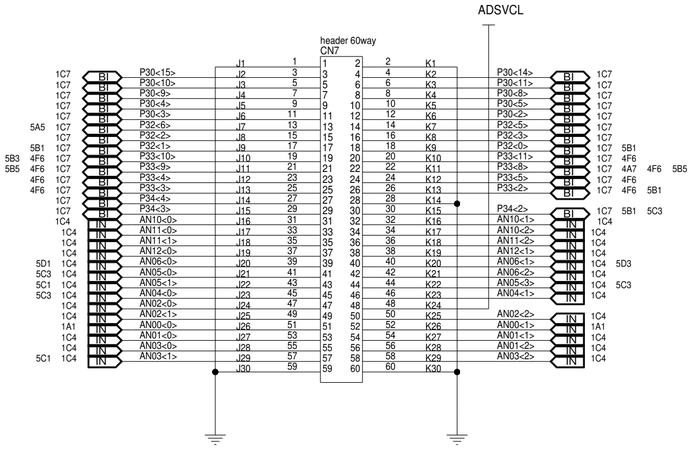
RENESAS Electronics Europe GmbH

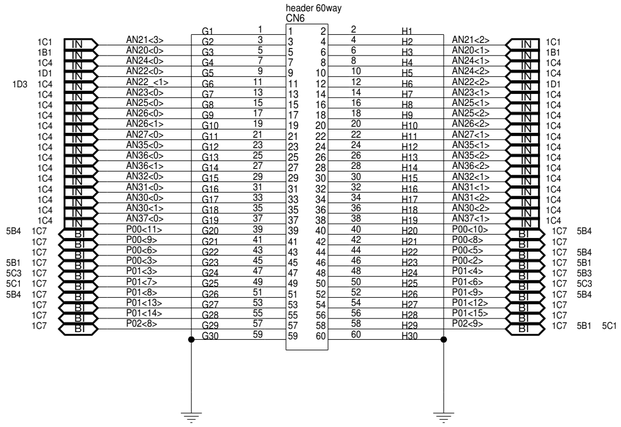
Title: rh850_e2x_468pin_pb_t1_v1

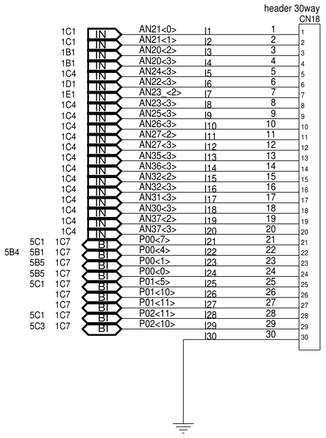
Size: A2 | Document Number: EESS-0400-159-01

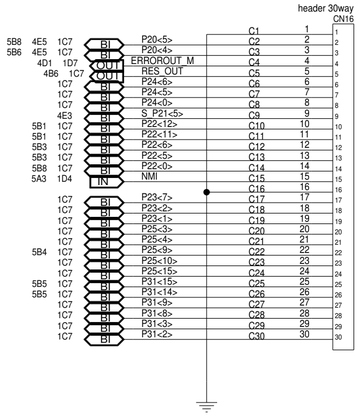
Date: Wed Dec 13 06:35:09 2017 | PAGE 1 OF 5 | 1.00

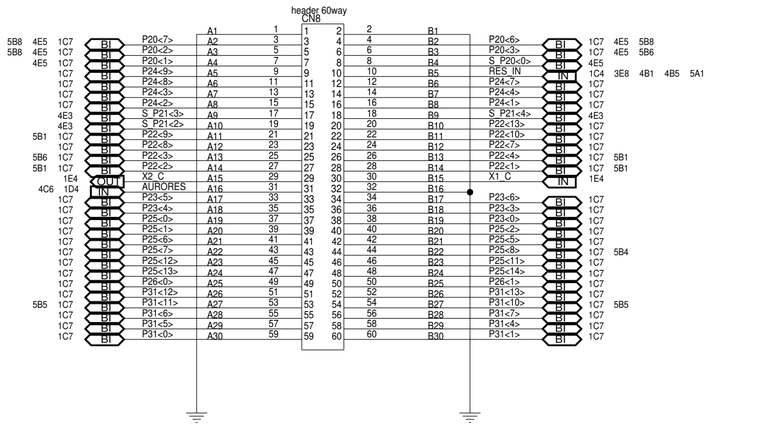


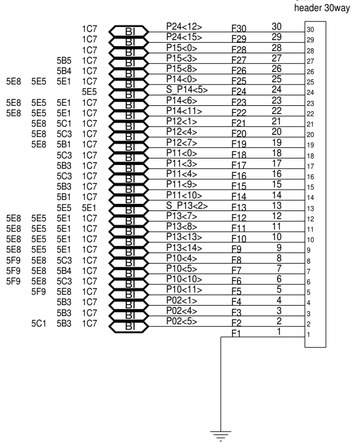


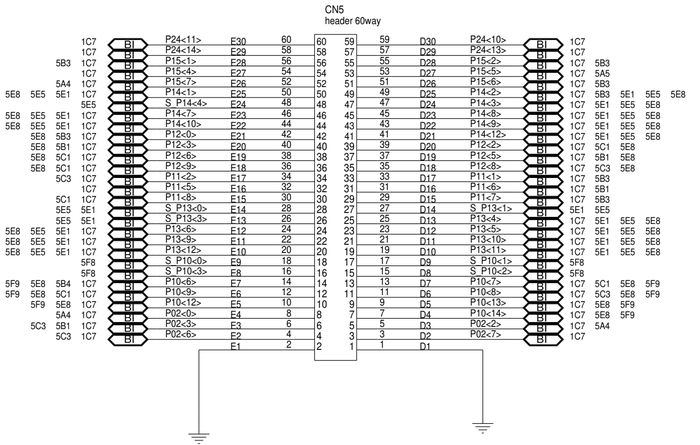












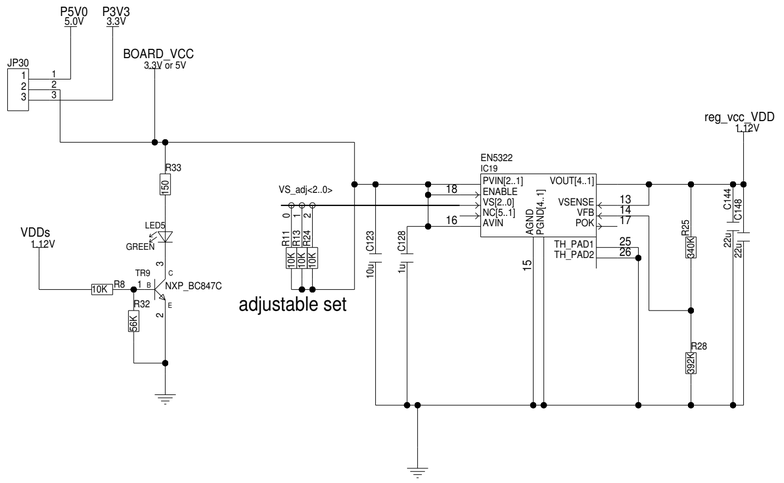
RENESAS Electronics Europe GmbH

Title: rh850_e2x_468pin_pb_t1_v1

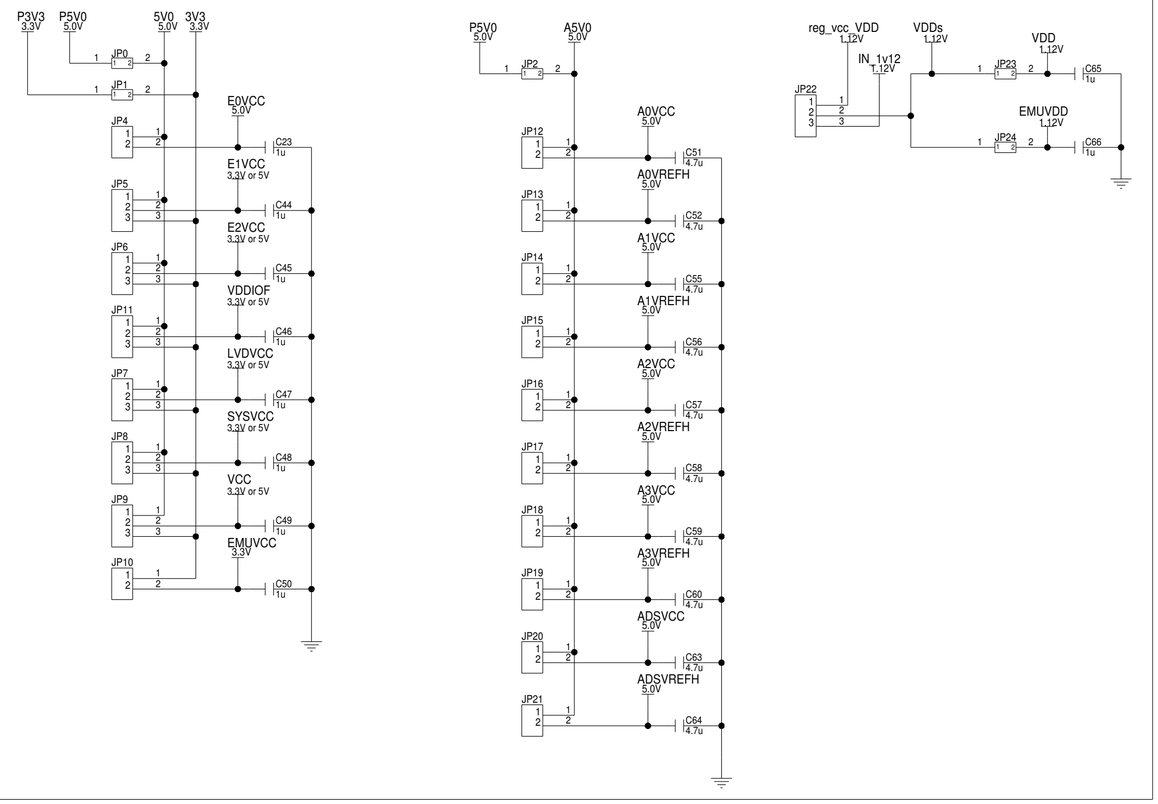
Size: A2 | Document Number: EESS-0400-159-01

Date: Tue Dec 12 15:57:40 2017 | PAGE 2 OF 5 | 1.00

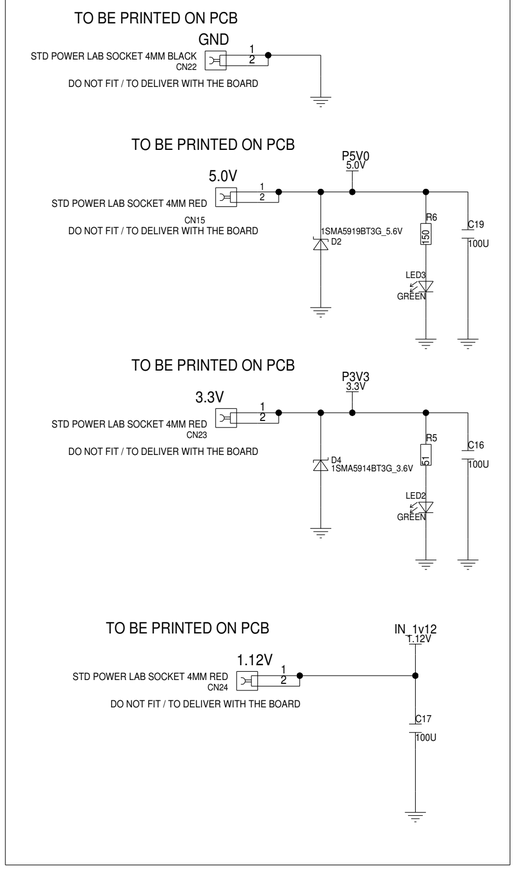
VOLTAGE REGULATOR



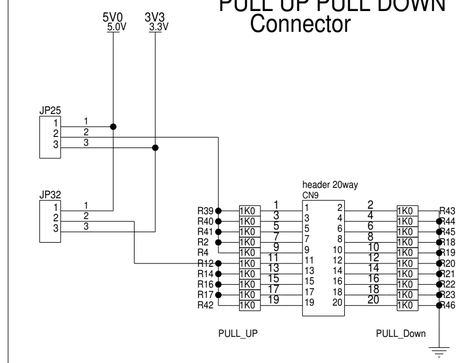
VOLTAGE DISTRIBUTION



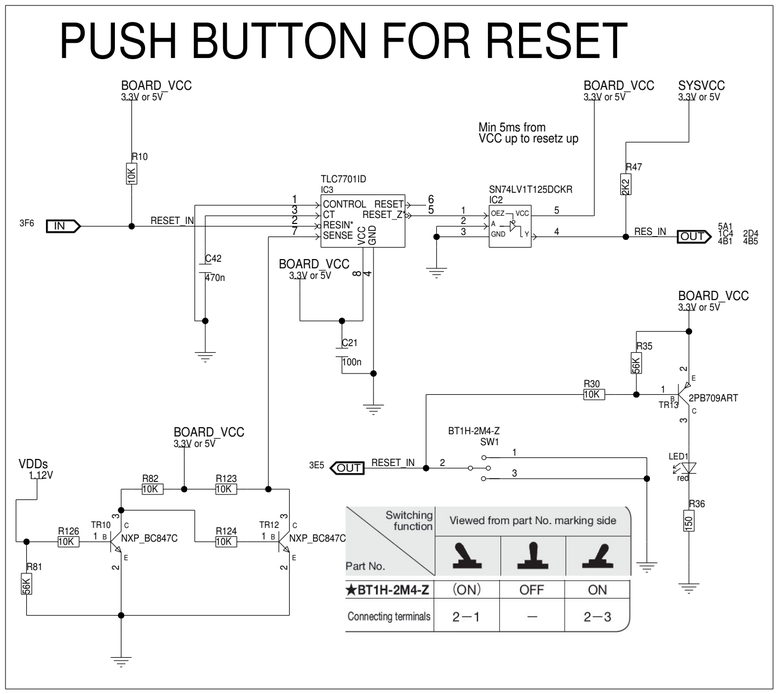
POWER SUPPLY



PULL UP PULL DOWN
Connector



PUSH BUTTON FOR RESET



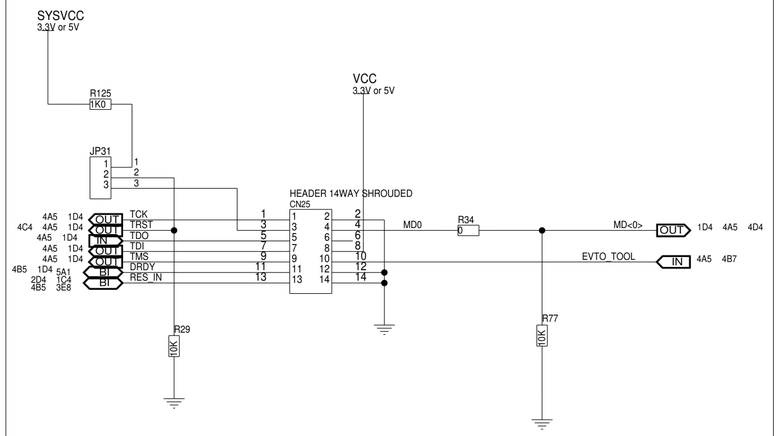
RENESAS Electronics Europe GmbH

Title: rh850_e2x_468pin_pb_t1_v1

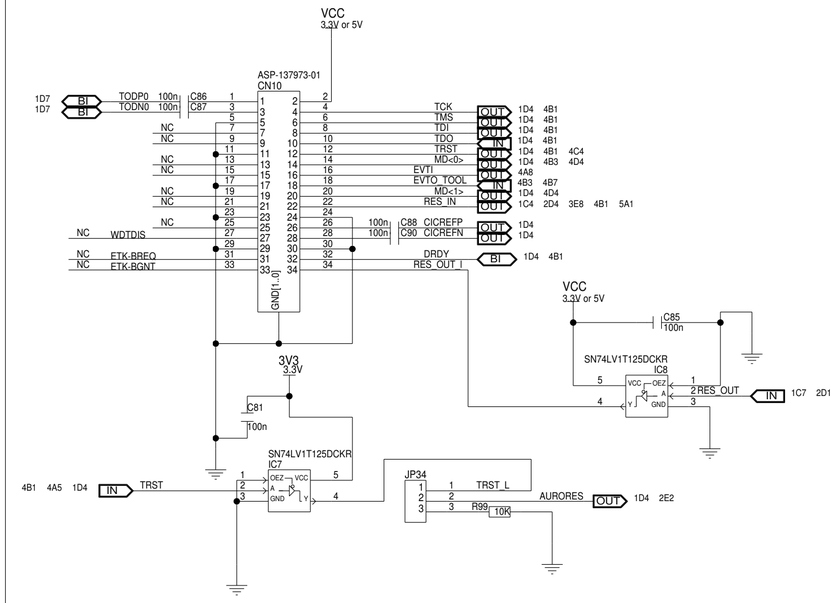
Size: A2 | Document Number: EESS-0400-159-01

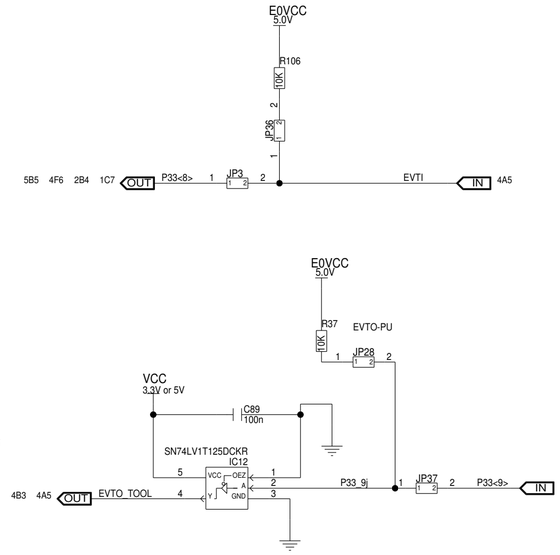
Date: Tue Dec 12 15:57:38 2017 | PAGE 3 OF 5 | 1.00

DEBUG AND PROGRAMMING INTERFACE

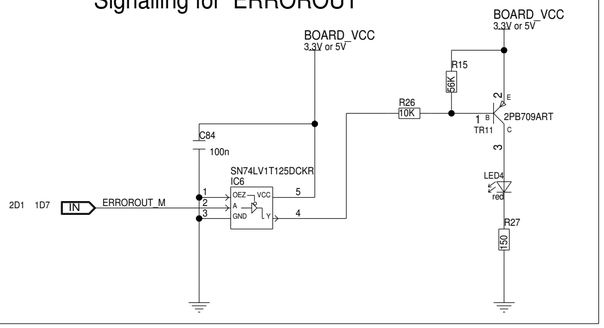


Aurora I/F

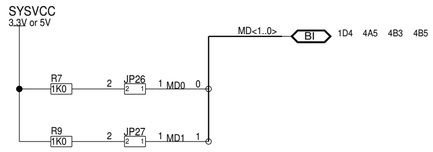




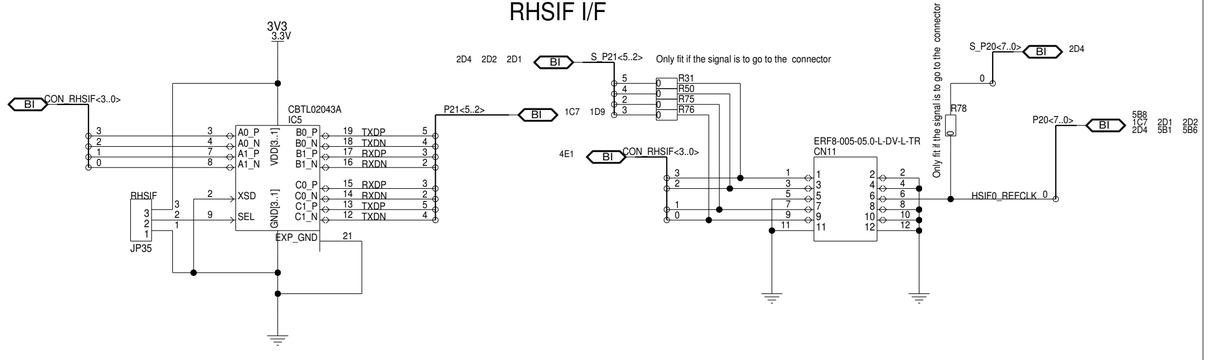
Signalling for ERROROUT



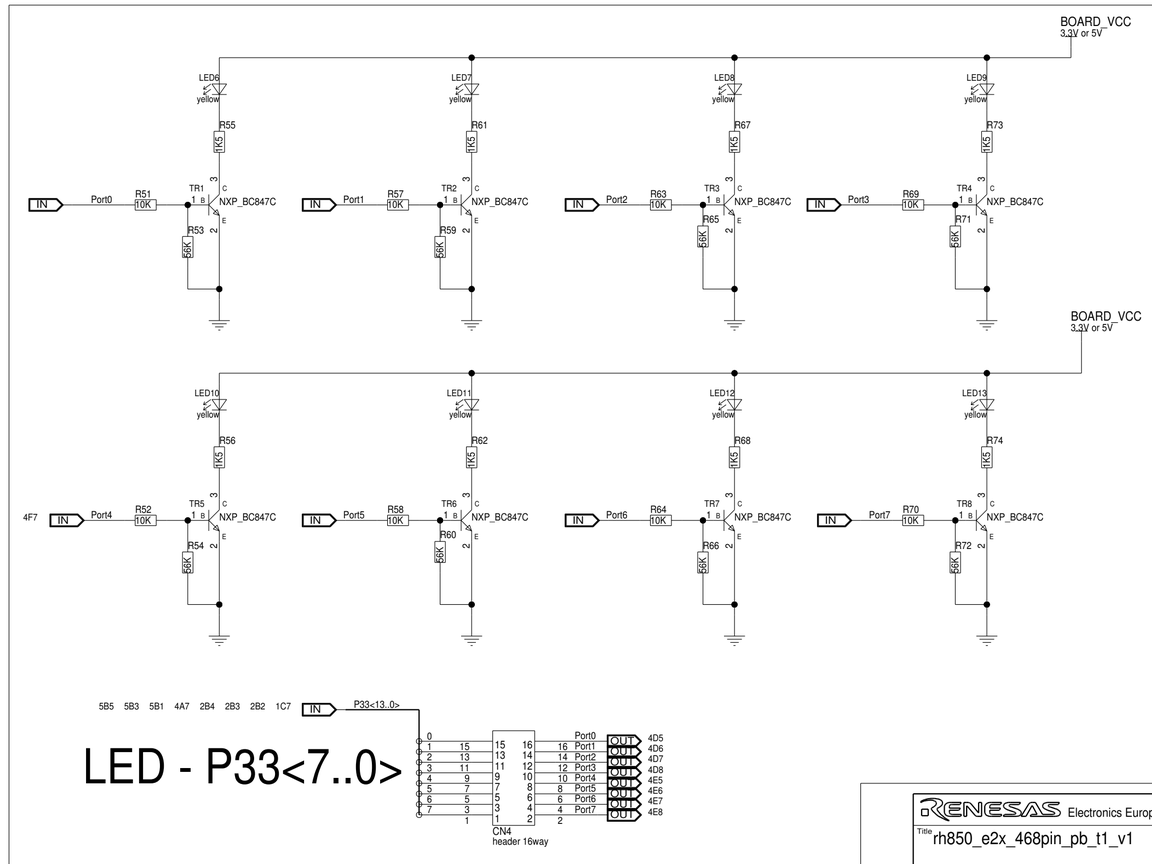
MODE Jumper



RHSIF I/F



LED - P33<7..0>



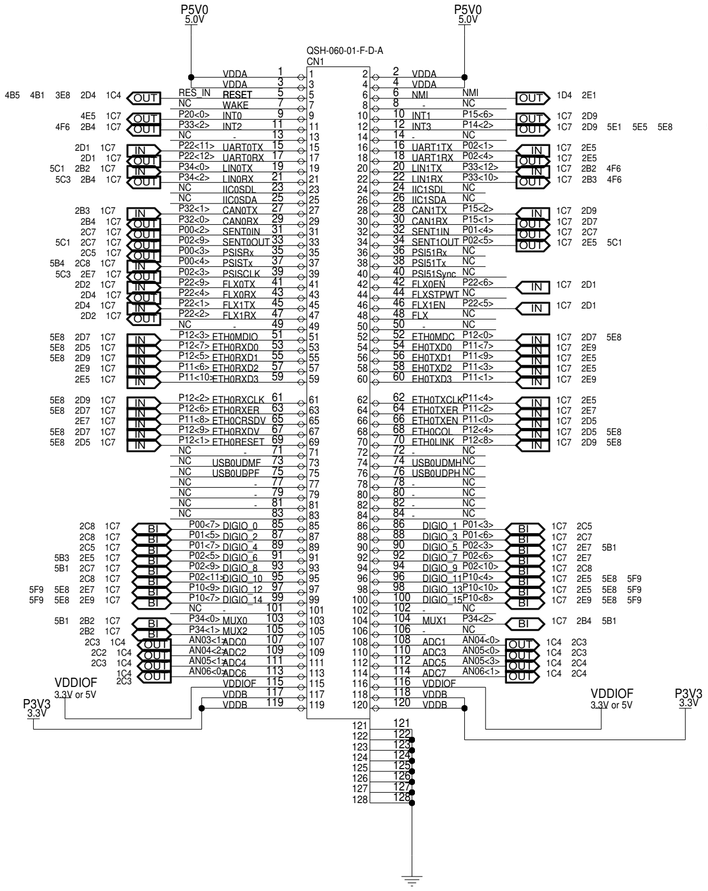
Title: rh850_e2x_468pin_pb_t1_v1

Size: A2 | Document Number: EESS-0400-159-01

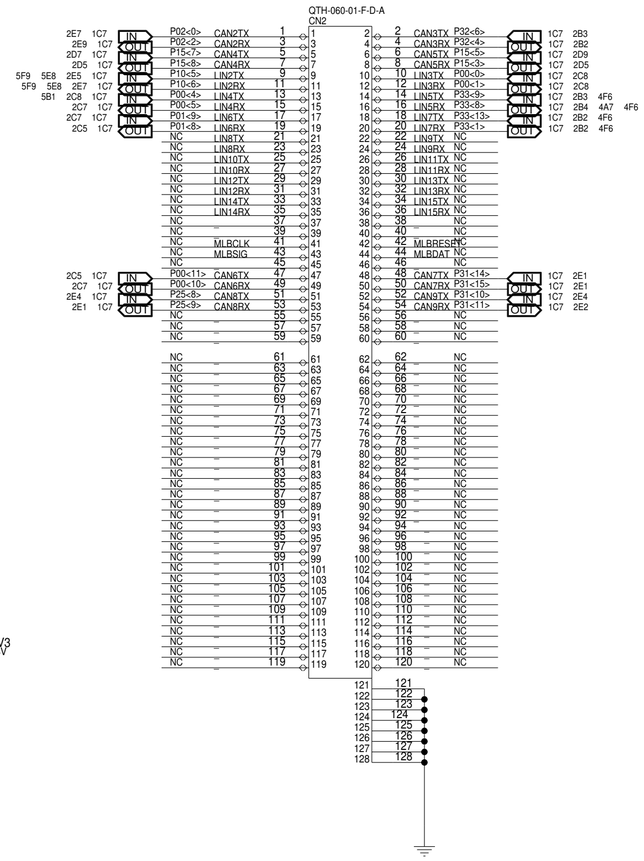
Date: Tue Dec 12 16:18:53 2017 | PAGE 4 OF 5 | 1.00

CONNECT TO MAIN BOARD

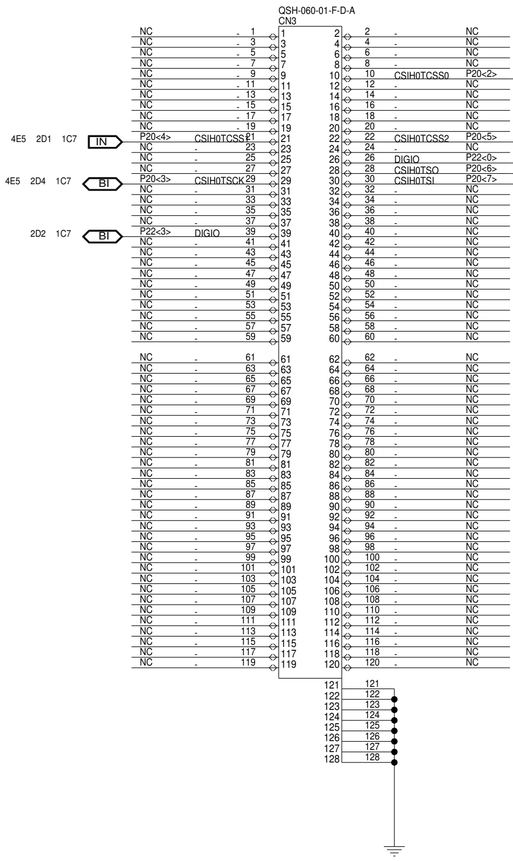
CONNECTOR1



CONNECTOR2



CONNECTOR3



FUDUCIALS

TOP

TP11 FIDUCIAL_1MM

TP12 FIDUCIAL_1MM

BOTTOM

TP14 FIDUCIAL_1MM

TP15 FIDUCIAL_1MM

GND TEST POINT

TP5 GND-TESTPOINT

TP6 GND-TESTPOINT

TP7 GND-TESTPOINT

TP8 GND-TESTPOINT

TP9 GND-TESTPOINT

TP10 GND-TESTPOINT

RUBBER FEET

BLACK MP1

BLACK MP2

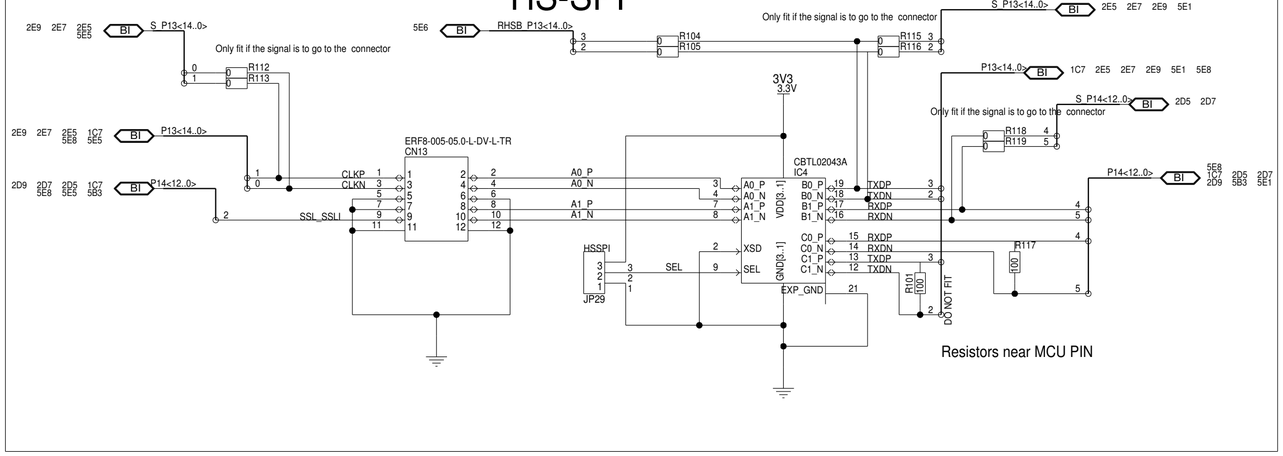
BLACK MP3

BLACK MP4

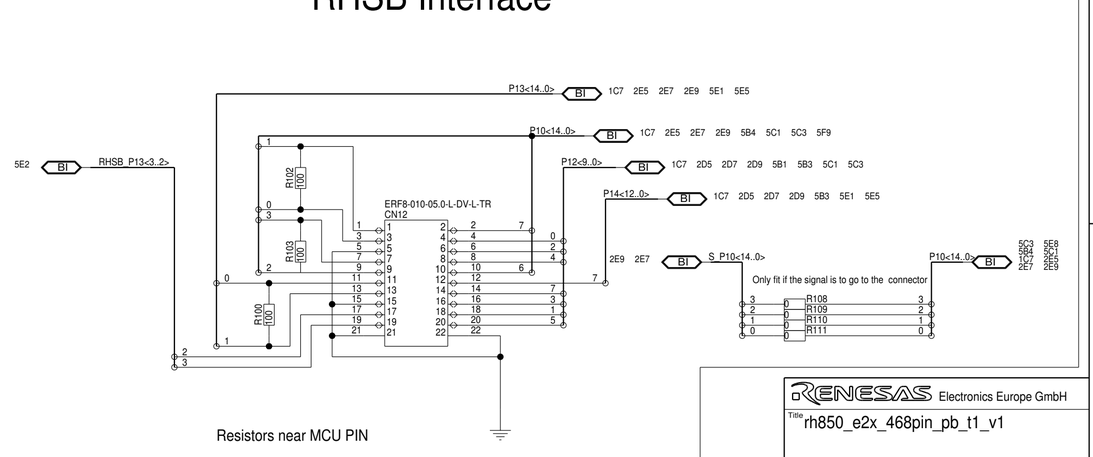
BLACK MP5

BLACK MP6

HS-SPI



RHSB Interface



Title	rh850_e2x_468pin_pb_t1_v1
Size	A2
Document Number	EESS-0400-159-01
Date:	Tue Dec 12 15:57:39 2017
	PAGE 5 OF 5
	1.00

Chapter 12 Revision History

The table provides information about the major changes of the document versions.

Date	Version	Description
2018-03-12	1.0	Initial release

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics.

   The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti- crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.

9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

    (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

    (Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

Renesas Electronics Corporation

www.renesas.com