

RH850 Evaluation Platform

RH850/U2A 156pin

User's Manual: Piggyback Board

Y-RH850-U2A-156PIN-PB-T1-V1

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

| | | |
|-------|--|----|
| 1. | Overview | 1 |
| 1.1 | Package Components | 1 |
| 1.2 | Supported Main Boards..... | 1 |
| 1.3 | Main Features | 1 |
| 1.4 | Piggyback Board Views..... | 2 |
| 1.5 | Mounting of the Device..... | 6 |
| 2. | Jumpers, Connectors, Switches and LEDs | 7 |
| 2.1 | Jumper Overview | 9 |
| 2.2 | Connector Overview..... | 11 |
| 2.3 | LED Overview | 12 |
| 3. | Power Supply | 13 |
| 3.1 | Board Power Connection | 13 |
| 3.2 | Voltage Distribution | 14 |
| 3.3 | Device Core Voltage (VDD) Selection | 15 |
| 3.4 | Current Measurement Bridges | 15 |
| 3.5 | Power Supply LEDs | 15 |
| 4. | Clock Supply | 16 |
| 4.1 | Main Oscillator..... | 16 |
| 4.2 | Programmable Oscillator..... | 17 |
| 4.3 | X1 and X2 on CN22 | 17 |
| 5. | Debug and Flash Programming Interfaces..... | 18 |
| 6. | Other Circuitry | 19 |
| 6.1 | Operation Mode Selection..... | 19 |
| 6.2 | RESET Switch..... | 21 |
| 6.3 | Signaling LEDs..... | 22 |
| 6.4 | Pull-Up/Pull-Down Pin Header | 23 |
| 7. | Connectors | 24 |
| 7.1 | Connectors to the Main Board CN1 to CN3..... | 24 |
| 7.1.1 | Main Board Connector CN1 | 24 |
| 7.1.2 | Main Board Connector CN2..... | 26 |
| 7.1.3 | Main Board Connector CN3..... | 28 |
| 7.2 | Debug Connector CN4..... | 31 |
| 7.3 | Pull-Up/Pull-Down Pin Header CN12..... | 31 |
| 7.4 | Device Ports Connectors CN18 and CN21 to CN23..... | 32 |
| 7.4.1 | Device Ports Connector CN18..... | 32 |
| 7.4.2 | Device Ports Connector CN21 | 33 |
| 7.4.3 | Device Ports Connector CN22..... | 34 |
| 7.4.4 | Device Ports Connector CN23..... | 35 |

| | | |
|--------|--|----|
| 8. | Jumper Configuration Examples | 36 |
| 8.1 | Stand-Alone Operation with Power Supply by Debugger | 36 |
| 8.2 | Configuration Examples | 37 |
| 8.2.1 | General Settings | 37 |
| 8.2.2 | Jumper Indicators..... | 37 |
| 8.2.3 | Stand-Alone Operation with Single External Power Supply 3.3 V: Minimum Configuration 1 | 38 |
| 8.2.4 | Stand-Alone Operation with Single External Power Supply 5.0 V: Minimum Configuration 2..... | 39 |
| 8.2.5 | Stand-Alone Operation with All External Power Supplies: Maximum Configuration | 40 |
| 8.2.6 | Operation on the Main Board: No External Supply | 41 |
| 9. | Precautions | 42 |
| 9.1 | Power-Off Sequence | 42 |
| 9.2 | CAN0RX is Shared with FLASH Programmer Signal FLMD1 | 42 |
| 9.3 | Power On Piggyback Board Without RH850 Microcontroller installed..... | 42 |
| 10. | Mechanical Dimensions..... | 43 |
| 11. | Schematics..... | 44 |
| 11.1 | Board Version D019450_06_V01 | 44 |
| 11.1.1 | Page 1 | 45 |
| 11.1.2 | Page 2 | 46 |
| 11.1.3 | Page 3..... | 47 |
| 11.1.4 | Page 4..... | 48 |
| 11.1.5 | Page 5..... | 49 |
| 11.2 | Board Version D019450_06_V02 | 50 |
| 11.2.1 | Page 1 | 51 |
| 11.2.2 | Page 2 | 52 |
| 11.2.3 | Page 3..... | 53 |
| 11.2.4 | Page 4..... | 54 |
| 11.2.5 | Page 5..... | 55 |

1. Overview

The RH850/U2A 156pin piggyback board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/U2A 156pin microcontrollers.

Notes

1. This document describes the functionality of the piggyback board and guides the user through its operation.
For details regarding the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document low active signals are marked by an appended 'Z' to the pin or signal name. E.g. the reset pin is named RESETZ.
3. In this document following abbreviations are used:
 - H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal

1.1 Package Components

The Y-RH850-U2A-156PIN-PB-T1-V1 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-U2A-156PIN-PB-T1-V1 package contains all of these items. *Table 1.1 Package Components for the Y-RH850-U2A-156PIN-PB-T1-V1* shows the packing components of the Y-RH850-U2A-156PIN-PB-T1-V1 package.

Table 1.1 Package Components for the Y-RH850-U2A-156PIN-PB-T1-V1

| Item | Description | Quantity |
|---------------------------------------|----------------------------------|--------------------|
| D019450 | RH850/U2A 156pin piggyback board | 1 |
| D019611 | Documentation CD | 1 |
| D010816-24 | China RoHS document | 1 |
| D010818-24 | WEEE+CE document | 1 |
| D019610-24 | Product contents list | 1 |
| Jumpers (2-way, 0.1") | In the bag | 30 (min. quantity) |
| Red Hirschmann 4 mm power lab sockets | In the bag | 1 |
| 16MHz Resonator | In the bag | 1 |
| 20MHz Resonator | In the bag | 1 |
| 24MHz Resonator | In the bag | 1 |

Note

Please keep the Y-RH850-U2A-156PIN-PB-T1-V1 packing box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original packing box when transporting the Y-RH850-U2A-156PIN-PB-T1-V1. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported Main Boards

This piggyback board can be used as a standalone board, or it can be mated with a main board. The following main boards are supported:

- Y-RH850-X1X-MB-T1-V1
- Y-RH850-X1X-MB-T2-V_x
- Y-RH850-X2X-MB-T1-V1
- Y-COMMON-MB-T1-V1

1.3 Main Features

- Burn-in socket for mounting of the device
- Several power set-up options
 - Combined operation with powering from main board
 - Stand-alone operation with single power supply (e.g. 3.3 V or 5.0 V only)
 - Stand-alone operation with flexible, individual power supply (typ. 1.12 V, 3.3 V, 5.0 V)
- Debugging and programming interface:
 - 14-pin LPD/JTAG Debug Connector (e.g. for using E2 OCD Emulator or PG-FP6 Flash Programmer)
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with an exchangeable 16/20/24/40 MHz Crystal Resonator
- General purpose signaling LEDs
- Jumpers for device mode selection and other configuration options
- Operating temperature from 0 °C to +40 °C

1.4 Piggyback Board Views

Following figures provide the top and bottom views of the piggyback board.

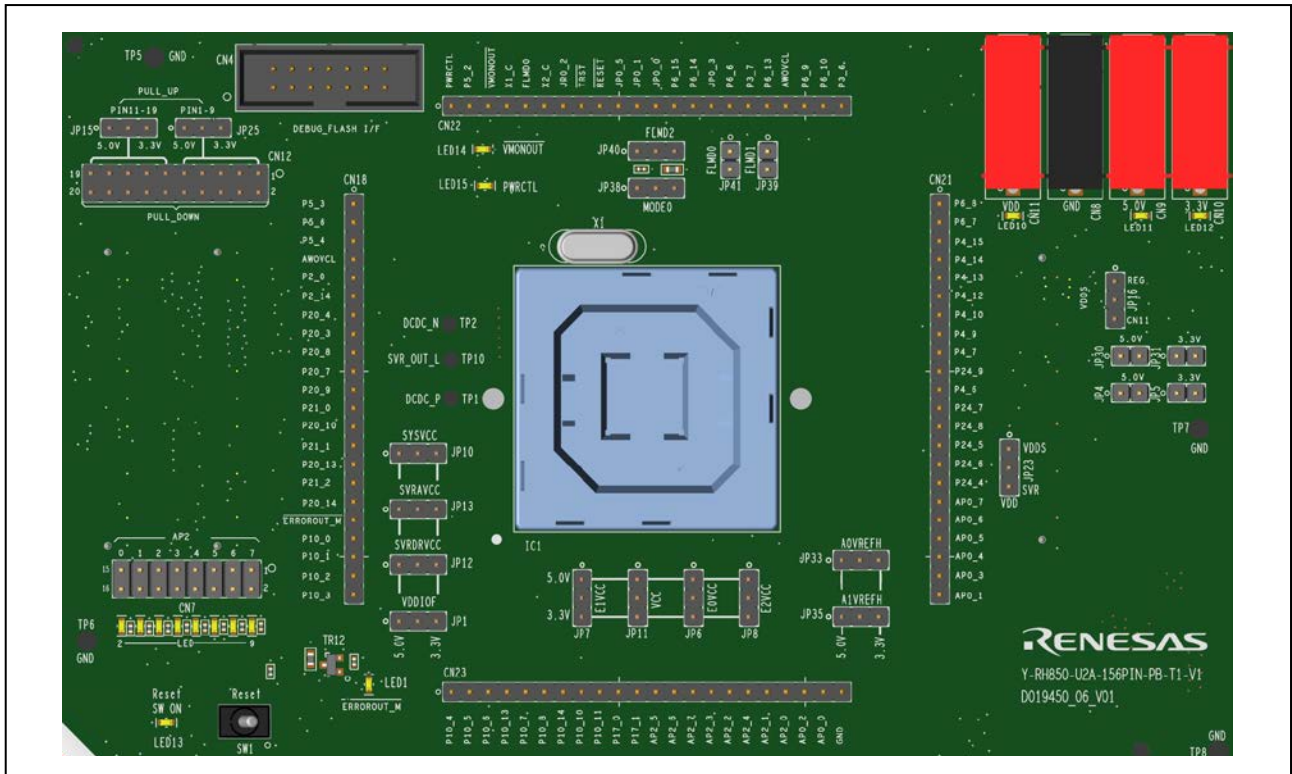


Figure 1.1 Piggyback board top view of board version D019450_06_V01

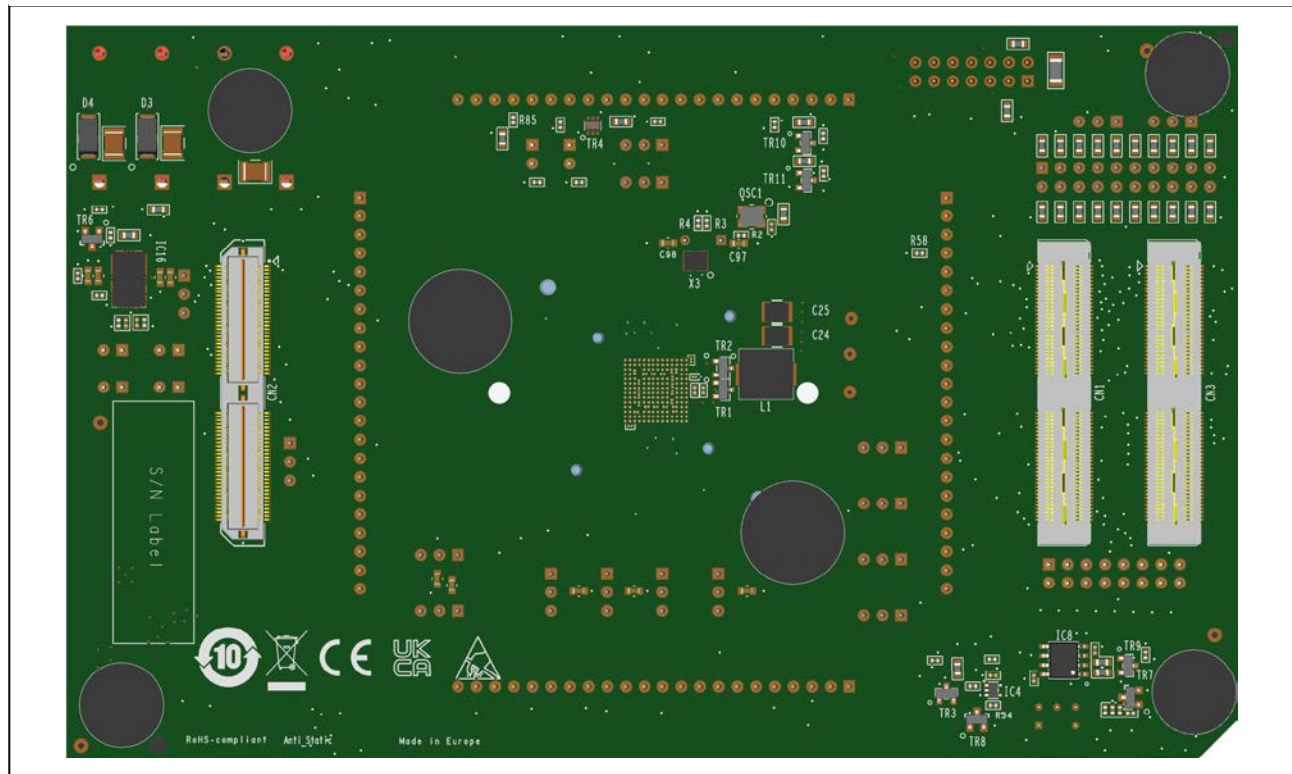


Figure 1.2 Piggyback board bottom view of board version D019450_06_V01

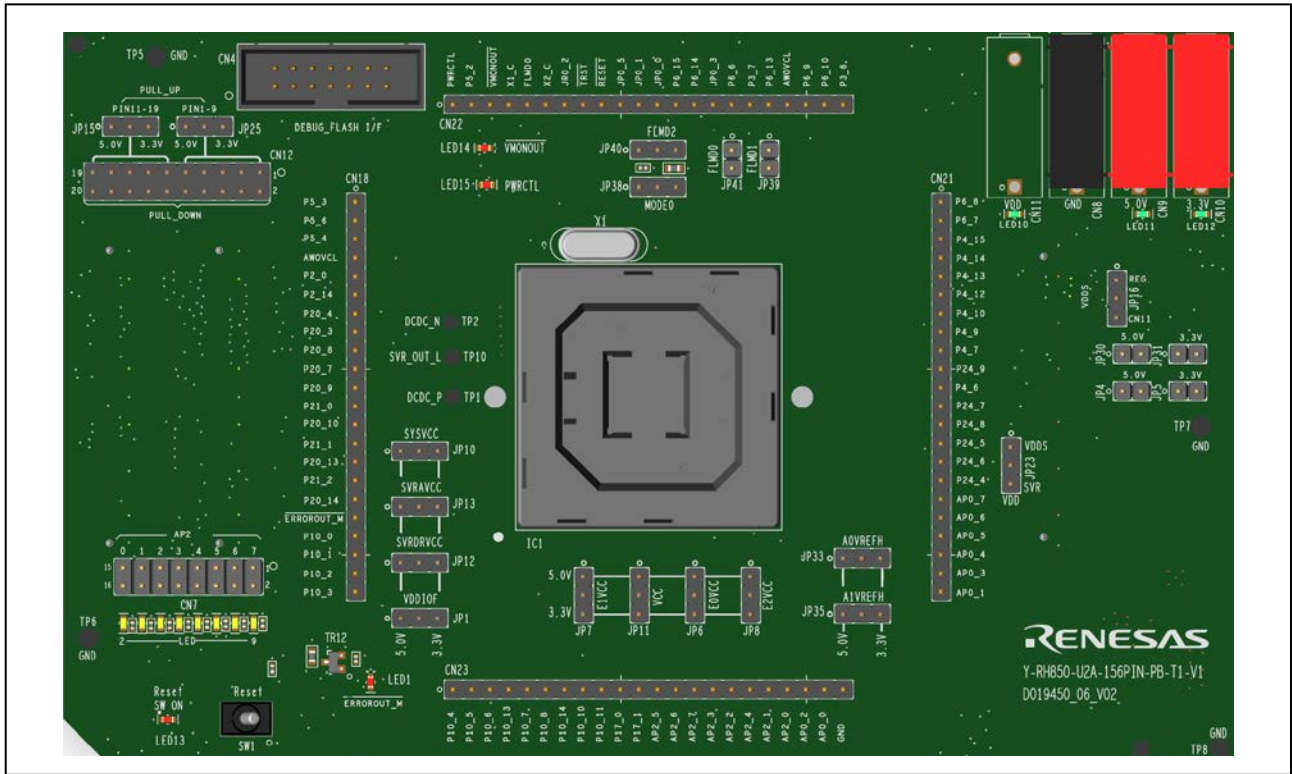


Figure 1.3 Piggyback board top view of board version D019450_06_V02

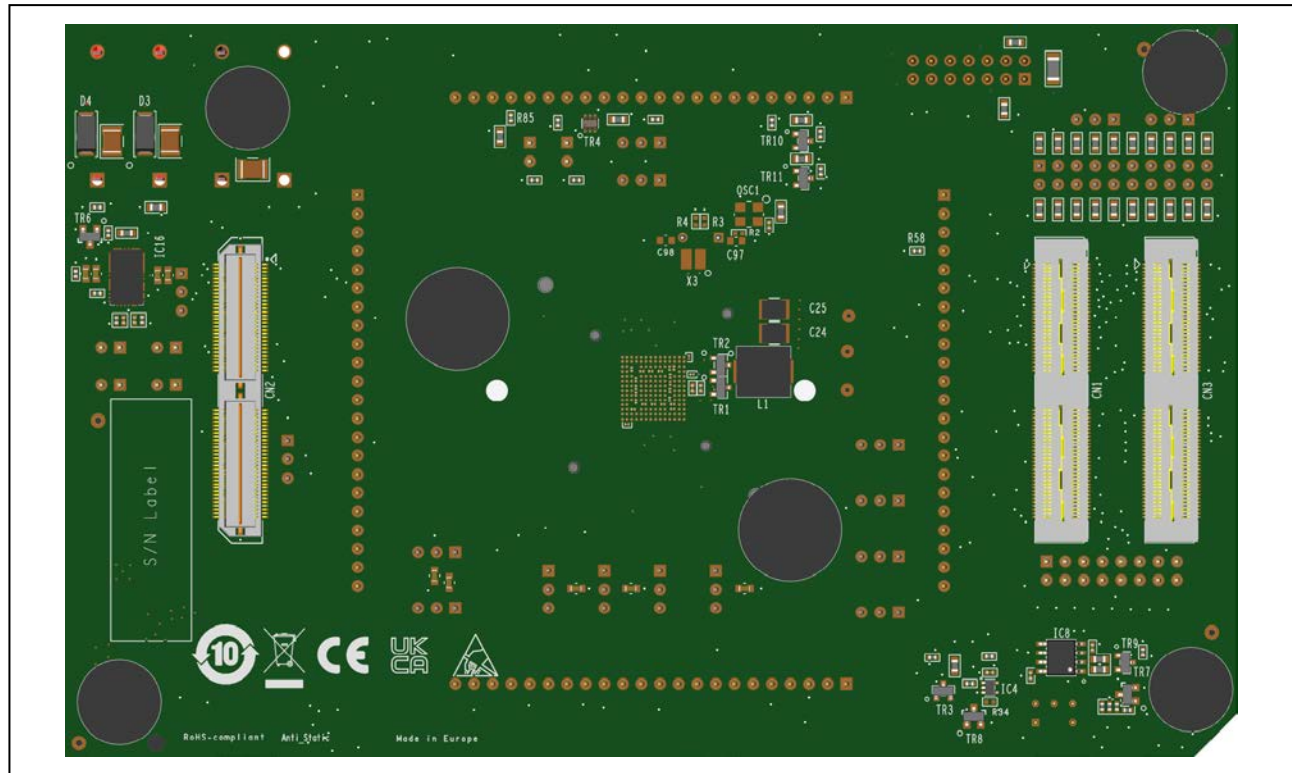


Figure 1.4 Piggyback board bottom view of board version D019450_06_V02

Following figures provide the drawing of top and bottom views of the piggyback board.

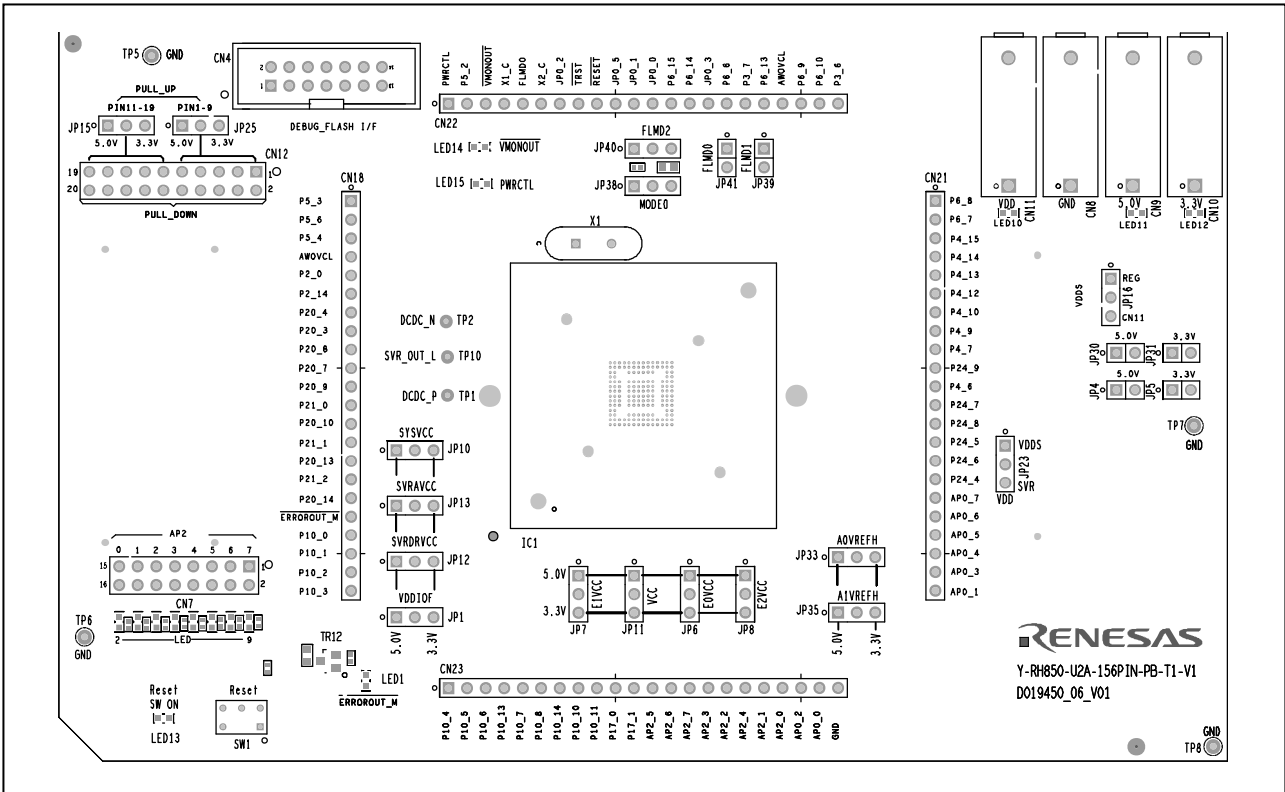
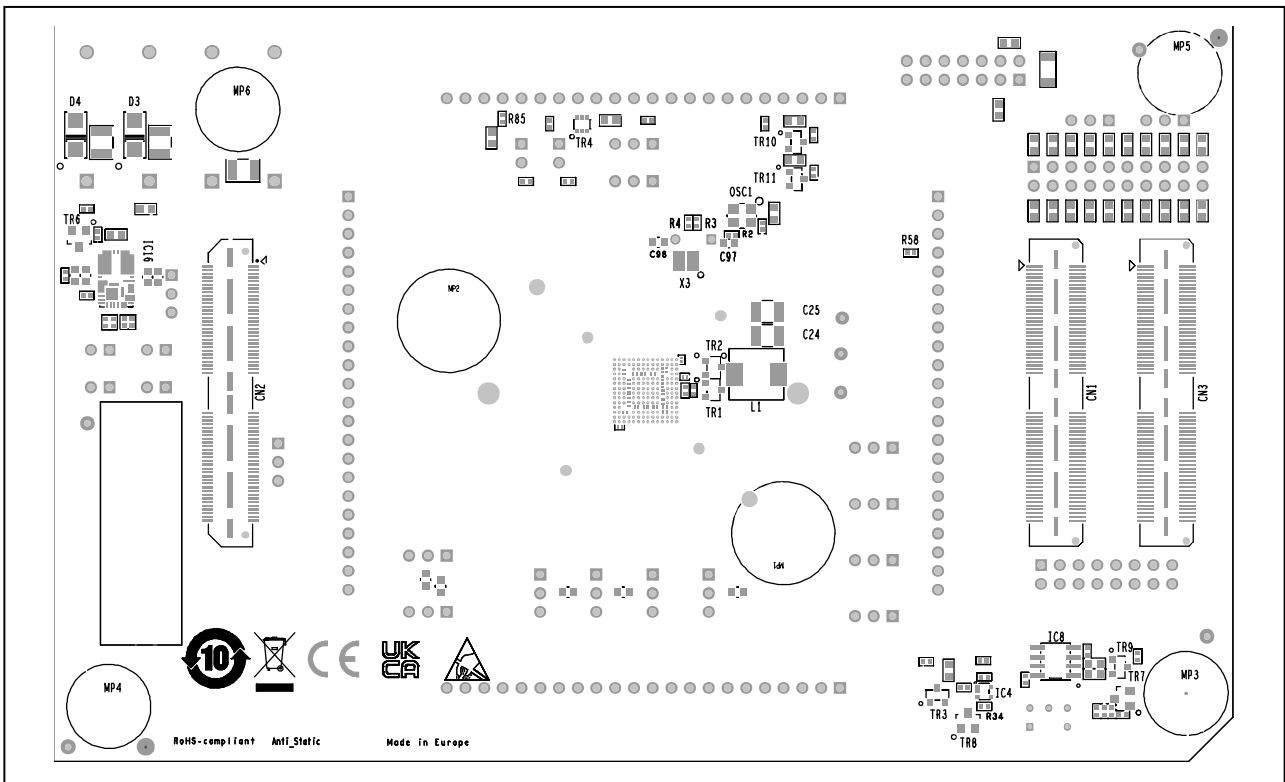


Figure 1.5 PiggyBack Board top view of board version D019450_06_V01



1.5 Mounting of the Device

The board is designed for use with the following device(s):

- R7F702302FABD (RH850/U2A6)

The device must be placed inside the socket IC1. To insert the device, align the device pin 1 with the marking of the socket.

Pin 1 of the socket is on the side with the “IC1” label (see also white point in *Figure 1.1 Piggyback board top view* and in *Figure 1.5 Yamaichi socket NP378-156-190-YD*).

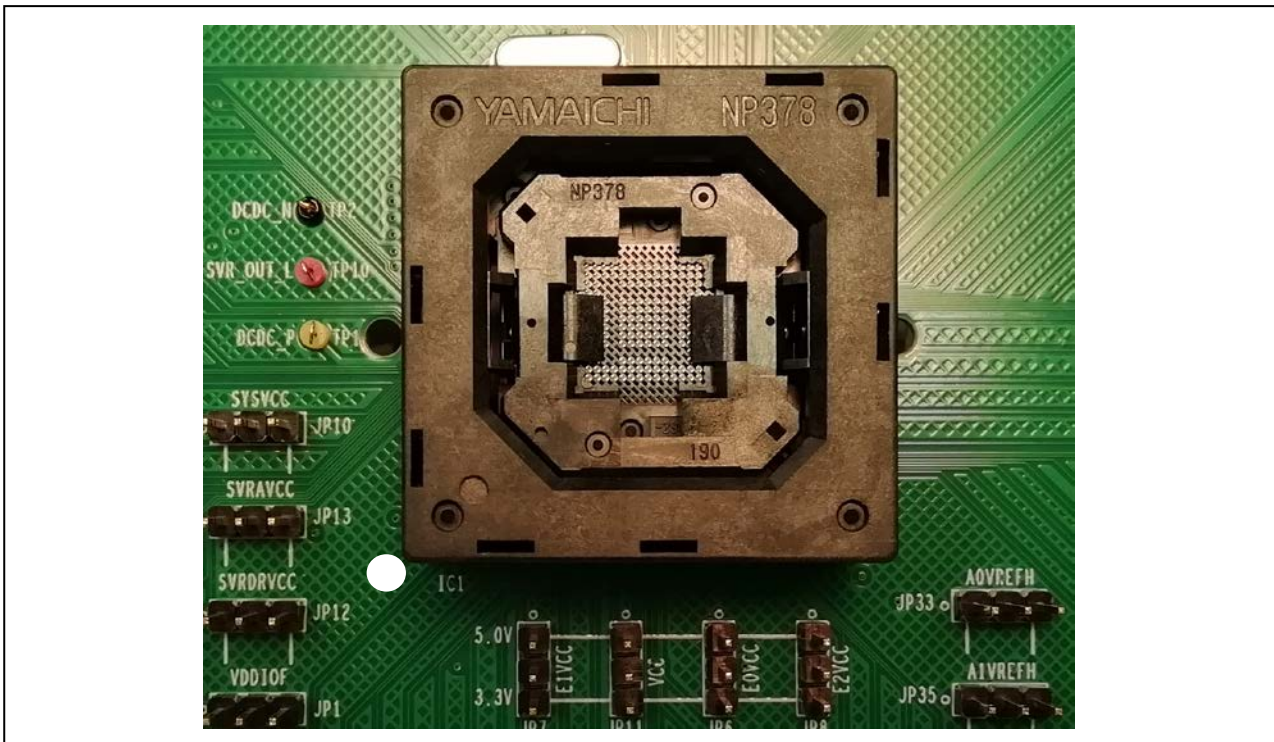


Figure 1.9 Yamaichi socket NP378-156-190-YD

CAUTION

Be careful with the device placement in the socket to avoid damage of the device.

2. Jumpers, Connectors, Switches and LEDs

This section provides complete lists of all jumpers, connectors, and LEDs.

The placement of these components on the board is depicted in the figure below.

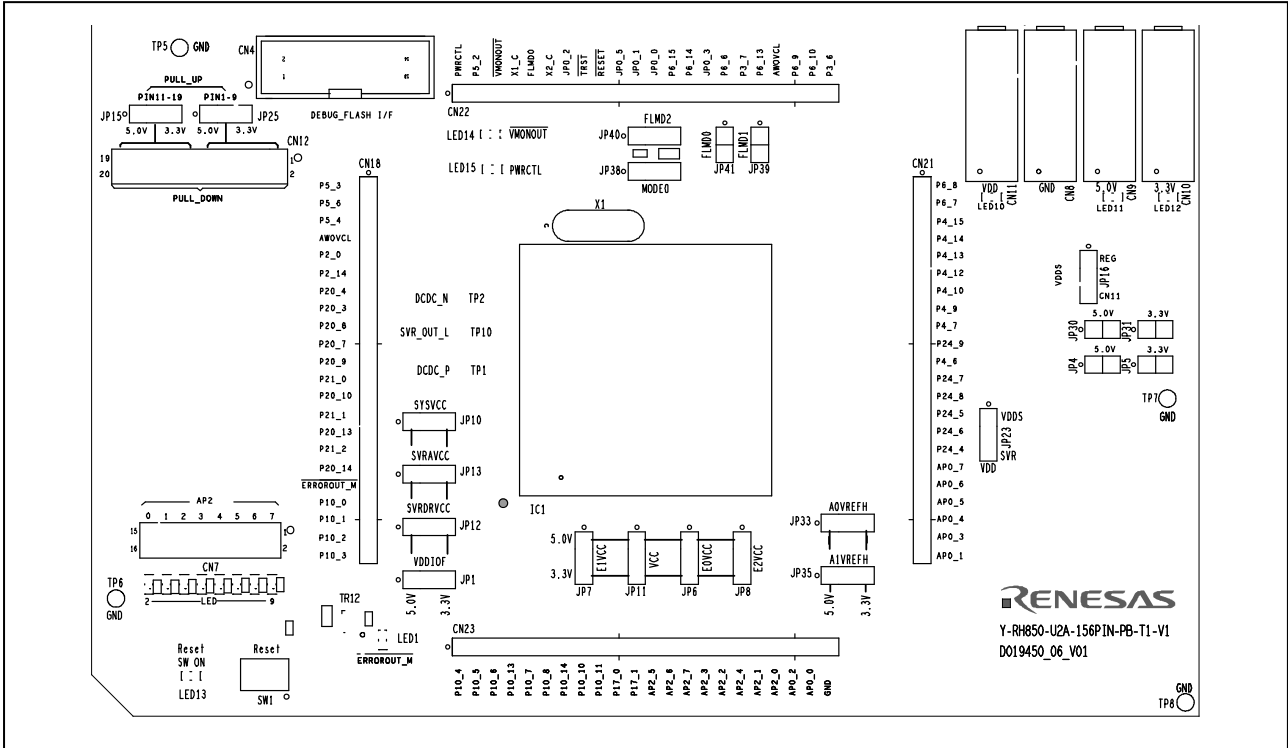


Figure 2.1 Placement of jumpers, connectors and LEDs on top side of board version D019450_06_V01

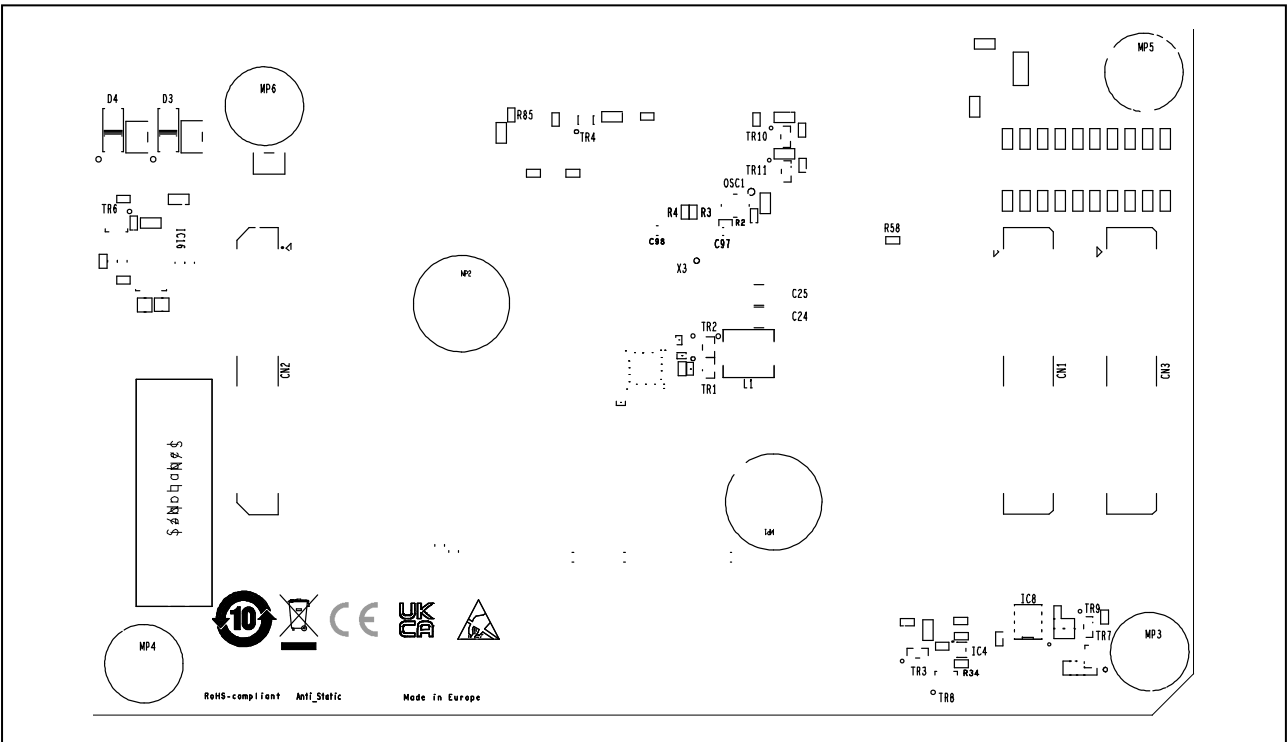


Figure 2.2 Placement of connectors on bottom side of board version D019450_06_V01

2.1 Jumper Overview

The following table provides an overview of all jumpers.

Table 2.1 Jumper overview

| Jumper | Function | Remark | |
|--------|--|--|---|
| JP1 | Voltage selection for VDDIOF <ul style="list-style-type: none"> JP1[2-1]: 5.0 V JP1[2-3]: 3.3 V | refer to 3.2 <i>Voltage Distribution</i> | |
| JP4 | Current measurement bridge of 5.0 V power rail | refer to 3.4 <i>Current Measurement Bridges</i> | |
| JP5 | Current measurement bridge of 3.3 V power rail | | |
| JP6 | Voltage selection for E0VCC <ul style="list-style-type: none"> JP6[2-1]: 5.0 V JP6[2-3]: 3.3 V | refer to 3.2 <i>Voltage Distribution</i> | |
| JP7 | Voltage selection for E1VCC <ul style="list-style-type: none"> JP7[2-1]: 5.0 V JP7[2-3]: 3.3 V | | |
| JP8 | Voltage selection for E2VCC <ul style="list-style-type: none"> JP8[2-1]: 5.0 V JP8[2-3]: 3.3 V | | |
| JP10 | Voltage selection for SYSVCC <ul style="list-style-type: none"> JP10[2-1]: 5.0 V JP10[2-3]: 3.3 V | | |
| JP11 | Voltage selection for VCC <ul style="list-style-type: none"> JP11[2-1]: 5.0 V JP11[2-3]: 3.3 V | | |
| JP12 | Voltage selection for SVRDRVCC <ul style="list-style-type: none"> JP12[2-1]: 5.0 V JP12[2-3]: 3.3 V | | |
| JP13 | Voltage selection for SVRAVCC <ul style="list-style-type: none"> JP13[2-1]: 5.0 V JP13[2-3]: 3.3 V | | |
| JP15 | Voltage selection for Pull-up/Pull-down pin header CN12 pins 11, 13, 15, 17, 19 <ul style="list-style-type: none"> JP15[2-1]: 5.0 V JP15[2-3]: 3.3 V | | refer to 6.4 <i>Pull-Up/Pull-Down Pin Header</i> |
| JP16 | Voltage selection for 1.12 V VDDs <ul style="list-style-type: none"> JP16[2-1]: reg_vcc_VDD JP16[2-3]: IN_1v12 | | refer to 3.3 <i>Device Core Voltage (VDD) Selection</i> |
| JP23 | Voltage selection for VDD <ul style="list-style-type: none"> JP23[2-1]: VDDs JP23[2-3]: SVR_OUTPUT | | |
| JP25 | Voltage selection for Pull-up/Pull-down pin header CN12 pins 1, 3, 5, 7, 9 <ul style="list-style-type: none"> JP25[2-1]: 5.0 V JP25[2-3]: 3.3 V | refer to 6.4 <i>Pull-Up/Pull-Down Pin Header</i> | |

Table 2.1 Jumper overview (cont'd)

| Jumper | Function | Remark |
|--------|--|---|
| JP30 | Current measurement bridge of 5.0 V A/D Converter power supply | refer to 3.4 <i>Current Measurement Bridges</i> |
| JP31 | Current measurement bridge of 3.3 V A/D Converter power supply | |
| JP33 | Voltage selection for A0VREFH <ul style="list-style-type: none"> • JP33[2-1]: 5.0 V • JP33[2-3]: 3.3 V | refer to 3.2 <i>Voltage Distribution</i> |
| JP35 | Voltage selection for A1VREFH <ul style="list-style-type: none"> • JP35[2-1]: 5.0 V • JP35[2-3]: 3.3 V | |
| JP38 | MODE0 level selection | refer to 6.1 <i>Operation Mode Selection</i> |
| JP39 | FLMD1 level selection | |
| JP40 | FLMD2 level selection | |
| JP41 | FLMD0 level selection | |

2.2 Connector Overview

The following table provides an overview of all connectors.

Table 2.2 Connector overview

| Connector | Function | Remark |
|-----------|---------------------------------|---|
| CN1 | Main Board connectors | refer to 7.1 <i>Connectors to the Main Board CN1 to CN3</i> |
| CN2 | | |
| CN3 | | |
| CN4 | Debug connector | refer to 5 <i>Debug and Flash Programming Interfaces</i> and 7.2 <i>Debug Connector CN4</i> |
| CN7 | Signaling LEDs pin header | refer to 6.3 <i>Signaling LEDs</i> |
| CN8 | GND for external power supply | refer to 3.1 <i>Board Power Connection</i> , connector CN11 is not assembled on the board |
| CN9 | +5.0 V external power supply | |
| CN10 | +3.3 V external power supply | |
| CN11 | +1.12 V external power supply * | |
| CN12 | Pull-up/Pull-down pin header | refer to 6.4 <i>Pull-Up/Pull-Down Pin Header</i> and 7.3 <i>Pull-Up/Pull-Down Pin Header CN12</i> |
| CN18 | Device ports connectors | refer to 7.4 <i>Device Ports Connectors CN18 and CN21 to CN23</i> |
| CN21 | | |
| CN22 | | |
| CN23 | | |

Note: * Refer to 3.3 *Device Core Voltage (VDD) Selection* for further details about VDD voltage.

2.3 LED Overview

The following table provides an overview of all LED.

Table 2.3 LED overview

| LED | Function | Color | Remark |
|-------|--------------------------------|--------|--|
| LED1 | Device ERROROUT_M signal | red | |
| LED2 | Signaling LED | yellow | connection via CN7, refer to 6.3 Signaling LEDs |
| LED3 | Signaling LED | | |
| LED4 | Signaling LED | | |
| LED5 | Signaling LED | | |
| LED6 | Signaling LED | | |
| LED7 | Signaling LED | | |
| LED8 | Signaling LED | | |
| LED9 | Signaling LED | | |
| LED10 | 1.12 V device core voltage VDD | green | refer to 3.5 Power Supply LEDs |
| LED11 | 5.0 V power supply P5V0 | green | |
| LED12 | 3.3 V power supply P3V3 | green | |
| LED13 | Reset switch SW1 on | red | |
| LED14 | Device VMONOUT signal | red | |
| LED15 | Device PWRCTL signal | red | |

3. Power Supply

3.1 Board Power Connection

The device and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board
- 5 V in case some ports shall be operated with 5 V I/O voltage
- 1.12 V for the device's VDD core voltage supply
Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Note

Within this document all voltage values are considered as 'typical'.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

The following connectors are available to supply external voltages:

- Four 4 mm 'banana-type' connectors are used to connect external power supplies:
 - black connector CN8 for GND (VSS)
 - red connector CN9 for 5 V
 - red connector CN10 for 3.3 V
 - red connector CN11 for 1.12 V
Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Connector CN11 is not assembled at delivery of the board, but separately supplied with the board package.

In case the piggyback board is mounted on a Main Board, all voltages except for 1.12 V (VDD) are supplied by the Main Board.

CAUTION

Do not power on the piggyback board when no RH850 microcontroller is installed in socket IC1 because the switching regulator in the SVR power supply circuit doesn't have defined control signals when the microcontroller is not installed and may be damaged.

If you want to power on the piggyback board without microcontroller, make sure jumper JP12[1-2-3] (SVRDRVCC) is open.

Do not supply the 5 V (CN9) and 3.3 V (CN10) voltage directly to the piggyback board in case it is mounted on the Main Board.

Connecting external 1.12 V via CN11 (and GND via CN8) is still an option also in this case.

For some general power supply scenarios, the jumper settings are described in *8 Jumper Configuration Examples*.

3.2 Voltage Distribution

The following table shows the required device power supply pins and their function:

Table 3.1 Device power supply pins

| Device power supply pin | Voltage | Function |
|-------------------------|------------|--|
| E0VCC, E1VCC, E2VCC | 3.3 V, 5 V | Power supply for I/O ports |
| SYSVCC | 3.3 V, 5 V | Power supply for System Logic and internal voltage regulator power I/O ports |
| VCC | 3.3 V, 5 V | Power supply for on-chip flash memory |
| SVRDRVCC | 3.3 V, 5 V | Power supply for on-chip Switching Voltage Regulator (SVR) |
| SVRAVCC | 3.3 V, 5 V | |
| VDDIOF | 3.3 V, 5 V | I/O voltage supply for the Main Board |
| A0VREFH, A1VREFH | 3.3 V, 5 V | A/D Converter's reference voltages |
| VDD | 1.12 V * | Core supply voltage |

Note: * Refer to 3.3 Device Core Voltage (VDD) Selection for further details about VDD voltage.

Each of the above voltages can be selected from

- 5.0 V, 3.3 V (where applicable, see table above)

by a set of jumpers. For details refer to *Figure 3.1 Voltage distribution* and *Table 2.1 Jumper overview*

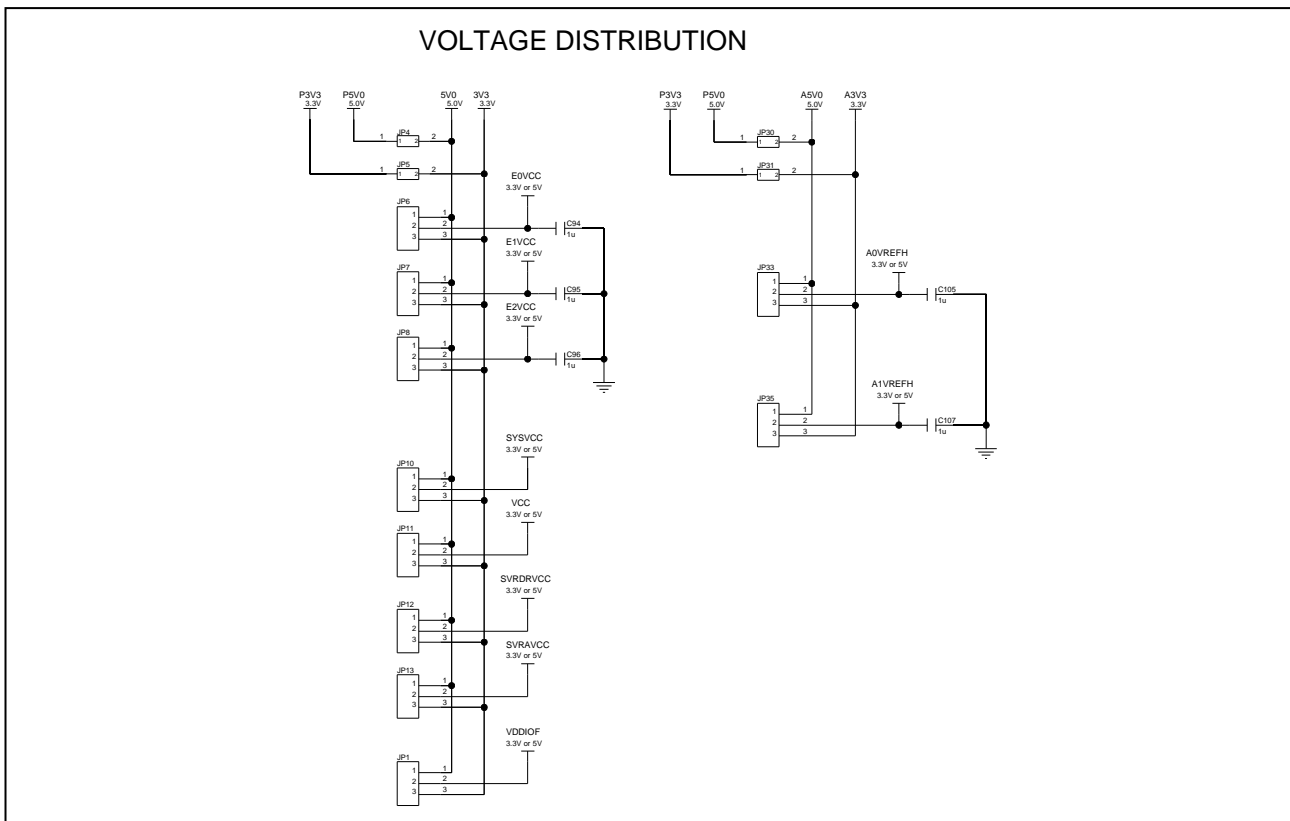


Figure 3.1 Voltage distribution

3.3 Device Core Voltage (VDD) Selection

The device core voltage VDD (typ.1.12 V) can be

- supplied from external via CN11 (voltage IN_1v12)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC16 (voltage reg_vcc_VDD)
- generated by the on-chip Switching Voltage Regulator (SVR) in combination with device external power transistors TR1, TR2 (voltage SVR_OUTPUT)

Note

The IN_1v12 and reg_vcc_VDD voltages have a level of typical 1.12 V, which is higher than the typical device core voltage VDD of 1.09 V. The 30 mV difference is supposed to compensate voltage drops over the power rails on the board, in particular over the jumpers.

Selection of the VDD source is achieved by use of the jumpers JP23 and JP16:

- JP23[2-1]: VDD = 1.12 V (VDDs) from
 - JP16[2-1]: VDDs = reg_vcc_VDD from on-board voltage regulator IC16
 - JP16[2-3]: VDDs = IN_1v12 from external supply CN11
- JP23[2-3]: VDD = 1.09 V (SVR_OUTPUT)

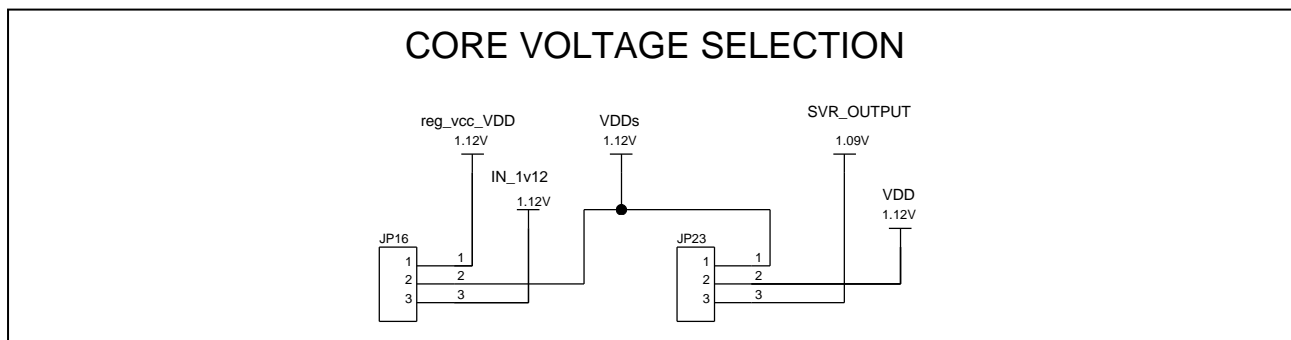


Figure 3.2 Device core voltage (VDD) selection

3.4 Current Measurement Bridges

The total current of the 5V0 and 3V3 power rails can be measured by replacing the jumpers JP4 and JP5 with a current meter.

Accordingly, the total current via the A/D Converter's supply voltages A5V0 and A3V3 can be measured via the jumpers JP30 and JP31 respectively.

The current of particular power supply pins of the device can be measured via their respective supply selection jumpers, refer to *Figure 3.1 Voltage distribution*.

3.5 Power Supply LEDs

The following green LEDs indicate the presence of various voltages on the piggyback board:

- LED10 for 1.12 V device core voltage VDD
- LED11 for 5.0 V power rail P5V0
- LED12 for 3.3 V power rail P3V3

4.2 Programmable Oscillator

Instead of using the on-chip main oscillator a programmable crystal oscillator (OSC1) circuit can be soldered on the board.

The available footprint and circuitry is designed for a SG-8018CE programmable crystal oscillator from Seiko Epson. The output of this oscillator can be connected to X1 terminal via resistor R2.

The SG-8018CE is neither mounted on nor provided with the board. For details about the available circuitry, refer to *Figure 4.1 Clock supply*.

CAUTION

A resonator mounted on socket X1 or soldered on X3 must not be used in parallel to another clock source.

4.3 X1 and X2 on CN22

To minimize disturbance on the resonator signal the device pins X1 and X2 are by default not connected to a pin header. If needed the pins can be connected to CN22 via 0 Ω resistors:

- X1: Pin 4 of CN22 to supply an external clock to the device via R3
- X2: Pin 6 of CN22 for measurement purposes of the clock via R4

5. Debug and Flash Programming Interfaces

For debugging and flash programming purposes debug and flash programming tools can be connected to the CN4 connector.

Refer to 7.2 *Debug Connector CN4* for details about the CN4 pin assignment.

The Renesas standard emulator for RH850/U2A is the E2 emulator. This can be used as emulator for debugging or as flash programmer.

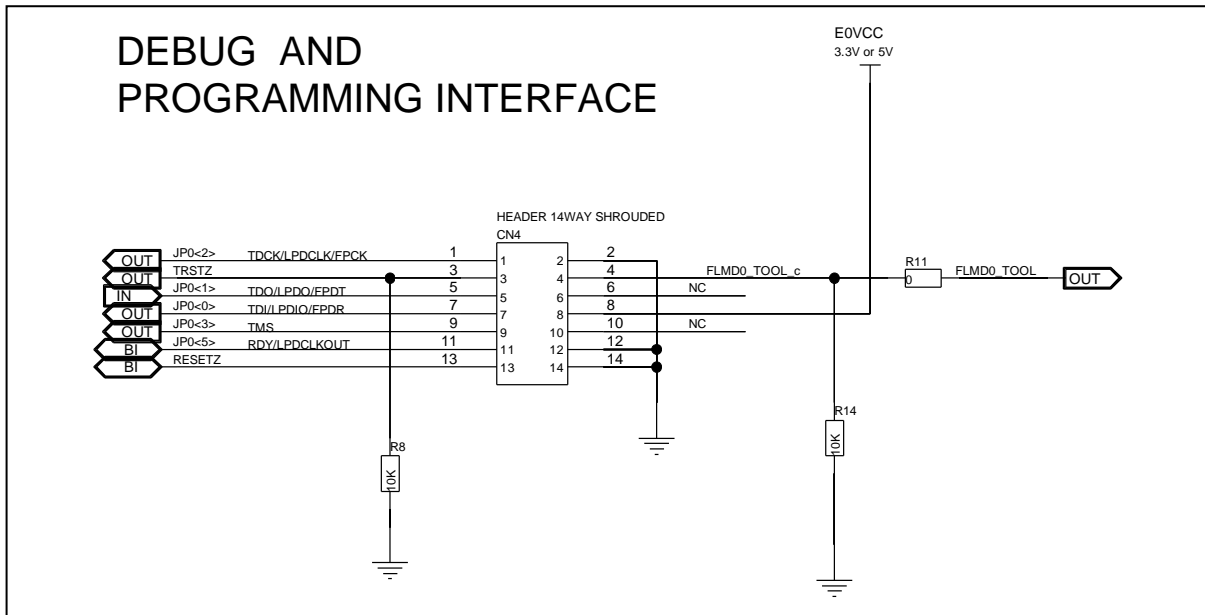


Figure 5.1 Debug interface

6. Other Circuitry

6.1 Operation Mode Selection

The piggyback board gives the possibility to configure the following jumpers for selection of the device operation mode:

Table 6.1 Device operation mode selection jumpers

| Jumper | Function |
|--------|---|
| JP38 | MODE0 pin level <ul style="list-style-type: none"> • JP38[2-1]: MODE0 = H level • JP38[2-3]: MODE0 = GND |
| JP41 | FLMD0 pin level <ul style="list-style-type: none"> • JP41[SHORT]: FLMD0 = H level • JP41[OPEN]: FLMD0 <ul style="list-style-type: none"> – controlled by debugger or programming tool if a tool is connected via CN4 – GND, if no tool connected |
| JP39 | FLMD1 pin level <ul style="list-style-type: none"> • JP39[SHORT]: FLMD1 = H level • JP39[OPEN]: FLMD1 = GND |
| JP40 | FLMD2 pin level <ul style="list-style-type: none"> • JP40[2-1]: FLMD2 = H level • JP40[2-3]: FLMD2 = GND |

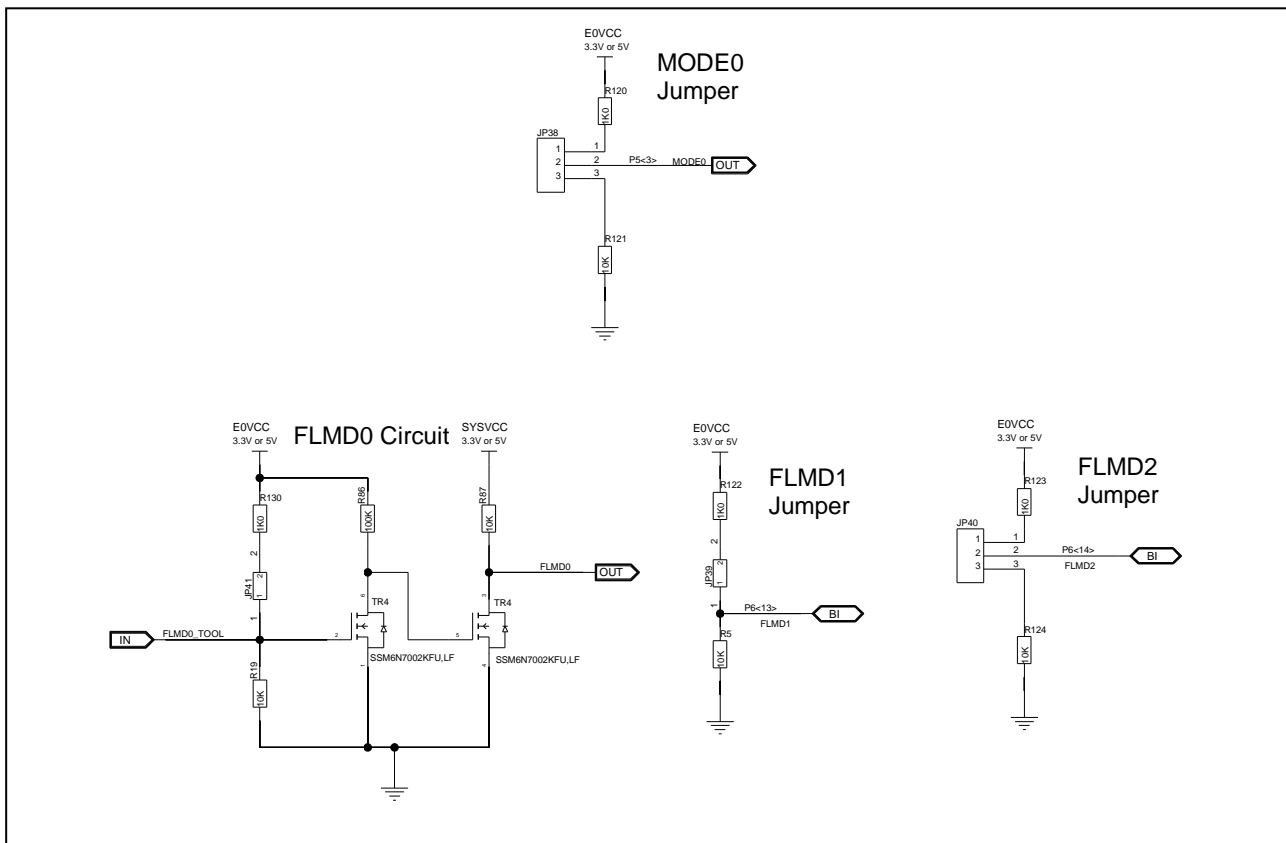


Figure 6.1 Operating mode selection

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User's Manual for details, which modes are specified for the used device.

Note

In most cases the 'normal operating mode' of the device will be used.

This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the 'normal operating mode' of the device, the FLMD0 pin must be pulled low. To do so, remove the jumper JP41.

All other jumpers related to the mode selection can be left open.

6.2 RESET Switch

The SW1 is used to issue a RESET to the device.

The SW1 toggle switch allows to activate the RESET in two different ways:

- SW1 in left '5-4 (ON)' position: temporary reset
Releasing the switch's lever returns the switch to its middle 'OFF' position and thus releases the reset.
- SW1 in right '5-6 ON' position: permanent reset
For reset release the switch has to be moved back manually to its middle 'OFF' position.

The left and right switch position is defined from the side of the part number marking, which is highlighted with a red arrow in *Figure 6.3 Operation of RESET switch*.

The lighted red LED13 indicates that SW1 is "on", i.e. in position '5-4 (ON)' or '5-6 ON'.

Note

LED13 does not light up when RESET is asserted by any other means than SW1.

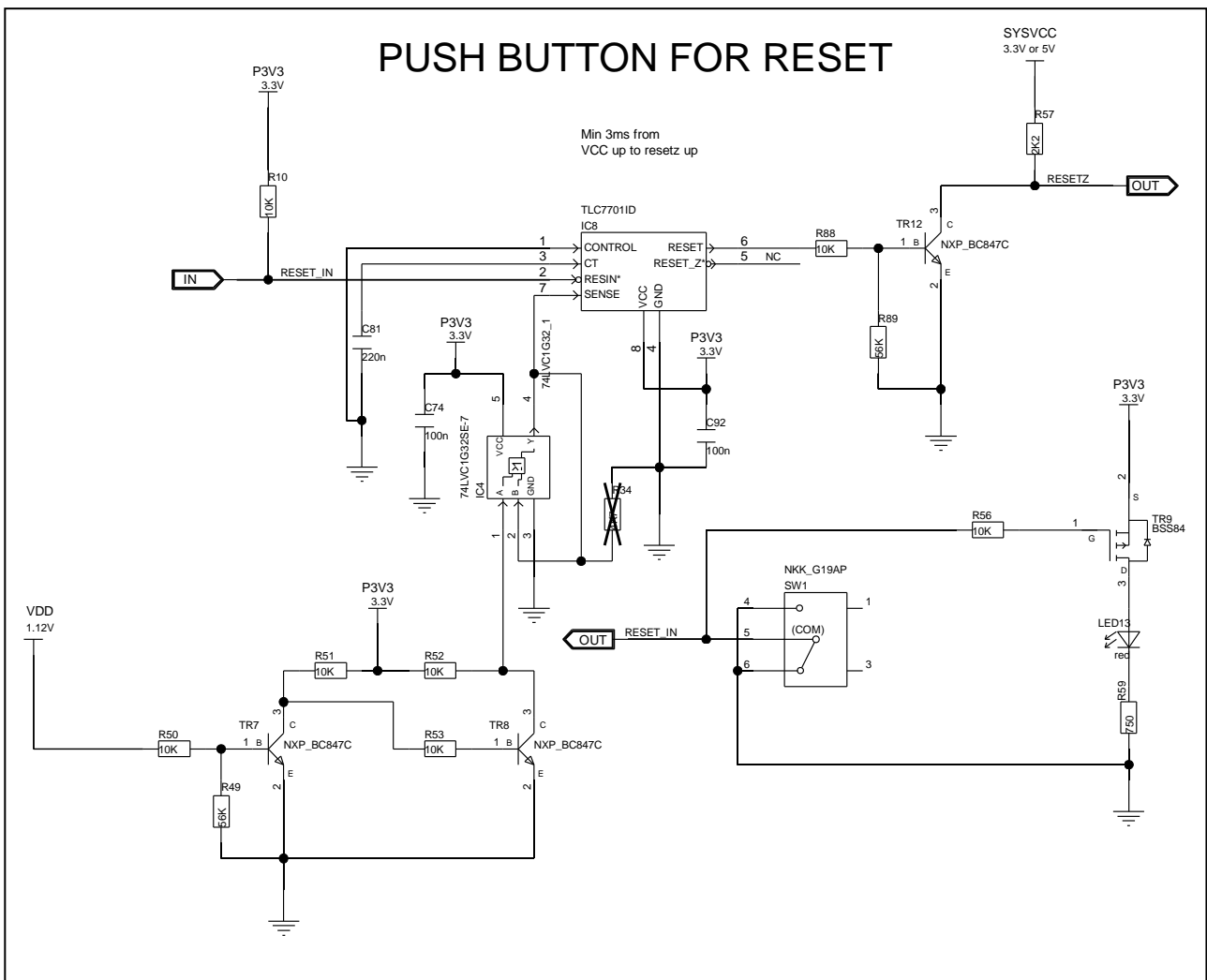


Figure 6.2 Reset circuit

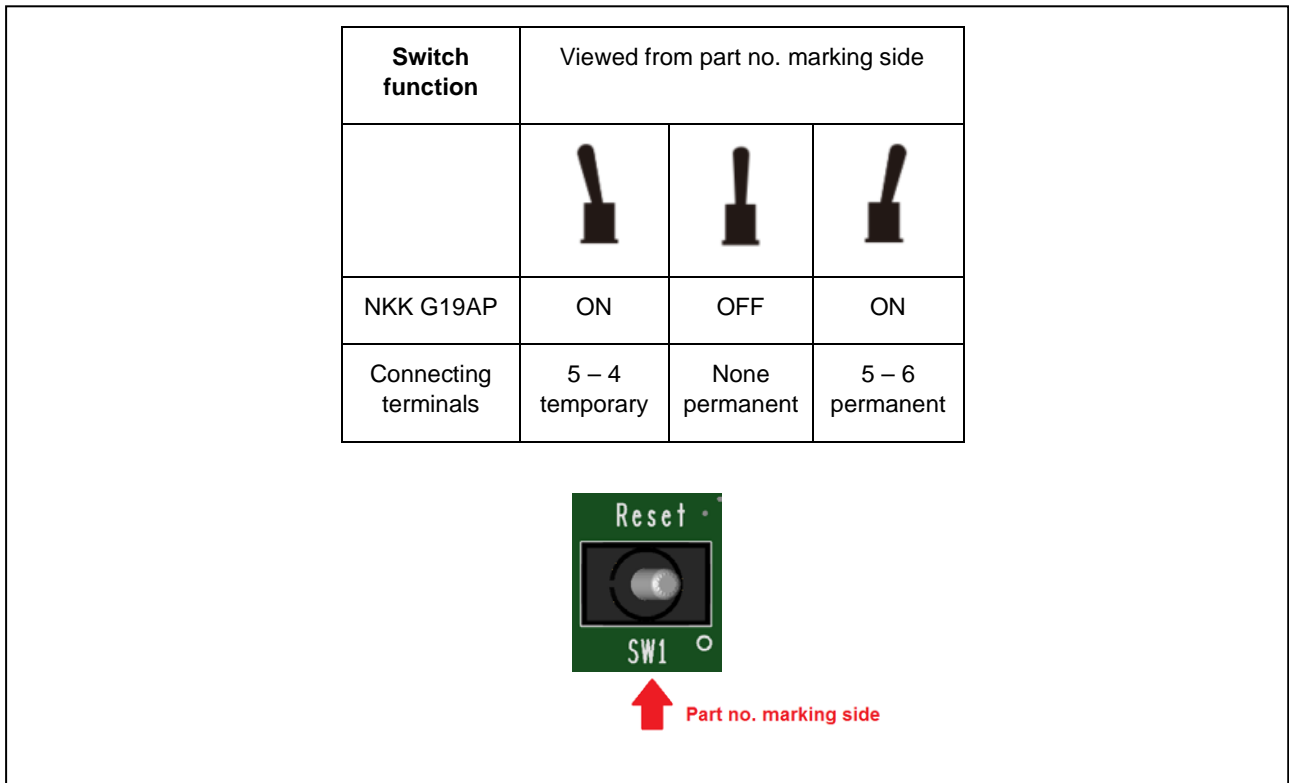


Figure 6.3 Operation of RESET switch

6.3 Signaling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins.

Device pins AP2_0 to AP2_7 are connected to the odd pins of the pin header CN7, while the LEDs 2 to 9 are connected to the even CN7 pins.

Thus, the LEDs can be either connected to

- the device pins AP2_0 to AP2_7 by closing the connection on CN7 using a jumper, or
- any device pin by connecting directly with the even CN7 pins using a separate cable.

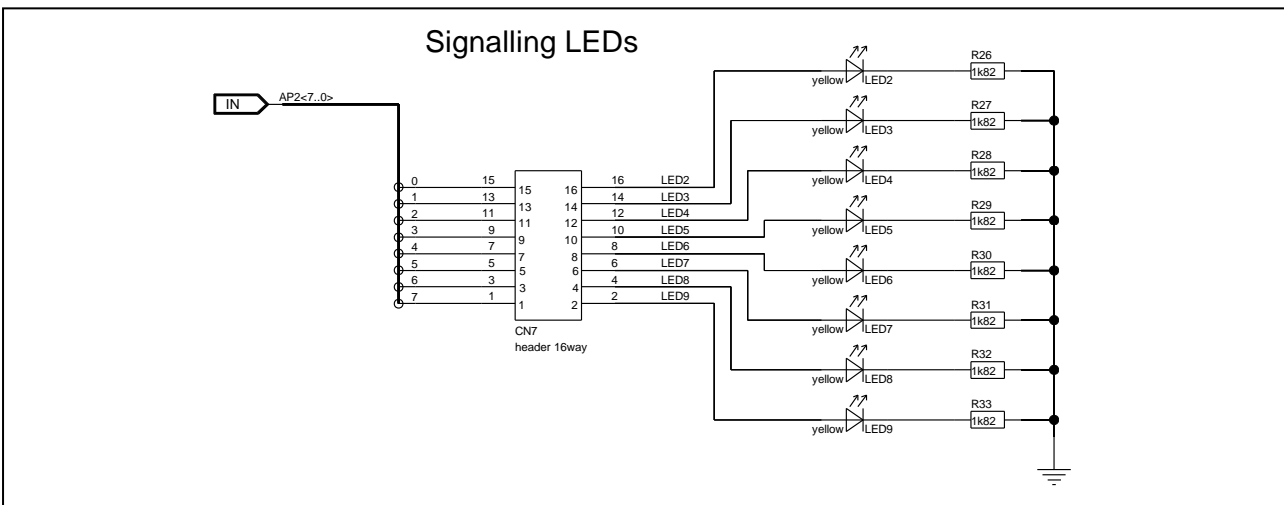


Figure 6.4 Signalling LED circuit

6.4 Pull-Up/Pull-Down Pin Header

The Pull-up/Pull-down pin header CN12 provides fixed voltage levels at its pins, that can be used to pull-up/pull-down a signal on the board or the device, respectively, by connecting a CN12 pin to the signal via a separate cable.

The CN12 pins have following pull-up or pull-down voltage levels:

- all even numbered pins are connected to L level, i.e. to GND
- odd numbered pins 1, 3, 5, 7, 9 can be connected to
 - 5.0 V, if JP25[2-1] is set
 - 3.3 V, if JP25[2-3] is set
- odd numbered pins 11, 13, 15, 17, 19 can be connected to
 - 5.0 V, if JP15[2-1] is set
 - 3.3 V, if JP15[2-3] is set

Refer to 7.3 Pull-Up/Pull-Down Pin Header CN12 for CN12 details.

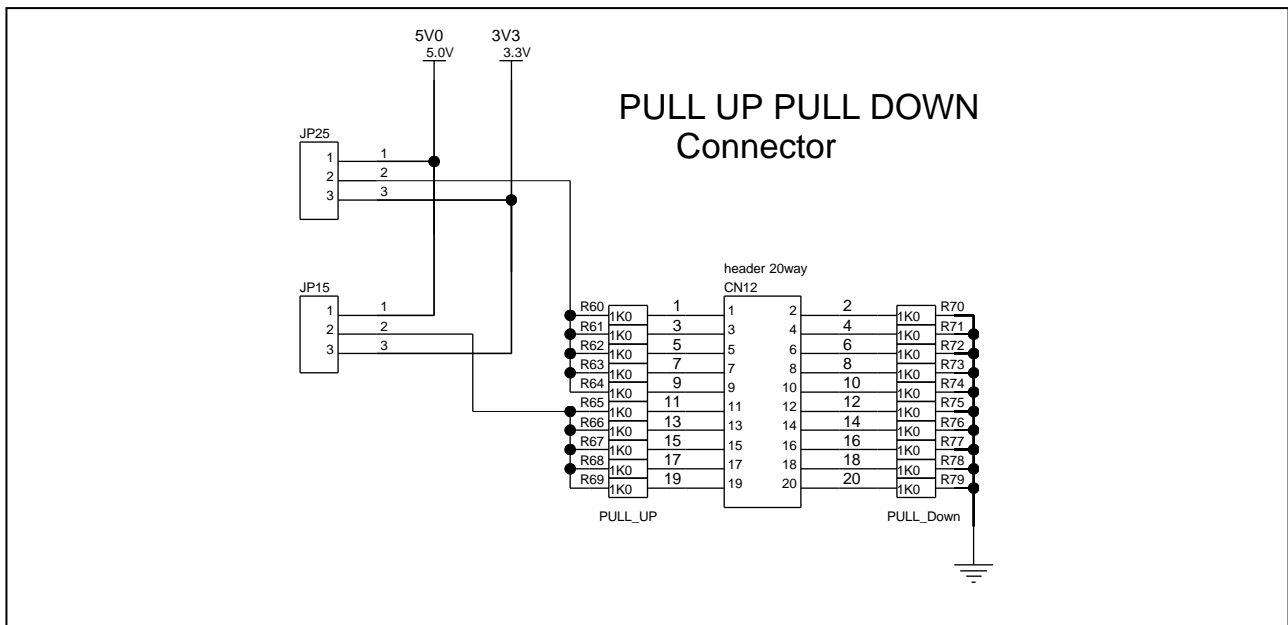


Figure 6.5 Pull-up / pull-down circuit

7. Connectors

7.1 Connectors to the Main Board CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the piggyback board to a Main Board. The signals of each connector are summarized in the following tables.

Note

Regarding the function on the Main Board, please refer to the User's Manual of any supported Main Board. Refer to *1.2 Supported Main Boards* for a list of supported Main Boards.

7.1.1 Main Board Connector CN1

Table 7.1 Main board connector CN1

| Pin | Main Board function | Piggyback board device port |
|-----|---------------------|-----------------------------|
| 1 | VDDA | – |
| 3 | VDDA | – |
| 5 | RESET | RESETZ |
| 7 | WAKE | – |
| 9 | INT0 | P10_7 |
| 11 | INT2 | P3_7 |
| 13 | – | – |
| 15 | UART0TX | P6_13 |
| 17 | UART0RX | P6_14 |
| 19 | LIN0TX | P20_7 |
| 21 | LIN0RX | P20_14 |
| 23 | IIC0SCL | P10_1 |
| 25 | IIC0SDA | P10_0 |
| 27 | CAN0TX | P6_14 |
| 29 | CAN0RX | P6_13 |
| 31 | SENT0RX | P10_7 |
| 33 | SENT0SPCO | P6_14 |
| 35 | PSI5SRX0 | P3_6 |
| 37 | PSI5STX0 | P3_7 |
| 39 | PSI5SCLK0 | – |
| 41 | FLX0TX | P10_4 |

| Pin | Main Board function | Piggyback board device port |
|-----|---------------------|-----------------------------|
| 2 | VDDA | – |
| 4 | VDDA | – |
| 6 | NMI | P4_7 |
| 8 | – | – |
| 10 | INT1 | P24_4 |
| 12 | INT3 | P5_4 |
| 14 | – | – |
| 16 | UART1TX | P6_15 |
| 18 | UART1RX | P6_9 |
| 20 | LIN1TX | P6_13 |
| 22 | LIN1RX | P6_14 |
| 24 | IIC1SCL | P24_9 |
| 26 | IIC1SDA | P24_8 |
| 28 | CAN1TX | P4_9 |
| 30 | CAN1RX | P4_10 |
| 32 | SENT1RX | P20_3 |
| 34 | SENT1SPCO | P20_9 |
| 36 | PSI5RX0 | P5_4 |
| 38 | PSI5TX0 | P5_6 |
| 40 | – | – |
| 42 | FLX0EN | P10_2 |

Table 7.1 Main board connector CN1 (cont'd)

| Pin | Main Board function | Piggyback board device port |
|-----|---------------------|-----------------------------|
| 43 | FLX0RX | P20_14 |
| 45 | FLX1TX | P10_3 |
| 47 | FLX1RX | P10_0 |
| 49 | – | – |
| 51 | ETH0MDIO | – |
| 53 | ETH0RXD0 | – |
| 55 | ETH0RXD1 | – |
| 57 | ETH0RXD2 | – |
| 59 | ETH0RXD3 | – |
| 61 | ETH0RXCLK | – |
| 63 | ETH0RXER | – |
| 65 | ETH0CRSDV | – |
| 67 | ETH0RXDV | – |
| 69 | ETH0RESET | – |
| 71 | – | – |
| 73 | USB0UDMF | – |
| 75 | USB0UDPF | – |
| 77 | – | – |
| 79 | – | – |
| 81 | – | – |
| 83 | – | – |
| 85 | DIGIO_0 | P21_0 |
| 87 | DIGIO_2 | P21_2 |
| 89 | DIGIO_4 | P24_8 |
| 91 | DIGIO_6 | – |
| 93 | DIGIO_8 | – |
| 95 | DIGIO_10 | P10_8 |
| 97 | DIGIO_12 | P10_10 |
| 99 | DIGIO_14 | P20_13 |
| 101 | – | – |
| 103 | MUX0 | – |

| Pin | Main Board function | Piggyback board device port |
|-----|---------------------|-----------------------------|
| 44 | FLXSTPWT | P10_1 |
| 46 | FLX1EN | P10_5 |
| 48 | FLX CLK | P10_8 |
| 50 | – | – |
| 52 | ETH0MDC | – |
| 54 | ETH0TXD0 | – |
| 56 | ETH0TXD1 | – |
| 58 | ETH0TXD2 | – |
| 60 | ETH0TXD3 | – |
| 62 | ETH0TXCLK | – |
| 64 | ETH0TXER | – |
| 66 | ETH0TXEN | – |
| 68 | ETH0COL | – |
| 70 | ETH0LINK | – |
| 72 | – | – |
| 74 | USB0UDMH | – |
| 76 | USB0UDPH | – |
| 78 | – | – |
| 80 | – | – |
| 82 | – | – |
| 84 | – | – |
| 86 | DIGIO_1 | P21_1 |
| 88 | DIGIO_3 | P24_6 |
| 90 | DIGIO_5 | – |
| 92 | DIGIO_7 | – |
| 94 | DIGIO_9 | – |
| 96 | DIGIO_11 | P20_10 |
| 98 | DIGIO_13 | P10_11 |
| 100 | DIGIO_15 | P10_13 |
| 102 | – | – |
| 104 | MUX1 | – |

Table 7.1 Main board connector CN1 (cont'd)

| Pin | Main Board function | Piggyback board device port |
|-----|---------------------|-----------------------------|
| 105 | MUX2 | – |
| 107 | ADC0 | AP0_0 |
| 109 | ADC2 | – |
| 111 | ADC4 | – |
| 113 | ADC6 | – |
| 115 | VDDIOF | – |
| 117 | VDDDB | – |
| 119 | VDDDB | – |
| 121 | GND | – |
| 123 | GND | – |
| 125 | GND | – |
| 127 | GND | – |

| Pin | Main Board function | Piggyback board device port |
|-----|---------------------|-----------------------------|
| 106 | – | – |
| 108 | ADC1 | AP0_1 |
| 110 | ADC3 | – |
| 112 | ADC5 | – |
| 114 | ADC7 | – |
| 116 | VDDIOF | – |
| 118 | VDDDB | – |
| 120 | VDDDB | – |
| 122 | GND | – |
| 124 | GND | – |
| 126 | GND | – |
| 128 | GND | – |

7.1.2 Main Board Connector CN2

Table 7.2 Main board connector CN2

| Pin | Function | Device port |
|-----|----------|-------------|
| 1 | CAN2TX | P24_8 |
| 3 | CAN2RX | P24_9 |
| 5 | CAN4TX | P4_6 |
| 7 | CAN4RX | P4_7 |
| 9 | LIN2TX | P5_4 |
| 11 | LIN2RX | P5_6 |
| 13 | LIN4TX | P4_12 |
| 15 | LIN4RX | P6_15 |
| 17 | LIN6TX | P6_15 |
| 19 | LIN6RX | P6_9 |
| 21 | LIN8TX | – |
| 23 | LIN8RX | – |
| 25 | LIN10TX | – |
| 27 | LIN10RX | – |

| Pin | Function | Device port |
|-----|----------|-------------|
| 2 | CAN3TX | P10_6 |
| 4 | CAN3RX | P10_5 |
| 6 | CAN5TX | P24_4 |
| 8 | CAN5RX | P24_5 |
| 10 | LIN3TX | P4_14 |
| 12 | LIN3RX | P4_15 |
| 14 | LIN5TX | P4_7 |
| 16 | LIN5RX | P4_6 |
| 18 | LIN7TX | P5_3 |
| 20 | LIN7RX | P5_2 |
| 22 | LIN9TX | – |
| 24 | LIN9RX | – |
| 26 | LIN11TX | – |
| 28 | LIN11RX | – |

Table 7.2 Main board connector CN2 (cont'd)

| Pin | Function | Device port |
|-----|-----------|-------------|
| 29 | LIN12TX | – |
| 31 | LIN12RX | – |
| 33 | LIN14TX | – |
| 35 | LIN14RX | – |
| 37 | – | – |
| 39 | CAN12TX | – |
| 41 | CAN12RX | – |
| 43 | CAN14TX | – |
| 45 | CAN14RX | – |
| 47 | CAN6TX | P4_14 |
| 49 | CAN6RX | P4_15 |
| 51 | CAN8TX | – |
| 53 | CAN8RX | – |
| 55 | CAN10TX | – |
| 57 | CAN10RX | – |
| 59 | – | – |
| 61 | LIN16TX | – |
| 63 | LIN16RX | – |
| 65 | LIN18TX | – |
| 67 | LIN18RX | – |
| 69 | LIN20TX | – |
| 71 | LIN20RX | – |
| 73 | LIN22TX | – |
| 75 | LIN22RX | – |
| 77 | – | – |
| 79 | SFMA0CLK | – |
| 81 | SFMA0IO0 | – |
| 83 | SFMA0IO2 | – |
| 85 | – | – |
| 87 | MMCA0CLK | – |
| 89 | MMCA0DAT0 | – |

| Pin | Function | Device port |
|-----|-----------|-------------|
| 30 | LIN13TX | – |
| 32 | LIN13RX | – |
| 34 | LIN15TX | – |
| 36 | LIN15RX | – |
| 38 | – | – |
| 40 | CAN13TX | – |
| 42 | CAN13RX | – |
| 44 | CAN15TX | – |
| 46 | CAN15RX | – |
| 48 | CAN7TX | P24_6 |
| 50 | CAN7RX | P24_7 |
| 52 | CAN9TX | – |
| 54 | CAN9RX | – |
| 56 | CAN11TX | – |
| 58 | CAN11RX | – |
| 60 | – | – |
| 62 | LIN17TX | – |
| 64 | LIN17RX | – |
| 66 | LIN19TX | – |
| 68 | LIN19RX | – |
| 70 | LIN21TX | – |
| 72 | LIN21RX | – |
| 74 | LIN23TX | – |
| 76 | LIN23RX | – |
| 78 | – | – |
| 80 | SFMA0SSL | – |
| 82 | SFMA0IO1 | – |
| 84 | SFMA0IO3 | – |
| 86 | – | – |
| 88 | MMCA0CMD | – |
| 90 | MMCA0DAT1 | – |

Table 7.2 Main board connector CN2 (cont'd)

| Pin | Function | Device port |
|-----|-----------|-------------|
| 91 | MMCA0DAT2 | – |
| 93 | MMCA0DAT4 | – |
| 95 | MMCA0DAT6 | – |
| 97 | – | – |
| 99 | ETH1MDIO | – |
| 101 | ETH1RXD0 | – |
| 103 | ETH1RXD1 | – |
| 105 | ETH1RXD2 | – |
| 107 | ETH1RXD3 | – |
| 109 | ETH1RXCLK | – |
| 111 | ETH1RXER | – |
| 113 | ETH1CRSDV | – |
| 115 | ETH1RXDV | – |
| 117 | ETH1RESET | – |
| 119 | – | – |
| 121 | GND | – |
| 123 | GND | – |
| 125 | GND | – |
| 127 | GND | – |

| Pin | Function | Device port |
|-----|-----------|-------------|
| 92 | MMCA0DAT3 | – |
| 94 | MMCA0DAT5 | – |
| 96 | MMCA0DAT7 | – |
| 98 | – | – |
| 100 | ETH1MDC | – |
| 102 | ETH1TXD0 | – |
| 104 | ETH1TXD1 | – |
| 106 | ETH1TXD2 | – |
| 108 | ETH1TXD3 | – |
| 110 | ETH1TXCLK | – |
| 112 | ETH1TXER | – |
| 114 | ETH1TXEN | – |
| 116 | ETH1COL | – |
| 118 | ETH1LINK | – |
| 120 | – | – |
| 122 | GND | – |
| 124 | GND | – |
| 126 | GND | – |
| 128 | GND | – |

7.1.3 Main Board Connector CN3

Table 7.3 Main board connector CN3

| Pin | Function | Device port |
|-----|----------|-------------|
| 1 | CSI0CS0 | P2_14 |
| 3 | CSI0CS1 | P17_1 |
| 5 | CSI0CS2 | P4_13 |
| 7 | CSI0CS3 | P10_10 |
| 9 | – | – |
| 11 | – | – |
| 13 | PSI5SRX1 | P6_13 |
| 15 | PSI5STX1 | P6_14 |

| Pin | Function | Device port |
|-----|----------|-------------|
| 2 | CSI0CLK | P6_8 |
| 4 | CSI0SI | P6_7 |
| 6 | CSI0SO | P6_9 |
| 8 | – | – |
| 10 | CSI1CS1 | P20_8 |
| 12 | – | – |
| 14 | PSI5RX1 | P5_2 |
| 16 | PSI5TX1 | P5_3 |

Table 7.3 Main board connector CN3 (cont'd)

| Pin | Function | Device port |
|-----|-----------|-------------|
| 17 | PSI5SCLK1 | P6_15 |
| 19 | – | – |
| 21 | CSI1CS2 | P17_0 |
| 23 | – | – |
| 25 | – | – |
| 27 | – | – |
| 29 | CSI1SCLK | P10_3 |
| 31 | – | – |
| 33 | – | – |
| 35 | – | – |
| 37 | – | – |
| 39 | – | – |
| 41 | – | – |
| 43 | – | – |
| 45 | – | – |
| 47 | – | – |
| 49 | – | – |
| 51 | – | – |
| 53 | – | – |
| 55 | AD1_0 | AP2_0 |
| 57 | AD1_2 | AP2_2 |
| 59 | AD1_4 | AP2_4 |
| 61 | AD1_6 | AP2_6 |
| 63 | PWM0 | P10_0 |
| 65 | PWM2 | P10_6 |
| 67 | PWM4 | P24_8 |
| 69 | PWM6 | P3_6 |
| 71 | DIGIO16 | AP0_0 |
| 73 | DIGIO18 | AP0_2 |
| 75 | DIGIO20 | AP0_4 |
| 77 | DIGIO22 | AP0_6 |

| Pin | Function | Device port |
|-----|----------|-------------|
| 18 | – | – |
| 20 | – | – |
| 22 | CSI1CS3 | P20_4 |
| 24 | CSI1CS0 | P2_0 |
| 26 | DIGIO_24 | P6_6 |
| 28 | CSI1SO | P10_2 |
| 30 | CSI1SI | P10_4 |
| 32 | – | – |
| 34 | – | – |
| 36 | – | – |
| 38 | – | – |
| 40 | – | – |
| 42 | – | – |
| 44 | – | – |
| 46 | – | – |
| 48 | – | – |
| 50 | – | – |
| 52 | – | – |
| 54 | – | – |
| 56 | AD1_1 | AP2_1 |
| 58 | AD1_3 | AP2_3 |
| 60 | AD1_5 | AP2_5 |
| 62 | AD1_7 | AP2_7 |
| 64 | PWM1 | P10_1 |
| 66 | PWM3 | P24_7 |
| 68 | PWM5 | P10_4 |
| 70 | PWM7 | P10_7 |
| 72 | DIGIO17 | AP0_1 |
| 74 | DIGIO19 | AP0_3 |
| 76 | DIGIO21 | AP0_5 |
| 78 | DIGIO23 | AP0_7 |

Table 7.3 Main board connector CN3 (cont'd)

| Pin | Function | Device port |
|-----|----------|-------------|
| 79 | ENC0 | – |
| 81 | – | – |
| 83 | – | – |
| 85 | – | – |
| 87 | – | – |
| 89 | – | – |
| 91 | – | – |
| 93 | – | – |
| 95 | – | – |
| 97 | – | – |
| 99 | – | – |
| 101 | – | – |
| 103 | – | – |
| 105 | – | – |
| 107 | – | – |
| 109 | – | – |
| 111 | – | – |
| 113 | – | – |
| 115 | – | – |
| 117 | – | – |
| 119 | – | – |
| 121 | GND | – |
| 123 | GND | – |
| 125 | GND | – |
| 127 | GND | – |

| Pin | Function | Device port |
|-----|----------|-------------|
| 80 | ENC1 | – |
| 82 | – | – |
| 84 | – | – |
| 86 | – | – |
| 88 | – | – |
| 90 | – | – |
| 92 | – | – |
| 94 | – | – |
| 96 | – | – |
| 98 | – | – |
| 100 | – | – |
| 102 | – | – |
| 104 | – | – |
| 106 | – | – |
| 108 | – | – |
| 110 | – | – |
| 112 | – | – |
| 114 | – | – |
| 116 | – | – |
| 118 | – | – |
| 120 | – | – |
| 122 | GND | – |
| 124 | GND | – |
| 126 | GND | – |
| 128 | GND | – |

7.2 Debug Connector CN4

Table 7.4 On-chip debug connector CN4

| Pin | Function | Device port |
|-----|----------------------|-------------|
| 1 | TDCK / LPDCLK / FPCK | JP0_2 |
| 3 | TRSTZ | |
| 5 | TDO / LPDO / FPDT | JP0_1 |
| 7 | TDI / LPDIO / FPDR | JP0_0 |
| 9 | TMS | JP0_3 |
| 11 | RDY / LPDCLKOUT | JP0_5 |
| 13 | RESETZ | |

| Pin | Function | Device port |
|-----|--------------|-------------|
| 2 | GND | |
| 4 | FLMD0_TOOL_c | FLMD0_TOOL |
| 6 | – | |
| 8 | E0VCC | |
| 10 | – | |
| 12 | GND | |
| 14 | GND | |

7.3 Pull-Up/Pull-Down Pin Header CN12

Table 7.5 Pull-up/pull-down header CN12

| Pin | Function |
|-----|---|
| 1 | fixed H level, depends on JP25: <ul style="list-style-type: none"> • JP25[2-1]: 5.0 V • JP25[2-3]: 3.3 V |
| 3 | |
| 5 | |
| 7 | |
| 9 | |
| 11 | fixed H level, depends on JP15: <ul style="list-style-type: none"> • JP15[2-1]: 5.0 V • JP15[2-3]: 3.3 V |
| 13 | |
| 15 | |
| 17 | |
| 19 | |

| Pin | Function |
|-----|---------------|
| 2 | fixed L level |
| 4 | |
| 6 | |
| 8 | |
| 10 | |
| 12 | |
| 14 | |
| 16 | |
| 18 | |
| 20 | |

7.4 Device Ports Connectors CN18 and CN21 to CN23

The device port connectors enable easy connection to almost all ports of the device.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.4.1 Device Ports Connector CN18

Table 7.6 Pull-up/pull-down header CN18

| Pin | Device port |
|-----|-------------|
| 1 | P5_3 |
| 2 | P5_6 |
| 3 | P5_4 |
| 4 | AWOVCL |
| 5 | P2_0 |
| 6 | P2_14 |
| 7 | P20_4 |
| 8 | P20_3 |
| 9 | P20_8 |
| 10 | P20_7 |
| 11 | P20_9 |
| 12 | P21_0 |
| 13 | P20_10 |
| 14 | P21_1 |
| 15 | P20_13 |
| 16 | P21_2 |
| 17 | P20_14 |
| 18 | ERROROUT_MZ |
| 19 | P10_0 |
| 20 | P10_1 |
| 21 | P10_2 |
| 22 | P10_3 |

7.4.2 Device Ports Connector CN21

Table 7.7 Pull-up/pull-down header CN21

| Pin | Device port |
|-----|-------------|
| 1 | P6_8 |
| 2 | P6_7 |
| 3 | P4_15 |
| 4 | P4_14 |
| 5 | P4_13 |
| 6 | P4_12 |
| 7 | P4_10 |
| 8 | P4_9 |
| 9 | P4_7 |
| 10 | P24_9 |
| 11 | P4_6 |
| 12 | P24_7 |
| 13 | P24_8 |
| 14 | P24_5 |
| 15 | P24_6 |
| 16 | P24_4 |
| 17 | AP0_7 |
| 18 | AP0_6 |
| 19 | AP0_5 |
| 20 | AP0_4 |
| 21 | AP0_3 |
| 22 | AP0_1 |

7.4.3 Device Ports Connector CN22

Table 7.8 Pull-up/pull-down header CN22

| Pin | Device port |
|-----|-------------|
| 1 | PWRCTL |
| 2 | P5_2 |
| 3 | VMONOUTZ |
| 4 | X1_C * |
| 5 | FLMD0 |
| 6 | X2_C * |
| 7 | JP0_2 |
| 8 | TRSTZ |
| 9 | RESETZ |
| 10 | JP0_5 |
| 11 | JP0_1 |
| 12 | JP0_0 |
| 13 | P6_15 |
| 14 | P6_14 |
| 15 | JP0_3 |
| 16 | P6_6 |
| 17 | P3_7 |
| 18 | P6_13 |
| 19 | AWOVCL |
| 20 | P6_9 |
| 21 | P6_10 |
| 22 | P3_6 |

Note * By default these signals are not connected to CN22 in order to minimize signal interference. If required they can be connected via 0 Ω resistors R3 and R4.

7.4.4 Device Ports Connector CN23

Table 7.9 Pull-up/pull-down header CN23

| Pin | Device port |
|-----|-------------|
| 1 | P10_4 |
| 2 | P10_5 |
| 3 | P10_6 |
| 4 | P10_13 |
| 5 | P10_7 |
| 6 | P10_8 |
| 7 | P10_14 |
| 8 | P10_10 |
| 9 | P10_11 |
| 10 | P17_0 |
| 11 | P17_1 |
| 12 | AP2_5 |
| 13 | AP2_6 |
| 14 | AP2_7 |
| 15 | AP2_3 |
| 16 | AP2_2 |
| 17 | AP2_4 |
| 18 | AP2_1 |
| 19 | AP2_0 |
| 20 | AP0_2 |
| 21 | AP0_0 |
| 22 | GND |

8. Jumper Configuration Examples

Several functions of the board can be configured via jumpers. The board is shipped without any jumpers set.

For a complete list of jumpers refer to *2.1 Jumper Overview*.

For jumper settings related to the device operation mode, refer to *6.1 Operation Mode Selection*.

The following sections show some jumper settings, that allow to operate the piggyback board in different power supply configurations.

8.1 Stand-Alone Operation with Power Supply by Debugger

Basically the piggyback board can solely be powered by a connected debugger. Please make sure the debug tool is able to provide sufficient current on the power supply rails in order to operate the board in a useful manner.

Due to the limited current capability of Renesas' E2 Emulator, powering the board only via this debugger is not feasible.

In case of using another debug tool check its specification whether powering the piggyback board with the tool is possible.

8.2 Configuration Examples

8.2.1 General Settings





All of the following board configurations are based on these conditions:

- Normal device operation mode (JP41[OPEN]: FLMD0 = L).
- All voltages for all functions are activated.
- Current measurements are not carried out, hence JP4, JP5, JP30 and JP31 are set.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN8 (GND), CN9 (+5.0 V) and CN10 (+3.3 V) are assembled on the board.
- If also the core supply voltage of 1.12 V will be supplied from an external power supply the connector CN11 (included in the package) must be assembled on the board.

8.2.2 Jumper Indicators

- The **green** jumper JP41 for FLMD0 must always be open for a 'normal' (user mode and debug) operation of the device.
- The **red** jumpers are related to the power supply configuration.

Following jumper symbols are used:

- : Jumper must not be set.
- : Jumper must be set in the indicated position, in this case position [2-3]
- : Jumper can be set to position [1-2] or position [2-3]
- : Jumper with optional setting. The red setting [2-3] is the default setting. The blue setting [1-2] is the optional setting.

Note

The pin 1 of a jumper can be identified by

- a small circle near the jumper
 - a square soldering pad.
-

8.2.4 Stand-Alone Operation with Single External Power Supply 5.0 V: Minimum Configuration 2

This example enables to operate the board with only the 5.0 V external power supply. Since no 3.3 V voltage is available, all I/O ports can only use 5.0 V.

- CN8: GND connection
- CN9: 5.0 V
- CN10: not connected, no 3.3 V
 - jumpers JP1, JP6 to JP8, JP10 to JP13, JP33 and JP35 are set to 5.0 V position [1-2]
- CN11: not connected, no IN_1v12
 - VDD from SVR_OUTPUT (JP23[2-3]) from on-chip Switching Voltage Regulator
 Refer to 3.3 Device Core Voltage (VDD) Selection for further details about VDD voltage.

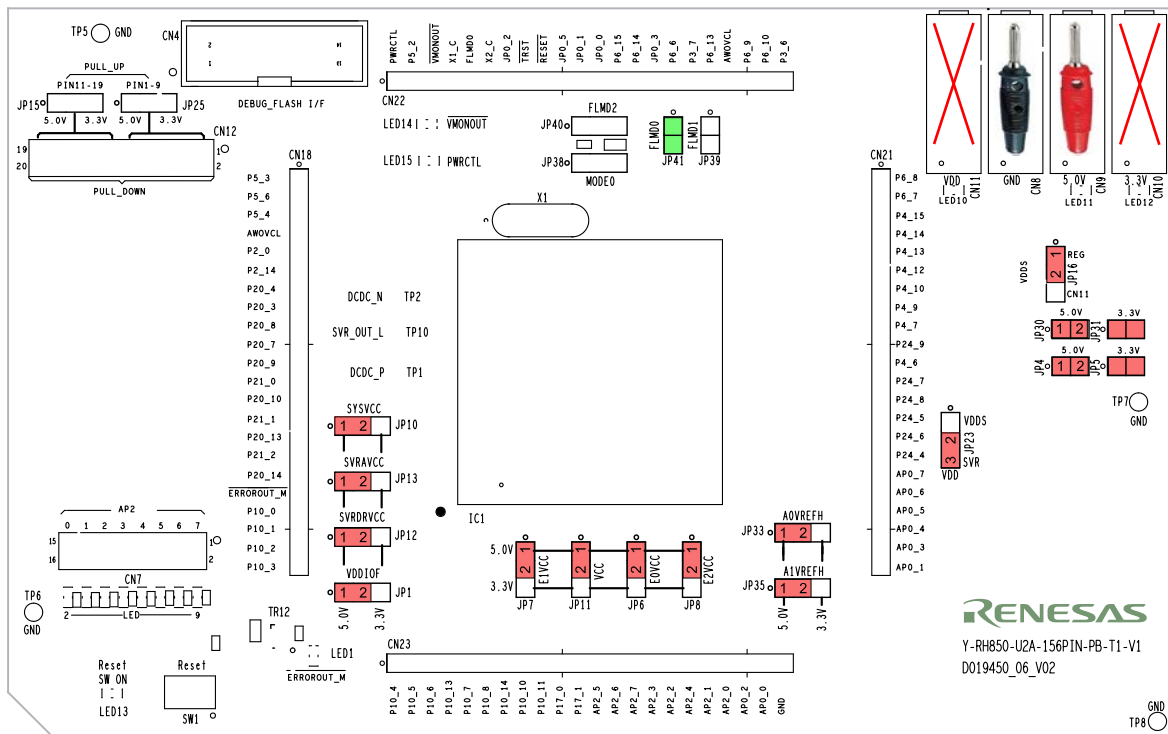


Figure 8.2 Stand-alone operation with single external power supply 5.0V

8.2.5 Stand-Alone Operation with All External Power Supplies: Maximum Configuration

This example assumes all external power supplies are connected and used.

- CN8: GND connection
 - CN9: 5 V
 - CN10: 3.3V
 - select desired 3.3 V/5.0 V via jumpers JP1, JP6 to JP8, JP10 to JP13, JP33 and JP35
 - CN11: 1.12 V (IN_1v12)
 - JP16[2-3], JP23[2-1]: use IN_1v12 for VDD voltage
- Refer to 3.3 Device Core Voltage (VDD) Selection for further details about VDD voltage.

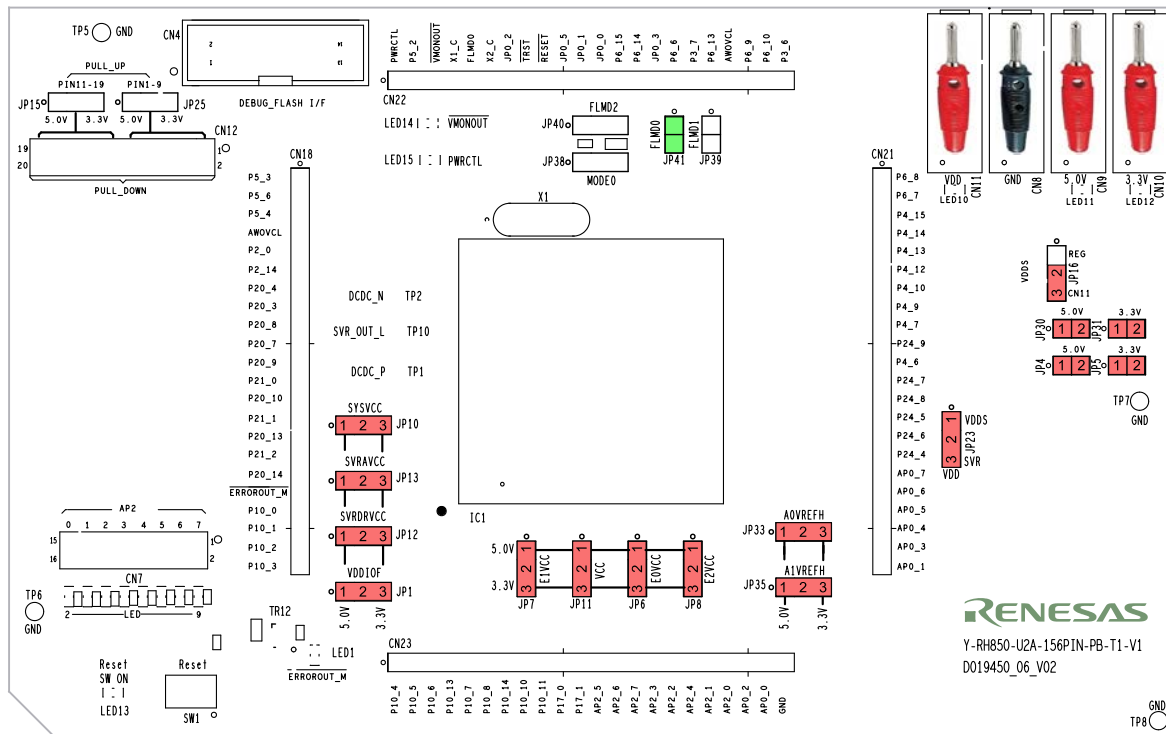


Figure 8.3 Stand-alone operation with maximum external power supply

8.2.6 Operation on the Main Board: No External Supply

This example assumes the piggyback board is plugged onto a Main Board, which provides 3.3 V and 5.0 V.

Do not supply the 5V (CN9) and 3.3V (CN10) voltage directly to the piggyback board

- CN8 to CN11: not connected, no external 5.0 V, 3.3 V, 1.12 V
Select desired 3.3 V/5.0 V via jumpers JP1, JP6 to JP8, JP10 to JP13, JP33 and JP35
 - VDD supply:
 - JP16[2-1]: use reg_vcc_VDD from on-board voltage regulator for supply of VDD voltage
 - VDD from reg_vcc_VDD (JP23[2-1]) or SVR_OUTPUT (JP23[2-3]) from on-chip Switching Voltage Regulator
- Refer to 3.3 Device Core Voltage (VDD) Selection for further details about VDD voltage.

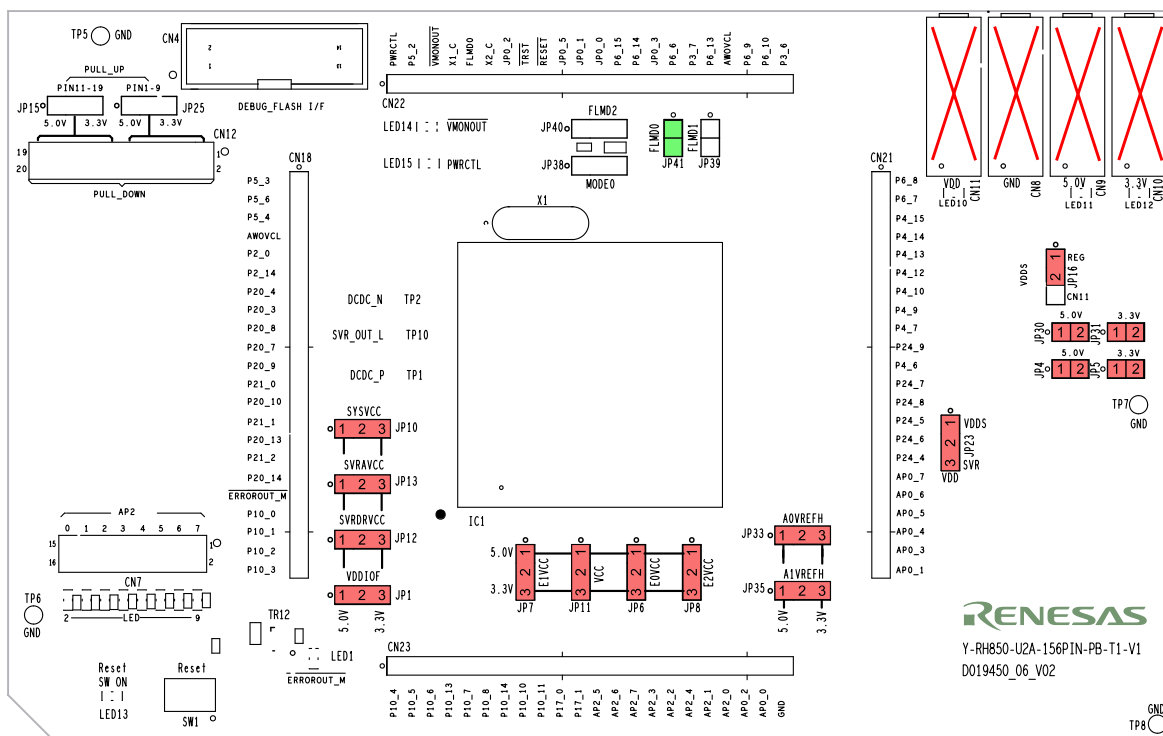


Figure 8.4 Main board operation without external power supply

Note

This configuration still allows to utilize an external IN_1v12 voltage (connected to CN8, CN11) as the source for VDD voltage. In this case set JP16[2-3] and JP23[2-1].

CAUTION

Do not supply 5V (CN9) and 3.3V (CN10) directly to the piggyback board if these voltages are already supplied by the main board.

9. Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied when power supply to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW1 into '5-6 ON' position, so that RESET is permanently asserted.
Alternatively keep SW1 manually in '5-4 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, release RESET by returning SW1 into the 'OFF' position.

For details how to apply a RESET, please refer to section *6.2 RESET Switch*.

9.2 CAN0RX is Shared with FLASH Programmer Signal FLMD1

When using this product plugged into a motherboard where CAN0 is connected to the CAN-transceiver the FLASH programmer will not work.

This is because the CAN0RX function is shared with the FLMD1 function on the same device PIN.

Most CAN-transceiver are driving the RX line actively and the FLASH programmer then is not able to change signal level as required for flashing.

9.3 Power On Piggyback Board Without RH850 Microcontroller installed

The piggyback board Y-RH850-U2A-156PIN-PB-T1-V1 is not designed to be powered on when the RH850 microcontroller is not installed in socket IC1.

If the microcontroller is not installed the SVR power supply circuit does not have the control signals SVRNGATE and SVRPGATE and may be damaged.

If for some reason the board has to be powered on without a microcontroller mounted in socket IC1 please make sure the jumper JP12[1-2-3] (SVRDRVCC) is open. In this case no power is supplied to the SVR control circuit, and it will not be damaged.

10. Mechanical Dimensions

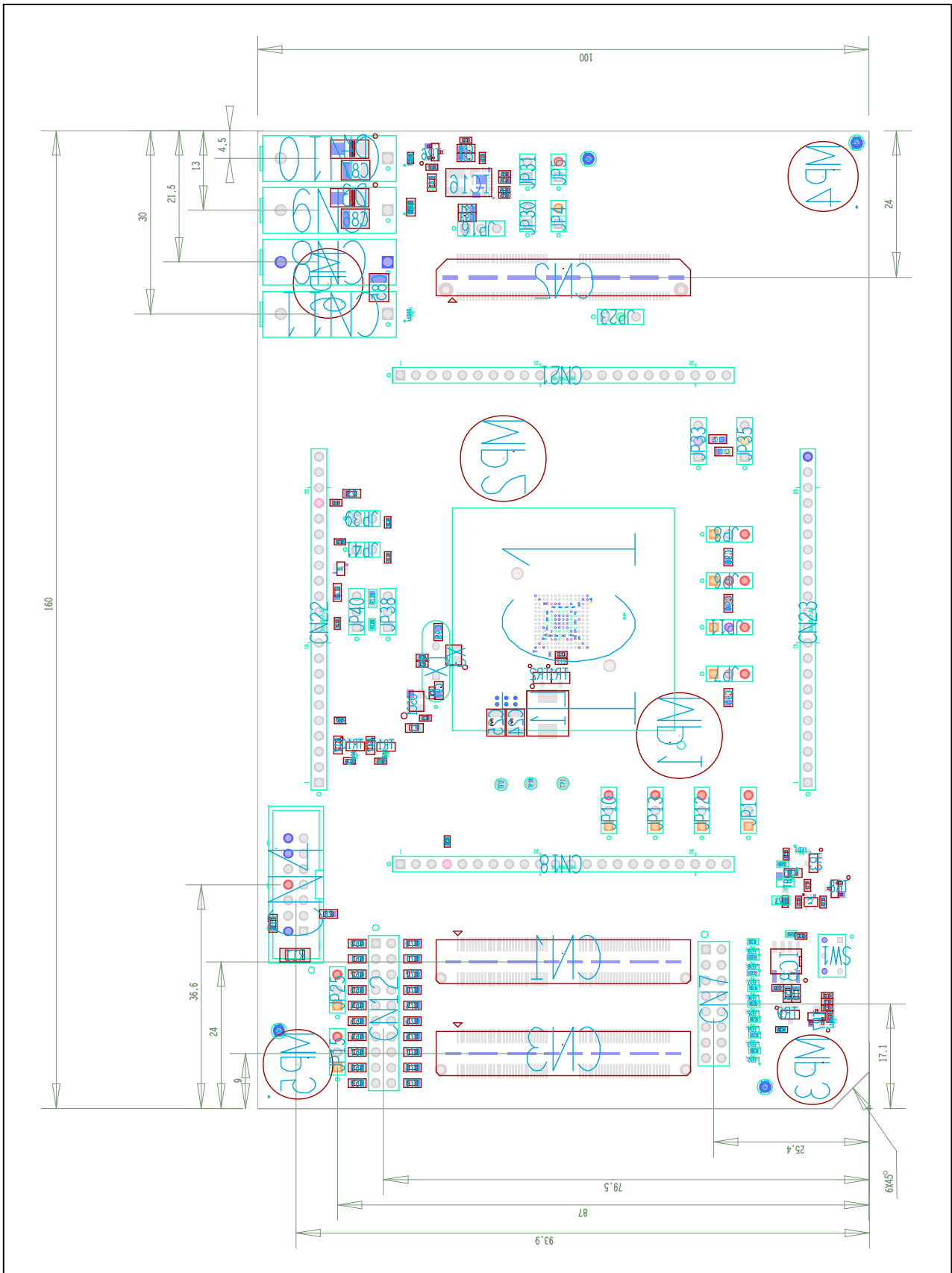


Figure 10.1 Mechanical dimensions

11. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.

11.1 Board Version D019450_06_V01

The following components described in the schematics are not provided with the board upon delivery:

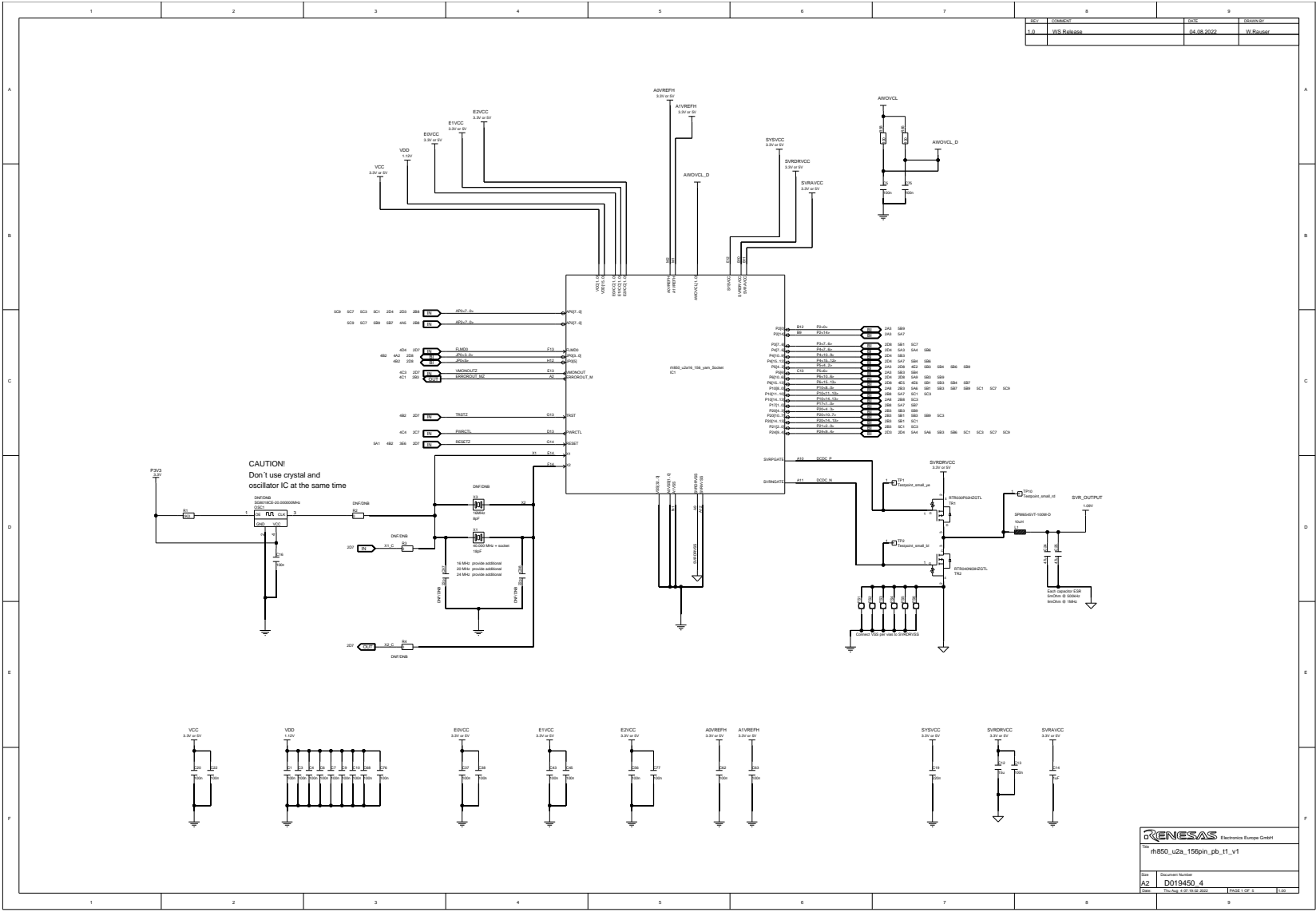
- Oscillators and resonators: OSC1, X3
- Capacitors: C97, C98
- Resistors: R2 – R4, R34

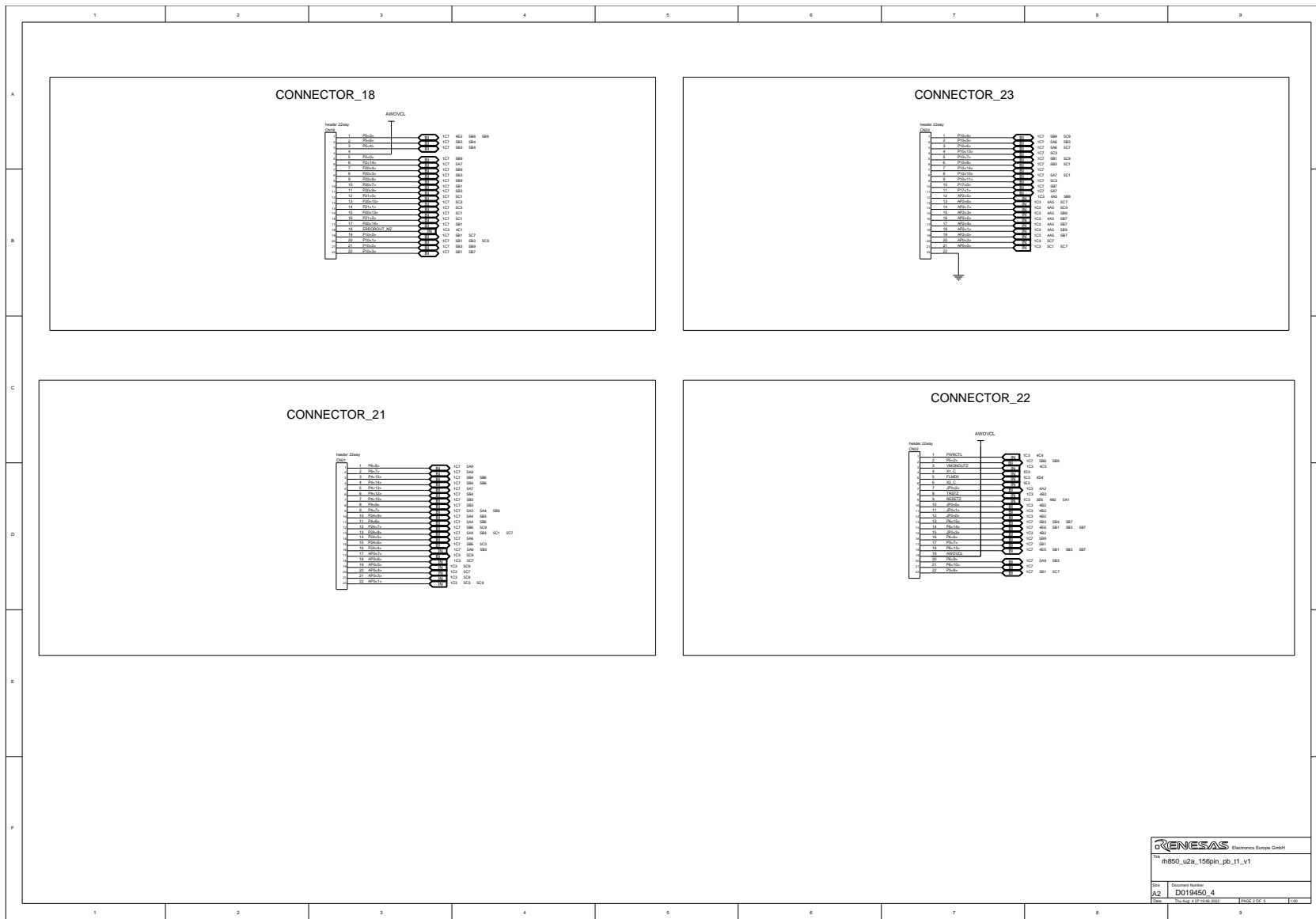
The above components are indicated with "DNF/DNB" in the schematics.

The following components described in the schematics are provided with but not mounted on the board upon delivery:

- 1 Hirschmann 4 mm power lab sockets, red for CN11
- Three resonators HC49 (16/20/24 MHz)
- 30 jumpers, 2.54 mm, black

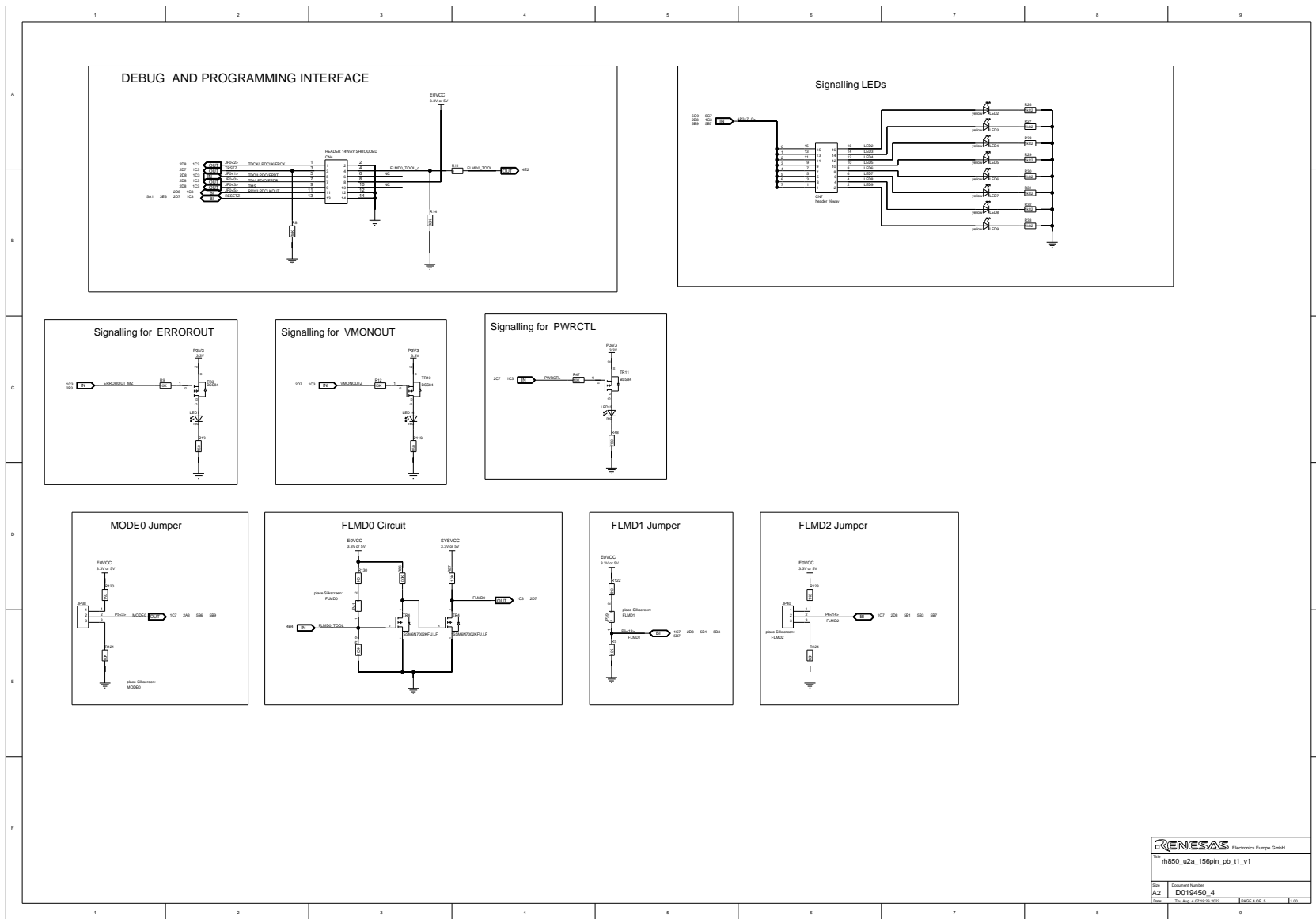
The above components are indicated with "DO NOT FIT / TO DELIVER WITH THE BOARD" or "provide additional" in the schematics.



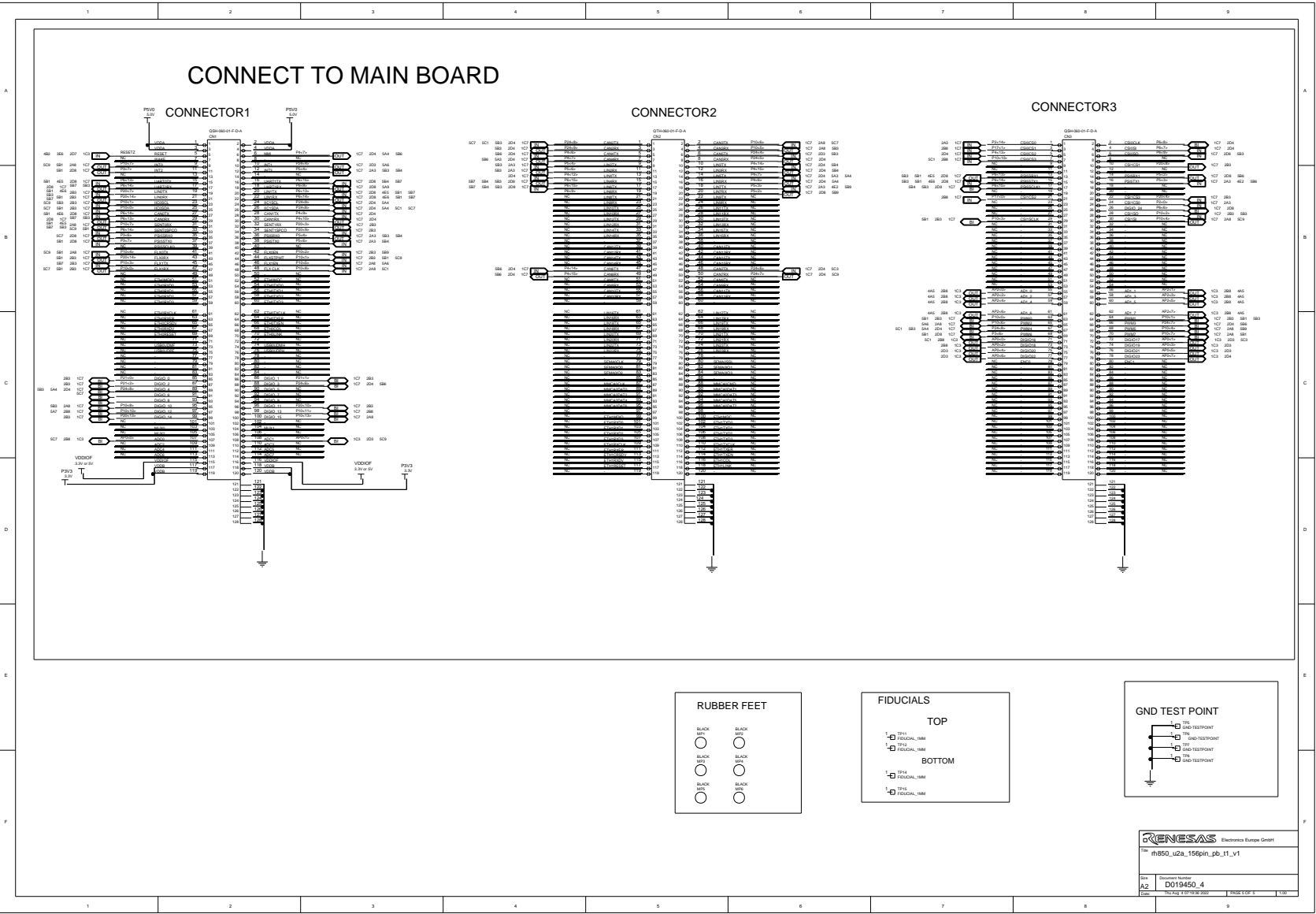


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| Doc. No. | Document Number |
| AZ | D019450_4 |
| Rev. | 10th. Rev. 4 (10/20/2023) (Rev. 7) (0/ 0) |

11.1.4 Page 4



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| 1.00 | 1.00 |



11.2 Board Version D019450_06_V02

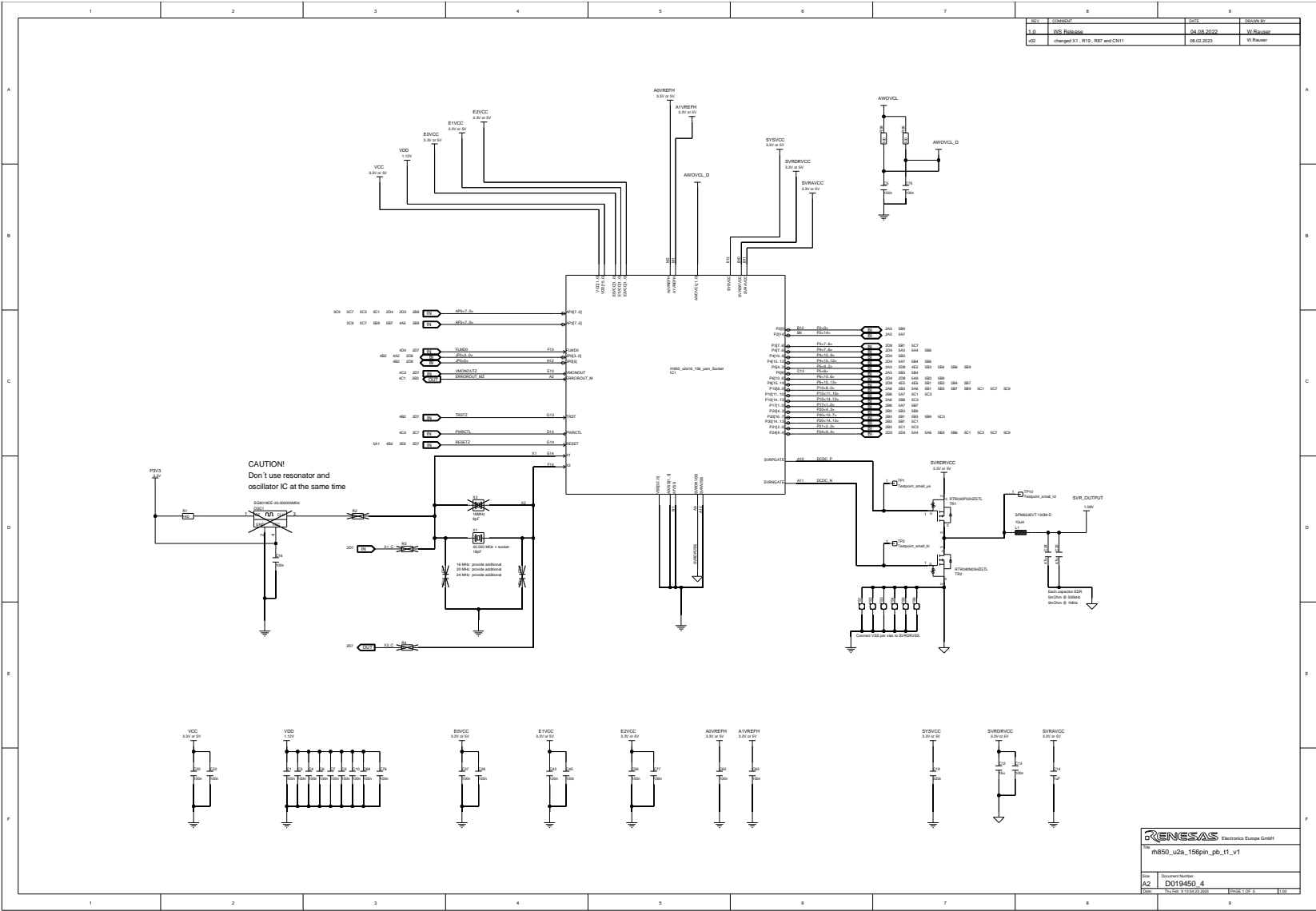
The following components described in the schematics are not provided with the board upon delivery:

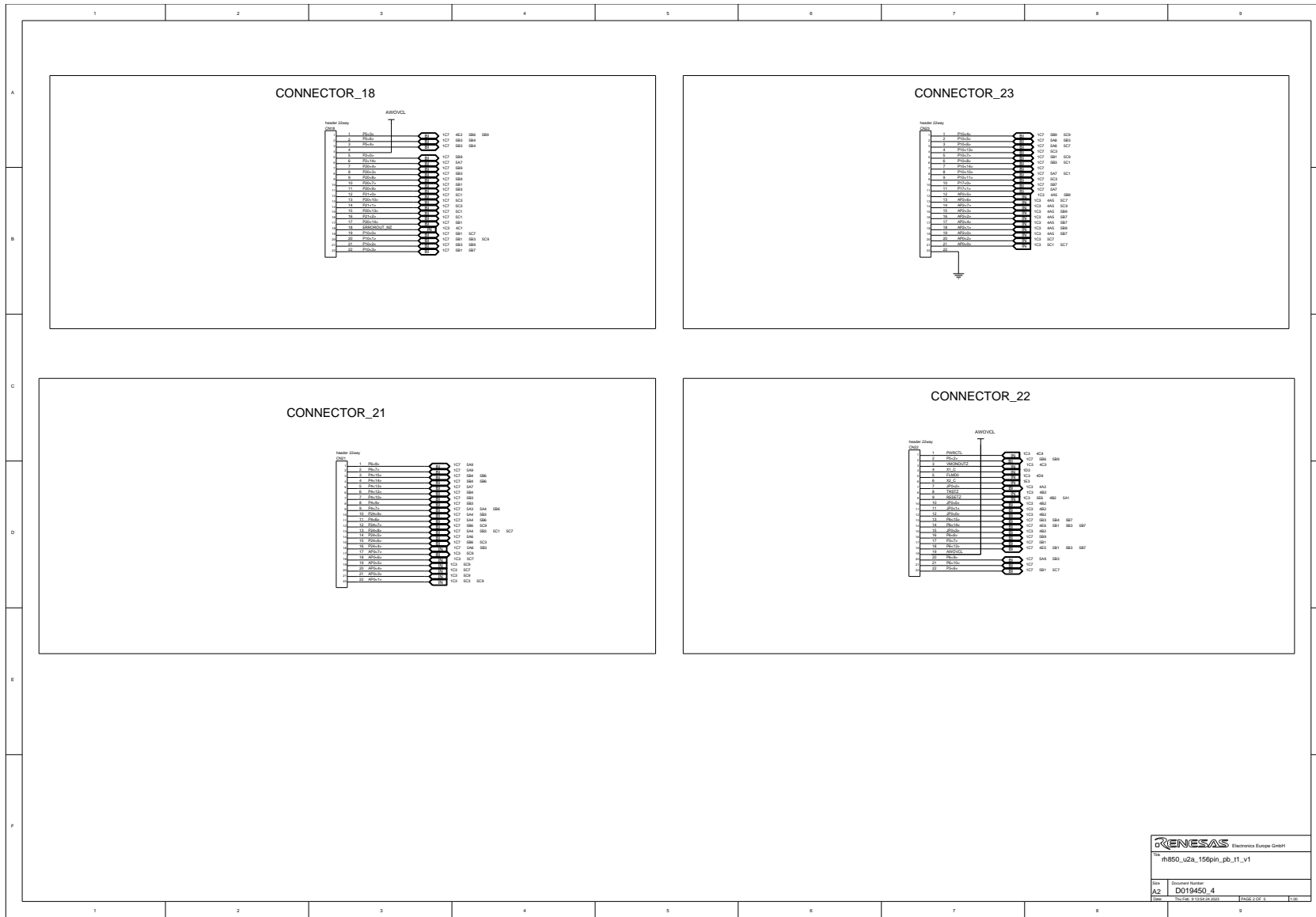
- Oscillators and resonators: OSC1, X3
- Capacitors: C97, C98
- Resistors: R2 – R4, R34

The following components described in the schematics are provided with but not mounted on the board upon delivery:

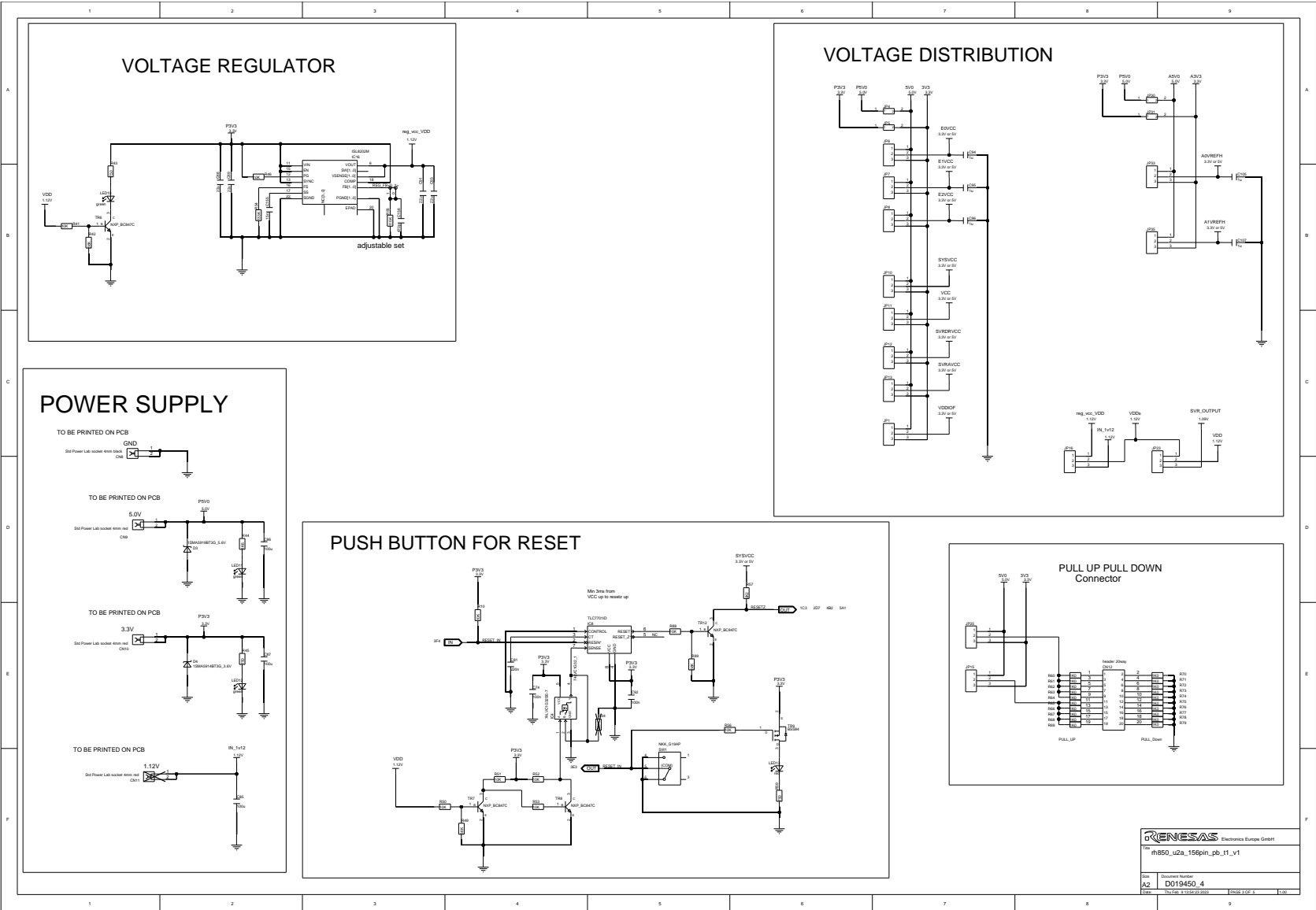
- 1 Hirschmann 4 mm power lab sockets, red for CN11
- Three resonators HC49 (16/20/24 MHz)
- 30 jumpers, 2.54 mm, black

Components that are not mounted in board production, are crossed out in the schematics.



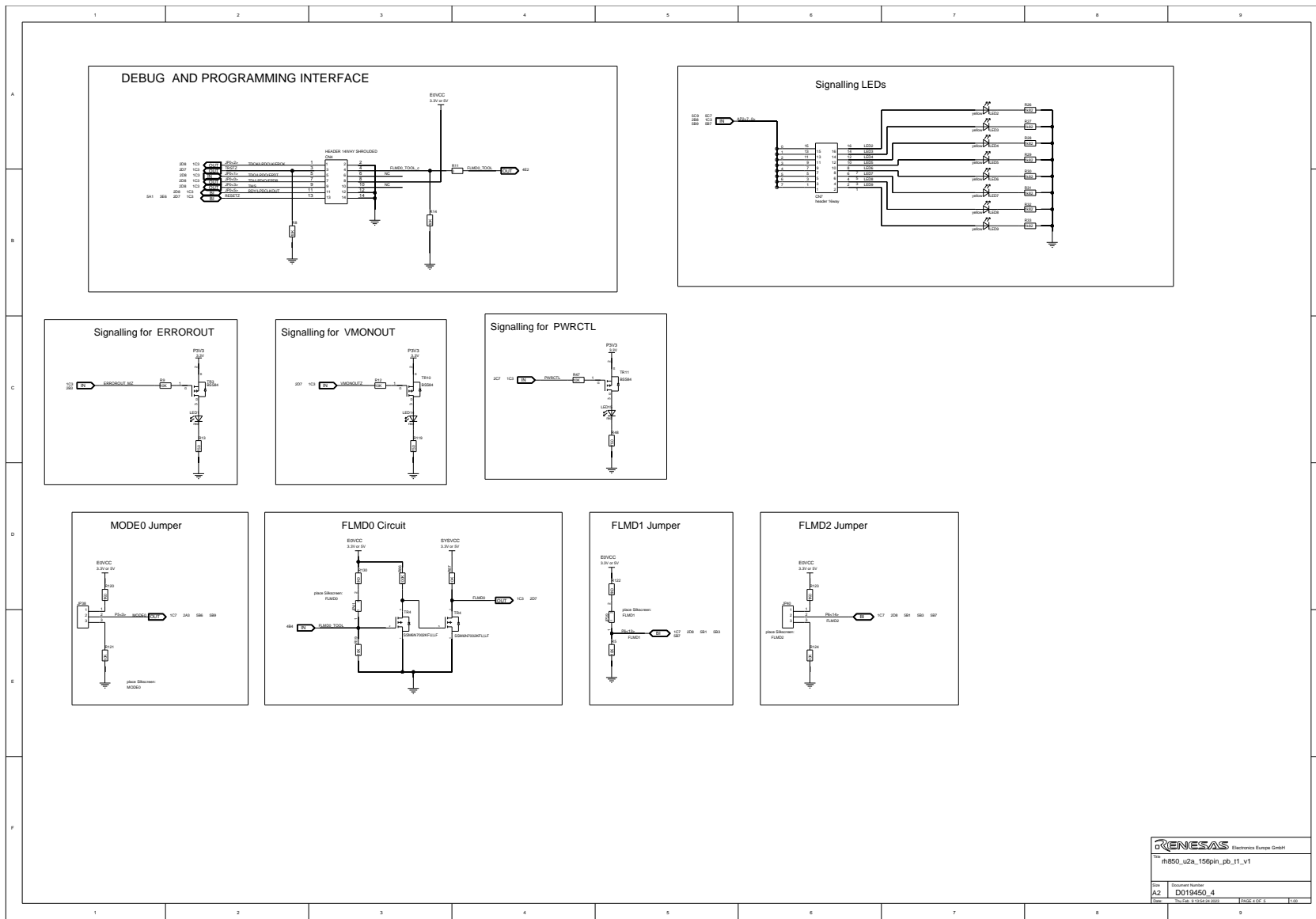


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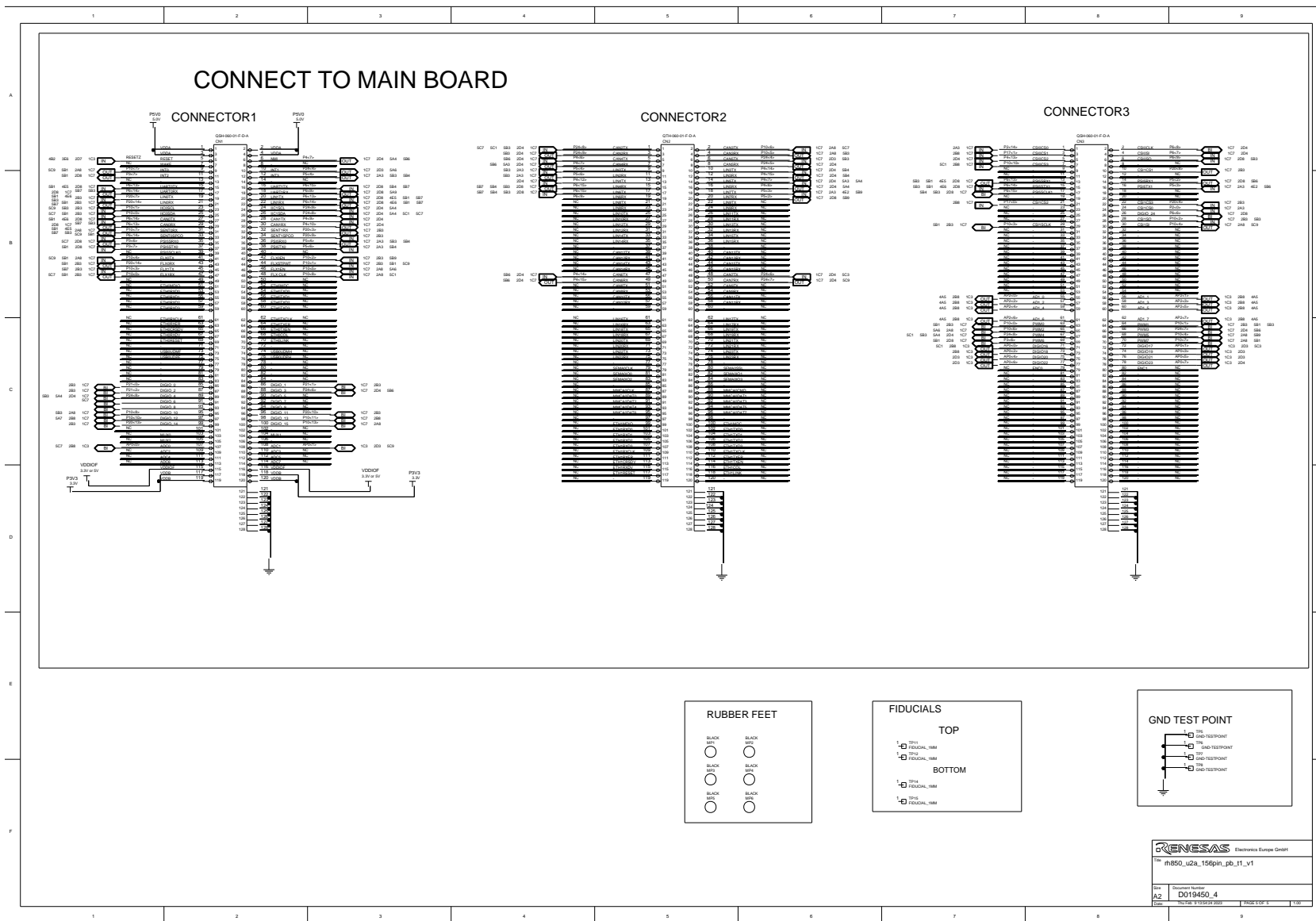


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11.2.4 Page 4



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| Page | 1 of 6 |



Revision History

| Rev. | Date | Description | |
|-------|------------|-----------------------|--|
| | | Page | Summary |
| V2.00 | 2023-10-26 | 13, 42 50 - 55 | Added precaution about power on of piggyback board without a microcontroller mounted. Caution in <i>3.1 Board Power Connection</i> . <i>9.3 Power On Piggyback Board Without RH850 Microcontroller installed</i> Added schematics for board revision D019450_06_V02 |
| V1.00 | 2022-11-30 | – | Initial release |

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