User's Manual

32

RH850 Evaluation Platform

RH850/U2B 468pin

User's Manual: Piggyback Board

Y-RH850-U2B-468PIN-PB-T1-V1

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

The RH850/U2B 468pin piggyback board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/U2B 468pin microcontrollers.

Notes

1. This document describes the functionality of the piggyback board and guides the user through its operation.
   For details regarding the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document low active signals are marked by an appended 'Z' or '#' to the pin or signal name. E.g., the reset pin is named RESETZ or RESET#.
3. In this document following abbreviations are used:
   – H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal

1.1 Package Components

The Y-RH850-U2B-468PIN-PB-T1-V1 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-U2B-468PIN-PB-T1-V1 package contains all these items. *Table 1.1 Package Components for the Y-RH850-U2B-468PIN-PB-T1-V1* shows the packing components of the Y-RH850-U2B-468PIN-PB-T1-V1 package.

Table 1.1 Package Components for the Y-RH850-U2B-468PIN-PB-T1-V1

Item	Description	Quantity
D018177	RH850/U2B 468pin piggyback board	1
D018172	Documentation CD	1
D010816-24	China RoHS document	1
D018171-24	Product contents list	1
Jumpers (2-way, 0.1")	In the bag	52 [1)] 47 [2)]
D018487	Y-RH850-DEBUG-ADAPTER-F14T46	1
Red Hirschmann 4 mm power lab sockets	In the bag	1
Würth PCB Terminal Block connector (including cable adapter plug)	In the bag	2
TE MATEnet 1000BASE-T1 Ethernet Port connector	In the bag	2

TE MATEnet 1000BASE-T1 Ethernet connection cable (1m)	In the bag	1
Resonators, HC49: 16 / 24 / 25 / 40 MHz	In the bag	4
100 Ohm chip resistor	In the bag	20 [3]

[1] For board version D018177_06_V01
[2] For board versions other than D018177_06_V01, min. quantity
[3] For board versions other than D018177_06_V01

Note

Please keep the Y-RH850-U2B-468PIN-PB-T1-V1 box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original box when transporting the Y-RH850-U2B-468PIN-PB-T1-V1. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported Main Boards

This piggyback board can be used as a standalone board, or it can be mated with a main board. The following main boards are supported:

- Y-RH850-X1X-MB-T1-V1
- Y-RH850-X1X-MB-T2-Vx
- Y-RH850-X2X-MB-T1-V1
- Y-COMMON-MB-T1-V1

1.3 Main Features

- Burn-in socket for mounting of the device
- Several power set-up options
  - Combined operation with powering from main board
  - Stand-alone operation with single power supply (3.3 V or 5.0 V only)
  - Stand-alone operation with flexible, individual power supply (typ. 1.12 V, 3.3 V, 5.0 V)
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
- Debugging and programming interface:
  - 46-pin Aurora Debug Connector (e.g., for using E2 OCD Emulator using the 46 pin to 14 pin adapter Y-RH850-DEBUG-ADAPTER-F14T46, included)
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with an exchangeable 16/20/24/25/40 MHz Crystal Resonator
- General purpose signaling LEDs
- Jumpers for device mode selection and other configuration options
- Automotive Ethernet Port 100/1000BASE-T1
- On-board interface connector for
  - Renesas High-Speed Serial I/F (RHSIF)
  - Renesas High Speed Bus (RHSB)
  - Multichannel Serial Peripheral Interface (MSPI)
  - Automotive Ethernet (ETN)
- Operating temperature from 0 °C to +40 °C

1.4 Piggyback Board Versions

The following versions of the Piggyback Board are available:

Table 1.2 Y-RH850-U2B-468PIN-PB-T1-V1 board versions

Board version	Schematic version
D018177_06_V01	D018177_04_V0110
D018177_06_V02	D018177_04_V0210
D018177_06_V03	D018177_04_V0300

The table shows the differences of the board versions:

Table 1.3 Y-RH850-U2B-468PIN-PB-T1-V1 board version differences

Nr	Modified Function	Detailed Description of Changes	D018177_06_V01	D018177_06_V02	D018177_06_V03
1	Improved signal quality when using P22_5 either for onboard functionality or offboard function on pin header or MainBoard.	- Changed signal of CN14.39. See chapter *7.3.3* for details. - Changed signal of CN3.24 See chapter *7.1.3* for details	P22_5	CN_P22_5	CN_P22_5
2	Changed port control signal for Ethernet0 Reset on the PiggyBoard.	Changed Ethernet0 RESET control signal on IC5.	P12_3	P10_8	P10_8
3	Changed port control signal for Ethernet0 Reset on the MainBoard.	Changed Ethernet0 RESET control signal for pin 69 on connector CN1.	P12_3	P12_3	P10_8
4	Changed port control signal for Ethernet1 Reset on the PiggyBoard.	Changed Ethernet1 RESET control signal on IC4.	P30_0	P12_3	P12_3
5	Changed port control signal for Ethernet1 Reset on the MainBoard.	Changed Ethernet1 RESET control signal for pin 117 on connector CN2.	P30_0	P30_0	P12_3
6	Access to 5.0V and GND is improved for measurements.	Added 5.0V and GND pin headers JP8 and JP9.	-	Yes	Yes

Nr	Modified Function	Detailed Description of Changes	D018177_06_V01	D018177_06_V02	D018177_06_V03
7	Improved signal quality when using device ports either for differential signals or single ended signals.	Changed circuitry for differential interfaces: - Changed multiplexers for LVDS signals. - Added switch SW3-3 for RHSB/MSPI multiplexer control. - Added SW5 for RHSB/MSPI/RHSIF multiplexer enable/disable. - Added (auxiliary) termination resistors for LVDS signals See chapters *6.5* to *6.9* for details.	-	Yes The print on the board for SW5-4 and SW5-5 is wrong. Please refer to chapter *9.4* for the correct print.	Yes
8	MSPI6 RX/TX signals can be switched to directly connected two boards for communication.	Changed signal routing for MSPI6 signals See chapter *7.5* and *0* for details.	-	Yes	Yes
9	Improved support for MSPI6 Master/Slave usage.	Added JP6 for selection of MSPI6 SSI_IN signal. See chapter *6.6* for details.	-	Yes	Yes
10	More flexible usage for EVTO signal source.	Added P32_0 as EVTO signal on AURORA connector. See SW4-3 in chapters *5* and *8.2* for details.	-	Yes	Yes
11	-	Factory rework for TR1 polarity and missing SVR capacitor. See chapter *9.2* for details.	Yes	-	-
12	Improved signal quality for Ethernet 0 clock signal.	Update for Ethernet0 clock signal: - Changed port control signal for Signaling LED 6. See chapter *6.3* for details. Changed signal on CN1.89 (DIGIO_4). See chapter *7.1.1* for details.	P11_4	P22_0 Implemented as factory rework. See chapter *9.3* for details.	P22_0
13	Access to 5.0V and GND is improved for measurements.	Added TP1 on SVRPGATE, TP2 on SVRNGATE, TP3 on SVR	-	Yes	Yes

1.5 Piggyback Board Views

Following figures provide the top and bottom views of the piggyback boards.

Note: The figures show the board with all assembled components. Not all components are assembled at all board versions at shipment.

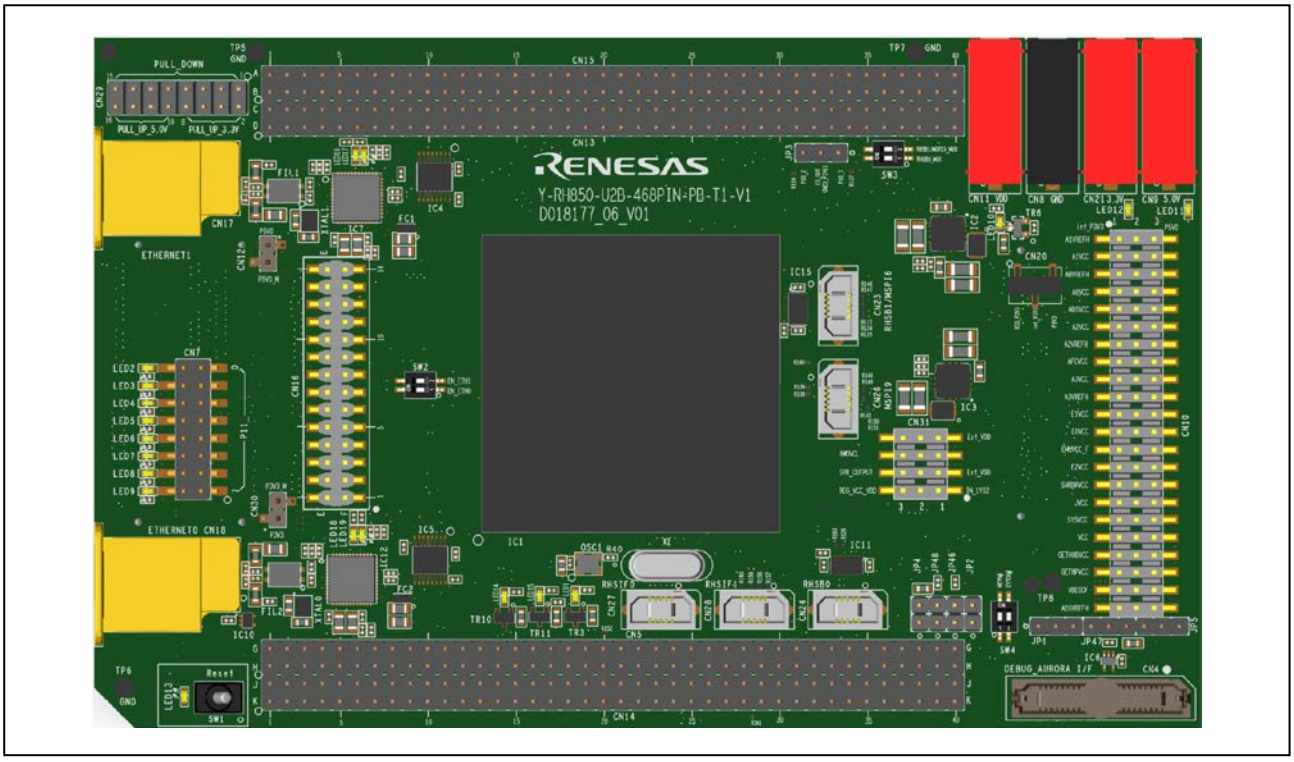


Figure 1.1 D018177_06_V01 Piggyback board top view

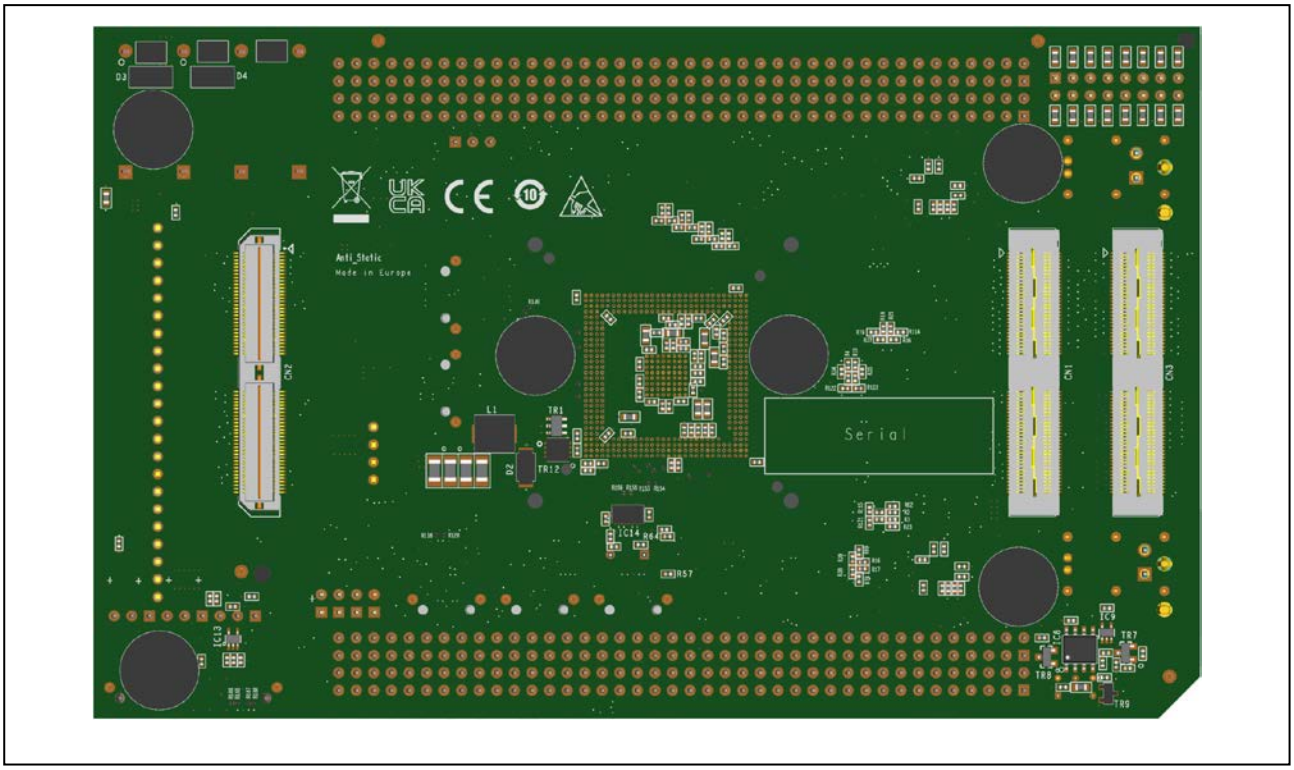


Figure 1.2 D018177_06_V01 Piggyback board bottom view

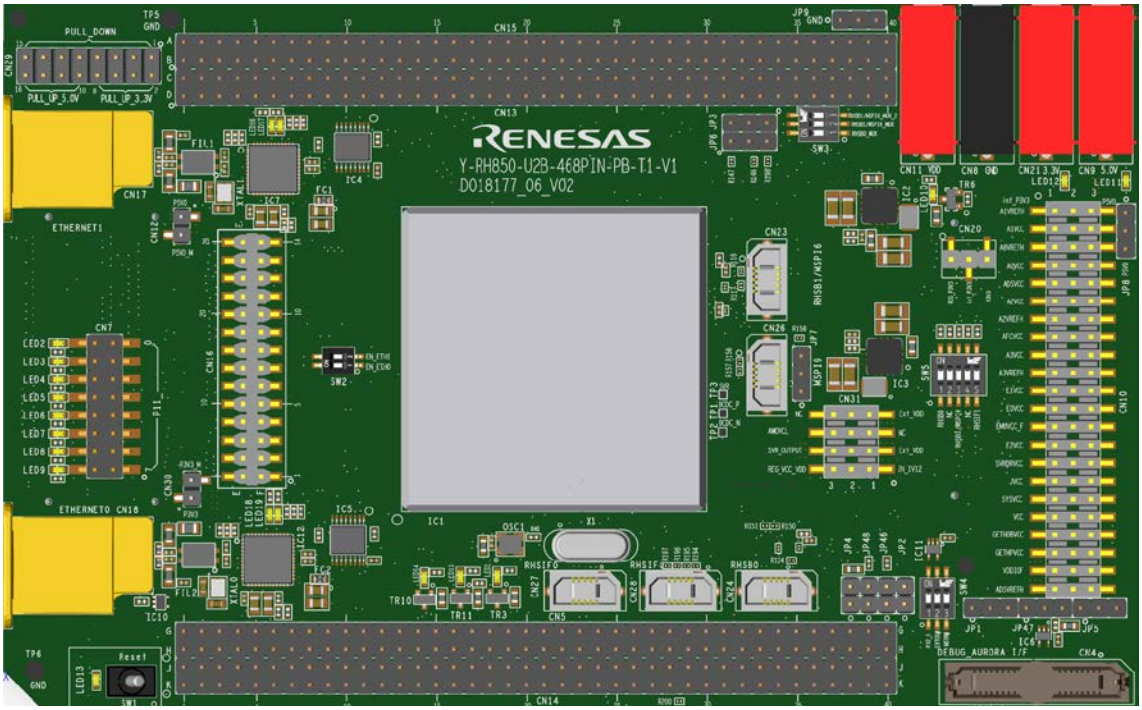


Figure 1.3 D018177_06_V02 Piggyback board top view

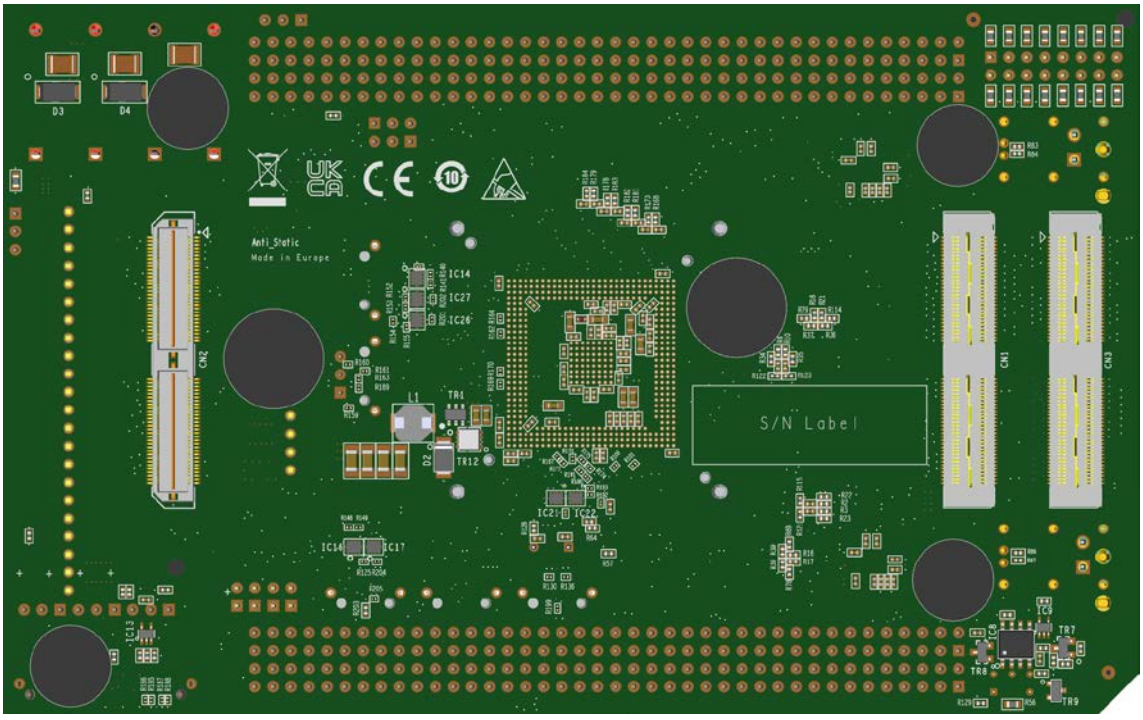


Figure 1.4 D018177_06_V02 Piggyback board bottom view

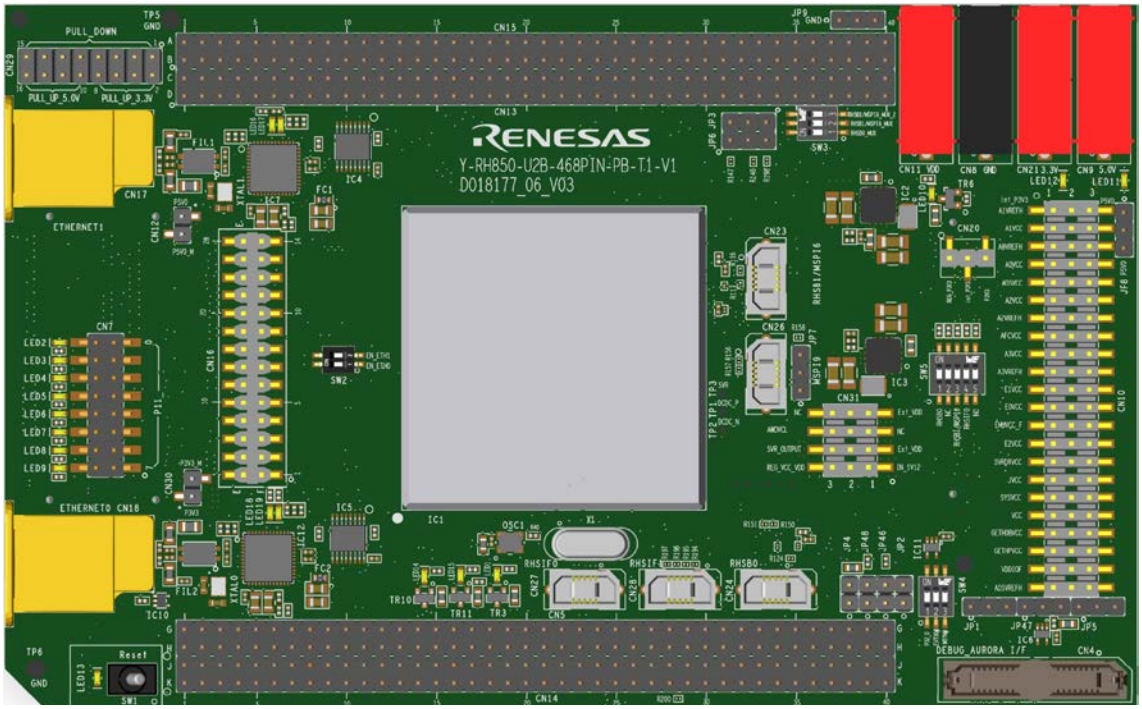


Figure 1.5 D018177_06_V03 Piggyback board top view

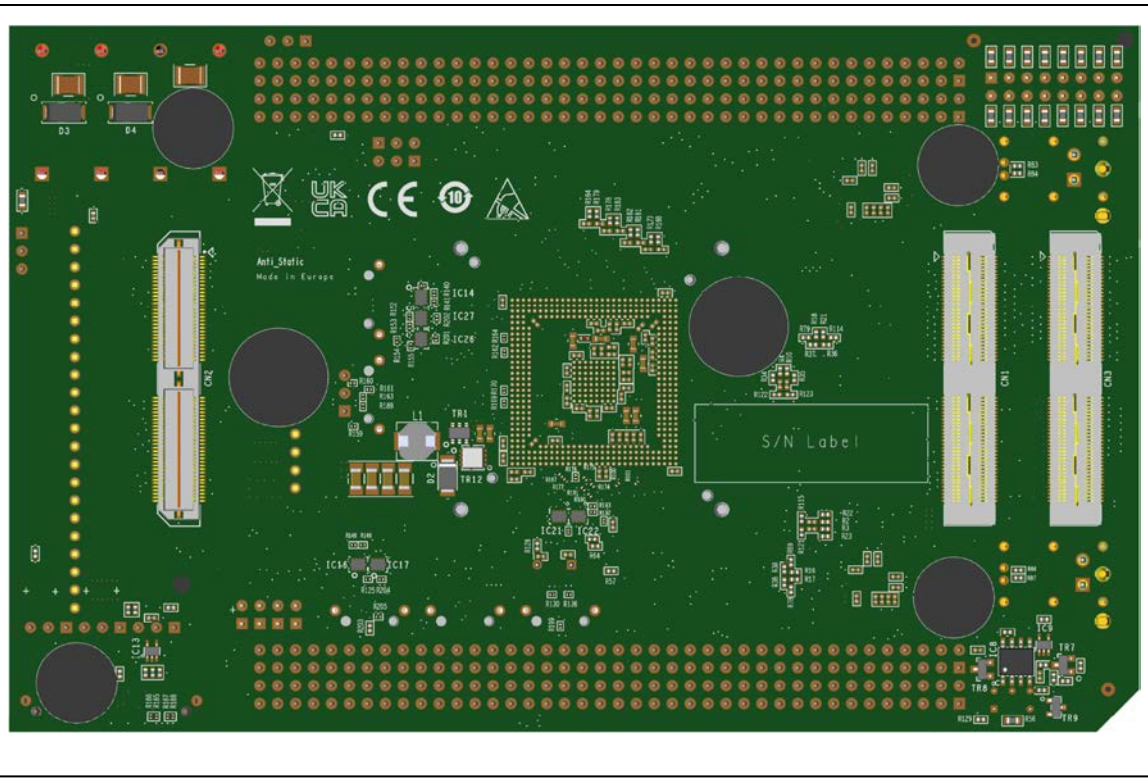


Figure 1.6 D018177_06_V03 Piggyback board bottom view

Following figures provide the drawing of top and bottom views of the piggyback board.

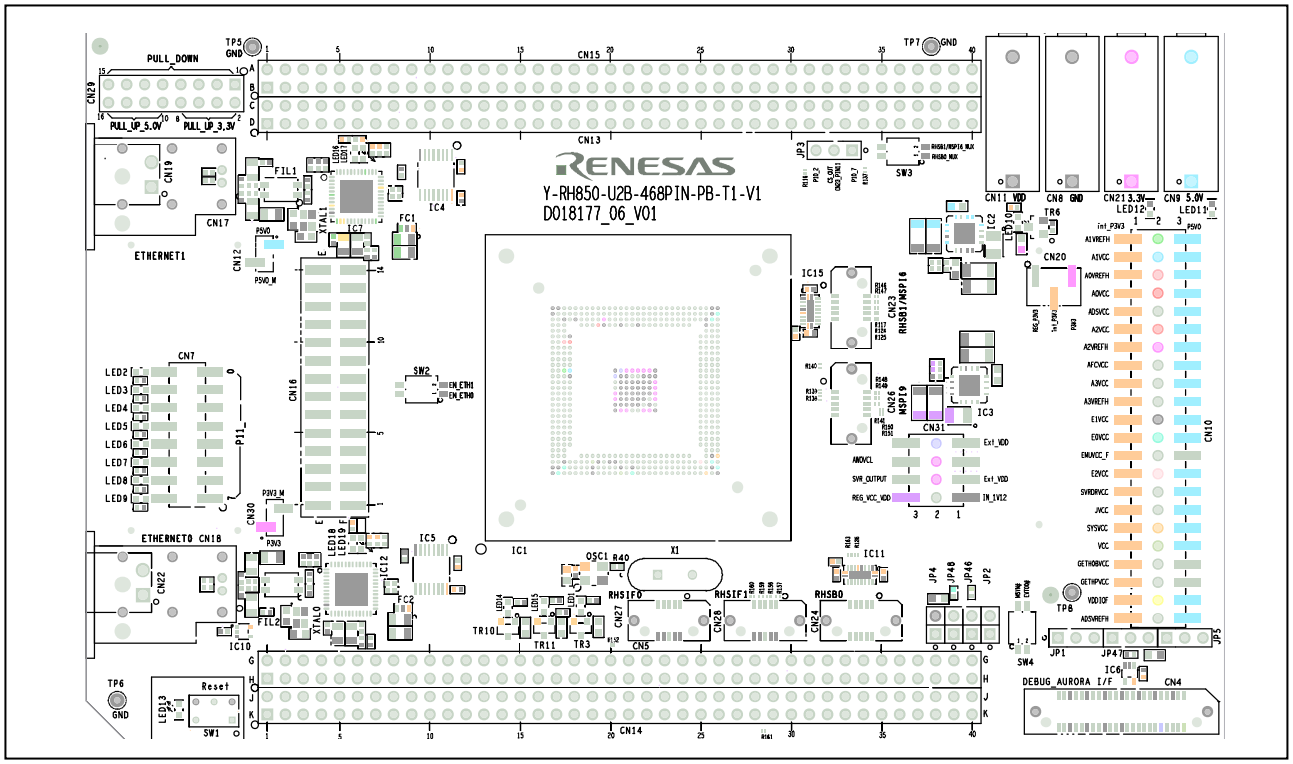


Figure 1.7 D018177_06_V01 Piggyback Board top view

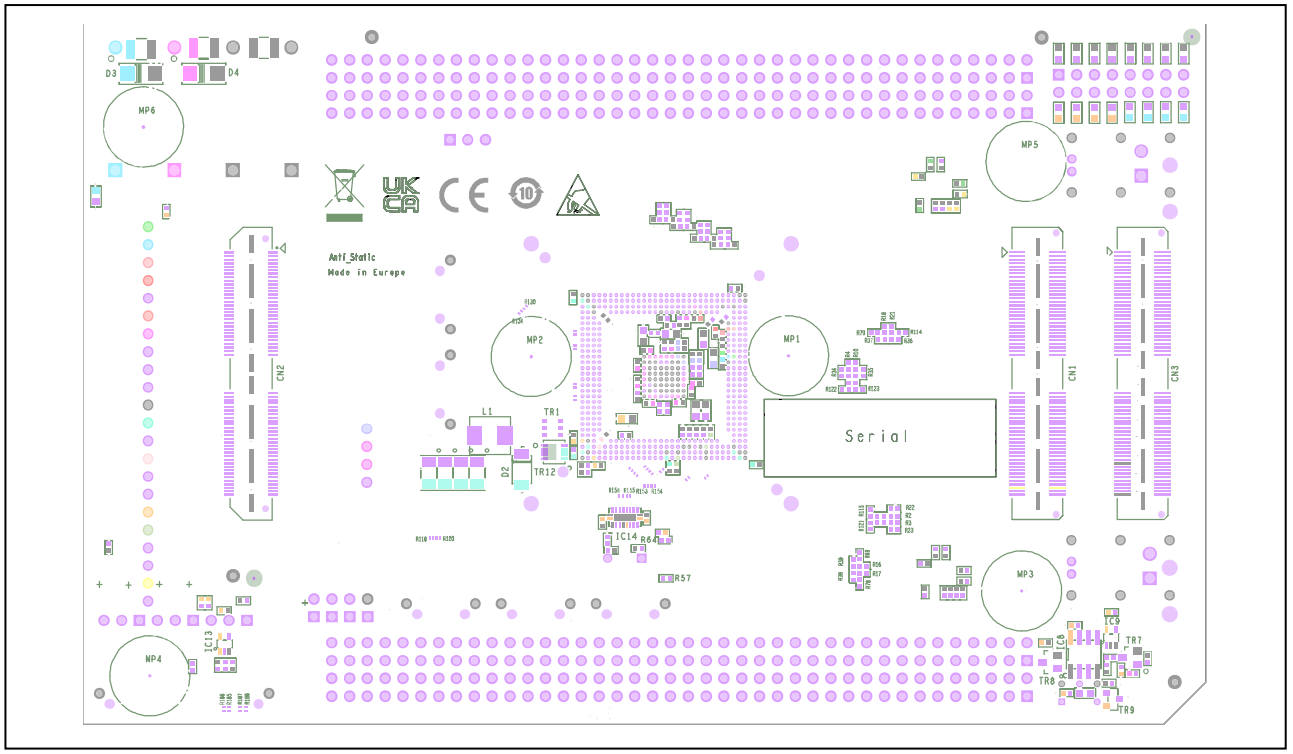


Figure 1.8 D018177_06_V01 Piggyback Board bottom view

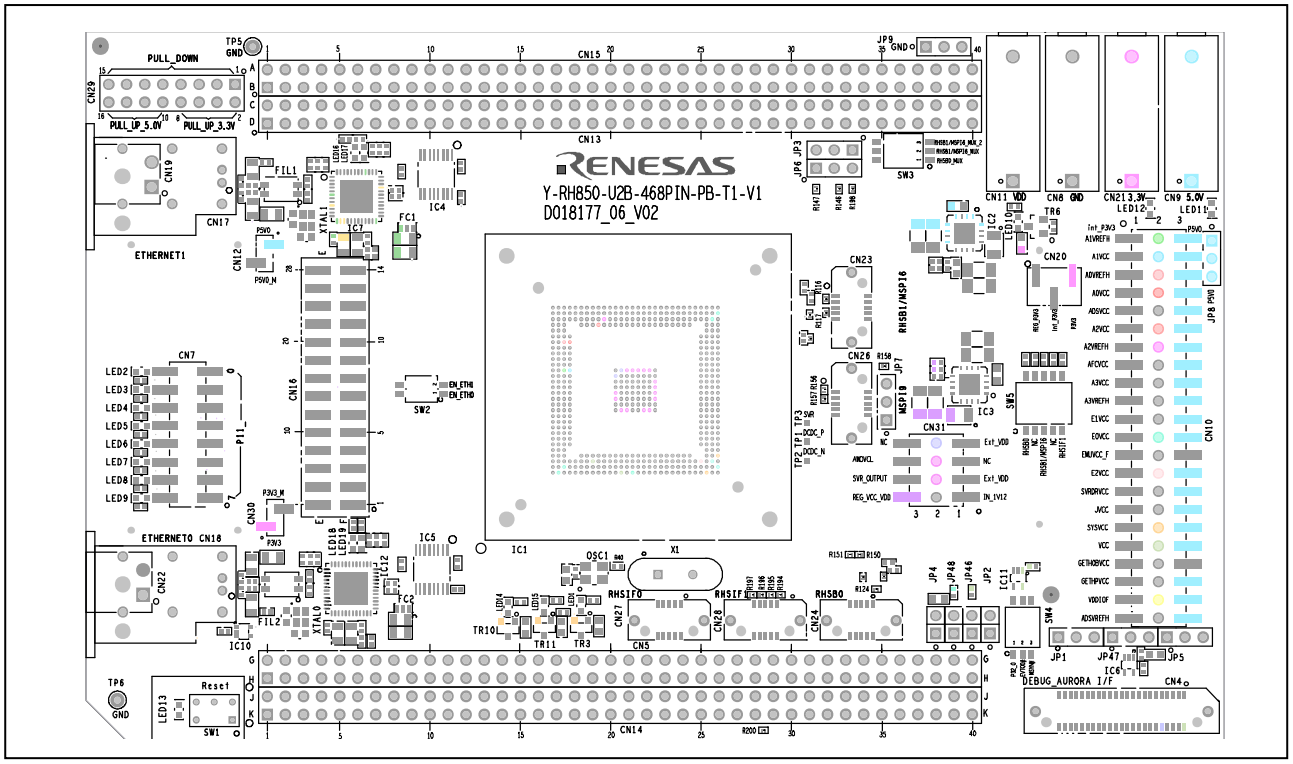


Figure 1.9 D018177_06_V02 Piggyback Board top view

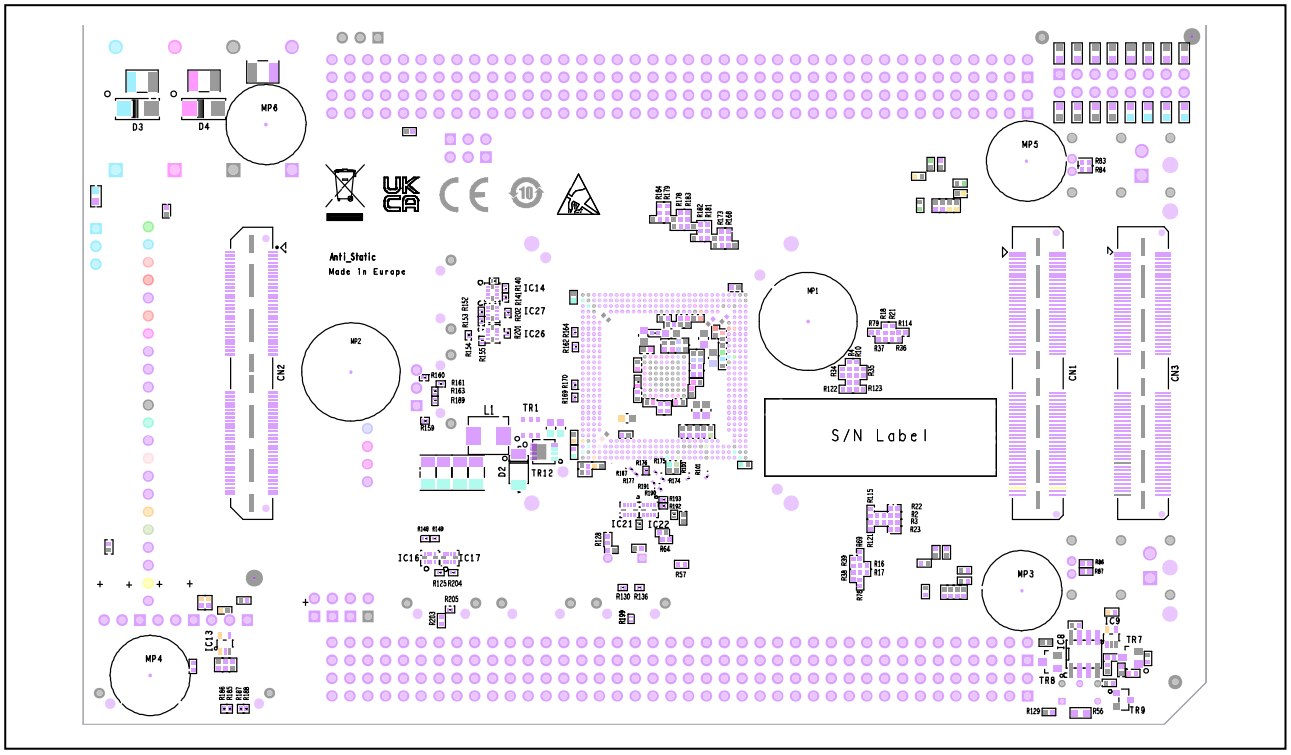


Figure 1.10 D018177_06_V02 Piggyback Board bottom view

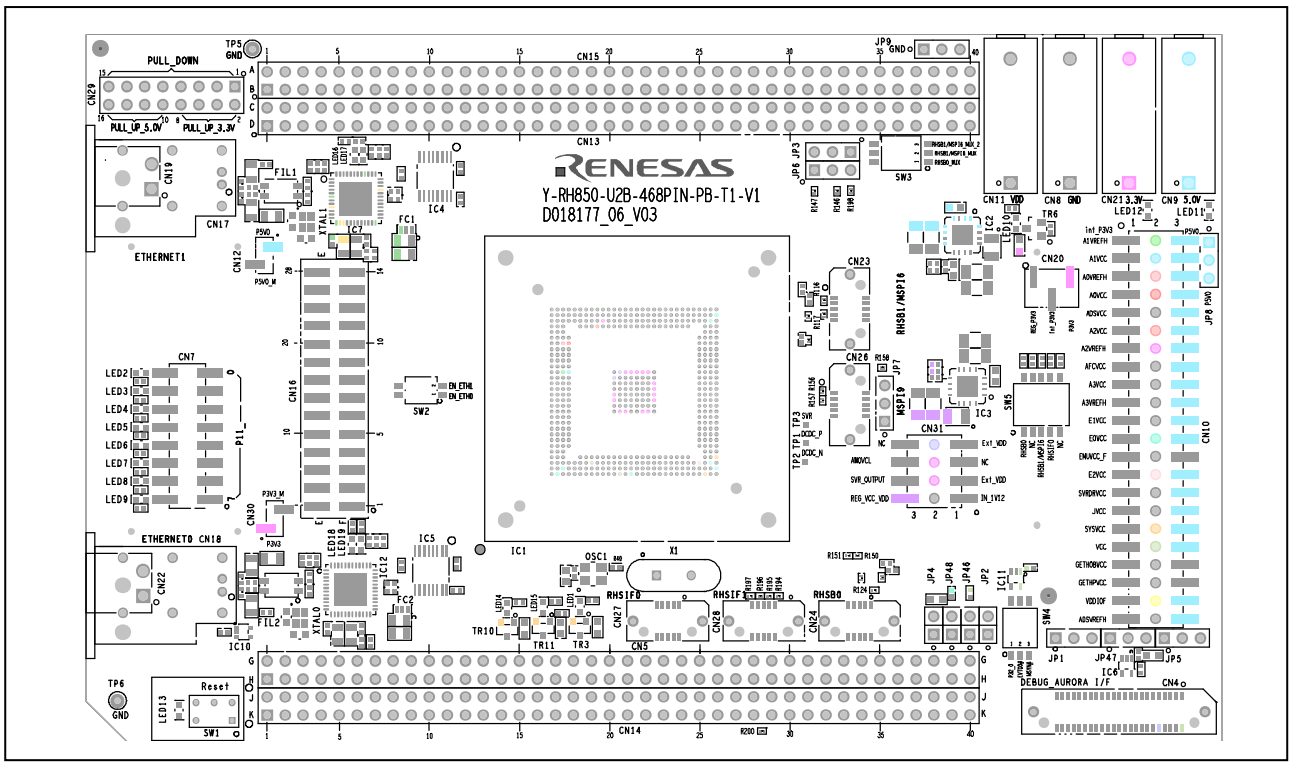


Figure 1.11 D018177_06_V03 Piggyback Board top view

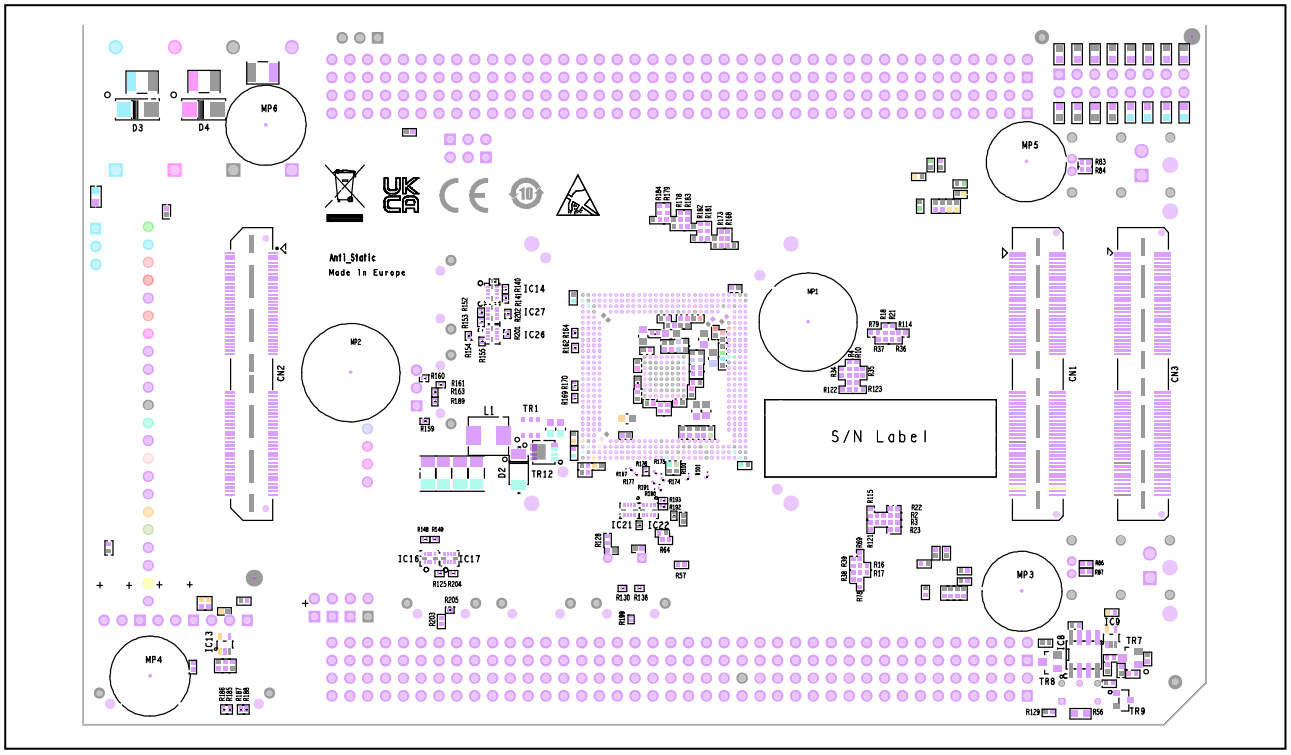


Figure 1.12 D018177_06_V03 Piggyback Board bottom view

1.6 Mounting of the Device

The board is designed for use with the devices listed in table 1.4.

Table 1.4 Devices that can be used with Y-RH850-U2B-468pin-PB-T1-V1

	FCC device	MP device	Comments
RH850/U2B	R7F702Z2*EDBG	TBD	FCC: Sixth through ninth characters of the part name indicate U2Bx-FCC(BGA468) PKG: The last 2 characters of the part name indicate BGA468.

The device must be placed inside the socket IC1. To insert the device, align the device package A1 pin with the marking of the socket.
The A1pin of the socket is marked with a circle near to the "IC1" label (see also white circle or white point in *Figure 1.1 D018177_06_V01 Piggyback* board top view, *Figure 1.3 D018177_06_V02 Piggyback board top view, Figure 1.5 D018177_06_V03 Piggyback board top view*).
On the device the index area is available on the corner near the A1 pin.

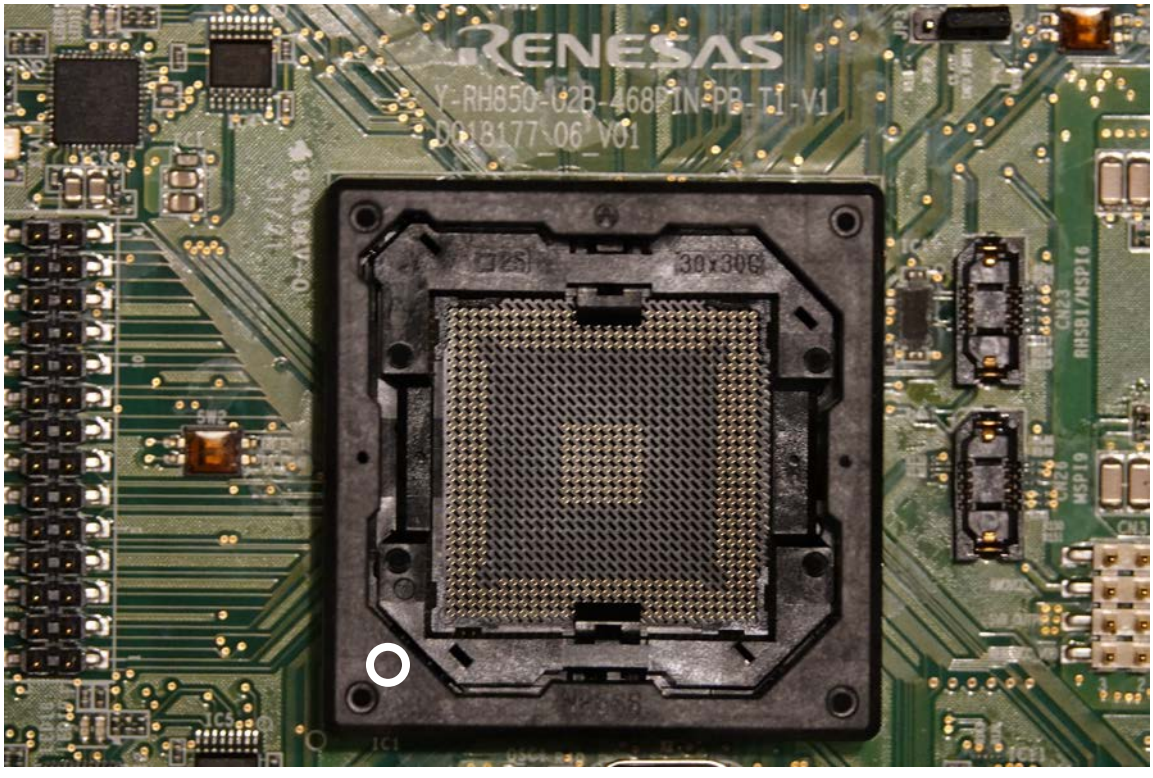


Figure 1.13 Yamaichi NP566-468-049-X socket

CAUTION

Be careful with the device placement in the socket to avoid damage of the device.

2. Jumpers, Connectors, Switches and LEDs

This section provides complete lists of all jumpers, connectors, and LEDs.

The placement of these components on the board is depicted in the figure below.

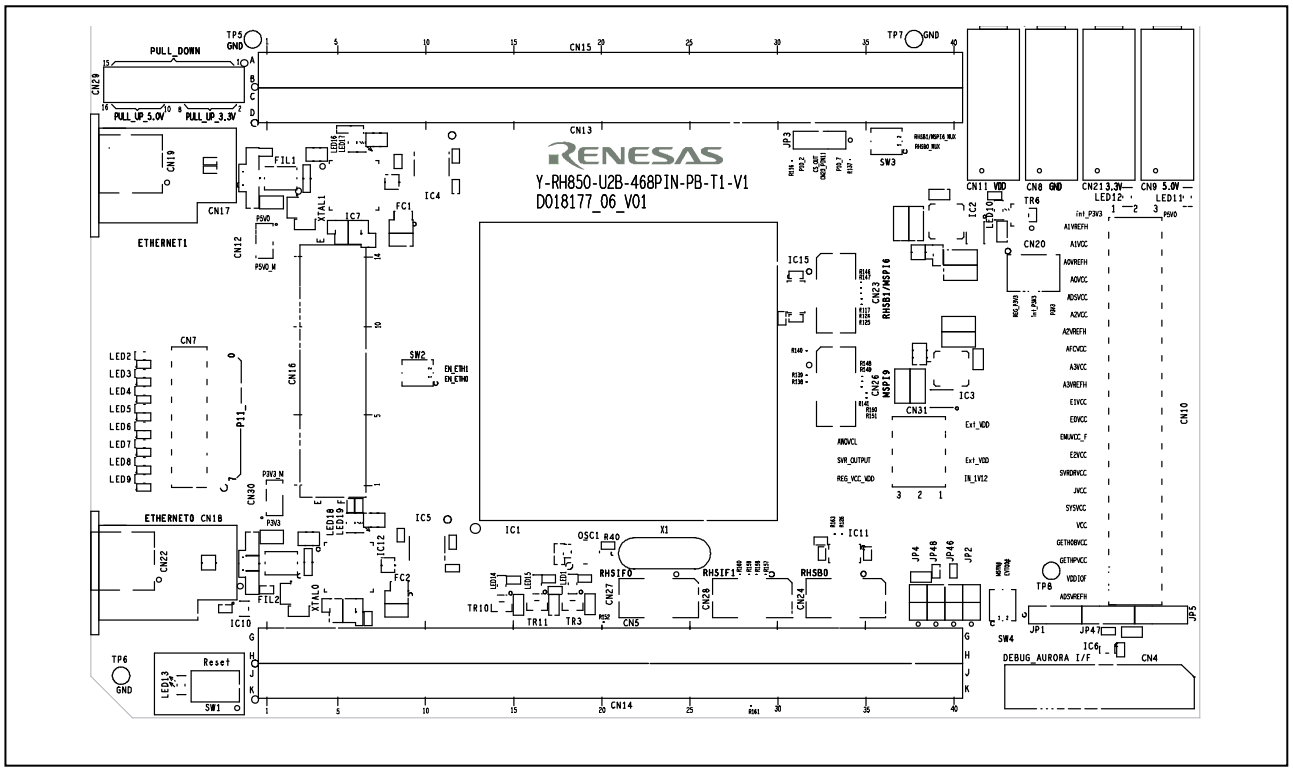


Figure 2.2 D018177_06_V01 Placement of jumpers, connectors and LEDs on top side

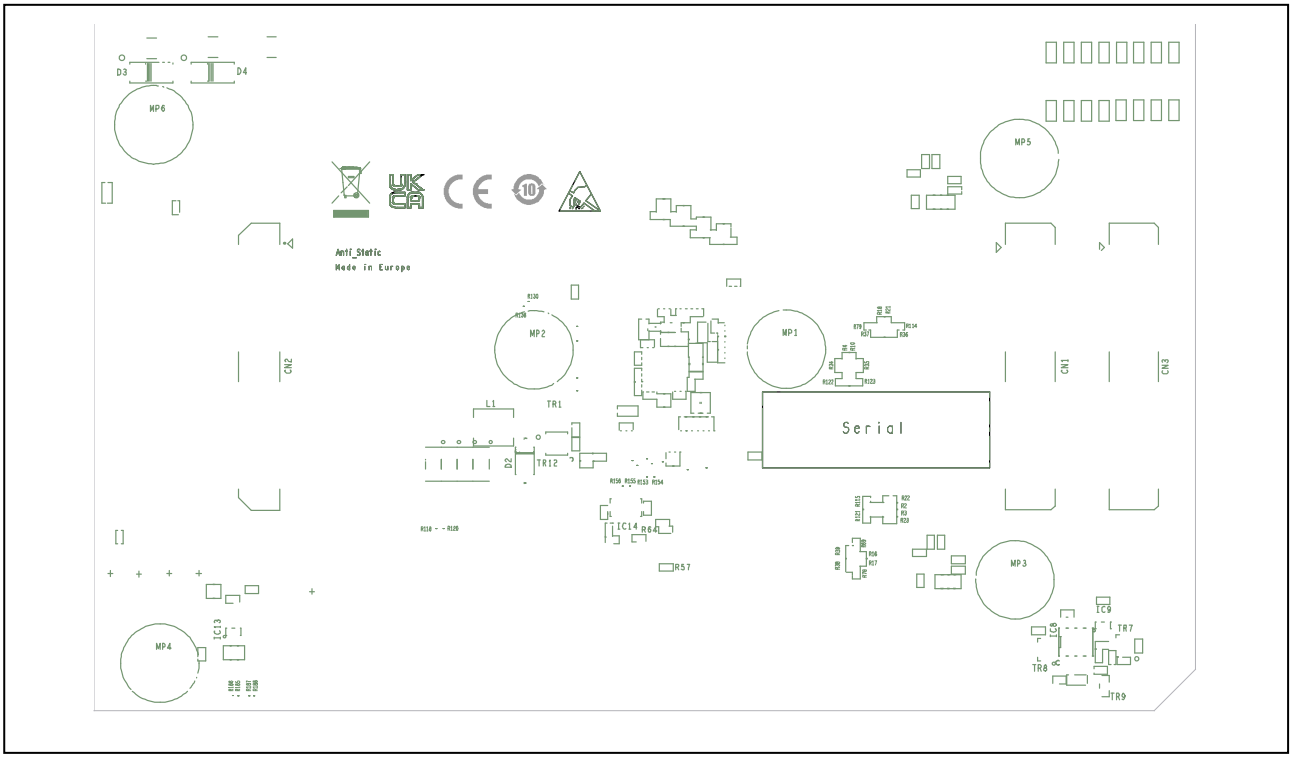


Figure 2.1 D018177_06_V01 Placement of connectors on bottom side

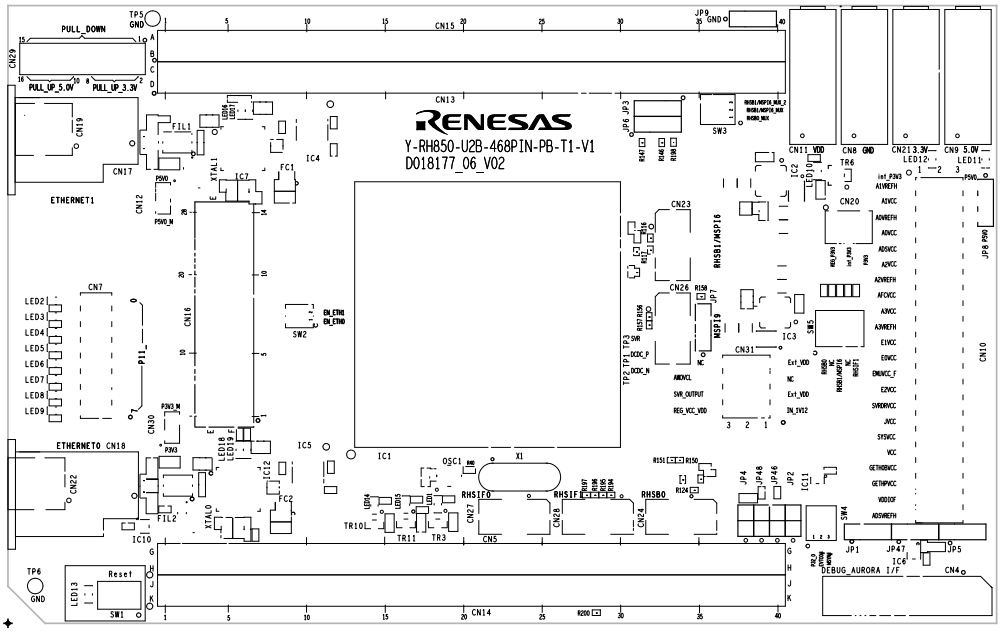


Figure 2.3 D018177_06_V02 Placement of jumpers, connectors and LEDs on top side

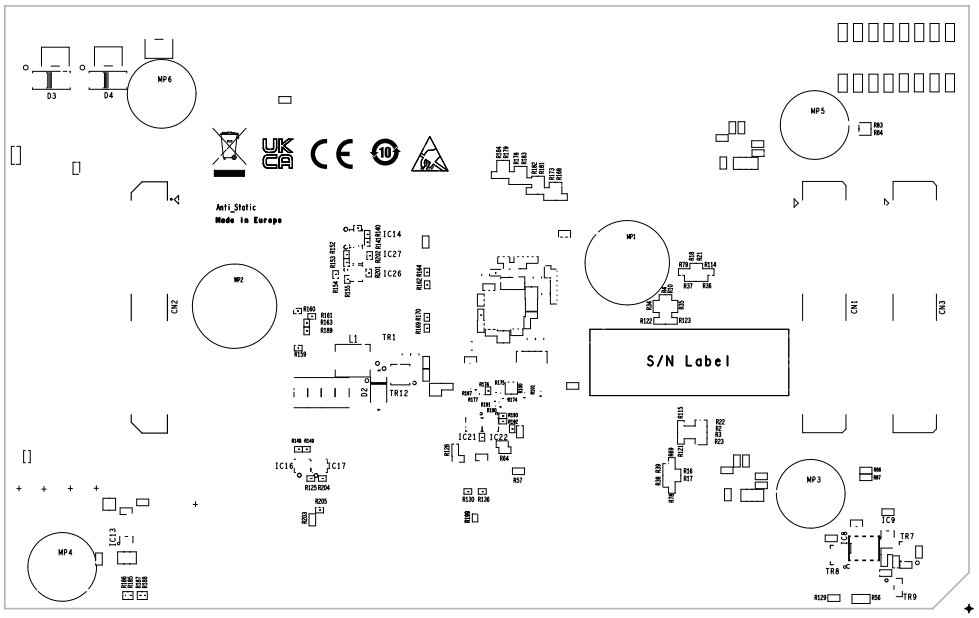


Figure 2.4 D018177_06_V02 Placement of connectors on bottom side

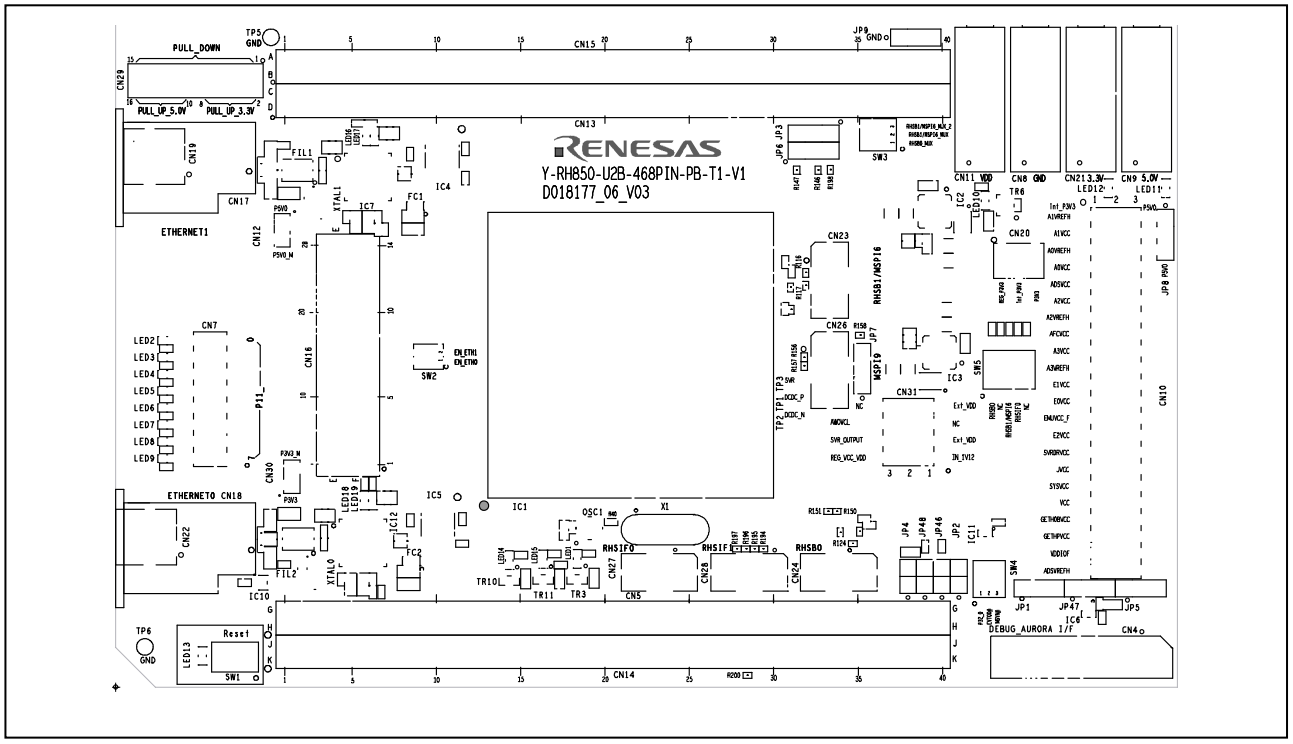


Figure 2.5 D018177_06_V03 Placement of jumpers, connectors and LEDs on top side

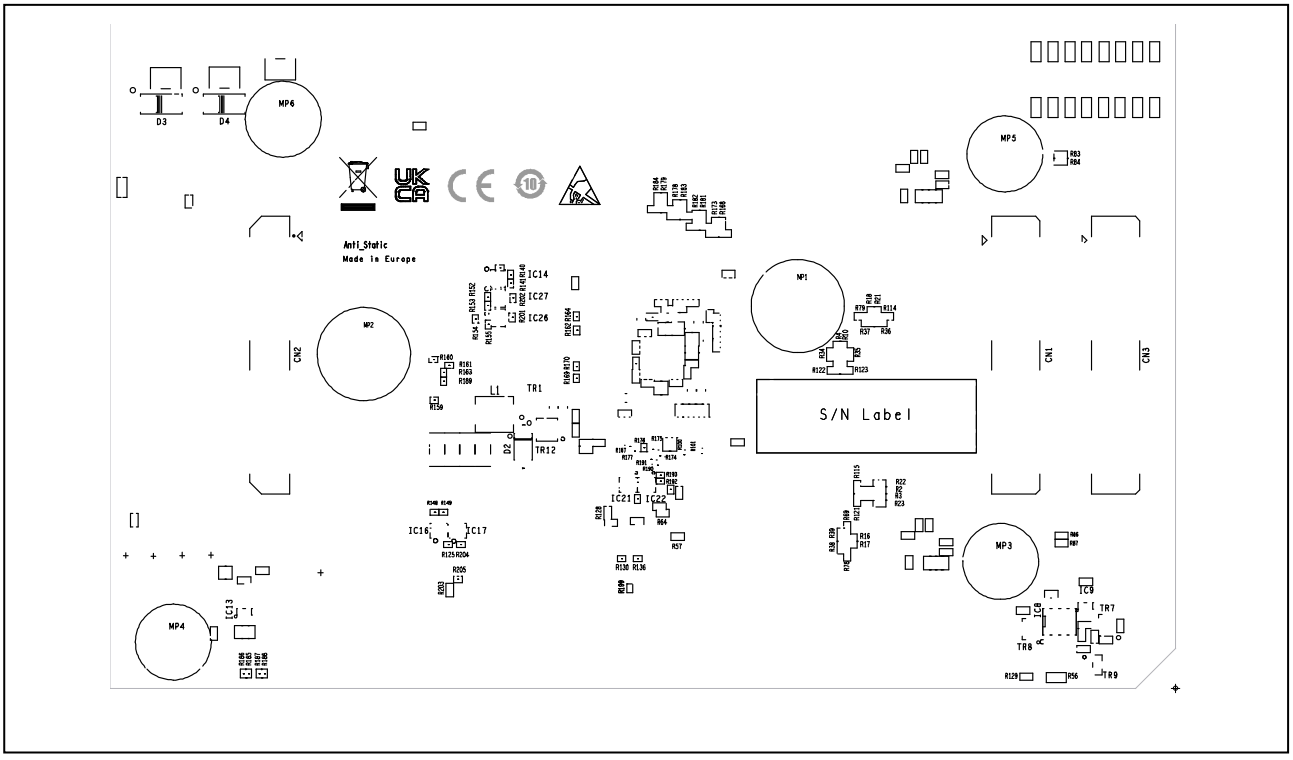


Figure 2.6 D018177_06_V03 Placement of connectors on bottom side

2.1 Jumper Overview

The following table provides an overview of all jumpers.

Table 2.1 Jumper overview

Jumper	Function	Remark
JP1	Select signal source for AURORES# input on RH850/U2B • JP1[2-1]: TRST# signal from Aurora debug I/F connector CN4 • JP1[2-3]: AURORES#_VCC signal from Aurora debug I/F connector CN4	refer to *5 Debug and Flash Programming Interfaces*
JP2	Enable signaling of PWRCTL for SYSVCC • JP2[1-2]: PWRCTL control of SYSVCC is signaled by LED15	refer to *6.1 Operation Mode Selection*
JP3, JP6[2)]	[1)] Select port for CS_OUT signal on CN23.5 [2)] Select port for CS_OUT/SSI_IN signal on CN23.6 • JP3[1-2]: connect to RHSB1CSD0 (P10_7) • JP3[2-3]: connect to MSPI6CSS0 (P11_2) [1)] o JP6[1-2][2)]: connect to MSPI6CSS0 (P11_2) o JP6[2-3][2)]: connect to MSPI6SSI (P12_4)	refer to *6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6* and *7.5 RHSB1/MSPI6 Connector CN23*
JP4	Swap TX and RX signals of RHSIF0 interface available at CN27	refer to *7.8 RHSIF0 Connector CN27*
JP5	Select signal source for TRST# signal • JP5[1-2]: Fix TRST# signal to SYSVCC • JP5[2-3]: TRST# signal is TRST# input from Aurora debug interface connector (pin 12 on connector CN4)	refer to *5 Debug and Flash Programming Interfaces*
JP8[2)]	Pin header for access to P5V0	Available at board versions other than D018177_06_V01
JP9[2)]	Pin header for access to GND	
JP46	Change FLMD0 signal to “H”.	refer to *6.1 Operation Mode Selection*
JP47	SBMD input selection • JP47[1-2]: connect to SYSVCC • JP47[2-3]: connect to GND	
JP48	Change FLMD1 signal to “H”.	
CN7	Enable LED outputs	refer to *6.3 Signalling LEDs*
CN10	Select +3.3 V / +5.0 V power supply configuration	refer to *3.2 Voltage Distribution*
CN12	Enable +5.0 V power supply from main board	refer to *3.1 Board Power Connection*
CN20	Select +3.3 V power supply source • CN20[1-2]: Get 3.3 V from onboard voltage regulator • CN20[2-3]: Get 3.3V from external power supply CN21 or from main board	refer to *3.2 Voltage Distribution*
CN30	Enable +3.3 V power supply from main board	refer to *3.1 Board Power Connection*
CN31	Device core voltage configuration	refer to *3.3 Device Core Voltage (VDD) Selection*

[1)] On board version D018177_06_V01

[2)] On board versions other than D018177_06_V01

2.2 Connector Overview

The following table provides an overview of all connectors.

Table 2.2 Connector overview

Connector	Function	Remark
CN1	Main board connectors	refer to *7.1 Connectors to the Main Board CN1 to* CN3
CN2		
CN3		
CN4	Debug connector	refer to *5 Debug and Flash Programming Interfaces* and *7.2 Debug Connector CN4*
CN5	Device ports connector	refer to *7.3 Device Ports Connectors CN5, CN13, CN14, CN15 and CN16*
CN7	Signaling LEDs pin header	refer to *6.3 Signalling LEDs*
CN8	GND external power supply	refer to *3.1 Board Power Connection*
CN9	+5.0 V external power supply	refer to *3.1 Board Power Connection*
CN10	+3.3 V / +5.0 V power supply configuration	refer to *3.2 Voltage Distribution*
CN11	+1.12 V external power supply	refer to *3.1 Board Power Connection*
CN12	+5.0 V power supply from main board	refer to *3.1 Board Power Connection*
CN13	Device ports connector	refer to *7.3 Device Ports Connectors CN5, CN13, CN14, CN15 and CN16*
CN14		
CN15		
CN16		
CN17	Ethernet interface connector	refer to *6.10 Automotive Ethernet Interface*
CN18		
CN19		
CN20	+3.3 V power supply configuration	refer to *3.2 Voltage Distribution*
CN21	+3.3 V external power supply	refer to *3.1 Board Power Connection*
CN22	Ethernet interface connector	refer to *6.10 Automotive Ethernet Interface*
CN23	RHSB1 / MSPI6 interface connector	refer to *6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6*
CN24	RHSB0 interface connector	refer to *6.5 Renesas High-Speed Bus RHSB0*
CN26	MSPI9 interface connector	refer to *6.7 Renesas Multichannel Serial Peripheral Interface MSPI9*
CN27	RHSIF0 interface connector	Refer to *6.8 Renesas High-Speed Serial I/F RHSIF0*
CN28	RHSIF1 interface connector	refer to *6.9 Renesas High-Speed Serial I/F RHSIF1*
CN29	Pull up / pull down configuration	refer to *6.4 Pull-Up/Pull-Down Pin Header*
CN30	+3.3 V power supply from main board	refer to *3.1 Board Power Connection*
CN31	Device core voltage configuration	refer to *3.3 Device Core Voltage (VDD) Selection*

2.3 Switches Overview

The following table provides an overview of all switches.

Table 2.3 Switches overview

Connector	Function	Remark
SW1	RESET#	refer to *6.2 RESET Switch*
SW2	Enable Ethernet outputs	refer to *6.10 Automotive Ethernet Interface*
SW3	Port selection RHSB0 / RHSB1 / MSPI6	refer to *6.5 Renesas High-Speed Bus RHSB0* and *6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6*
SW5[1)]	Enable control for RHSB0 / RHSB1 / MSPI6 multiplexers.	
SW4	Debug port connection EVTO0 / MSYN#	refer to *5 Debug and Flash Programming Interfaces*

1) On board versions other than D018177_06_V01

2.4 LED Overview

The following table provides an overview of all LED.

Table 2.4 LED overview

LED	Function	Color	Remark
LED1	Device ERROROUT_M# signal	red	
LED2	Signaling LED	yellow	connection via CN7, refer to *6.3 Signalling LEDs*
LED3			
LED4			
LED5			
LED6			
LED7			
LED8			
LED9			
LED10	1.12 V device core voltage VDD	green	refer to *3.4 Power Supply LEDs*
LED11	5.0 V power supply P5V0	green	
LED12	3.3 V power supply int_P3V3	green	
LED13	Reset switch SW1 on	red	refer to *6.2 RESET Switch*
LED14	Device VMONOUT# signal	red	
LED15	Device PWRCTL signal	red	
LED16	Ethernet channel 1 activity LED	red	refer to *6.10 Automotive Ethernet Interface*
LED17		green	
LED18	Ethernet channel 0 activity LED	red	refer to *6.10 Automotive Ethernet Interface*
LED19		green	

3. Power Supply

3.1 Board Power Connection

The device and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board
- 5.0 V in case some ports shall be operated with 5.0 V I/O voltage
- 1.12 V for the device's VDD core voltage supply
  Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Note

Within this document all voltage values are considered as 'typical'.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

The following connectors are available to supply external voltages:

- Four 4 mm 'banana-type' connectors are used to connect external power supplies:
  - black connector CN8 for GND (VSS)
  - red connector CN9 for 5 V
  - red connector CN21 for 3.3 V
  - red connector CN11 for 1.12 V
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
    Connector CN11 is not assembled at delivery of the board, but separately supplied with the board package.

In case the piggyback board is mounted on a main board, all voltages except for 1.12 V (VDD) can be supplied by the main board. The jumpers CN12 (5.0 V) and CN30 (3.3 V) are used to enable power supply from the main board.

CAUTION

Do not power on the piggyback board when no RH850 microcontroller is installed in socket IC1 because the switching regulator in the SVR power supply circuit doesn't have defined control signals when the microcontroller is not installed and may be damaged.

If you want to power on the piggyback board without microcontroller, make sure jumper CN10[43-44-45] (SVRDRVCC) is open.

If the piggyback board is being used with the microcontroller installed please make sure the ports SVRNGATE and SVRPGATE are set to "Fixed" (output) in bit SVRENDCDCHZ in option byte 25.

Do not supply the 5 V (CN9) and 3.3 V (CN21) voltage directly to the piggyback board in case the power supply from the main board is enabled.

Connecting external 1.12 V via CN11 (and GND via CN8) is still an option also in this case.

For some general power supply scenarios, the jumper settings are described in *8 Jumper Configuration Examples*.

3.2 Voltage Distribution

The following table shows the required device power supply pins and their function:

Table 3.1 Device power supply pins

Device power supply pin	Voltage	Function
E0VCC, E1VCC, E2VCC	3.3 V, 5 V	Power supply for I/O ports
EMUVDD	1.09V	Power supply for debug circuits, only available on FCC devices
EMUVCC	3.3 V	
J0VCC, J1VCC	3.3 V, 5 V	
SYSVCC	3.3 V, 5 V	Power supply for System Logic and internal voltage regulator power I/O ports
VCC	3.3 V, 5 V	Power supply for on-chip flash memory
SVRDRVCC	3.3 V, 5 V	Power supply for on-chip Switching Voltage Regulator (SVR)
SVRAVCC	3.3 V, 5 V	Connected to SYSVCC
LVDVCC	3.3V, 5 V	RHSIF/RHSB supply voltage
OSCVCC	3.3 V, 5 V	Power supply for OSC
GETH0BVCC	3.3 V	Power supply for Ethernet
GETH0PVCC	3.3 V	Power supply for Ethernet
VDDIOF	3.3 V, 5 V	I/O voltage supply for the main board
A0VCC, A1VCC, A2VCC, A3VCC	3.3 V, 5 V	A/D Converter's power supplies and reference voltages
A0VREFH, A1VREFH, A2VREFH, A3VREFH, ADSVREFH	3.3 V, 5 V	
ADSVCC, AFCVCC	3.3 V, 5 V	
VDD	1.09 V	Core supply voltage Refer to *3.3 Device Core Voltage (VDD) Selection*

Each of the above voltages can be selected from 5.0 V or 3.3 V (where applicable, see table above) by a set of jumpers.

The supply for 3.3 V can be selected from external power supply / main board power supply or from the onboard voltage regulator using jumper CN20:

- CN20 [1-2]: 3.3 V supply comes from the onboard voltage regulator.
- CN20 [2-3]: 3.3 V supply comes from the external power supply or from the main board power supply.

Table 3.2 Voltage Selection shows which jumpers to set to select the different device supply voltages, and *Figure 3.1 Voltage distribution* shows the schematic for it.

Table 3.2 Voltage Selection

Device power supply pin	Connection for 3.3 V	Connection for 5.0 V
A1VREFH	CN10 [1-2]	CN10 [2-3]
A1VCC	CN10 [4-5]	CN10 [5-6]
A0VREFH	CN10 [7-8]	CN10 [8-9]
A0VCC	CN10 [10-11]	CN10 [11-12]
ADSVCC	CN10 [13-14]	CN10 [14-15]
A2VCC	CN10 [16-17]	CN10 [17-18]
A2VREFH	CN10 [19-20]	CN10 [20-21]
AFCVCC	CN10 [22-23]	CN10 [23-24]
A3VCC	CN10 [25-26]	CN10 [26-27]
A3VREFH	CN10 [28-29]	CN10 [29-30]
E1VCC	CN10 [31-32]	CN10 [32-33]
E0VCC (LVDVCC)	CN10 [34-35]	CN10 [35-36]
EMUVCC	CN10 [37-38]	---
E2VCC	CN10 [40-41]	CN10 [41-42]
SVRDRVCC	CN10 [43-44]	CN10 [44-45]
J0VCC, J1VCC	CN10 [46-47]	CN10 [47-48]
SYSVCC (SVRAVCC)	CN10 [49-50]	CN10 [50-51]
VCC (OSCVCC)	CN10 [52-53]	CN10 [53-54]
GETH0BVCC	CN10 [55-56]	--- *
GETH0PVCC	CN10 [58-59]	---
VDDIO	CN10 [61-62]	CN10 [62-63]
ADSVREFH	CN10 [64-65]	CN10 [65-66]

CN10

	int_P3V3		P5V0
A1VREFH	1	2	3
A1VCC	4	5	6
A0VREFH	7	8	9
A0VCC	10	11	12
ADSVCC	13	14	15
A2VCC	16	17	18
A2VREFH	19	20	21
AFCVCC	22	23	24
A3VCC	25	26	27
A3VREFH	28	29	30
E1VCC	31	32	33
E0VCC	34	35	36
EMUVCC	37	38	39
E2VCC	40	41	42
SVRDRVCC	43	44	45
J0VCC[1)]/JVCC[2)]	46	47	48
SYSVCC	49	50	51
VCC	52	53	54
GETH0BVCC	55	56	57
GETHPVCC	58	59	60
VDDIOF	61	62	63
ADSVREFH	64	65	66

Note * CN10 [56-57]: Connected to GND via 4.7kΩ pull-down

1) In board version D018177_04_V01

2) In board versions other than D018177_04_V01

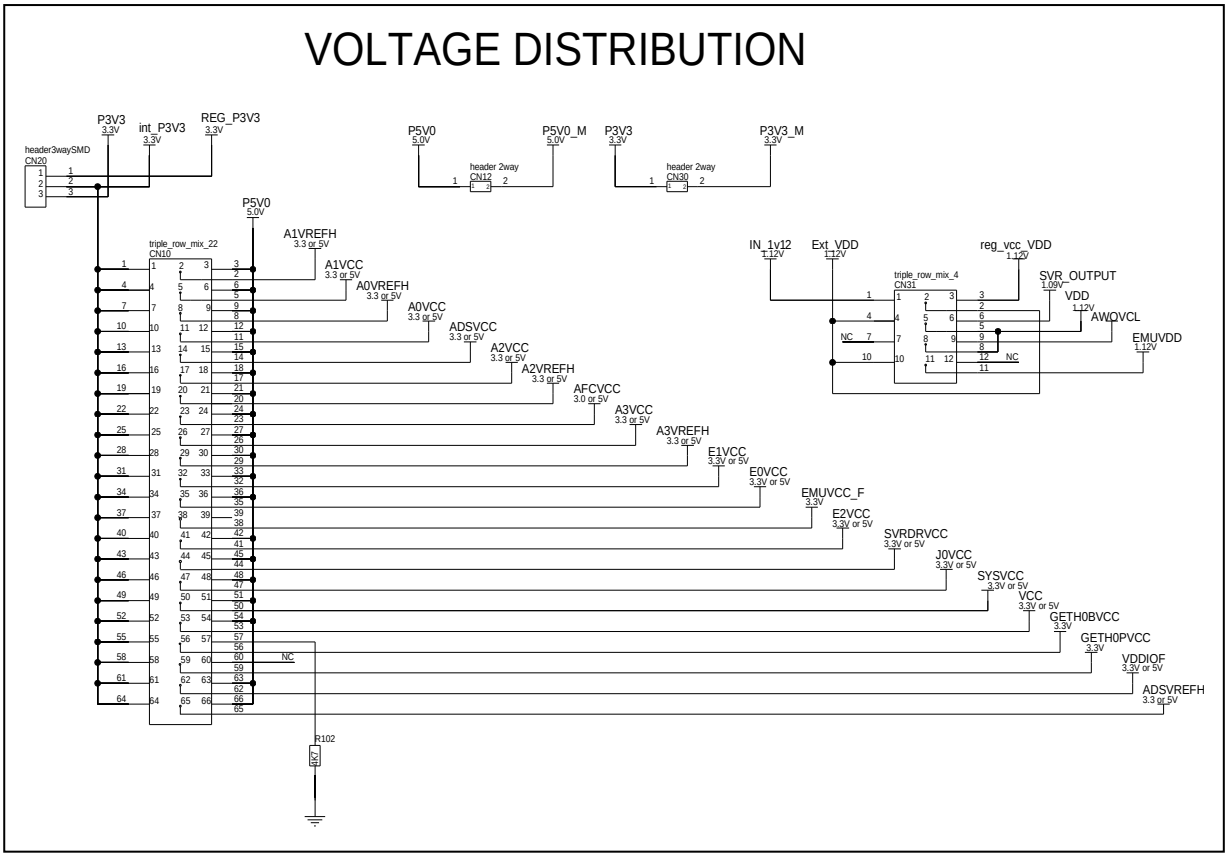


Figure 3.1 Voltage distribution on board version D018177_06_V01

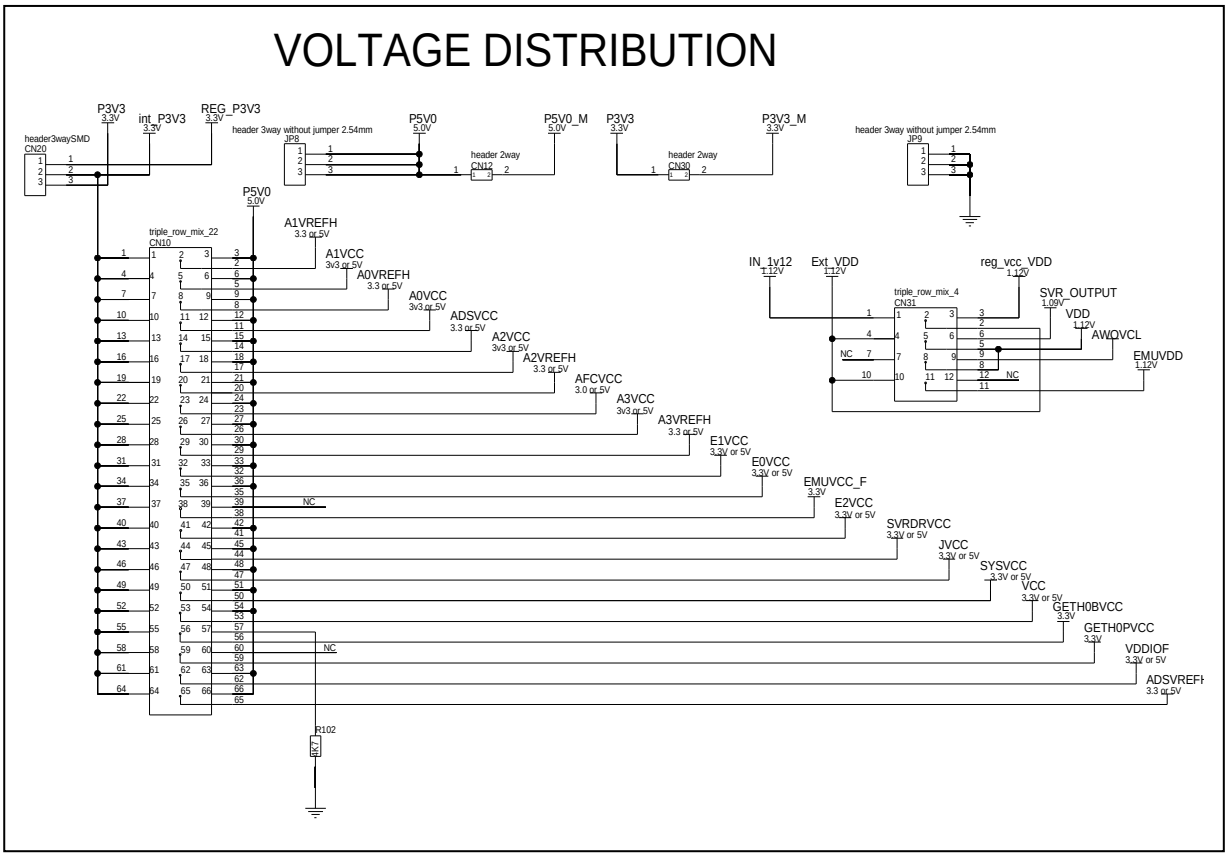


Figure 3.2 Voltage distribution on board versions other than D018177_06_V01

3.3 Device Core Voltage (VDD) Selection

The device core voltage VDD (typ.1.12 V) can be

- supplied from external via CN11 (voltage IN_1v12)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC3 (voltage reg_vcc_VDD)
- generated by the on-chip Switching Voltage Regulator (SVR) in combination with device external power transistors TR1, TR12 (voltage SVR_OUTPUT)

Note

The IN_1v12 and reg_vcc_VDD voltages have a level of typical 1.12 V, which is higher than the typical device core voltage VDD of 1.09 V. The 30 mV difference is supposed to compensate voltage drops over the power rails on the board, in particular over the jumpers.

Selection of the VDD source is achieved by use of the jumpers in CN31:

CN31[1-2]: Ext_VDD = IN_1v12

CN31[2-3]: Ext_VDD = reg_vcc_VDD

CN31[4-5]: VDD = Ext_VDD

CN31[5-6]: VDD = SVR_OUTPUT

CN31[10-11] enables the output of the supply voltage to the device debug circuit EMUVDD.

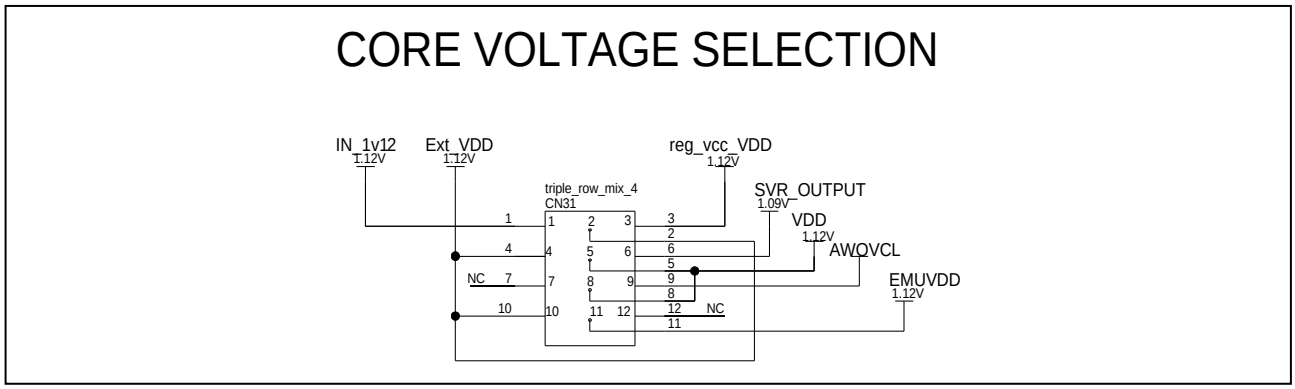


Figure 3.3 Device core voltage (VDD) selection

3.4 Power Supply LEDs

The following green LEDs indicate the presence of various voltages on the piggyback board:

- LED10 for 1.12 V device core voltage VDD
- LED11 for 5.0 V power rail P5V0
- LED12 for 3.3 V power rail P3V3

4. Clock Supply

The device's operation clock can be generated by

- the on-chip main oscillator circuit in combination with an off-chip resonator, connected to the X1, X2 terminals
- an off-chip oscillator, the clock is fed into the X1 terminal

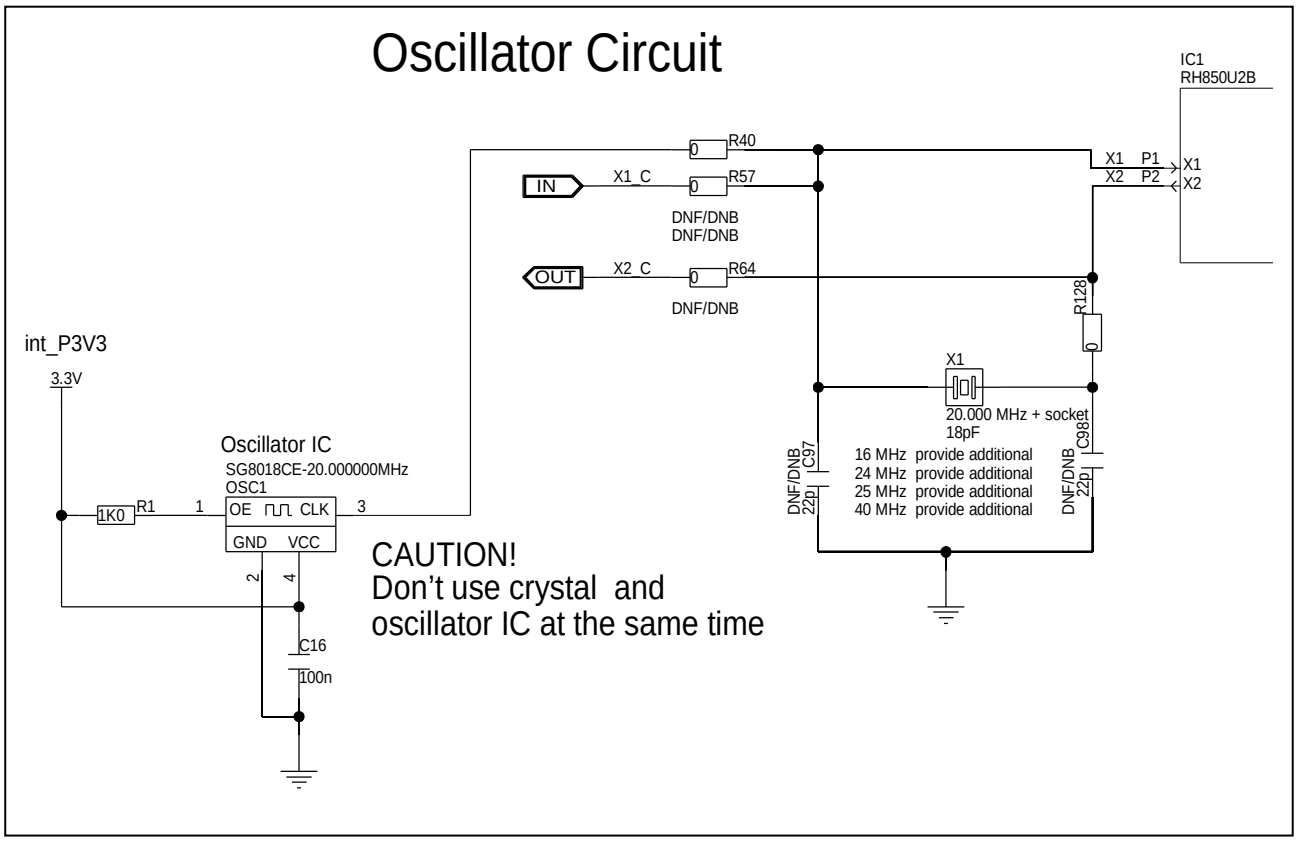


Figure 4.1 Clock supply

4.1 Main Oscillator

For operating the on-chip main oscillator the piggyback board provides a socket (X1) for a resonator.

Several resonators for various main oscillator frequencies (16 MHz, 20 MHz, 24 MHz, 25MHz, 40 MHz) are included in the board package.

The 20MHz resonator is by default mounted to X1.

For package content please refer to *1.1 Package Components*

CAUTION

Only one oscillator, either X1 or OSC1, can be used at any one time for the main oscillator.

4.2 Programmable Oscillator

Instead of using the on-chip main oscillator a programmable crystal oscillator (OSC1) circuit can be used on the board.

The available footprint and circuitry is designed for a SG-8018CE programmable crystal oscillator from Epson Toyocom. The output of this oscillator can be connected to X1 terminal via resistor R40.

For details about the available circuitry, refer to *Figure 4.1 Clock supply*.

CAUTION

A resonator mounted on socket X1 must not be used in parallel to another clock source.

4.3 X1 and X2 on CN14

To minimize disturbance on the resonator signal the device pins X1 and X2 are by default not connected to a pin header. If needed the pins can be connected to CN14 via 0 Ω resistors:

- Device pin X1: Connect to pin 25 of CN14 via R57 to supply an external clock to the device.
- Device pin X2: Connect to pin 26 of CN14 via R64 for measurement purposes of the clock.

5. Debug and Flash Programming Interfaces

For debugging and flash programming purposes debug and flash programming tools can be connected to the CN4 connector.

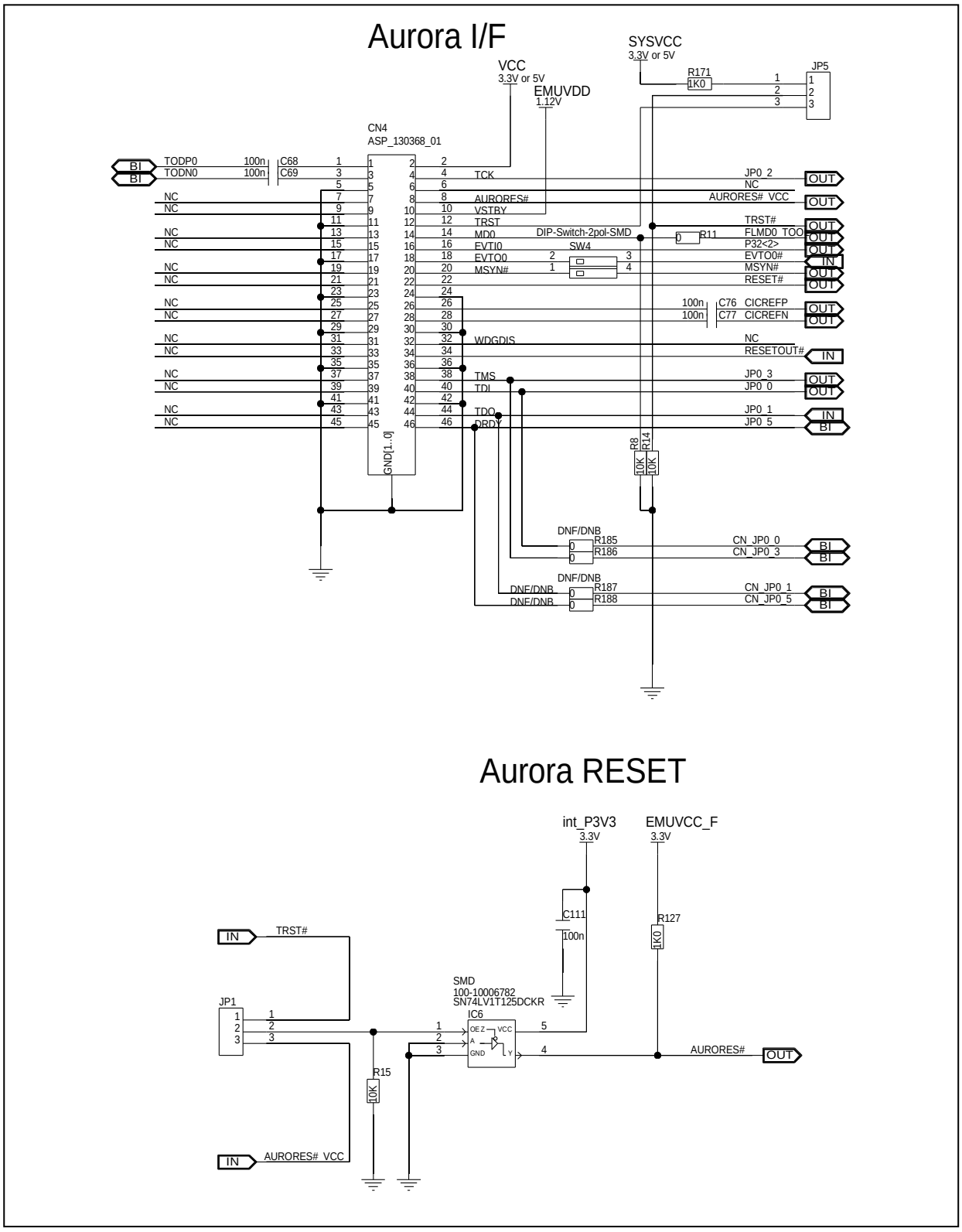


Figure 5.1 Debug connector CN4 and Aurora Reset circuit on board version D018177_06_V01

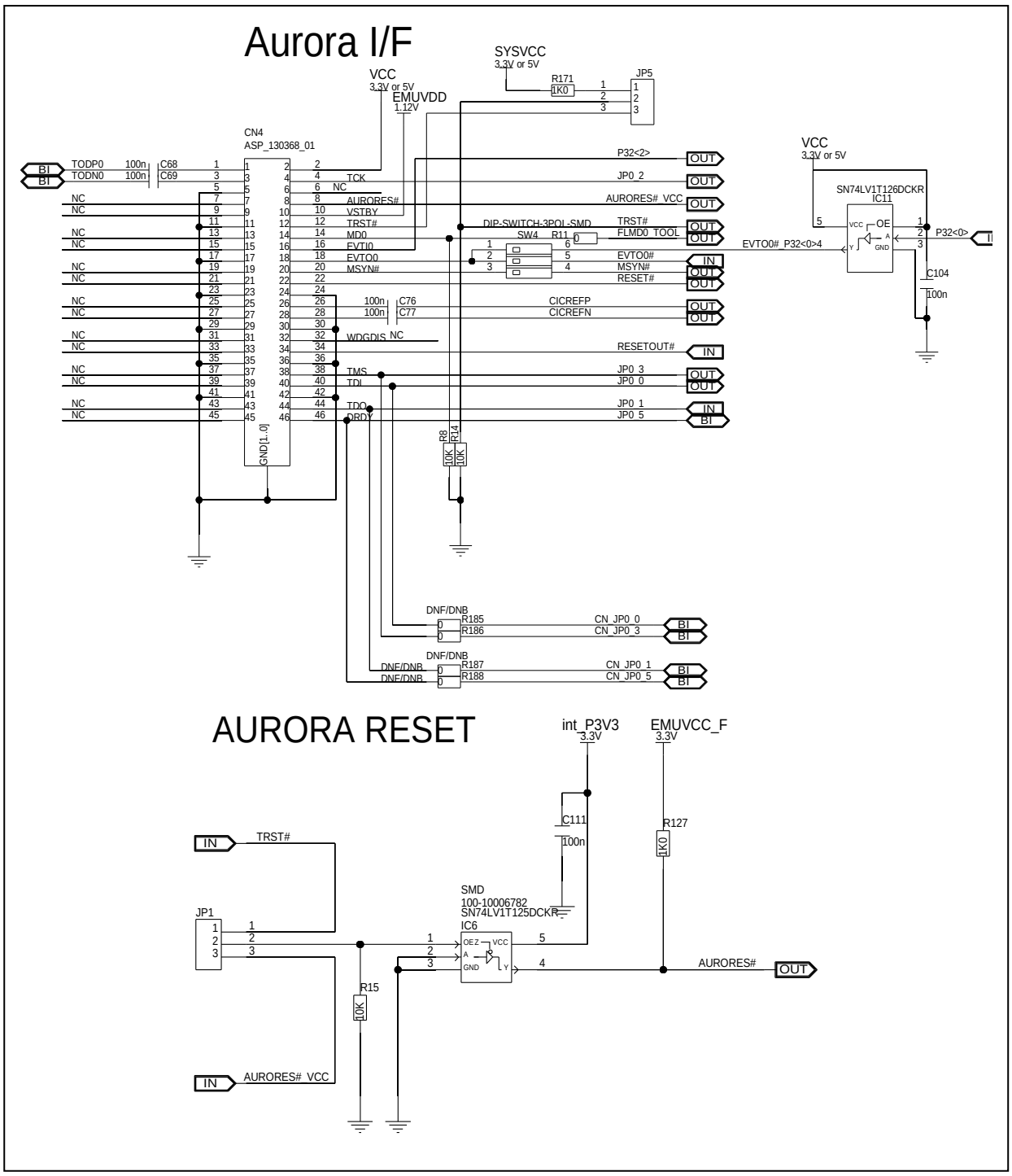


Figure 5.2 Debug connector CN4 and Aurora Reset circuit on board versions other than D018177_06_V01

Refer to *7.2 Debug Connector CN4* for details about the CN4 pin assignment.

Refer to *8.2 Operation using FCC Device or Mass Production Device* for details about the usage of SW4 and its related signals.

The Renesas standard emulator for RH850/U2B is the E2 emulator. This can be used as emulator for debugging or as flash programmer.

To connect the E2 emulator to Y-RH850-U2B-468PIN-PB-T1-V1 you have to use the adapter Y-RH850-DEBUG-ADAPTER-F14T46.

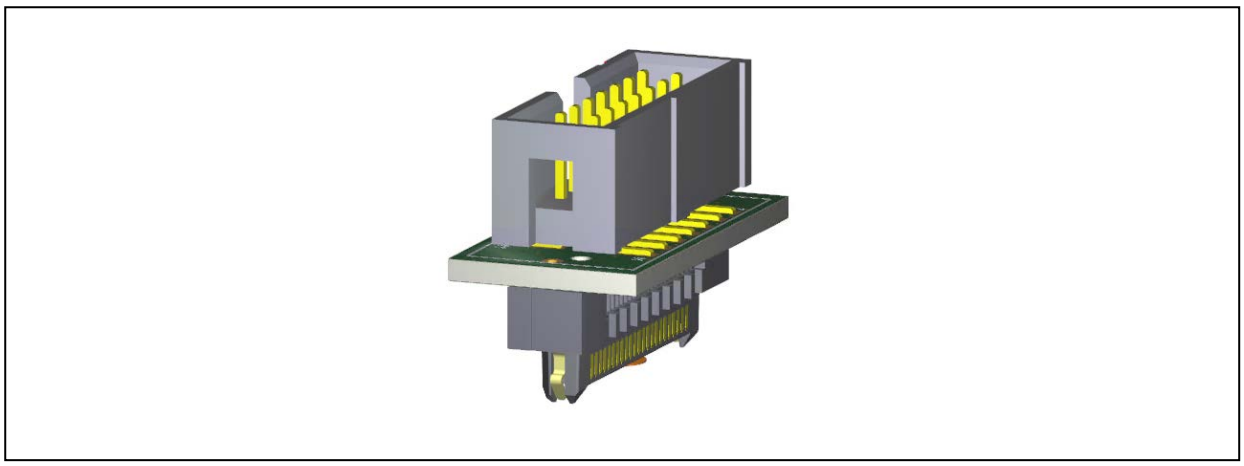


Figure 5.3 Outline view of debug adapter Y-RH850-DEBUG-ADAPTER-F14T46

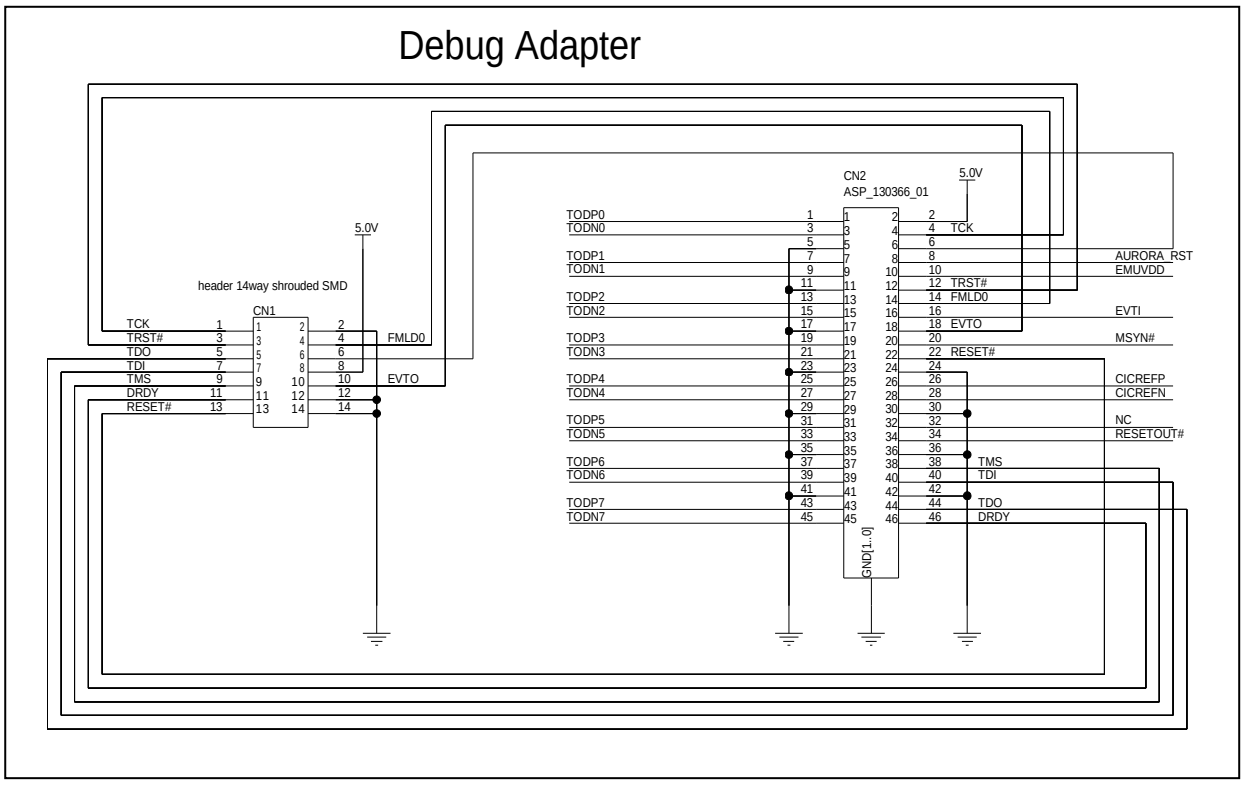


Figure 5.4 Circuit diagram of debug adapter Y-RH850-DEBUG-ADAPTER-F14T46

6. Other Circuitry

6.1 Operation Mode Selection

The piggyback board gives the possibility to configure the following jumpers for selection of the device operation mode.

Table 6.1 Device operation mode selection jumpers

Jumper	Function
JP46	FLMD0 pin level • JP46[SHORT]: FLMD0 = H level; do not connect a debugger or programming tool. • JP46[OPEN]: FLMD0 is - controlled by debugger or programming tool if a tool is connected via CN4 - GND if no tool is connected
JP48	FLMD1 pin level • JP48[SHORT]: FLMD1 = H level • JP48[OPEN]: FLMD1 = GND
JP47	SBMD pin level (RH850/U2B20 and RH850/U2B24 only, for RH850/U2B10 jumper JP47 can be left open) • JP47[1-2]: connect to SYSVCC (SBMD = 1), please leave CN31_9 open (AWOVCL connected to GND via capacitor C47) • JP47[2-3]: connect to GND (SBMD = 0), please connect CN31[8-9] with a jumper (AWOVCL connect to VDD) • JP47[OPEN]: Use for RH850/U2B10 only
JP2	Enable PWRCTL signaling • JP2[SHORT]: PWRT signal is shown on LED15

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User's Manual for details, which modes are specified for the used device.

Note

In most cases the 'normal operating mode' of the device will be used.
This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the 'normal operating mode' of the device, the FLMD0 pin must be pulled low. To do so, please leave jumper JP46 open.

All other jumpers related to the mode selection can be left open.

6.2 RESET Switch

The SW1 is used to issue a RESET to the device.

The SW1 toggle switch allows to activate the RESET in two different ways:

- SW1 in left '5-4(ON)' position: temporary reset
  Releasing the switch's lever returns the switch to its middle 'OFF' position and thus releases the reset.
- SW1 in right '5-6 ON' position: permanent reset
  For reset release the switch has to be moved back manually to its middle 'OFF' position.

The left and right switch position is defined from the side of the part number marking, which is highlighted with a red arrow in the figure below.

The lighted red LED13 indicates that SW1 is "on", i.e. in position '5-4 (ON)' or '5-6 ON'.

Note

LED13 does not light up when RESET is asserted by any other means than SW1.

Switch function	Viewed from part no. marking side		
			
NKK G19AP	ON	OFF	ON
Connecting terminals	5 – 4 momentary	None permanent	5 – 6 permanent

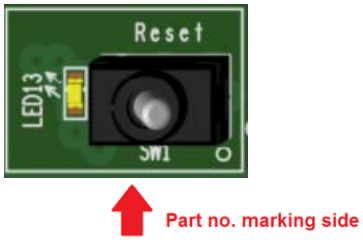


Figure 6.1 Operation of RESET switch

6.3 Signalling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins.

On the board version D018177_06_V01 the device pins P11_0 to P11_7 are connected to the odd pins of the pin header CN7.
On other board versions P11_0 to P11_3, P11_5 to P11_7 and P22_0 are connected to the odd pins of the pin header CN7.

The LEDs 2 to 9 are connected to the even CN7 pins.

Thus, the LEDs can be either connected to

- the device port pins P11_0 to P11_7 / P11_0 to P11_3, P11_5 to P11_7 and P22_0 by closing the connection on CN7 using a jumper, or
- any device pin by connecting the pin (from the connectors CN5, CN13, CN14, CN15 or CN16) directly with the even CN7 pins using a separate cable.

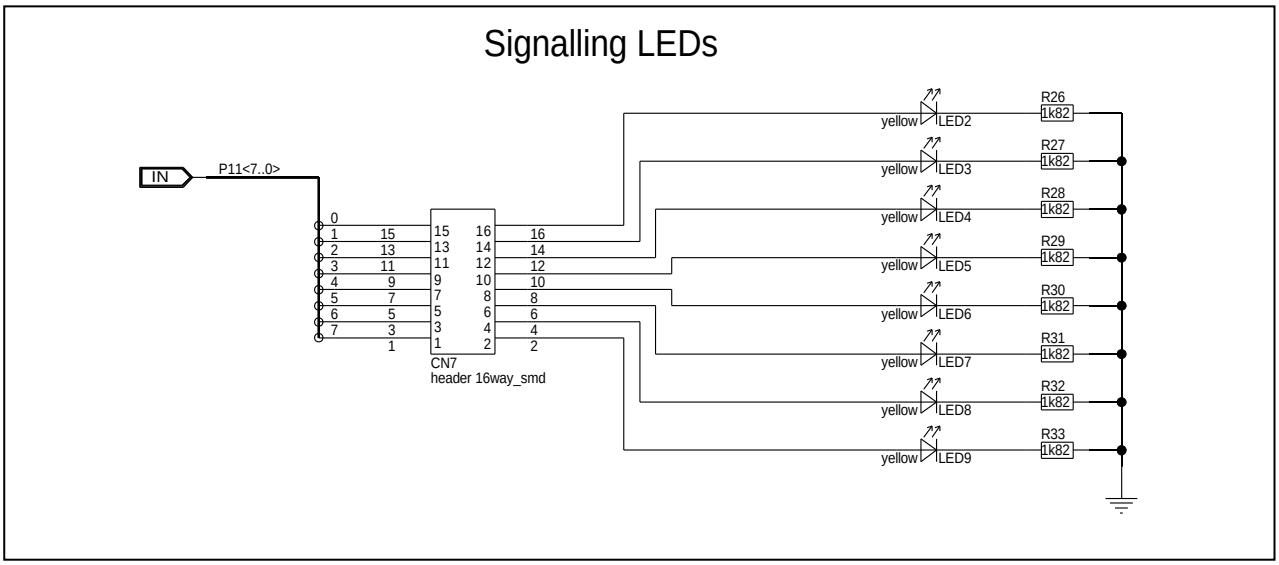


Figure 6.2 Circuit diagram for signalling LEDs on board version D018177_06_V01

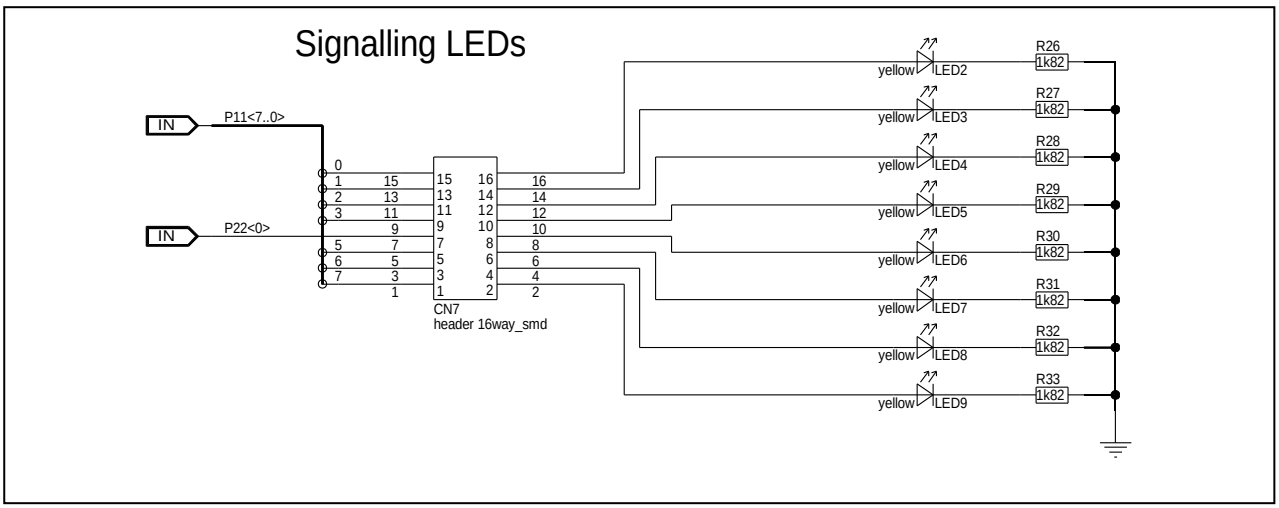


Figure 6.3 Circuit diagram for signaling LEDs on board versions other than D018177_06_V01

6.4 Pull-Up/Pull-Down Pin Header

The Pull-up/Pull-down pin header CN29 provides fixed voltage levels at its pins, that can be used to pull-up/pull-down a signal on the board or the device by connecting a CN29 pin to the signal via a separate cable.

All pull-up or pull-down resistors use 1kΩ resistors.

The CN29 pins have following pull-up or pull-down voltage levels:

- All odd numbered pins are connected to L level.
- Even numbered pins 2, 4, 6, 8 are connected to int_P3V3, which means 3.3 V. The source for the 3.3V supply is selected using jumper CN20:
    - CN20[1-2]: 3.3 V input from external power supply via connector CN21 or from a connected main board (jumper CN30[1-2] closed).
    - CN20[2-3]: 3.3 V comes from REG_P3V3 generated by the onboard voltage regulator.
- Even numbered pins 10, 12, 14, 16 are connected to P5V0, which means 5.0 V. P5V0 is either provided from external power supply via connector CN9 or from a connected main board (jumper CN12[1-2] closed).

Refer to *7.10 Pull-Up/Pull-Down Pin Header CN29* for CN29 details.

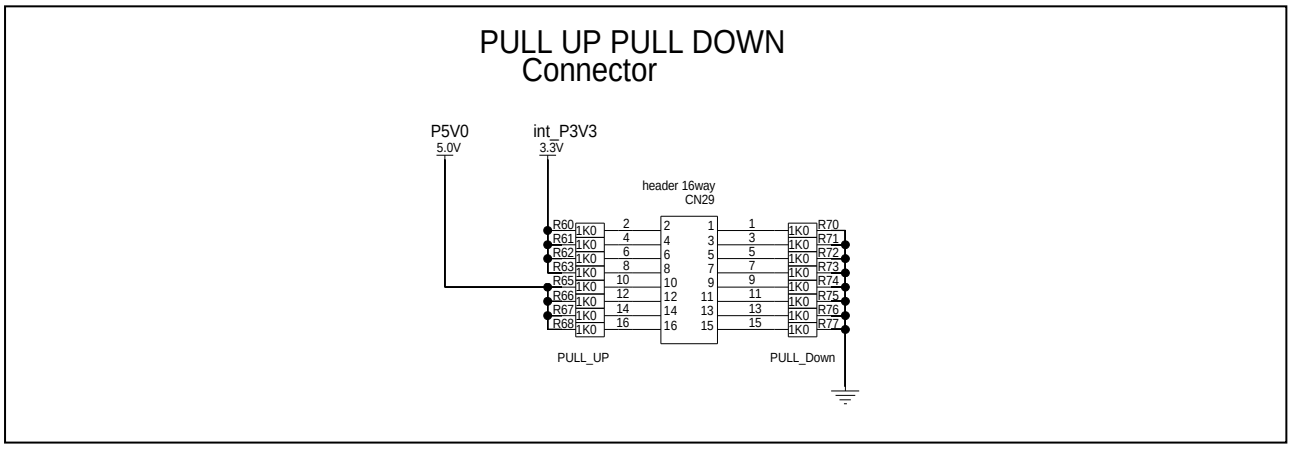


Figure 6.4 Circuit diagram for pull up / pull down signals

6.5 Renesas High-Speed Bus RHSB0

The piggyback board provides access to the high-speed bus interface RHSB0 on connector CN24.

On boards other than D018177_06_V01 connection of RHSB0 interface to CN24 has to be enabled using switch SW5-1.

The pin configuration on connector CN24 can be modified using the RHSB0_MUX signal from switch SW3-1.

Refer to *7.6 RHSB0 Connector CN24* for the possibility to configure the pin assignment on CN24.

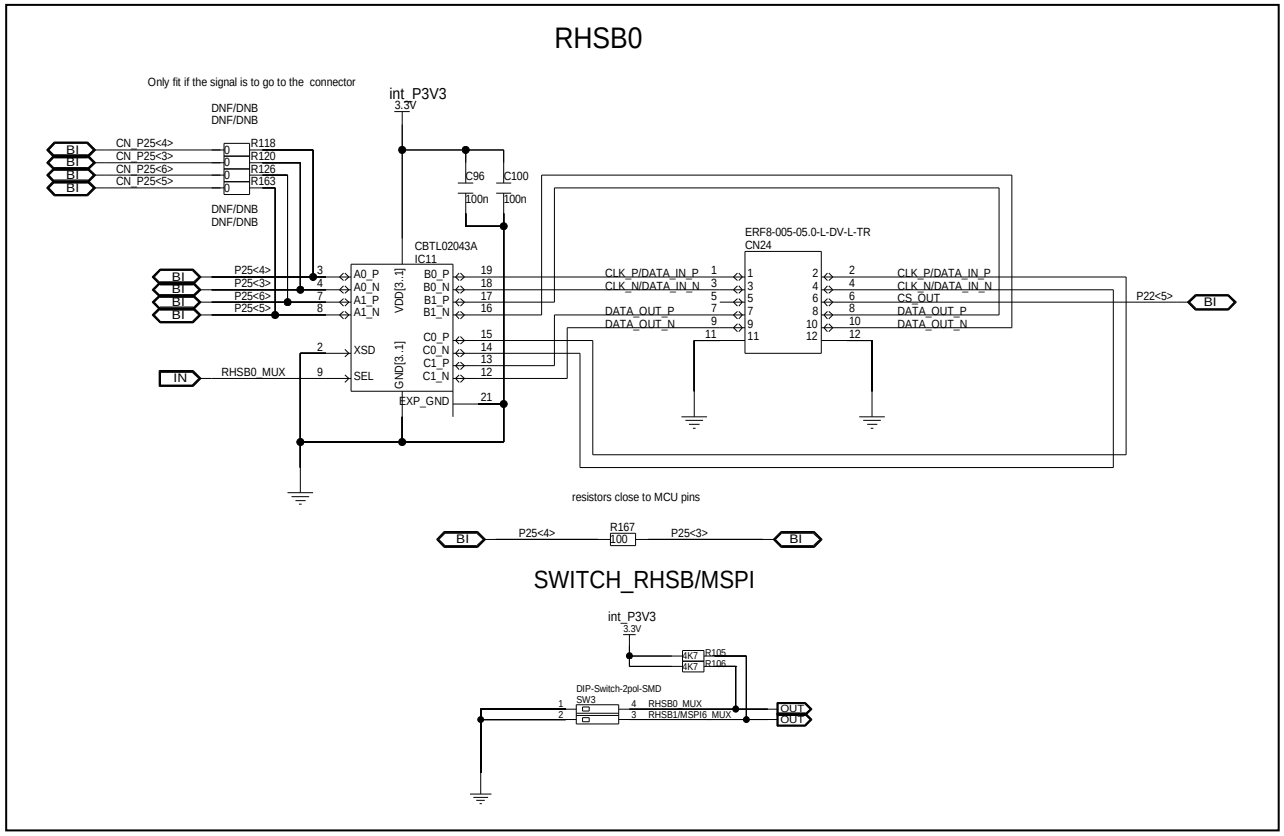


Figure 6.5 Circuit diagram for RHSB0 interface on board version D018177_06_V01

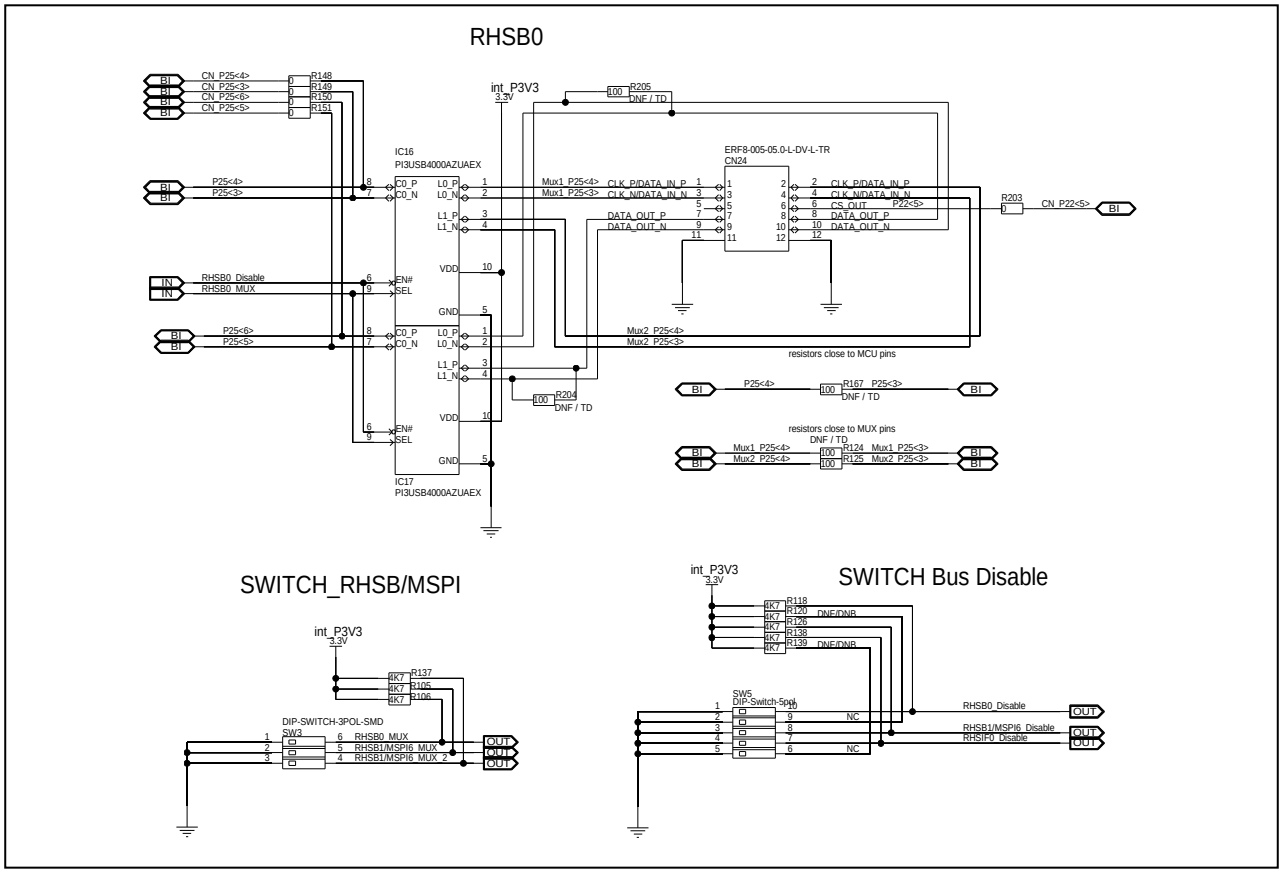


Figure 6.6 Circuit diagram for RHSB0 interface on board versions other than D018177_06_V01

CAUTION

The piggyback board can apply 100Ω termination resistors for different use cases.
See in this document the attachment 'Guideline for termination resistors.xlsx' for the detailed information.

Notes

1. To minimize signal interference on the RHSB0 interface the related port signals are not connected directly to the MainBoard connectors CN1-CN3, or device port connectors CN5, CN13-CN16.
   They are connected via 0 Ω resistors
   - R118, R120, R126, R163 on board version D018177_06_V01
   - R148-R151, R203 on other board versions other than D018177_06_V01
2. Swapping the Rx/Tx signals allows board-to-board communication e.g. with another piggyback board via separate cables.

6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6

The CN23 connector can be used to connect to the device's RHSB1 and MSPI6 interface.

On boards other than D018177_06_V01 connection of RHSB1/MSPI6 interface to CN23 has to be enabled using switch SW5-3.

The pin configuration on connector CN23 can be modified using

- the RHSB1/MSPI6_MUX signal from switch SW3-2.
- the RHSB1/MSPI6_MUX_2 signal from switch SW3-3 (on board versions other than D018177_06_V01).

Refer to *7.5 RHSB1/MSPI6 Connector CN23* for the CN23 pin assignment.

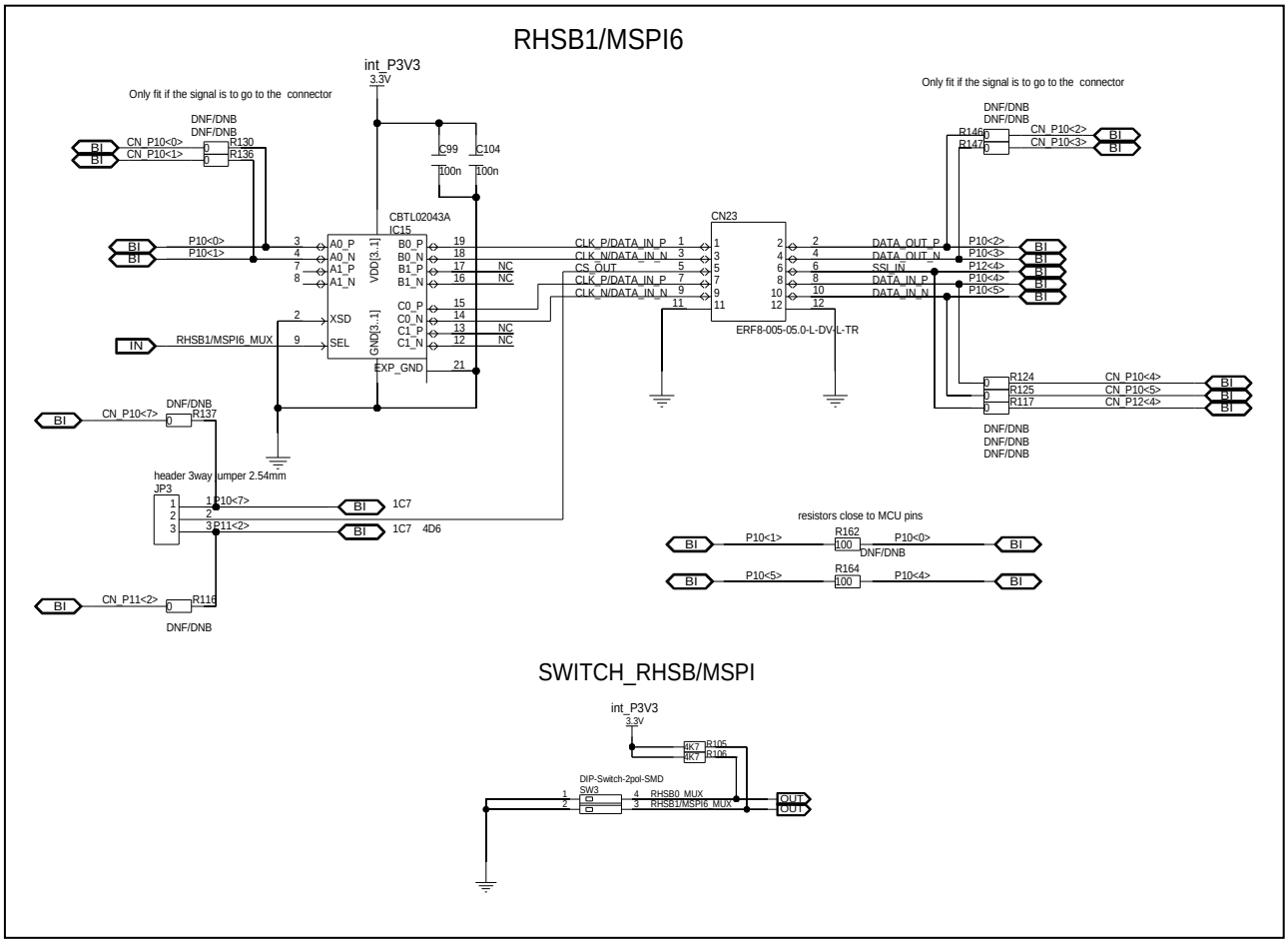


Figure 6.7 Circuit diagram for RHSB1/MSPI6 interface on board version D018177_06_V01

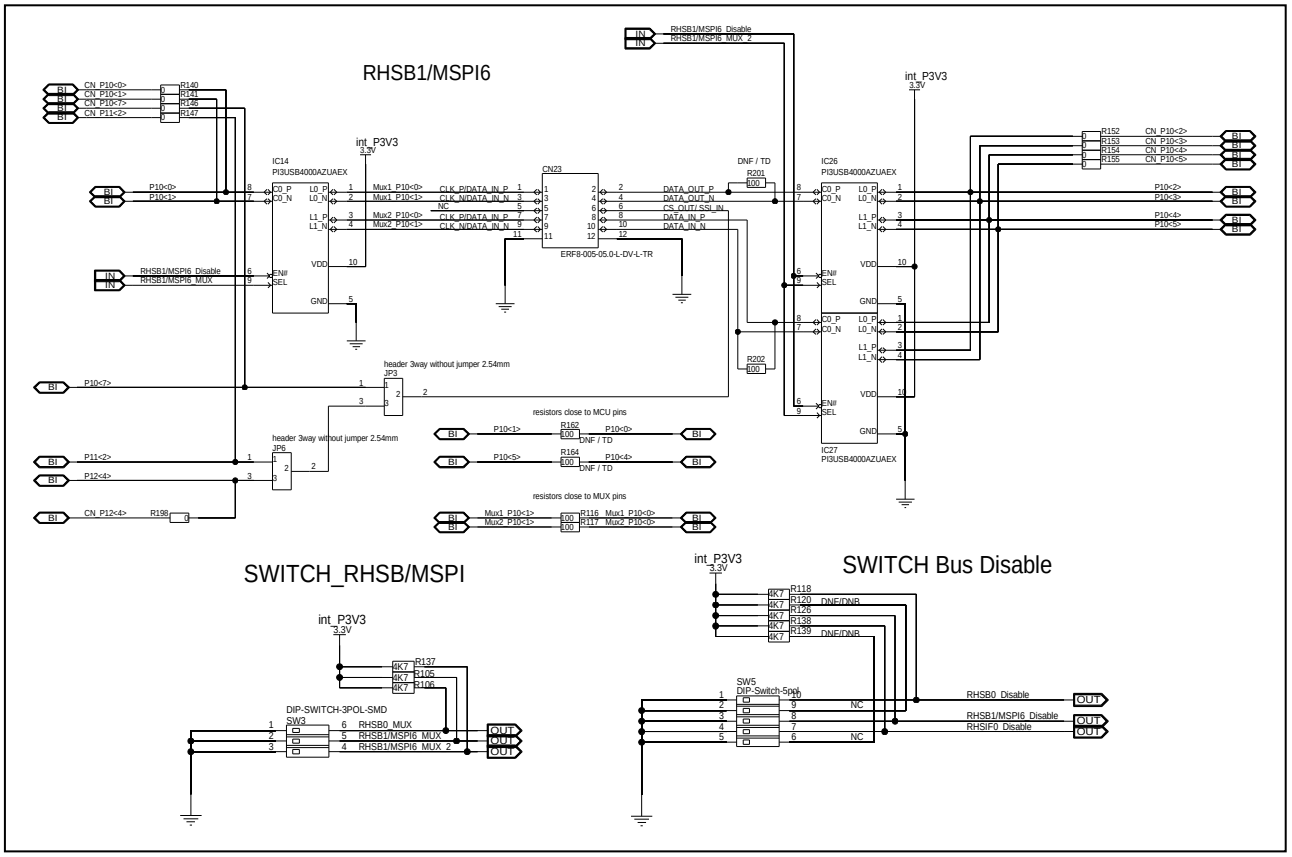


Figure 6.8 Circuit diagram for RHSB1/MSPI6 interface on board versions other than D018177_06_V01

CAUTION

The piggyback board can apply 100Ω termination resistors for different use cases.
See in this document the attachment 'Guideline for termination resistors.xlsx' for the detailed information.

Notes

1. To minimize signal interference on the RHSB1/MSPI6 interface the related port signals are not connected directly to the MainBoard connectors CN1-CN3, or device port connectors CN5, CN13-CN16. They are connected via 0 Ω resistors
   - R116, R117, R124, R125, R130, R136, R137, R146, R147 (on board version D018177_06_V01)
   - R140-R141, R146-R147, R152-R155, R198 (on board versions other than D018177_06_V01)
2. Swapping the Rx/Tx signals allows board-to-board communication e.g., with another piggyback board via separate cables.

6.7 Renesas Multichannel Serial Peripheral Interface MSPI9

Connector CN26 provides access to the MSPI9 interface.

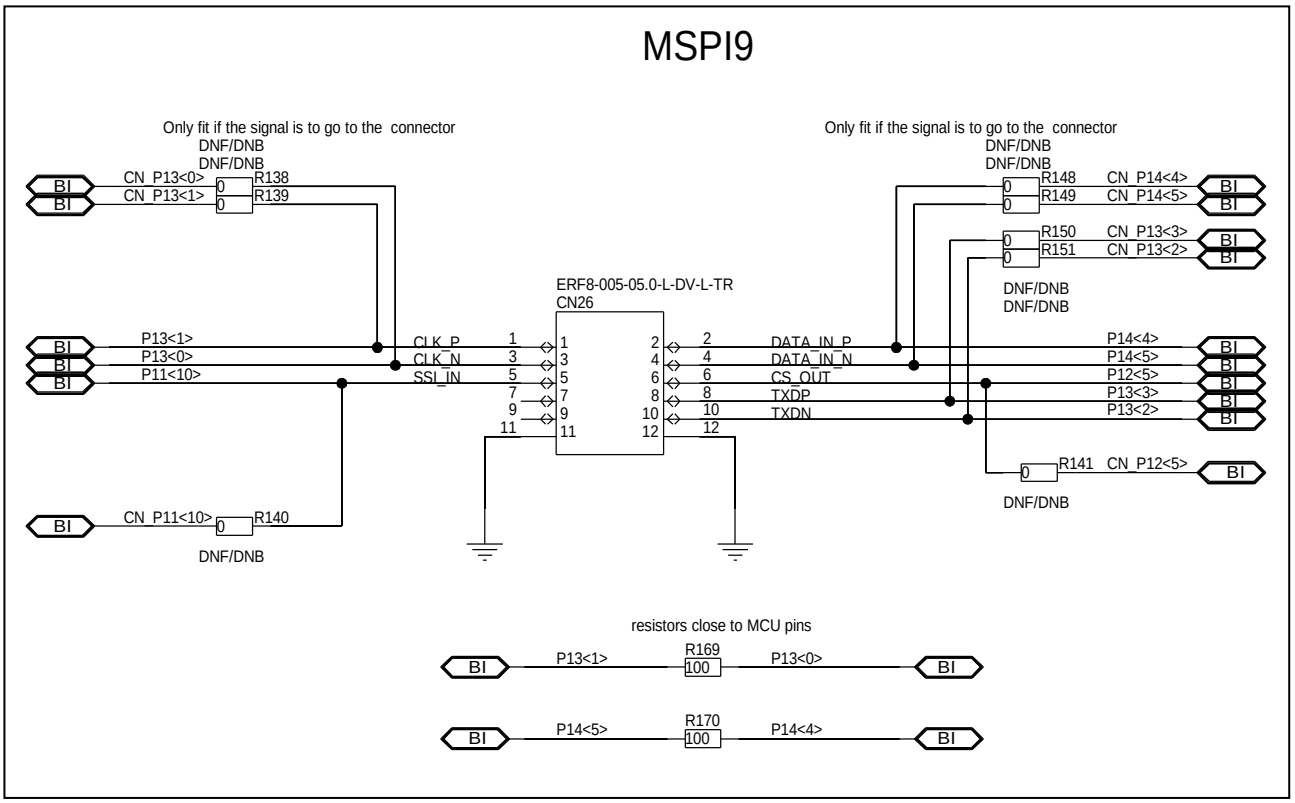


Figure 6.9 Circuit diagram for MSPI9 interface on board version D018177_06_V01

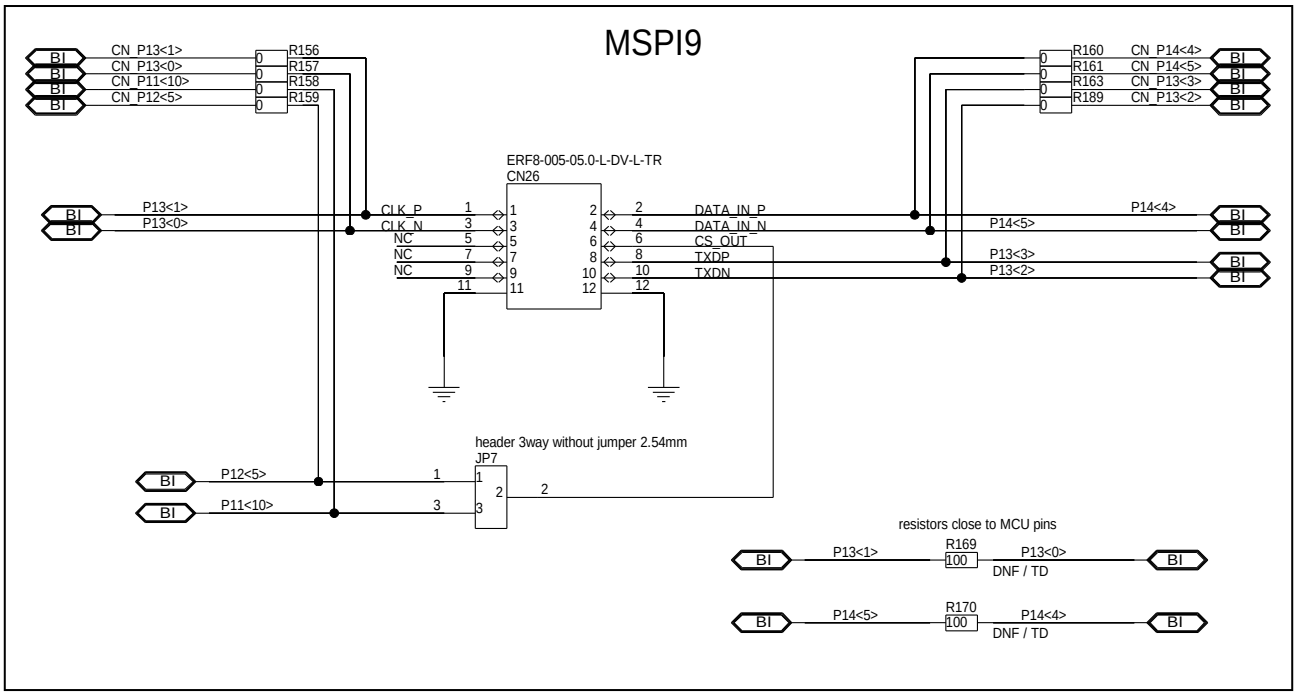


Figure 6.10 Circuit diagram for MSPI9 interface on board versions other than D018177_06_V01

Refer to *7.7 MSPI9 Connector CN26* for the CN26 pin assignment.

Notes

To minimize signal interference on the MSPI9 interface the related port signals are not connected directly to the MainBoard connectors CN1-CN3, or device port connectors CN5, CN13-CN16.
They are connected via 0 Ω resistors

- R138 to R141, R148 to R151 (on board version D018177_06_V01)
- R156 to R161, R163, R189 (on board versions other than D018177_06_V01)

6.8 Renesas High-Speed Serial I/F RHSIF0

Connector CN27 provides access to the RHSIF0 interface.

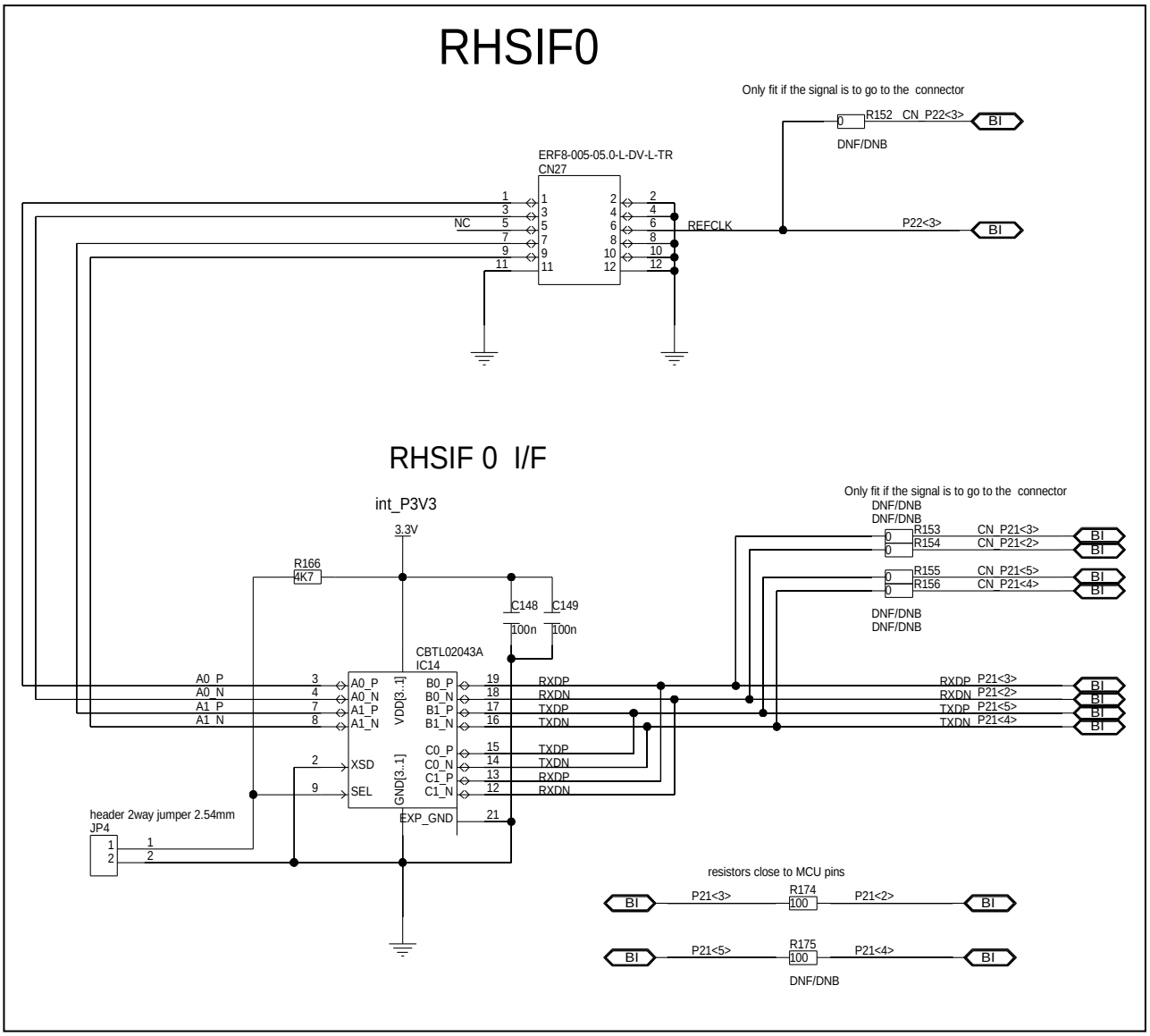


Figure 6.11 Circuit diagram for RHSIF0 interface on board version D018177_06_V01

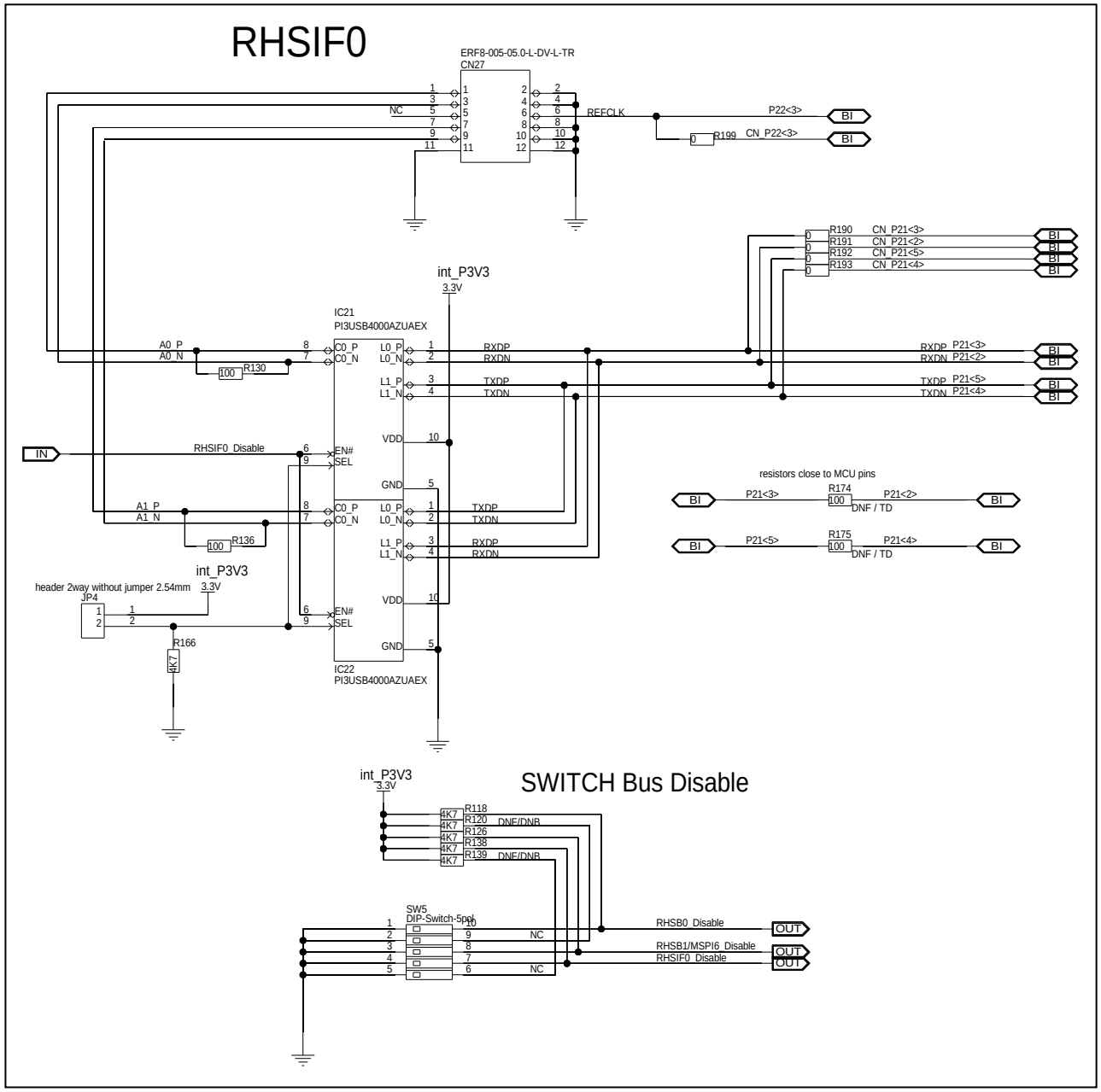


Figure 6.12 Circuit diagram for RHSIF0 interface on board versions other than D018177_06_V01

On boards other than D018177_06_V01 connection of RHSIF0 interface to CN27 has to be enabled using switch SW5-4.

Rx and Tx signals available at CN27 can be swapped by setting the jumper JP4:

- JP4[1-2] = ON:
  - RXDP/RXDN at CN27 pins 1 and 3
  - TXDP/TXDN at CN27 pins 7 and 9
- JP4[1-2] = OFF:
  - RXDP/RXDN at CN27 pins 7 and 9
  - TXDP/TXDN at CN27 pins 1 and 3

Refer to *7.8 RHSIF0 Connector CN27* for the CN27 pin assignment.

Notes

1. To minimize signal interference on the RHSIF0 interface the related port signals are not connected to connectors CN2, CN3 and CN14. They are connected via 0 Ω resistors
   - R152 to R156 (on board version D018177_06_V01)
   - R190-R193, R199 (on board versions other than D018177_06_V01).
2. Swapping the Rx/Tx signals allows board-to-board communication e.g., with another piggyback board via separate cables.

6.9 Renesas High-Speed Serial I/F RHSIF1

Connector CN28 provides access to the RHSIF1 interface.

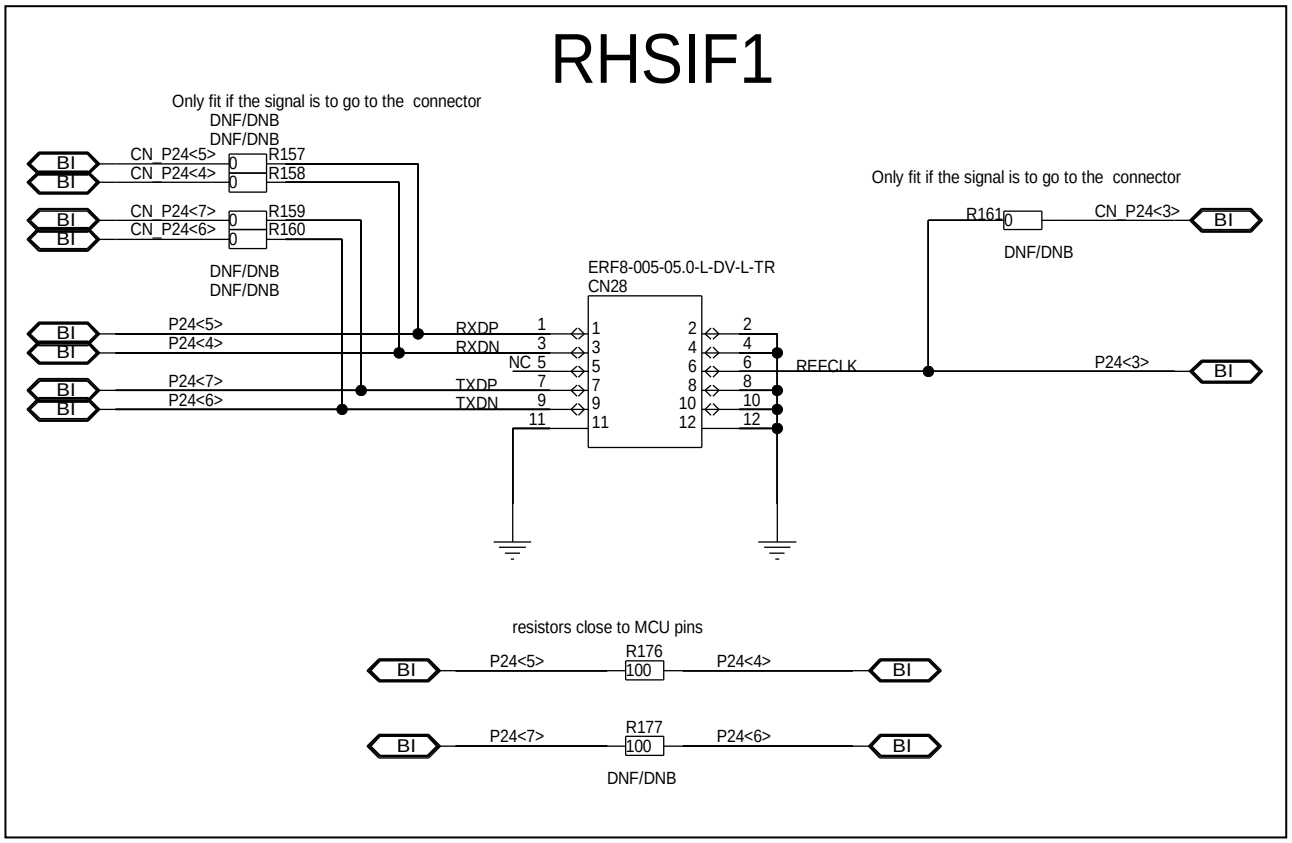


Figure 6.13 Circuit diagram for RHSIF1 interface on board version D018177_06_V01

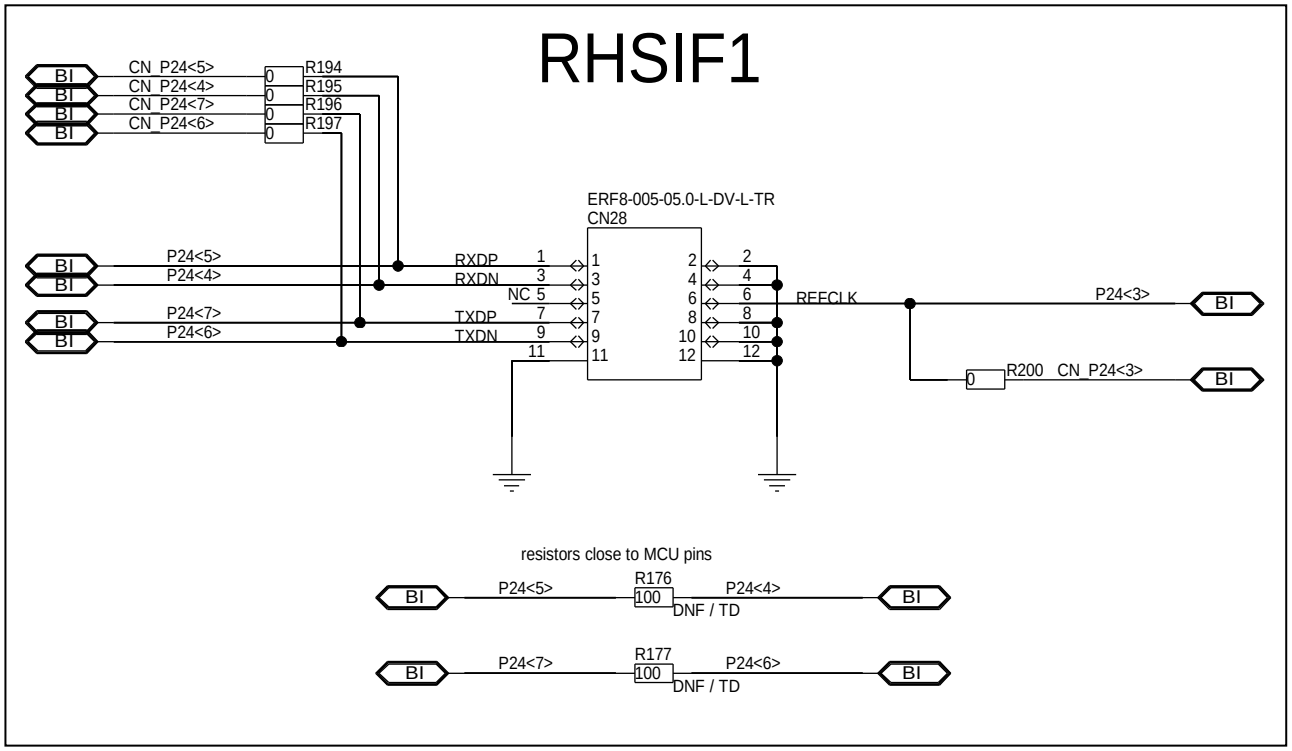


Figure 6.14 Circuit diagram for RHSIF1 interface on board versions other than D018177_06_V01

See chapter *7.9 RHSIF1 Connector CN28* for the CN28 pin assignment.

Notes

To minimize signal interference on the RHSIF1 the related port signals are not connected directly to the MainBoard connectors CN1-CN3, or device port connectors CN5, CN13-CN16. They are connected via 0 Ω resistors

- R157-R161 (on board version D018177_06_V01)
- R194-R197, R200 (on board versions other than D018177_06_V01.

6.10 Automotive Ethernet Interfaces ETN0 and ETN1

Depending on the device being used the piggyback board offers up to 2 Ethernet interfaces.

Device	Ethernet Interfaces RMII (max 100Mbps) / SGMII (max 1Gbps)
RH850/U2B10	1 (ETND0) / -
RH850/U2B20	1 (ETND0) / 1 (ETND1)
RH850/U2B24	- / 2 (ETNE0 ch0, ETNE0 ch1)

The piggyback board features two Marvell 88Q2112 Automotive Ethernet PHY (IC7 and IC12) for using the device's SGMII interface ETN0 and ETN1 via the TE MATEnet connector on CN18 (ETN0) / CN17 (ETN1) or straight wires on block connector CN22 (ETN0) / CN19 (ETN1).

The Ethernet channels can be enabled using switch SW2.

- SW2-1 enables Ethernet channel ETN0.
- SW2-2 enables Ethernet channel ETN1.

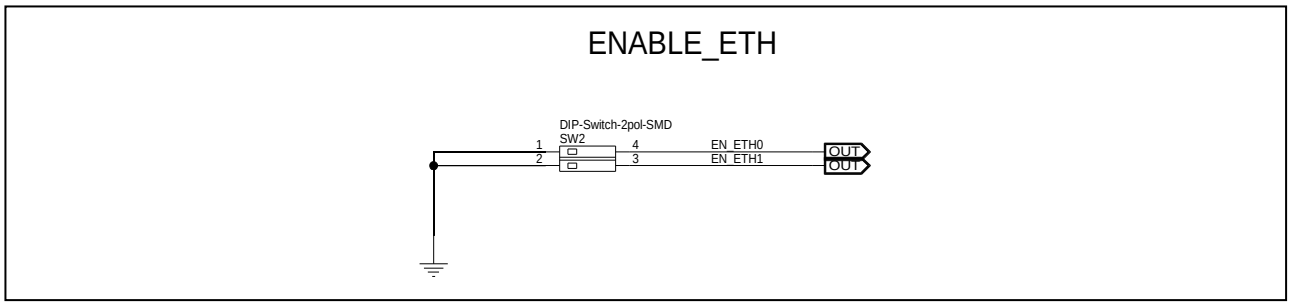


Figure 6.15 Switches to enable Ethernet channels

Below picture shows the circuit diagrams of both Ethernet channels.

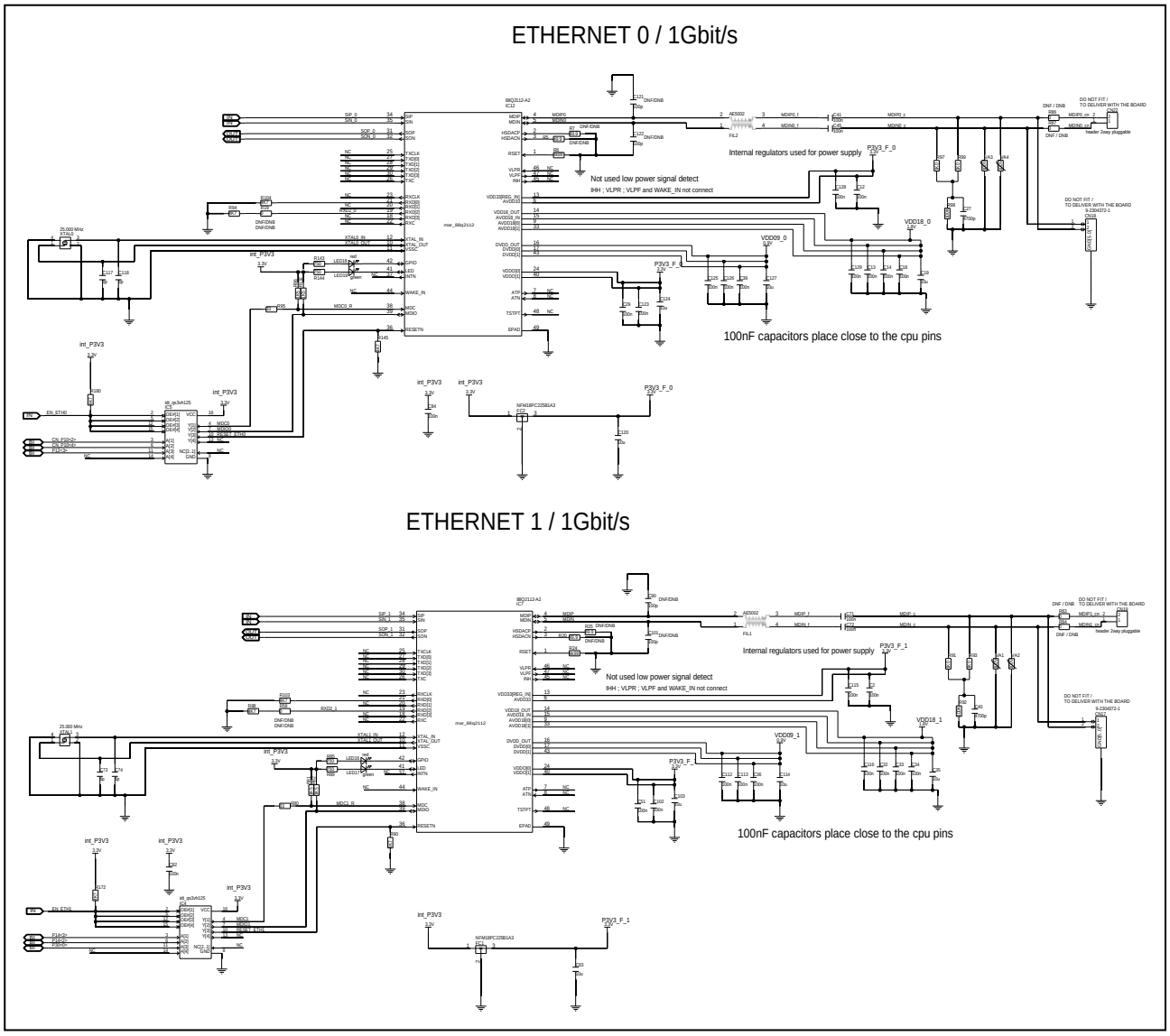


Figure 6.16 Ethernet circuits for ETN0 and ETN1 on board version D018177_06_V01

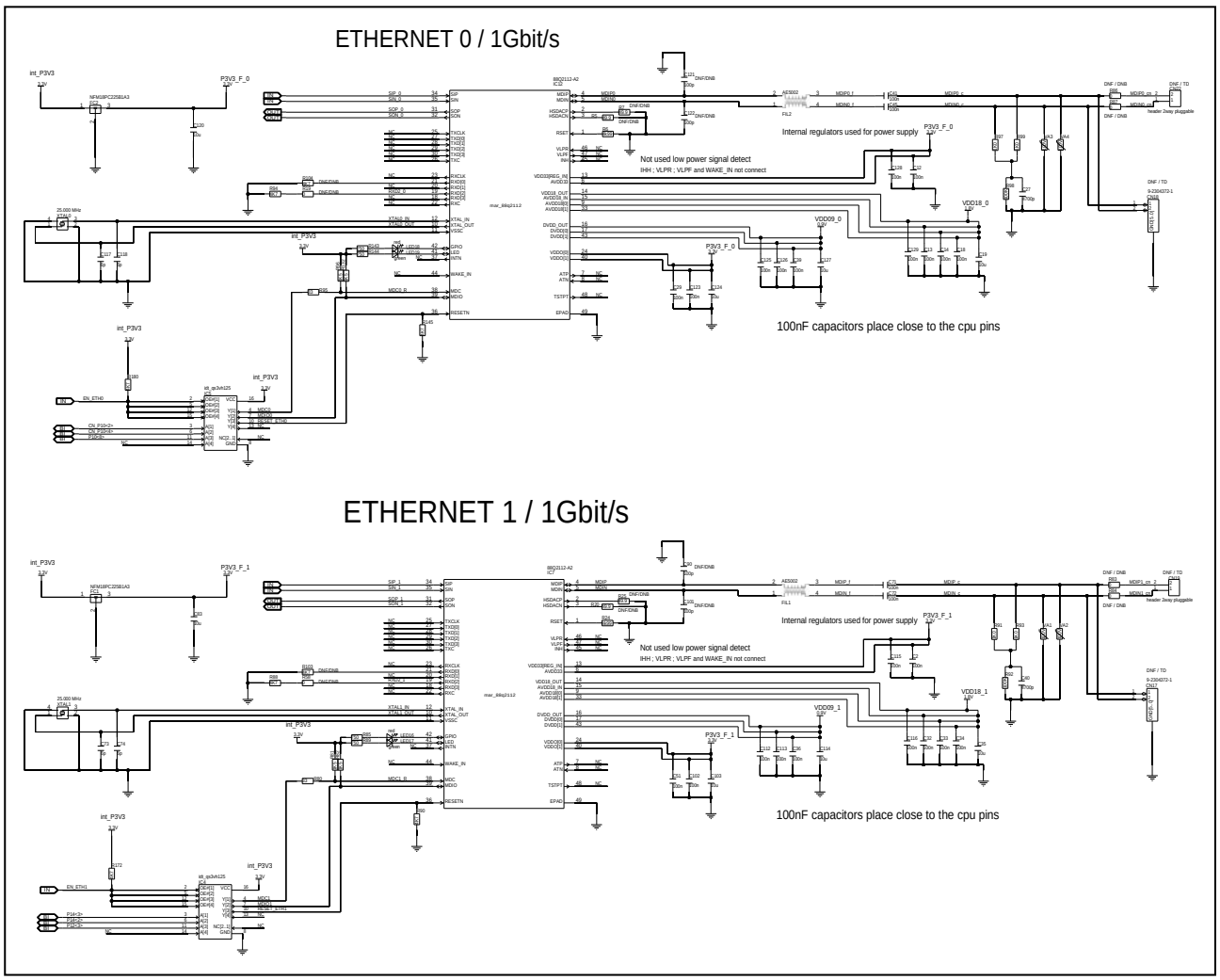


Figure 6.17 Ethernet circuits for ETN0 and ETN1 on board versions other than D018177_06_V01

If the TE MATEnet connector should be used, connector CN17 and/or connector CN18 must be assembled with the connector(s) included in the delivery.

Please refer to *Figure 6.18 Ethernet connectors CN17 and CN18* for the placement of the connector(s).

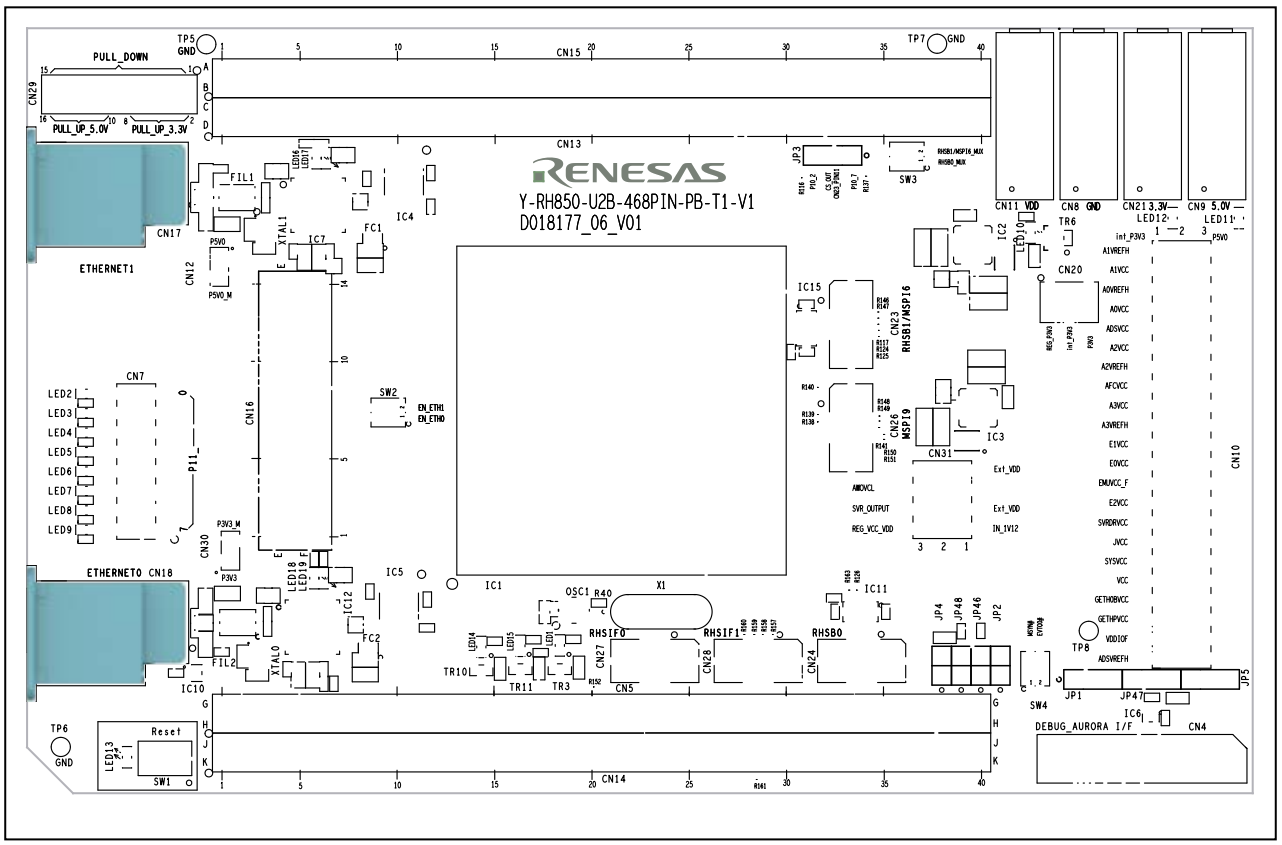


Figure 6.18 Ethernet connectors CN17 and CN18

If a 2-wire connection should be used the connectors CN19 and/or CN22 must be assembled with the Würth block connector(s) included in the delivery.

To use CN19 it is necessary to populate the resistors R83 and R84 with 0 Ω resistors.

To use CN22 it is necessary to populate the resistors R86 and R87 with 0 Ω resistors.

Please refer to *Figure 6.19 Ethernet connector CN19 and CN22* for the placement of the connector(s).

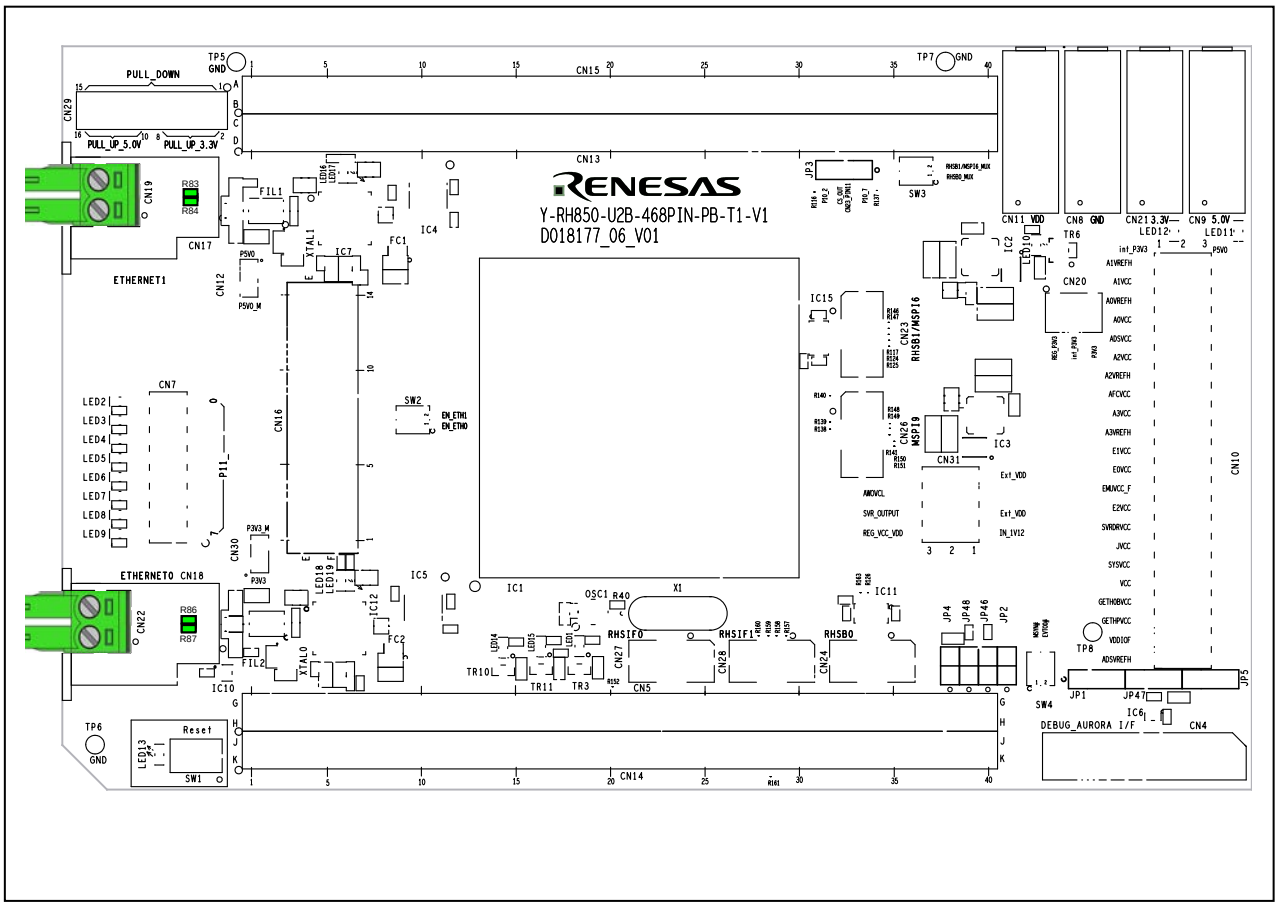


Figure 6.19 Ethernet connector CN19 and CN22

Notes

1. For ETNx initial setup please refer to the device UM.
   For ETNx operation the ETNxSGCLKSEL register must be set to ETNxSGCLKSEL=0x01 to select the Internal MOSC clock of 20MHz.
   For an internal MOSC clock of 20MHz the crystal X1 has to be the 20MHz crystal installed by default.
   For package content please refer to *Table 1.1 Package Components for the Y-RH850-U2B-468PIN-PB-T1-V1*
2. The signals of the device's Fast Ethernet (R)MII interface (ETN0 and ETN1) are available on the main board connectors. Thus, ETNx can control an Ethernet PHY on the main board.

3. Alternatively, ETNx can also be used to operate the main board's 100 Mbps Ethernet PHY. In this case the ETNx Fast Ethernet mode is selected by Option Bytes settings and the pin multiplexing needs to be configured accordingly.
   ETN0 uses the port P10_2 (MDC0), P10_4 (MDIO0) and P12_3[1)] / P10_8[2)] (RESET_ETH0) to control the Ethernet PHY IC12.
   ETN0 uses the port P10_2 (ETH0MDC), P10_4 (ETH0MDIO) and P12_3 (ETH0RESET) to control the Ethernet PHY on the main board.
   ETN1 uses the port P14_3 (MDC1), P14_2 (MDIO1) and P30_0[1)]/P12_3[2)] (RESET_ETH1) to control the Ethernet PHY IC7.
   ETN1 uses the port P14_3 (ETH1MDC), P14_2 (ETH1MDIO) and P30_0 (ETH1RESET) to control the Ethernet PHY on the main board.

   [1)] Board version D018177_06_V01
   [2)] Board version other than D018177_06_V01

Refer to *7.4 Ethernet Connector CN17, CN18, CN19 and CN22* for the CN17, CN18, CN19 and CN22 pin assignment.

6.11 Low Pass Filter

The piggyback board includes a set of low pass filters to filter input signals to analog input ports.

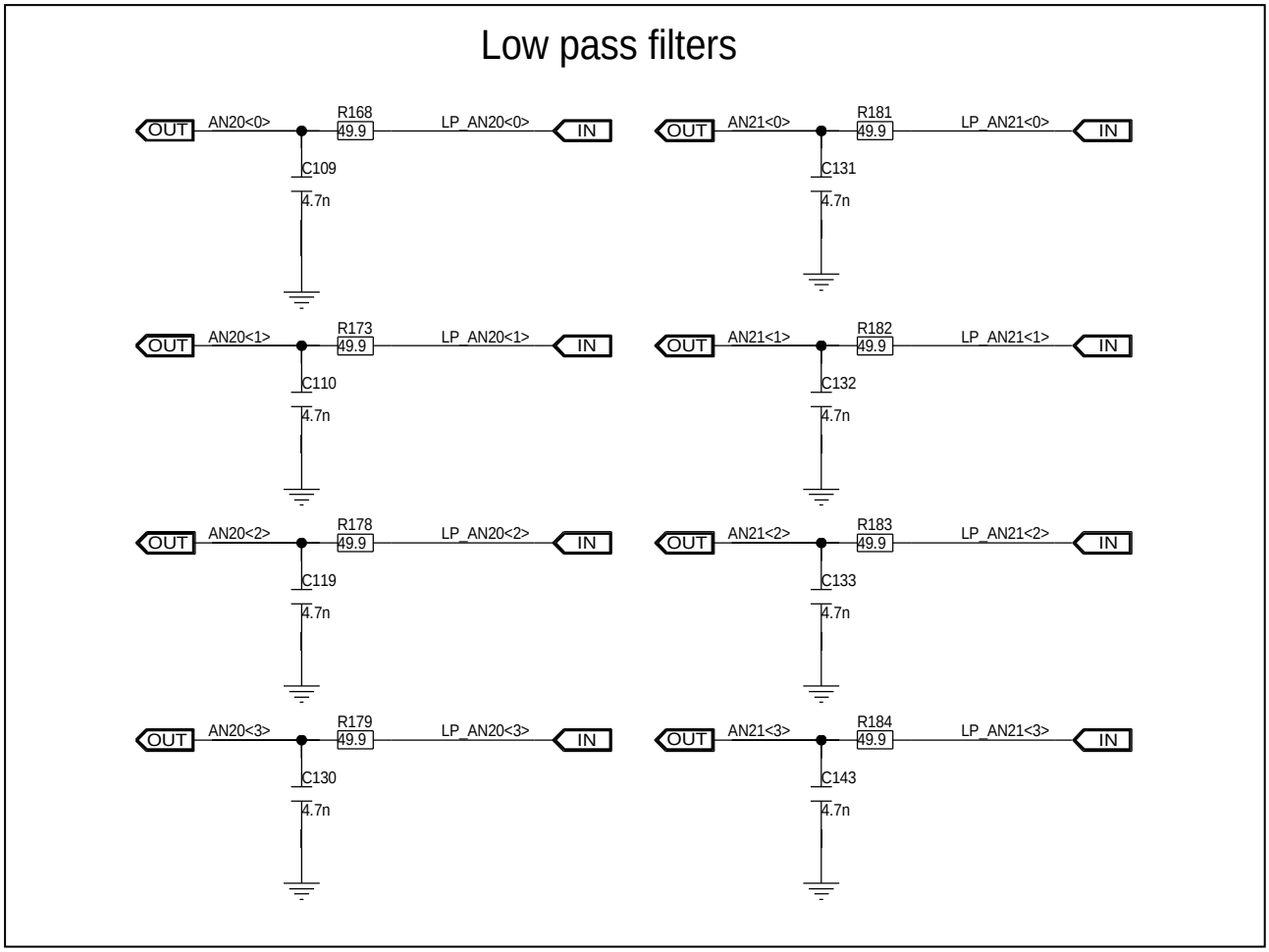


Figure 6.20 Circuit diagram for low pass filters

The analog input ports on RH850/U2B can be accessed through the device port connectors CN13 and CN15. Inputs including the low pass filter can be identify by the leading "LP_" in the pin name.

Please refer to *7.3.2 Device Ports Connector CN13* and *7.3.4 Device Ports Connector CN15* for details on the pin assignments.

7. Connectors

7.1 Connectors to the Main Board CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the piggyback board to a main board.

The signals of each connector are summarized in the following tables.

Note

Regarding the function on the main board, please refer to the User's Manual of any supported main board.
Refer to *1.2 Supported Main Boards* for a list of supported main boards.

7.1.1 Main Board Connector CN1

Table 7.1 Main board connector CN1

Pin	Main board function	Piggyback board device port	Pin	Main board function	Piggyback board device port
1	VDDA	–	2	VDDA	–
3	VDDA	–	4	VDDA	–
5	RESET	RESET#	6	NMI	P25_2
7	WAKE	–	8	–	–
9	INT0	P23_2	10	INT1	P23_3
11	INT2	P23_4	12	INT3	P23_5
13	–	–	14	–	–
15	UART0TX	P12_6	16	UART1TX	P33_1
17	UART0RX	CN_P12_5 *	18	UART1RX	P33_0
19	LIN0TX	P34_0	20	LIN1TX	P20_7
21	LIN0RX	P34_2	22	LIN1RX	P20_6
23	IIC0SCL	CN_P10_7 *	24	IIC1SCL	P00_6
25	IIC0SDA	P10_8	26	IIC1SDA	P00_7
27	CAN0TX	CN_P21_4 *	28	CAN1TX	P02_7
29	CAN0RX	CN_P21_5 *	30	CAN1RX	P02_10
31	SENT0RX	P00_0	32	SENT1RX	P00_4
33	SENT0SPCO	P00_1	34	SENT1SPCO	P00_5
35	PSI5SRX0	P02_10	36	PSI5RX0	P02_0
37	PSI5STX0	P02_8	38	PSI5TX0	P02_1
39	PSI5SCLK0	P02_6	40	–	–
41	FLX0TX	P12_1	42	FLX0EN	P12_0

Table 7.1 Main board connector CN1 (cont'd)

Pin	Main board function	Piggyback board device port
43	FLX0RX	P12_7
45	FLX1TX	P22_11
47	FLX1RX	P12_8
49	–	–
51	ETH0MDIO	CN_P10_4 *
53	ETH0RXD0	P11_3
55	ETH0RXD1	CN_P11_2 *
57	ETH0RXD2	CN_P10_3 *
59	ETH0RXD3	CN_P10_0 *
61	ETH0RXCLK	CN_P10_1 *
63	ETH0RXER	P11_6
65	ETH0CRSDV	–
67	ETH0RXDV	P11_7
69	ETH0RESET	P12_3 [1) 2)] P10_8 [3)]
71	–	–
73	USB0UDMF	–
75	USB0UDPF	–
77	–	–
79	–	–
81	–	–
83	–	–
85	DIGIO_0	P11_0
87	DIGIO_2	CN_P11_2 *
89	DIGIO_4	P11_4 [1)] P22_0 [2) 3)]
91	DIGIO_6	P11_6
93	DIGIO_8	P11_8
95	DIGIO_10	CN_P10_0 *
97	DIGIO_12	CN_P10_2 *
99	DIGIO_14	CN_P10_4 *
101	–	–

Pin	Main board function	Piggyback board device port
44	FLXSTPWT	CN_P12_4 *
46	FLX1EN	P12_9
48	FLXCLK	–
50	–	–
52	ETH0MDC	CN_P10_2 *
54	ETH0TXD0	P11_8
56	ETH0TXD1	P11_9
58	ETH0TXD2	P11_5
60	ETH0TXD3	P11_1
62	ETH0TXCLK	P11_4
64	ETH0TXER	CN_P11_10 *
66	ETH0TXEN	P11_0
68	ETH0COL	–
70	ETH0LINK	CN_P10_7 *
72	–	–
74	USB0UDMH	–
76	USB0UDPH	–
78	–	–
80	–	–
82	–	–
84	–	–
86	DIGIO_1	P11_1
88	DIGIO_3	P11_3
90	DIGIO_5	P11_5
92	DIGIO_7	P11_7
94	DIGIO_9	P11_9
96	DIGIO_11	CN_P10_1 *
98	DIGIO_13	CN_P10_3 *
100	DIGIO_15	CN_P10_5 *
102	–	–

Table 7.1 Main board connector CN1 (cont'd)

Pin	Main board function	Piggyback board device port
103	MUX0	P34_0
105	MUX2	P34_1
107	ADC0	AN02_0
109	ADC2	AN02_2
111	ADC4	AN03_0
113	ADC6	AN03_2
115	VDDIOF	–
117	VDDB	–
119	VDDB	–
121	GND	–
123	GND	–
125	GND	–
127	GND	–

Pin	Main board function	Piggyback board device port
104	MUX1	P34_2
106	–	–
108	ADC1	AN02_1
110	ADC3	AN02_3
112	ADC5	AN03_1
114	ADC7	AN03_3
116	VDDIOF	–
118	VDDB	–
120	VDDB	–
122	GND	–
124	GND	–
126	GND	–
128	GND	–

Note * By default these signals are not connected to CN1 to minimize signal interference. If required, they can be connected via 0 Ω resistors. Check with the schematic for the related resistor of a signal.

[1)] For board version D018177_06_V01
[2)] For board version D018177_06_V02
[3)] For board version D018177_06_V03

7.1.2 Main Board Connector CN2

Table 7.2 Main board connector CN2

Pin	Main board function	Piggyback board device port
1	CAN2TX	P02_1
3	CAN2RX	P02_4
5	CAN4TX	CN_P10_5 *
7	CAN4RX	P10_6
9	LIN2TX	P22_2
11	LIN2RX	CN_P22_3 *
13	LIN4TX	P12_6
15	LIN4RX	CN_P12_5 *
17	LIN6TX	P00_11
19	LIN6RX	P00_10

Pin	Main board function	Piggyback board device port
2	CAN3TX	P02_2
4	CAN3RX	P02_3
6	CAN5TX	P14_2
8	CAN5RX	P14_0
10	LIN3TX	P32_6
12	LIN3RX	P32_4
14	LIN5TX	P33_1
16	LIN5RX	P33_0
18	LIN7TX	P01_7
20	LIN7RX	P01_5

Table 7.2 Main board connector CN2 (cont'd)

Pin	Main board function	Piggyback board device port
21	LIN8TX	P22_11
23	LIN8RX	P22_12
25	LIN10TX	P10_14
27	LIN10RX	P10_13
29	LIN12TX	P32_3
31	LIN12RX	P32_2
33	LIN14TX	P33_13
35	LIN14RX	P33_11
37	–	–
39	–	–
41	–	–
43	–	–
45	–	–
47	CAN6TX	P02_6
49	CAN6RX	P02_5
51	CAN8TX	P31_14
53	CAN8RX	P31_15
55	–	–
57	–	–
59	–	–
61	LIN16TX	P02_8
63	LIN16RX	P02_9
65	LIN18TX	P14_6
67	LIN18RX	CN_P14_5 *
69	LIN20TX	P00_3
71	LIN20RX	P00_2
73	LIN22TX	CN_P10_0 *
75	LIN22RX	CN_P10_1 *
77	–	–
79	SFMA0CLK	P20_4
81	SFMA0IO0	P20_0

Pin	Main board function	Piggyback board device port
22	LIN9TX	P10_12
24	LIN9RX	P10_11
26	LIN11TX	P23_6
28	LIN11RX	P23_5
30	LIN13TX	P33_5
32	LIN13RX	P33_2
34	LIN15TX	P20_3
36	LIN15RX	P20_2
38	–	–
40	–	–
42	–	–
44	–	–
46	–	–
48	CAN7TX	P20_5
50	CAN7RX	P20_4
52	CAN9TX	P31_10
54	CAN9RX	P31_11
56	–	–
58	–	–
60	–	–
62	LIN17TX	P34_3
64	LIN17RX	P34_4
66	LIN19TX	P14_8
68	LIN19RX	P14_7
70	LIN21TX	P00_8
72	LIN21RX	P00_9
74	LIN23TX	P32_1
76	LIN23RX	P32_0
78	–	–
80	SFMA0SSL	P20_5
82	SFMA0IO1	P20_1

Table 7.2 Main board connector CN2 (cont'd)

Pin	Main board function	Piggyback board device port
83	SFMA0IO2	P20_2
85	–	–
87	MMCA0CLK	CN_P13_0 *
89	MMCA0DAT0	CN_P13_1 *
91	MMCA0DAT2	CN_P13_3 *
93	MMCA0DAT4	P14_0
95	MMCA0DAT6	P14_3
97	–	–
99	ETH1MDIO	P14_2
101	ETH1RXD0	P13_8
103	ETH1RXD1	P13_9
105	ETH1RXD2	P13_10
107	ETH1RXD3	P13_11
109	ETH1RXCLK	P13_13
111	ETH1RXER	P13_14
113	ETH1CRSDV	–
115	ETH1RXDV	P13_12
117	ETH1RESET	P30_0 [1) 2)] P12_3 [3)]
119	–	–
121	GND	–
123	GND	–
125	GND	–
127	GND	–

Pin	Main board function	Piggyback board device port
84	SFMA0IO3	P20_3
86	–	–
88	MMCA0CMD	CN_P14_5 *
90	MMCA0DAT1	CN_P13_2 *
92	MMCA0DAT3	P14_1
94	MMCA0DAT5	P14_2
96	MMCA0DAT7	CN_P14_4 *
98	–	–
100	ETH1MDC	P14_3
102	ETH1TXD0	P14_12
104	ETH1TXD1	P14_10
106	ETH1TXD2	P14_7
108	ETH1TXD3	P14_9
110	ETH1TXCLK	P14_11
112	ETH1TXER	P14_8
114	ETH1TXEN	P14_6
116	ETH1COL	–
118	ETH1LINK	CN_P14_4 *
120	–	–
122	GND	–
124	GND	–
126	GND	–
128	GND	–

Note * By default these signals are not connected to CN2 to minimize signal interference. If required, they can be connected via 0 Ω resistors. Check with the schematic for the related resistor of a signal.

1) For board version D018177_06_V01
2) For board version D018177_06_V02
3) For board version D018177_06_V03

7.1.3 Main Board Connector CN3

Table 7.3 Main board connector CN3

Pin	Main board function	Piggyback board device port
1	CSI0CS0	P23_2
3	CSI0CS1	P23_4
5	CSI0CS2	P23_3
7	CSI0CS3	P23_0
9	–	–
11	–	–
13	PSI5SRX1	P33_2
15	PSI5STX1	P33_0
17	PSI5SCLK1	P33_1
19	–	–
21	CSI1CS2	P33_7
23	–	–
25	–	–
27	–	–
29	CSI1SCLK	P33_6
31	–	–
33	MOT0ADU (RFU)	AN00_0
35	MOT0ADV (RFU)	AN00_1
37	MOT0ADW (RFU)	AN00_2
39	MOT0RDCS1 (RFU)	AN24_3
41	MOT0RDCS3 (RFU)	AN24_2
43	MOT0RDCS2 (RFU)	AN24_0
45	MOT0RDCS4 (RFU)	AN24_1
47	MOT0RDCCOM (RFU)	AN25_1
49	MOT0RDCRSO (RFU)	AN25_0
51	–	–
53	–	–
55	AD1_0	AN11_0
57	AD1_2	AN11_2

Pin	Main board function	Piggyback board device port
2	CSI0CLK	P23_7
4	CSI0SI (MSPI3)	P23_6
6	CSI0SO	P23_5
8	–	–
10	CSI1CS1	P33_4
12	–	–
14	PSI5RX1	P02_9
16	PSI5TX1	P02_7
18	–	–
20	–	–
22	CSI1CS3	P33_8
24	CSI1CS0	P22_5 [1)] CN_P22_5 [2) 3)]
26	DIGIO_24	P22_6
28	CSI1SO	CN_P22_3 *
30	CSI1SI	P33_3
32	–	–
34	AD0 (RFU)	AN10_0
36	AD1 (RFU)	AN10_1
38	AD2 (RFU)	AN10_2
40	RDCS1 (RFU)	AN27_2
42	RDCS3 (RFU)	AN27_1
44	RDCS2 (RFU)	AN26_0
46	RDCS4 (RFU)	AN26_2
48	RDCCOM (RFU)	AN27_3
50	RDCRSO (RFU)	AN26_3
52	–	–
54	–	–
56	AD1_1	AN11_1
58	AD1_3	AN11_3

Table 7.3 Main board connector CN3 (cont'd)

Pin	Main board function	Piggyback board device port
59	AD1_4	AN12_0
61	AD1_6	AN12_2
63	PWM0	P33_0
65	PWM2	P33_2
67	PWM4	P33_4
69	PWM6	P33_6
71	DIGIO16	P20_0
73	DIGIO18	P20_2
75	DIGIO20	P20_4
77	DIGIO22	P20_6
79	ENC0	CN_P10_5 *
81	–	–
83	MOT0U_P (RFU)	CN_P21_2 *
85	MOT0U_N (RFU)	CN_P21_3 *
87	MOT0V_P (RFU)	CN_P21_4 *
89	MOT0V_N (RFU)	CN_P21_5 *
91	MOT0W_P (RFU)	CN_P25_4 *
93	MOT0W_N (RFU)	CN_P25_3 *
95	–	–
97	–	–
99	–	–
101	GND	–
103	–	AN04_1
105	–	AN04_3
107	–	AN01_3
109	–	AN01_2
111	–	AN23_3
113	–	AN22_2
115	–	AN23_2
117	–	AN22_3
119	GND	–

Pin	Main board function	Piggyback board device port
60	AD1_5	AN12_1
62	AD1_7	AN12_3
64	PWM1	P33_1
66	PWM3	P33_3
68	PWM5	P33_5
70	PWM7	P33_7
72	DIGIO17	P20_1
74	DIGIO19	P20_3
76	DIGIO21	P20_5
78	DIGIO23	P20_7
80	ENC1	P10_6
82	–	–
84	O1 (RFU)	CN_P13_0 *
86	O2 (RFU)	CN_P13_1 *
88	O3 (RFU)	CN_P13_2 *
90	O4 (RFU)	CN_P13_3 *
92	O5 (RFU)	CN_P14_5 *
94	O6 (RFU)	CN_P14_4 *
96	–	–
98	–	–
100	–	CN_ETH0_SG_TXD_P *
102	–	CN_ETH0_SG_TXD_N *
104	–	–
106	–	CN_ETH0_SG_RXD_P *
108	–	CN_ETH0_SG_RXD_N *
110	–	–
112	–	CN_ETH1_SG_TXD_P *
114	–	CN_ETH1_SG_TXD_N *
116	–	–
118	–	CN_ETH1_SG_RXD_P *
120	–	CN_ETH1_SG_RXD_N *

Table 7.3 Main board connector CN3 (cont'd)

Pin	Main board function	Piggyback board device port
121	GND	–
123	GND	–
125	GND	–
127	GND	–

Pin	Main board function	Piggyback board device port
122	GND	–
124	GND	–
126	GND	–
128	GND	–

Note * By default these signals are not connected to CN3 to minimize signal interference. If required they can be connected via 0 Ω resistors. Check with the schematic for the related resistor of a signal.

[1)] For board version D018177_06_V01
[2)] For board version D018177_06_V02
[3)] For board version D018177_06_V03

(RFU) Ready for use with future main boards, available main boards do not support this function.

7.2 Debug Connector CN4

Table 7.4 On-chip debug connector CN4

Pin	Function	Device port
1		TODP0
3		TODN0
5	GND	
7	–	–
9	–	–
11	GND	
13	–	–
15	–	–
17	GND	
19	–	–
21	–	–
23	GND	
25	–	–
27	–	–
29	GND	
31	–	–
33	–	–
35	GND	
37	–	–

Pin	Function	Device port
2	VCC	
4	TCK	JP0_2
6	–	–
8	AURORES#	AURORES#_VCC
10	VSTBY	EMUVDD
12	TRST	TRST#
14	MD0	FLMD0_TOOL
16	EVTI0	P32_2
18	EVTO0	EVTO0#
20	MSYN#	MSYN#
22		RESET#
24	GND	
26		CICREFP
28		CICREFN
30	GND	
32	WDGDIS	–
34		RESETOUT#
36	GND	
38	TMS	JP0_3

Table 7.4 On-chip debug connector CN4

Pin	Function	Device port
39	–	–
41	GND	
43	–	–
45	–	–

Pin	Function	Device port
40	TDI / LPDIO / FPDR	JP0_0
42	GND	
44	TDO / LPDO / FPDT	JP0_1
46	DRDY	JP0_5

7.3 Device Ports Connectors CN5, CN13, CN14, CN15 and CN16

The device port connectors enable easy connection to almost all ports of the device.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.3.1 Device Ports Connector CN5

Table 7.5 Device ports connector CN5

Pin	PCB Silk	Device port	Pin	PCB Silk	Device port
1	H1	P30_7	2	G1	P30_0
3	H2	P30_9	4	G2	P30_2
5	H3	P30_11	6	G3	P30_4
7	H4	P34_0	8	G4	P30_6
9	H5	P34_4	10	G5	P34_3
11	H6	P33_11	12	G6	P31_11
13	H7	P33_12	14	G7	P32_3
15	H8	P31_14	16	G8	P31_15
17	H9	P23_1	18	G9	P23_0
19	H10	P23_5	20	G10	P23_4
21	H11	P23_7	22	G11	P23_6
23	H12	P24_2	24	G12	GETH1VCL
25	H13	P25_2	26	G13	P25_10
27	H14	P23_9	28	G14	P23_8
29	H15	P24_9	30	G15	P24_8
31	H16	P25_11	32	G16	P25_7
33	H17	CN_P21_3 *	34	G17	CN_P21_2 *
35	H18	CN_P21_5 *	36	G18	CN_P21_4 *
37	H19	CN_P24_5 *	38	G19	CN_P24_4 *
39	H20	CN_P24_7 *	40	G20	CN_P24_6 *
41	H21	CN_P25_3 *	42	G21	CN_P25_4 *
43	H22	CN_P25_5 *	44	G22	CN_P25_6 *
45	H23	P25_13	46	G23	P25_12
47	H24	P25_15	48	G24	P25_14

Table 7.5 Device ports connector CN5 (cont'd)

Pin	PCB Silk	Device port
49	H25	TRST#
51	H26	ERROROUT M#
53	H27	CN_JP0_3 *
55	H28	CN_JP0_1 *
57	H29	P20_0
59	H30	P20_4
61	H31	P20_5
63	H32	P20_6
65	H33	P15_11
67	H34	P15_12
69	H35	P14_0
71	H36	P14_1
73	H37	P14_12
75	H38	P12_0
77	H39	CN_P14_5 *
79	H40	CN_P14_4 *

Pin	PCB Silk	Device port
50	G25	FLMD0
52	G26	JP0_2
54	G27	CN_JP0_0 *
56	G28	CN_JP0_5 *
58	G29	P20_7
60	G30	P15_0
62	G31	P15_1
64	G32	P15_2
66	G33	P14_6
68	G34	P14_7
70	G35	P14_2
72	G36	P14_3
74	G37	P12_1
76	G38	P12_2
78	G39	P12_3
80	G40	CN_P12_4 *

Note * By default these signals are not connected to CN5 to minimize signal interference. If required they can be connected via 0 Ω resistors R117, R118, R120, R126, R148, R149, R153-R160, R163, R185-R188.

7.3.2 Device Ports Connector CN13

Table 7.6 Device ports connector CN13

Pin	PCB Silk	Device port
1	D1	AN03_3
3	D2	AN04_3
5	D3	AN12_2
7	D4	AN06_0
9	D5	AN04_0
11	D6	AN02_1
13	D7	AN01_0
15	D8	AN00_1
17	D9	LP_AN20_2

Pin	PCB Silk	Device port
2	C1	AN05_0
4	C2	AN04_1
6	C3	AN12_0
8	C4	AN06_3
10	C5	AN03_0
12	C6	AN03_1
14	C7	AN02_0
16	C8	AN01_1
18	C9	LP_AN20_0

Table 7.6 Device ports connector CN13 (cont'd)

Pin	PCB Silk	Device port
19	D10	LP_AN21_0
21	D11	AN22_0
23	D12	LP_AN21_2
25	D13	–
27	D14	AN24_1
29	D15	AN25_3
31	D16	AN26_3
33	D17	AN27_1
35	D18	AN30_0
37	D19	AN31_0
39	D20	AN36_1
41	D21	AN37_1
43	D22	AN38_1
45	D23	P00_5
47	D24	P00_4
49	D25	P00_3
51	D26	P00_2
53	D27	P00_1
55	D28	P00_8
57	D29	P00_7
59	D30	P00_0
61	D31	P01_12
63	D32	P01_10
65	D33	P10_10
67	D34	CN_P11_10 *
69	D35	CN_P10_3 *
71	D36	CN_P10_2 *
73	D37	P13_11
75	D38	P13_12
77	D39	P13_13
79	D40	P13_14

Pin	PCB Silk	Device port
20	C10	AN22_1
22	C11	LP_AN21_1
24	C12	AN23_3
26	C13	AN22_2
28	C14	–
30	C15	AN25_0
32	C16	AN25_2
34	C17	AN27_2
36	C18	AN30_1
38	C19	AN31_2
40	C20	AN36_2
42	C21	AN37_2
44	C22	AN38_2
46	C23	AN39_1
48	C24	P00_11
50	C25	P00_10
52	C26	P00_9
54	C27	P02_4
56	C28	P02_2
58	C29	P00_6
60	C30	P01_3
62	C31	P01_15
64	C32	P01_11
66	C33	P10_12
68	C34	P10_11
70	C35	CN_P10_5 *
72	C36	CN_P10_4 *
74	C37	P11_0
76	C38	P11_1
78	C39	CN_P11_2 *
80	C40	P11_3

Note * By default these signals are not connected to CN13 to minimize signal interference. If required they can be connected via 0 Ω resistors. Check with the schematic for the related resistor of a signal.

7.3.3 Device Ports Connector CN14

Table 7.7 Device ports connector CN14

Pin	PCB Silk	Device port
1	K1	P30_8
3	K2	P30_10
5	K3	P30_12
7	K4	P34_2
9	K5	P32_0
11	K6	P32_2
13	K7	P33_13
15	K8	P31_13
17	K9	P32_6
19	K10	P23_3
21	K11	P24_1
23	K12	GETH0VCL
25	K13	X1_C
27	K14	P23_11
29	K15	P24_11
31	K16	P25_9
33	K17	P22_3
35	K18	P22_1
37	K19	P24_3 1) CN_P24_3 * 2) 3)
39	K20	P22_5 1) CN_P22_5 * 2) 3)
41	K21	P22_8
43	K22	P22_10
45	K23	P22_12
47	K24	P22_13
49	K25	RESETOUT#
51	K26	RESET#
53	K27	VMONOUT#

Pin	PCB Silk	Device port
2	J1	P30_1
4	J2	P30_3
6	J3	P30_5
8	J4	P34_1
10	J5	P32_1
12	J6	P31_12
14	J7	P32_4
16	J8	P32_5
18	J9	NC
20	J10	P23_2
22	J11	P24_0
24	J12	ETH_SG_REFCLK
26	J13	X2_C
28	J14	P23_10
30	J15	P24_10
32	J16	P25_8
34	J17	P22_0
36	J18	P22_2
38	J19	P22_4
40	J20	P22_6
42	J21	P22_7
44	J22	P22_9
46	J23	P22_11
48	J24	RAMSVCL
50	J25	SBMD
52	J26	PWRCTL
54	J27	P20_2

Table 7.7 Device ports connector CN14 (cont'd)

Pin	PCB Silk	Device port
55	K28	P20_1
57	K29	P15_3
59	K30	P15_4
61	K31	P15_5
63	K32	P15_6
65	K33	P14_8
67	K34	P14_9
69	K35	P13_0 [1)] CN_P13_0 [* 2) 3)]
71	K36	P13_1 [1)] CN_P13_1 [* 2) 3)]
73	K37	P12_5
75	K38	P12_6
77	K39	P12_7
79	K40	P12_8

Pin	PCB Silk	Device port
56	J28	P20_3
58	J29	P15_7
60	J30	P15_8
62	J31	P15_9
64	J32	P15_10
66	J33	P14_10
68	J34	P14_11
70	J35	P13_2 [1)] CN_P13_2 [* 2) 3)]
72	J36	P13_3 [1)] CN_P13_3 [* 2) 3)]
74	J37	P13_8
76	J38	P13_9
78	J39	P13_10
80	J40	P12_9

Note * By default these signals are not connected to CN14 to minimize signal interference. If required they can be connected via 0 Ω resistors R138, R139, R141, R150-R152, R156, R157, R161, R163, R189, R200, R203.
[1)] For board version D018177_06_V01
[2)] For board version D018177_06_V02
[3)] For board version D018177_06_V03

Device Ports Connector CN15

Table 7.8 Device ports connector CN15

Pin	PCB Silk	Device port
1	B1	AN05_1
3	B2	AN05_2
5	B3	AN12_3
7	B4	AN06_1
9	B5	AN04_2
11	B6	AN03_2
13	B7	AN01_3
15	B8	AN00_3
17	B9	AN00_0
19	B10	LP_AN20_3

Pin	PCB Silk	Device port
2	A1	AN10_0
4	A2	AN05_3
6	A3	AN12_1
8	A4	AN10_3
10	A5	AN06_2
12	A6	AN02_3
14	A7	AN02_2
16	A8	AN01_2
18	A9	AN00_2
20	A10	LP_AN20_1

Table 7.8 Device ports connector CN15 (cont'd)

Pin	PCB Silk	Device port
21	B11	LP_AN21_3
23	B12	AN23_0
25	B13	AN24_0
27	B14	–
29	B15	AN24_2
31	B16	AN26_0
33	B17	AN26_2
35	B18	AN30_2
37	B19	AN31_3
39	B20	AN36_3
41	B21	AN37_3
43	B22	AN38_3
45	B23	AN39_2
47	B24	P02_10
49	B25	P02_8
51	B26	P02_6
53	B27	P02_5
55	B28	P02_3
57	B29	P02_0
59	B30	P01_4
61	B31	P01_6
63	B32	P01_13
65	B33	P10_14
67	B34	P10_13
69	B35	CN_P10_7 *
71	B36	P10_6
73	B37	P11_4
75	B38	P11_5
77	B39	P11_6
79	B40	P11_7

Pin	PCB Silk	Device port
22	A11	AN23_1
24	A12	AN22_3
26	A13	AN23_2
28	A14	AN24_3
30	A15	AN25_1
32	A16	AN26_1
34	A17	AN27_0
36	A18	AN27_3
38	A19	AN30_3
40	A20	AN31_1
42	A21	AN36_0
44	A22	AN37_0
46	A23	AN38_0
48	A24	AN39_0
50	A25	AN39_3
52	A26	P02_11
54	A27	P02_9
56	A28	P02_7
58	A29	P02_1
60	A30	P01_5
62	A31	P01_7
64	A32	P01_14
66	A33	P01_9
68	A34	P01_8
70	A35	P10_9
72	A36	P10_8
74	A37	P11_9
76	A38	P11_8
78	A39	CN_P10_1 *
80	A40	CN_P10_0 *

Note * By default these signals are not connected to CN15 to minimize signal interference. If required they can be connected via 0 Ω resistors R130, R136, R137.

7.3.4 Device Ports Connector CN16

Table 7.9 Device ports connector CN16

Pin	PCB Silk	Device port
1	F1	P33_10
3	F2	P33_9
5	F3	P33_8
7	F4	P33_7
9	F5	P33_6
11	F6	P33_5
13	F7	P33_4
15	F8	P33_3
17	F9	P33_2
19	F10	P33_1
21	F11	P33_0
23	F12	AN11_1
25	F13	AN11_0
27	F14	AN10_1

Pin	PCB Silk	Device port
2	E1	P31_10
4	E2	P31_9
6	E3	P31_8
8	E4	P31_7
10	E5	P31_6
12	E6	P31_5
14	E7	P31_4
16	E8	P31_3
18	E9	P31_2
20	E10	P31_1
22	E11	P31_0
24	E12	AN11_2
26	E13	AN11_3
28	E14	AN10_2

7.4 Ethernet Connector CN17, CN18, CN19 and CN22

Table 7.10 Device ports connector CN17

Pin	Device port
1	MDIN1
2	MDIP1
3	GND
4	GND
5	GND
6	GND
7	GND
8	GND

Table 7.11 Device ports connector CN18

Pin	Device port
1	MDIN0
2	MDIP0
3	GND
4	GND
5	GND
6	GND
7	GND
8	GND

Table 7.12 Device ports connector CN19

Pin	Device port
1	MDIN1 *
2	MDIP1 *

Note * By default these signals are not connected to CN19. If required they can be connected via 0 Ω resistors R83, R84.

Table 7.13 Device ports connector CN22

Pin	Device port
1	MDIN0 *
2	MDIP0 *

Note * By default these signals are not connected to CN22. If required they can be connected via 0 Ω resistors R86, R87.

7.5 RHSB1/MSPI6 Connector CN23

Table 7.14 RHSB1/MSPI6 connector CN23

Pin	SW3-2 = ON (RHSB1/MSPI6_MUX)		SW3-2 = OFF (RHSB1/MSPI6_MUX)	
	Device port	Function	Device port	Function
1	P10_0	CLK_P, DATA_IN_P (RHSB1MCSIP / RHSB1FCLP / MSPI6_SCKP)	–	–
3	P10_1	CLK_N, DATA_IN_N (RHSB1MCSIN / RHSB1FCLN / MSPI6_SCKN)	–	–
7	–	–	P10_0	CLK_P, DATA_IN_P (RHSB1MCSIP / RHSB1FCLP / MSPI6_SCKP)
9	–	–	P10_1	CLK_N, DATA_IN_N (RHSB1MCSIN / RHSB1FCLN / MSPI6_SCKN)

Pin	Device port	Function
5[1)]	JP3[1-2]: P10_7 JP3[2-3]: P11_2	RHSB1CSD0 MSPI6CSS0
5[2)]	-	-
6[1)]	P12_4	MSPI6SSI
6[2)]	JP3[1-2]: P10_7 JP3[2-3] and JP6[1-2]: P11_2 JP3[2-3] and JP6[2-3]: P12_4	RHSB1CSD0 MSPI6CSS0 MSPI6SSI
11	–	GND
12	–	GND
2[1)]	P10_2	DATA_OUT_P
4[1)]	P10_3	DATA_OUT_N
8[1)]	P10_4	DATA_IN_P
10[1)]	P10_5	DATA_IN_N

Pin	[2)]SW3-3 = ON (RHSB1/MSPI6_MUX_2)		[2)]SW3-3 = OFF (RHSB1/MSPI6_MUX_2)	
	Device port	Function	Device port	Function
2[2)]	P10_4	DATA_IN_P (MSPI6_SIP)	P10_2	DATA_OUT_P (RHSB1MCSOP / RHSB1SOP / MSPI6_SOP)
4[2)]	P10_5	DATA_IN_N (MSPI6_SIN)	P10_3	DATA_OUT_N (RHSB1MCSON / RHSB1SON / MSPI6_SON)

8[2)]	P10_4	DATA_OUT_P (RHSB1MCSOP / RHSB1SOP / MSPI6_SOP)	P10_2	DATA_IN_P (MSPI6_SIP)
10[2)]	P10_5	DATA_OUT_N (RHSB1MCSON / RHSB1SON / MSPI6_SON)	P10_3	DATA_IN_N (MSPI6_SIN)

[1)] On board version D018177_06_V01
[2)] On board versions other than D018177_06_V01

The chapter 6.6 for further information.

7.6 RHSB0 Connector CN24

Table 7.15 RHSB0 connector CN24

Pin	SW3-1 = ON (RHSB0_MUX)		SW3-1 = OFF (RHSB0_MUX)	
	Device port	Function	Device port	Function
1	P25_4	CLK_P/DATA_IN_P	–	–
2	–	–	P25_4	CLK_P/DATA_IN_P
3	P25_3	CLK_P/DATA_IN_N	–	–
4	–	–	P25_3	CLK_P/DATA_IN_N
5	–	–		–
6	P22_5	CS_OUT	P22_5	CS_OUT
7	–	–	P25_6	DATA_OUT_P
8	P25_6	DATA_OUT_P	–	–
9	–	–	P25_5	DATA_OUT_N
10	P25_5	DATA_OUT_N	–	–
11	–	GND		GND
12	–	GND		GND

See chapter 6.5 for further information.

7.7 MSPI9 Connector CN26

Table 7.16 MISP9 connector CN26

Pin	Device port	Function
1	P13_1	CLK_P
2	P14_4	DATA_IN_P
3	P13_0	CLK_N
4	P14_5	DATA_IN_N
5[1)] 5[2)]	P11_10 -	SSI_IN -
6[1)] 6[2)]	P12_5 JP7[1-2]: P12_5 JP7[2-3]: P11_10	CS_OUT CS_OUT SSI_IN
7	–	–
8	P13_3	TXDP
9	–	–
10	P13_2	TXDN
11	–	GND
12	–	GND

1) On board version D018177_06_V01
2) On board versions other than D018177_06_V01

See chapter 6.7 for further information.

7.8 RHSIF0 Connector CN27

Table 7.17 RHSIF0 connector CN27

Pin	JP4 connected		JP4 open	
	Device port	Function	Device port	Function
1	P21_3	RXDP	P21_5	TXDP
2	–	GND	–	GND
3	P21_2	RXDN	P21_4	TXDN
4	–	GND	–	GND
5	–	–	–	–
6	P22_3	REFCLK	P22_3	REFCLK
7	P21_5	TXDP	P21_3	RXDP
8	–	GND	–	GND
9	P21_4	TXDN	P21_2	RXDN

Table 7.17 RHSIF0 connector CN27 cont'd

Pin	JP4 connected		JP4 open	
	Device port	Function	Device port	Function
10	–	GND	–	GND
11	–	GND	–	GND
12	–	GND	–	GND

See chapter 6.8 for further details.

7.9 RHSIF1 Connector CN28

Table 7.18 RHSIF1 connector CN28

Pin	JP4 connected	
	Device port	Function
1	P24_5	RXDP
2	–	GND
3	P24_4	RXDN
4	–	GND
5	–	–
6	P24_3	REFCLK
7	P24_7	TXDP
8	–	GND
9	P24_6	TXDN
10	–	GND
11	–	GND
12	–	GND

See chapter 6.9 for further details.

7.10 Pull-Up/Pull-Down Pin Header CN29

Table 7.19 Pull-up/pull down connector CN29

Pin	Function
1	fixed L level
3	
5	
7	
9	
11	
13	
15	

Pin	Function
2	fixed H level, 3.3V
4	
6	
8	
10	fixed H level, 5.0V
12	
14	
16	

8. Jumper Configuration Examples

Several functions of the board can be configured via jumpers.
The board is shipped without any jumpers set.

For a complete list of jumpers refer to *2.1 Jumper Overview*.

For jumper settings related to the device operation mode, refer to *6.1 Operation Mode Selection*.

The following sections show some jumper settings, that allow to operate the piggyback board in different power supply configurations.

8.1 Stand-Alone Operation with Power Supply by Debugger

Basically, the piggyback board can solely be powered by a connected debugger. Please make sure the debug tool can provide sufficient current on the power supply rails to operate the board in a useful manner.

Due to the limited current capability of Renesas' E2 Emulator, powering the board only via this debugger is not feasible.

In case of using another debug tool check its specification whether powering the piggyback board with the tool is possible.

8.2 Operation using FCC Device or Mass Production Device

It is possible to use a device with additional debug functions called FCC device or a mass production device with the piggyback board. There are some differences between FCC device or mass production (MP) device.

Jumper JP1

- When using a MP device do open jumper JP1.
- When using the FCC device, the AURORES# signal has to be provided to the device. On the CN4 debug connector there are 2 signals that can be used for this signal.
  - If the AURORES# signal on CN4 is to be used for the FCC device put a jumper to JP1[2-3].
  - If the TRST# signal on CN4 is to be used for the FCC device put a jumper to JP1[1-2].

Switch SW4

- When using a MP device, or an FCC device with a debug tool that does not support Aurora interface, the signals EVTO0 and MSYN# are not needed on the processor. The switches SW4-1, SW4-2, SW4-3 must be set OFF.
- When using an FCC device with a debug tool supporting Aurora interface the signals EVTO0 and MSYN# on connector CN4 must be connected to the device.
  SW4-1 must be set ON to select the MSYN# signal,
  For EVTO0 control set
  - SW4-2 to ON to select the device EVTO# signal, or
  - SW4-3 to ON to select P32_0.

Power supply for debug interface

Some power supply jumpers only must be connected when the device is an FCC device. They are not needed when a MP device is used.

- CN10[37-38]: This jumper must be set to provide 3.3V to EMUVCC
- CN10[46-47-48]: This jumper must be set to provide supply voltage to J0VCC/J1VCC. The voltage level must be the same as for VCC.
  - CN10[46-47]: use 3.3V for J0VCC/J1VCC
  - CN10[47-48]: use 5.0V for J0VCC/J1VCC
- CN31 has a jumper to enable EMUVDD supply for an FCC device. This is not needed when a MP device is used.
  - CN31[10-11]: use onboard VDD as EMUVDD

Table 8.1 Power supply jumper settings for FCC devices and MP devices

Purpose	Jumper	RH850/U2B10 RH850/U2B20 RH850/U2B24	RH850/U2B10-FCC RH850/U2B20-FCC RH850/U2B24-FCC
AURORES# Config	JP1	---	O
PWRCTL Config	JP2	U2B10: --- U2B20, U2B24: O	U2B10-FCC: --- U2B20-FCC, U2B24-FCC: O
Port Select for CS_OUT on CN23	JP3	O	O
TX and RX Signal swap on RHSIF0 Interface	JP4	O	O
TRST# Signal Source Select	JP5	O	O
FLMD0 Config	JP46	---	---
SBMD Config	JP47	--- (U2B10) / O (U2B20, U2B24) Please refer to *Table 6.1 Device operation mode selection jumpers*	--- (U2B10-FCC) / O (U2B20-FCC, U2B24-FCC) Please refer to *Table 6.1 Device operation mode selection jumpers*
FLMD1 Config	JP48	---	---
LED Output Config	CN7	O	O
A1VREFH Config	CN10[1-2-3]	O	O
A1VCC Config	CN10[4-5-6]	O	O
A0VREFH Config	CN10[7-8-9]	O	O
A0VCC Config	CN10[10-11-12]	O	O
ADSVCC Config	CN10[13-14-15]	O	O
A2VCC Config	CN10[16-17-18]	O	O
A2VREFH Config	CN10[19-20-21]	O	O
AFCVCC Config	CN10[22-23-24]	O	O
A3VCC Config	CN10[25-26-27]	O	O
A3VREFH Config	CN10[28-29-30]	O	O
E1VCC Config	CN10[31-32-33]	O	O
E0VCC Config	CN10[34-35-36]	O	O
EMUVCC Config	CN10[37-38-39]	---	CN10[37-38]
E2VCC Config	CN10[40-41-42]	O	O
SVRDRVCC Config	CN10[43-44-45]	O	O
J0VCC, J1VCC Config	CN10[46-47-48]	O, same as VCC Config	O
SYSVCC Config	CN10[49-50-51]	O	O

Table 8.1 Power supply jumper settings for FCC devices and MP devices

Purpose	Jumper	RH850/U2B10 RH850/U2B20 RH850/U2B24	RH850/U2B10-FCC RH850/U2B20-FCC RH850/U2B24-FCC
VCC Config	CN10[52-53-54]	O	O
GETH0BVCC Config	CN10[55-56-57]	U2B10: open, U2B20, U2B24: CN10[55-56]	U2B10-FCC: open, U2B20-FCC, U2B24-FCC: CN10[55-56]
GETH0PVCC Config	CN10[58-59-60]	U2B10: NC (CN10[59-60] or open) U2B20, U2B24: CN10[58-59]	U2B10-FCC: NC (CN10[59-60] or open) U2B20-FCC, U2B24-FCC: CN10[58-59]
VDDIOF Config	CN10[61-62-63]	O	O
ADVSREFH Config	CN10[64-65-66]	O	O
+5.0V power supply from main board	CN12	O	O
int_P3V3 Config	CN20	O	O
+3.3V power supply from main board	CN30	O	O
Ext_VDD Config	CN31[1-2-3]	O	O
VDD Config	CN31[4-5-6]	O	O
VDD Config	CN31[7-8-9]	O	O
EMUVDD Config	CN31[10-11-12]	---	CN31[10-11]
Ethernet enable switch	SW2	U2B10: OFF U2B20, U2B24: O	U2B10-FCC: OFF U2B20-FCC, U2B24-FCC: O
Debug port connection EVTO0 / MSYN#	SW4	OFF	O

--- : Jumper open
O : possible setting
The lines marked in yellow are for use with FCC devices only.

8.3 Configuration Examples

8.3.1 General Settings

All the following board configurations are based on these conditions:

- Normal device operation mode (JP46[OPEN]: FLMD0 = L).
- All voltages for all functions are activated.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN8 (GND), CN9 (+5.0 V) and CN21 (*3.3 V) are assembled on the board.
- If also the core supply voltage of 1.12 V will be supplied from an external power supply the connector CN11 (included in the package) must be assembled on the PCB.

8.3.2 Jumper Indicators

- The green jumper JP46 for FLMD0 must always be open for a ‘normal’ (user mode and debug) operation of the device.
- The red jumpers are related to the power supply configuration.
  Following jumper symbols are used:
  - : Jumper must not be set.
  - 1 2 3: Jumper must be set in the indicated position, in this case position [2-3]
  - 1 2 3: Jumper can be set to position [1-2] or position [2-3]
  - 1 2 3: Jumper with optional setting. The red setting [2-3] is the default setting. The blue setting [1-2] is the optional setting.

Note

The pin 1 of a jumper can be identified by

- a small circle near the jumper
- a square soldering pad.

8.3.3 Stand-Alone Operation with Single External Power Supply 3.3V: Minimum Configuration 1

This example enables to operate the board with only the 3.3 V external power supply.
VDD is provided from SVR controller.
Since no 5 V voltage is available, all I/O ports can only use 3.3 V.

Table 8.2 Power supply connectors for single power supply 3.3V

Connector	Name	Ext. Power Supply	Remarks
CN8	GND	Connected, GND	
CN9	5.0 V	Not connected	Jumpers in CN10 (VCC and VREF selection) are set to 3.3 V position CN10[1-2]
CN11	1.12 V	Not connected	VDD from SVR_OUTPUT (CN31[6-5]) from on-chip Switching Voltage Regulator. Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
CN21	3.3 V	Connected, +3.3 V	

Note

・AWOVCL: Regarding AWOVCL setting (CN31[7-8-9]) please refer to *Table 6.1 Device operation mode selection jumpers*
・PWRCTL: for U2B10: JP2[open]

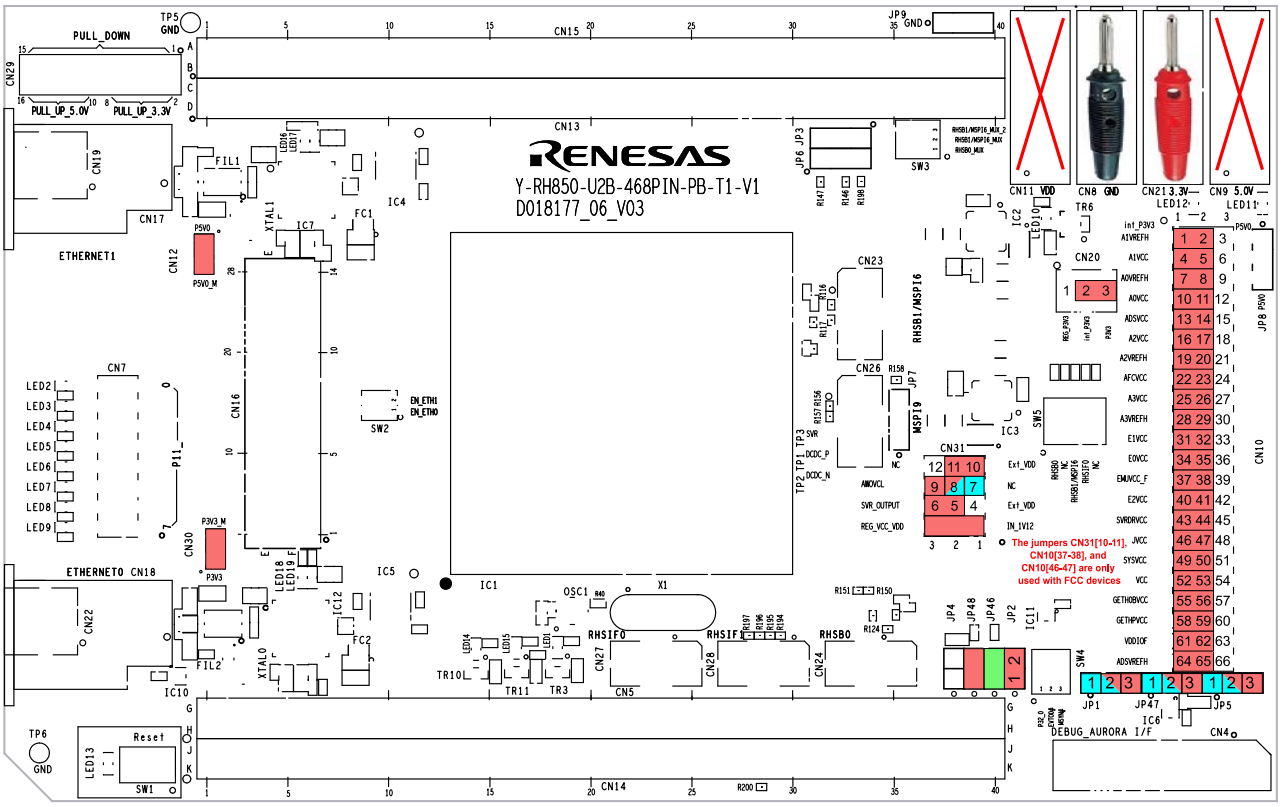


Figure 8.1 Stand-alone operation with single external power supply 3.3V

8.3.4 Stand-Alone Operation with Single External Power Supply 5.0V: Minimum Configuration 2

This example enables to operate the board with only the 5.0 V external power supply. VDD is generated using the voltage generator on the piggyback board. All I/O ports can only use 5.0 V.

Table 8.3 Power supply connectors for single power supply 5.0V

Connector	Name	Ext. Power Supply	Remarks
CN8	GND	Connected, GND	
CN9	5.0 V	Connected, 5.0 V	
CN11	1.12 V	Not connected	VDD from onboard voltage regulator (CN31[5-4] and CN31[2-3]). Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
CN21	3.3 V	Not connected	3.3V from onboard voltage regulator (CN20[1-2]). Jumpers in CN10 (VCC and VREF selection) are set to 5.0 V position. EMUVCC can only be connected to 3.3V (CN31[37-38]).

Note

- GETH0BVCC: U2B10: open, U2B20 and U2B24: CN10[55-56]
- GETH0PVCC: U2B10: NC(CN10[59-60] or open), U2B20 and U2B24: CN10[58-59]
- PWRCTL: for U2B10: JP2[open]
- SMBD input selection (JP47): Please refer to *Table 6.1 Device operation mode selection jumpers*

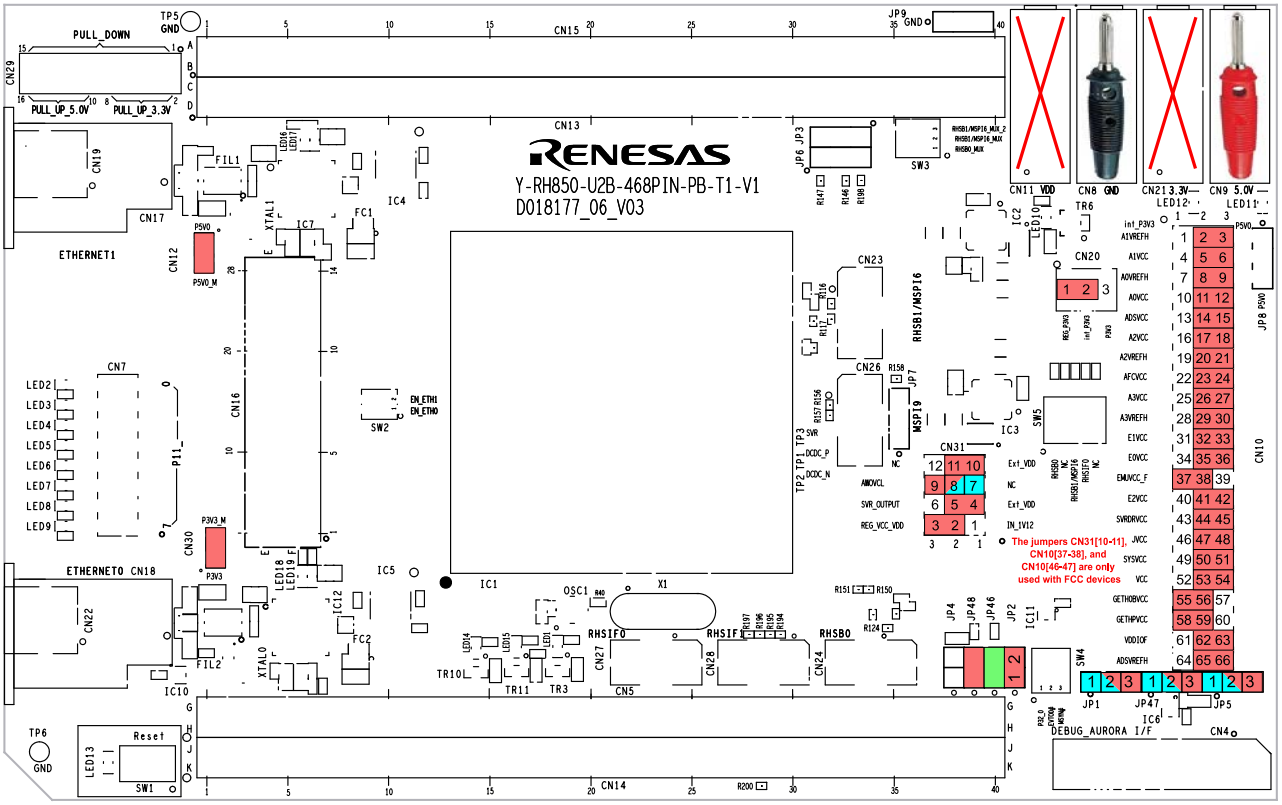


Figure 8.2 Stand-alone operation with single external power supply 5.0V

8.3.5 Stand-Alone Operation with All External Power Supplies: Maximum Configuration

This example assumes all external power supplies are connected and used.

Table 8.4 Power supply connectors to use all external power supplies

Connector	Name	Ext. Power Supply	Remarks
CN8	GND	Connected, GND	
CN9	5.0 V	Connected, 5.0 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in CN10 Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in CN10.
CN11	1.12 V	Connected, 1.12 V	CN31[1-2] and CN31[4-5]: use IN_1v12 for VDD voltage Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
CN21	3.3 V	Connected, 3.3 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in CN10 CN20[2-3]: use p3V3 supply for 3.3 V Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in CN10.

Note

- CN11：solder connector for CN11 to the piggyback board
- GETH0BVCC：U2B10: open, U2B20 and U2B24: CN10[55-56]
- GETH0PVCC：U2B10: NC(CN10[59-60] or open), U2B20 and U2B24: CN10[58-59]
- PWRCTL: for U2B10: JP2[open]

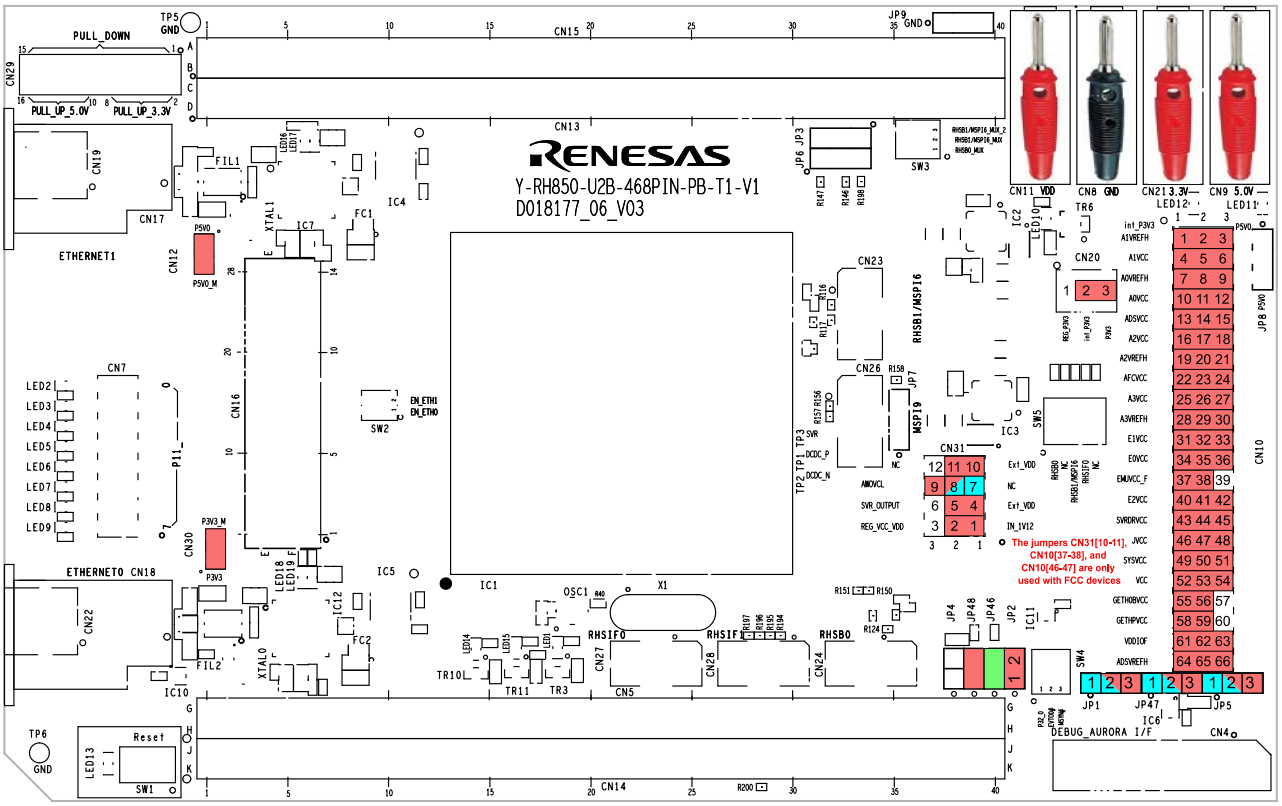


Figure 8.3 Stand-alone operation with all external power supplies

8.3.6 Operation on the Main Board: No External Supply

This example assumes the piggyback board is plugged onto a main board, which provides 3.3 V and 5.0 V.

Do not supply the 5V (CN9) and 3.3V (CN21) voltage directly to the piggyback board

Table 8.5 Power supply connectors to use power supply from main board

Connector	Name	Ext. Power Supply	Remarks
CN8	GND	Not connected	
CN9	5.0 V	Not connected	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in CN10. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in CN10.
CN11	1.12 V	Not connected	VDD supply: – CN31[2-3] and CN31[4-5]: use reg_vcc_VDD from onboard voltage regulator for supply of VDD voltage – CN31[6-5]: use SVR_OUTPUT from on-chip Switching Voltage Regulator Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage and possible settings of jumpers in CN31.
CN12	P5V0_M		Use jumper CN12[1-2] to connect the 5.0 V supply from the main board to the piggyback board
CN21	3.3 V	Not connected	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in CN10. 3.3V from Main Board (CN20[2-3]) or from onboard voltage regulator (CN20[1-2]). Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in CN10.
CN30	P3V3_M		Use jumper CN30[1-2] to connect the 3.3 V supply from the main board to the piggyback board

Note

This configuration still allows to utilize an external IN_1v12 voltage (connected to CN8, CN11) as the source for VDD voltage. In this case set CN31[1-2] and CN31[4-5].

- GETH0BVCC：U2B10: open, U2B20 and U2B24: CN10[55-56]
- GETH0PVCC：U2B10: NC(CN10[59-60] or open), U2B20 and U2B24: CN10[58-59]
- PWRCTL: for U2B10: JP2[open]

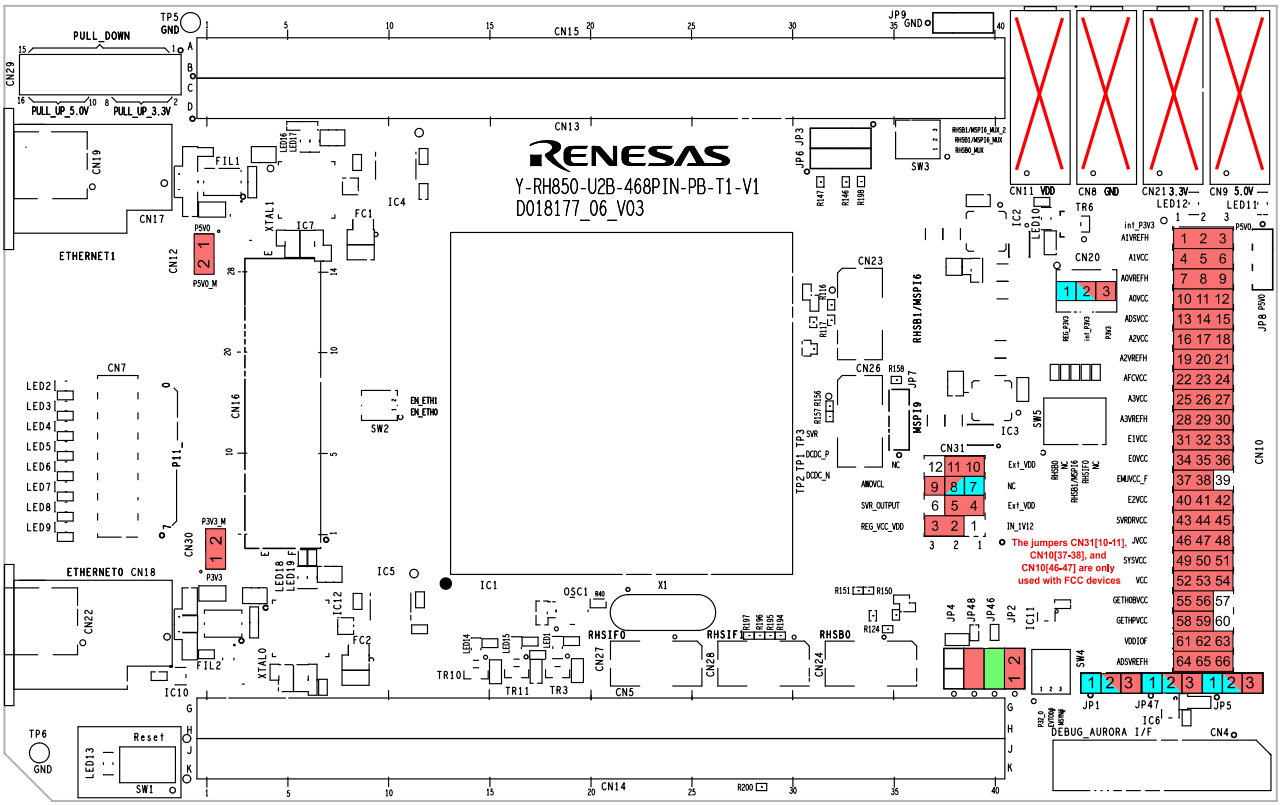


Figure 8.4 Main board operation without external power supply

CAUTION

Do not supply 5V (CN9) and 3.3V (CN21) directly to the piggyback board if these voltages are already supplied by the main board.

9. Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied when the power supply to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW1 into '5-6 ON' position, so that RESET is permanently asserted.
   Alternatively keep SW1 manually in' 5-4 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, release RESET by returning SW1 into the 'OFF' position.

For details how to apply a RESET, please refer to *6.2 RESET Switch*.

.

9.2 Factory Rework on Board Marked D018177_06_V01

The PCB layout of Y-RH850-U2B-468PIN-PB-T1-V1 (board marked D018177_06_V01)) has 2 faults:

- Source and drain pins on FET TR1 are wrongly connected.
- A capacitor of min 24.1µF is missing on the SVR circuit.

These faults are corrected in production as described in *9.2.1 Connection of FET TR1* and *9.2.2 Capacitors on SVR Circuit*.

Below picture shows the reworked PCB where both modifications have been applied.

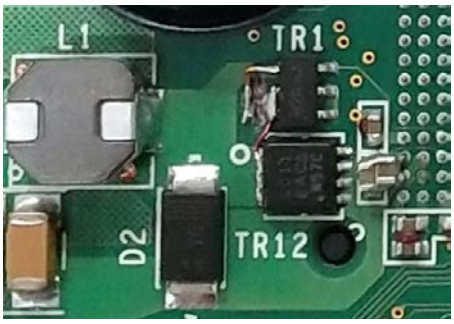


Figure 9.1 Reworked PCB

9.2.1 Connection of FET TR1

The signals to source pin and drain pins of FET TR1 (Vishay SQ3425EV) are wrongly connected.

The source signal is available on pin #4.

The drain signal is available on pins #1,2,5,6.

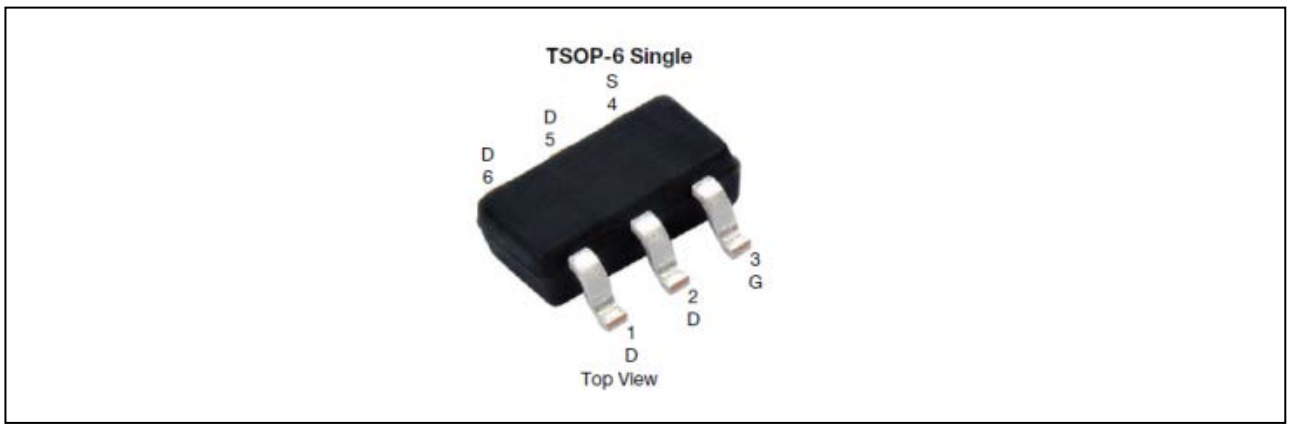


Figure 9.2 Pin assignment of FET TR1

For correct operation the signal connection at source and drain must be swapped.

TR1 is placed on the bottom side of the PCB. The change is done in 3 steps.

Step1:

Cut the PCB traces on the left side (facing away from the microcontroller) of TR1.

See the green lines in *Figure 9.3 Changes on TR1 to swap source and drain pins*.

Instead of cutting the line at pin 4, possibly also bending the pin up may be applicable.

Step2:

Use a wire to connect the Source pin 4 to the former signal of pins 1,2,5,6.

See the yellow line in in *Figure 9.3 Changes on TR1 to swap source and drain pins*.

Step 3:

Use a wire to connect the four drain pins (#1,2,5,6) to the former signal of pin4.

See the yellow line in in *Figure 9.3 Changes on TR1 to swap source and drain pins*.

This signal also available at TR12 or D2.

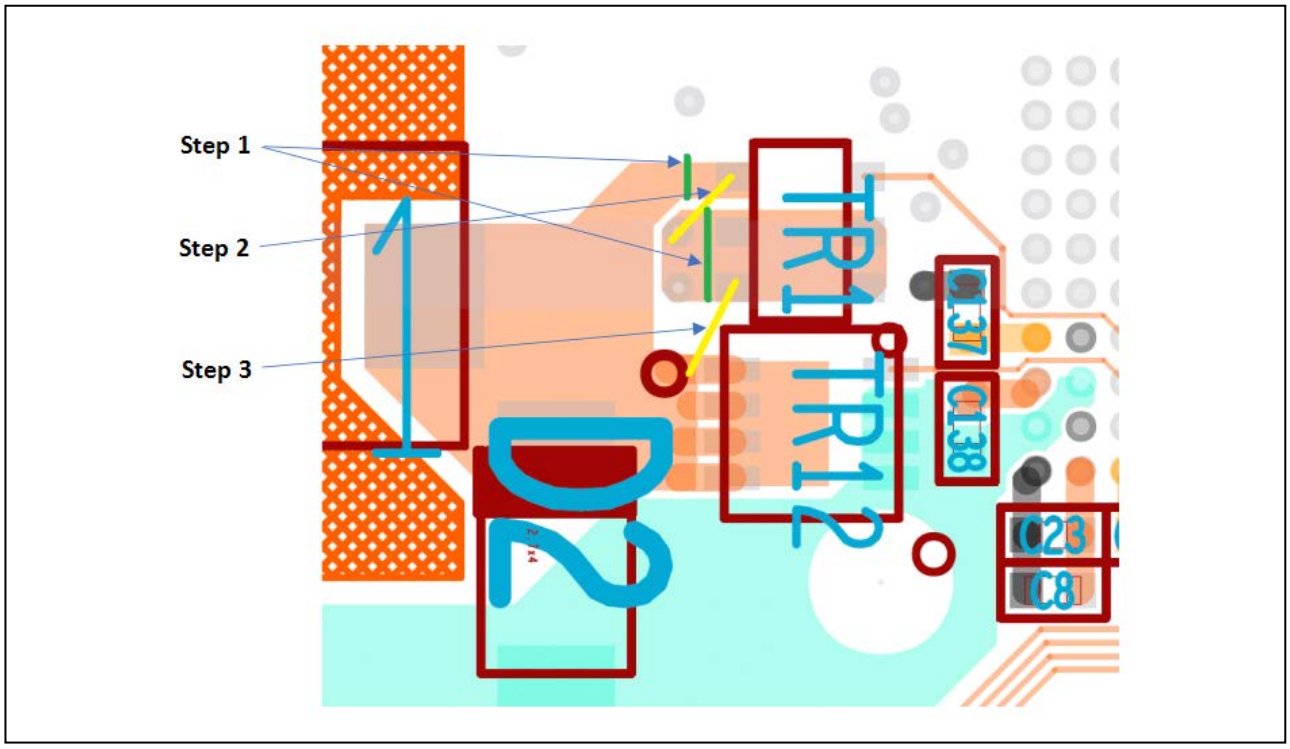


Figure 9.3 Changes on TR1 to swap source and drain pins

9.2.2 Capacitors on SVR Circuit

A capacitor of min 24.1µF is missing within the SVR circuitry.

To solve this issue three capacitors of 10µF each are added manually on the board.

The 10µF must be X5R or X7R type, 6.3V, 0402 package.

The three capacitors can be placed on top of the assembled capacitor C138 on the bottom side of the PCB:

Figure 9.4 Place to add additional capacitors

9.3 Factory Rework on Board Marked D018177_06_V02

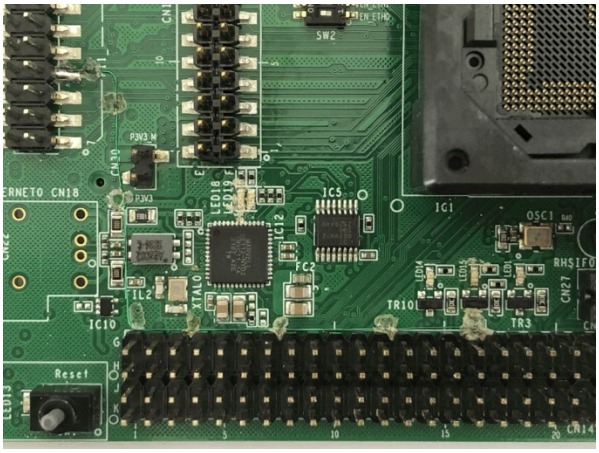
The PCB layout of Y-RH850-U2B-468PIN-PB-T1-V1 (board marked D018177_06_V01 and board marked with D018177_06_V02) have one fault:

- The ETH0TXCLK signal that is output by the U2B device on P11_4 is connected to CN1.62, as well as to CN1.89 (DIGIO4) and CN7.9 (LED6).
  As a result the signal quality is degraded and a reliable communication to the Ethernet circuitry on the main board is not possible.

To solve this fault, P11_4 is exchanged to the port P22_0 at CN1.89 (DIGIO_4) and CN7.9 (LED6).

The required changes to the D018177_06_V02 board version are applied during production and can be seen in the pictures below.

Top side rework



Bottom side rework

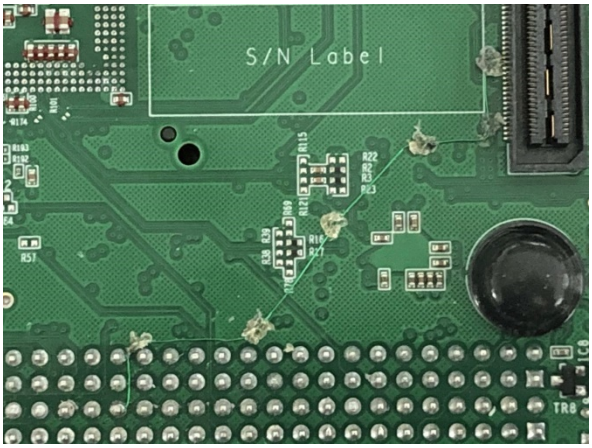


Figure 9.5 Board rework

9.4 Misprint at Switch SW5 on Board Marked D018177_06_V02

The printing on the DIP switches SW5-4 and SW5-5 on board D01877_06_V02 is wrong.

Table 9.1 PCB print at switch SW5 lists the printing on the board for all switches and shows the corrections.

Table 9.1 PCB print at switch SW5

Switch	Printing on the board	Correct print
SW5-1	RHSB0	RHSB0
SW5-2	NC	NC
SW5-3	RHSB1/MSPI6	RHSB1/MSPI6
SW5-4	NC	**RHSIF0**
SW5-5	RHSIF1	**NC**

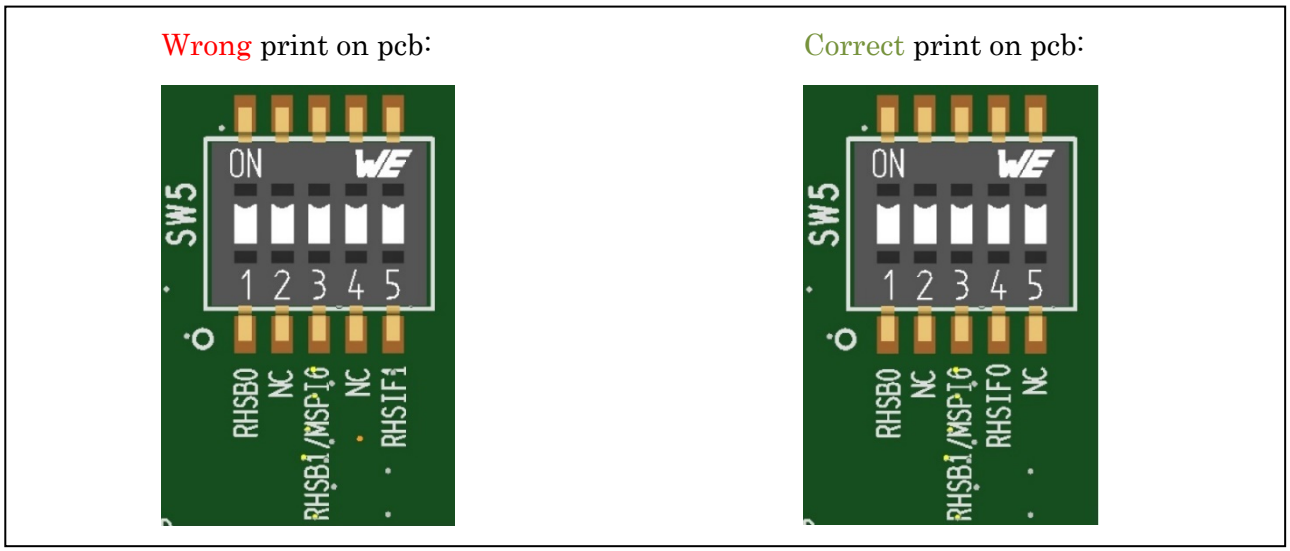


Figure 9.6 Printing at switch SW5

9.5 Ethernet Reset Signals

The piggyback board provides 2 Ethernet channels. For each channel it is possible to use either the PHY included in the piggyback board, or to use a PHY connected to the main board.

The power supply for these PHY are 3.3V. Therefore the domain power supply for Reset signal as well as other input signals should be set 3.3V. *Table 9.2 Ports for Ethernet reset signals* shows the power supply sources used for the ports.

On the first revision of the piggyback board (D018177_06_V01) both the onboard PHY and the PHY on the main board use the same RH850 port for Ethernet reset.

On the second revision of the piggyback board (D018177_06_V02) the onboard PHY and the PHY on the main board use different RH850 ports for Ethernet reset.

On the third revision of the piggyback board (D018177_06_V03) the onboard PHY and the PHY on the main board will again use the same RH850 ports for Ethernet reset.

Table 9.2 Ports for Ethernet reset signals

	Board D018177_06_V01		Board D018177_06_V02		Board D018177_06_V03	
	PHY on piggyback board	PHY on main board	PHY on piggyback board	PHY on main board	PHY on piggyback board	PHY on main board
Port used for reset signal of ETH0	P12_3 (E2VCC)	P12_3 (E2VCC)	P10_8 (E1VCC)	P12_3 (E2VCC)	P10_8 (E1VCC)	P10_8 (E1VCC)
Port used for reset signal of ETH1	P30_0 (E0VCC)	P30_0 (E0VCC)	P12_3 (E2VCC)	P30_0 (E0VCC)	P12_3 (E2VCC)	P12_3 (E2VCC)

9.6 Power On Piggyback Board Without RH850 Microcontroller installed

The piggyback board Y-RH850-U2B-468PIN-PB-T1-V1 is not designed to be powered on when the RH850 microcontroller is not installed in socket IC1.

If the microcontroller is not installed the SVR power supply circuit does not have the control signals SVRNGATE and SVRPGATE and may be damaged.

If for some reason the board has to be powered on without a microcontroller mounted in socket IC1 please make sure the jumper CN10[43-44-45] (SVRDRVCC) is open. In this case no power is supplied to the SVR control circuit, and it will not be damaged.

If the piggyback board is being used with the microcontroller installed please make sure the ports SVRNGATE and SVRPGATE are set to “Fixed” (output) in bit SVRENDCDCHZ in option byte 25.

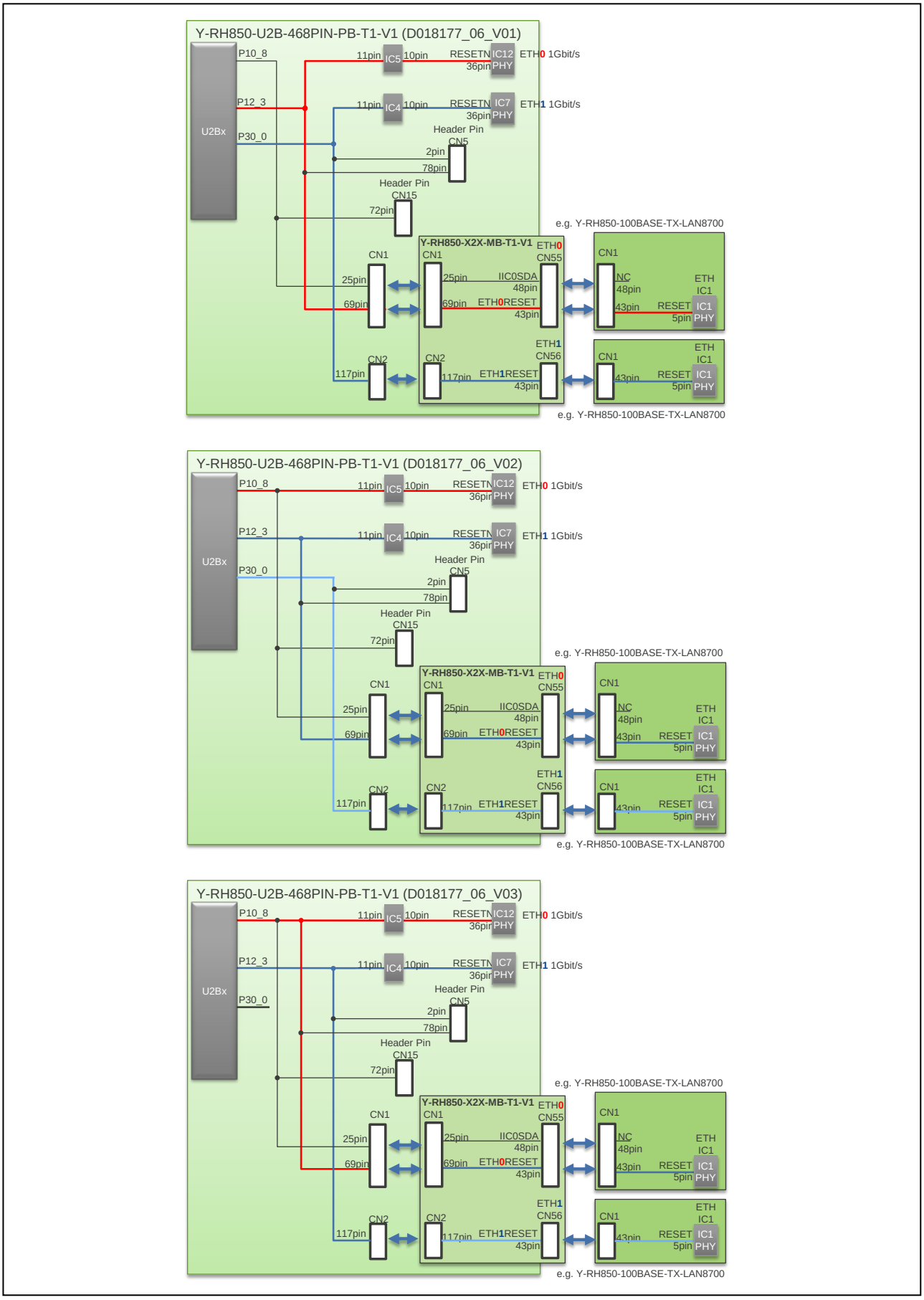


Figure 9.7 Ethernet reset signals on boards D018177_06_V01, D018177_06_V02 and D018177_06_V03

10. Mechanical Dimensions

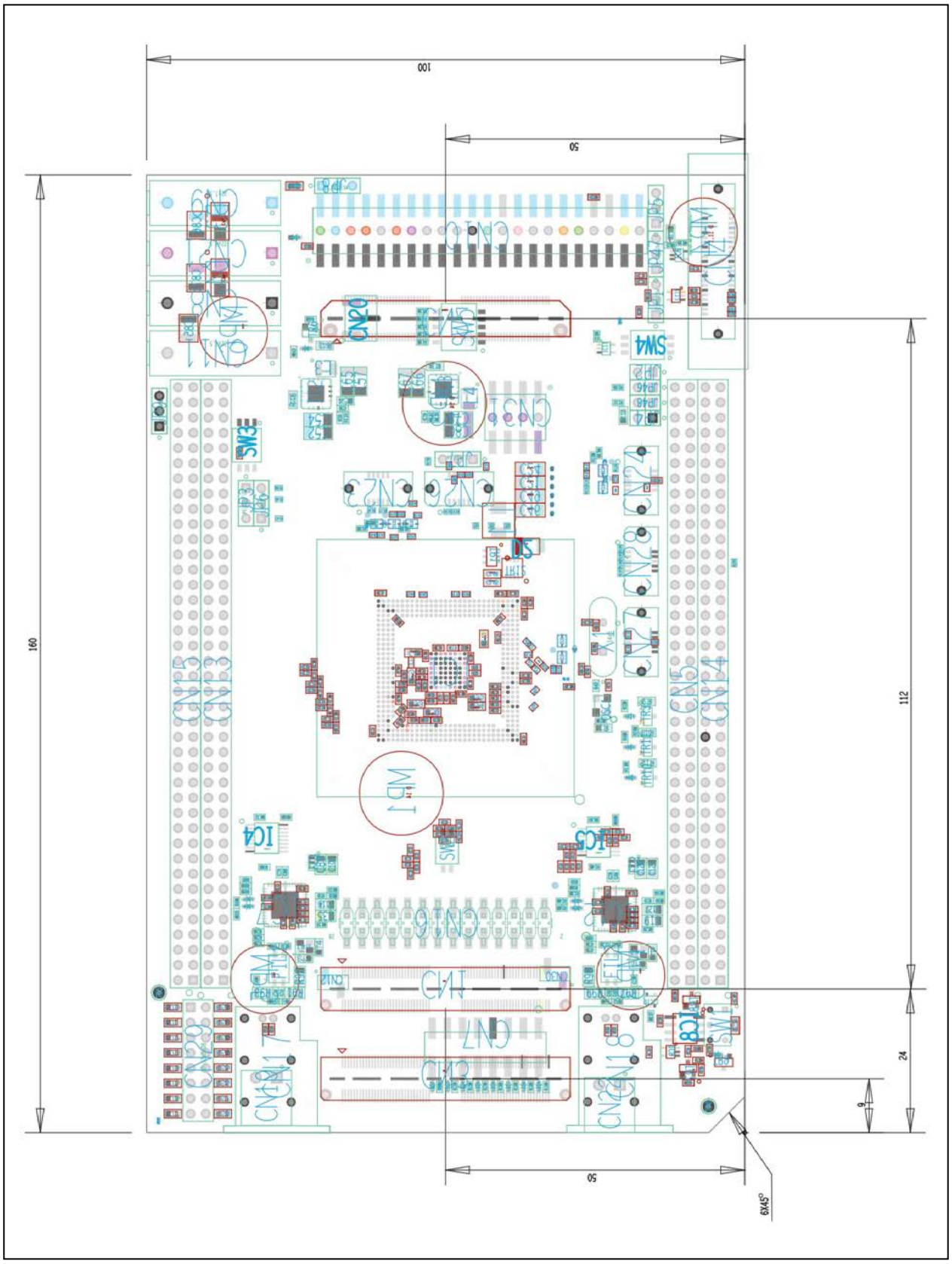


Figure 9.1 Mechanical dimensions

11. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.

The following components described in the schematics are not provided with the board upon delivery:

- Capacitors: C90, C97, C98, C101, C121, C122
- Resistors: R5, R7, R19, R20, R22, R23, R25, R34-R40, R57, R58, R64, R69, R78, R79, R103, R104, R107, R114-R118, R120-R126, R130, R136-R141, R146-R161, R163, R175, R177, R185 – R188
  (Board version D018177_06_V01).
- Resistors: R5, R7, R19-R20, R22-R23, R25, R34-R39, R40, R57-R58, R64, R69, R78-R79, R103-R104, R107, R114-R115, R120-R123, R139, R185-R188
  (Board versions other than D018177_06_V01)

The above components are indicated with "DNF/DNB" in the schematics.

The following components described in the schematics are provided with but not mounted on the board upon delivery:

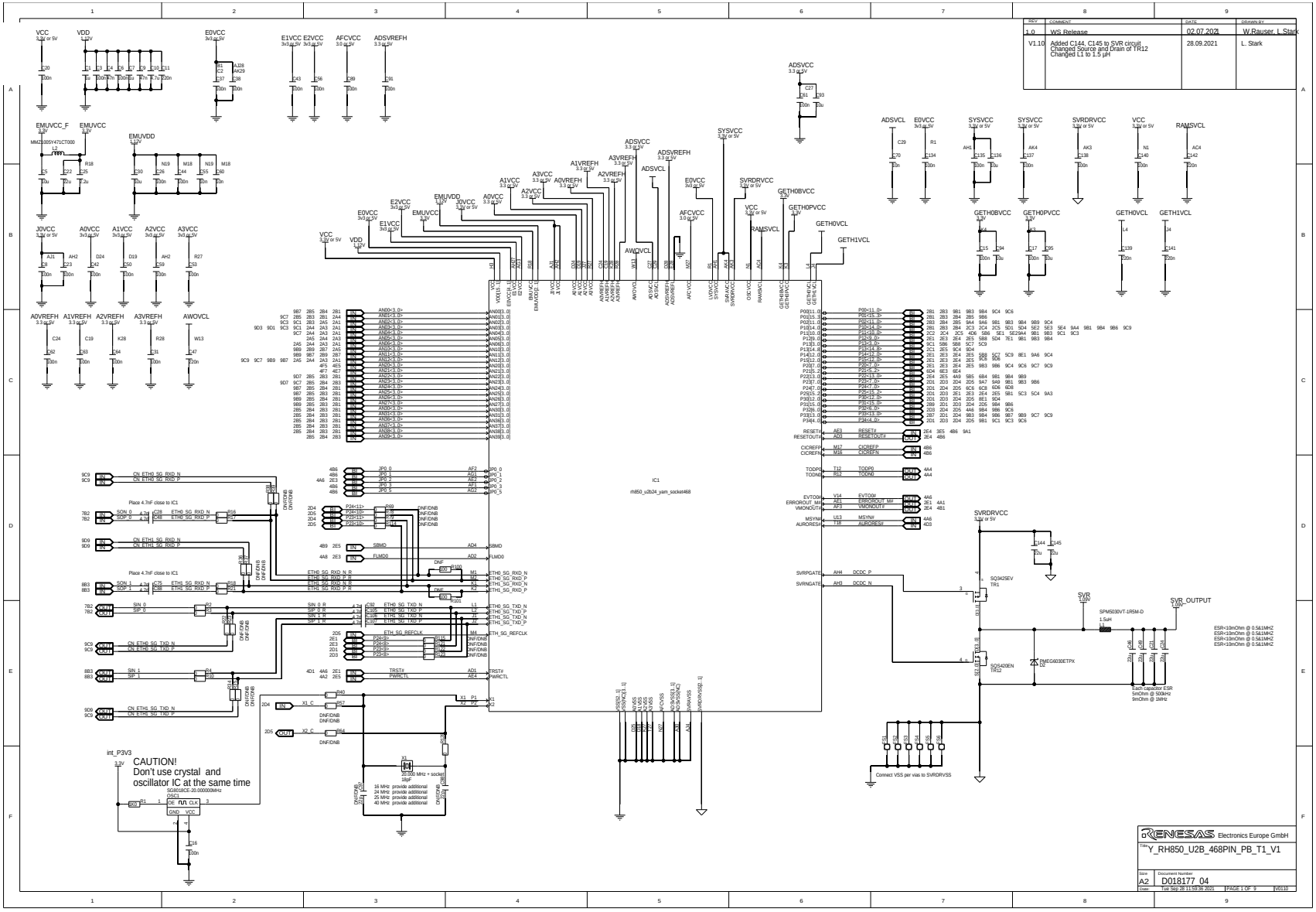
- 1 Hirschmann 4 mm power lab sockets, red for CN11
- Four resonators HC49 (16/24/25/40 MHz)
- 52 jumpers, 2.54 mm, black (for board version D018177_06_V01)
  47 jumpers, 2.54 mm, black (for board versions other than D018177_06_V01)
- Würth PCB Terminal Block connector (CN19, CN22)
- TE MATEnet 1000BASE-T1 Ethernet Port connector (CN17, CN18)
- 100 Ohm resistors for
  - R100, R101, R124, R162, R164, R167, R169, R170, R174-R177, R201, R204, R205
    (Board versions other than D018177_06_V01)

The above components are indicated with "DNF / TD " in the schematics.

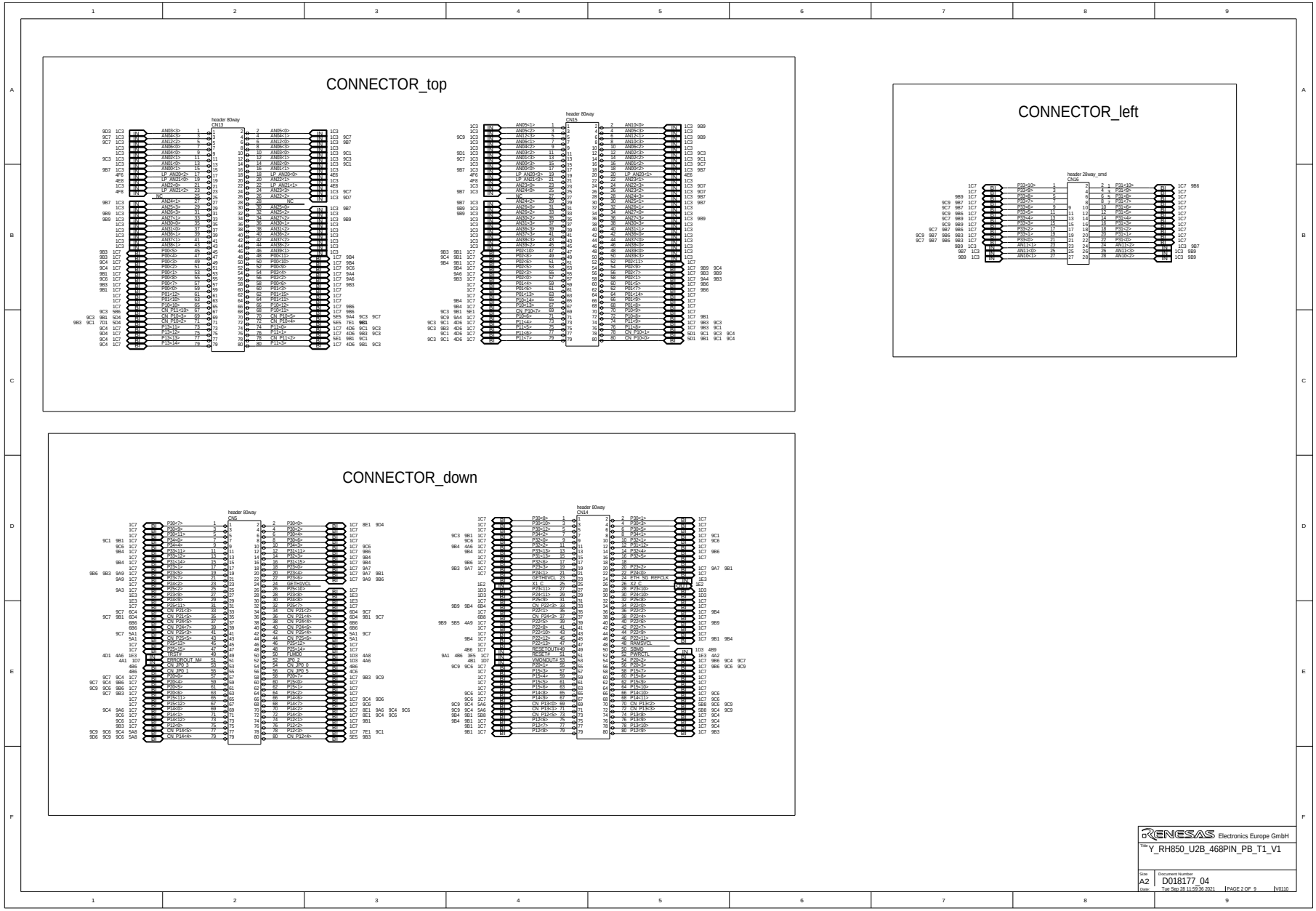
The resistors R83, R84, R86 and R87 (0 Ohm) are not provided with the board as their pads can be connected by a simple solder bridge.

11.1 Board version D018177_06_V01

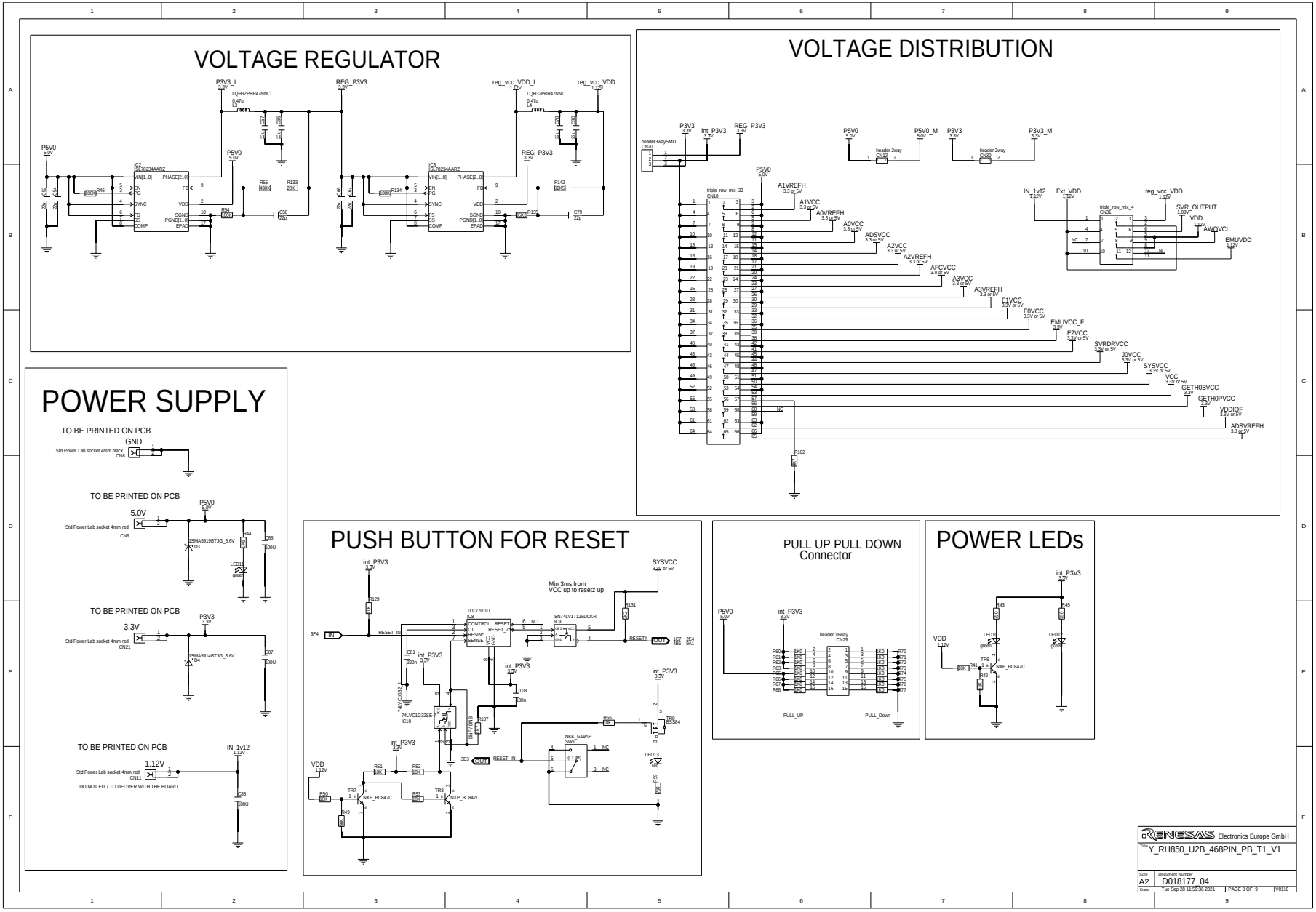
11.1.1 Page 1



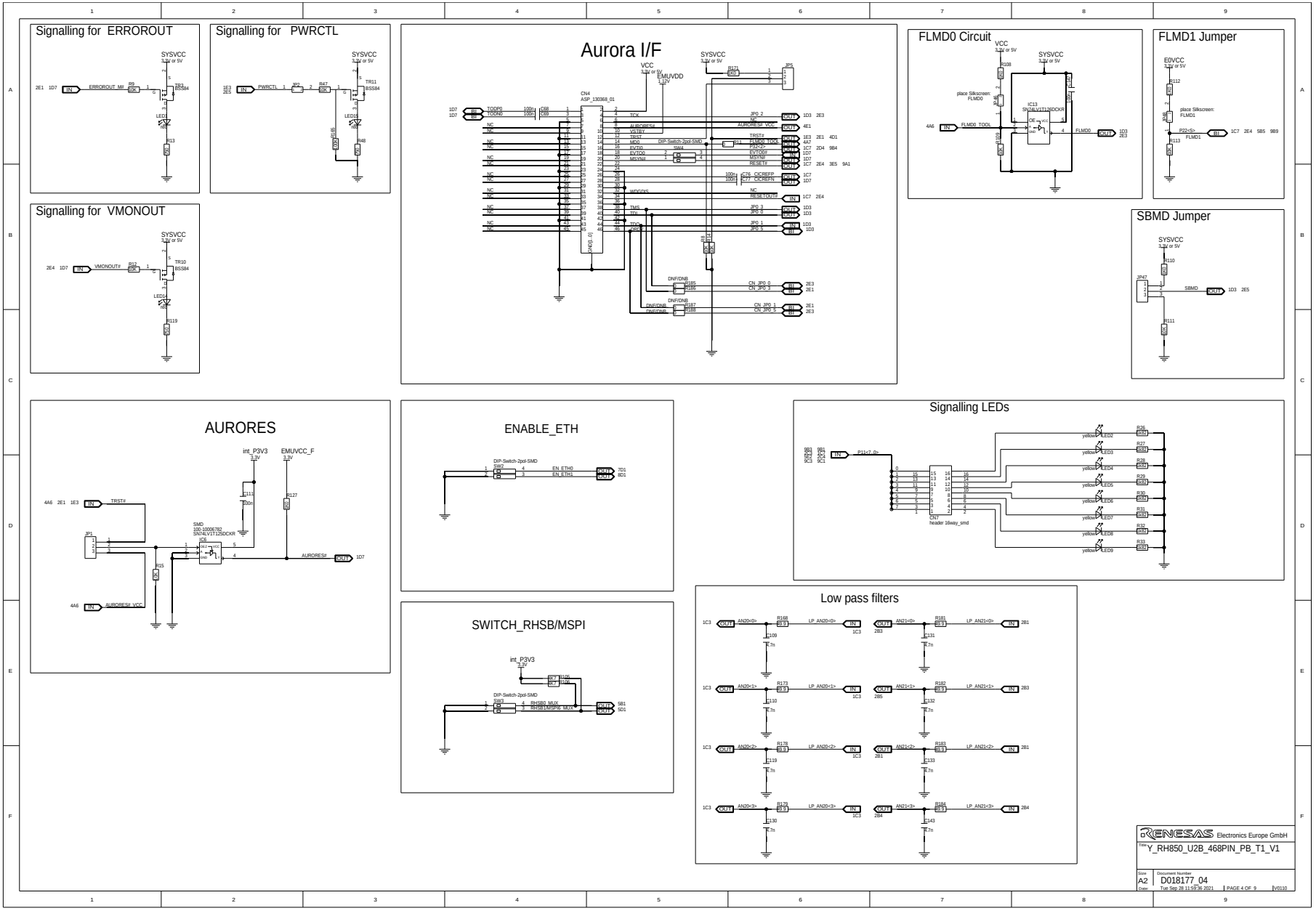
11.1.2 Page 2


CONNECTOR_top
CONNECTOR_left
CONNECTOR_down
RENESAS Electronics Europe GmbH
Title Y_RH850_U2B_468PIN_PB_T1_V1
Size A2
Document Number D018177_04
Date: Tue Sep 28 11:59:36 2021
PAGE 2 OF 9
V0110

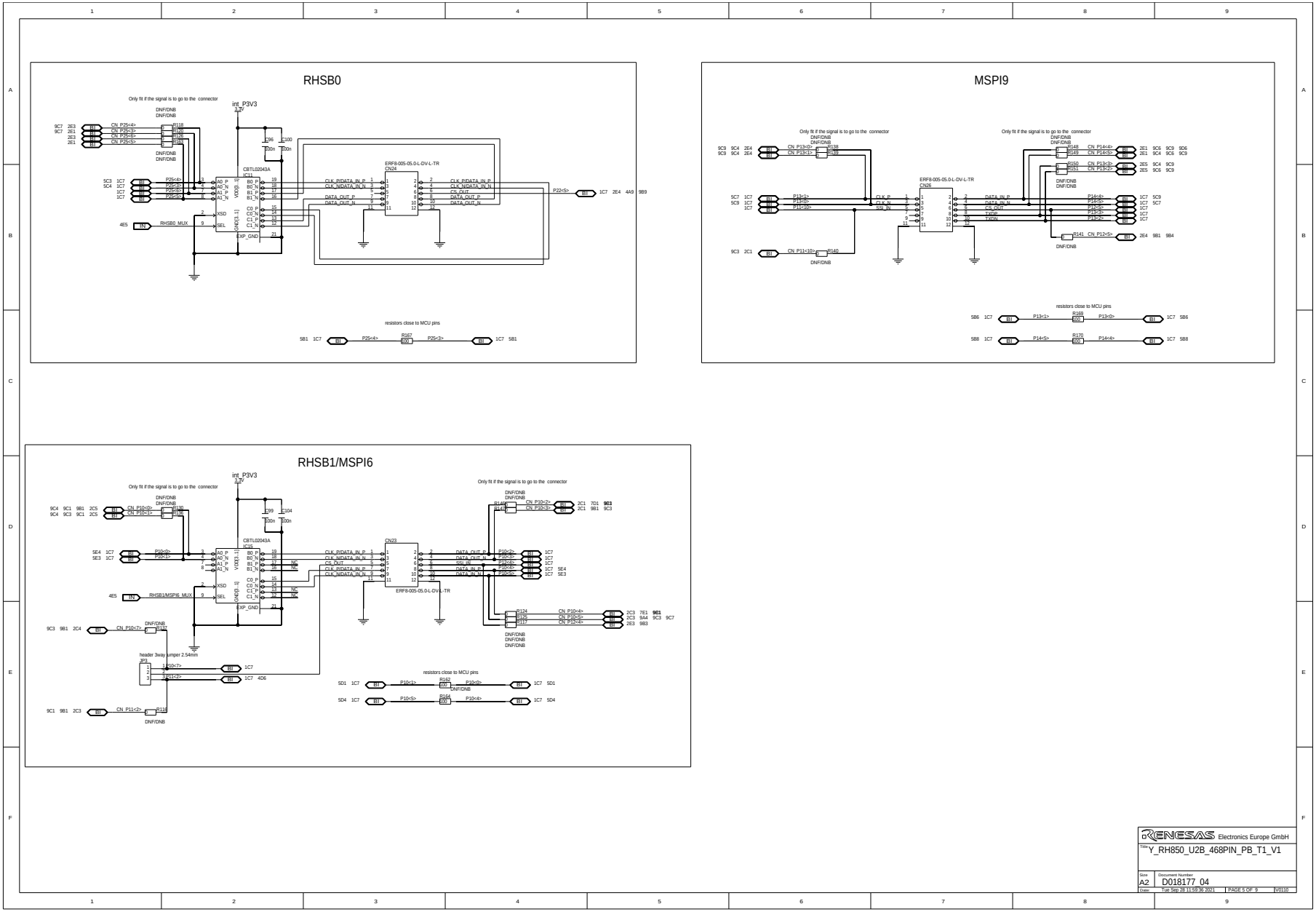
11.1.3 Page 3


VOLTAGE REGULATOR
VOLTAGE DISTRIBUTION
POWER SUPPLY
PUSH BUTTON FOR RESET
PULL UP PULL DOWN Connector
POWER LEDs
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

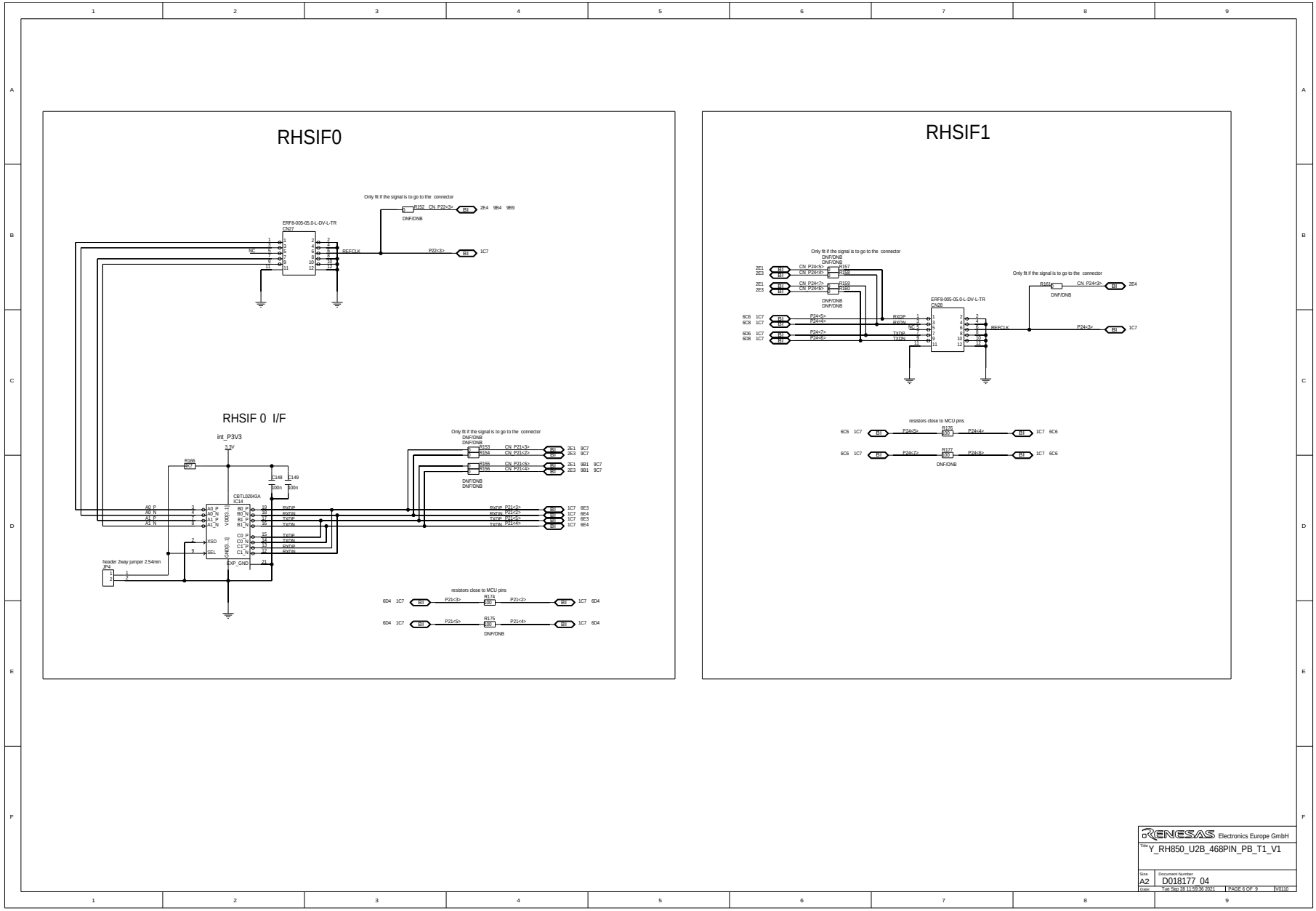
11.1.4 Page 4


Signalling for ERROROUT
Signalling for PWRCTL
Signalling for VMONOUT
Aurora I/F
FLMD0 Circuit
FLMD1 Jumper
SBMD Jumper
AURORES
ENABLE_ETH
SWITCH_RHSB/MSPI
Signalling LEDs
Low pass filters
RENESAS Electronics Europe GmbH
Title Y_RH850_U2B_468PIN_PB_T1_V1
Size A2
Document Number D018177_04
Date Tue Sep 28 11:59:36 2021
PAGE 4 OF 9
V0110

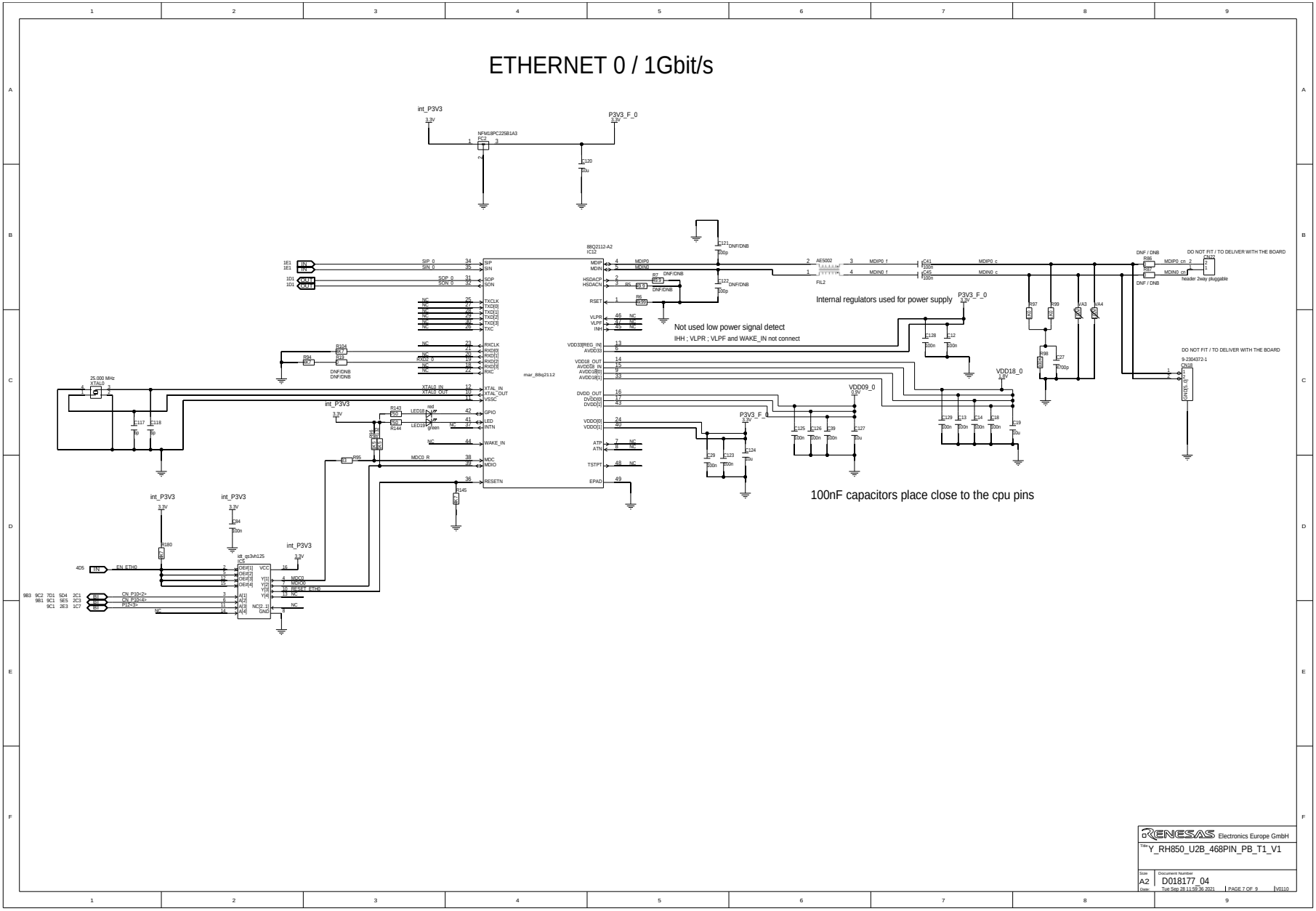
11.1.5 Page 5


RHSB0
MSPI9
RHSB1/MSPI6
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04
PAGE 5 OF 9

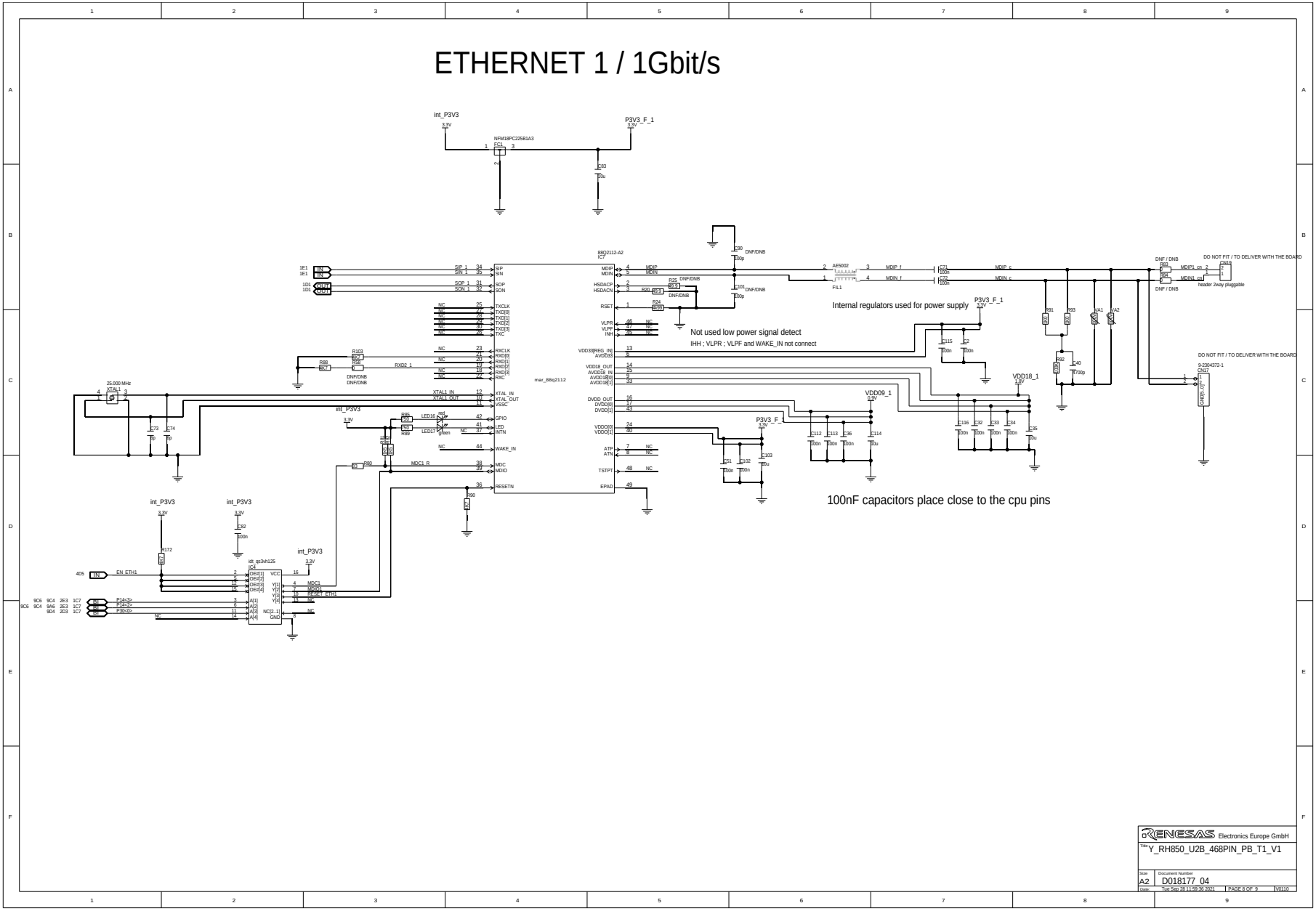
11.1.6 Page 6


RHSIF0
RHSIF 0 I/F
int_P3V3
CBTL02043A
IC14
ERF8-005-05.0-L-DV-L-TR
CN27
header 2way jumper 2.54mm
JP4
Only fit if the signal is go to the connector
DNF/DNB
resistors close to MCU pins
RHSIF1
ERF8-005-05.0-L-DV-L-TR
CN28
REFCLK
Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04
PAGE 6 OF 9

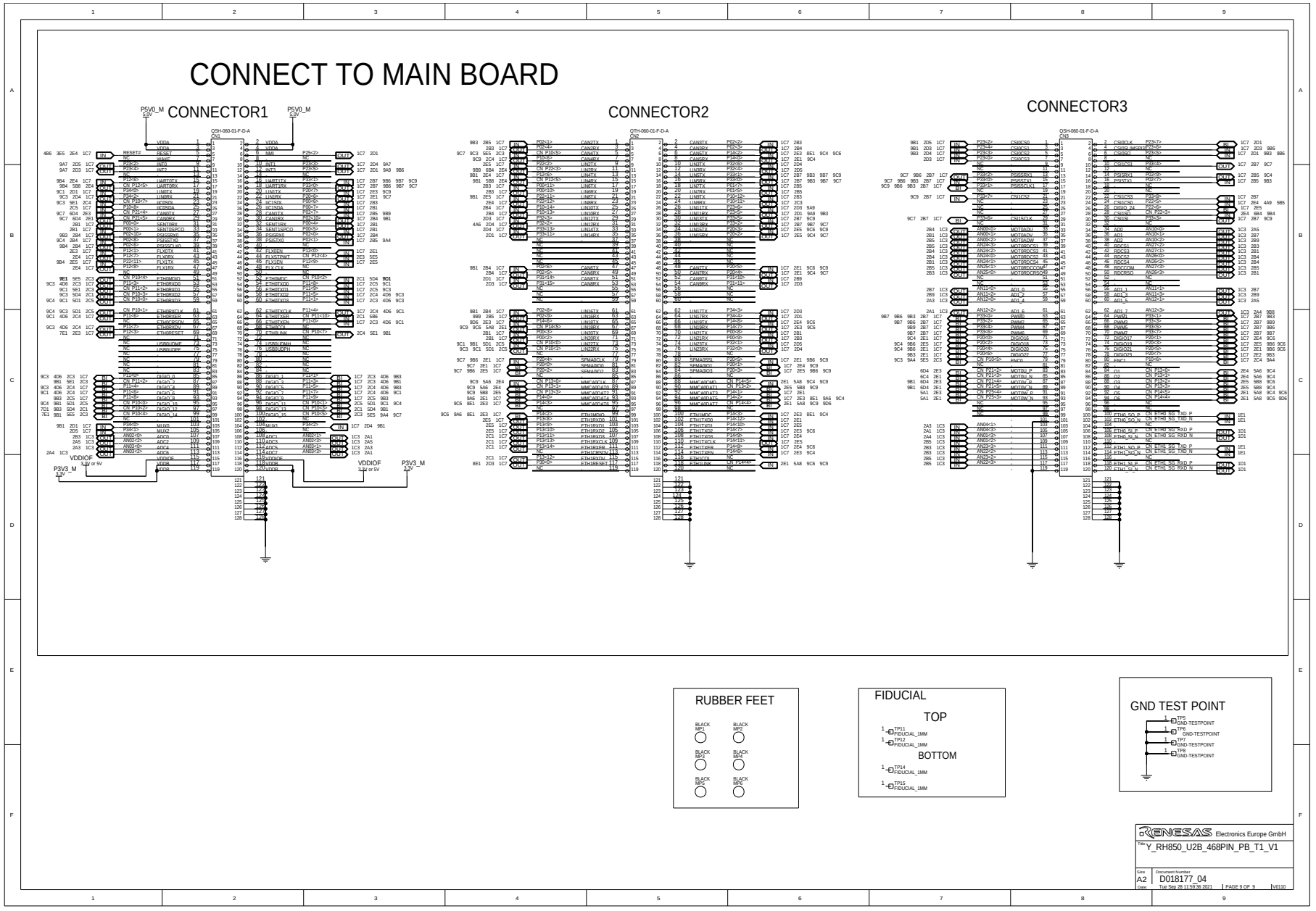
11.1.7 Page 7


ETHERNET 0 / 1Gbit/s
int_P3V3
P3V3_F_0
88Q2112-A2
IC12
Internal regulators used for power supply
Not used low power signal detect
IHH ; VLPR ; VLPF and WAKE_IN not connect
100nF capacitors place close to the cpu pins
DO NOT FIT / TO DELIVER WITH THE BOARD
header 2way pluggable
VDD18_0
VDD09_0
25.000 MHz
EN_ETH0
RESET_ETH0
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04
PAGE 7 OF 9

11.1.8 Page 8

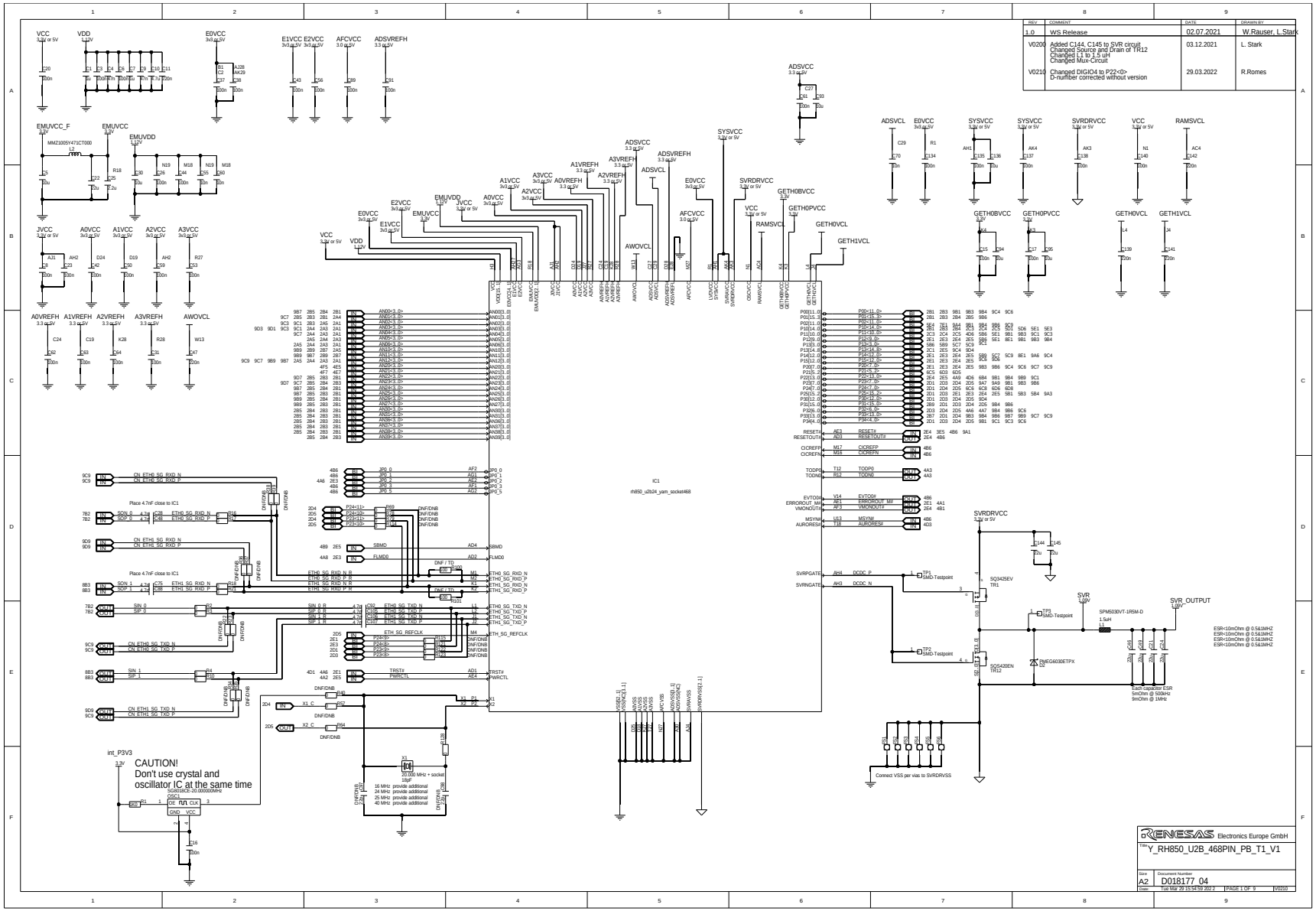

ETHERNET 1 / 1Gbit/s
int_P3V3
P3V3_F_1
NFM18PC225B1A3
8BQ2112-A2
IC7
mar_88q2112
AES002
FIL1
Internal regulators used for power supply
Not used low power signal detect
IHH ; VLPR ; VLPF and WAKE_IN not connect
100nF capacitors place close to the cpu pins
VDD09_1
VDD18_1
P3V3_F_2
DO NOT FIT / TO DELIVER WITH THE BOARD
header 2way pluggable
9-2304372-1
25.000 MHz
EN_ETH1
RESET_ETH1
idt_qs3vh125
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04
PAGE 8 OF 9
V0110

11.1.9 Page 9

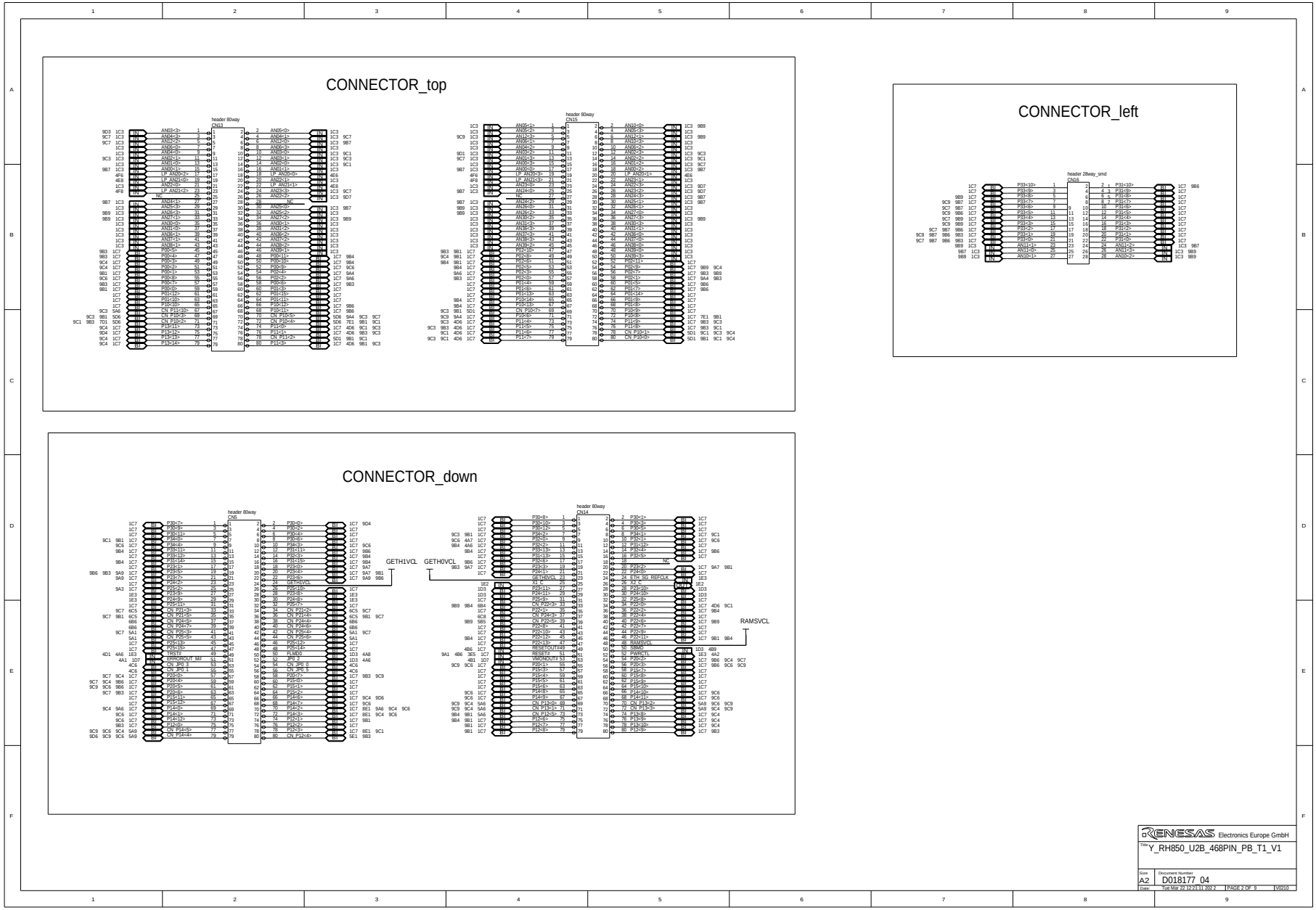

CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
RUBBER FEET
FIDUCIAL
TOP
BOTTOM
GND TEST POINT
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

11.2 Board version D018177_06_V02

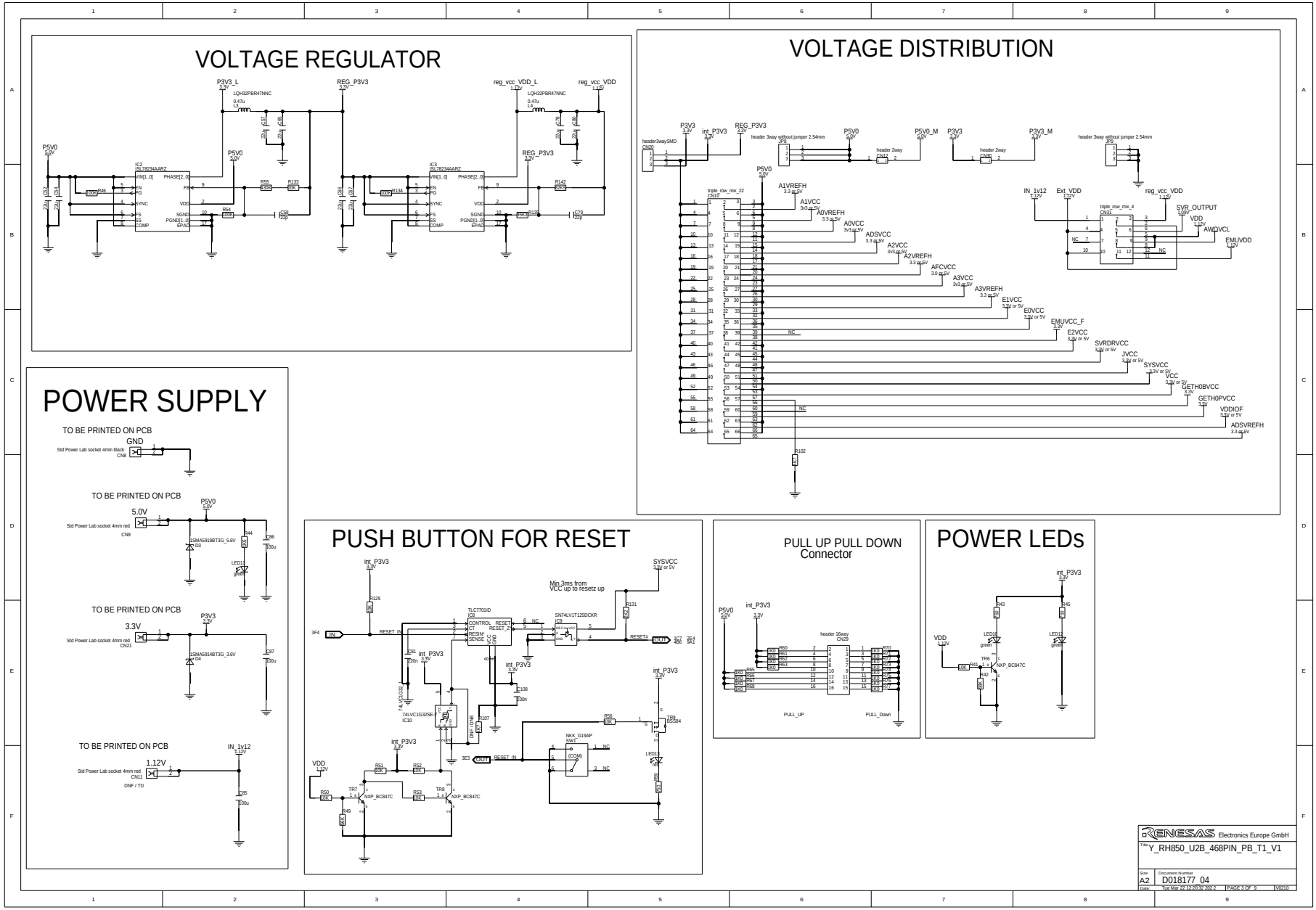
11.2.1 Page 1



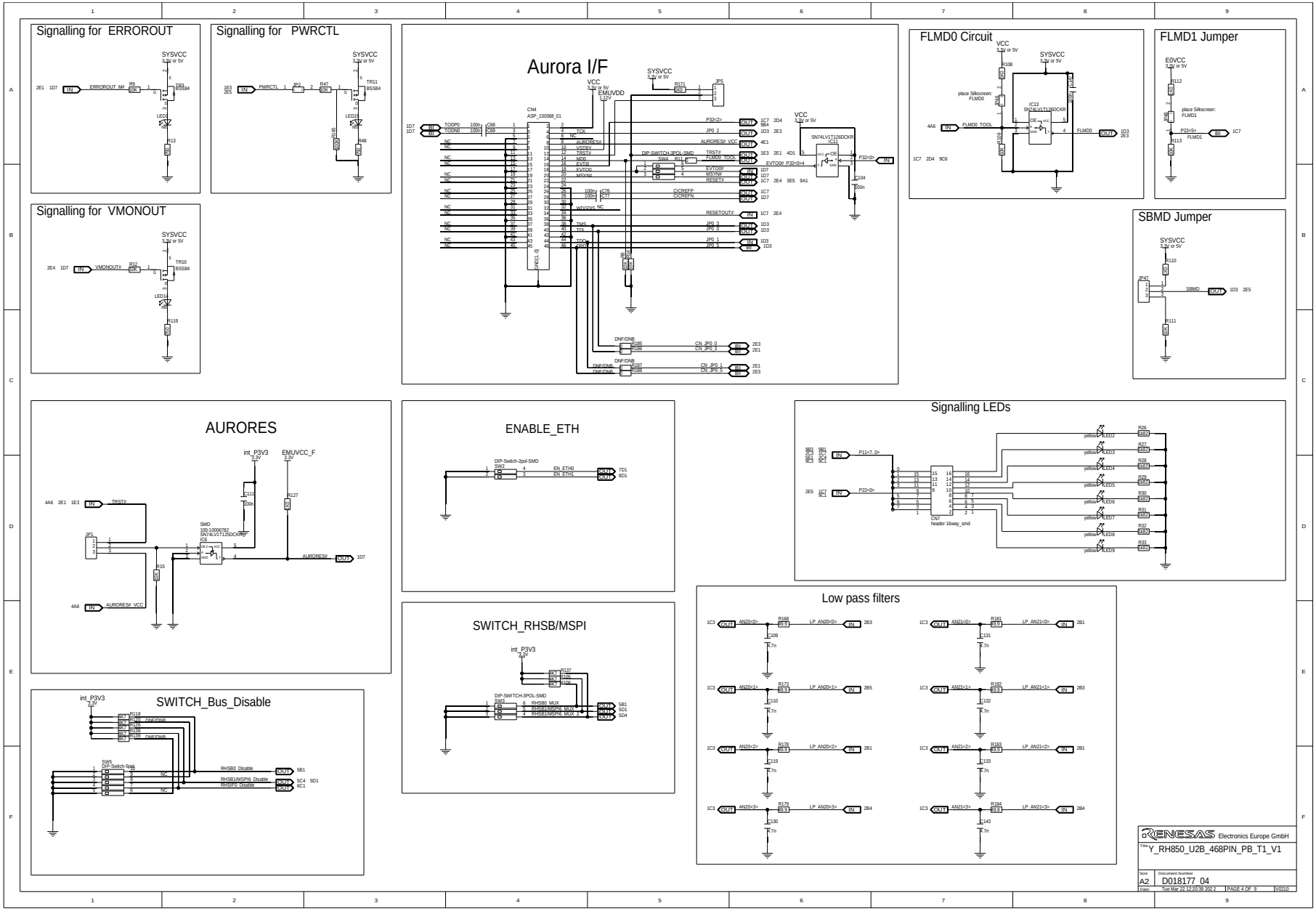
11.2.2 Page 2


CONNECTOR_top
CONNECTOR_left
CONNECTOR_down
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04
PAGE 2 OF 9

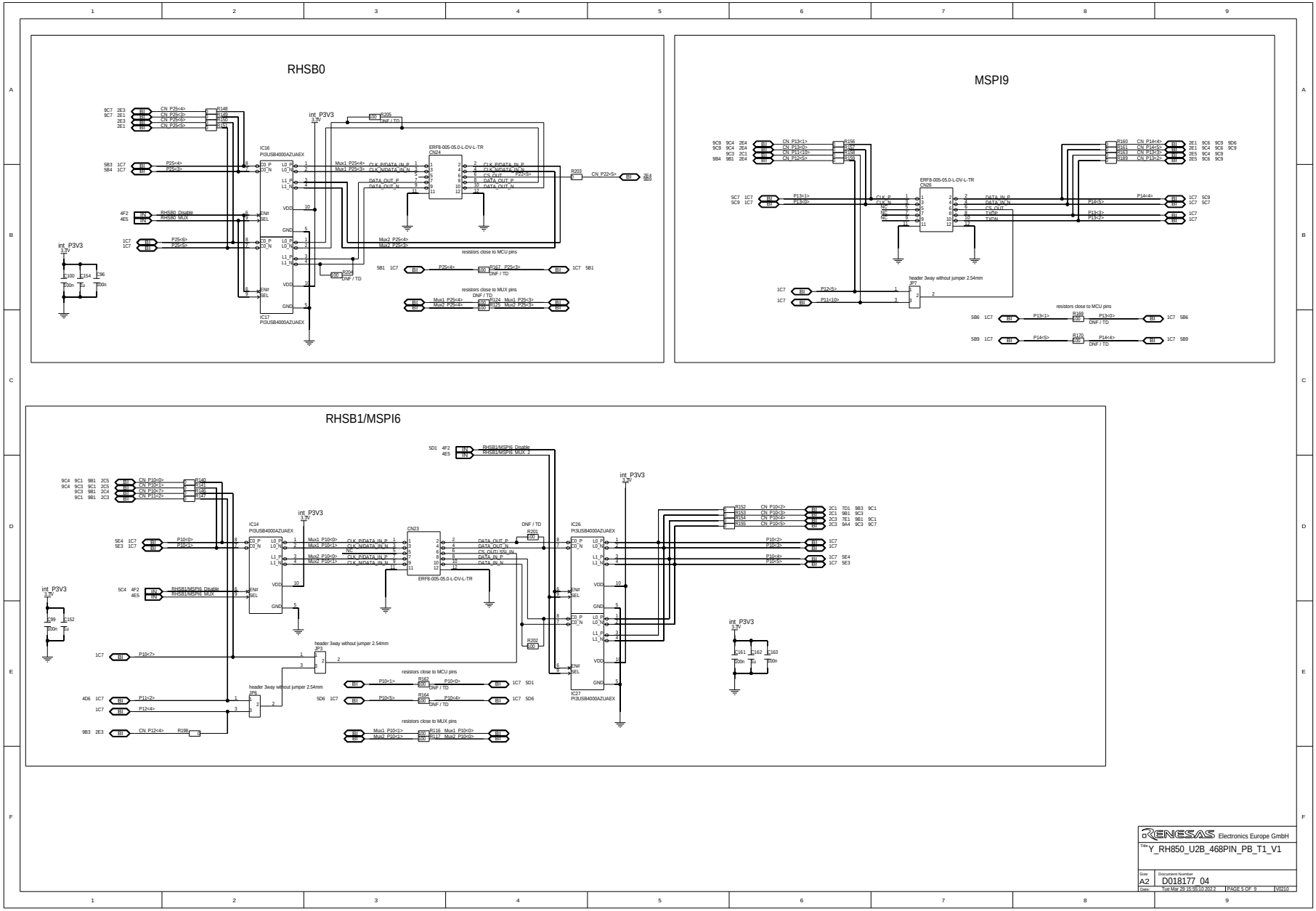
11.2.3 Page 3


VOLTAGE REGULATOR
VOLTAGE DISTRIBUTION
POWER SUPPLY
PUSH BUTTON FOR RESET
PULL UP PULL DOWN Connector
POWER LEDs
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

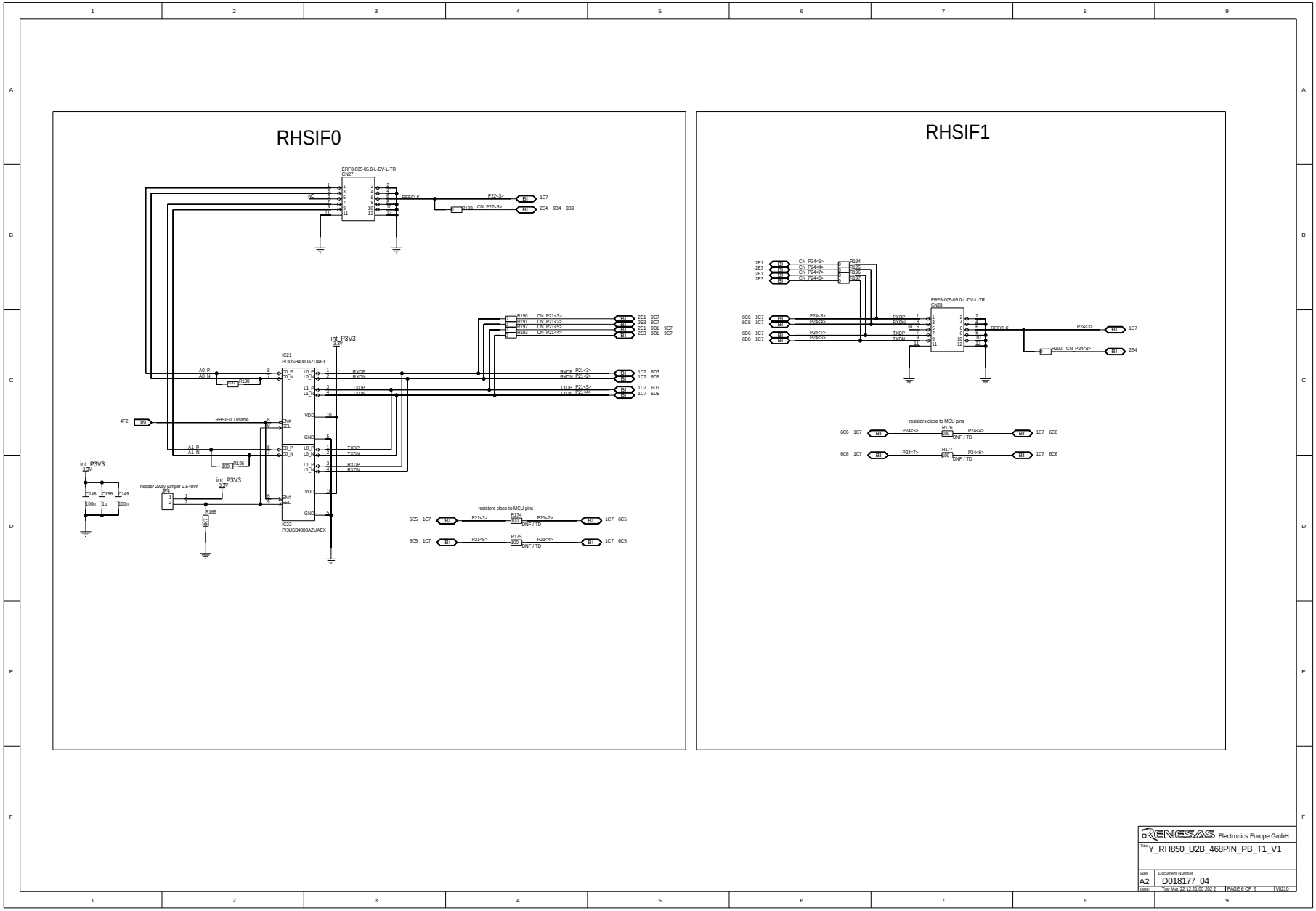
11.2.4 Page 4


Signalling for ERROROUT
Signalling for PWRCTL
Signalling for VMONOUT
Aurora I/F
FLMD0 Circuit
FLMD1 Jumper
SBMD Jumper
AURORES
ENABLE_ETH
SWITCH_RHSB/MSPI
SWITCH_Bus_Disable
Signalling LEDs
Low pass filters
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

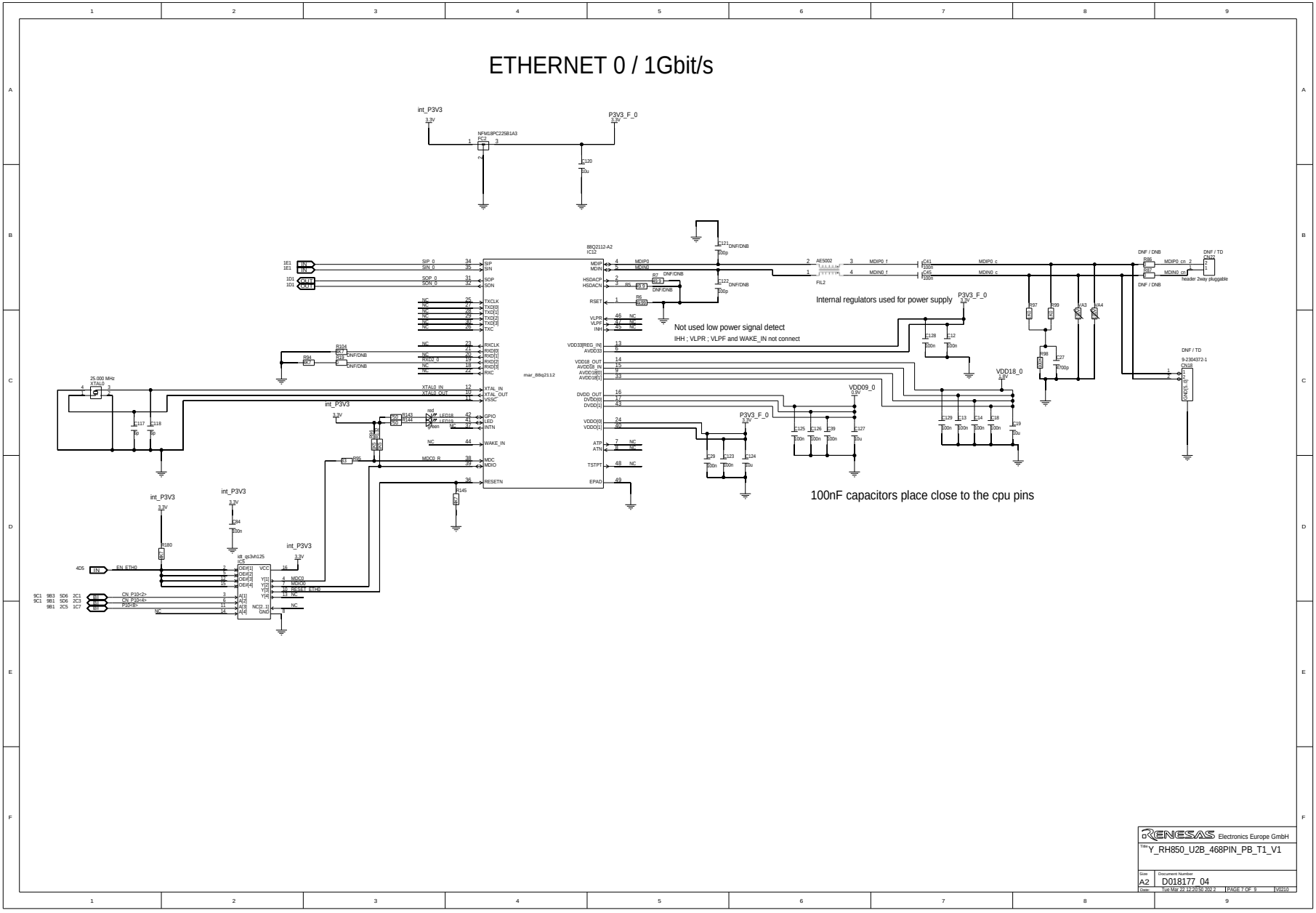
11.2.5 Page 5


RHSB0
MSPI9
RHSB1/MSPI6
int_P3V3
3.3V
resistors close to MCU pins
resistors close to MUX pins
header 3way without jumper 2.54mm
DNF / TD
RENESAS Electronics Europe GmbH
Title Y_RH850_U2B_468PIN_PB_T1_V1
Size A2
Document Number D018177_04
Date: Tue Mar 29 15:55:10 2022
PAGE 5 OF 9
V0210

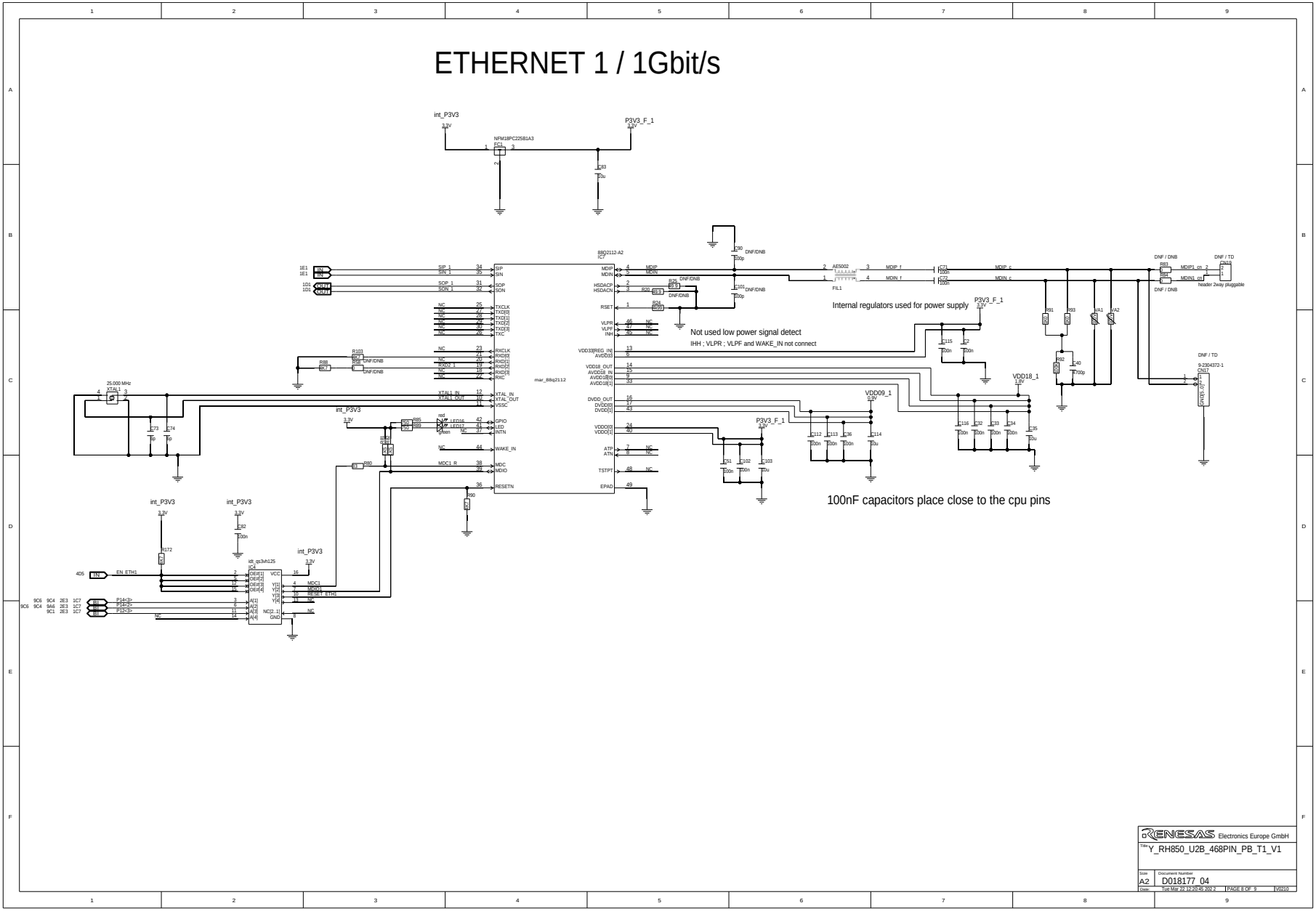
11.2.6 Page 6


RHSIF0
RHSIF1
ERF8-005-05.0-L-DV-L-TR
CN27
CN28
IC21
PI3USB4000AZUAEX
IC22
int_P3V3
3.3V
RHSIF0_Disable
header 2way jumper 2.54mm
resistors close to MCU pins
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

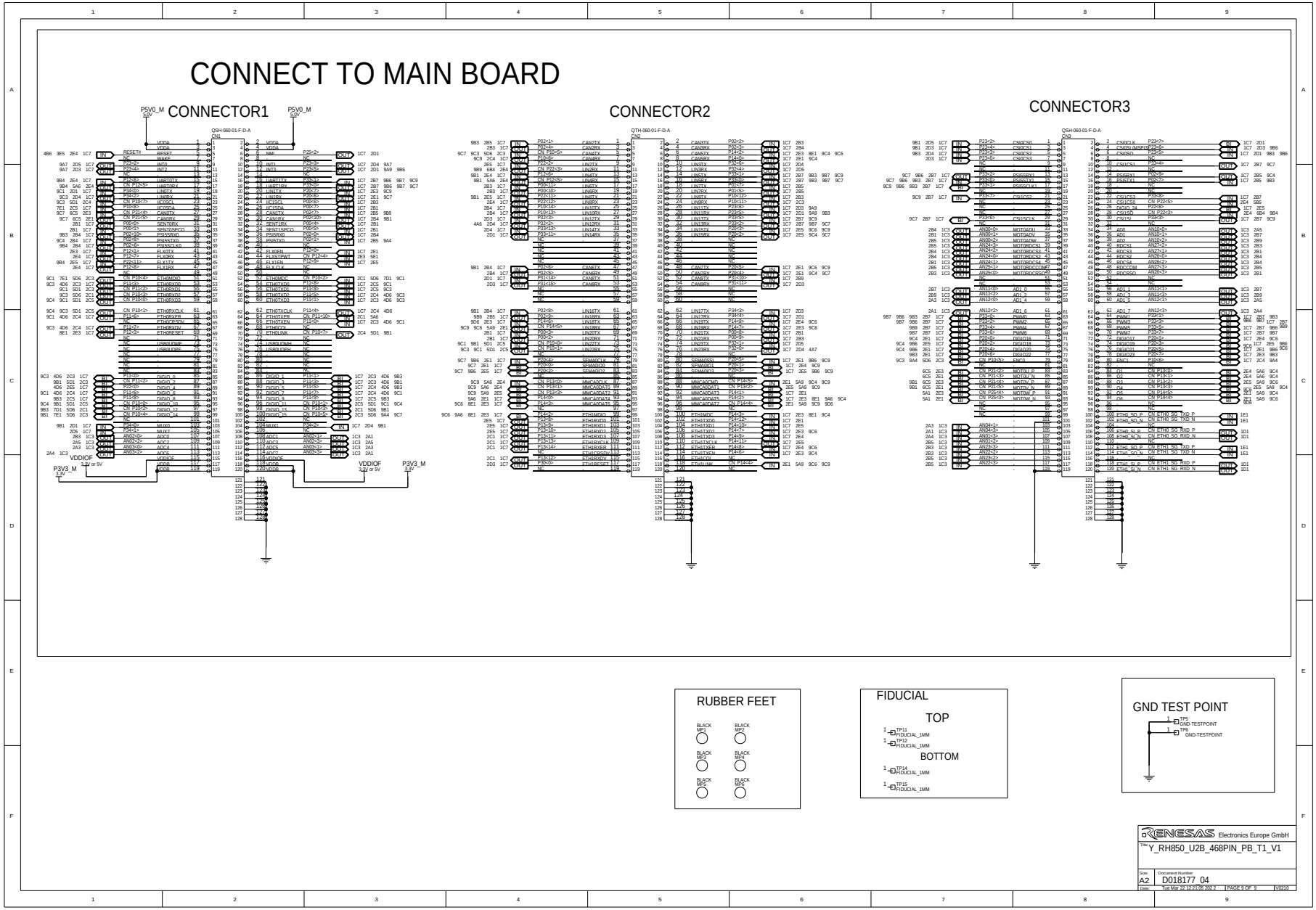
11.2.7 Page 7


ETHERNET 0 / 1Gbit/s
Not used low power signal detect
IHH ; VLPR ; VLPF and WAKE_IN not connect
Internal regulators used for power supply
100nF capacitors place close to the cpu pins
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

11.2.8 Page 8

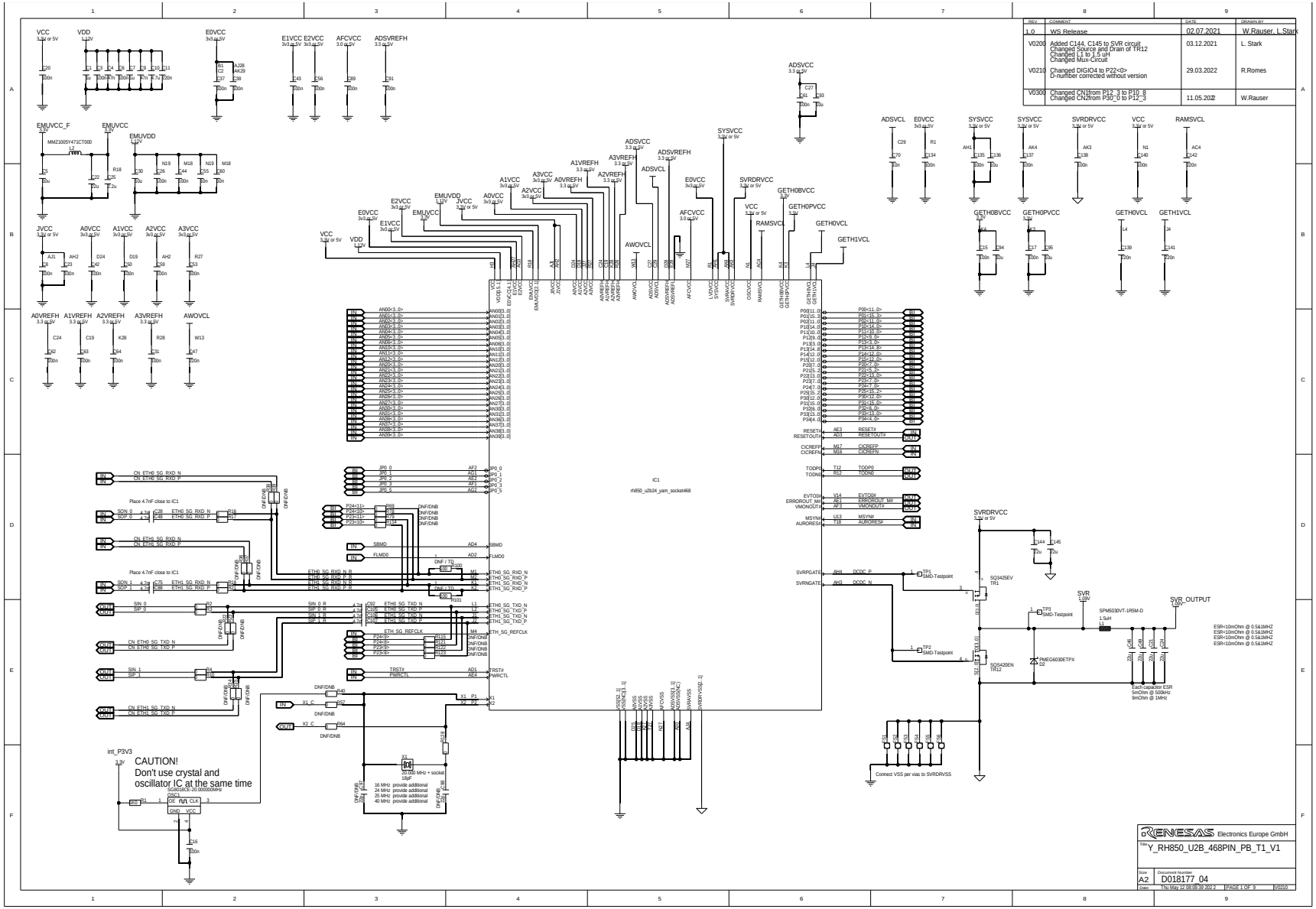

ETHERNET 1 / 1Gbit/s
int_P3V3
P3V3_F_1
NFM18PC225B1A3
Internal regulators used for power supply
Not used low power signal detect
IHH ; VLPR ; VLPF and WAKE_IN not connect
100nF capacitors place close to the cpu pins
VDD18_1
VDD09_1
25.000 MHz
EN_ETH1
RESET_ETH1
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

11.2.9 Page 9

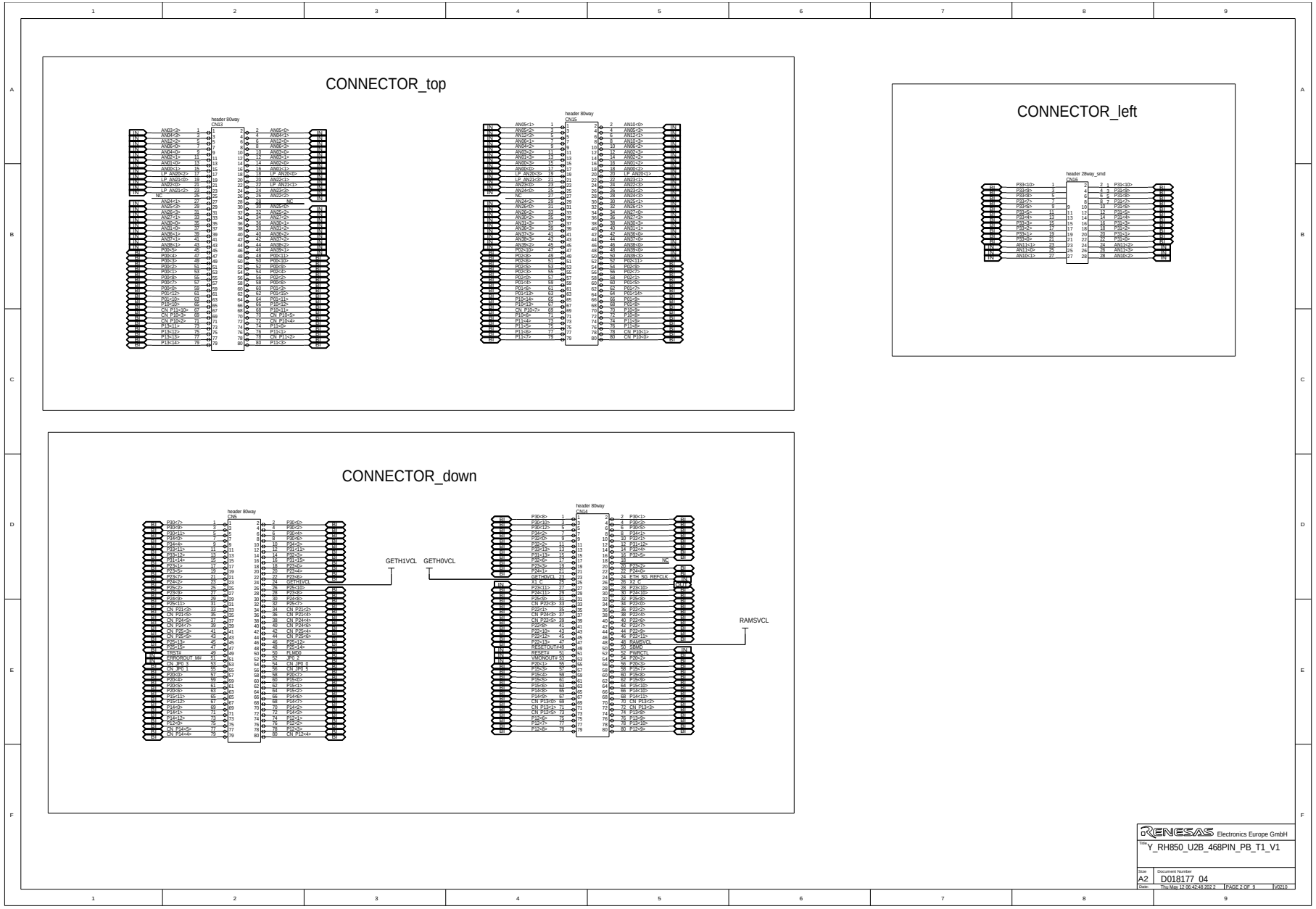

CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
RUBBER FEET
FIDUCIAL
TOP
BOTTOM
GND TEST POINT
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

11.3 Board version D018177_06_V03

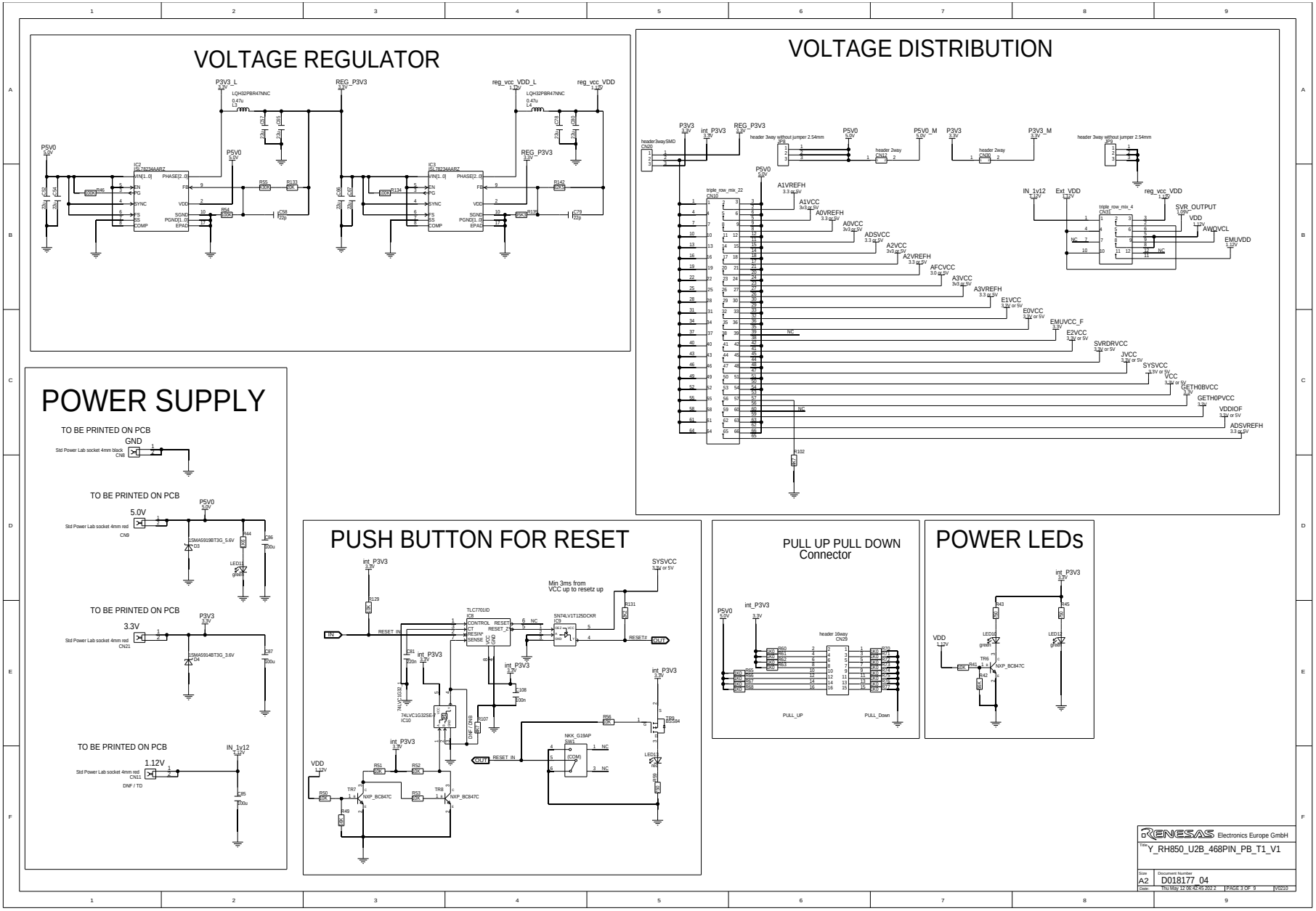
11.3.1 Page 1



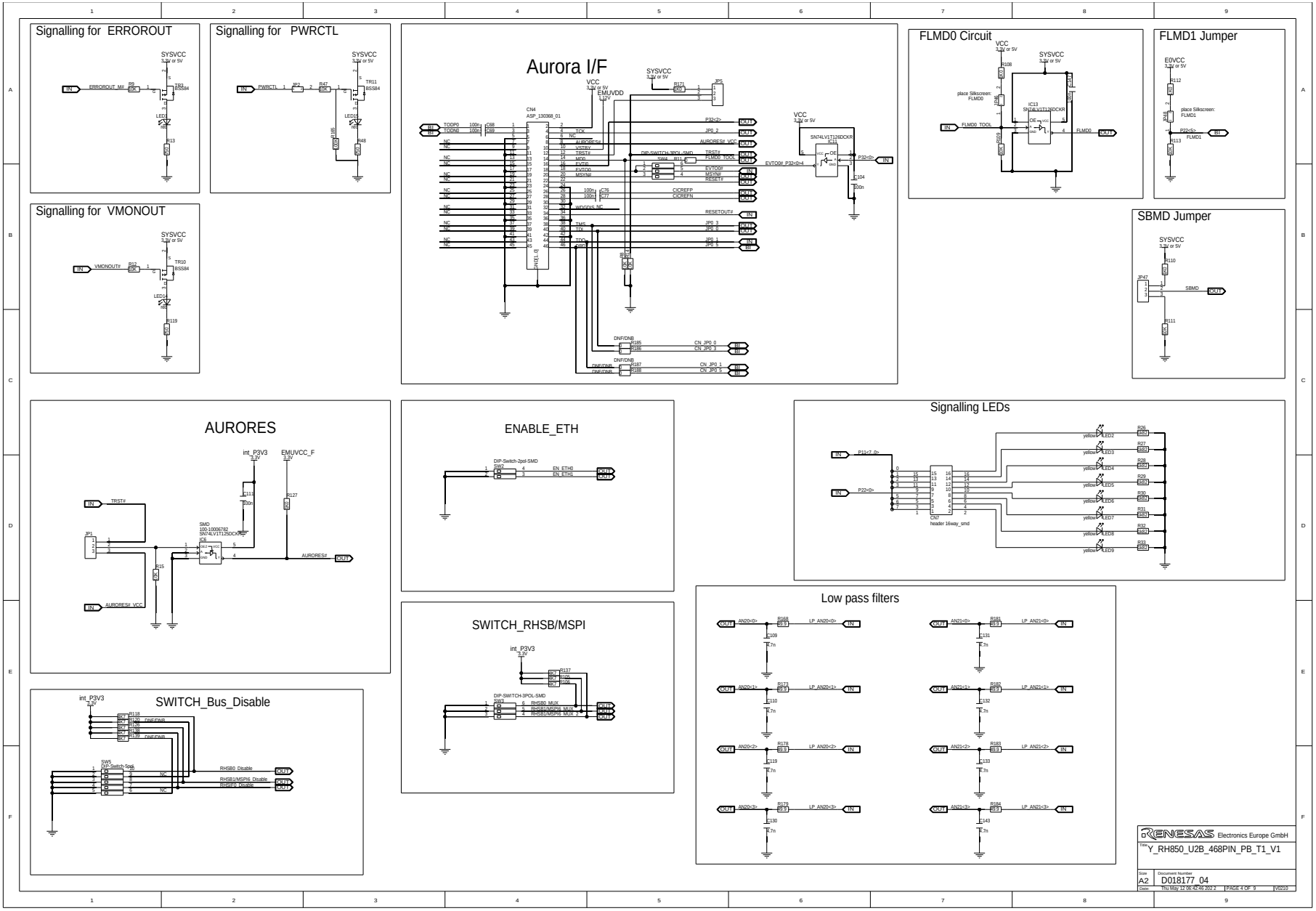
11.3.2 Page 2


CONNECTOR_top
CONNECTOR_left
CONNECTOR_down
GETH1VCL
GETH0VCL
RAMSVCL
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
A2
D018177_04

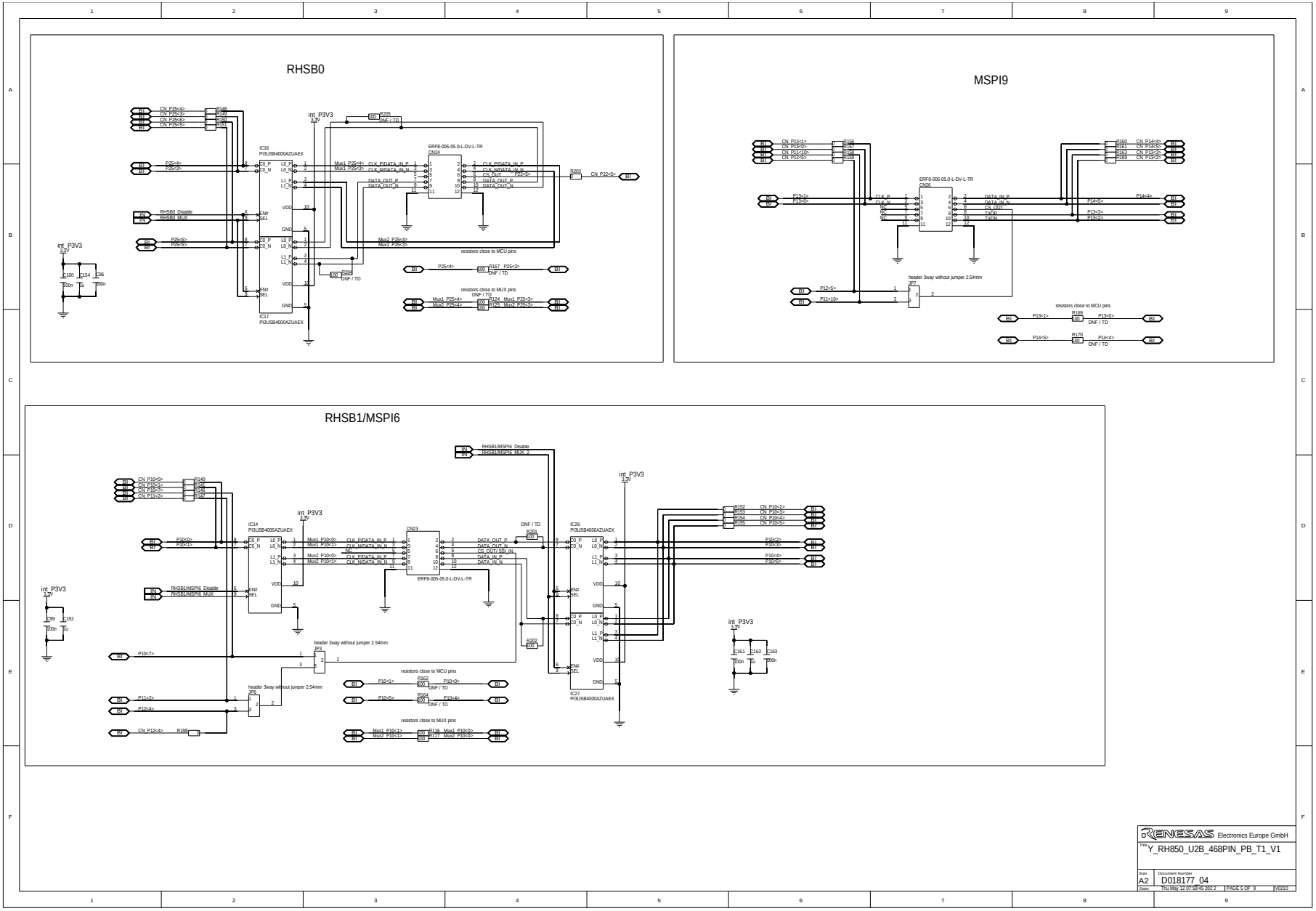
11.3.3 Page 3


VOLTAGE REGULATOR
VOLTAGE DISTRIBUTION
POWER SUPPLY
PUSH BUTTON FOR RESET
PULL UP PULL DOWN Connector
POWER LEDs
TO BE PRINTED ON PCB
GND
5.0V
3.3V
1.12V
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

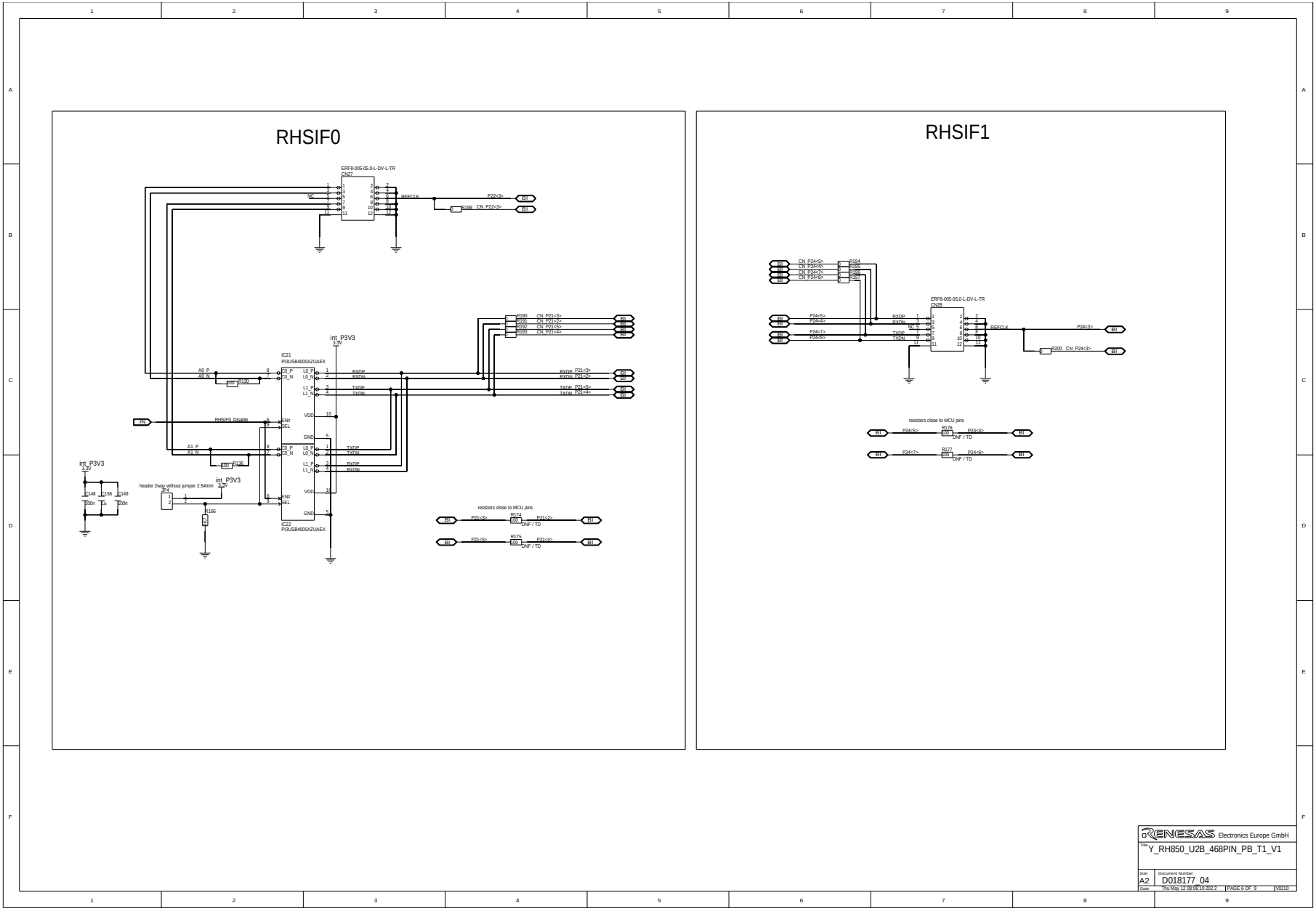
11.3.4 Page 4


Signalling for ERROROUT
Signalling for PWRCTL
Signalling for VMONOUT
Aurora I/F
FLMD0 Circuit
FLMD1 Jumper
SBMD Jumper
AURORES
ENABLE_ETH
SWITCH_RHSB/MSPI
SWITCH_Bus_Disable
Signalling LEDs
Low pass filters
Renesas Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

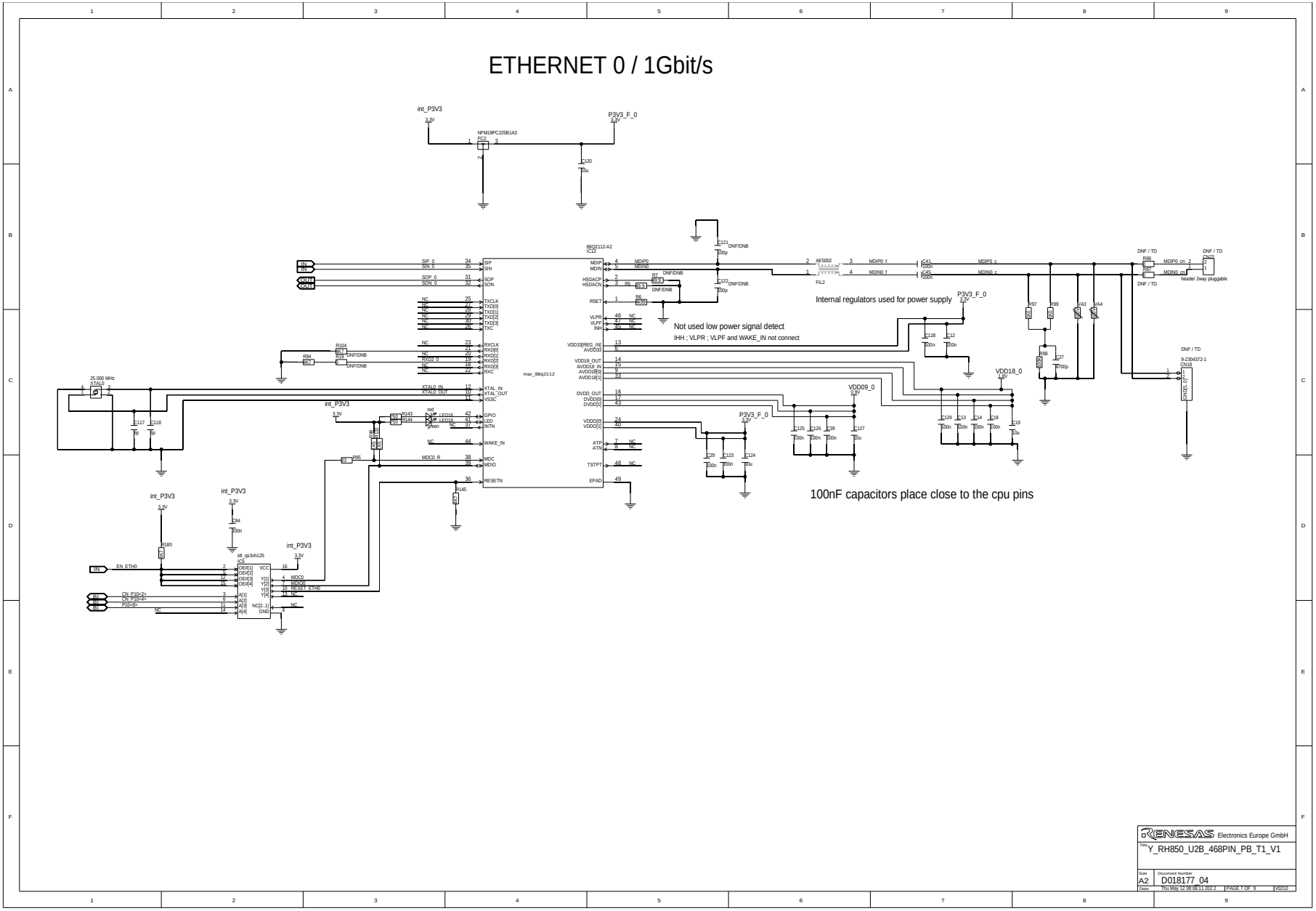
11.3.5 Page 5


RHSB0
MSPI9
RHSB1/MSPI6
int_P3V3
3.3V
IC16
PI3USB4000AZUAEX
IC17
PI3USB4000AZUAEX
ERF8-005-05.0-L-DV-L-TR
CN24
CN26
IC14
IC26
IC27
CN23
RHSB0_Disable
RHSB0_MUX
RHSB1/MSPI6_Disable
RHSB1/MSPI6_MUX
RHSB1/MSPI6_Disable
RHSB1/MSPI6_MUX_2
header 3way without jumper 2.54mm
resistors close to MCU pins
resistors close to MUX pins
DNF / TD
RENESAS Electronics Europe GmbH
Title
Y_RH850_U2B_468PIN_PB_T1_V1
Size
A2
Document Number
D018177_04
Date
Thu May 12 07:58:45 2022
PAGE 5 OF 9
V0210

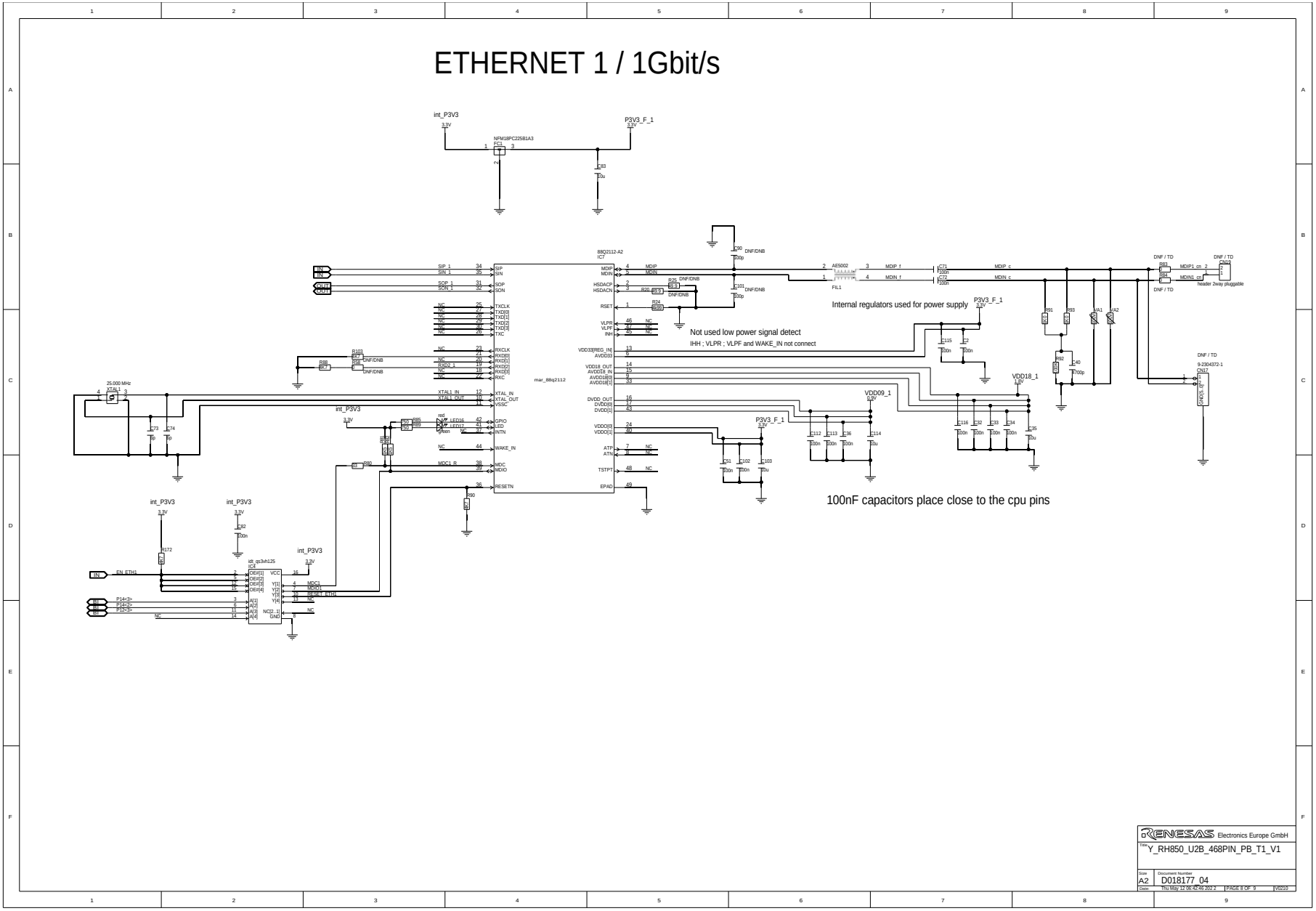
11.3.6 Page 6


RHSIF0
RHSIF1
ERF8-005-05.0-L-DV-L-TR
CN27
CN28
REFCLK
int_P3V3
3.3V
IC21
PI3USB4000AZUAEX
IC22
RHSIF0_Disable
header 2way without jumper 2.54mm
resistors close to MCU pins
DNF / TD
Y_RH850_U2B_468PIN_PB_T1_V1
RENESAS Electronics Europe GmbH
D018177_04

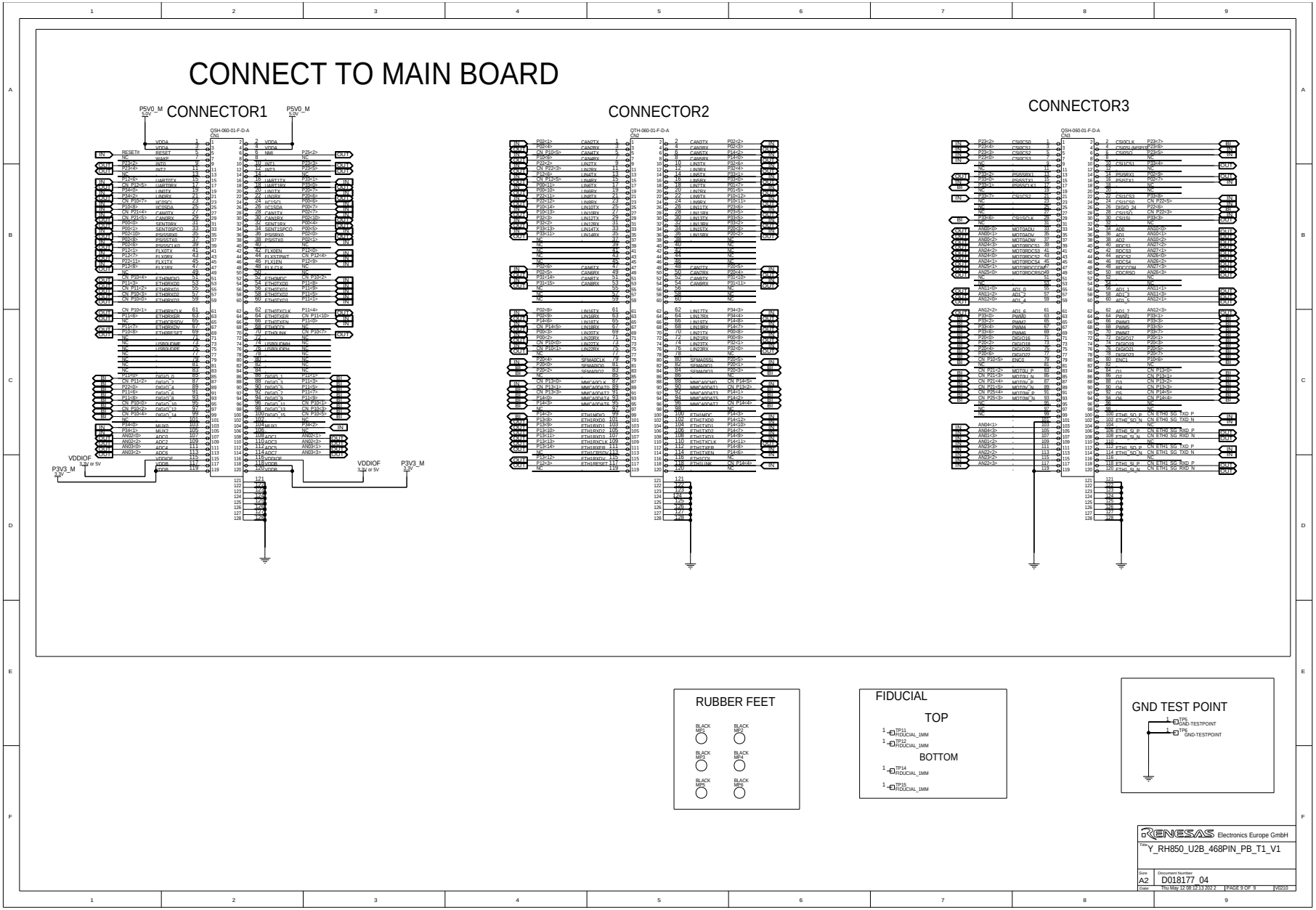
11.3.7 Page 7


ETHERNET 0 / 1Gbit/s
int_P3V3
P3V3_F_0
Internal regulators used for power supply
Not used low power signal detect
IHH ; VLPR ; VLPF and WAKE_IN not connect
100nF capacitors place close to the cpu pins
VDD18_0
VDD09_0
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

11.3.8 Page 8


ETHERNET 1 / 1Gbit/s
Internal regulators used for power supply
Not used low power signal detect
IHH ; VLPR ; VLPF and WAKE_IN not connect
100nF capacitors place close to the cpu pins
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

11.3.9 Page 9


CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
RUBBER FEET
FIDUCIAL
TOP
BOTTOM
GND TEST POINT
RENESAS Electronics Europe GmbH
Y_RH850_U2B_468PIN_PB_T1_V1
D018177_04

Revision History

Rev.	Date	Summary
V1.00	2021-11-30	Initial release
V1.01	2021-12-08	• Updated list of package components (*1.1 Package Components*). • Added description of GETH0BVCC and GETH0PVCC to *Table 3.1 Device power supply pins.* • Added description of connector CN16 (*7.3.5 Device Ports Connector CN16*).
V1.02	2021-12-09	• Corrected GETH0PVCC voltage in *Table 3.1 Device power supply pins* and *Figure 3.1 Voltage distribution.*
V2.00	2022-03-30	• Added information about available board versions. See chapter 1.1 for details. • Corrected references to J0VCC, J1VCC, JVCC (See chapters *3.2* and *8.2* for details).
V2.01	2022-04-07	• Added a precaution *9.4 Misprint at Switch SW5 on Board Marked D018177_06_V02*
V2.02	2022-05-03	• Added explanations about switch SW5 usage in chapters *6.5*, *0* and *6.8*
V2.03	2022-05-13	• Modified the jumper setting examples in chapter *8.3 Configuration Examples*
V3.00	2022-12-21	• The revised board D018177_06_V03 implemented the modifications, that were added to board version D018177_06_V02
V3.01	2023-03-31	• Corrected name of Ethernet interface in the feature list. *1.3 Main Features*
V3.02	2023-10-26	• Corrected jumper settings for GETH0BVCC and GETH0PVCC in chapters 8.3.4 – 8.3.6. *8.3.4Stand-Alone Operation with Single External Power Supply 5.0V: Minimum Configuration 2* *8.3.5Stand-Alone Operation with All External Power Supplies: Maximum Configuration* *8.3.6Operation on the Main Board: No External Supply* • Added precaution about power on of piggyback board without a microcontroller mounted. Caution in *3.1 Board Power Connection*. *9.6 Power On Piggyback Board Without RH850 Microcontroller installed*

RH850/U2B 468pin Piggyback Board V1 User's Manual: Piggyback Board

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Colophon 5.0

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