RTKA210030DR0000BU

The RTKA210030DR0000BU demonstration board (shown in Figure 2 and Figure 3) features the RTKA210030DR0000BU. Capable of delivering up to 3A of continuous current, the RAA210030 is a compact, synchronous step-down, non-isolated complete power supply that is optimized for space-constrained applications. The RTKA210030DR0000BU is based on a peak current mode PWM control scheme that provides a fast transient response and excellent loop stability. The switching frequency is programmable from 500kHz to 4MHz with either the external resistor or synchronization to an external clock through the SYNC pin.

The RTKA210030DR0000BU demonstration board is a 1×1 inch 4-layer FR4 board with 2oz. copper on external layers and 1oz. copper on internal layers. It is optimized to minimize the complete power module solution size. Operating from a single 2.7V to 5.5V input power rail, the RTKA210030DR0000BU demonstration board offers adjustable output voltages down to 0.6V, up to 95% efficiency, and better than ±1.5% accuracy over line, load, and temperature. A dedicated enable pin and power-good flag allow for easy system power rails sequencing.

By default, the board is set to a 1.8V output voltage with a 2MHz switching frequency.

Features

- Wide input voltage range from 2.7V to 5.5V
- Adjustable output voltage down to 0.6V with ±1.5% accuracy over line, load, and temperature
- Up to 95% conversion efficiency
- 100% duty cycle
- Internal 1ms soft-start time
- Pre-bias output start-up
- External frequency synchronization up to 4MHz
- Dedicated enable pin and PGOOD flag
- UVLO, overcurrent, negative overcurrent, overvoltage, and over-temperature protections

Specifications

The demonstration board is configured and optimized for the following operating conditions:

- V_{IN} = 2.7V to 5.5V
- V_{OUT} = 1.8V
- $I_{OUT-MAX}$ = 3A
- f_{SW} = 2MHz

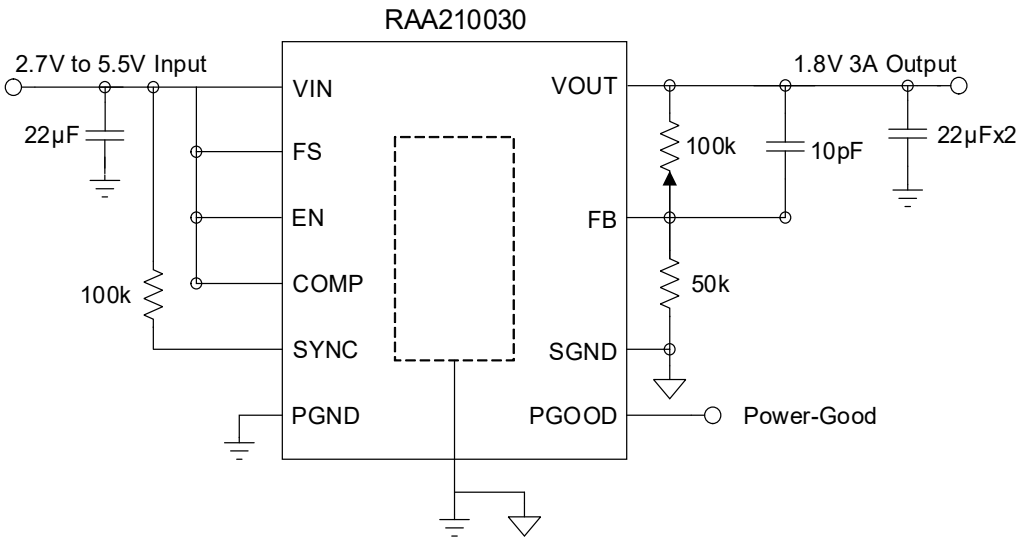

Figure 1. Block Diagram

Contents

1. Functional Description

The RTKA210030DR0000BU provides the peripheral circuitry to demonstrate the feature set of the RAA210030. The demonstration board includes several connectors that simplify the validation of the module. The module is enabled and disabled by moving the jumper across the J4.3-J4.6 as shown in Figure 2. Selecting features like external frequency synchronization is performed by removing the pull-up resistor R_3 of the SYNC pin and connecting the signal generator (square pulse waveform clock signal) to J3.2 of the SYNC pin. The output voltage (0.6V - 5V) and the switching frequency (500kHz to 4MHz) are programmed by changing the resistors as shown in Table 1.

Table 1. RTKA210030DR0000BU Design Guide Matrix (See Figure 7)

Case	V_{IN} (V)	V_{OUT} (V)	R_{10} (kΩ)	R_{11} (kΩ)	R_7 (kΩ)	R_8 (kΩ)	Freq (MHz)	R_1 (kΩ)	R_2 (kΩ)	C_8 (pF)	C_7 (pF)
1	3.3	0.6	0.1	Open	Open	33	1	Open	206	Open	680
2	3.3	0.8	33.2	100	Open	33	1.4	Open	143	Open	680
3	3.3	0.9	50	100	Open	33	1.5	Open	133	Open	680
4	3.3	1	66.5	100	Open	33	1.7	Open	115	Open	680
5	3.3	1.2	100	100	Open	33	2	0	Open	Open	680
6	3.3	1.5	100	66.5	0	Open	2	0	Open	10	Open
7	3.3	1.8	100	50	0	Open	2	0	Open	10	Open
8	3.3	2.5	100	31.6	0	Open	2	0	Open	Open	Open
9	5	1	66.5	100	Open	33	1	Open	206	Open	680
10	5	1.2	100	100	Open	33	1.4	Open	143	Open	680
11	5	1.5	100	66.5	0	Open	1.7	Open	115	10	Open
12	5	1.8	100	50	0	Open	2	0	Open	10	Open
13	5	2.5	100	31.6	0	Open	2	0	Open	Open	Open
14	5	3.3	100	22.1	0	Open	2	0	Open	Open	Open

1.1 Recommended Testing Equipment

- 0V to 5.5V power supply with at least 3A source current capability
- Electronic loads capable of sinking current up to 3A
- Digital Multimeters (DMMs)
- Oscilloscope with higher than 100MHz bandwidth

1.2 Quick Test Guide

1. Disable the module by connecting the jumper across 3 and 4 on J4 for the EN pin as shown in Figure 2 and Figure 7.
2. Use the appropriate cables to connect the DC input power supply to banana sockets J1.1-2 and J1.5-6 and the electronic load to sockets J2.5-6 and J2.1-2. Ensure that the polarity for the power leads is correct and the input voltage is within the operating range (2.7V - 5.5V) of the module. Use test points J3.6 (VIN) and J3.5 (PGND) for accurately measuring the input voltage.
3. Turn on the input power supply.
4. To enable the module, you can connect the jumper across 5 and 6 on J4 for the EN pin to enable the module.

5. To enable external frequency synchronization, remove the pull-up resistor R_3 of the SYNC pin and connect the external clock to J3.2 (SYNC). To ensure proper operation, Renesas recommends that the external SYNC frequency is within ±25% of the switching frequency set by R_2 at the FS pin.
6. Probe test points J4.1 (VOUT) and J4.2 (PGND) to observe the output voltage. The output voltage should read 1.8V.
7. Adjust the input voltage, V_{IN}, within the specified range and observe the output voltage. The output voltage variation should be within ±1.5%.
8. Adjust the load current to within the specified range (0 - 3A) and observe the output voltage. The output voltage variation should be within ±1.5%.
9. To change V_{OUT}, disconnect the demonstration board from the setup and populate standard 0402 resistors at the R_{10} and R_{11} locations on the top layer. The Output Voltage Resistor Settings table in the *RAA210030 Datasheet* can be used as a reference for programming different output voltages. See the RTKA210030DR0000BU Design Guide Matrix table in Table 1 for correct input and output capacitors, switching frequency, and output voltage combinations.
10. The switching frequency is modified by removing pull-up resistor R_1 and populating a standard 0402 resistor at the R_2 location on the top layer. See Equation 1 in the *RAA210030 Datasheet* for selecting the correct value of R_2 within the admissible operating range (500kHz - 4MHz).

1.3 Thermal Considerations and Current Derating

To ensure the module can operate safely and deliver the maximum allowable power, the board layout is critical. For the board to operate properly at high ambient temperature environments and carry full load current, carefully design the board layout to maximize thermal performance. To achieve this, use enough trace width, copper weight, and proper connectors.

The RTKA210030DR0000BU demonstration board is capable of operating at 3A full-load current at room temperature without the need for additional cooling systems. However, if the board needs to operate at elevated ambient temperatures, the available output current may need to be derated. See the derated current curves in the *RAA210030 Datasheet* to determine the maximum output current that the module can supply.

2. Board Design

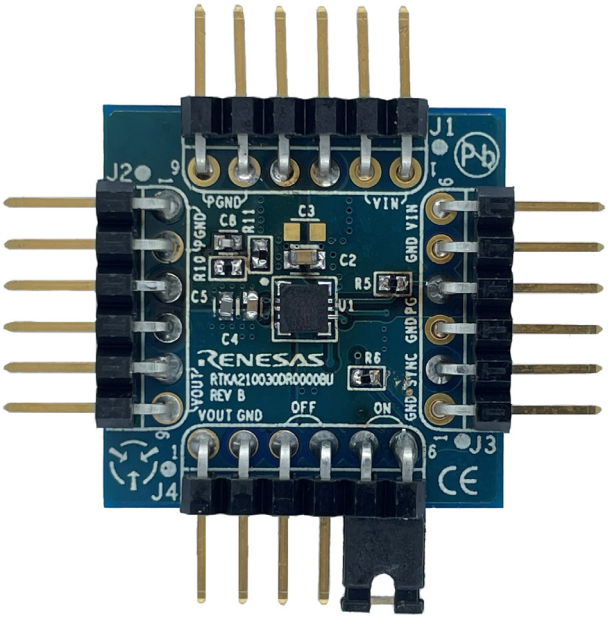

Figure 2. RTKA210030DR0000BU Evaluation Board (Top)

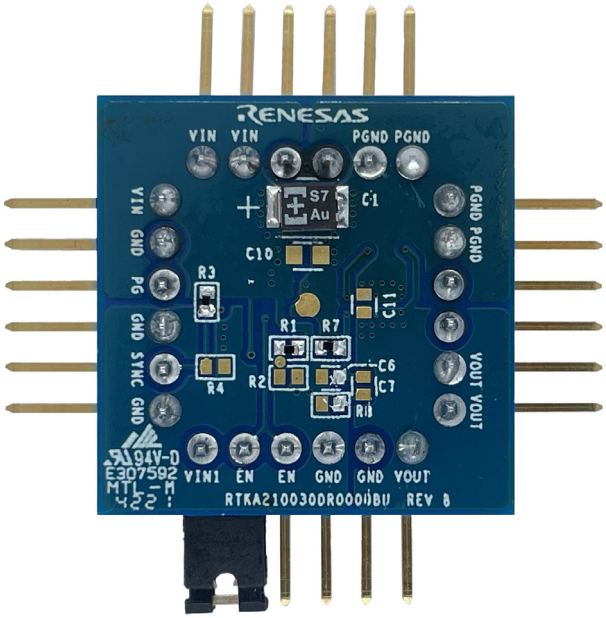

Figure 3. RTKA210030DR0000BU Evaluation Board (Bottom)

2.1 Layout Guidelines

The RTKA210030DR0000BU demonstration board is a 1x1 inch four-layer FR-4 board with 2oz copper on external layers and 1oz copper on internal layers. The board can be used as a single 3A reference design. See Figure 8 through Figure 13 for board layout information.

The RTKA210030DR0000BU board layout is optimized for compact complete power module solution size, good electrical and thermal performance. For similar performance in designs involving RTKA210030DR0000BU, follow these layout design tips.

2.1.1 Layout Considerations

- Place the input ceramic capacitors as close as possible to the module input. These ceramic capacitors minimize the high frequency noise by reducing the parasitic inductance of the power loop. Proper placement of these capacitors not only leads to less PHASE node spikes and ringing, but also minimizes the switching noise coupled to the module. Renesas recommends using dielectric X5R or better with a minimum total capacitance of 22µF at the module input. A layout example is shown in Figure 4 and Figure 5.
- Use large copper planes to minimize conduction loss and thermal stress for VIN, VOUT, and PGND. Use multiple vias to connect the power planes in different layers.
- Use a separate SGND plane for components that are connected to SGND. Connect SGND and PGND at a single point on the top layer as shown in Figure 6.
- Use a remote-sensing trace to connect to the point-of-load and achieve tight output voltage regulation. Route the remote-sensing trace underneath the PGND layer and avoid routing it near noisy planes. Place an optional 2Ω resistor close to the output voltage resistor divider and FB pin to damp the noise on the trace.

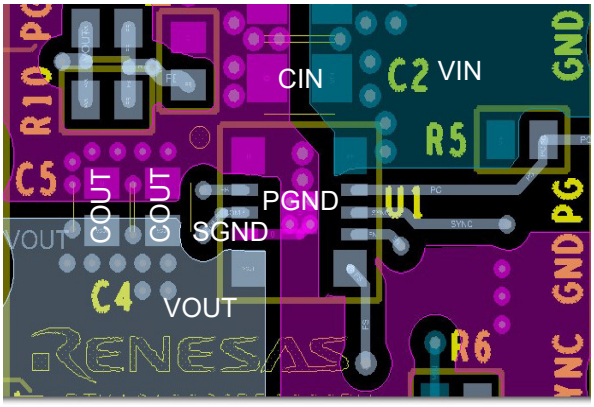

Figure 4. Layout Example - Top Layer

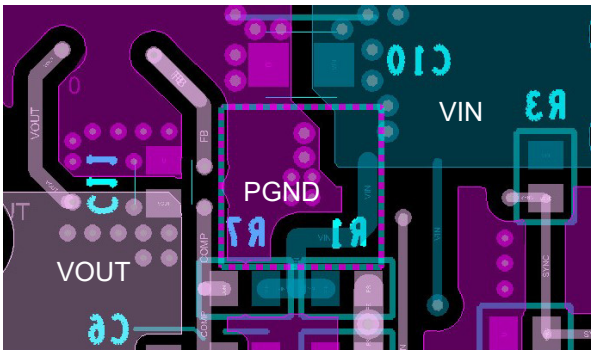

Figure 5. Layout Example - Bottom Layer

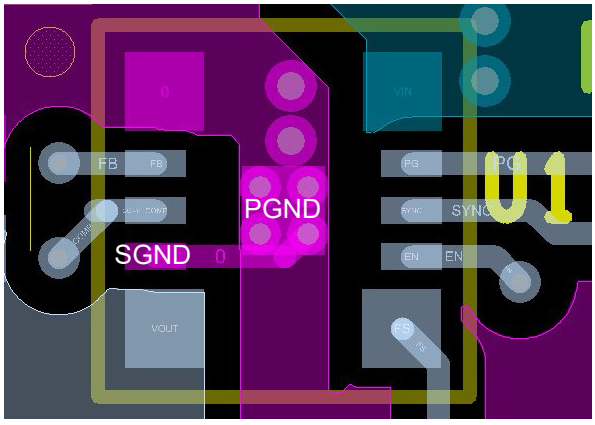

Figure 6. Layout Example - SGND is Connected to PGND at Single Point

2.2 Schematic Diagrams

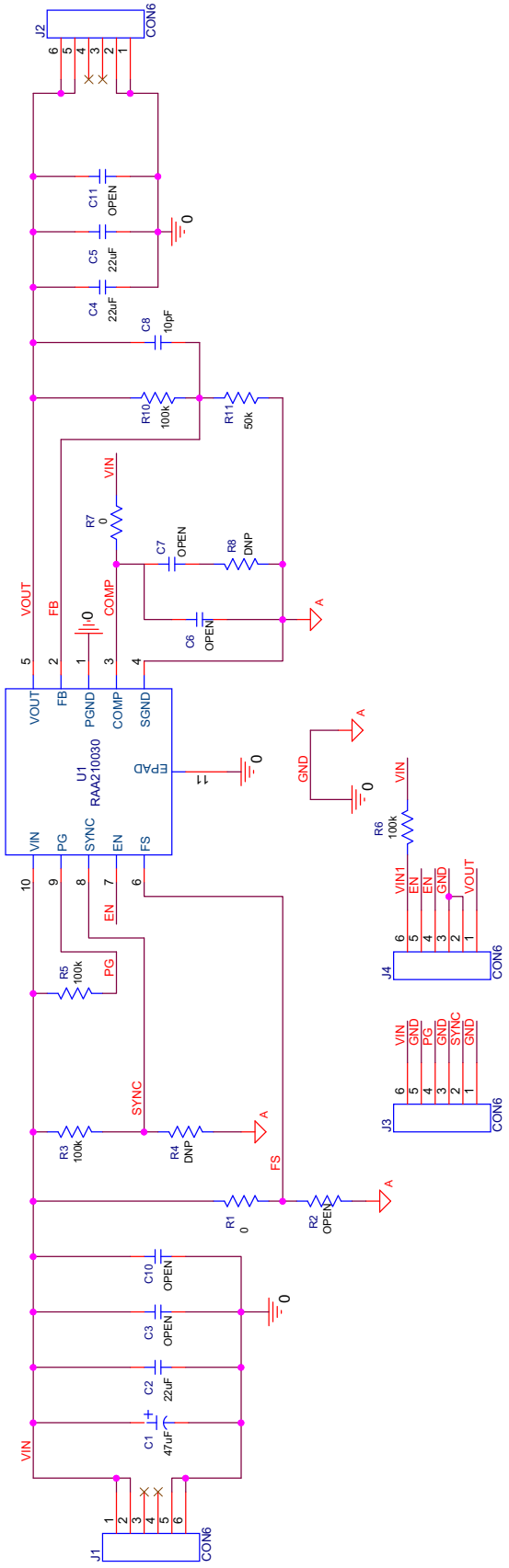

Figure 7. RTKA210030DR0000BU Schematic

2.3 Bill of Materials

Qty	Reference Designators	Manufacturer	Manufacture	Part Number
1	U1	IC-3A,5V,DC/DC STEP-DOWN PWR MODULE, 10P, DFN, 3×3, ROHS	Renesas	RAA210030
1	C1	CAP-POL, SMD, 47μF, 70mΩ, 20%,10V	Panasonic	10TAB47M
1	C2	CAP, SMD, 0603, 22μF, 10V, 20%, X5R, ROHS	Murata	GRM188R61A226ME15D
1	C8	CAP, SMD, 0402,10pF, 50V, 5%C0G, ROHS	Murata	GCM1555C1H100JA16
2	C4, C5	CAP, SMD, 0402, 22μF, 6.3V, 20%, X5R, ROHS	Murata	GRM158R60J226ME01D
4	R3, R5, R6, R10	RES-AEC-CQ200, SMD, 0402, 100K, 1/16W, 0.5%, ROHS	Vishay/dale	CRCW0402100KDHEDP
2	R1,R7	RES, SMD, 0402, 0Ω, 1/16W, 0.5%, TF, ROHS	Venkel	CR0402-16W-00T
1	R11	RES-AEC-Q200, SMD, 0402, 50K, 1/16W, 0.5%, ROHS	Vishay/Dale	CRCW040250KDHEDP
4	J1, J2, J3, J4	CONN HEADER R/A 6POS 2.54MM	Amphenol FCI	68015-106HLF

2.4 Board Layout

Include color images of board layout. Page width or multi-column is acceptable.

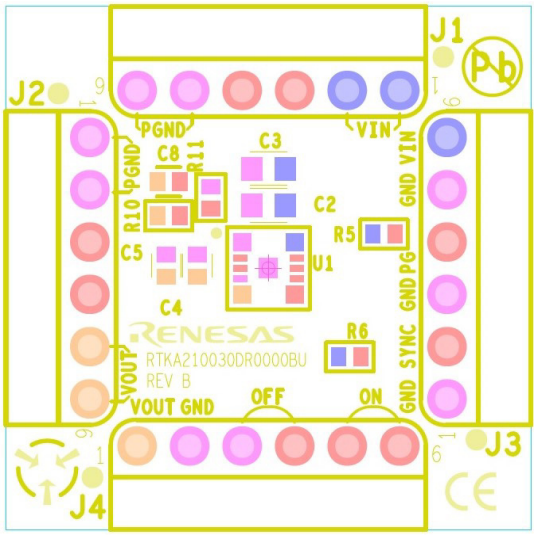

Figure 8. Silkscreen Top

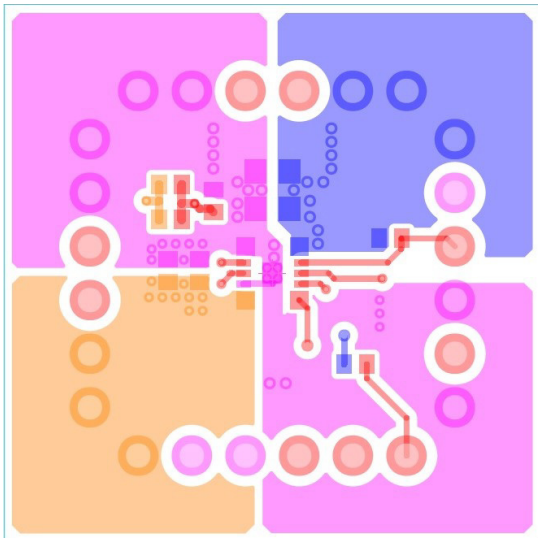

Figure 9. Top Layer

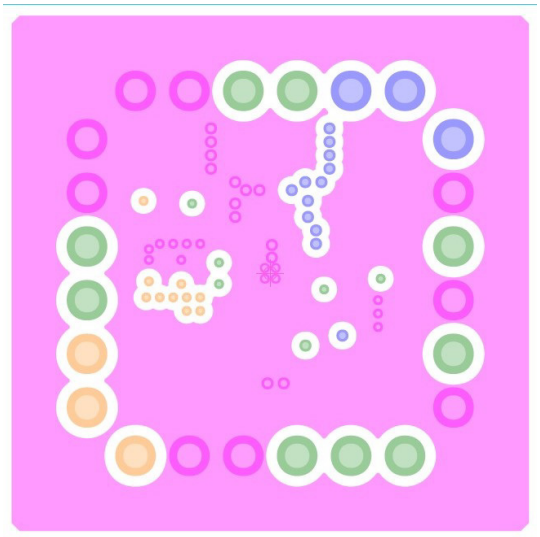

Figure 10. Layer 2

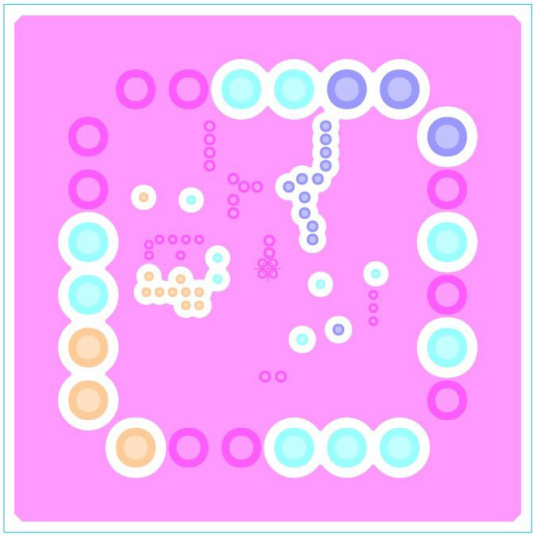

Figure 11. Layer 3

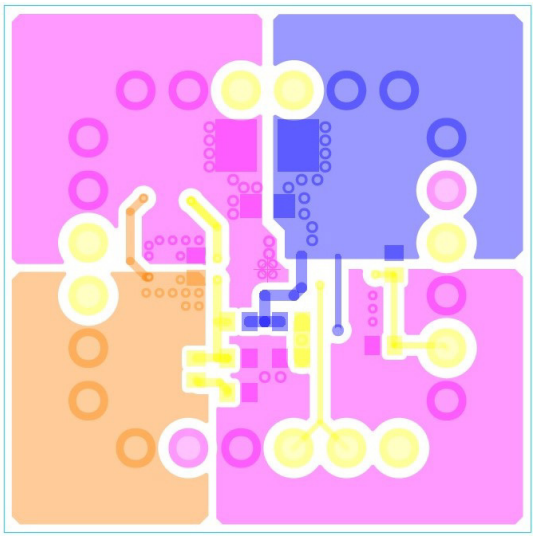

Figure 12. Layer 4

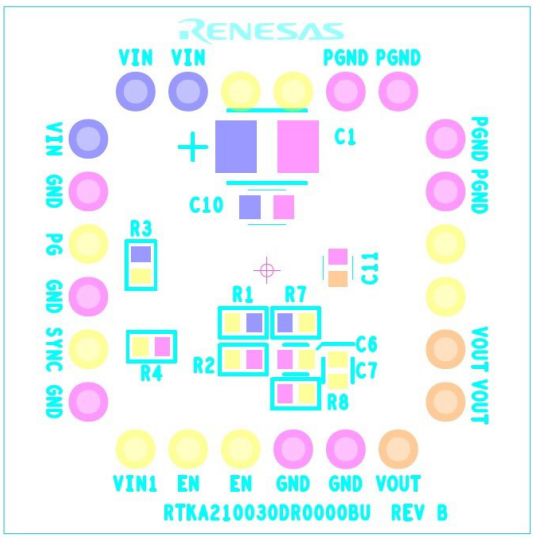

Figure 13. Silkscreen Bottom

3. Typical Performance Graphs

The following data was acquired using the RTKA210030DR0000BU demonstration board at +25C ambient and free air 0LFM.

Operating condition: V_{OUT} = 1.8V, f_{SW} = 2MHz, unless otherwise noted. See the Table 1 for recommended configurations for different output voltages.

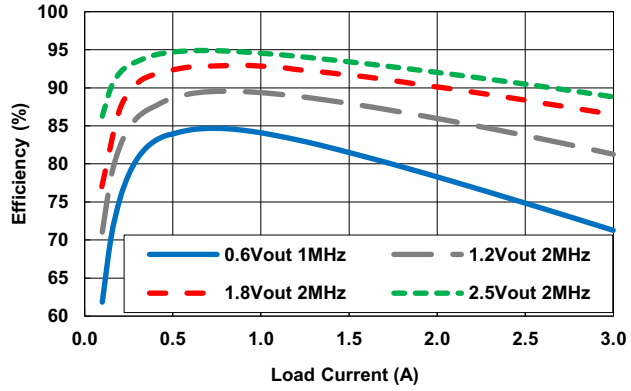

Figure 14. Efficiency vs Load Current, PWM, V_{IN} = 3.3V

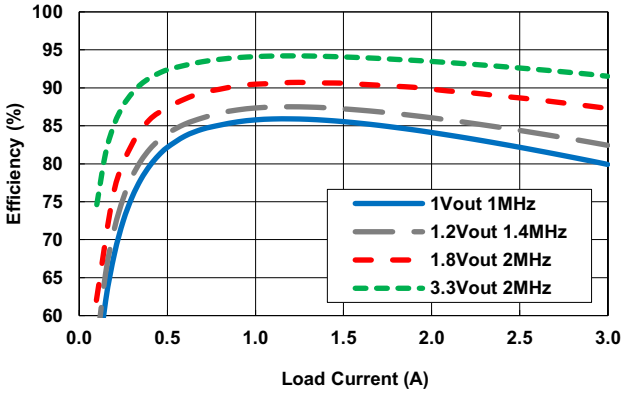

Figure 15. Efficiency vs Load Current, PWM, V_{IN} = 5V

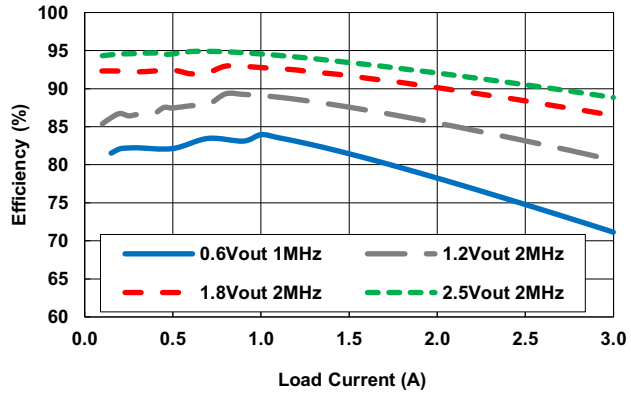

Figure 16. Efficiency vs Load Current, PFM, V_{IN} = 3.3V

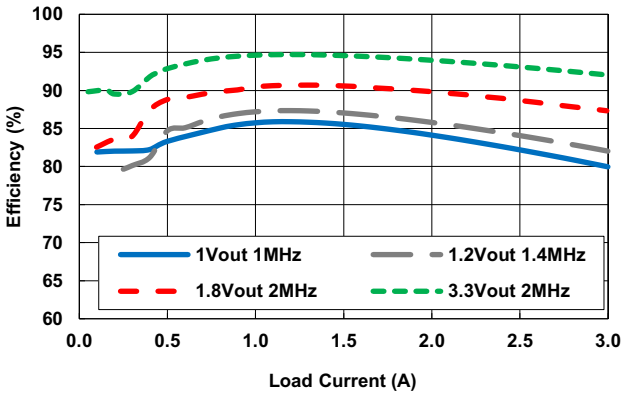

Figure 17. Efficiency vs Load Current, PFM, V_{IN} = 5V

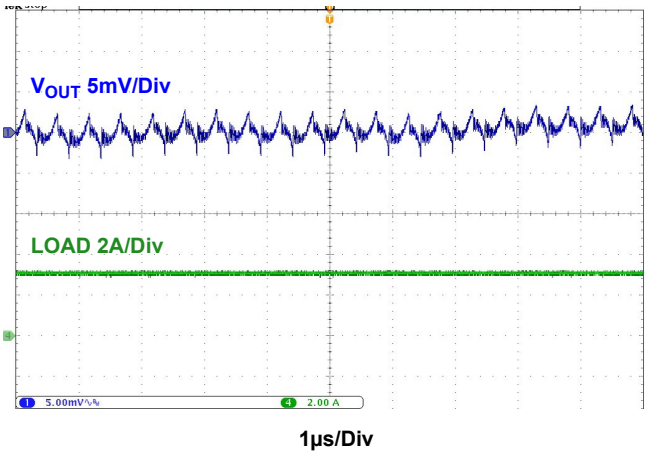

Figure 18. Output Ripple, V_{IN} = 3.3V, V_{OUT} = 1.8V, f_{SW} = 2MHz, Full Load, C_{OUT} = 2x22µF Ceramic

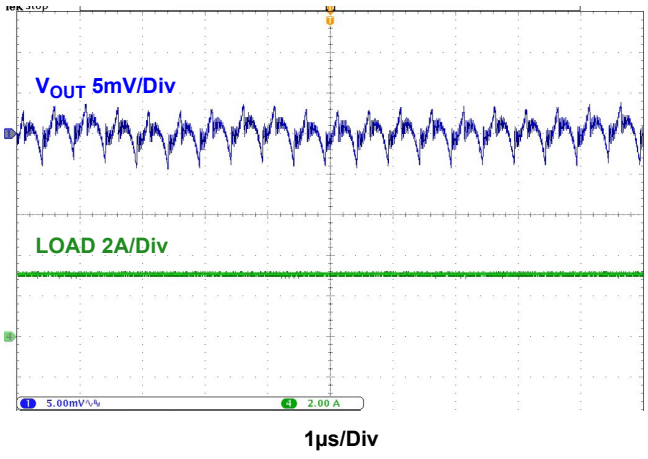

Figure 19. Output Ripple, V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 2MHz, Full Load, C_{OUT} = 2x22µF Ceramic

Operating condition: V_{OUT} = 1.8V, f_{SW} = 2MHz, unless otherwise noted. See the Table 1 for recommended configurations for different output voltages. (Cont.)

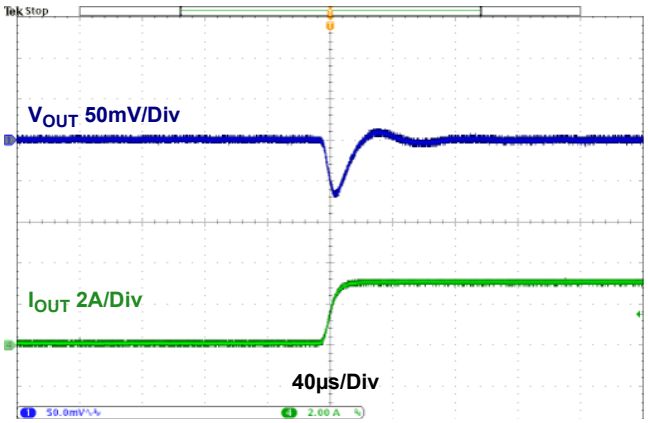

Figure 20. Transient Response, V_{IN} = 3.3V, V_{OUT} = 1.8V, f_{SW} = 2MHz, 0A to 3A, C_{OUT} = 2x22µF Ceramic, FPWM

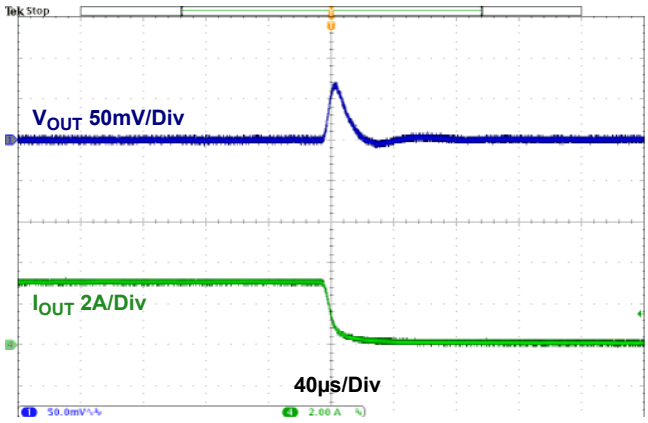

Figure 21. Transient Response, V_{IN} = 3.3V, V_{OUT} = 1.8V, f_{SW} = 2MHz, 3A to 0A, C_{OUT} = 2x22µF Ceramic, FPWM

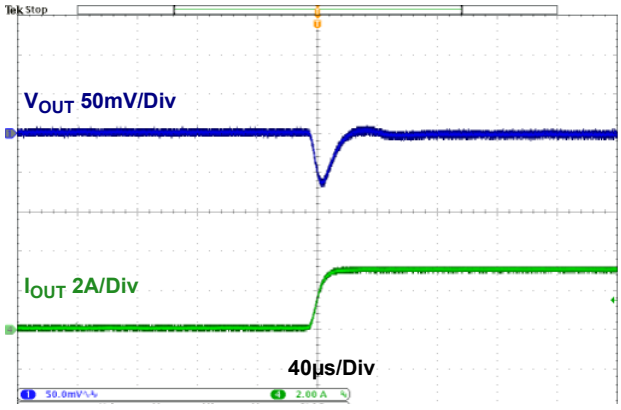

Figure 22. Transient Response, V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 2MHz, 0A to 3A, C_{OUT} = 2x22µF Ceramic, FPWM

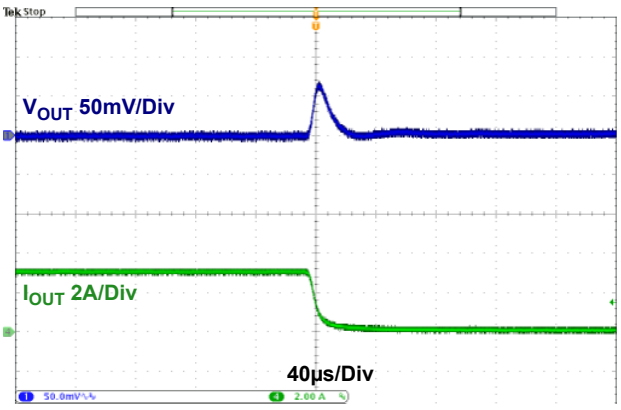

Figure 23. Transient Response, V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 2MHz, 3A to 0A, C_{OUT} = 2x22µF Ceramic, FPWM

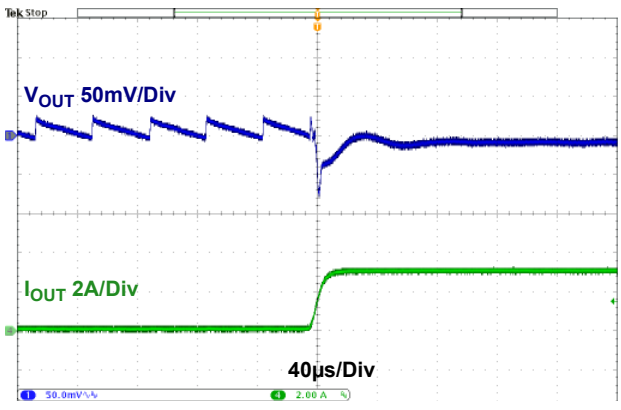

Figure 24. Transient Response, V_{IN} = 3.3V, V_{OUT} = 1.8V, f_{SW} = 2MHz, 0A to 3A, C_{OUT} = 2x22µF Ceramic, PFM

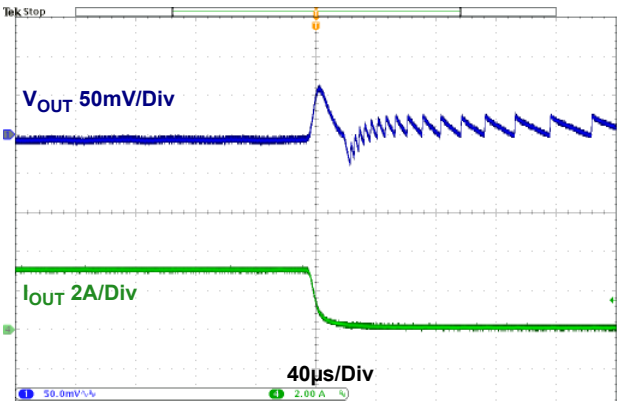

Figure 25. Transient Response, V_{IN} = 3.3V, V_{OUT} = 1.8V, f_{SW} = 2MHz, 3A to 0A, C_{OUT} = 2x22µF Ceramic, PFM

Operating condition: V_{OUT} = 1.8V, f_{SW} = 2MHz, unless otherwise noted. See the Table 1 for recommended configurations for different output voltages. (Cont.)

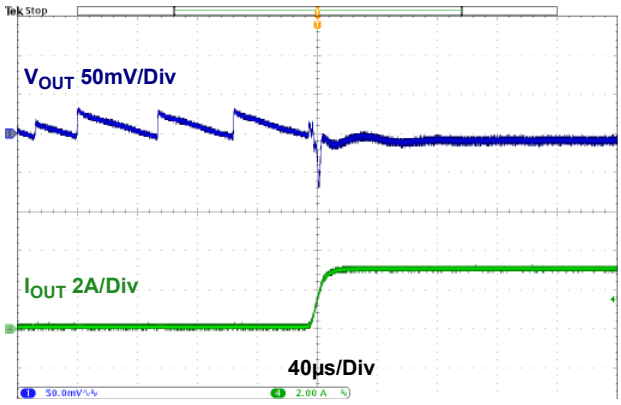

Figure 26. Transient Response, V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 2MHz, 0A to 3A, C_{OUT} = 2x22µF Ceramic, PFM

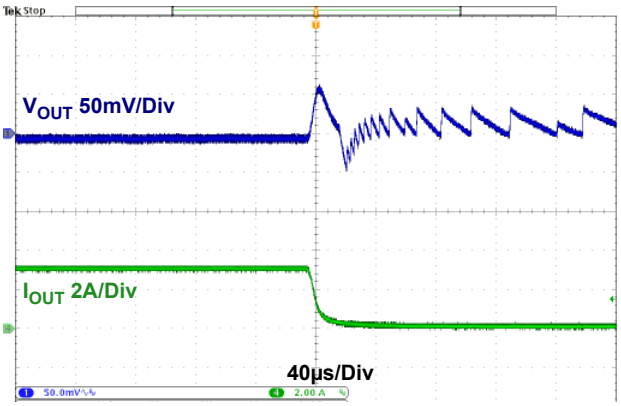

Figure 27. Transient Response, V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 2MHz, 3A to 0A, C_{OUT} = 2x22µF Ceramic, PFM

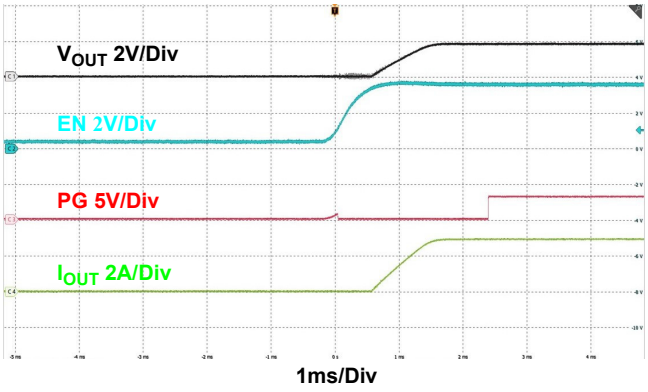

Figure 28. Start-Up Waveform, V_{IN} = 3.3V, V_{OUT} = 1.8V, f_{SW} = 2MHz, I_{OUT} = 3A, C_{OUT} = 2x22µF Ceramic

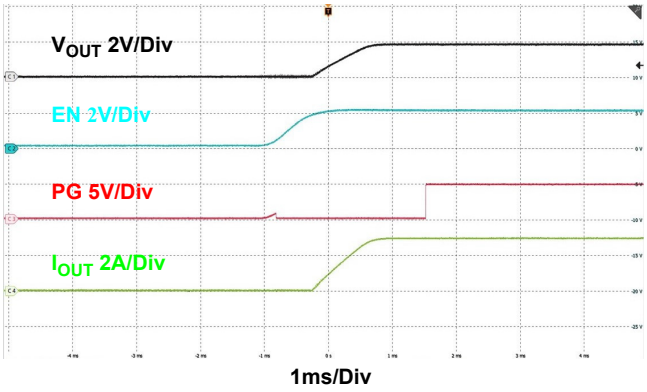

Figure 29. Start-Up Waveform, V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 2MHz, I_{OUT} = 3A, C_{OUT} = 2x22µF Ceramic

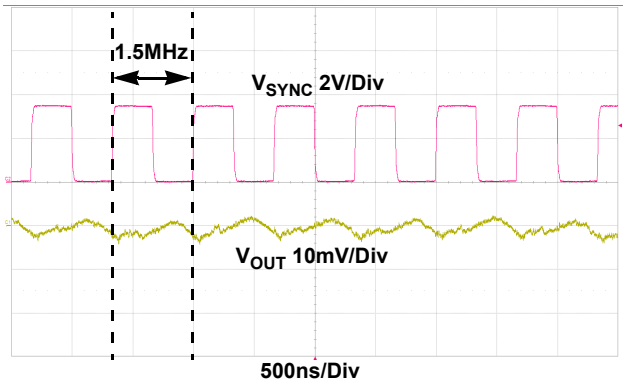

Figure 30. External Frequency Synchronization Waveform, V_{IN}= 3.3V, V_{OUT} = 1.8V, f_{SYNC} = 1.5MHz, I_{OUT} = 0A, C_{OUT} = 2x22uF Ceramic

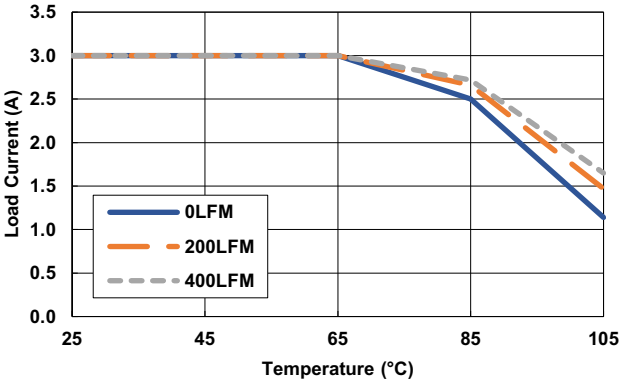

Figure 31. Derating Curve, V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{OUT} = 2x22µF Ceramic

Operating condition: V_{OUT} = 1.8V, f_{SW} = 2MHz, unless otherwise noted. See the Table 1 for recommended configurations for different output voltages. (Cont.)

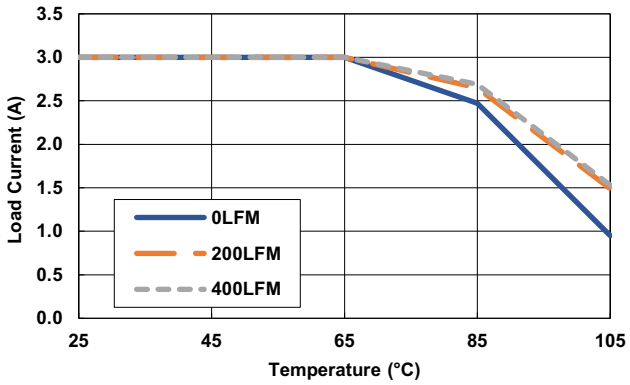

Figure 32. Derating Curve, V_{IN} = 5V, V_{OUT} = 1.8V, C_{OUT} = 2x22µF Ceramic

4. Ordering Information

Part Number	Description
RTKA210030DR0000BU	RAA210030 5V, 3A power module demonstration board

5. Revision History

Revision	Date	Description
1.00	May 28, 2022	Initial release

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