User's Manual

RTKA2108252H00000BU

User's Manual: Evaluation Board

Industrial Analog and Power

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1. Overview

The RAA210825 is a pin-strap configurable 25A step-down PMBus-compliant DC/DC power supply module that integrates a digital PWM controller, synchronous MOSFETs, a power inductor, and passive components. Only input and output capacitors are needed to finish the design. Because of its thermally-enhanced HDA packaging technology, the module can deliver up to 25A of continuous output current without the need for airflow or additional heat sinking. The RAA210825 simplifies configuration and control of Renesas digital power technology while offering an upgrade path to a full PMBus configuration through the pin-compatible ISL8277M.

The RTKA2108252H00000BU evaluation board is a 4.0inx4.5in 4-layer FR4 board with 2oz. copper in all layers. The RAA210825 comes with a preprogrammed configuration for operating in Pin-Strap mode. Output voltage, switching frequency, input UVLO, soft-start/stop delay and ramp times, and the device SMBus address can be programmed with external pin-strap resistors.

The ZLUSBEVAL3Z (USB to PMBus adapter) is provided with this evaluation board, which connects the evaluation board to a PC to activate the PMBus communication interface. The PMBus command set is accessed by using the PowerNavigator™ software from a PC running Microsoft Windows. The RTKA2108252H00000BU can operate in Pin-Strap mode without needing the ZLUSBEVAL3Z adapter or PMBus communication.

1.1 Key Features

- V_{IN} range of 4.5V to 14V, V_{OUT} adjustable from 0.6V to 5V
- Pin-Strap mode for standard setting: V_{OUT}, switching frequency, input UVLO, soft-start/stop, and external synchronization
- Real-time telemetry for V_{IN}, V_{OUT}, I_{OUT}, temperature, duty cycle, switching frequency, and fault logging
- ChargeMode™ control that is tunable with pin-strap resistors or the PMBus interface
- Mechanical switch for enable and the power-good LED indicator

1.2 Specifications

This board has been configured and optimized for the following operating conditions:

- V_{IN} = 5V to 12V
- V_{OUT} = 1.2V
- I_{MAX} = 25A
- f_{SW} = 364kHz
- ASCR gain = 250, ASCR residual = 100
- On/off delay = 5ms, on/off ramp time = 5ms
- Input UVLO = 4.2V
- PMBus address = 0x28h

1.3 Ordering Information

Part Number	Description
RTKA2108252H00000BU	RAA210825 evaluation board (also included: ZLUSBEVAL3Z adapter, USB cable)

1.4 Related Literature

For a full list of related documents, visit our website

- RAA210825 product page

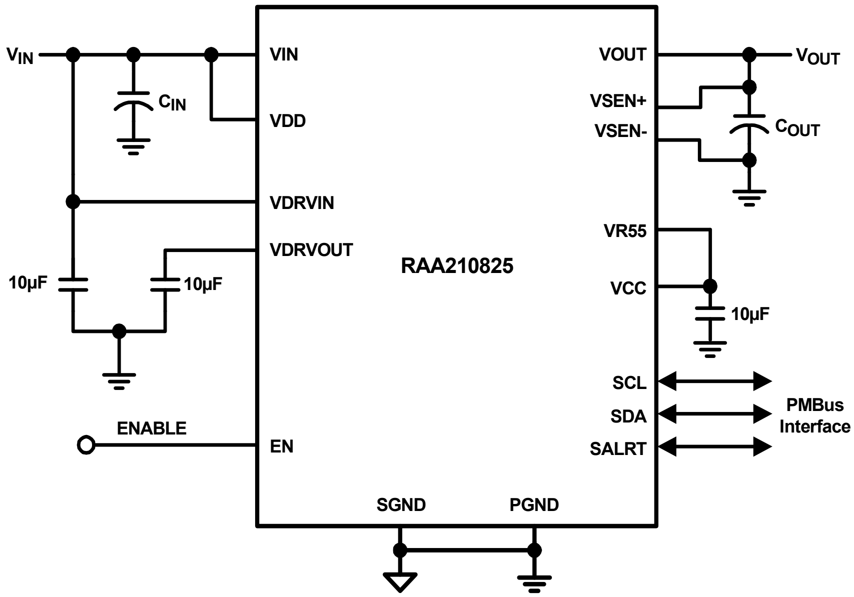

Figure 1. Block Diagram

1.5 Recommended Equipment

- DC power supply with minimum 15V/20A sourcing capacity
- Electronic load capable of sinking current up to 25A
- Digital multimeters (DMMs)
- Oscilloscope with higher than 100MHz bandwidth

2. Functional Description

The RTKA2108252H00000BU provides all circuitry required to evaluate the features of the RAA210825. A majority of the features of the RAA210825, such as compensation-free ChargeMode control, soft-start delay and ramp times, external clock synchronization, and bode plot measurement are available on this evaluation board.

Figure 4 on page 10 shows an image of the RTKA2108252H00000BU evaluation board.

2.1 Operating Range

By default, the RTKA2108252H00000BU is configured to operate at V_{OUT} = 1.2V, f_{SW} = 364kHz. V_{IN} ranges from 4.5V to 12V. The board can also support a wider operating range to meet the requirements of specific applications. The V_{OUT} can be adjusted from 0.6V to 5V. Load current range is 0A to 25A. Note that airflow across the board may be needed for continuous operation at 25A (at elevated ambient temperatures). The f_{SW} and output voltage can also be tuned. However, to ensure sufficient stability margins, the switching frequency and output capacitors can only be selected using the “RAA210825 Design Matrix Guide and Output Voltage Response” table in the RAA210825 datasheet.

If the input voltage is less than 5.3V, tie the VCC test point directly to VIN or to a separate 5V power supply for normal operation and best efficiency.

The RTKA2108252H00000BU is capable of handling a 0A to 25A output current transient in which the slew rate is less than 2A/µs, such as electronic load. If the slew rate exceeds the 2A/µs, it may be necessary to increase the output capacitance or change VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT values for proper operation (refer to “PMBus Option” on page 5).

If external synchronization is used, connect the SYNC test point to the external clock. Note that the external clock signal should be active before the module is enabled.

2.2 PMBus Operation

Install the PowerNavigator software from the Renesas website.

For board operation, connect the included ZLUSBEVAL3Z dongle to the 6-pin male connector labeled as “PMBus DONGLE IN”. Connect the desired load and an appropriate power supply to the input, and connect the included USB cable to the PC running PowerNavigator. Set the ENABLE switch to “DISABLE” before turning on the power.

PowerNavigator allows modification of all RAA210825 PMBus parameters for debugging purposes.

The ENABLE switch can then be moved to “ENABLE” and the RTKA2108252H00000BU board can be tested. Alternately, the PMBus ON_OFF_CONFIG and OPERATION commands can be used from PowerNavigator.

2.3 Quick Start Guide

2.3.1 Pin-Strap Option

The RTKA2108252H00000BU can be configured in Pin-Strap mode with standard 1% 0603 resistors. The PMBus interface is not required to evaluate RAA210825 in Pin-Strap mode. Output voltage (V_{OUT}), switching frequency (f_{SW}), input undervoltage protection (UVLO) threshold, Start/Stop time delay and ramp time, ASCR setting, and the device PMBus address can be changed by populating the recommended resistors at placeholders provided in the evaluation board. By default, the evaluation board is programmed to regulate at V_{OUT} = 1.2V, f_{SW} = 364kHz, UVLO = 4.5V, and PMBus address = 28h. Follow these steps to evaluate RAA210825 in Pin-Strap mode.

(1) Set the ENABLE switch to “DISABLE”.
(2) Connect a load to the VOUT lug connectors (J_8 and J_9).
(3) Connect a power supply to the VIN connectors (J_1 and J_2). Make sure the power supply is not enabled when making the connection.
(4) Adjust the V_{IN} = 12V and turn the power supply on.
(5) Set the ENABLE switch to “ENABLE”.
(6) Measure 1.2V V_{OUT} at probe points TP_9 and TP_{13}.
(7) Observe switching frequency of 364kHz at probe point labeled VSWH (TP_8).
(8) To change the V_{OUT}, disconnect the board from the setup and populate with a 1% standard 0603 resistor at R_6 placeholder location on bottom layer. Refer to the “Output Voltage Resistor Settings” table in the RAA210825 datasheet for recommended values. By default, VOUT_MAX is set 110% of V_{OUT} set by pin-strap resistor.
(9) To change the switching frequency, disconnect the board from the setup and populate with a 1% standard 0603 resistor at the R_2 placeholder location on the bottom layer. Refer to the “Switching Frequency Resistor Settings” table in the RAA210825 datasheet for recommended values.
(10) To change the soft-start/stop ramp and delay time or UVLO, disconnect the board from the set up and populate with a 1% standard 0603 resistor at R_7 placeholder location on bottom layer. Refer to the “Soft-Start/Stop Resistor Settings” or “UVLO Resistor Settings” table in the RAA210825 datasheet for recommended values.
(11) To change the ASCR, disconnect the board from the setup and populate with a 1% standard 0603 resistor at the R_8/R_{20} placeholder location on the bottom layer. Refer to the “ASCR Resistor Settings” table in the RAA210825 datasheet for recommended values.

2.3.2 PMBus Option

The RTKA2108252H00000BU can be evaluated for all features using the provided ZLUSBEVAL3Z dongle and PowerNavigator. Follow these steps to evaluate the RAA210825 with the PMBus option.

(1) Install PowerNavigator.
(2) Set the ENABLE switch to “DISABLE”
(3) Connect a load to the VOUT lug connectors (J_8 and J_9).
(4) Connect a power supply to the VIN connectors (J_1 and J_2). Make sure the power supply is not enabled when making the connection.
(5) Adjust the V_{IN} = 12V and turn the power supply on.
(6) Connect the ZLUSBEVAL3Z dongle (USB to PMBus adapter) to the RTKA2108252H00000BU board to the 6-pin male connector labeled as “PMBus DONGLE IN”.
(7) Connect the supplied USB cable from the computer through USB to the ZLUSBEVAL3Z dongle.
(8) Launch PowerNavigator.
(9) The RAA210825 device on the board operates in Pin-Strap mode from factory default, but the user can modify the operating parameters through the evaluation software to monitor faults, debug a test case, and read real-time values of the input/output parameters, switching frequency, duty cycle, and temperature.
(10) Set the ENABLE switch to “ENABLE”. Alternatively, the PMBus ON_OFF_CONFIG and OPERATION commands can be used from PowerNavigator to allow PMBus Enable.
(11) Monitor and configure the RTKA2108252H00000BU board using the PMBus commands in the evaluation software.

3. Evaluation Board Information

3.1 External Clock Synchronization

The RAA210825 is capable of synchronizing to an external clock. External clock synchronization allows the user to operate multiple converters at the same switching frequency and can lead to improved EMI characteristics. The RTKA2108252H00000BU evaluation board can be used to assess this functionality. A function generator will be required. Follow the steps below to operate the RAA210825 with an external clock frequency of 593kHz:

(1) Set the Enable switch to “DISABLE” position.
(2) Solder a 17.8kΩ resistor at RSET on CFG pin (R_{16}).
(3) Program the function generator to output a continuous square pulse waveform of 593kHz. Program the pulse width to be at least 150ns.
(4) Ensure that the clock signal is stable by monitoring the waveform on an oscilloscope.
(5) Once verified, connect the output cables from the function generator to test point J_4 labeled “SYNC”.
(6) Turn the function generator to “ON”.
(7) Enable the module by setting the Enable switch to the “ENABLE” position.
(8) Observe the switching frequency at test point TP_8 labeled “VSWH”.
(9) The module will synchronize to the 593kHz external clock from the function generator.
(10) Ensure that the module is always disabled before changing the frequency of the external clock.
(11) A Loss of Sync fault is generated when the external clock is lost.

3.2 Bode Plots Measurement

Assessing the stability of the converter is an important step in the design process. Bode plots can be a useful and reliable tool to identify the loop response of the converter. Phase and gain margins give an insight into the stability of the system, and the bandwidth can indicate how quickly the converter responds to disturbances in input voltage or load transients. Correctly measuring the loop response is critical for designing stable converter systems.

A network analyzer is required to perform the frequency response measurements on the RTKA2108252H00000BU evaluation board. Follow the steps below to evaluate the converter loop response for RAA210825 on the RTKA2108252H00000BU evaluation board.

(1) Break the feedback loop by removing the R_9 resistor in the remote sense path, connected between VSEN+ and VOUT.
(2) Solder a 20Ω resistor in its place. The value of the resistor could be in the range of 10Ω to 50Ω.
(3) Solder a twisted wire pair to the 20Ω resistor. Ensure that the wires are short in length. A small twisted pair works well by minimizing noise pickup, which is important for a good measurement.
(4) Enable the module.
(5) Use a “Network Analyzer” to inject a small AC signal (~20mV) across the 20Ω resistor as shown in Figure 2.
(6) Measure the amplitudes of the signals at points A and B as shown in Figure 2.
(7) Sweep the frequency using the “Network Analyzer” to observe the bandwidth, phase, and gain margin.

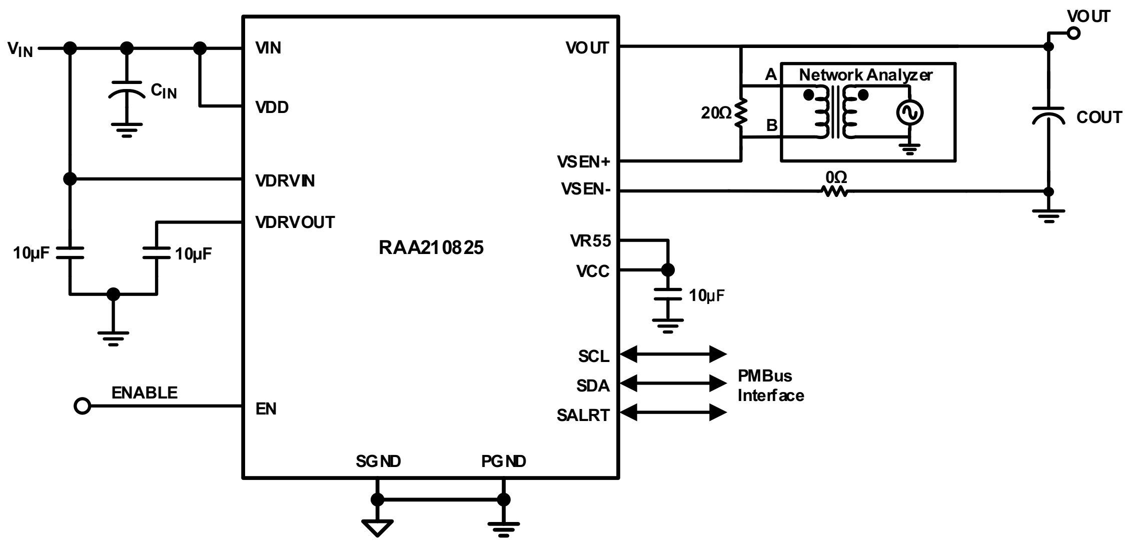

Figure 2. Network Analyzer

Figure 3 shows an example plot generated by the network analyzer for the RAA210825 at 12V input and 1.2V/25A output at 364kHz with 10x100µF ceramic capacitors + 2x470µF POSCAPs at output. ASCR Gain = 250 and Residual = 100 have been used. The plot shows a crossover frequency of 50kHz with a phase margin of 69.12°. A 10.7dB gain margin is observed at 144.54kHz.

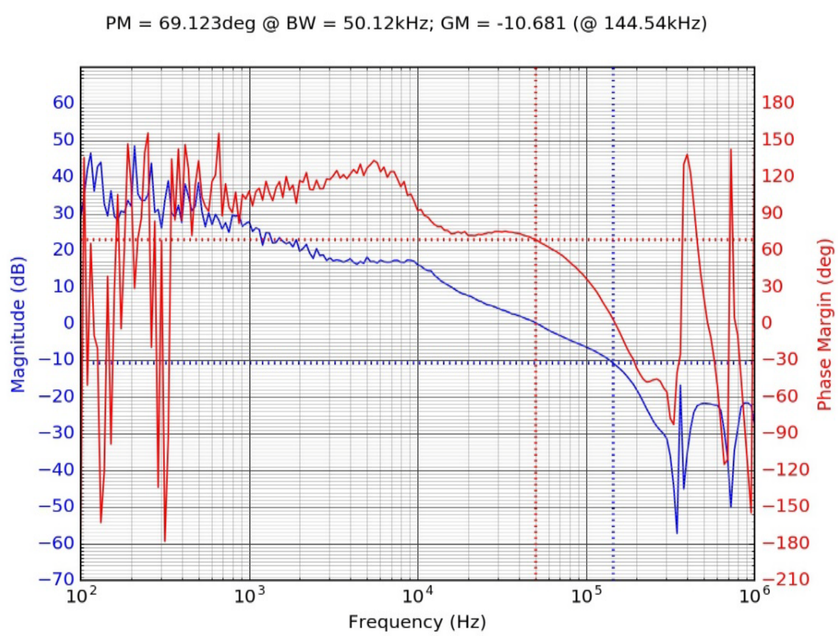

Figure 3. Network Analyzer Example Plot

Refer to the RAA210825 datasheet for detailed design guideline including selection of input/output capacitors and different ASCR gain and residual values.

3.3 Interleave Operation

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device, so that all devices do not start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce the input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, while the power losses proportional to the I^2_{RMS} are reduced dramatically.

To enable phase spreading in a multi-module operation, all converters must be synchronized to the same switching clock. The phase offset of each device may be set to any value between 0° and 360° in 22.5° increments by choosing the device PMBus address from the “INTERLEAVE Settings from SA” table in the RAA210825 datasheet. The lower 4 bits of the PMBus address set the value of INTERLEAVE command. To implement Interleave functionality for a two module operation, follow the steps below:

(1) Choose SA (SMBus Address) for Module 1 and Module 2 from the “INTERLEAVE Settings from SA” table in the RAA210825 datasheet based on the desired phase difference. Populate the corresponding RSET for SA (R_5) according to the “SMBus Address and VSET Group Resistor Settings” table in the RAA210825 datasheet.
For example: when Module 1 has SA = 28h (INTERLEAVE = 8, 180° phase shift from the rising edge of the external clock) and Module 2 has SA = 24h (INTERLEAVE = 4, 90° phase shift from the rising edge of the external clock), the net phase difference between Module 1 and Module 2 will be 180 - 90 = 90°.
(2) Populate RSET on CFG for both boards to synchronize to an external clock source of a particular switching frequency based on the “External Frequency Sync Settings” table in the RAA210825 datasheet.
(3) Connect the power supply to the V_{IN} connectors (VIN/GND) on both boards.
(4) Connect the ZLUSBEVAL3Z dongle to the 6-pin male connector labeled “PMBus DONGLE In” to one of the boards.
(5) Daisy chain the second board to the first board by connecting “PMBus DONGLE Out” of the first board to the “PMBus DONGLE In” of the second board.
(6) Provide an external clock on the SYNC pins of the two boards from a function generator. External clock frequency from the function generator should be within ±10% of the listed options shown in the “External Frequency Sync Settings” table in the RAA210825 datasheet. Incoming clock signal must be stable before the enable pin is asserted. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns.
(7) Turn the input power supply ON. Next, set the ENABLE switch to the “ENABLE” position.
(8) Monitor the VSWH node at the probe point labeled VSWH (TP_8) on the two boards using an oscilloscope to verify the phase spread set.
(9) This functionality can also be verified using the INTERLEAVE command in PowerNavigator.
(10) Note that every module gets assigned a unique Rail ID based on the SA setting. This can be observed in the Power Map window of PowerNavigator.

4. PCB Layout Guidelines

To achieve stable operation, low losses, and good thermal performance some layout considerations are necessary.

The key features of the RTKA2108252H00000BU layout are as follows:

- Establish a separate SGND and PGND plane, and next, connect the SGND to PGND plane in the middle layer. To make connections between SGND/PGND on the top layer and other layers, use multiple vias for each pin to connect to the inner SGND/PGND layer. Do not connect SGND directly to PGND on a top layer. Connecting SGND directly to PGND without establishing an SGND plane will bypass the decoupling capacitor at the internal reference supplies, making the controller susceptible to noise.
- Place enough ceramic capacitors between VIN and PGND, VOUT and PGND, and bypass capacitors between VDD and the ground plane, as close to the module as possible to minimize high frequency noise.
- Use large copper areas for a power path (VIN, PGND, and VOUT) to minimize conduction loss and thermal stress. Use multiple vias to connect the power planes in different layers. Extra ceramic capacitors at VIN and VOUT can be placed on the bottom layer under the VIN and VOUT pads when using multiple vias for connecting copper pads on the top and bottom layers.
- Connect differential remote sensing traces to the regulation point to achieve a tight output voltage regulation. Route a trace from VSEN+ and VSEN- to the point-of-load where the tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENSE signal near the VSWH pads.
- For noise sensitive applications, Renesas recommends connecting the VSWH pads only on the top layer; however, thermal performance will be sacrificed. External airflow might be required to keep the module heat at a desired level. For applications where switching noise is less critical, excellent thermal performance can be achieved in this power module by increasing the copper mass attached to the VSWH pad. To increase copper mass on the VSWH node, create copper islands in the middle and bottom layers under the VSWH pad and connect them to the top layer with multiple vias. Shield those copper islands with a PGND layer to avoid any interference to noise sensitive signals.

4.1 Thermal Considerations and Current Derating

Board layout is critical for safe module operation and maximum allowable power delivery. To work in high temperature environments and carry large currents, the board layout needs to be carefully designed to maximize thermal performance. To achieve this, select enough trace width, copper weight, and the proper connectors.

This evaluation board is designed for running 25A at room temperature without additional cooling systems needed. However, if the output voltage is increased or the board is operated at elevated temperatures, the available current is derated. Refer to the derated current curves in the RAA210825 datasheet to determine the maximum output current that the evaluation board can supply. θ_{JA} is measured by inserting a thermocouple inside the module to measure the peak junction temperature.

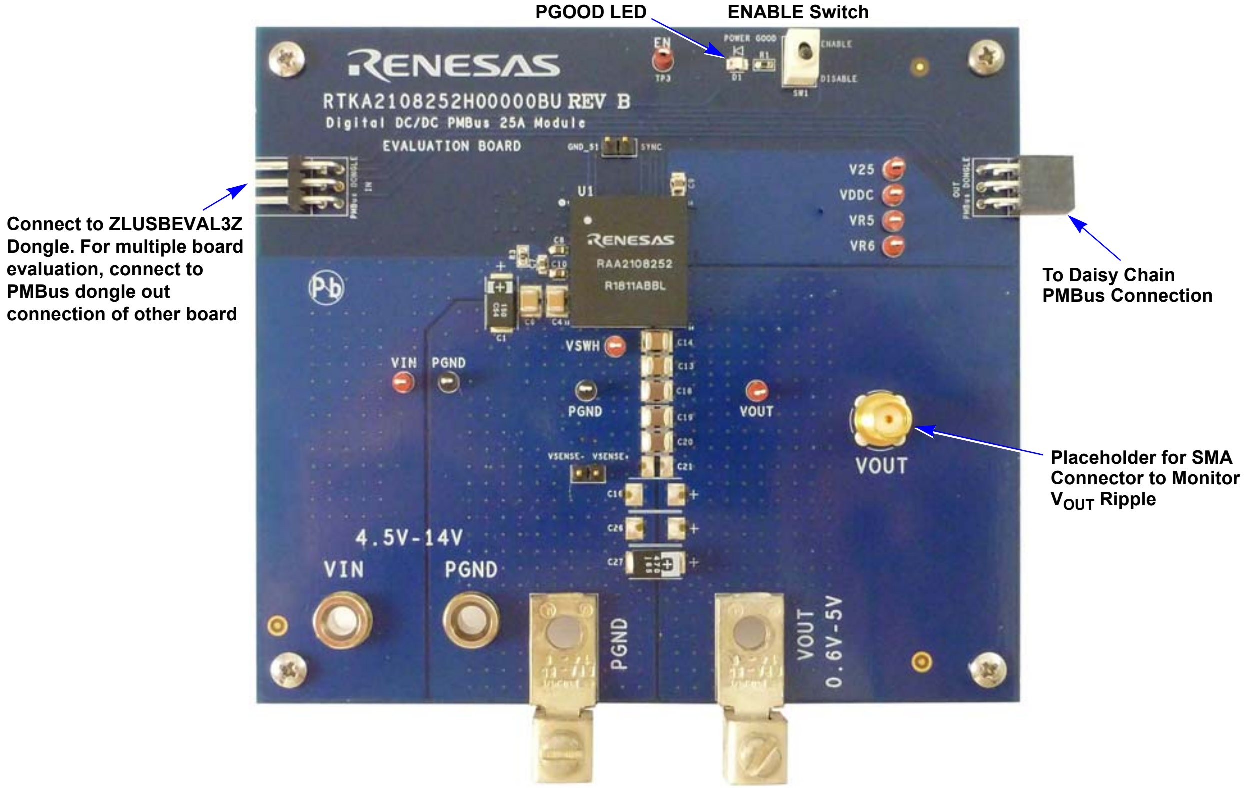

Figure 4. RTKA2108252H00000BU Evaluation Board (Top Side)

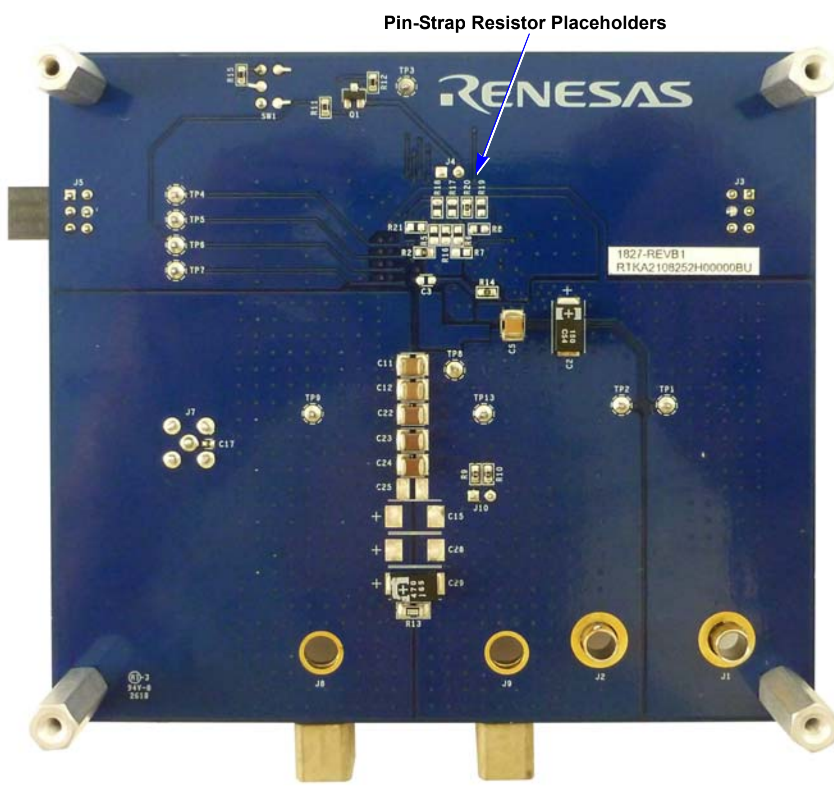

Figure 5. RTKA2108252H00000BU Evaluation Board (Bottom Side)

4.2 RTKA2108252H00000BU Board Schematic

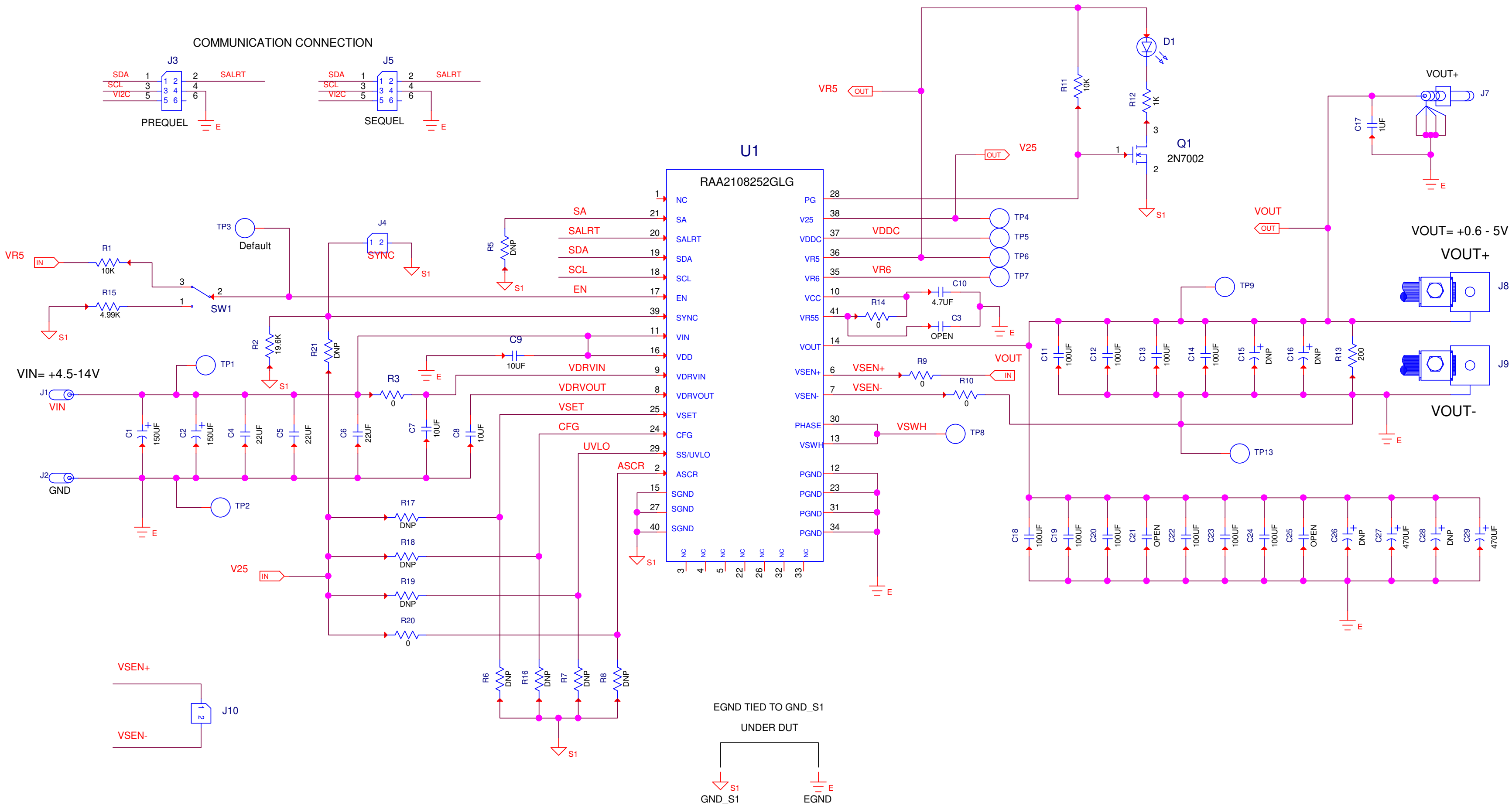

Figure 6. Schematic

4.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, RTKA2108252H00000BU, REVB, ROHS	MULTILAYER PCB TECHNOLOGY/HI TECH	RTKA2108252H00000BURBPCB
1	C9	CAP, SMD, 0805, 10µF, 25V, 10%, X5R, ROHS	TDK	C2012X5R1E106K085AC
10	C11-C14, C18-C20, C22-C24	CAP, SMD, 1210, 100µF, 6.3V, 20%, X5R, ROHS	TDK	C3225X5R0J107M
1	C17	CAP, SMD, 0402, 10µF, 6.3V, 10%, X5R, ROHS	PANASONIC	ECJ-0EB0J105K
2	C7, C8	CAP, SMD, 0603, 10µF, 16V, 20%, X5R, ROHS	MURATA	GRM188R61C106MA73D
1	C10	CAP, SMD, 0603, 4.7µF, 16V, 10%, X5R, ROHS	MURATA	GRM188R61C475KAAJD
0	C3	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
3	C4, C5, C6	CAP, SMD, 1210, 22µF, 25V, 10%, X5R, ROHS	MURATA	GRM32ER61E226KE15K
0	C21, C25	CAP, SMD, 1210, DNP-PLACE HOLDER, ROHS		
2	C1, C2	CAP-POSCAP, SMD, 7.3x4.3, 150µF, 16V, 20%, 50mΩ, ROHS	SANYO/PANASONIC	16TQC150MYF
2	C27, C29	CAP-POSCAP, LOW ESR, SMD, D4, 470µF, 6.3V, 20%, 18mΩ, ROHS	SANYO	6TPE470MI
1	J7	CONN-RF, SMA JACK, 50Ω, PCB MNT, STRAIGHT, ROHS	JOHNSON COMPONENTS	142-0701-231
8	TP1, TP3-TP9	CONN-MINI TEST PT, VERTICAL, RED, ROHS	KEYSTONE	5000
2	TP2, TP13	CONN-MINI TEST PT, VERTICAL, BLK, ROHS	KEYSTONE	5001
2	J1, J2	CONN-JACK, MINI BANANA, 0.175 PLUG, NICKEL/BRASS, ROHS	KEYSTONE	575-4
2	J4, J10	CONN-HEADER, 1x2, BRKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
1	J5	CONN-SOCKET STRIP, TH, 2x3, 2.54mm, TIN, R/A, ROHS	SAMTEC	SSQ-103-02-T-D-RA
1	J3	CONN-HEADER, 2x3, BRKAWY, 2.54mm, TIN, R/A, ROHS	SAMTEC	TSW-103-08-T-D-RA
1	D1	LED, SMD, 0805, GREEN, CLEAR, 10mcd, 2.1V, 20mA, 570nm, ROHS	CHICAGO MINIATURE	CMD17-21VGC/TR8
1	U1	IC-MODULE, 25A, DIGITAL, DC/DC POWER SUPPLY, 41P, HDA, ROHS	RENESAS ELECTRONICS AMERICA	RAA2108252GLG#AG0
1	Q1	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	DIODES, INC.	2N7002-7-F
0	R5-R8, R16-R19, R21	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER		
5	R3, R9, R10, R14, R20	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL	CR0603-10W-000T

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	R12	RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF1001V
2	R1, R11	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1002FT
1	R2	RES, SMD, 0603, 19.6k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1962FT
1	R15	RES, SMD, 0603, 4.99k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF4991V
1	R13	RES, SMD, 1206, 200Ω, 1/8W, 1%, TF, ROHS	PANASONIC	ERJ-8ENF2000V
1	SW1	SWITCH-TOGGLE, THRU-HOLE, SPDT, 5P, ROHS	C&K COMPONENTS	GT11MCBE
4	Four corners	SCREW, 4-40x1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	BUILDING FASTENERS	PMSSS 440 0025 PH
4	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	KEYSTONE	2204
2	J8, J9	HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SCREW, ROHS	BERG/FCI	KPA8CTP
1	Place assy in bag	BAG, STATIC, 6x8, ZIPLOC, ROHS	ULINE	S-2262
0	C15, C16, C26, C28 (6TPE470MI)	DO NOT POPULATE OR PURCHASE		
1	AFFIX TO BACK OF PCB	LABEL-DATE CODE_LINE 1: YRWK/REV#, LINE 2: BOM NAME	RENESAS ELECTRONICS AMERICA	LABEL-DATE CODE

4.4 RTKA2108252H00000BU Board Layout

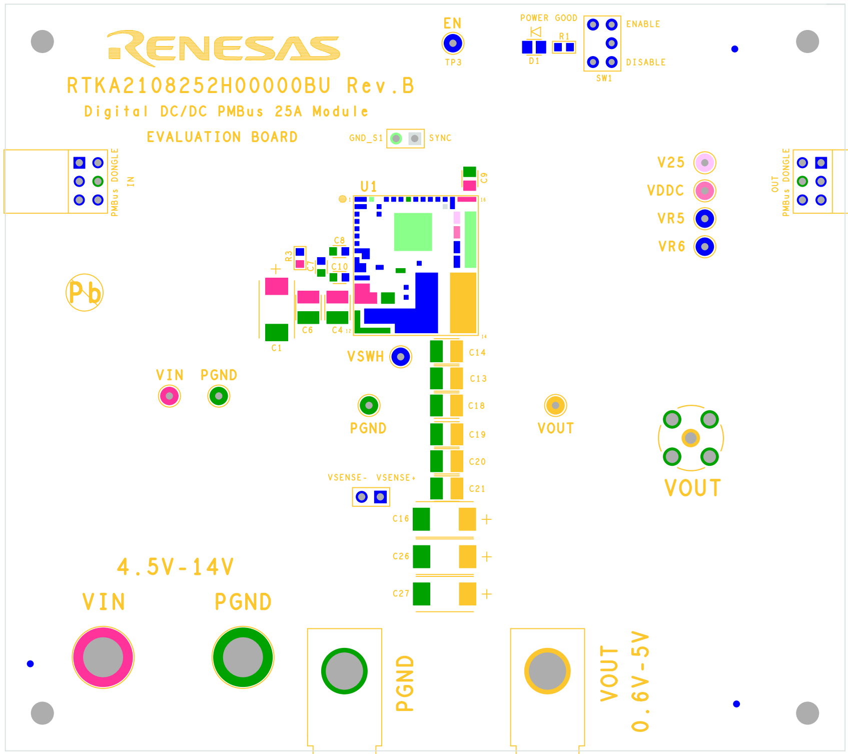

Figure 7. PCB - Silkscreen Top

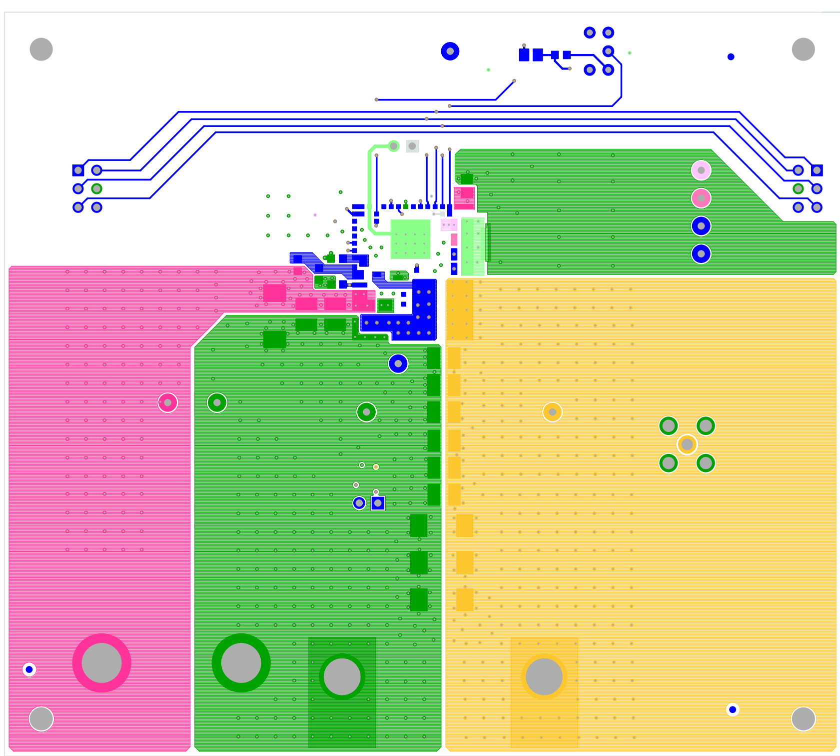

Figure 8. PCB - Top Layer Component Side

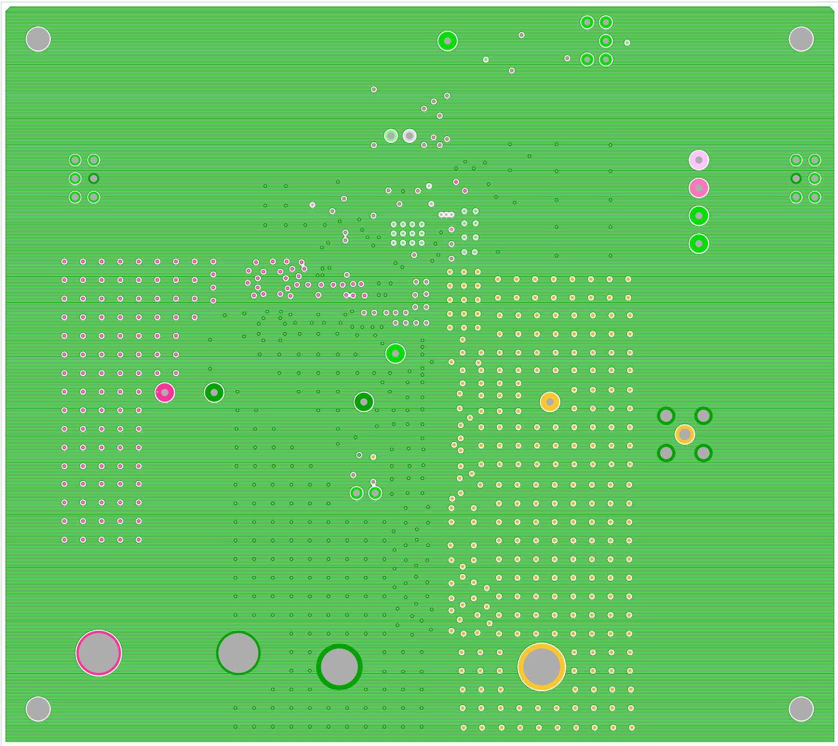

Figure 9. PCB - Inner Layer - Layer 2 (Top View)

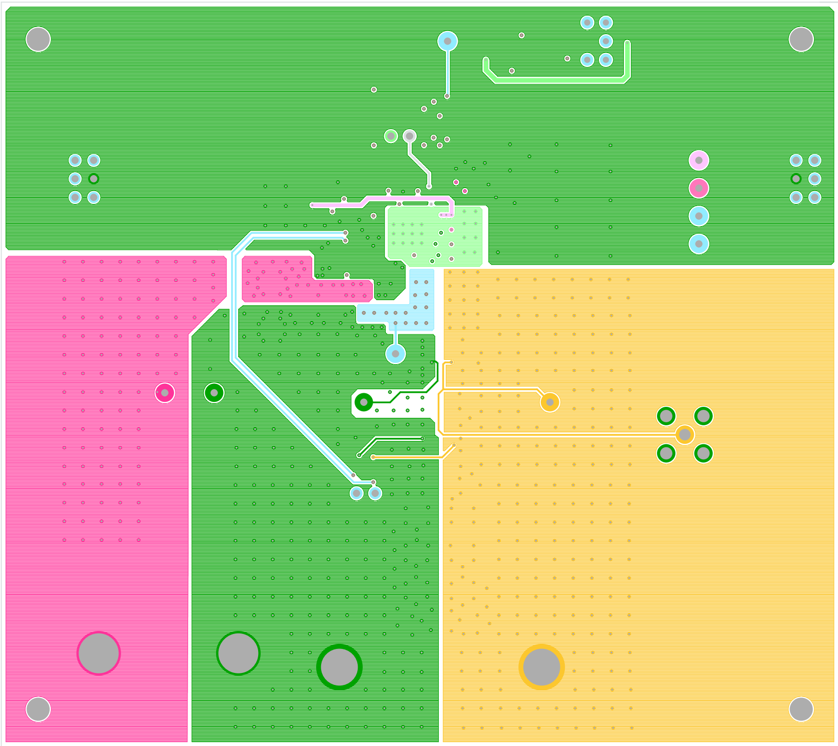

Figure 10. PCB - Inner Layer - Layer 3 (Top View)

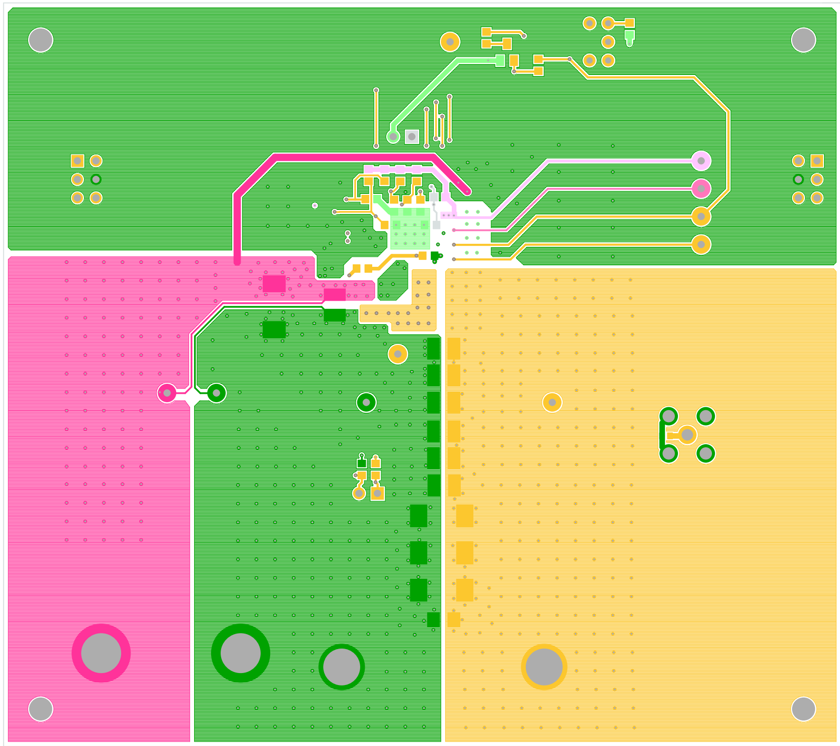

Figure 11. PCB - Bottom Layer Solder Side (Bottom View)

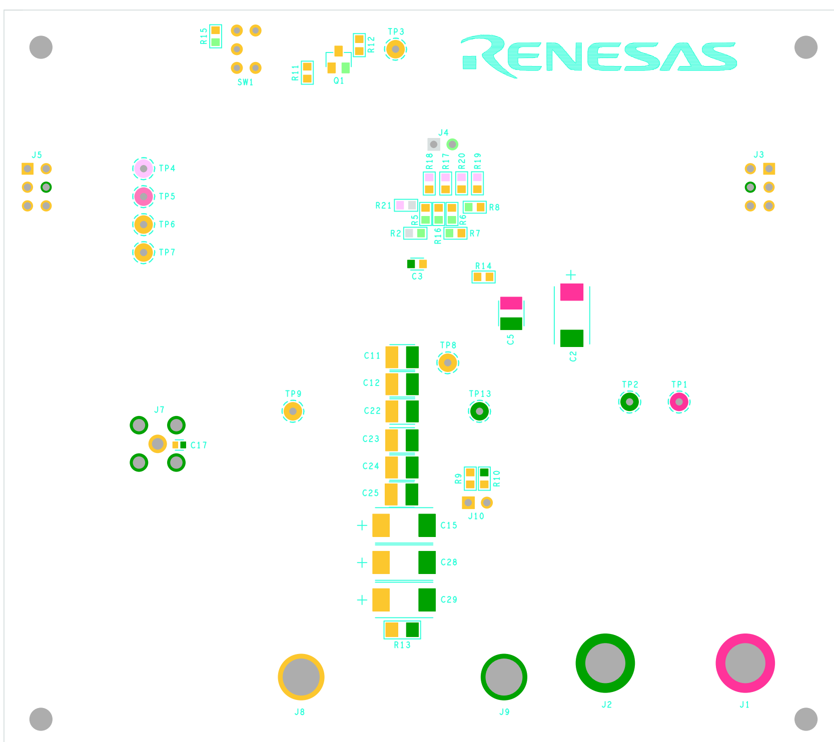

Figure 12. PCB - Silkscreen Bottom

5. Measured Data

The following data was acquired using an RTKA2108252H00000BU evaluation board.

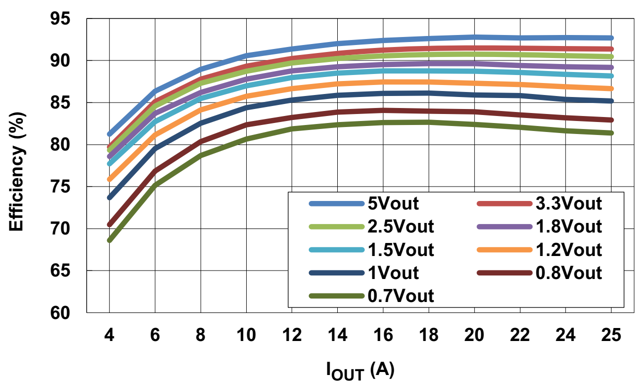

Figure 13. Efficiency vs Output Current at V_{IN} = 12V, f_{SW} = 364kHz for Various Output Voltages

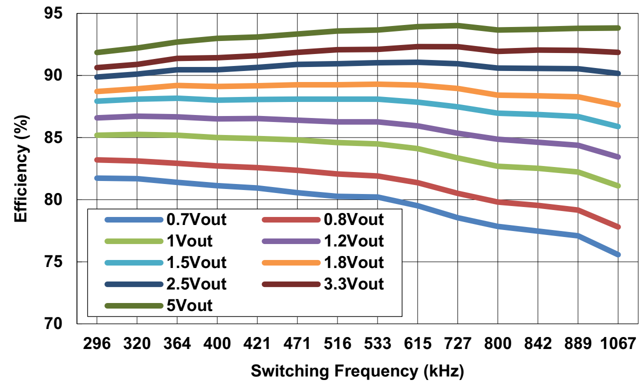

Figure 14. Efficiency vs Switching Frequency at V_{IN} = 12V, I_{OUT} = 25A for Various Output Voltages

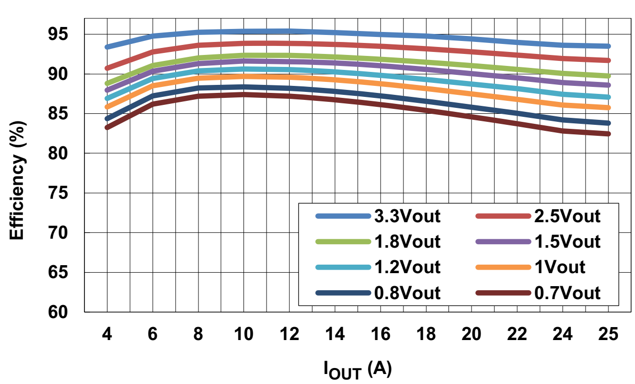

Figure 15. Efficiency vs Output Current at V_{IN} = 5V, f_{SW} = 364kHz for Various Output Voltages

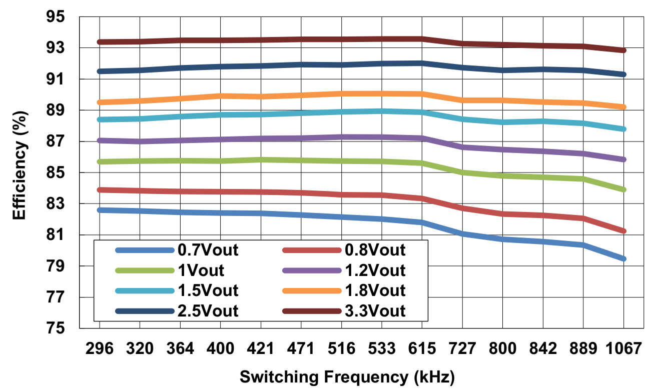

Figure 16. Efficiency vs Switching Frequency at V_{IN} = 5V, I_{OUT} = 25A for Various Output Voltages

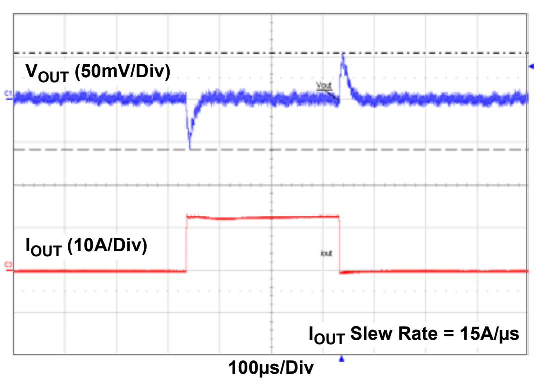

Figure 17. $12V_{IN}$ to $1.2V_{OUT}$ Transient Response, 364kHz, C_{OUT} = 10x100µF Ceramic + 2x470µF POSCAP, ASCR Gain = 250, Residual = 100

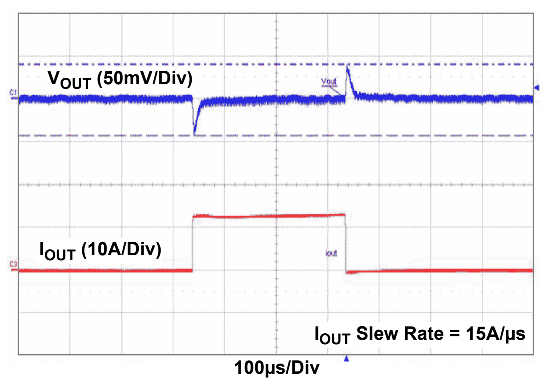

Figure 18. $12V_{IN}$ to $2.5V_{OUT}$ Transient Response, 615kHz, C_{OUT} = 4x100µF Ceramic + 1x470µF POSCAP, ASCR Gain = 250, Residual = 100

The following data was acquired using an RTKA2108252H00000BU evaluation board. **(Continued)**

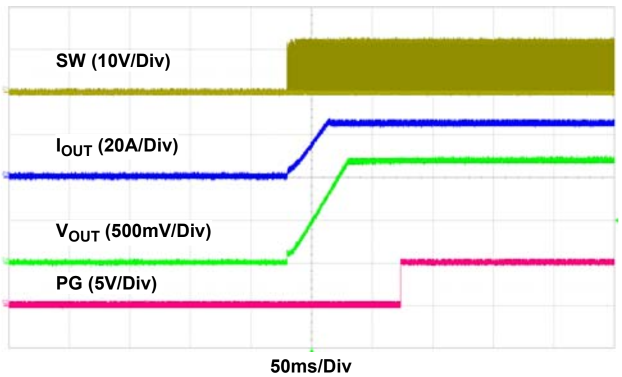

Figure 19. Startup at $12V_{IN}$, $1.2V_{OUT}$, 25A

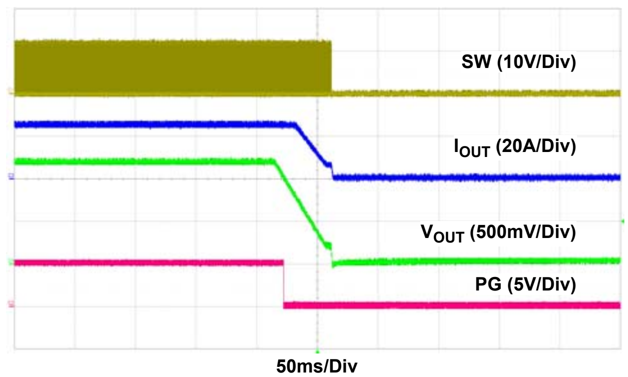

Figure 20. Soft-Off at $12V_{IN}$, $1.2V_{OUT}$, 25A

6. Revision History

Rev.	Date	Description
0.00	Sep 11, 2018	Initial release

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