RTKA214035DE0000BU

The RTKA214035DE0000BU evaluation board provides a simple platform to evaluate the 3.5×3.5mm 20-Ld QFN RAA214035 low-dropout linear regulator (LDO).

RAA214035 is ultra-low noise, high PSRR LDO regulators capable of sourcing up to 3A of load current with very low dropout. These LDOs' output voltage can be programmed from 0.5V to 3.65V by means of voltage setting pins on the IC in 50mV steps. The evaluation board has convenient jumpers to exercise these pins. For higher output voltage applications external feedback resistors can still be used allowing the output voltage to be programmed anywhere from 0.5V to 5.1V.

The LDO operate from an input voltage of 1.4V to 6.5V without VBIAS and 1.1V to 6.5V with VBIAS.

Features

- Output Voltage Set IC Pins easily programmed with JP_VSET
- Switch between Voltage Set IC pins or External Resistor Divider using jumper JP_FB
- Convenient shutdown mode function using Jumper JP_EN
- Power Good (PG) indication test point
- VBIAS banana jack or turret for applications where VIN < 1.4V
- BNC_VIN and BNC_VOUT connections for PSRR and output noise testing

Specifications

This evaluation board is specified for the following operating conditions:

- Input Voltage Range: 1.4V to 6.5V without VBIAS and 1.1V to 6.5V with VBIAS
- VBIAS Voltage Range: 3V to 6.5V Ultra-Low Output Noise: 7µVRMS

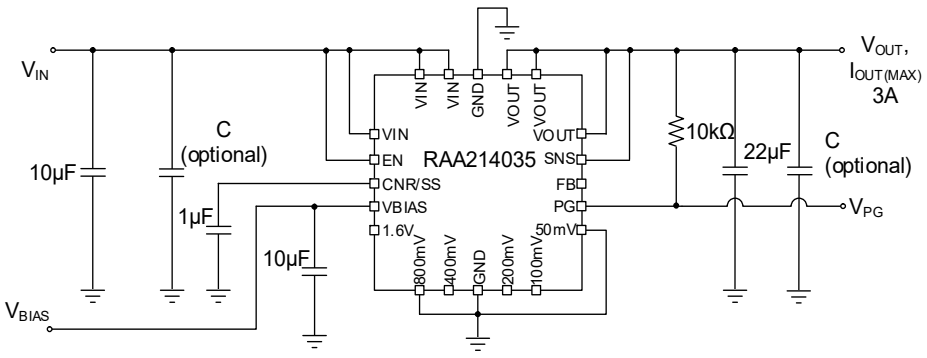

Figure 1. Typical Application Schematic

Contents

1. Functional Description

The RTKA214035DE0000BU evaluation board provides a simple platform to demonstrate the features of the RAA214035 low-noise, high-PSRR LDOs to help design and system engineers evaluate critical performance parameters for their application.

1.1 Setup and Configuration

1.1.1 Programming the Output Voltage

The output voltage can be programmed using the EVB PCB layout using convenient output voltage set IC pins (50mV, 100mV, 200mV, 400mV, 800mV, 1.6V) or with traditional external feedback (FB) resistors. To switch between the two configurations, use the 3-pin JP_FB jumper.

The RAA214035 has an output voltage range of 0.5V to 3.65V using internal FB resistors and an output voltage range of 0.5V to 5.1V using traditional external FB resistors.

1.1.2 Internal Feedback Resistors and Output Voltage Set Pins

The evaluation board can use the internal FB resistors by shorting the device VOUT pins to SNS using the JP_FB jumper (short pins 1 & 2).

The output voltage set pins on the PCB are labeled 50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V. Grounding these pins adds the voltages assigned to each grounded pin to the reference voltage (VREF), and the total equals the desired output voltage, as expressed in Equation 1. The VREF for the RAA214035 is 0.5V. The voltage set pins can be quickly grounded on the evaluation board using the J1 jumper.

(EQ. 1) $$V_{OUT} = V_{REF} + \sum(\text{GroundedOutputVoltageSetPins})$$

For example, to program the output voltage on the RAA214035 to 3.3V, ground the 400mV, 800mV, and 1.6V pins using the J1 jumper. The sum of these three pins (2.8V) added to the 0.5V voltage reference gives 3.3V on the output of the LDO. The schematic in Figure 2 illustrates the proper connections.

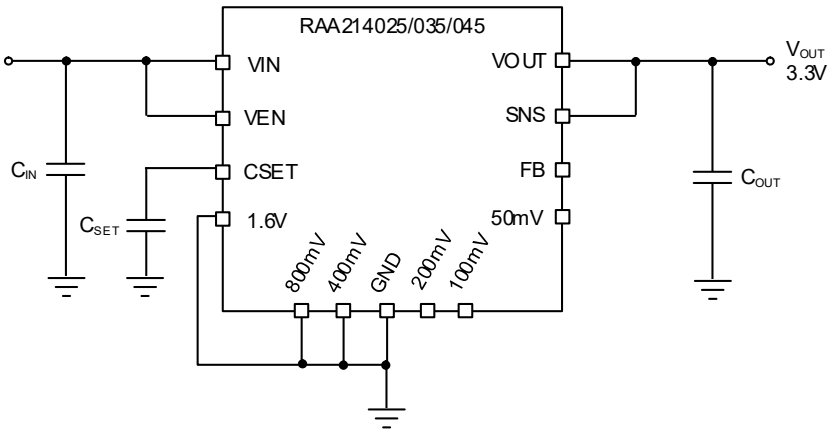

Figure 2. RAA214035 Simplified Schematic Using the Internal FB Resistors (V_{OUT} = 3.3V)

Table 1 provides a list of all the possible voltage set pin configurations and the corresponding output voltage for the RAA214035.

Table 1. Voltage Set Pin Configuration and Corresponding Output Voltages for the RAA214035 (V_{REF} = 0.5V)

V_{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V	V_{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V
0.50	Open	Open	Open	Open	Open	Open	2.1	Open	Open	Open	Open	Open	GND
0.55	GND	Open	Open	Open	Open	Open	2.15	GND	Open	Open	Open	Open	GND
0.60	Open	GND	Open	Open	Open	Open	2.2	Open	GND	Open	Open	Open	GND
0.65	GND	GND	Open	Open	Open	Open	2.25	GND	GND	Open	Open	Open	GND
0.70	Open	Open	GND	Open	Open	Open	2.3	Open	Open	GND	Open	Open	GND
0.75	GND	Open	GND	Open	Open	Open	2.35	GND	Open	GND	Open	Open	GND
0.80	Open	GND	GND	Open	Open	Open	2.4	Open	GND	GND	Open	Open	GND
0.85	GND	GND	GND	Open	Open	Open	2.45	GND	GND	GND	Open	Open	GND
0.90	Open	Open	Open	GND	Open	Open	2.50	Open	Open	Open	GND	Open	GND
0.95	GND	Open	Open	GND	Open	Open	2.55	GND	Open	Open	GND	Open	GND
1.00	Open	GND	Open	GND	Open	Open	2.60	Open	GND	Open	GND	Open	GND
1.05	GND	GND	Open	GND	Open	Open	2.65	GND	GND	Open	GND	Open	GND
1.10	Open	Open	GND	GND	Open	Open	2.70	Open	Open	GND	GND	Open	GND
1.15	GND	Open	Open	GND	Open	Open	2.75	GND	Open	GND	GND	Open	GND
1.20	Open	GND	Open	GND	Open	Open	2.80	Open	GND	GND	GND	Open	GND
1.25	GND	GND	Open	GND	Open	Open	2.85	GND	GND	GND	GND	Open	GND
1.30	Open	Open	Open	Open	GND	Open	2.90	Open	Open	Open	Open	GND	GND
1.35	GND	Open	Open	Open	GND	Open	2.95	GND	Open	Open	Open	GND	GND
1.40	Open	GND	GND	Open	GND	Open	3.00	Open	GND	Open	Open	GND	GND
1.45	GND	GND	GND	Open	GND	Open	3.05	GND	GND	Open	Open	GND	GND
1.50	Open	Open	GND	GND	GND	Open	3.10	Open	Open	GND	Open	GND	GND
1.55	GND	Open	GND	GND	GND	Open	3.15	GND	Open	GND	Open	GND	GND
1.60	Open	GND	Open	GND	GND	Open	3.20	Open	GND	GND	Open	GND	GND
1.65	GND	GND	Open	GND	GND	Open	3.25	GND	GND	GND	Open	GND	GND
1.70	Open	Open	Open	Open	GND	Open	3.30	Open	Open	Open	GND	GND	GND
1.75	GND	Open	Open	Open	GND	Open	3.35	GND	Open	Open	GND	GND	GND
1.80	Open	GND	Open	Open	GND	Open	3.40	Open	GND	Open	GND	GND	GND
1.85	GND	GND	GND	Open	GND	Open	3.45	GND	GND	Open	GND	GND	GND
1.90	Open	Open	GND	GND	GND	Open	3.50	Open	Open	GND	GND	GND	GND
1.95	GND	Open	GND	GND	GND	Open	3.55	GND	Open	GND	GND	GND	GND
2.00	Open	GND	GND	GND	GND	Open	3.60	Open	GND	GND	GND	GND	GND
2.05	GND	GND	Open	GND	GND	Open	3.65	GND	GND	GND	GND	GND	GND

1.1.3 External Feedback Resistors

For applications with an output voltage exceeding 3.65V, use an external feedback resistor divider (R_{TOP} and R_{BOT}) as shown in Figure 3. This layout extends the output voltage range for the LDO up to 5.1V.

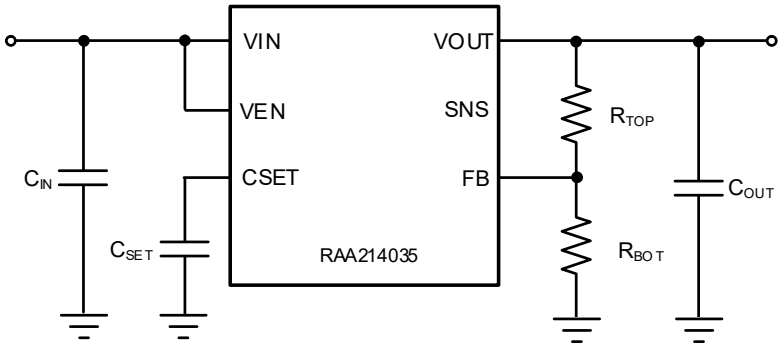

Figure 3. Simplified Schematic of LDO Using External FB resistors

The evaluation board can be configured to use the external FB resistors by shorting the VOUT PCB plane to the top of R_{TOP} using the JP_FB jumper (short pin 2 & 3).

R_{BOT} can be easily calculated to program the output voltage by setting R_{TOP} to a required resistor value and solving Equation 2 where $V_{OUT(TARGET)}$ is the ideal output voltage. The V_{REF} for RAA214035 is 0.5V.

(EQ. 2) $$R_{BOT} = R_{TOP} \times \left(\frac{V_{REF}}{V_{OUT(TARGET)} - V_{REF}} \right)$$

Use Equation 3 to calculate the output voltage based on the R_{TOP} and R_{BOT} resistors.

(EQ. 3) $$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}} \right)$$

Table 2 provides a non-exhaustive list of recommended FB resistor values to obtain some common output voltages for RAA214035. The FB resistors are commercially available in 1% tolerances.

Table 2. Recommended FB Resistor Values for Common Output Voltages (V_{REF} = 0.5V)

$V_{OUT(TARGET)}$ (V)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	$V_{OUT(CALCULATED)}$ (V)	Accuracy
0.5	0	DNP	0.500	0.00%
0.6	11.0	54.9	0.600	-0.03%
0.7	10.2	25.5	0.700	0.00%
0.75	10.0	20.0	0.750	0.00%
0.8	10.7	17.8	0.801	-0.07%
0.9	11.0	13.7	0.901	-0.16%
1	12.4	12.4	1.000	0.00%
1.05	11.0	10.0	1.050	0.00%
1.1	10.7	8.9	1.103	-0.29%
1.2	9.31	6.7	1.200	0.00%
1.5	12.4	6.19	1.502	-0.11%

Table 2. Recommended FB Resistor Values for Common Output Voltages (V_{REF} = 0.5V) (Cont.)

$V_{OUT(TARGET)}$ (V)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	$V_{OUT(CALCULATED)}$ (V)	Accuracy
1.8	10.2	3.92	1.801	-0.06%
1.9	12.4	4.42	1.903	-0.14%
2.5	12.4	3.09	2.506	-0.26%
3	12.4	2.49	2.990	0.33%
3.3	10.7	1.91	3.301	-0.03%
3.6	12.4	2.00	3.600	0.00%
4.2	12.1	1.64	4.189	0.26%
4.5	14.7	1.84	4.495	0.12%
5	12.4	1.38	4.993	0.14%
5.1	20.5	2.23	5.093	-0.09%

1.1.4 VBIAS

If the input supply voltage (VIN) is less than 1.4V but greater than 1.1V, use a VBIAS voltage of 3V to 6.5V. If the input voltage exceeds 1.4V, the VBIAS pin does not have to be connected and can be left floating or shorted to GND.

1.1.5 CNR/SS

Use a 1µF bypass capacitor between the CNR/SS pin and GND for optimal noise and ripple rejection performance. A minimum capacitance of 100nF is required for LDO stability.

1.1.6 VEN

The ENABLE feature of the LDOs can be exercised using the JP_EN jumper. Short the VEN pin to VIN to automatically ENABLE the device when VIN is applied.

To DISABLE the LDO, connect the EN pin to GND.

To control the EN pin with a separate power supply, such as a function generator or logic signal from an MCU, remove the jumper from JP_EN and connect the separate supply to the TP_EN turret.

1.2 Recommended Equipment

- A VIN power supply to power up the LDO. The supply should be able to supply the load current the LDO needs to supply to its load.
- An EN power supply such as a function generator, pulse generator, logic signal from an MCU, or a regular supply to power EN. If not using an external EN power supply, tie EN to VIN for automatic enabling.
- A VBIAS power supply to power VBIAS for applications where V_{IN} < 1.4V.
- An electronic load or resistor load.
- Measurement equipment such as multimeters, oscilloscopes, and spectrum analyzers to evaluate the LDO.

1.3 Quick Start Guide

1.3.1 Internal FB Resistor Configuration Start Guide

1. If not using an external supply on EN, skip step 6 and use the JP_EN jumper to short EN to VIN for automatic enabling.
2. Use the JP_FB jumper to short the SNS pin to VOUT.

3. Use jumpers to ground the required IC voltage set pins to obtain the required output voltage.
4. Twist the positive input lead and ground return lead from the input power supply together, forming a twisted pair power supply wire, and keep them as short as possible to minimize input inductance. Turn the supply off.
5. Connect the positive input lead of the VIN power supply to the VIN banana jack and the ground return lead to the GND_IN banana jack.
6. (Optional) Connect the positive input lead of the VEN power supply to the TP_EN turret and the ground lead to any input side GND, such as TP_10. Turn the supply off.
7. (Optional) Connect the positive input lead of the VBIAS power supply to the VBIAS banana jack, and the ground lead to the GND_VBIAS banana jack. Turn the supply off.
8. Connect the electronic or resistor load between VOUT and GND. The positive lead should be connected to the VOUT banana jack and the ground return lead should be connected to the GND_OUT banana jack.
9. Power up all the necessary power supplies followed by the load (if using an electronic load).
10. Verify the output voltage with a voltmeter and/or oscilloscope.

1.3.2 External FB Resistor Configuration Start Guide

1. If not using an external supply on EN, skip step 6 and use the JP_EN jumper to short EN to VIN for automatic enabling.
2. Use the JP_FB jumper to short the top of R_TOP to the VOUT plane.
3. Populate the R_TOP and R_BOT resistor divider to obtain the desired output voltage.
4. Twist the positive input lead and ground return lead from the input power supply together and keep them as short as possible to minimize input inductance. Turn the supply off.
5. Connect the positive input lead of the VIN power supply to the VIN banana jack and the ground return lead to the GND_IN banana jack.
6. (Optional) Connect the positive input lead of the VEN power supply to the TP_EN turret and the ground lead to any input side GND, such as TP_10. Turn the supply off.
7. (Optional) Connect the positive input lead of the VBIAS power supply to the VBIAS banana jack and the ground lead to the GND_VBIAS banana jack. Turn the supply off.
8. Connect the electronic or resistor load between VOUT and GND. The positive lead should be connected to the VOUT banana jack, and the ground return lead should be connected to the GND_OUT banana jack.
9. Power up all the necessary power supplies followed by the load (if using an electronic load).
10. Verify the output voltage with a voltmeter and/or oscilloscope.

2. Board Design

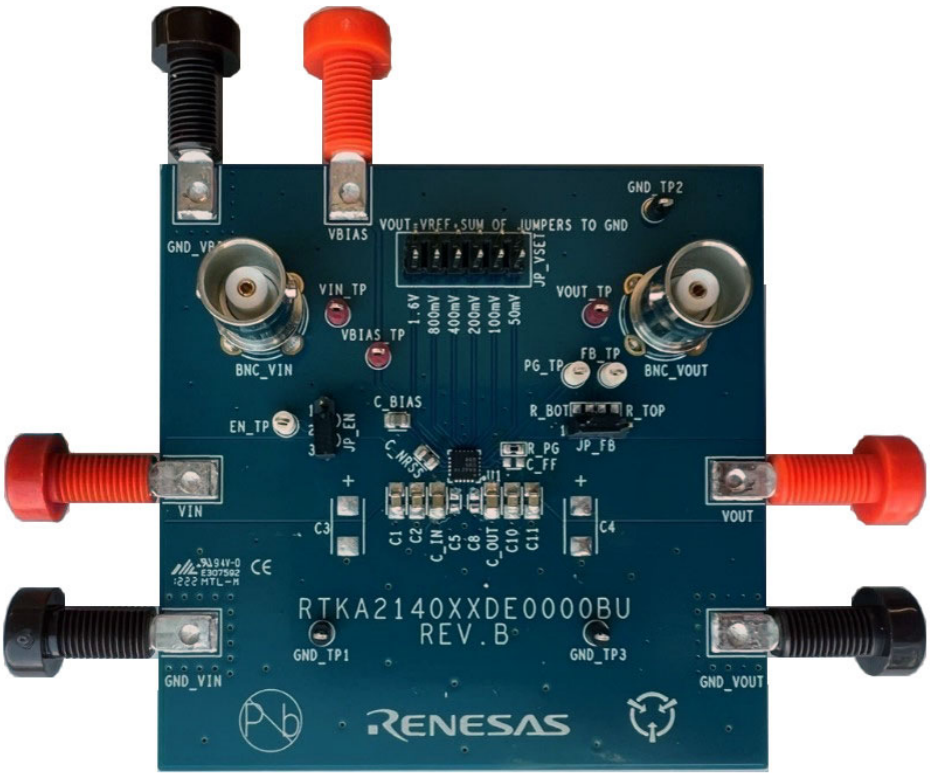

Figure 4. RTKA214035DE0000BU Evaluation Board (Top)

2.1 PCB Layout Guidelines

The following are recommendations for the PCB layout to achieve optimal LDO performance:

- Ensure the input and output capacitors have a good ground connection and place them as close to the IC as possible.
- The FB pin trace should be short, direct, and away from other noisy traces.
- If using external FB resistors, place them as close as possible to the IC.
- The package thermal EPAD is the largest heat conduction path for the package. Solder it to a copper pad on the PCB underneath the part. The PCB thermal pad should have as many plated vias as possible to increase the heat flow from the package thermal EPAD to the inner PCB areas and/or the bottom PCB area. Add thermal vias around the PCB package to help improve heat spread from the package to other board layers. Keep the vias small but not so small that their inside diameter prevents the solder from wicking through the holes during reflow. For efficient heat transfer, the vias must have low thermal resistance. Do not use thermal relief patterns to connect the vias. It is essential to have a complete connection of the plated through-hole to each plane. The top copper GND layer that the EPAD is connected to is the least thermally resistant path for heat flow. To this end, minimize the components and traces that cut this layer.

2.2 Schematic Diagrams

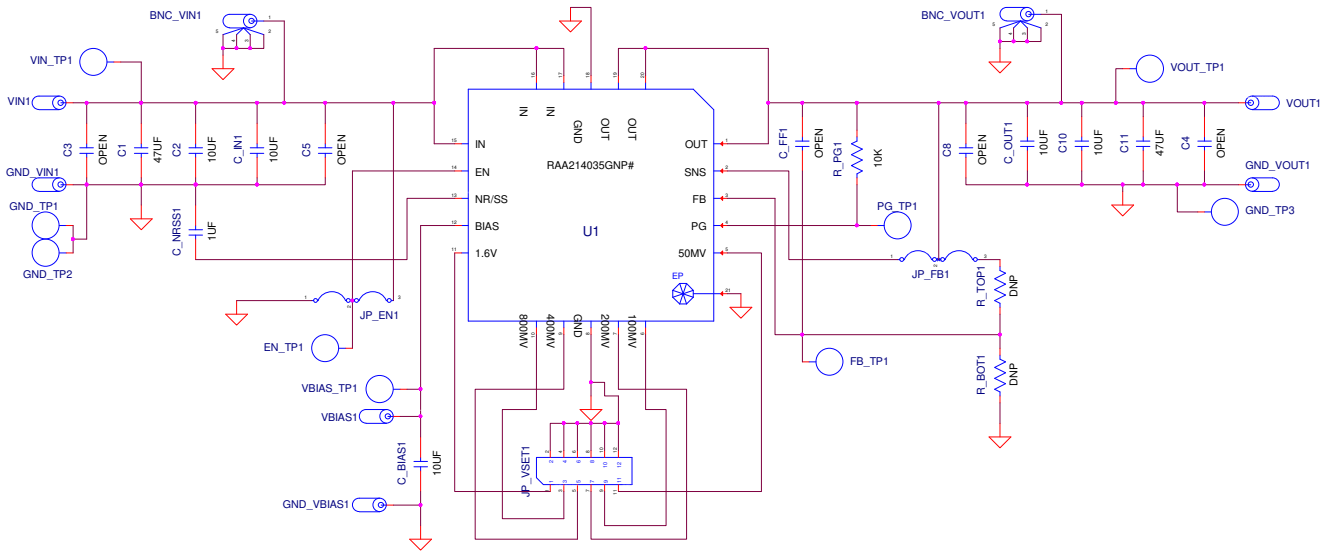

Figure 5. RTKA214035DE0000BU Schematic Diagram

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
5	C_BIAS, C_IN, C_OUT C2, C10	CAP, SMD, 0805, 10µF, 16V, 10%, X7R, RoHS	Samsung	CL21B106KOQNNNE
2	C1, C11	CAP, SMD, 0805, 47µF, 10V, 20%, X5R, RoHS	Murata	GRM21BR61A476ME15
0	C_FF	CAP, SMD, 0603, DNP-PLACE HOLDER, RoHS	-	-
1	C_NRSS	CAP, SMD, 0805,1µF, 16V, 10%, X7R, RoHS	Kemet	C0805C105K4RACTU
0	C3, C4	CAP, SMD, 1206, DNP-PLACE HOLDER, RoHS	-	-
0	C5, C8	CAP, SMD, 0603, DNP-PLACE HOLDER, RoHS	-	-
3	VIN, VOUT, VBIAS	CONN-BANANA JACK, INSULATED, ORANGE, NYLON, RoHS	Johnson Components	108-0906-001
3	GND_VIN, GND_VOUT, GND_VBIAS	CONN-BANANA JACK, FE MALE, TH, W/SOLDER TABS, BROWN, RoHS	Cinch	108-0908-001
2	BNC_VIN, BNC_VOUT	CONN-BNC, RECEPTACLE, TH, 4 POST, 50Ω, GOLDCONTACT, RoHS	Amphenol	31-5329-52RFX
3	VIN_TP, VOUT_TP, VBIAS_TP	CONN-MINI TEST PT, VERTICAL, RED, RoHS	Keystone	5000
3	GND_TP1-GND_TP3	CONN-MINI TEST PT, VERTICAL, BLK, RoHS	Keystone	5001
3	EN_TP, FB_TP, PG_TP	CONN-MINI TEST POINT, VERTICAL, WHITE, RoHS	Keystone	5002
1	JP_VSET	CONN-HEADER,2×6, BRKAWY-2×36,2.54mm, RoHS	BERG/FCI	67996-272HLF

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
2	JP_EN, JP_FB	CONN-HEADER,1×3, BREAKAWY 1×36,2.54mm, RoHS	BERG/FCI	68000-236HLF
0	R_BOT, R_TOP	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER	-	-
1	R_PG	RES, SMD, 0603,10K, 1/10W, 1%, TF, RoHS	Venkel	CR0603-10W-1002FT
1	U1	RAA214020 LDO, 20-QFN, Ultra Loise Noise High PSSR LDO	Renesas	RAA214035GNP

2.4 Board Layout

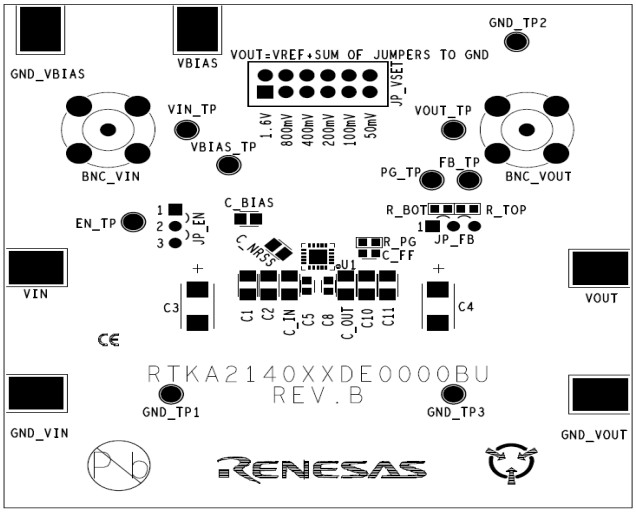

Figure 6. Assembly Layer

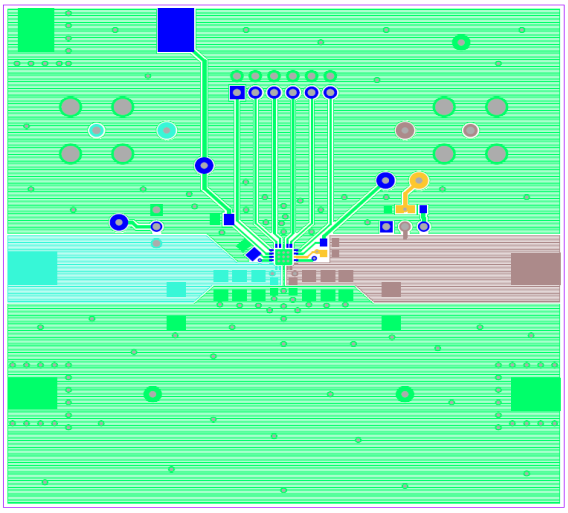

Figure 7. Top Layer

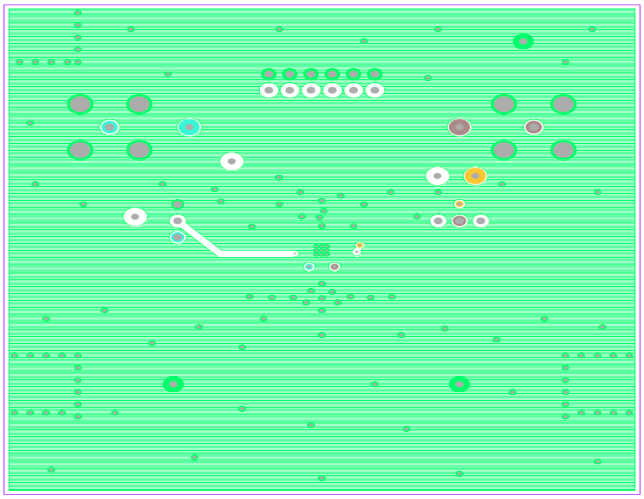

Figure 8. Second Layer

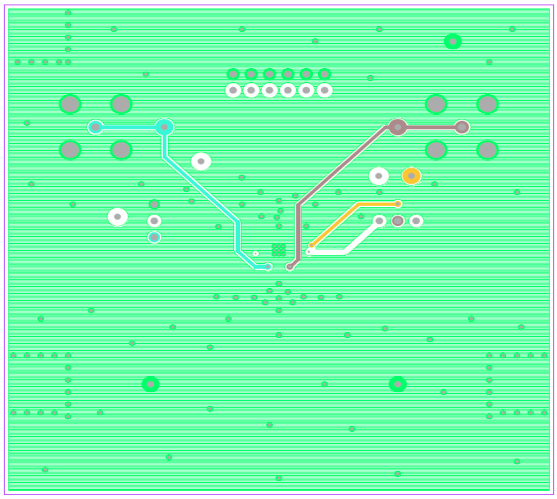

Figure 9. Third Layer

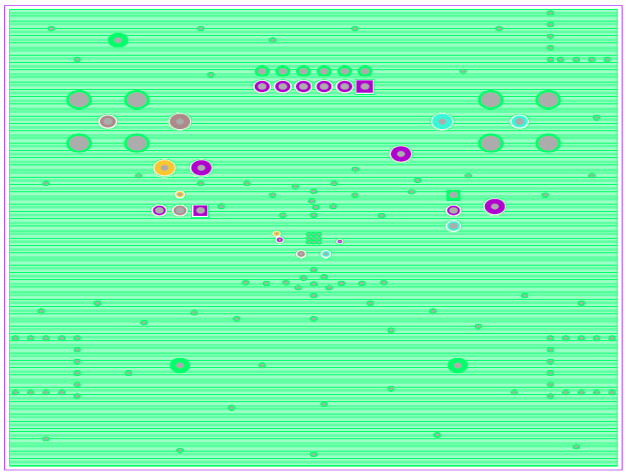

Figure 10. Bottom Layer

3. Typical Performance Graphs

Operating conditions unless otherwise noted: TA = 25°C, VBIAS = open, and PG pulled up to VIN with 10kΩ. Typical values are at T_A = +25°C, unless otherwise specified.

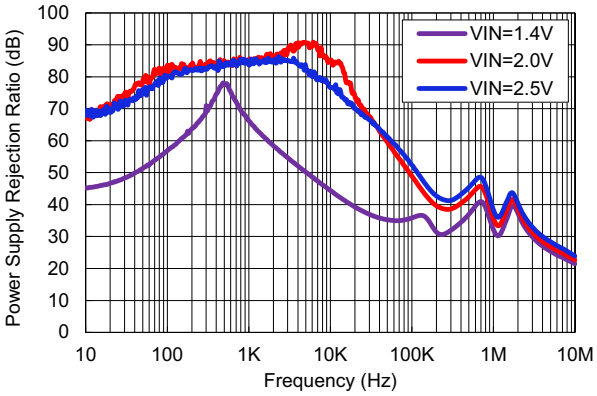

Figure 11. PSRR vs Frequency for Various V_{IN} (I_{OUT} = 1A, V_{OUT} = 0.5V, $C_{NR/SS}$ = 0.1µF)

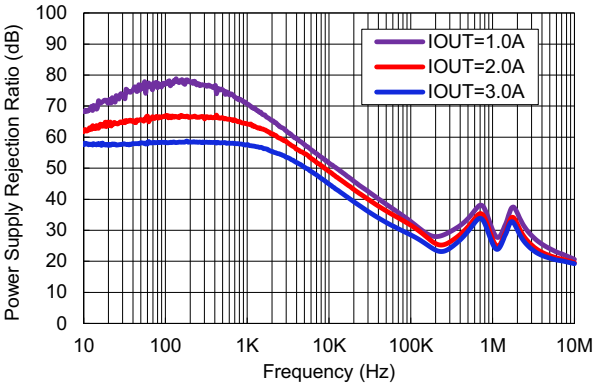

Figure 12. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 1.1V, V_{OUT} = 0.8V, V_{BIAS} = 5V, $C_{NR/SS}$ = 0.1µF)

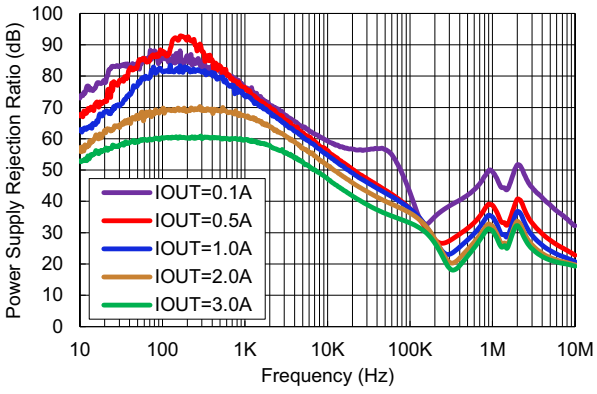

Figure 13. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 3.7V, V_{OUT} = 3.3V, $C_{NR/SS}$ = 0.1µF)

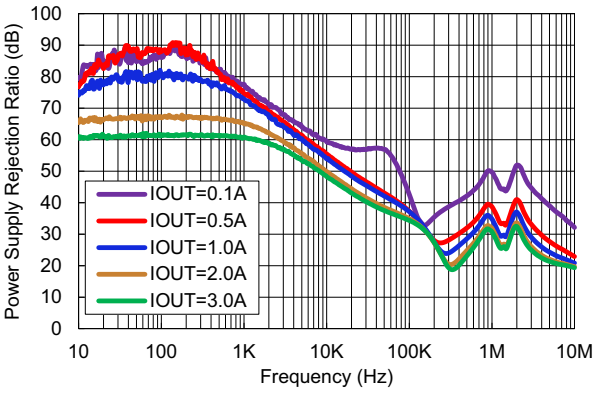

Figure 14. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 3.7V, V_{OUT} = 3.3V, $C_{NR/SS}$ = 1µF)

4. Ordering Information

Part Number	Description
RTKA214035DE0000BU	RAA214035 Evaluation Board

5. Revision History

Revision	Date	Description
1.00	Jan 29, 2023	Initial release

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