RTKA236100DE0010BU

RAA236100 Evaluation Board

The evaluation board (RTKA236100DE0010BU) is a platform for evaluating the functionality and performance of the RAA236100 regulator in DFN packages. The RAA236100 is an highly efficient and integrated synchronous buck-boost regulator featuring an ultra-low input quiescent current of 130nA and down to <22nA when disabled. The evaluation board provides access to the regulator switching node, inductor current, input current, input/output voltages, and other control lines. Furthermore, changing many operating characteristics and access the internal registers using the onboard I^2C interface is available.

Features

- Small and compact design.
- I^2C interface for programmable V_{OUT}, slew rate and various operation modes (Forced Bypass, Auto-PFM, Forced PWM)
- Connectors, test points, and jumpers for easy probing.

Specifications

The board is designed to operate at the following operating conditions:

- Input voltage range: 1.8V to 5.5V
- Programmable output voltage range of 1.8V to 5.0V and selectable forced bypass power saving mode
- Up to 400mA output current (V_{IN} > 2.5V, V_{OUT} = 3.3V)
- Operating temperature range: -40°C to +85°C

Board Contents

- EVB PCB assembly
- Mini USB I^2C dongle with USB cable (ISLUSBMINIEVAL1Z)

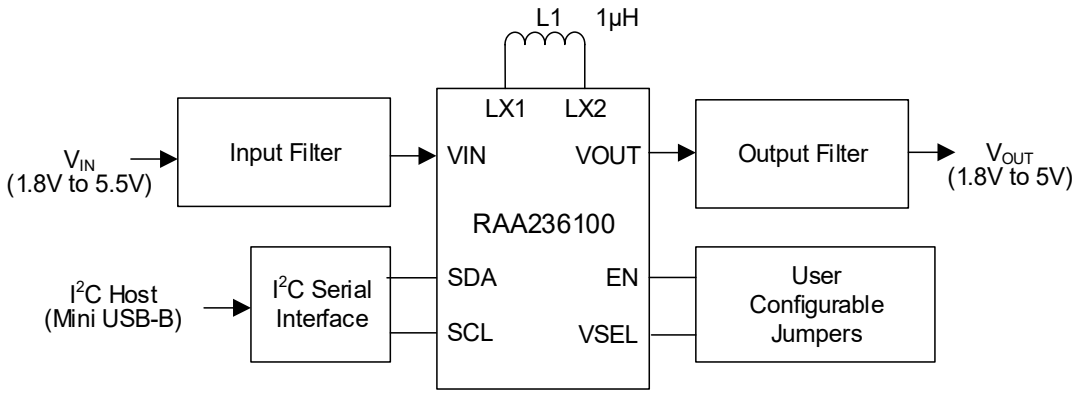

Figure 1. EVB Block Diagram

Contents

1. Functional Description

The evaluation board provides a default output voltage of 3.3V at startup, which then can be reconfigured using I^2C as described in the later section. Special pin posts are provided for connecting the input supply and load, along with S+/S- pins which provide voltage sense points close to the IC pins for accurate measurements. The evaluation board is shown in Figure 7. Pin connectors, test points, and jumpers along with their descriptions are listed in Table 1.

Table 1. Description of Connectors, Test Points and Jumpers for RTKA236100DE0010BU

Test Points	Description
TP1, TP4 (VIN, GND)	Input supply power connections.
TP2, TP3 (S+, S-)	Kelvin connection for input voltage measurement.
TP5, TP8 (VOUT, GND)	Output voltage (load) power connections.
TP6, TP7 (S+, S-)	Kelvin connection for output voltage measurement.
TP28	BYPASS Input (Buck-boost forced bypass control input)
TP9	VSEL input pin (Fast DVS input to select different targets for the output voltage).
TP10	EN input pin (Active high device enable input).
TP12, TP14	SCL and SDA I^2C bi-directional serial data
TP13 and TP24	I^2C High side and low side voltages HV_SUPPLY and LV_SUPPLY
TP19, TP22	SUPPLY_LOAD and PGND_LOAD (connection pins for the transient circuit power rail)
TP15	V_EXT (connection pin for external supply for when an external pullup is selected).
TP21	+IN (positive pin connection for function generator, to control the transient circuit).
TP20	Connection point for load transient circuit
TP23	VOUT coaxial pin connection for lower noise output voltage measurement.
J1, J2	LX1 and LX2 (switching nodes monitoring test points for input and output sides of the inductor respectively (buck and boost nodes respectively).
J3	Header connector for monitoring SCL, VSEL, and SDA
J4	Mini USB I^2C dongle connector (for use with ISLUSBMINIEVAL1Z).
J6	Jumper connection/configuration for VSEL to VPULLUP or to GND
J7	Jumper connection/configuration for EN to VPULLUP or to GND
J8	Jumper connection/configuration for VPULLUP to VIN or V_EXT
J22	Jumper connection/configuration for BYPASS to VPULLUP or GND
J21	Header pin connection for +IN and GND.
J17	Connects SCL to SCL_LV (closed)
J18	Connects SDA to SDA_LV (closed)
JP1	Connects SCL to a pull-up resistor
JP2	Connects SDL to a pull-up resistor
TP16, TP17, TP18, TP25, TP26, TP27	Supplementary ground plane (GND) connections

Note: The DFN Package provides an exposed pad to optimize thermal performance, which must be soldered to the PCB ground plane.

1.1 Operational Characteristics

The input voltage range of the evaluation board, which matches the RAA236100 device, is 1.8V to 5.5V. The output voltage range is adjustable from 1.8V to 5.0V. The maximum load that can be applied is 400mA, which is not achievable at all input/output voltage conditions. The corresponding input/output operating load range is shown in Figure 2.

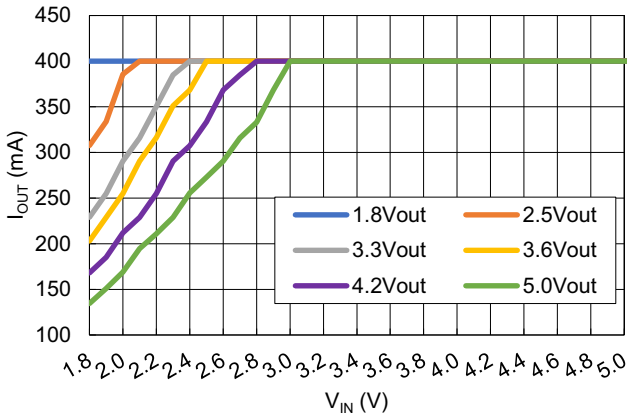

Figure 2. Input/Output operating load range

The operating ambient temperature range of the boards is -40°C to +85°C.

1.2 Setup and Configuration

1.2.1 Power Supply and Load

1. Connect a power supply to VIN (TP1) and GND (TP4), and set the voltage to 3.6V. Keep the power supplies off until all connections are complete.
2. If using an external power supply for the pull-up voltage, connect a power supply to V_EXT (TP15) and GND (TP27), and set the voltage to 1.8V. Ensure J8 is set to the upper position in this case.
3. If using the load transient circuit, connect a power supply to SUPPLY_LOAD (TP19) and PGND_LOAD (TP22), and set the voltage to 5.0V.
4. As a precaution, set current limits on the power supplies. For example: VIN (1A), V_EXT (100mA), and SUPPLY_LOAD (1A).
5. Connect an electronic load to VOUT (TP5) and GND (TP8), and set the load to constant current at 0A.
6. Connect DMM or Oscilloscope probes to monitor the input voltage (S+/S-; TP2/TP3), output voltage (S+/S-; TP6/TP7 - or VOUT; TP23), and inductor switching nodes (LX1/LX2; J1/J2).
7. Turn on the power supplies in any sequence.

At power-on with a supply voltage of 3.6V, the expected power up waveform is shown in Figure 3.

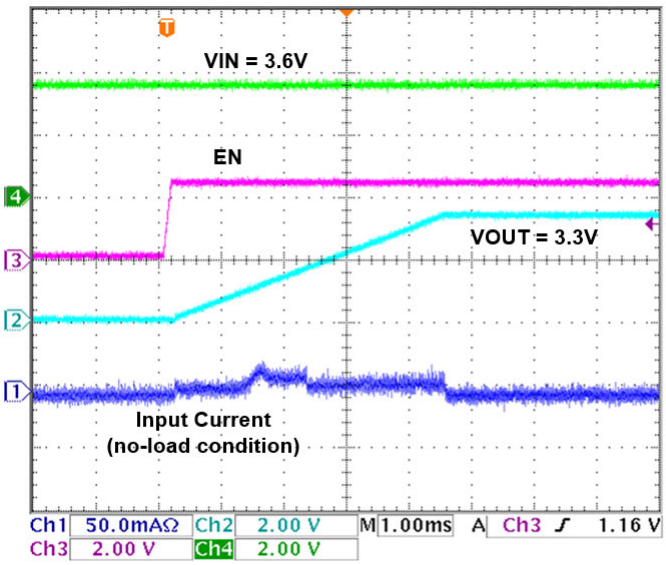

Figure 3. Startup Illustration Waveform

1.2.2 Evaluation Software and GUI

The evaluation boards operate without running the RAA236100 evaluation software. For enhanced access and register read/write, the RAA236100 evaluation software and manual are available for download from the RAA236100 board page on the Renesas website. Save the software file and install the software by double clicking on the file name and follow the on-screen instructions.

1. Before proceeding, power off all supplies.
2. Attach the USB I²C interface dongle to the computer using the supplied USB cable (dongle is connected using J4).
3. Run the RAA236100 evaluation software. When the evaluation software launches, connect the power supply, DC load, and any other test and measurement equipment to the evaluation board, and then reapply power.

The GUI provides read and write access to the registers. The GUI is organized through tabs, showing controls for the buck-boost regulator output, fault configuration and status, and general configuration settings. A screenshot for the main GUI window is shown in Figure 4.

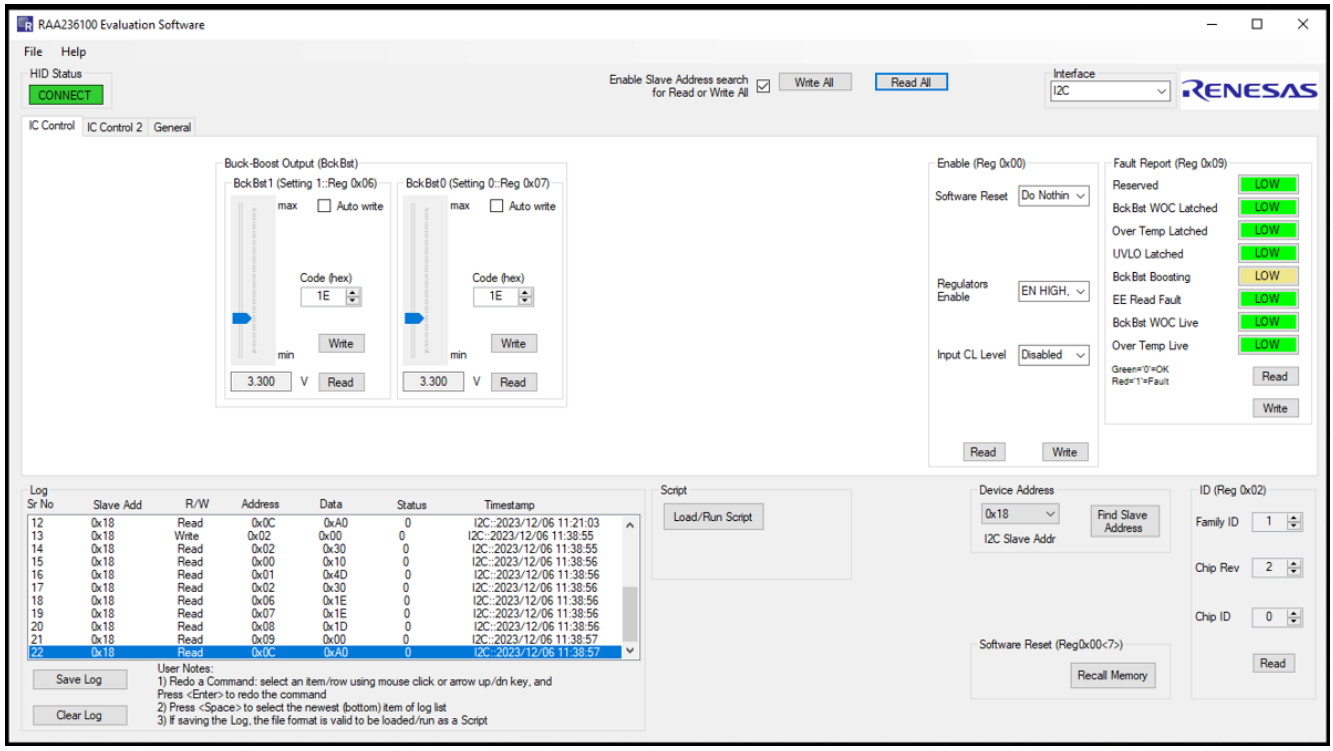

Figure 4. GUI Main IC Control Window

The following is a quick guide to explore the available GUI features to monitor and control the PMIC. Refer to the datasheet before proceeding.

1. After powering on the board and connecting the USB cable to the host computer, click on the **Find Slave address** button to identify the I^2C slave address.
2. On the **IC Control** Tab, the **Register ID** panel (Address: 0x02) provides chip identification information. This is a read-only register, and the read button in this panel only reads the information in this register.
3. To change the output voltage, you can use the **BckBst0** (Address: 0x07) panel slider or enter the Hex code (0x00 to 0x40) to adjust the output (from 1.8V to 5.0V, steps of 0.05V). **BckBst0** sets the output voltage target when the VSEL pin is low. Click the **Read** button to apply. A read operation can be performed for this register to read the contents beforehand, if required.
4. Register **BckBst1** (Address: 0x06) sets the output voltage target when the VSEL pin is high. Similarly, to edit the register value, use the panel slider or enter the Hex code (0x00 to 0x40) to adjust the output (from 1.8V to 5.0V, with steps of 0.05V).
5. The **Fault Report Register** (Address: 0x09) shows the status of various available fault registers. When low (Green), no fault is detected, and when high (RED), a fault is registered:
   - BckBst WOC Latched Bit – Latched if overcurrent protection is triggered.
   - Over Temp Latched Bit – Latched if way over-temperature is triggered.
   - UVLO Latched Bit – Latched if V_{IN} UVLO comparator is triggered.
   - BckBst Boosting Bit – This bit is high when V_{OUT} is 0.4V above V_{IN}, which indicates the regulator is in Boost operation.
   - EE Read Fault Bit – Latched if EPROM read fails at startup.
   - BckBst WOC Live Bit – This bit indicates the live status of the way overcurrent comparator.
   - Over Temp Live Bit – this bit indicates the live status of the way over-temperature comparator.

Note: High (Red) bits can be cleared by clicking on the button to flip the color to green, and then clicking **write**.

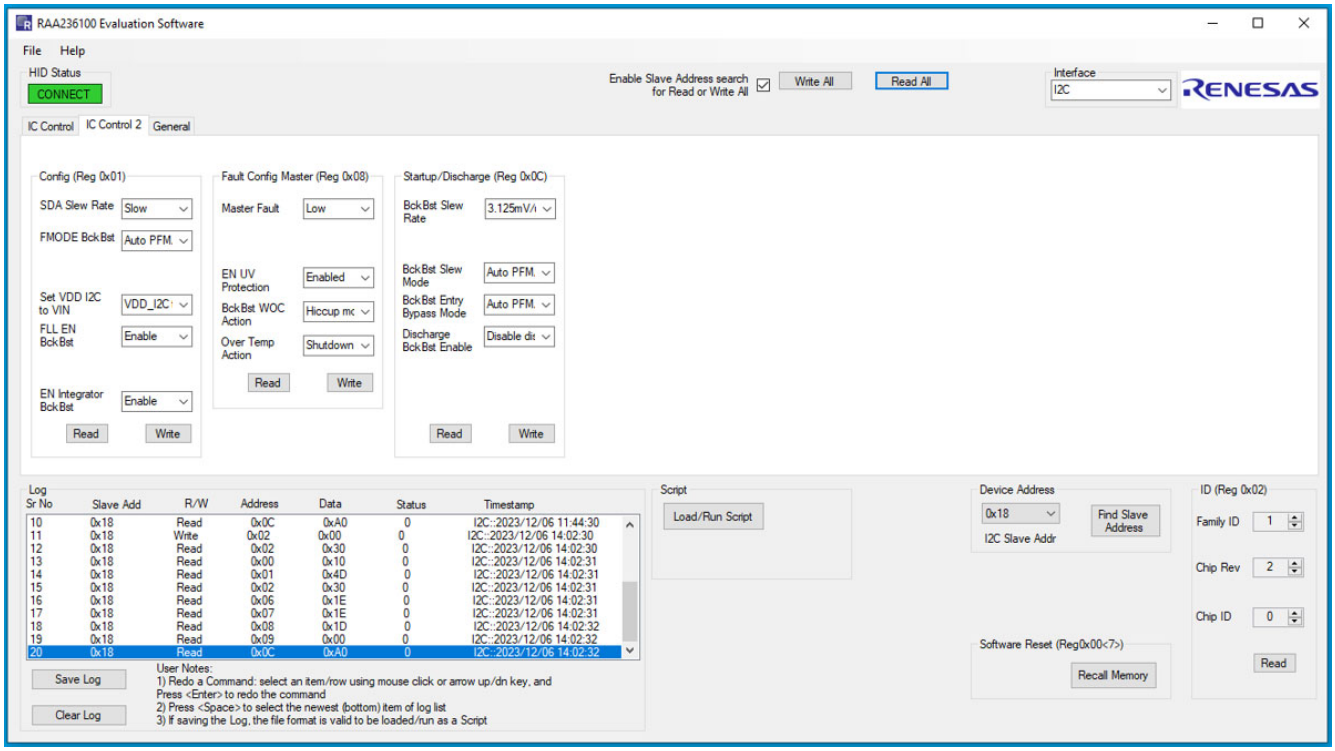

Figure 5. GUI IC Control 2 Tab

6. On the **IC Control 2** Tab, the **Config** Register (Address: 0x01) panel has controls for the following:
   - SDA Slew Rate – To adjust the SDA falling time depending the I^2C mode (Standard, Fast, Fast plus, and High speed etcetera), pick for the drop-down menu (slowest, slow, fast, or fastest).
   - FMODE BckBst – Select the buck-boost operating mode from the drop-down menu (auto PFM/PWM, auto PFM/PWM with ultrasonic mode enabled, forced PWM, or bypass mode).
   - Set VDD I2C to VIN – Select from the drop-down list if VDD_I2C is connected to a fixed 1.8V/3.3V rail, or if it is pulled up to VIN.
   - FLL EN BckBst – Select from the drop-down list to enable or disable the frequency control loop (FLL). When enabled, this locks the frequency to 2MHz in PWM mode, and Ton + Toff = 1/2MHz in PFM mode.
   - EN Integrator BckBst – Enables the buck-boost error amplifier integrator. when disabled, it is a Type-I error amplifier for best transient response, and when enabled it is a Type-II error amplifier for best DC accuracy.
7. The **Fault Config Master** Register (Address: 0x08) panel has controls for the following:
   - Master Fault – Goes high if any of the latched faults transition from 0 to 1.
   - EN UV Protection – Enable undervoltage protection. The action is defined by the following **BckBst WOC Action** register.
   - BckBst WOC Action – Select from the drop-down menu (no action, hard shutdown, hiccup mode with discharge resistor enabled, or hiccup mode with discharge resistor disabled).
   - Over Temp Action – Select from the drop-down menu (shut down and restart when cooled with discharge resistor enabled, shutdown and restart when cooled with discharge resistor disabled, or hard shutdown).
8. The **Startup/Discharge** Register (Address: 0x0C) panel has controls for the following:
   - BckBst Slew Rate – Buck-boost soft start and slew rate between levels. Select from the drop-down list (0.78125mV/µs, 1.5625mV/µs, 3.125mV/µs, or 6.25mV/µs).

- BckBst Fast DVS – Multiplier for soft start and slew rate between levels. Select from the drop-down list (1x, 2x, 4x, or 8x).
- BckBst Slew Mode – Select between Auto PFM/PWM and FPWM when V_{OUT} is slewed down. If FPWM is selected, this allows for a faster ramp down rate if no load is applied.
- BckBst Entry Bypass Mode – Select between Auto PFM/PWM and FPWM in Bypass mode when V_{OUT} is slewed down.
- Discharge BckBst Enable – Enable or Disable the discharge resistor. *Note*: The discharge resistor is disabled independently when V_{IN} goes below the internal POR level.

9. The **General** tab contains ancillary controls to help user interaction with the IC, dongle, and GUI. Refer to the evaluation software manual for further information.

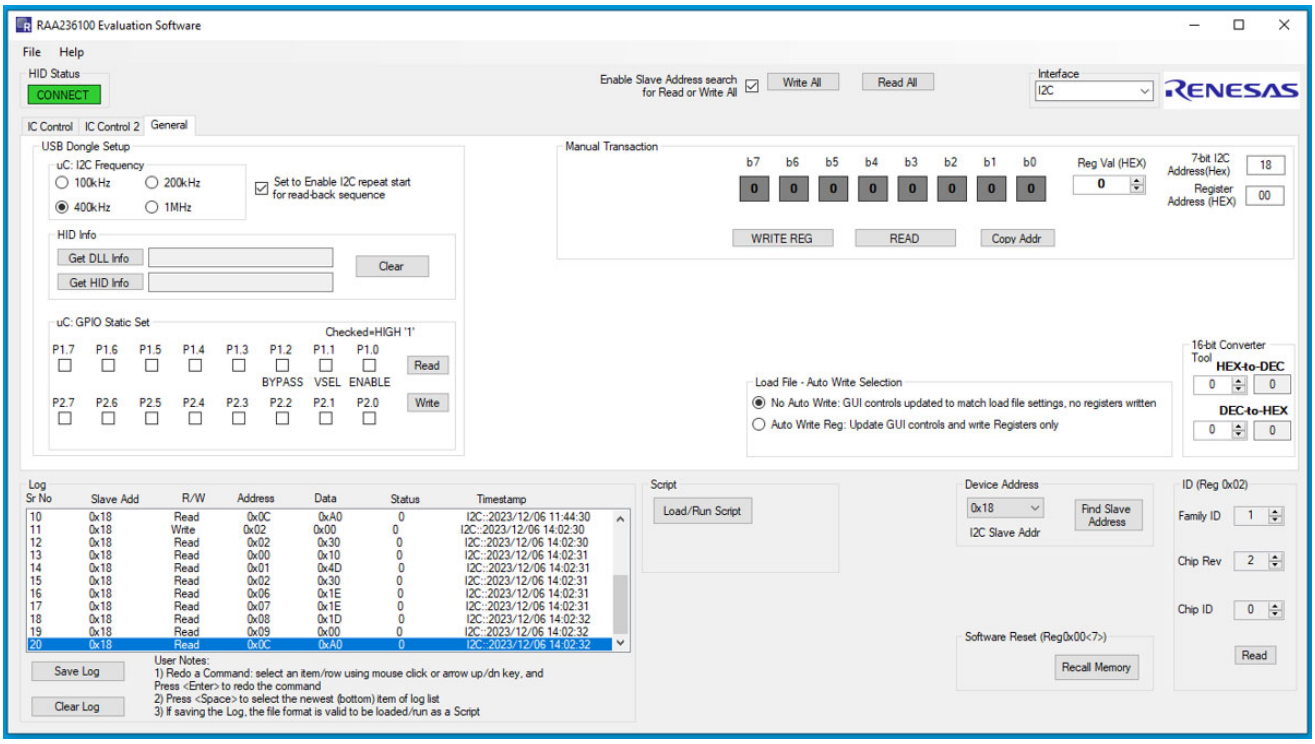

Figure 6. GUI General Tab

1.2.3 Startup Voltage and Pin Reader

The startup voltage for the I²C variant of this regulator is determined using the voltage setting registers bckBst_0 (address: 0x07) and bckBst_1 (address: 0x06). The dedicated voltage selection pin (VSEL) is used to select which register value is used, with the target taken from bckBst_0 when VSEL is low, and bckBst_1 when high. The startup voltage can be initially changed by altering the voltage setting value and then setting the enable pin to high.

2. Board Design

2.1 RTKA236100DE0010BU (DFN)

2.1.1 Board Image

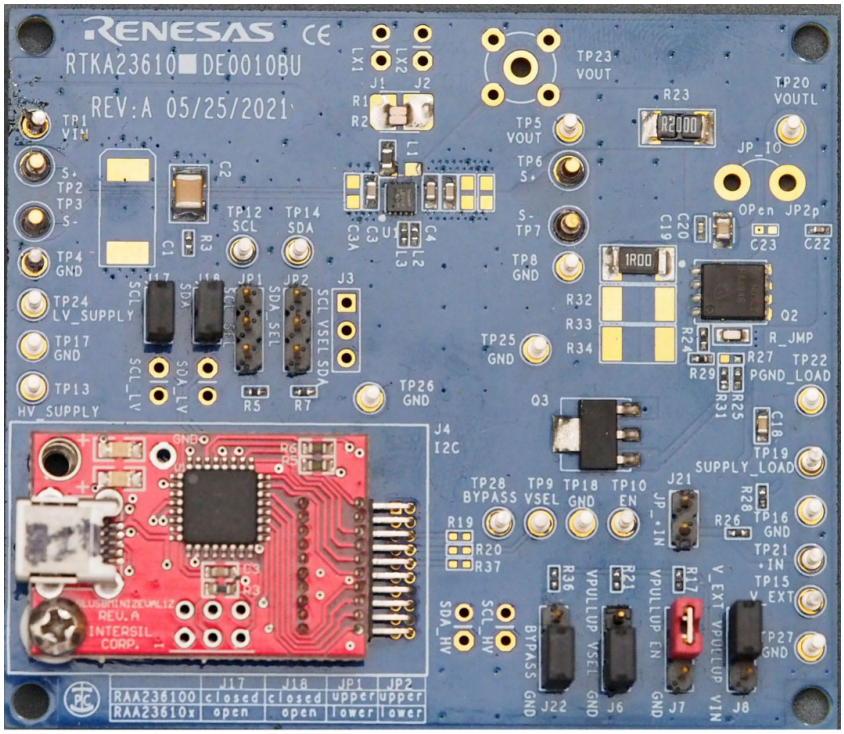

Figure 7. RTKA236100DE0010BU Evaluation board (Top)

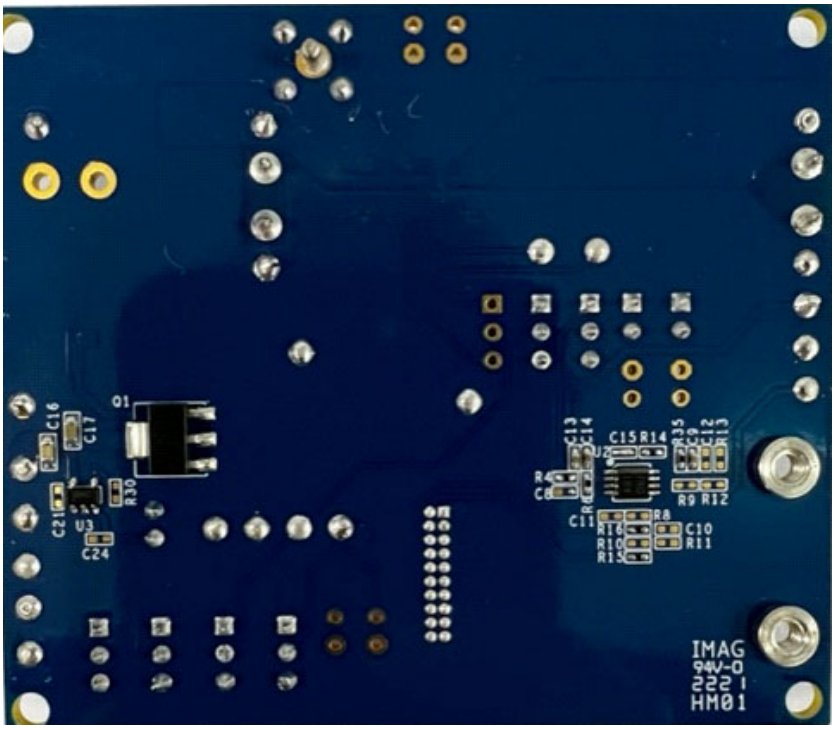

Figure 8. RTKA236100DE0010BU Evaluation board (Bottom)

2.1.2 Schematic Diagram

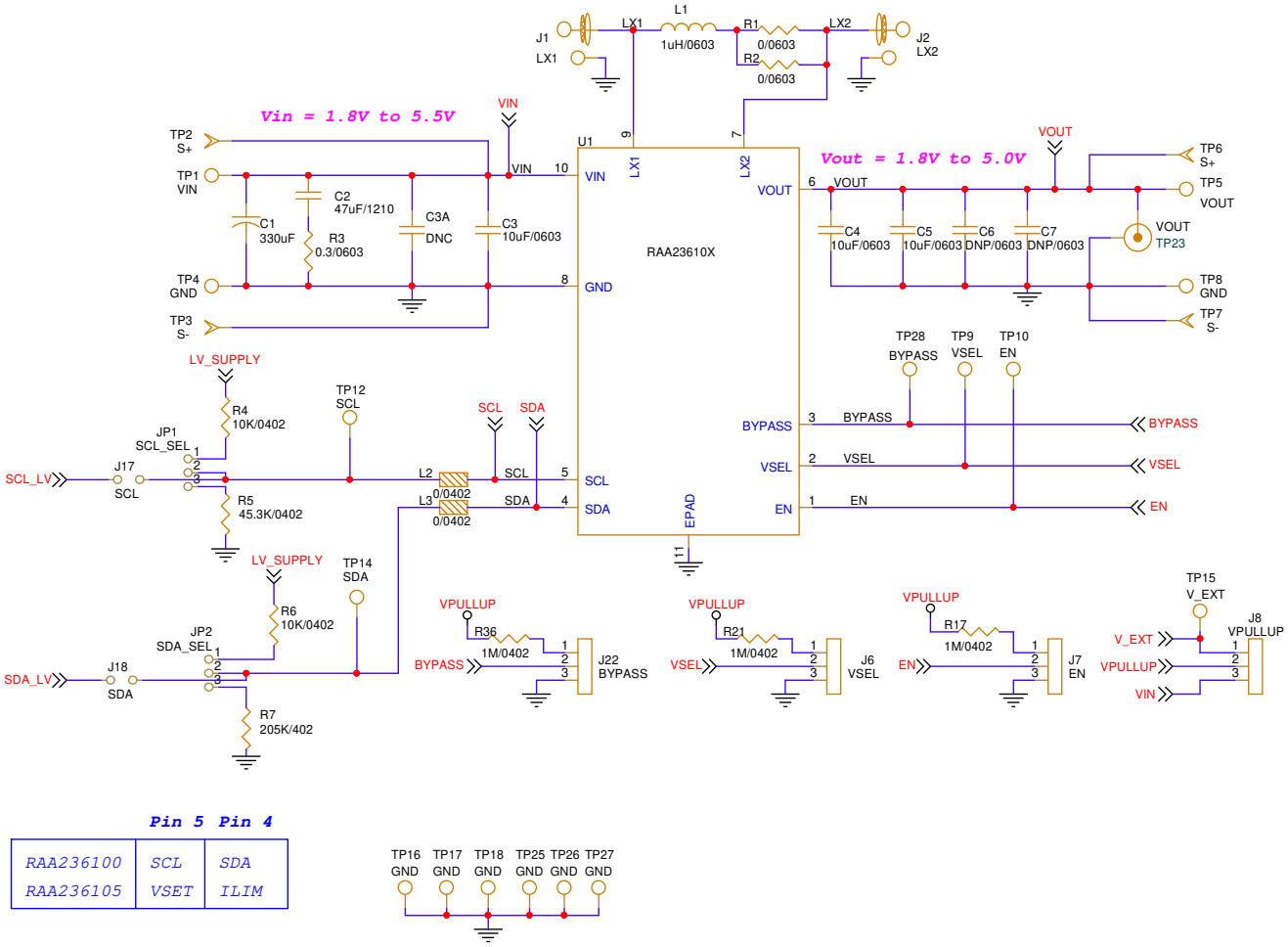

Figure 9. RTKA23610xDE0010BU Schematic - Page 1

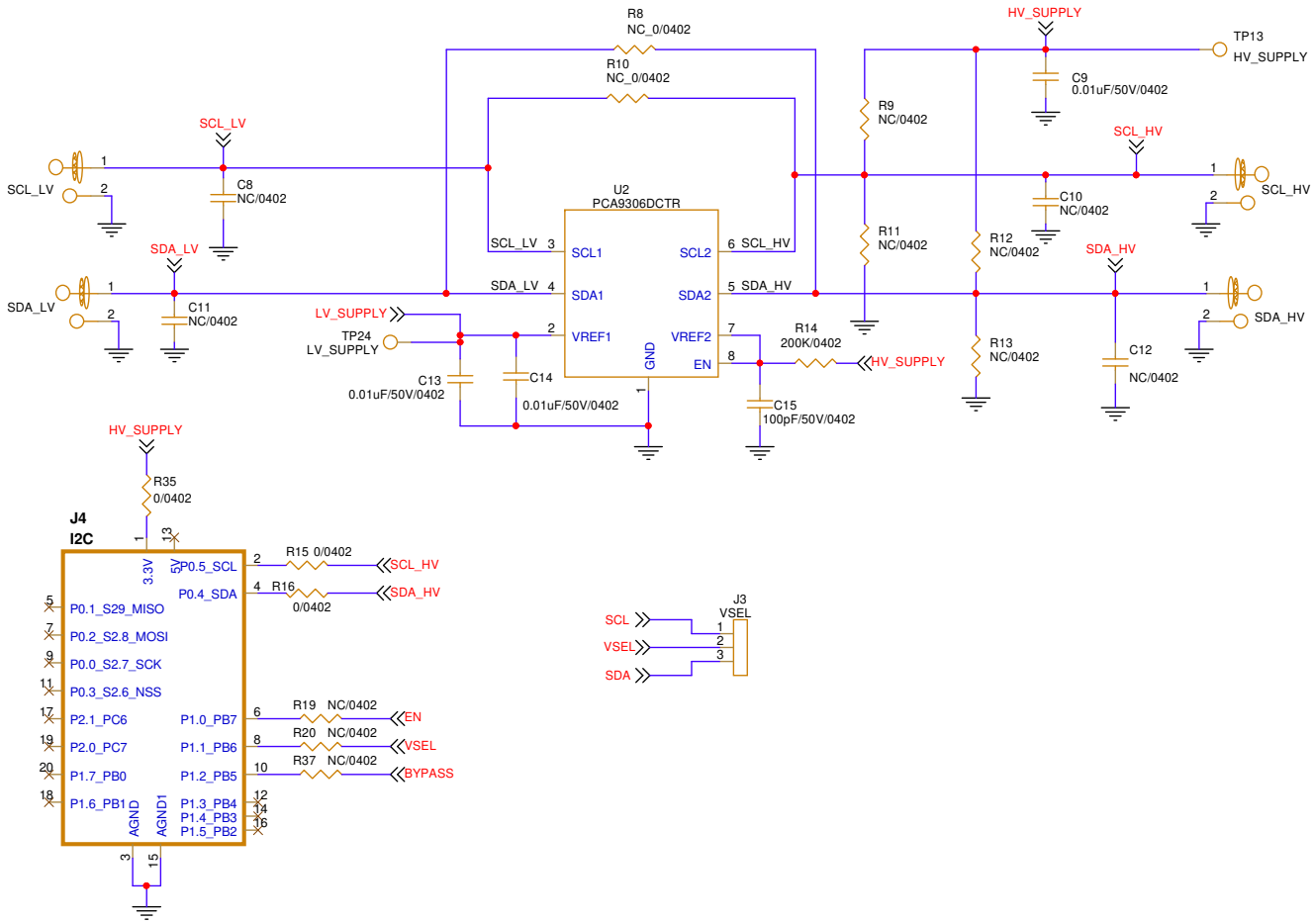

Figure 10. RTKA23610xDE0010BU Schematic - Page 2 (For RAA236100 use only)

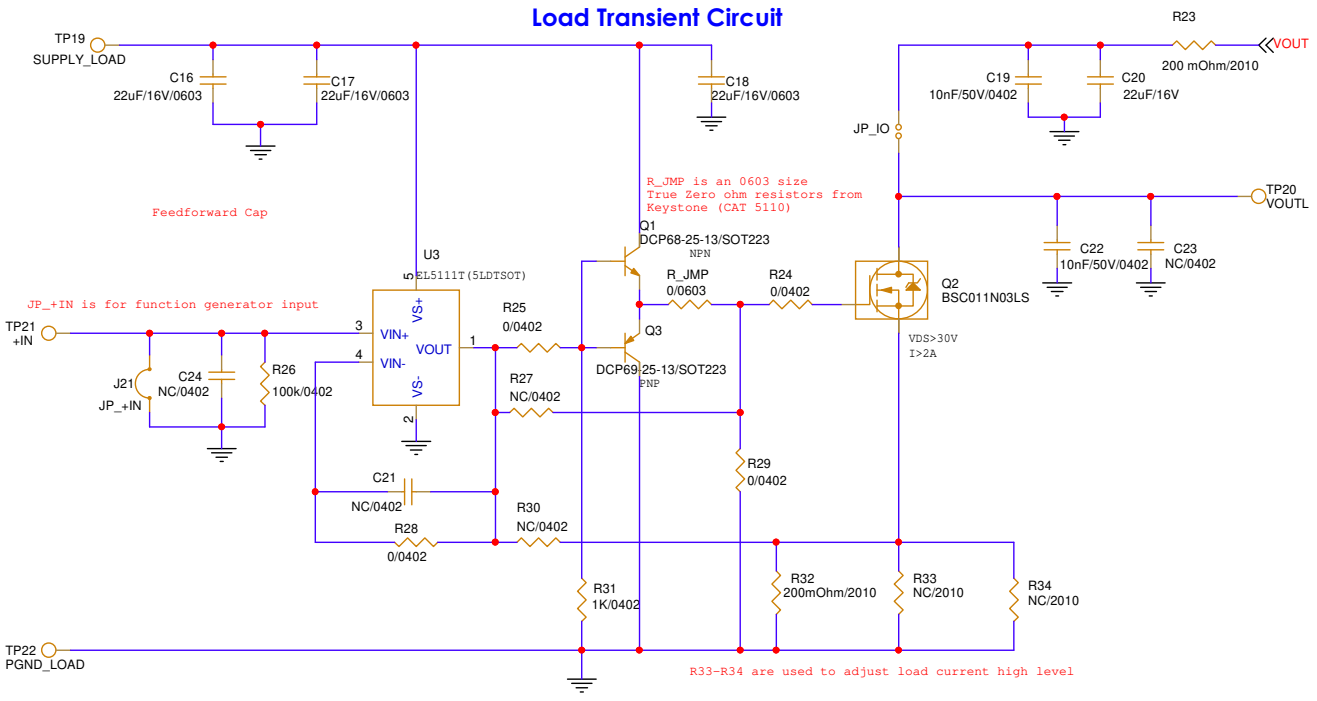

Figure 11. RTKA23610xDE0010BU Schematic - Page 3

2.1.3 Bill of Materials

Table 2. Bill of Materials for DFN package evaluation board (RTKA236100DE0010BU)

Qty	Ref	Part/Value	Description	Manufacturer Part Number	Manufacturer
1	C2	47µF/16V/1210	CAP CER 47µF 16V X5R 1210	GRM32ER61C476ME15	Murata
3	C3, C4, C5	10µF/6.3V/0603	10µF ±20% 6.3V Ceramic Capacitor X5R 0603	GRM188R60J106ME47	Murata
5	C9, C13, C14, C19, C22	0.01µF/50V/0402	0.01µF/50V/0402 Ceramic Capacitors	GRM155R71H103MA88D	Murata
1	C15	100pF/50V/0402	100pF/50V/0402 Ceramic Capacitors	GRT1555C1H101JA02D	Murata
3	C16, C17, C18	22µF/10V/0603	22µF/10V/0603 Ceramic Capacitors	GRM188R61A226ME15D	Murata
1	C20	22µF/10V	22µF ±20% 10V Ceramic Capacitor X5R 0805	GRM21BR61A226ME51L	Murata
1	JP1	SCL_SEL	CONN HEADER VERT 3POS 2.54MM	961102-6404-AR	3M
1	JP2	SDA_SEL	CONN HEADER VERT 3POS 2.54MM	961102-6404-AR	3M
2	J6, TP9	VSEL	CONN HEADER VERT 3POS 2.54MM	22284360	3M
1	J4	I2C	CONN HEADER R/A 20POS 1.27MM	M50-3901042	-
2	J7, TP10	EN	CONN HEADER VERT 3POS 2.54MM	22284360	3M
1	J8	VPULLUP	CONN HEADER VERT 3POS 2.54MM	22284360	3M
2	TP12, J17	SCL	CONN HEADER VERT 2POS 2.54MM	22284360	3M
2	TP14, J18	SDA	CONN HEADER VERT 2POS 2.54MM	22284360	3M
1	J21	JP_+IN	CONN HEADER VERT 2POS 2.54MM	22284360	3M
1	J22	BYPASS	CONN HEADER VERT 3POS 2.54MM	22284360	3M
1	L1	1uH/0603	FIXED IND 1UH 1.8A 120 MΩ SMD	DFE18SBN1R0ME0L	Murata
2	L2, L3	0/0402	RES 0Ω 1% 1/4W 0402	Generic	Various
7	R15, R16, R24, R25, R28, R29,R35	0/0402	RES 0Ω 1% 1/4W 0402	Generic	Various
1	Q1	DCP68-25-13/SOT223	DCP68-25-13/SOT223	DCP68-25-13	-
1	Q2	BSC011N03LS	BSC011N03LS	-	-

Table 2. Bill of Materials for DFN package evaluation board (RTKA236100DE0010BU) (Cont.)

Qty	Ref	Part/Value	Description	Manufacturer Part Number	Manufacturer
1	Q3	DCP69-25-13/SOT223	DCP69-25-13/SOT223	DCP69-25-13	-
3	R1, R2, R_JMP	0/0603	RES SMD 0Ω JUMPER 1/2W 0603	5110	-
1	R3	0.3/0603	RES 0.3Ω 1% 1/4W 0603	Generic	Various
2	R4, R6	10K/0402	RES 10kΩ 1% 1/4W 0402	Generic	Various
1	R7	205K/0402	RES 45.3kΩ 1% 1/4W 0402	Generic	Various
2	R8, R10	NC_0/0402	RES DNP/0Ω 1% 1/4W 0402	Generic	Various
1	R14	200K/0402	RES 200kΩ 1% 1/4W 0402	Generic	Various
3	R17, R21, R36	1M/0402	RES 1MΩ 1% 1/4W 0402	Generic	Various
1	R23, R32	200mΩ/2010	RES 0.2Ω 2.0 W 1% 2010 SMD	WSL2010R2000FEA	-
1	R26	100k/0402	RES 100kΩ 1% 1/4W 0402	Generic	Various
1	R31	1K/0402	RES 1kΩ 1% 1/4W 0402	Generic	Various
2	R32	1Ω/2010	RES 1Ω 1% 3/4W 2010	RMCF2010FT1R00DKR-ND	Stackpole
1	TP1	VIN	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP2, TP6	S+	TERM TURRET SINGLE L = 5.84MM TIN	575-3156100150000	Mill-Max
2	TP3,TP7	S-	TERM TURRET SINGLE L = 5.84MM TIN	575-3156100150000	Mill-Max
8	TP4, TP8, TP16, TP17, TP18, TP25, TP26, TP27	GND	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP5	VOUT	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP13	HV_SUPPLY	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP15	V_EXT	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP19	SUPPLY_LOAD	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP20	VOUTL	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP21	+IN	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP22	PGND_LOAD	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP24	LV_SUPPLY	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP28	BYPASS	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max

Table 2. Bill of Materials for DFN package evaluation board (RTKA236100DE0010BU) (Cont.)

Qty	Ref	Part/Value	Description	Manufacturer Part Number	Manufacturer
1	U1	RAA236100 or RAA236105	8 pin DFN	RAA2361002GNP#HC5	Renesas
1	U2	PCA9306DCTR	IC TRNSLTR BIDIRECTIONAL SM8	PCA9306DCTR	-
1	U3	EL5111T	IC OPAMP VFB 1 CIRCUIT TSOT23-5	EL5111IWTZ-T7A	Renesas
1	C1	DNP/330µF	DNP	TR3D337K6R3C0100	Vishay Sprague
1	C3A	DNP	DNP	-	-
2	C6, C7	DNP/0603	DNP	-	-
11	R8, R9, R10, R11, R12, R13, R19, R20, R27, R30, R37	DNP/0402	DNP	-	-
7	C8, C10, C11, C12, C21, C23, C24	DNP/0402	DNP	-	-
1	J1	DNP/LX1	DNP	-	-
1	J2	DNP/LX2	DNP	-	-
1	J3	DNP/VSEL	DNP	22284360	3M
1	JP_IO	DNP/ JP2p	DNP	-	-
1	SCL_HV	DNP/SCL_HV	DNP	961102-6404-AR	3M
1	SCL_LV	DNP/SCL_LV	DNP	961102-6404-AR	3M
1	SDA_HV	DNP/SDA_HV	DNP	961102-6404-AR	3M
1	SDA_LV	DNP/SDA_LV	DNP	961102-6404-AR	3M
2	R33, R34	DNP/2010	DNP	-	-
1	TP23	DNP/VOUT	DNP	131-5031-00	Mouser

2.1.4 Board Layout

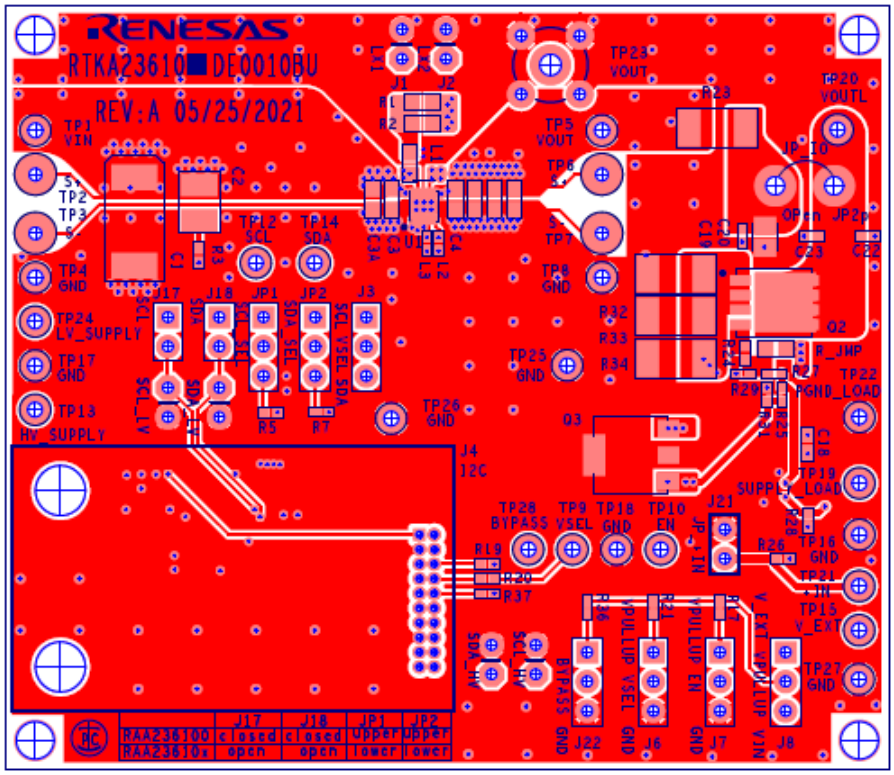

Figure 12. Top Layer Copper

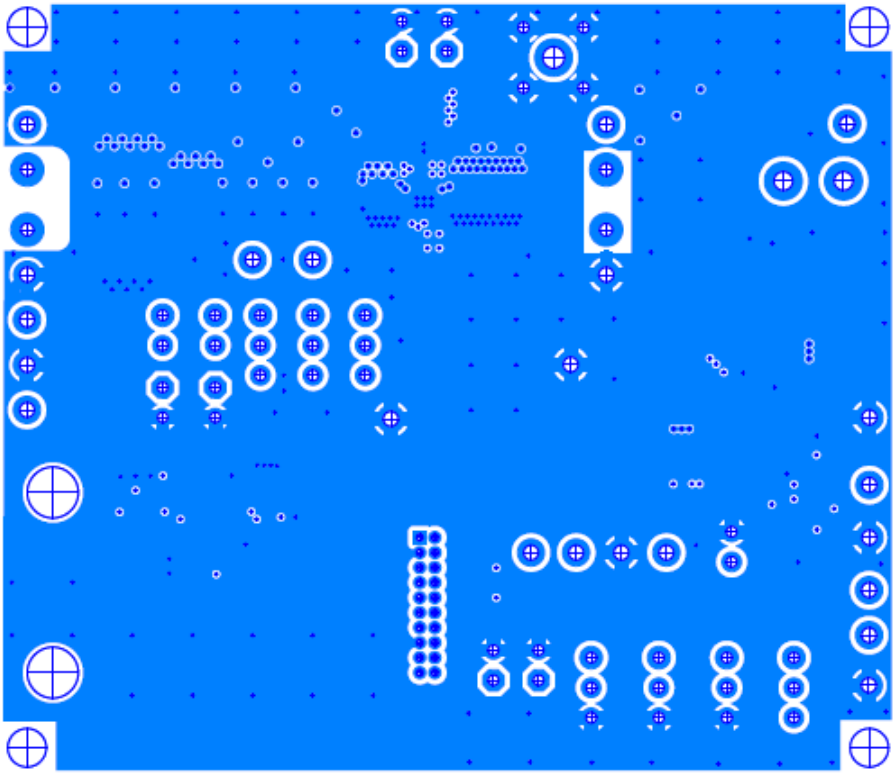

Figure 13. Layer 2 Copper

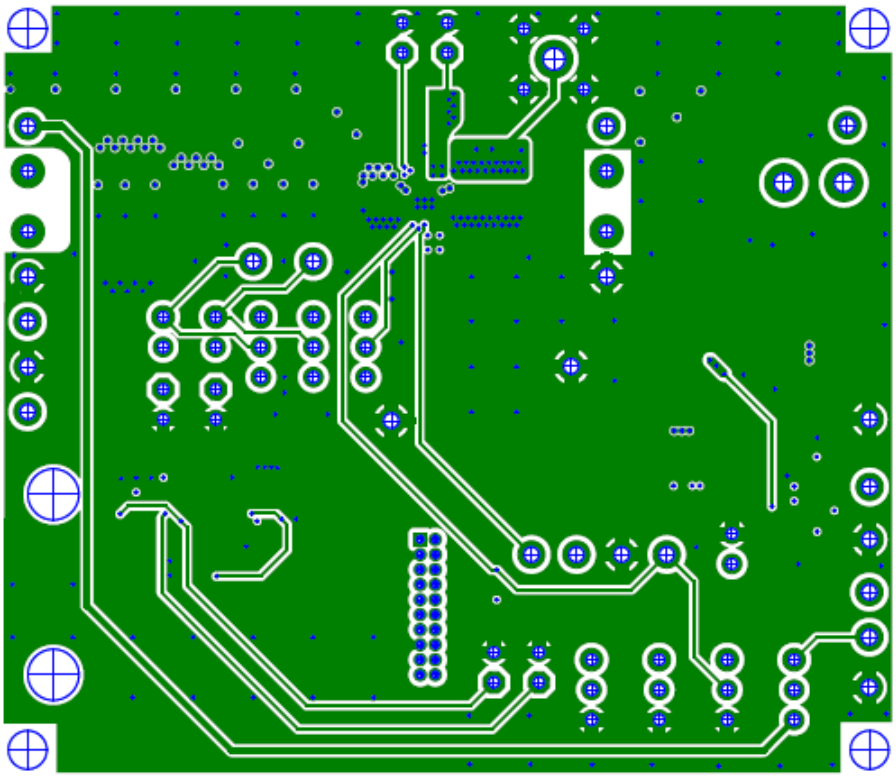

Figure 14. Layer 3 Copper

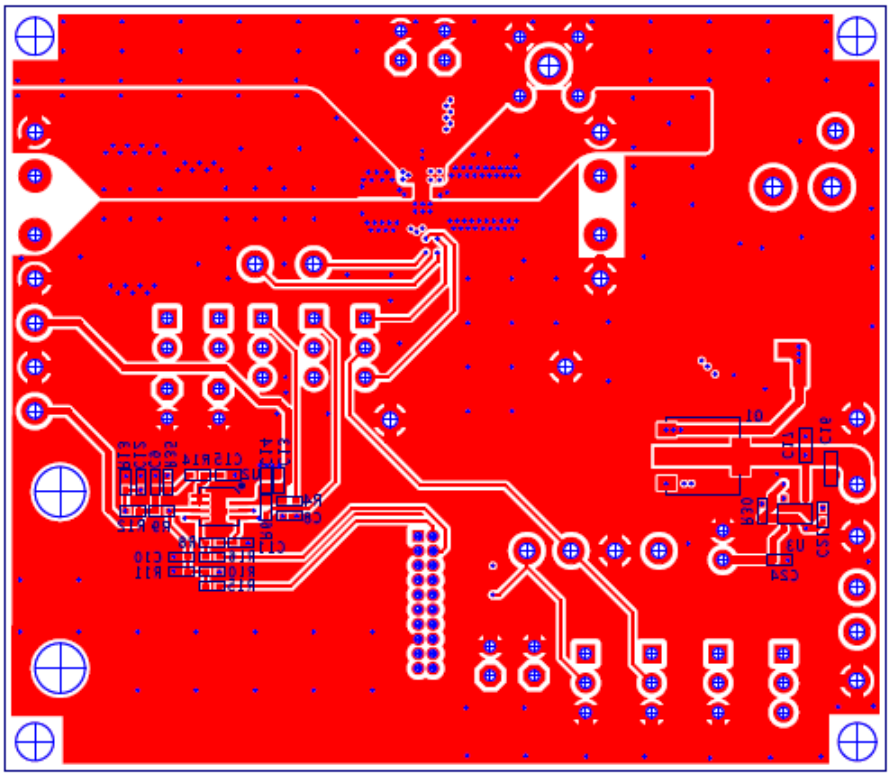

Figure 15. Bottom Layer Copper

2.2 Layout Guidelines

The layout is optimized for excellent electrical and thermal performance. However, when designing a PCB, use the following general practices:

- Position the input and output capacitors close to the IC. Both input and output currents can be discontinuous in a buck-boost converter; therefore, it is important to place both the input and output capacitors as close as possible to reduce loop areas. This reduces radiated EMI emissions.
- Keep the ground connections of the input and output capacitors as short as possible and placed on the component layer to avoid problems caused by high-switching currents flowing through PCB vias. If it is necessary to use the vias, use multiple vias to minimize the effective trace inductance.
- It is strongly advised that the second layer be a clean GND to mitigate problems that arise from long GND traces and subsequent parasitic inductive components. Also, a clean GND shields the intermediate layers from high power traces on the top layer.
- After placing short input and output loops, place an inductor as close as possible to the IC. While being cautious of any EMI concerns, ensure that the switch node traces (from LX1 and LX2 to the inductor) are short and wide.
- Route the EN, VSEL, SDA, and SCL traces away from high energy and high dV/dt traces to prevent mistriggering. These traces can be routed through intermediate layers.

3. Ordering Information

Part Number	Description
RTKA236100DE0010BU	DFN package evaluation board

4. Revision History

Revision	Date	Description
1.01	Nov 14, 2024	Updated input quiescent and Shutdown current. Updated schematics so they are readable. Update BOM
1.00	Dec 21, 2023	Initial release

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