

RTKA489220DK0000BU

The [RAA489220](#) IC is a 10-cell Battery Management Front End (BFE) with both autonomous measurement protection FET response and MCU controlled health monitoring of a battery pack. the RAA489220 measures pack voltage, cell voltage, charge and discharge current, external temperature and internal temperature per serial instructions from the master. The RAA489220 has system and internal checks to monitor the health of the part and the state of the system. The IC supports I²C communication with CRC capability for reliably interfacing with the connected MCU. The device has six open drain high voltage GPIOs that are capable of driving LEDs or fuse blowing.

Features

- VPACK voltages: 5V to 44V
- Built-in low-side FET drivers
- Open wire and internal system checks
- Hotplug tolerance

Kit Contents

- RTKA489220DE0000BU: Evaluation board
- RTKAPMODDONGLEV1Z: Communications dongle with USB cable
- BMS_PS_CELL10: Cell resistor ladder board

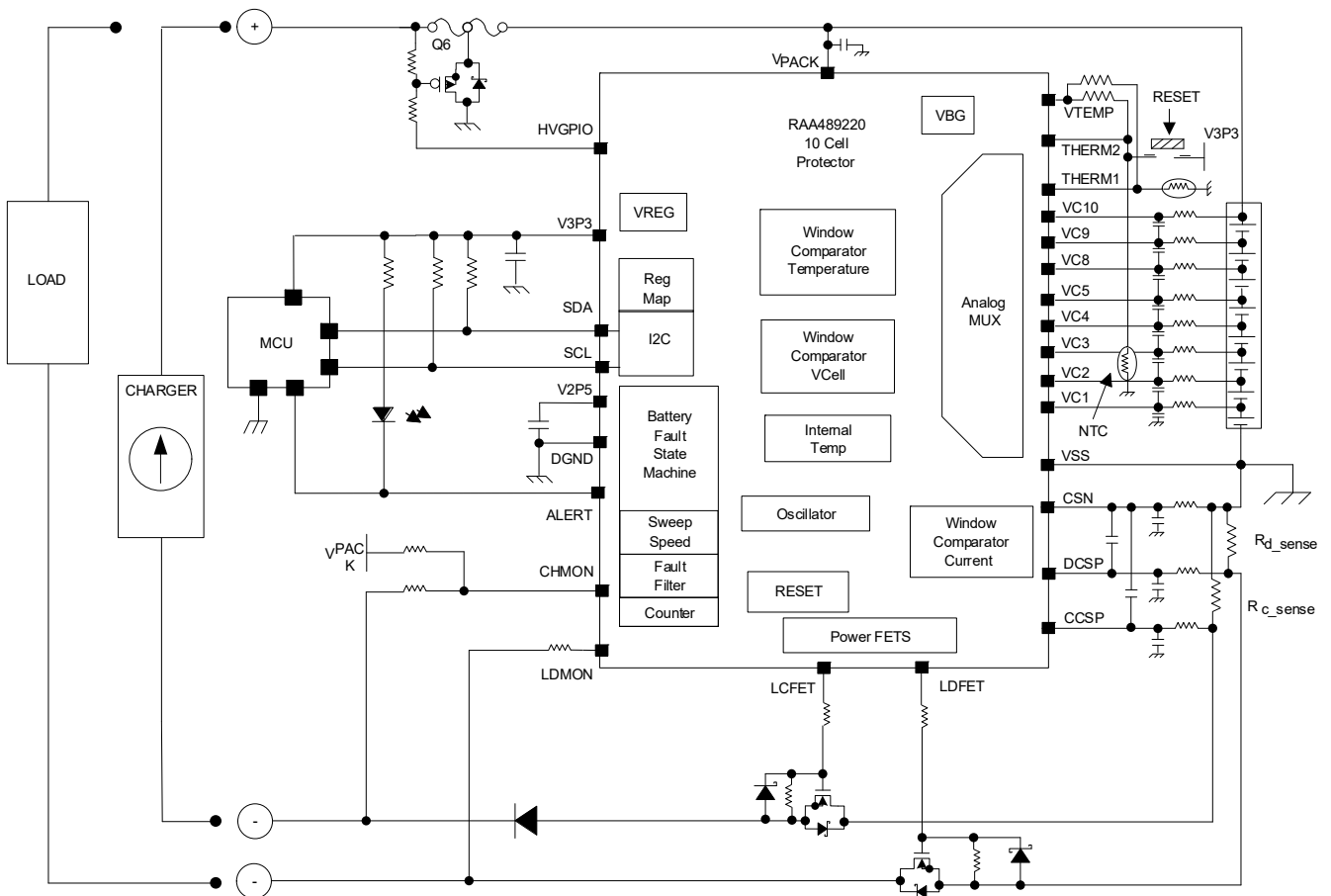


Figure 1. Application Diagram

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1. VBA Based GUI

The GUI is built using Visual Basic for Applications (VBA). VBA is the programming language used by Microsoft Excel, so all computers that have Microsoft Excel installed can run the GUI without needing any additional software.

2. Hardware Setup for Lab

- RTKA489220DE0000BU: RAA489220 evaluation board
- RTKAPMODDONGLEV1Z: RAA489220 communications dongle with USB cable
- BMS_PS_10CELLZ
- Power supply x3, or three total independent power supply outputs
- Current meter
- Voltmeter
- Oscilloscope

2.1 Evaluation Board

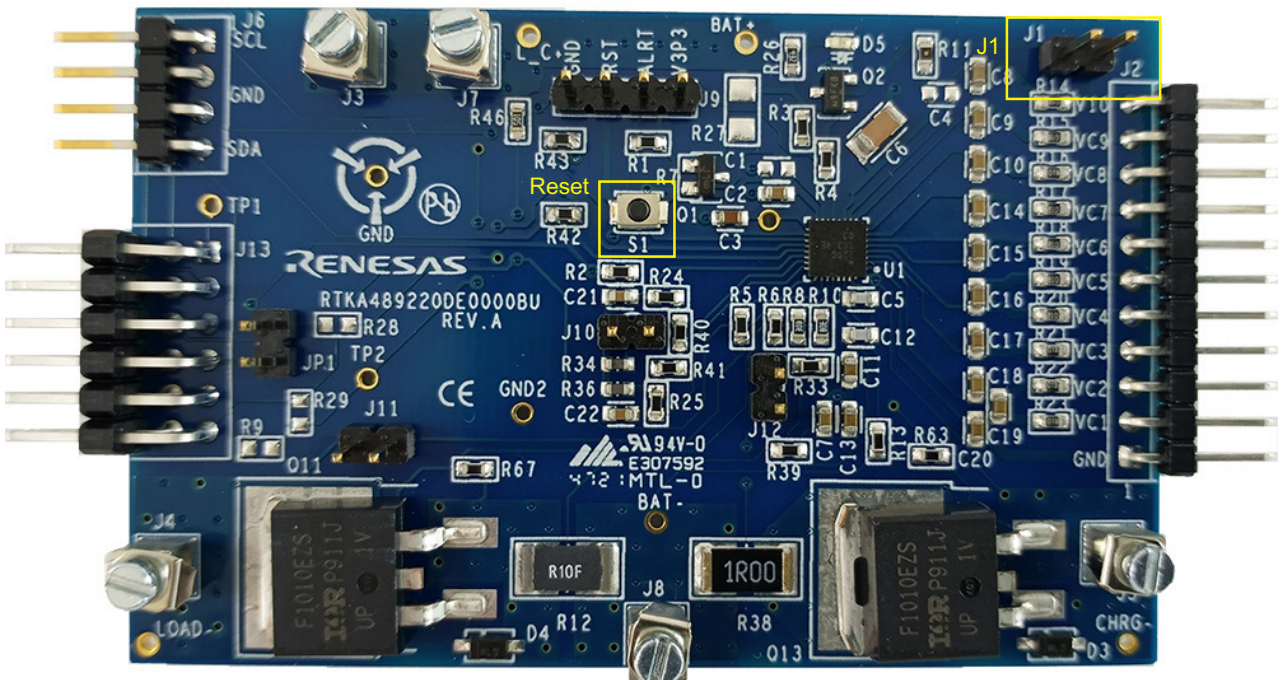


Figure 2. RTKA489220DE0000BU Evaluation Board

The RTKA489220DE0000BU evaluation board (Figure 2) as shipped from stock is set up for 10 cells. Supply current can be monitored by connecting the current meter across J1. *Note:* You must place a jumper across J1 if a current meter is not there. See the [Appendix](#) for a complete schematic of the evaluation board.

2.2 Communications Dongle

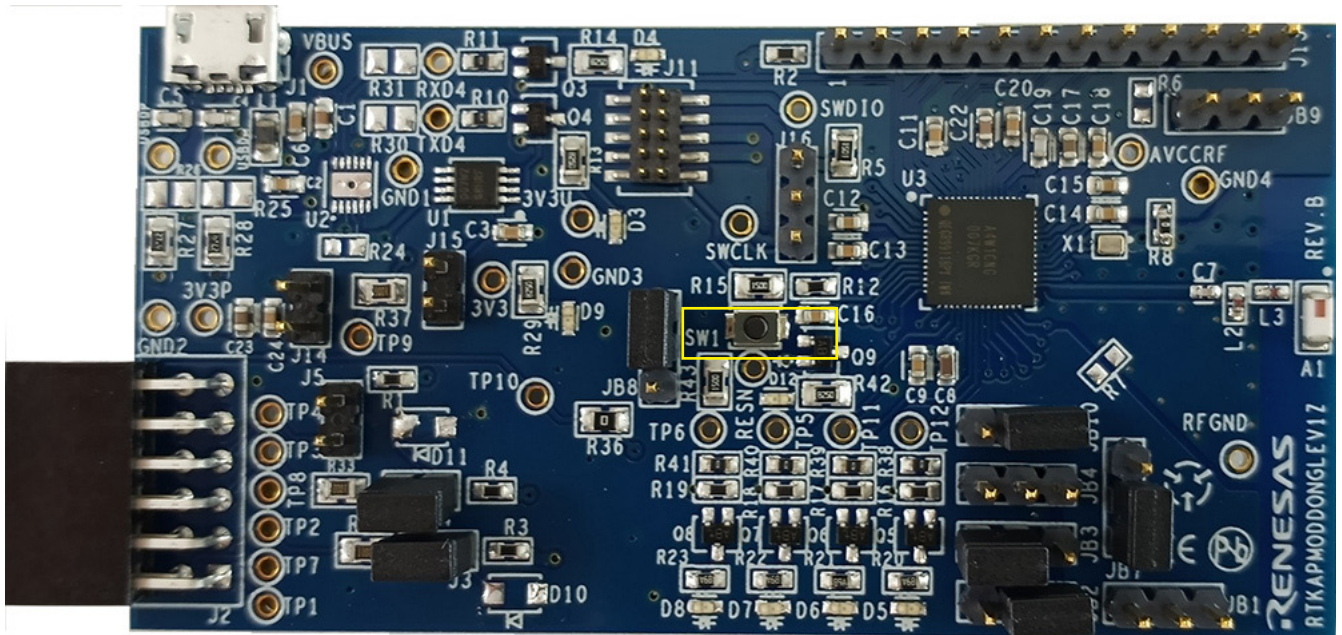


Figure 3. Communications Dongle

The communications dongle enables I²C communication with the RAA489220 through a PMOD interface (see [Figure 3](#)). **IMPORTANT:** This dongle is not electrically isolated. Therefore, the negative terminal of the Resistor Ladder must be connected to earth ground before connecting the communications dongle. Connect the dongle to the PC using a Micro USB to USB cable. Highlighted in [Figure 3](#) is SW1, the reset button that is used for troubleshooting (see the [Connect](#) section).

2.3 Resistor Ladder

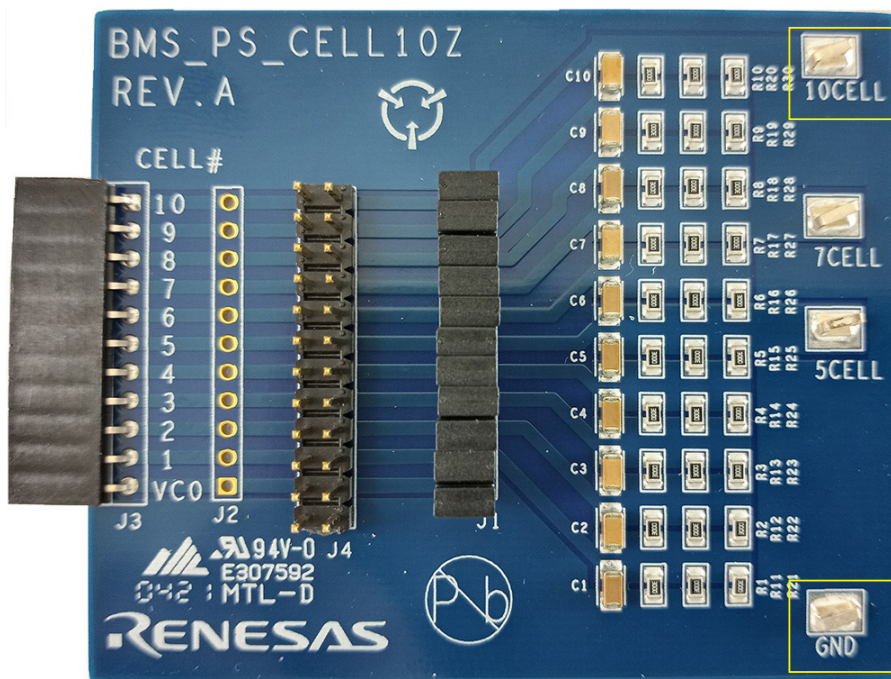


Figure 4. BMS_PS_CELL10Z Resistor Ladder

The resistor ladder board mimics a cell stack (limited) if a battery pack is not available. AC or heavy load currents cause voltage fluctuations when using a resistor ladder that does not occur with batteries.

Connector 10CELL, highlighted in Figure 4, should be used as the positive connection to the power supply for evaluation of systems with 10 cells. The negative terminal, each cell of the resistor ladder, consists of three 300Ω resistors in parallel resulting in 100Ω per cell. A typical operating voltage of 36V, when connected between GND and 10CELL, simulates a 36V cell voltage. The assembly board consumes ~35mA in this configuration.

2.4 Power Supply

In many cases a battery pack is not available, so the combination of a power supply and a resistor ladder is used. The power supply must be selected so that it can supply the ladder, the RAA489220 evaluation board, and the load currents at the required voltage without current limiting.

With the power supply output disabled, connect the negative terminal to the GND clip and the positive terminal to the 10CELL clip on the resistor ladder board.

Set the power supply output voltage to 36V but keep the output disabled. Do not either exceed 50V VBAT or 5.0V per cell depending on which is lower.

2.5 Current Meter

A current meter can be used to measure the current consumed by the RAA489220 Evaluation Board. If a multimeter is used, verify that it is connected and set to measure current. The current meter should be connected in place of a jumper on the evaluation board. *Note:* The following sections assume that this meter is installed at J1.

2.6 Voltmeter

Renesas recommends using a voltmeter to probe different points of interest on the assembly. By default, Renesas recommends to connect (1) the negative terminal to the GND pin of the 4-pin header on the EVK and (2) the positive terminal to the ALERT pin on the same header. Both pins are highlighted in Figure 5.

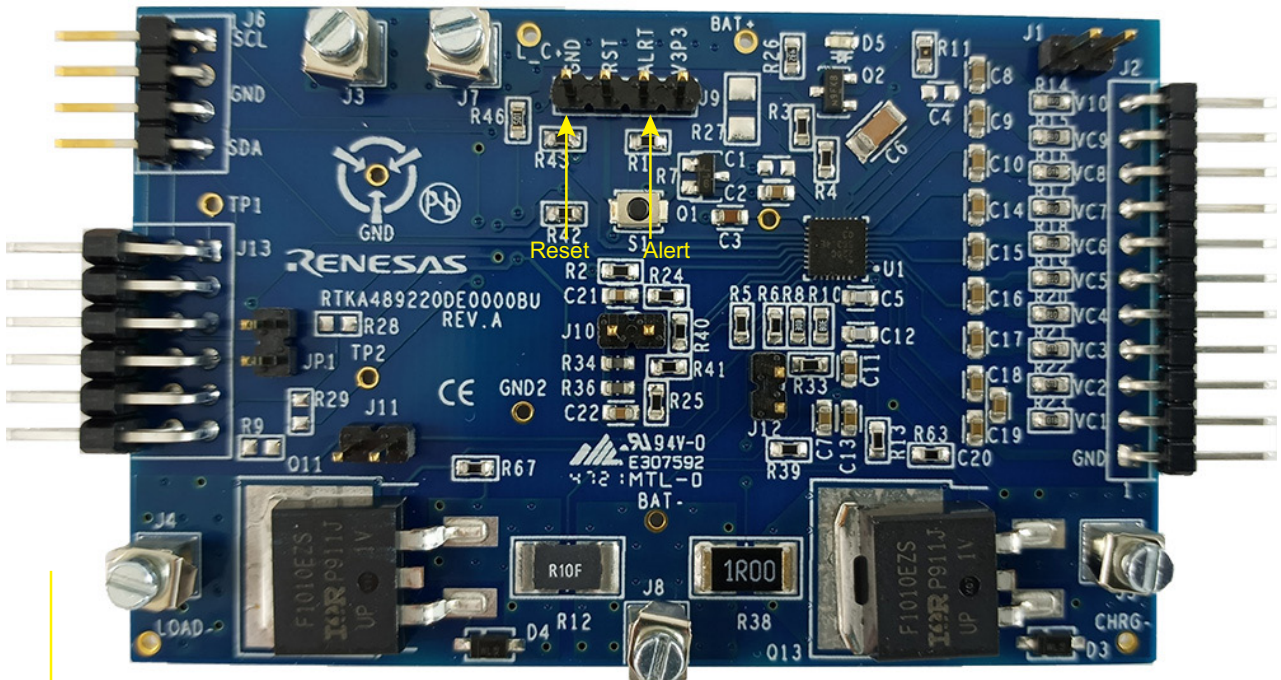


Figure 5. RAA489220 EVK

2.7 Oscilloscope

During evaluation, an oscilloscope can aid in capturing the communications and analog and digital signals that are associated with the RAA489220.

2.8 Full Lab Assembly

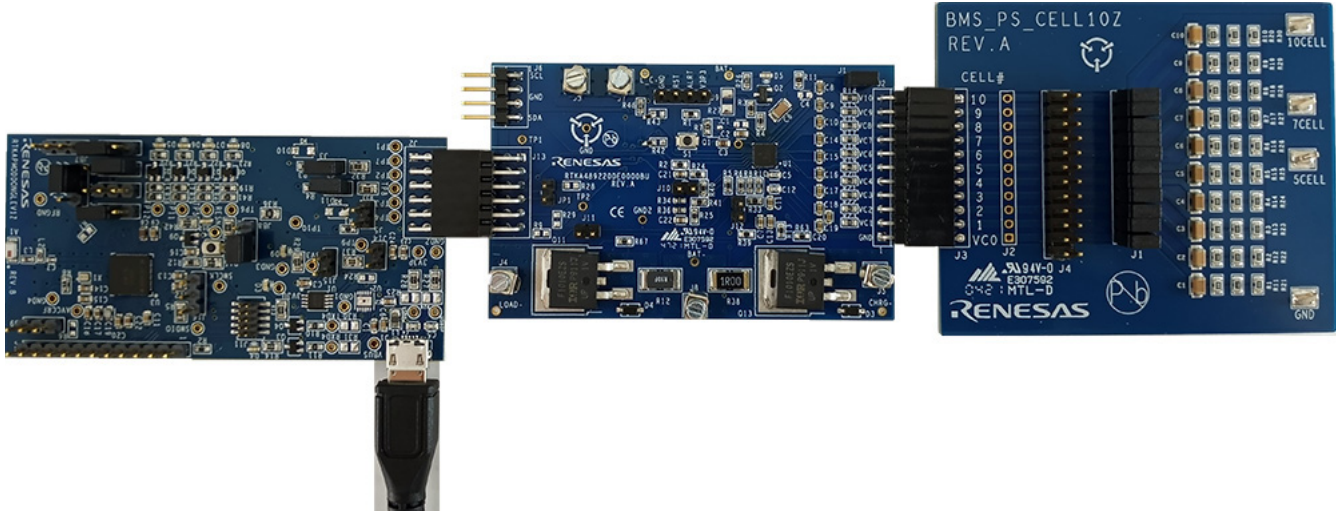


Figure 6. Full RAA489220 Assembly

The resistor ladder and RAA489220 evaluation boards connectors line up VC0 of the resistor ladder 1 to GND of the RAA489220EVK (see Figure 6). By default, a jumper or current meter should be connected across J1 of the RAA489220 EVK. If this jumper or current meter is not installed across J1, a separate wire from 10CELL of the resistor ladder must be connected to the top of J1 to provide a path to VPACK.

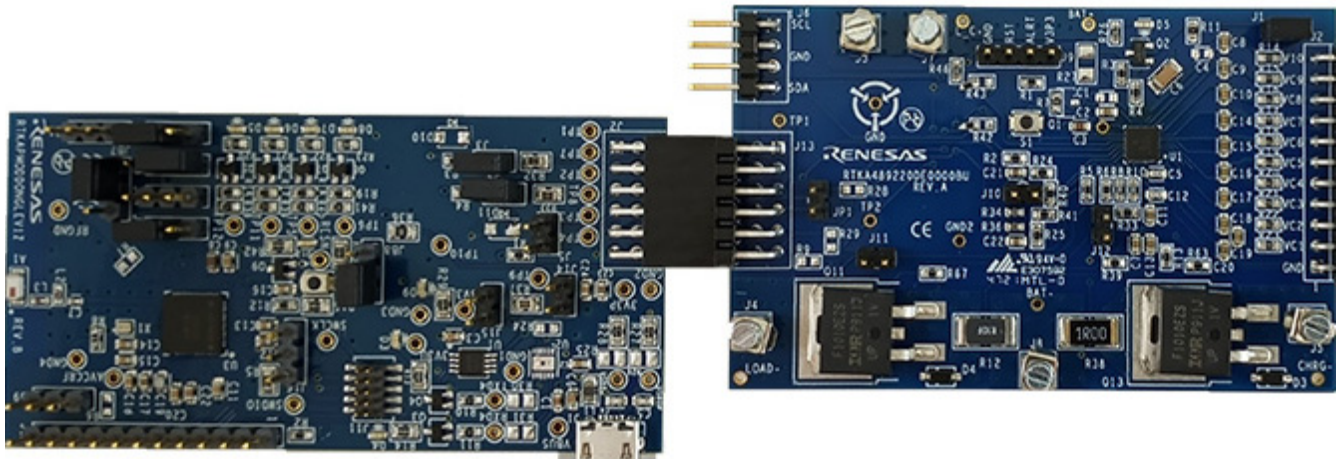


Figure 7. Communication Dongle and Evaluation Board Connection

The Communication Dongle and EVK are connected using a PMOD interface. Ensure the two headers are aligned properly such that no pins from the EVK side are not inserted into the header on the dongle side.

3. RAA489220 GUI Start

To begin, open the workbook; there is no installation required. Macros may be disabled, so under the menu bar if the message appears *SECURITY WARNING Macros have been disabled*, select **Enable Content** (see [Figure 8](#)).

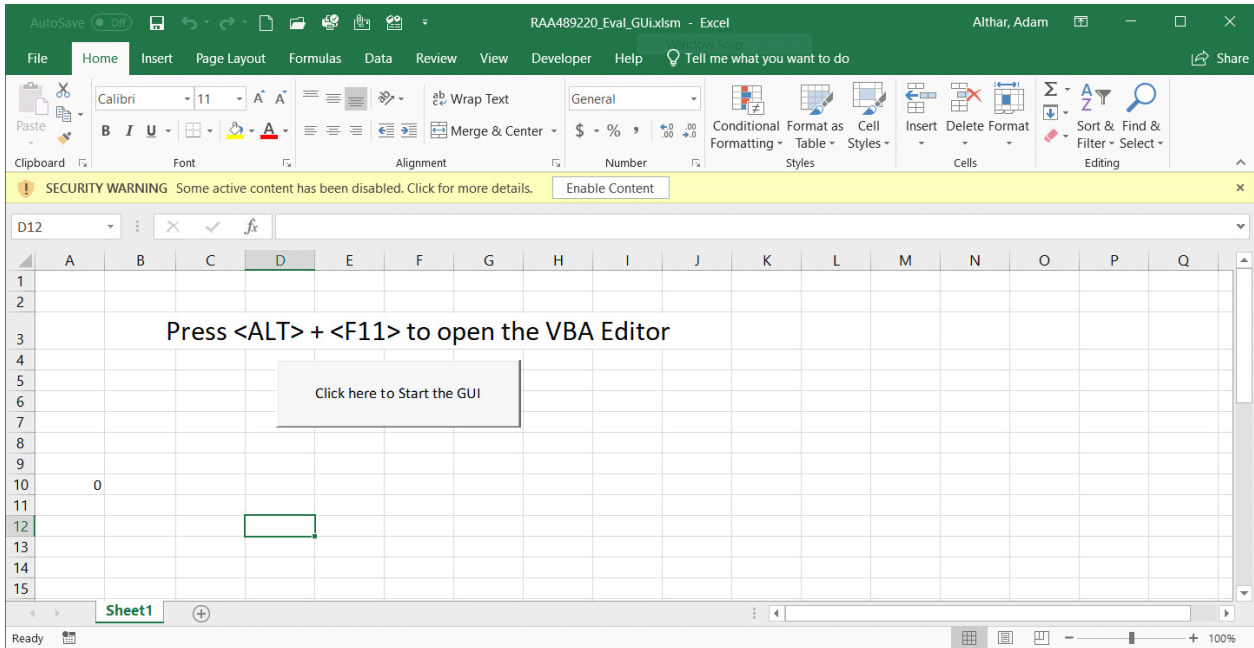


Figure 8. Macro Enable Warning

To start the GUI, click the button **Click here to Start the GUI**. The first time the GUI is launched, the Software License Agreement appears; after reviewing the agreement, choose **I accept the agreement** and click **Continue** to start the GUI (see [Figure 9](#)). *Note:* Unless the spreadsheet is saved before closing, the license agreement opens each time that the GUI is launched.

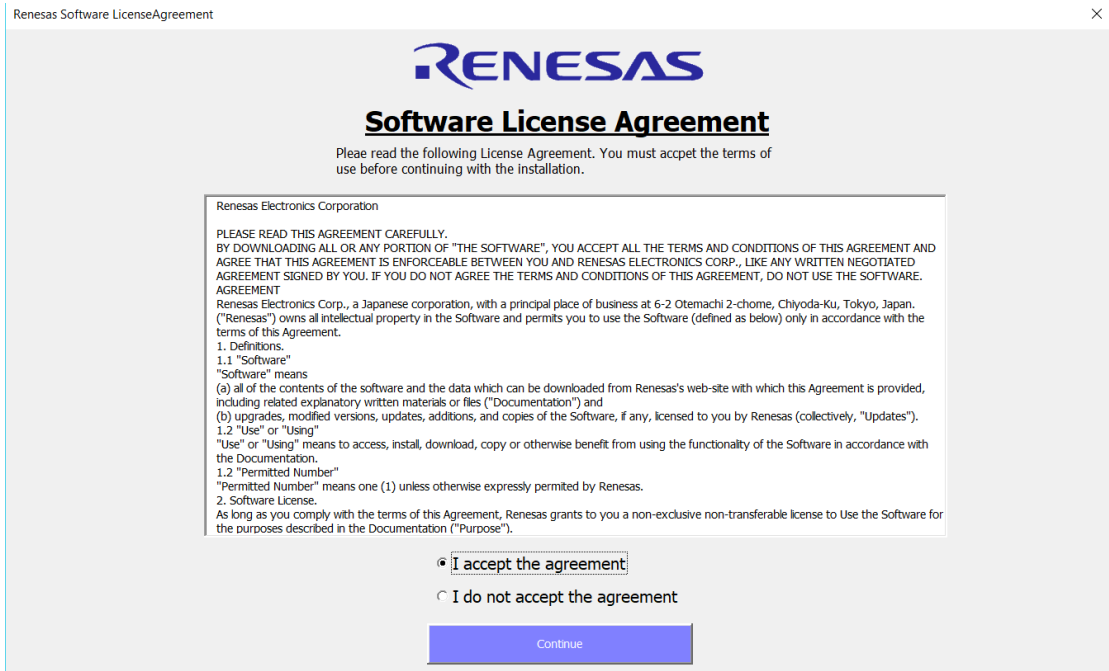


Figure 9. Renesas SLA Window

The RAA489220 GUI code is open source, which can be helpful when attempting to develop system level MCU code. To access the code, press **<alt> + <F11>** to open the VBA editor.

3.1 Power Supply

Enable the power supply connected to the resistor ladder board (or connect the battery pack). With VBAT set to 36V, the power supply should source ~35mA. Text in the following sections assumes this VPACK = 36 and VCELL = ~3.6V.

Typical power only supplies the source current by preventing the demonstration of charging features when using this type of supply. A battery pack or four quadrant source/sink type of supply is required to demonstrate charging.

4. Connect

The GUI must detect the dongle as present to operate; this is referred to as the connect step. Insert the USB cable between the dongle and PC; next, connect the dongle to the evaluation board. Press the green **Connect** button to start the detection process as shown in [Figure 10](#). *Note:* The connect step verifies that the dongle is connected to the PC properly, but it does not verify that the EVK is properly connected to the dongle.

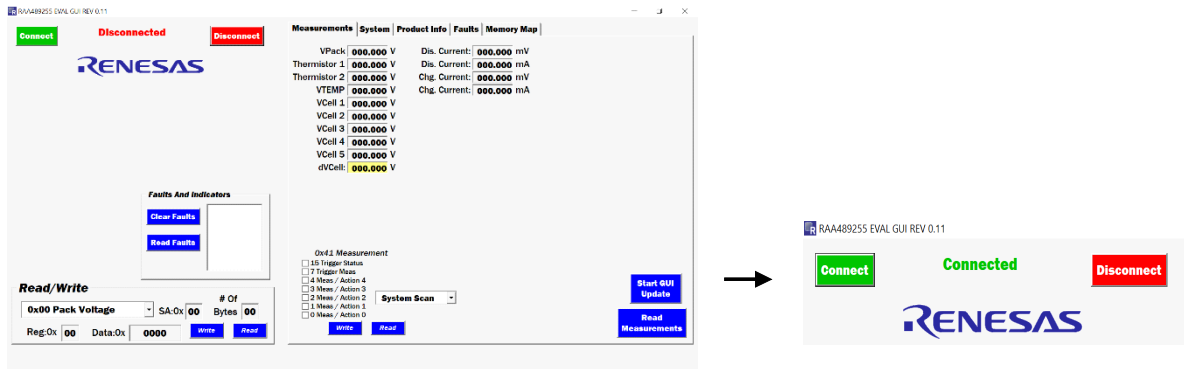


Figure 10. Connect Sequence

If the dongle is not connected to PC, an error message appears informing you that Dongle was not detected. When this error occurs, you should either unplug and plug back in the communications dongle or press the reset button on the dongle (see Figure 3).

4.1 Initial Communication

After a successful connection is made with the dongle, navigate in the GUI to the **Memory Map** tab and click the **Read Register** button at the bottom right. If the error message pops up as seen in Figure 11, the Dongle is not able to communicate with the RAA489220 IC. Verify the EVK is properly powered and that the PMOD headers between the EVK and communications dongle are securely connected.

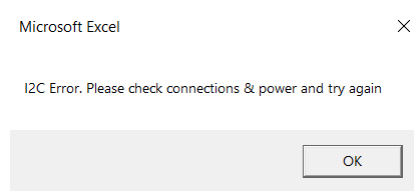


Figure 11. Communication Error Example

The PC user must have read/write access permission for the USB port, which may require assistance by your IT resources if the connection continuously fails.

If the device is properly powered and connected, the measurement registers, 0x00 - 0x06, should read 0000 (as shown in Figure 12), and the other register values may vary. The **Memory Map** tab can be used to directly read and write to the device registers.

System	Thresholds	Thresholds 2	Product Info	Faults	Memory Map	CRC
Memory Map						
0x00: 0x	0000	W	R	0x80: 0x	EA80	W R
0x01: 0x	0000	W	R	0x81: 0x	CC2D	W R
0x02: 0x	0000	W	R	0x82: 0x	0C25	W R
0x03: 0x	0000	W	R	0x83: 0x	98B4	W R
0x04: 0x	0000	W	R	0x84: 0x	CC71	W R
0x05: 0x	0000	W	R	0xFD: 0x	0003	W R
0x06: 0x	0000	W	R	0xFE: 0x	0049	W R
0x10: 0x	0000	W	R	0xFF: 0x	0010	W R
0x11: 0x	FF00	W	R			
0x40: 0x	0800	W	R			
0x41: 0x	0000	W	R			
0x42: 0x	4000	W	R			
0x6F: 0x	0000	W	R			

Figure 12. Initial Register Values

5. System Initialization

After confirming communication is working properly, configure to make the evaluation easier by disabling the communications time-out of the device. First, locate the Measurement section of the GUI (on the left side of the screen), and press the **Start GUI Update** button (see Figure 13). The update causes the GUI to periodically read the measurement, fault, and status registers displaying them in the GUI. As this can later be useful for monitoring the measurements, the continuous polling is also helpful to prevent the device from transitioning into Low-Power mode while disabling the communications timeout.

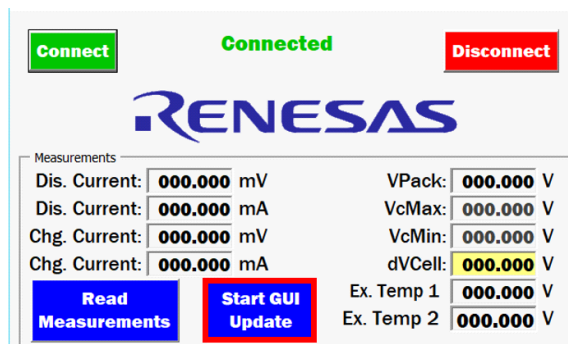


Figure 13. Start GUI Update Button

When the GUI is in continuous update mode, navigate to the **Thresholds** tab and locate the Unlock Registers button (see Figure 14). This button writes the unlock sequence to register 0x6F that is required to modify the upper registers, 0x80-84. Whenever the device is reset, the key must be written to write to the upper registers. In practice, Renesas recommends writing 0x0000 to register 0x6F after the modification is done to prevent unintentional threshold modification. The registers can be read without being unlocked.

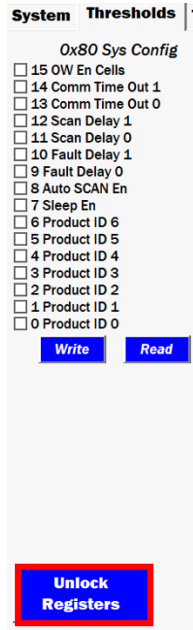


Figure 14. Unlock Registers Button

When the registers are unlocked, locate register 0x80 Sys Config, which is located on the same tab, and press the **Read** button to get the current setting of the register. Renesas recommends to always first read a register back before modifying it to avoid unintentional changes to the settings. Uncheck bits 0x80.14 (Comm Time Out 1) and 0x80.13 (Comm Time Out 0). Next, press the **Write** button. This sequence is outlined in Figure 15.

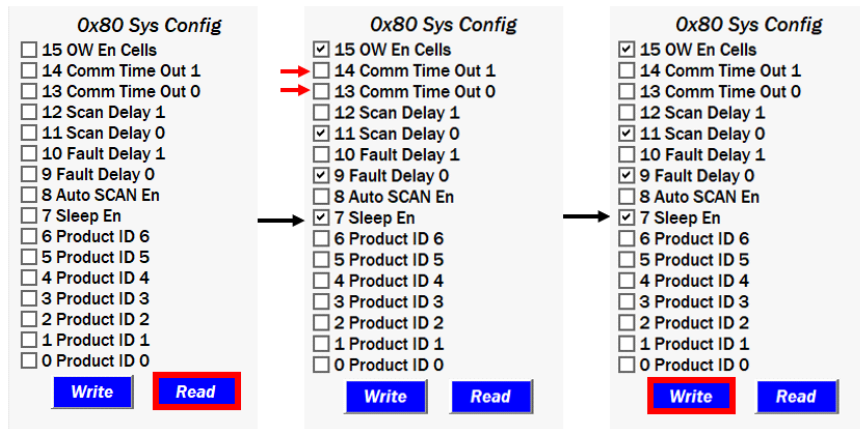


Figure 15. COMMTO Disable Sequence

Click the **Read** button again to verify the register was properly modified. Now that Comms TO has been disabled, the GUI can be taken out of continuous update mode by relocating the GUI Measurement section so that the **Stop GUI Update** button is in view. Click the **Stop GUI Update** button to stop the continuous readings.

6. Performing Measurements

The default method of measurement for the RAA489220 is MCU triggered scans. There are two categories of measurement: System Scans and Individual Measurements. System Scans perform a vast amount of measurements along with other tests depending on the device configuration. During system scans, fault bits are set in response to threshold violation, and individual measurements perform a only a specified measurement. As

a result, system scans take longer to perform but they provide more information, while individual measurements are used to closely monitor specified areas. For more information on the measurement scans, see the *RAA489220 Datasheet*.

6.1 System Scans

Performing System Scans: Navigate to the **System** tab and locate register 0x41 Measure Select. By default, the drop-down menu (to the right of the register) is set to System Scan. Check the box for **7 Trigger Meas**, and click the **Write** button as shown in [Figure 16](#).

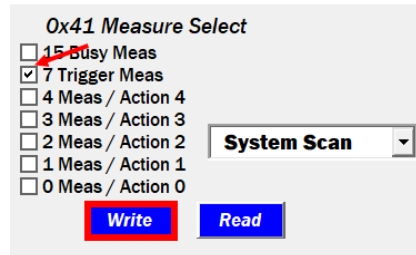


Figure 16. System Scan Execution

Click the **Read** button for register 0x41 Measure Select, and Bit 0x41.15 Busy and Bit 0x41.7 Measure Select are now clear indicating that the scan has executed and completed.

Locate and click the **Read Measurements** button in the measurement section of the GUI, and the measurement fields update with the recent measurements. With a pack voltage of 36V, the measurements resemble those in [Figure 17](#).

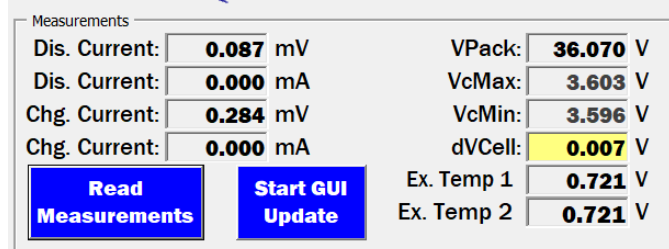


Figure 17. Measurement Results

Next, click the **Read Faults** button in the **Faults and Status** box, and the box updates with any fault or status bits that were set during the system scan (see [Figure 18](#)). Renesas highly recommends performing a read of the measurements and faults every time a system scan is executed.

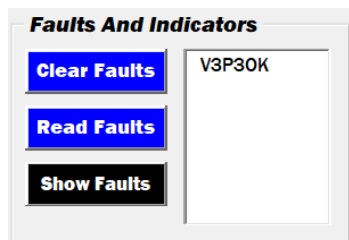


Figure 18. Faults and Indicators Box

6.2 Individual Measurements

The process to perform an individual measurement from the GUI is similar to performing a system scan. To perform an individual measurement first locate the drop-down menu next to register **0x41 Measure Select**. Click the drop-down list and select **Vcell 1** from the list. The check boxes for the appropriate Measure Select bits, 0x41.4:0, will automatically populate based on which measurement is selected from the drop-down menu. Check the box for bit **0x41.7 Trigger Meas** and click the **Write** button. This process is outlined in [Figure 19](#).

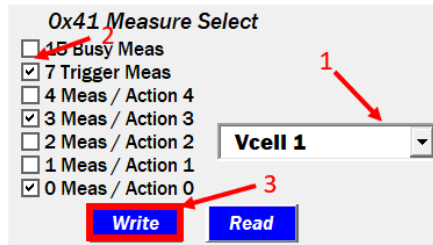


Figure 19. Vcell 1 Measure Sequence

If the measurement is correctly performed, the result appears next to the drop-down menu (see [Figure 20](#)). This is because the results of individual measurements are typically stored in the Thermistor 2 data register 0x04, and each measurement requires a specific equation to calculate the decimal value from the hex value. The GUI streamlines this process to make the result easier to understand by immediately reading back the result of the individual measurement and converting it to its decimal value using the appropriate equation.

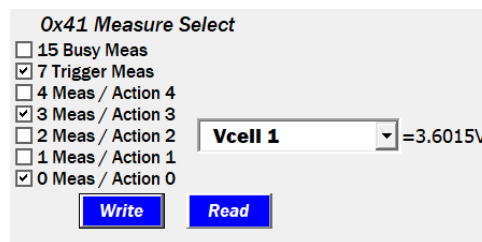


Figure 20. Vcell 1 Measurement Result

6.3 Voltage Faults

After the process for performing system scans is reviewed, some RAA489220 protection features can be examined such as the voltage faults. To begin examining the voltage faults, navigate to the **Thresholds** tab and click the **Unlock Registers** button to allow the threshold registers to be modified. Next, locate register 0x81 VCell OV and press the **Read** button to get the current value of the register. Adjust the value in the text box next to the OV Bits, 0x81.15 - 0x81.9 to 3800mV. The check boxes for the bits automatically update when the write is performed, the individual bits do not need to be checked. Additionally, if the value in the text box is not a valid OV setting, the GUI automatically adjusts to the closest valid setting. Next, locate the drop-down menu next to the OVLO bits, 0x81.3 - 0x81.0 and select **4.0V** as the setting. Finally, perform a write followed by a read to confirm the settings wrote properly. The register should appear as in [Figure 21](#).

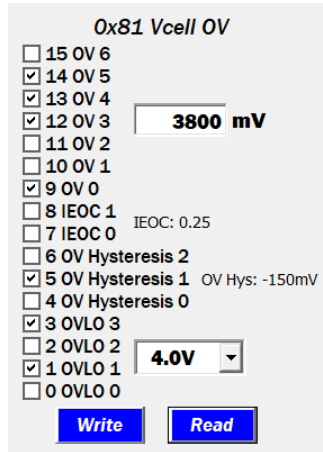


Figure 21. OV Threshold Settings

Return to the **System** tab. Select **System Scan** from the Measure Select register drop-down menu. Check bit **41.7 Trigger Meas**, and click the **Write** button followed by a **Read Measurements**. The measurements should be similar to the results of the previous system scan. Raise the voltage of the power supply above 38V but less than 40V. Perform another system scan by clicking the **Write** button for register 0x41 Measure Select. Next, perform a **Read Measurements** and then a **Read Faults**. The measurements should reflect the increased voltage, but the OV bit should not yet be set. Perform another system scan while monitoring the multimeter connected to the ALERT pin. Verify it is at 0V. Read the results again, and the OV indicator should appear in the **Faults and Indicators** box as shown in Figure 22. The reason for this behavior is that OV is one of many faults that require two consecutive system scans with the fault condition present to set.

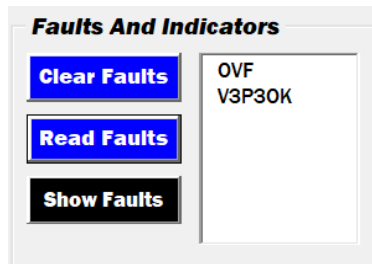


Figure 22. OVF Fault Indicator

Next, click the **Clear All Faults** button in the **Faults and Status** box, and press the **Read Faults** button. The OVF bit should no longer be present in the **Faults and Indicators** box. Additionally, the ALERT pin should no longer be asserted. Keep an eye on the voltmeter connected to the ALERT pin for the remainder of this guide to see when the pin asserts and clears. The **Clear All Faults** button writes bit 0x40.6 Clear Faults, which resets the fault bits and counters. This means that two consecutive system scans with the OV condition present are required to reset the OV bit.

Continue to raise the supply voltage until it is >40V. Perform a system scan and read the results. The **Faults and Status** box should not have any new indicators. Perform another system scan and check the voltage of the ALERT pin, which should be asserted. Read the measurement and fault results again. The OVF bit is set along with the LOF bit (see Figure 23). The LOF bit being set along with the OVF bit indicates that the OVLO threshold has been violated.

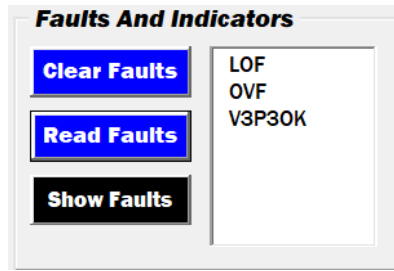


Figure 23. LOF and OVF Fault – Indicating OVLO

Lower the supply voltage until it is between 37V and 38V; perform a system scan and read the results. The LOF bit is clear, but the OVF bit is set despite that all the cell values are below the 3800mV OV setting. This is because the device has hysteresis on the OV, which by default is -100mV. Lower the voltage to 36V; perform a scan and read the results. The bit is now clear because the hysteresis threshold has been crossed. The same form of protection exists at the low end of cell voltage in the form of a UV threshold, UVLO threshold, and UV hysteresis.

7. Current Faults

There are also several protection features based on abnormal current detection. Demonstrating these features requires a power supply with floating positive and negative terminals to apply a voltage across the sense resistors to act as a current signal to measure.

Before you can apply the voltage across the sense resistors, you must turn on the FETs. Navigate to the **System** tab and locate register **0x40 System Setup**. First, click the **Read** button to get the present value of the register. Next, check the boxes for **0x40.1 LDFET En** and **0x40.0 LCFET En**, followed by clicking the **Write** button. Click the **Read** button again. **0x48.9 LDFET status** and **0x48.8 LCFET status** should now be set as in [Figure 24](#).

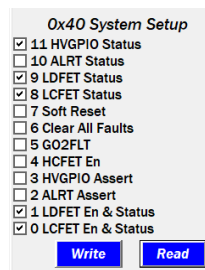


Figure 24. LDFET and LCFET Status Bits Set

7.1 Charging Current

The FETs are now on a current signal and can be induced. Connect the positive terminal of the floating supply to J8 that is tied to the BAT- pin and (2) connect the negative terminal to J5 that is tied to the CHRG- pin. Turn on the supply and raise the voltage to ~5mV. Perform a system scan and click **Read Measurements**. The **Fault and Indicators** box should now have a CHRGI indicator and the **Chg. Current** measurement should read 5mV as seen in [Figure 25](#). If the measurement value is significantly lower, the charge and discharge sense resistors might need to be replaced with a larger value so that examining the current related functionality is easier without requiring large amounts of current.

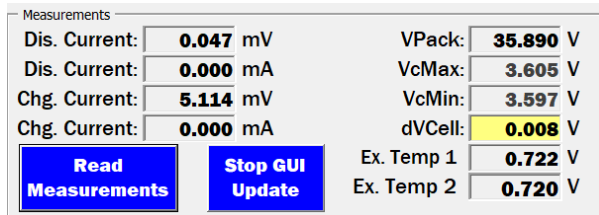


Figure 25. Chg. Current Measurement

Charging is now possible so navigate to the **Threshold 2** tab and click the **Read** button for register 0x84 Pack Threshold. Adjust the DSC Threshold to 50mV by unchecking bit **0x84.14 DSC2** and checking bit **0x84.13 DSC1**. The label to the right of the DSC threshold reads DSC Thresh: 50mV if the proper bits were selected. Next, change the value in the text boxes for DOC and COC to 15mV. Click the **Write** button followed by the **Read** button to confirm the values are properly set; the register reflects [Figure 26](#).

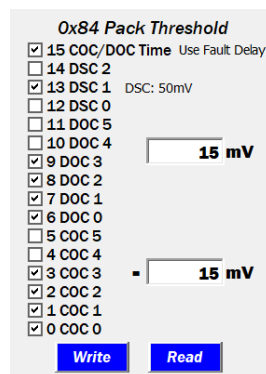


Figure 26. Pack Threshold Register

Navigate back to **System** tab. Perform a system scan and read the results. There should be no additional bits displayed in the **Faults and Indicators** box. Raise the voltage of the supply across the sense resistor until it is greater than 15mV. Perform another system scan and read the results. The COC bit should now be displayed in the **Faults and Indicators** box as in [Figure 27](#). COC/DOC take two consecutive scans to set like other faults; however, a single system scan performs multiple current measurements. Therefore, the fault bit sets if the current is above the fault threshold at two consecutive measurements during a single system scan.

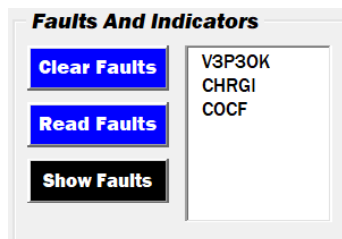


Figure 27. COCF Indicator

Continue to raise the supply voltage across the resistors until it is above 50mV. Click on **Read Measurements**. The SCF bit is not set in the **Faults and Indicators** box despite being above the DSC Threshold, because the discharge short-circuit threshold setting only changes the short-circuit threshold for current in the discharge direction. For short-circuit in the charging direction, the threshold is fixed at 200mV. Raise the voltage on the supply across the sense resistors while periodically clicking the **Read Measurements** button. The SCF bit automatically sets when the threshold is crossed. A system scan is not required for short-circuit detection, because while the short-circuit response circuitry uses an analog comparator, the digital comparator is used in

many of the other faults that require system scans to trigger. The SCF bit might not set until the voltage across the sense resistor is around 250mV, so continue to raise the voltage until the bit is set as seen in [Figure 28](#).

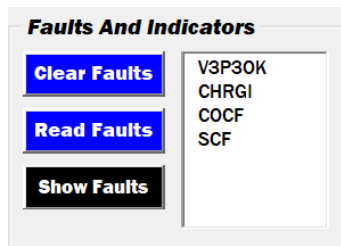


Figure 28. Charging SCF Indicator

When the SCF bit is set, use a multi-meter to check the GATE pins voltage of the CFET and DFET. The voltage at both pins should be 0V, because in idle mode the device shuts off the FETs. **IMPORTANT:** The FET status bits 0x40.9 and 0x40.8 do not update when the FETs turn off because of an SCF. With the short-circuit condition present, click **Clear All Faults** followed by **Read Faults**; because the condition is present, the SCF bit remains set.

Reduce the voltage across the sense resistor to 0V and perform a **Clear All Faults** followed by a **Read Faults**. SCF is no longer be present and the FETs are on. Confirm this with a multi-meter.

7.2 Discharge Current

Evaluating discharge current and its related faults is like evaluating charge current. However, the pins the terminals of the supply must be adjusted to apply the voltage across the discharge sense instead of the charge sense resistor. To do this, connect the positive terminal of the supply to the LOAD- pin, and the negative terminal to BAT-. Confirm the CFET is on by reading register 0x40 and confirm that the bit 0x40.9 LDFET Status is set.

Raise the voltage of the supply across the sense resistor to about 5mV. Trigger a system scan and read the results. The Dis. Current measurement reads approximately 5mV, and the DCHRG I bit is set in the **Faults and Indicators** box (see [Figure 29](#)).

Raise the voltage of the supply across the sense resistor to above 15mV, trigger another system scan, and read the results. The DOC bit now is set as the 15mV DOC Threshold has been crossed (see [Figure 29](#)).

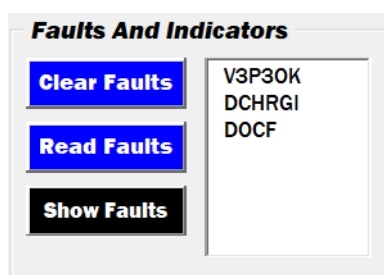


Figure 29. DOCF Indicator

Continue to raise the voltage on the supply across the sense resistor until it is above 50mV and click the **Read Faults** button. The SCF bit is now set in the **Faults and Indicators** box, because the previously set 50mV DSCF threshold is crossed. Additionally, turn off the FETs. Confirm this with a multimeter. Reduce the voltage across the sense resistor back down to 5mV. Click **Clear Faults** followed by **Read Faults**. The DOC and SCF bits are not present.

7.3 End of Charge

The RAA489220 has two key indicators used in the charging process. These are the End-of-Charge Voltage (VEOC), and End-of-Charge Current (IEOC). The IEOC has dedicated threshold bits, while the VEOC threshold is the OV threshold minus the OV hysteresis. For example, with an OV Threshold of 4200mV with a -50mV hysteresis, the VEOC threshold is 4150mV. Before evaluating these features, modify these thresholds to simplify testing by navigating to the **Thresholds** tab and locating register 0x81 VCell OV. Click the **Read** button for the register to retrieve the present settings. For OV, enter 4100mV in the text box. For IEOC, check the boxes for 0x81.8:7 for IEOC 1 and IEOC 0. The IEOC label reads 3mV if the correct boxes are checked. Check boxes 0x81.6:4 for OV Hysteresis 6 -4. The OV Hysteresis label should update to -400mV. Finally, change the OVLO value to 4.2V. These settings are being configured with wide ranges so that they can easily trip power supplies with limited resolution. Click the **Write** button followed by **Read** to confirm the settings are correct. See [Figure 30](#) for the register.

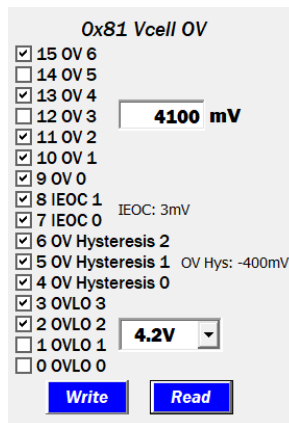


Figure 30. VEOC/IEOC Settings

Confirm the hardware is configured to induce a charging current by confirming that the terminals of the power supply are connected to the proper pins and that the charging FET is on. Turn on the power supply that is placed across the sense resistor with a value of 5mV on the output. Perform a system scan and read the results to confirm the CHRG1 bit is set in the **Faults and Indicators** box, (see [Figure 31](#)). VEOC and IEOC both require a CHRG1 signal before they trigger.

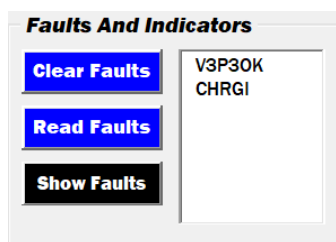


Figure 31. CHRG1 Indicator

Increase the voltage of the power supply connected to the resistor ladder so that it is above 37V, or 3700mV a cell. This causes the cells to cross the previously configured VEOC threshold. Trigger a system scan and read the results. The VEOC bit should not be set until performing two consecutive scans with the condition present. Perform another system scan and read the results; the VEOC bit does not appear in the **Faults and Indicators** box (see [Figure 32](#)).

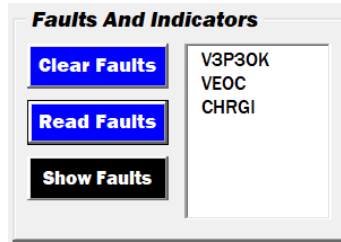


Figure 32. VEOC Indicator

To trigger the IEOC bit, the current measurement must fall beneath the IEOC threshold while staying above the CHRGI threshold of 600µV. Additionally, the VEOC bit must be set before IEOC. Lower the voltage across the sense resistor so that it is beneath 3mV but at above 600µV. Perform a system scan followed by a read measurement. The IEOC bit is now set (see Figure 33).

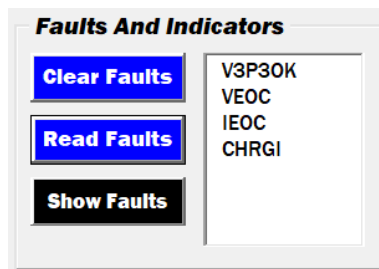


Figure 33. IEOC Indicator

7.4 CRC Communication

The RAA489220 has Cyclical Redundancy Check (CRC) for a more secure communication between master and slave. The GUI contains a demonstration of the CRC communication using the three communication command codes supported by the device. To evaluate these features, navigate to the **CRC** tab. Along with evaluating the CRC capabilities, this tab can be used to evaluate the command codes without CRC by clicking the command buttons while CRC is disabled. Try this by clicking on the **Command 0xC1 Read Faults and Status** button. The fields on the right update (see Figure 34).

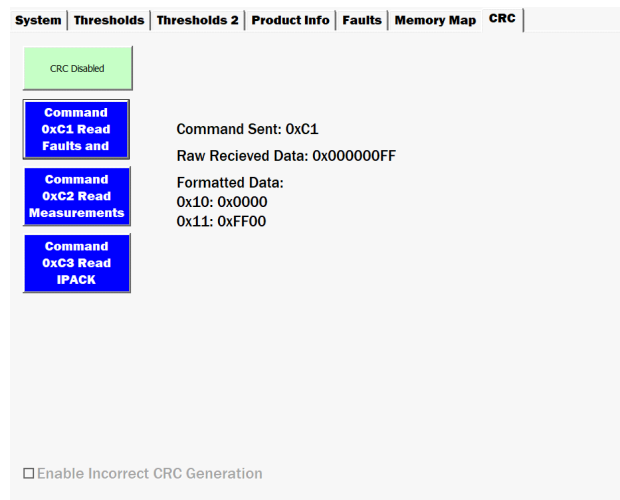


Figure 34. Non-CRC Command 0xC1

The Command Sent field shows which command code was sent to the device. The Raw Data field shows the data received from the device by the dongle, in the order it was received. The Formatted Data field breaks down the raw data into a readable format, organizing it into MSB -> LSB order and indicating which register the data originates from.

To enable CRC, click the button labeled **CRC Disabled**. It reads CRC Enabled as in [Figure 35](#). While the button indicates CRC is enabled, any command codes uses CRC communication. The GUI does not attempt to use CRC with any other functions besides the command code as it has not been designed to do so.

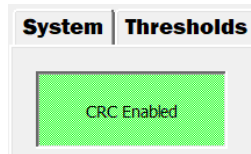


Figure 35. CRC Enabled Indicator

Click the **Command 0xC1 Read Faults** button. Along with the previous data fields, there are two additional fields, Received CRC and Calculated CRC. The Received CRC field displays the CRC byte received from the device. It should match the final byte of the Raw Data field. The Calculated CRC field displays the CRC calculated by the GUI based on the data received from the device. The two matching values indicate that the communication correctly executed. [Figure 36](#) provides an example of executing command 0xC1 with CRC Enabled. An oscilloscope connected to SCL and SDA can further help to understand the CRC format.

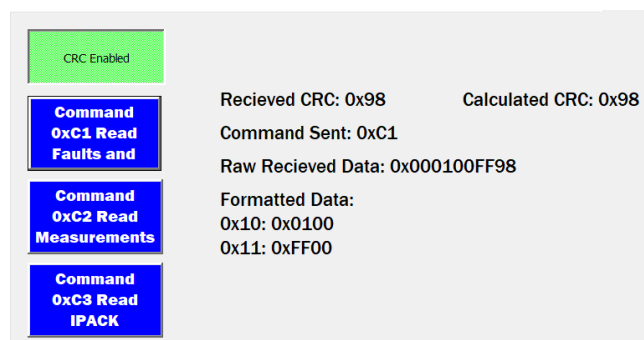


Figure 36. CRC Command 0xC1

7.5 Temperature Faults

The RAA489220 also features Discharge Over-Temperature (DOT) and Discharge Under-Temperature (DUT) protection, along with Charge Over-Temperature (COT) and Charge Under-Temperature (CUT) protection. To evaluate these features, a third power-supply output is required to apply the voltage across the thermistor to simulate the under-temperature and over-temperature conditions. If a third supply is not available, the supply placed across the sense resistor can instead be used for limited testing. When there is no current bit set, the discharge thresholds are always used.

To apply a voltage across the thermistor, connect the negative terminal of the supply to any easily accessible GND pin. Connect the positive terminal of the supply to J10 on the pin closest to the RAA489220 IC (see [Figure 37](#)). With the default thermistors, the room temperature equates to about 700mV, so set the power supply to that value.

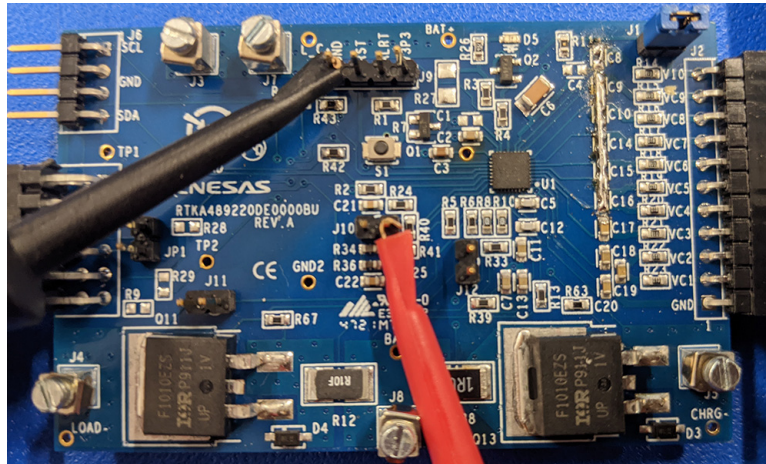


Figure 37. Applying Voltage across THERM2

When the supply has been configured across VTEMP, navigate to the **Thresholds 2** tab and locate register 0x83 Thermistor Threshold. Press the **Read** button for the register to update the GUI to reflect the current settings of the register (see Figure 38).

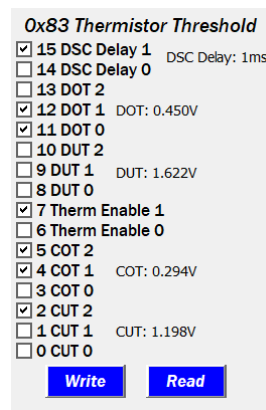


Figure 38. 0x83 Thermistor Threshold Defaults

There is no need to modify the defaults as they are easily reachable by the connected power supply. Configure the part to induce a discharge signal as in previous steps. Perform a system scan and read the results confirming that the DCHRG1 bit is set. When the DCHRG1 bit is set, lower the voltage until it is below 0.450V and perform a system scan. Read the results. The OTF bit is now set alongside the DCHRG1 bit, indicating there is a discharge over-temperature fault (see Figure 39).

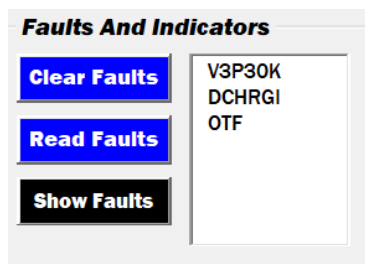


Figure 39. DCHRG1 & OTF Indicators

Click **Clear Faults** followed by **Read Faults** to confirm that the OTF bit cleared. Raise the voltage across the thermistor until it is above 1.622V. Perform two more scans and read the results. The DCHRG1 bit is now set alongside the UTF bit (see [Figure 40](#)). The combination of DCHRG1 and UTF indicates the fault was a discharge under-temperature.

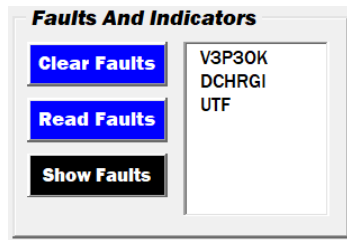


Figure 40. DCHRG1 and UTF Indicators

Evaluating the COT and CUT functionality is similar: reconfigure the power supply across the sense resistors to induce a charge current instead of discharge.

7.6 Auto SCAN

The RAA489220 has an Auto SCAN mode that performs device system scans at a programmable interval and has an autonomous FET response to faults and threshold violations. To enable Auto SCAN, navigate to the **Thresholds** tab and click the **Unlock Registers** button to verify that the registers can be modified. Locate register **0x80 Sys Config** and check the box for bit **0x80.8 Auto SCAN En**; next, press the **Write** button followed by the **Read** button. See [Figure 37](#) for the register.

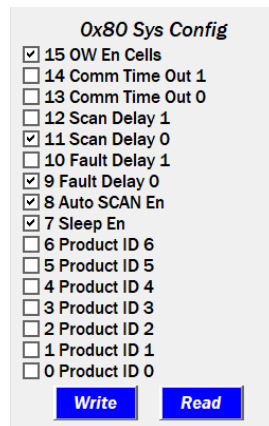


Figure 41. Auto SCAN Configuration

Note: The scan rate of the device is determined by bits 0x80.12 Scan Delay 1 and 0x80.11 Scan Delay 0.

7.7 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1	Bag and Ship with Board	PWB-10 Cell Resistor Ladder	Renesas Electronics America	BMS_PS_CELL 10Z
1	Bag and Ship with Board	PWB-PMOD Communications Dongle	Renesas Electronics America	RTKAPMODDONGLEV1Z REV B
1	Bag and Ship with Board	PWB-RAA489220 Evaluation Board	Renesas Electronics America	RTKA489220DE0000BU
1	Bag and Ship with Board	Cable - USB A MALE - MICRO-B MALE, 3FT. RoHS	Qualtek	3025010-03
12	Bag and Ship with Board	CONN Jumper Shorting Gold Flash	Sullins Connector Solutions	SPC02SYAN

8. Ordering Information

Part Number	Description
RTKA489220DE0000BU	Evaluation board
RTKAPMODDONGLEV1Z	Communications dongle with USB cable

9. Revision History

Revision	Date	Description
1.00	Oct 5, 2022	Initial release

Appendix

In addition to the manual, the appendix adds general information relevant to the user.

GUI Tabs

System Tab

The **System** tab contains registers that effect the general operation and status of the system. This tab is used to trigger system scans, enable the FETs, and check status bits and other functions. Also, the RSense value is modified on the **System** tab. RSense is the value that the GUI uses to calculate the current value in mA based on the mV value read from the device.

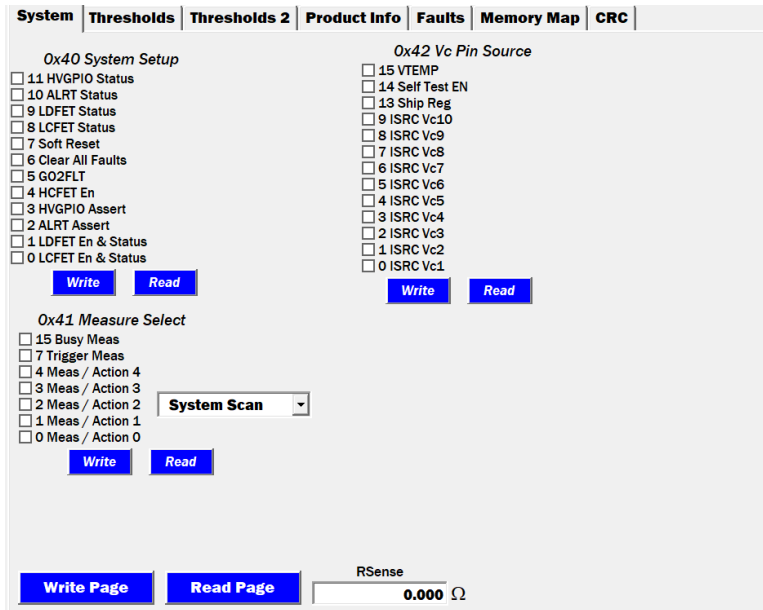


Figure 42. System Tab

Thresholds

The **Thresholds** tab contains the registers that adjust the thresholds for OV and UV and the register 0x80 that determines assorted system behavior. *Note:* Modification of the registers on the tab require writing the unlock sequence to register 0x6F.

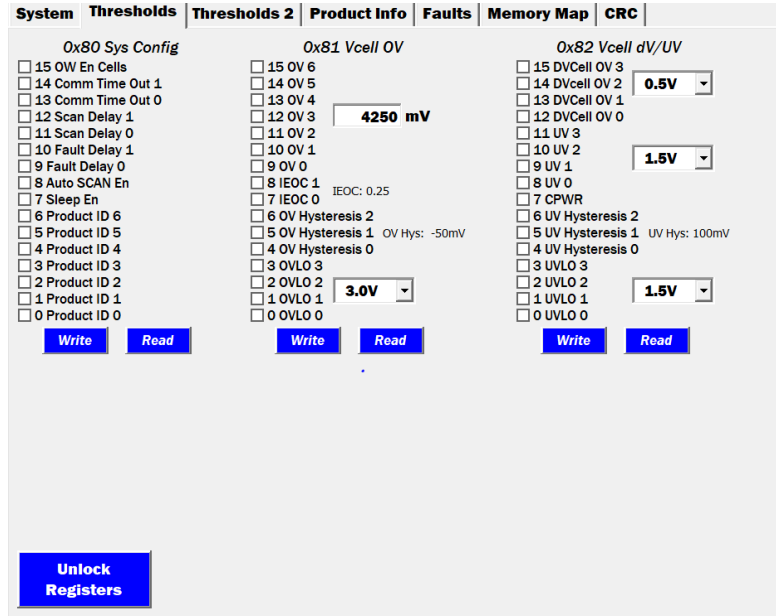


Figure 43. Thresholds Tab

Thresholds 2

The **Thresholds 2** tab contains registers related to fault thresholds of the device including current and temperature. These registers require the unlock sequence to be written before they can be modified.

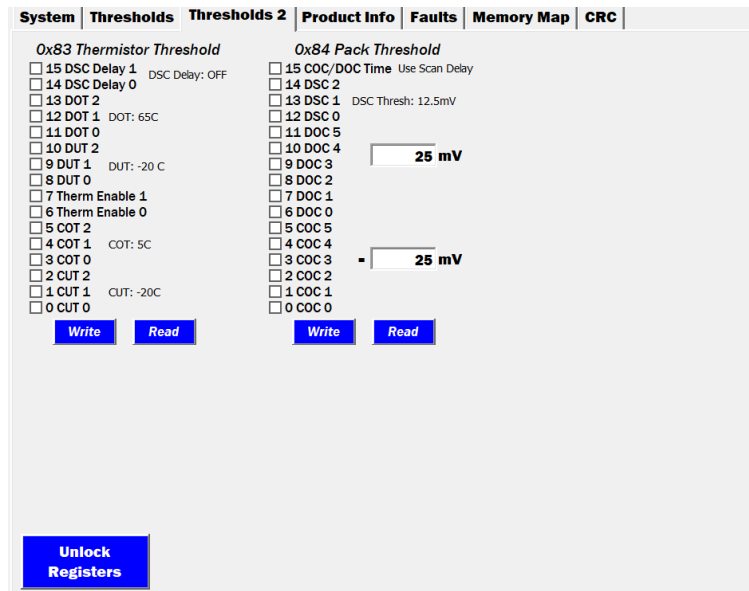


Figure 44. Thresholds 2 Tab

Product Info

The **Product Info** tab contains a registers that provide information about the device.

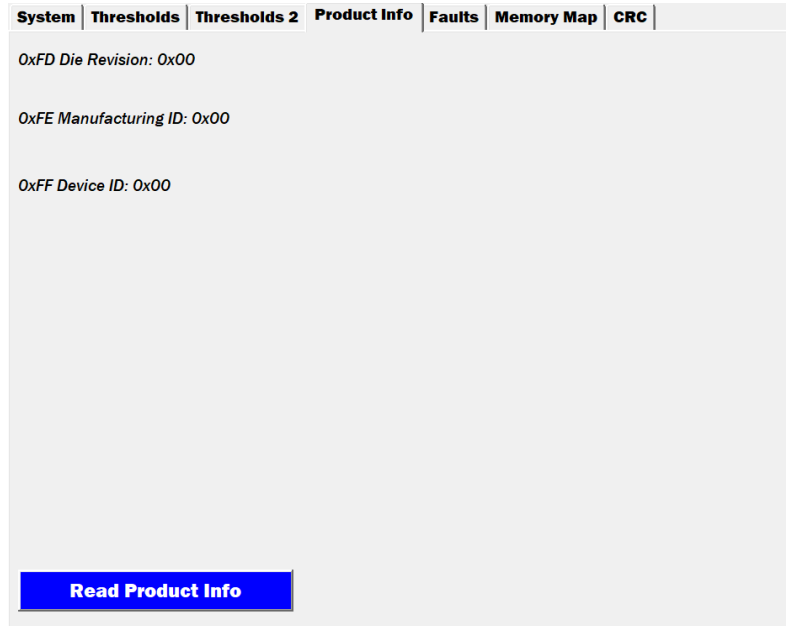


Figure 45. Product Info Tab

Faults Tab

The **Faults** tab contains the information display for the fault bits and the ability to modify the mask bits.

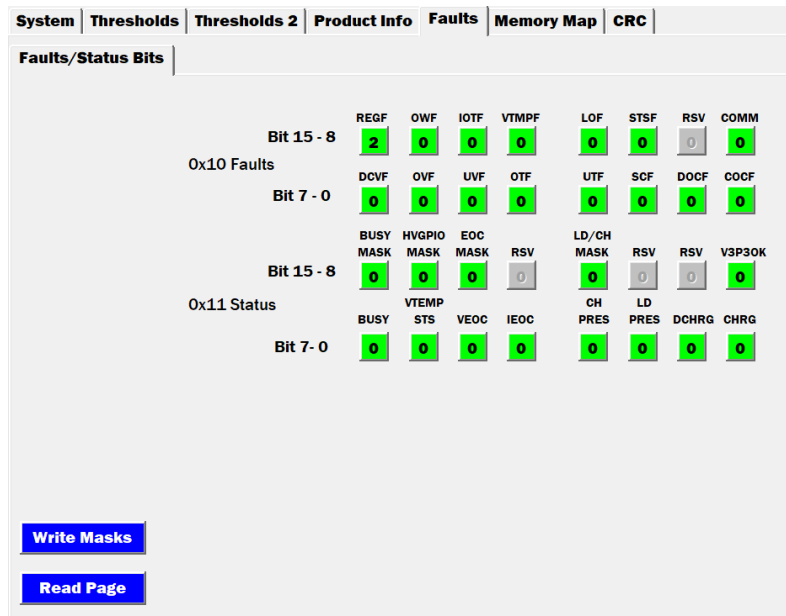


Figure 46. Faults Tab

Memory Map Tab

The **Memory Map** tab is used to read and write all the registers of the device. The registers can be read and written to individually by using the **R** and **W** buttons beside each register or simultaneously by using the **Read Registers** or **Write Registers** button.

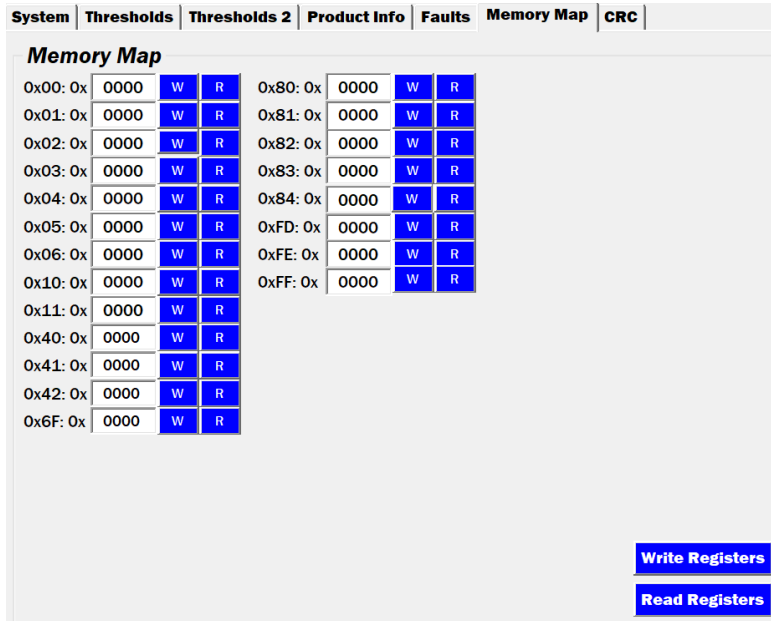


Figure 47. Memory Map Tab

CRC Tab

The **CRC** tab contains the ability to execute the command codes supported by the RAA489220 with and without CRC enabled, and the tab formats and displays all the relevant data related to these codes.

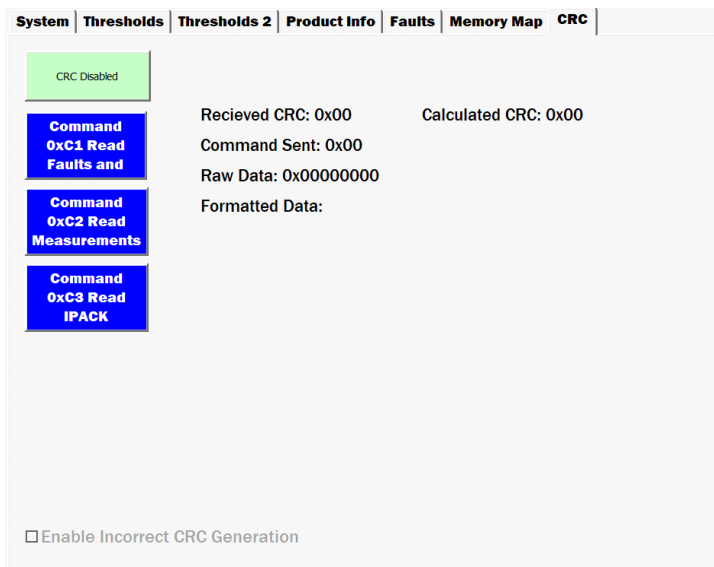


Figure 48. CRC Tab

Schematic

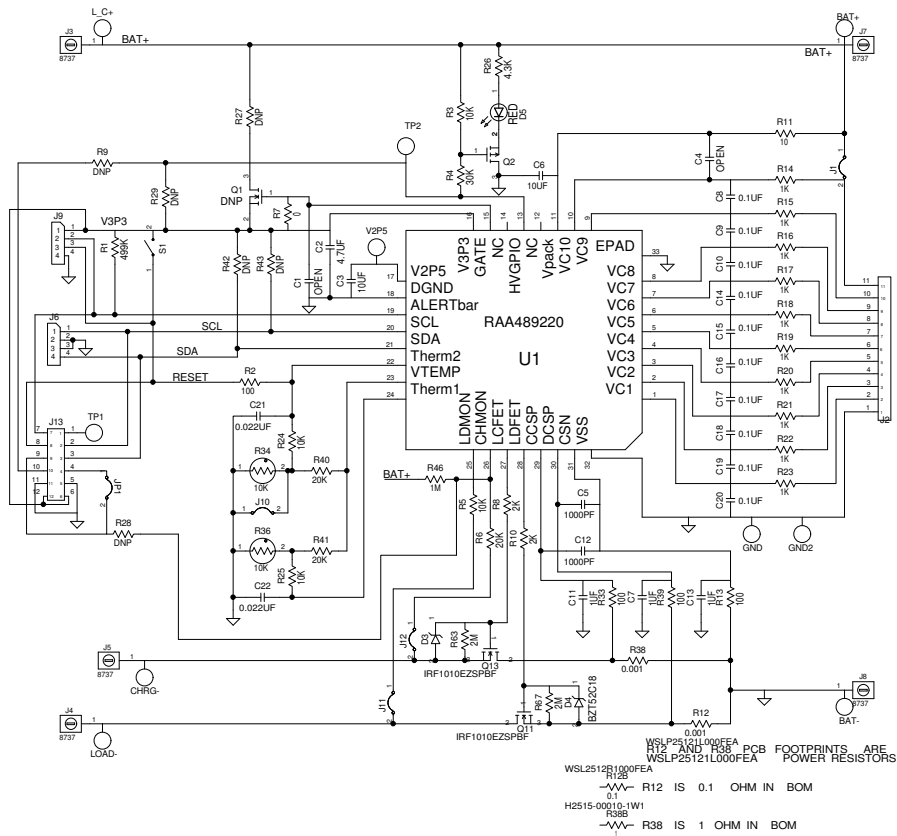


Figure 49. RTKA489220DK000BU Schematic

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