User's Manual

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RZ/N2H Group

RZ/N2H Evaluation Board
User's Manual

RZ/N Series for Real-Time Control

RZ Family

64-Bit & 32-Bit Arm®-Based High-End MPUs

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Precautions

This product is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

• Ensure attached cables do not lie across the equipment.

• Reorient the receiving antenna.

• Increase the distance between the equipment and the receiver.

• Connect the equipment into an outlet on a circuit different from that which the receiver is connected.

• Power down the equipment when not in use.

• Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

• The user is advised that mobile phones should not be used within 10 m of the product when in use.

• The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

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How to Use This Manual

1. Purpose and Target Readers

The intention of this manual is to assist users in understanding the hardware functionality and electrical characteristics of this product in overview. The target users of this manual are engineers designing sample code that runs on the product, with the use of various peripheral devices.

Though this manual includes an overview of the functionality of the product, it is not intended to be a guide for embedded programming or hardware design.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Handling Precautions section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the product. Be sure to refer to the latest versions of these documents. The newest versions of the listed documents are available on the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual	Explanation of the hardware specifications of the evaluation board	RZ/N2H Evaluation Board User's Manual	R20UT5522EJ (this manual)
Quick start guide	Explanation of the flow from turning on the power to confirming initial operation	RZ/N2H Evaluation Board Quick Start Guide	R20QS0056EJ
User's manual for the hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and descriptions of operation	RZ/T2H and RZ/N2H Groups User's Manual: Hardware	R01UH1039EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DIP	Dual In-line Package
DNF	Do Not Fit
EEPROM	Electronically Erasable Programmable Read Only Memory
ESC	EtherCAT Slave Controller
ESD	Electrostatic Discharge
EtherCAT	Ethernet for Control Automation Technology
GPT	General PWM Timer
I^2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
J-Link™	SEGGER debug probe
J-Link™ OB	SEGGER On-board debug probe
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MAC	Media Access Control
MCU	Micro Controller Unit
MPU	Micro Processor Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
OTP	One-Time Programmable (Memory)
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	PCI Express
POE	Port Output Enable
POEG	Port Output Enable for GPT
PWM	Pulse Width Modulation
RAM	Random Access Memory
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
ROM	Read Only Memory
SCI	Serial Communications Interface
SEI	System Error Interrupt
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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Table of Contents

1. Overview

1.1 Purpose

This evaluation board (hereafter referred to as this board) is an evaluation tool for a Renesas microprocessor. This manual describes the technical elements of the hardware of this board in detail. The method for installing software and the debugging environment are explained in the quick start guide.

1.2 Features

This board has the following features.

- Programming of a Renesas microprocessor
- Debugging of user code
- User circuits for switches, LEDs, and potentiometers

This board is equipped with all of the circuits that are required for operating the microprocessor.

1.3 Board Specifications

Table 1-1 and Table 1-2 list the board specifications.

Table 1-1 Board Specifications (1)

Item	Specification
Microprocessor	Part No.: R9A09G087M44GBG*1
	Package: 576-pin FCBGA
	On-chip memory: 2 Mbyte of RAM
On-board memory	OctaFlash: 512 Mbits
	QSPI serial flash memory: 128 Mbits
	I^2C EEPROM: 16 Kbits
	LPDDR4: 8 G-bytes
	eMMC: 32 G-bytes
Input clocks	RZ/N2H main: 25 MHz
	PCIe: 25 MHz
	USB-to-Serial Conversion: 12 MHz
Power supplies	Power inputs: 15-V/3-A USB PD supporting type-C connector (CN13) 15-V/3-A power jack (J1) for the AC adapter 24-V/3-A bipolar terminal block (J3)
	Power-supply IC: 24-V input, 15-V output
	Power-supply IC: 15-V input, 12-V output
	Power-supply IC: 15-V input, 5-V output
	Power-supply IC: 5-V input, 3.3-V output
	Power-supply IC: 5-V input, 1.8-V output
	Power-supply IC: 5-V input, 1.1-V output
	Power-supply IC: 5-V input, 0.8-V output
	Power-supply IC: 5-V input, 2.5-V output (for Ethernet PHY)
	Power-supply IC: 5-V input, 1.0-V output (for Ethernet PHY)
	Power-supply IC: 5-V input, 3.3-V output (for PCIe x4)
	Power-supply IC: 5-V input, 3.3-V output (for PCIe x1)
Debug interfaces	MIPI-10: 1.27-mm pitch, 10-pin box header (CN23)
	MIPI-20: 1.27-mm pitch, 20-pin box header (CN24)
	J-Link™ OB: USB micro-B (CN26)
Slide switch	Power-supply switch: Single-pole double-throw type × 1 (SW1)
DIP switches	Mode setting: 8 switches × 1
	Signal selection: 10 switches × 2, 8 switches × 9, 6 switches × 2, 4 switches × 3, and 2 switches × 1
	User switch: 4 switches × 1
Push switches	Reset switch × 1
	User switch × 3

Potentiometer (for A/D conversion)	Single-turn type (10 kΩ)
LEDs	For the power supply: (yellow) × 1 and (green) × 1
	For the user: (green) × 6, (yellow) × 1, and (red) × 2 Among the above, (green) × 4 and (red) × 1 are also used for indicating the EtherCAT status.
	Ethernet status: (green) × 4 and (yellow) × 4 (built in to each RJ-45)
	J-Link™ OB status: (yellow) × 1
Ethernet ports	Connector: RJ-45 × 4 (CN37, CN38, CN39, and CN40)
	PHY: Single-channel PHY × 4
USB	USB function: USB mini-B (CN8)
	USB host: USB type-A (CN7)
	USB MicroAB (CN9)*2
CAN	Connector*3: 2.54-mm pitch, 3 pins × 1 (CN35)
	CAN transceiver × 1

Notes: 1. Evaluation of the one-time programmable memory (OTP) is not possible with the device mounted on this product.
2. Cannot be used in this product.
3. The connector is not mounted on the product as shipped.

Table 1-2 Board Specifications (2)

Item	Specification
RS485	Connector*: 10 pins × 1 (CN36)
	RS485 transceiver × 1
USB-to-serial conversion interface	Connector: USB mini-B (CN27)
	Driver: FT2232HQ
Pmod™	PMOD-2A, 6A: 12-pin connector (CN28)
	PMOD-3A: 12-pin connector (CN31)
mikroBUS™	2.54-mm pitch, 8 pins × 2 (CN33 and CN34)
Grove	2.00-mm pitch, 4 pins × 2 (CN29 and CN32)
QWIIC	1.00-mm pitch, 4 pins × 1 (CN30)
Serial host interface	2.54-mm pitch, 14 pins × 1 (CN41)
LCDC	FPC connector, 45 pins × 1 (CN20)
SD	SD slot × 1 (CN21), microSD slot × 1 (CN22)
PCIe	The selectable configurations are 1 lane × 2 ports or 2 lanes × 1 port and root complex or endpoint.
	Connectors: 1 lane × 1 (CN12), 4 lanes × 1 (CN11, with only 2 lanes actually in use)
Pin headers (2.54-mm pitch)	ENCIF: 30 pins × 2 (CN44 and CN51), 22 pins × 1 (CN53)
	DSMIF: 30 pins × 2 (CN45 and CN46)
	GPT: 36 pins × 2 (CN49 and CN52)
	ETHSW: 10 pins × 1 (CN48)
	GMAC: 10 pins × 1 (CN47)
	External Bus*: 40 pins × 2 (CN42 and CN43)
	ADC: 10 pins × 2 (CN3 and CN4), 16 pins × 2 (CN5 and CN6)

Note: The connector is not mounted on the product as shipped.

2. Power Supply

2.1 Specifications of Power Supply

This board has a USB type-C connector (CN13), a power jack (J1), and a bipolar terminal block (J3). Power can be supplied from any one of these. Table 2-1 lists the specifications of power supply.

Table 2-1 Specifications of Power Supply

Connector	Specifications and Supply Voltage
CN13	USB power delivery (USB PD) supporting type-C, 15-V/3-A DC*1
J1	2.0-mm center-positive power jack, 15-V/3-A DC*2
J3	5.08-mm pitch bipolar terminal block, 24-V/3-A DC*3

Notes: 1. When supplying power through CN13, always use an AC adapter for USB supporting 15-V/3-A.
2. Though some of our boards, such as Renesas Starter Kit, require a 12-V or 5-V power supply, in the case of supplying power to this board through J1, always use a 15-V/3-A power supply and do not connect a 12-V or 5-V power supply.
3. When supplying power through J3, always use a stabilized power source that is capable of supplying 24-V/3-A.

2.2 Methods for Turning the Power On and Off

This board is equipped with a power switch (POWER_SW slide switch). When turning the power on, connect the power to CN13, J1, or J3 with the power switch turned off, and then turn the power switch on to start the power supply. To end the supply of power, turn the power switch off and then disconnect the power cable from CN13, J1, or J3. Figure 2-1 shows the arrangement and manipulation method of the power switch.

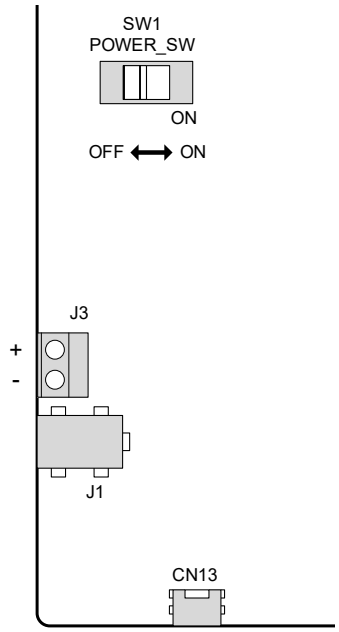


Figure 2-1 Arrangement and Method of Manipulating the Power Switch

2.3 Connectors for Current Measurement

This board has connectors for measuring currents, and each current value can be measured by inserting an ammeter between pins 1-2 of the given connector. Table 2-2 is a list of the connectors for measuring currents.

Table 2-2 List of Connectors for Current Measurement

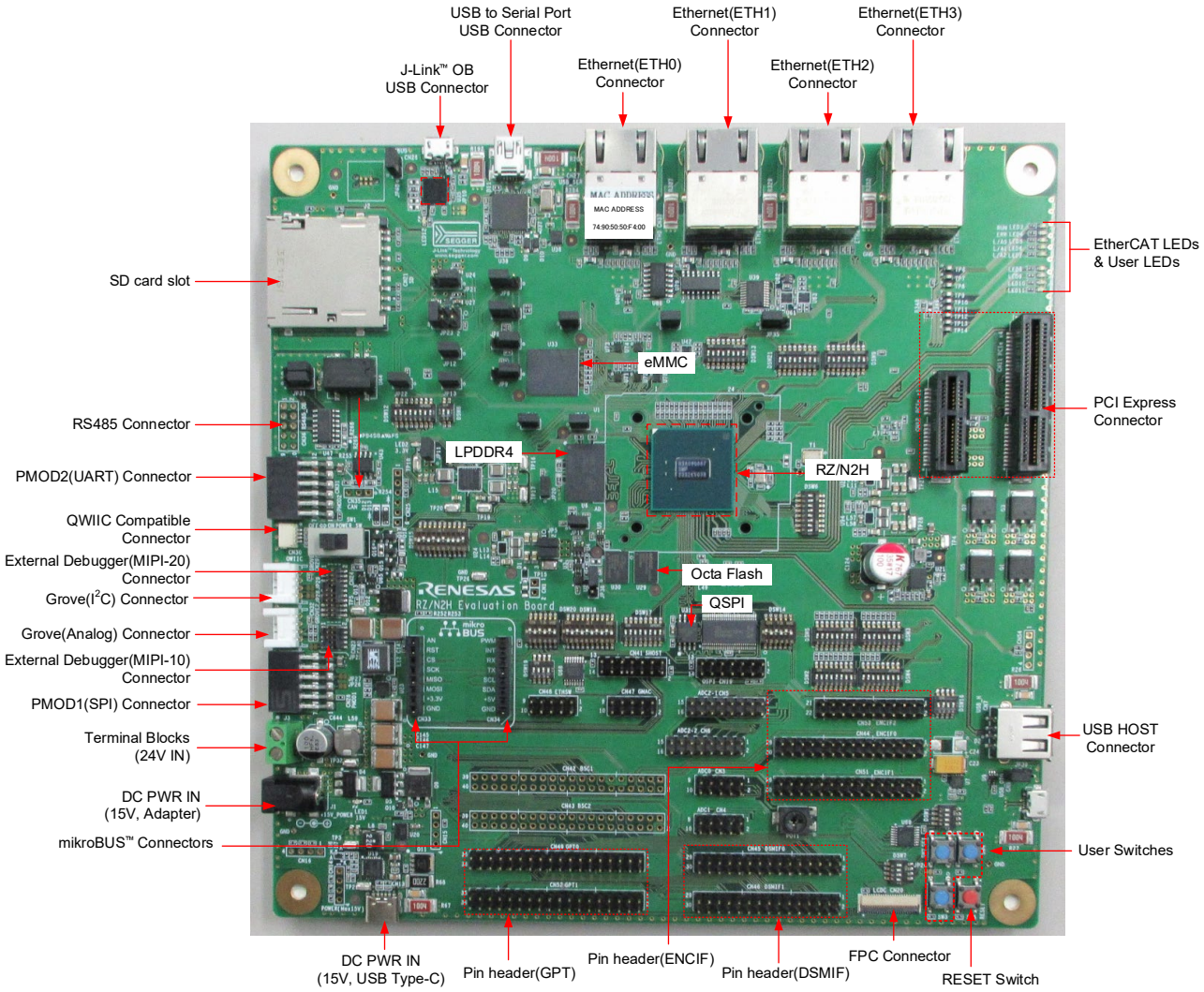
Connector	Purpose
JP5*	For measuring the current of the power supply (CPU0V8) line input to the 0.8-V power supply of the RZ/N2H
JP11	For measuring the current of the power supply (CPU3V3) line input to the 3.3-V power supply of the RZ/N2H
JP12	For measuring the current of the power supply (CPU_VCC1833_0) line input to the VCC1833_0 power supply of the RZ/N2H
JP13	For measuring the current of the power supply (CPU_VCC1833_1) line input to the VCC1833_1 power supply of the RZ/N2H
JP14	For measuring the current of the power supply (CPU_VCC1833_2) line input to the VCC1833_2 power supply of the RZ/N2H
JP15	For measuring the current of the power supply (CPU_VCC1833_3) line input to the VCC1833_3 power supply of the RZ/N2H
JP16	For measuring the current of the power supply (CPU1V1) line input to the 1.1-V power supply of the RZ/N2H
JP18	For measuring the current of the power supply (CPU1V8) line input to the 1.8-V power supply of the RZ/N2H
JP19	For measuring the current of the power supply (CPU_VCC1833_4) line input to the VCC1833_4 power supply of the RZ/N2H
JP20	For measuring the current of the power supply (CPU_VCC1833_5) line input to the VCC1833_5 power supply of the RZ/N2H
JP22	For measuring the current of the power supply (CPU_VCC1833_6) line input to the VCC1833_6 power supply of the RZ/N2H

Note: This is a 4-pin connector. To measure the current, insert an ammeter between pins 1-3 and 2-4.

3. Board Layout

3.1 Component Layouts

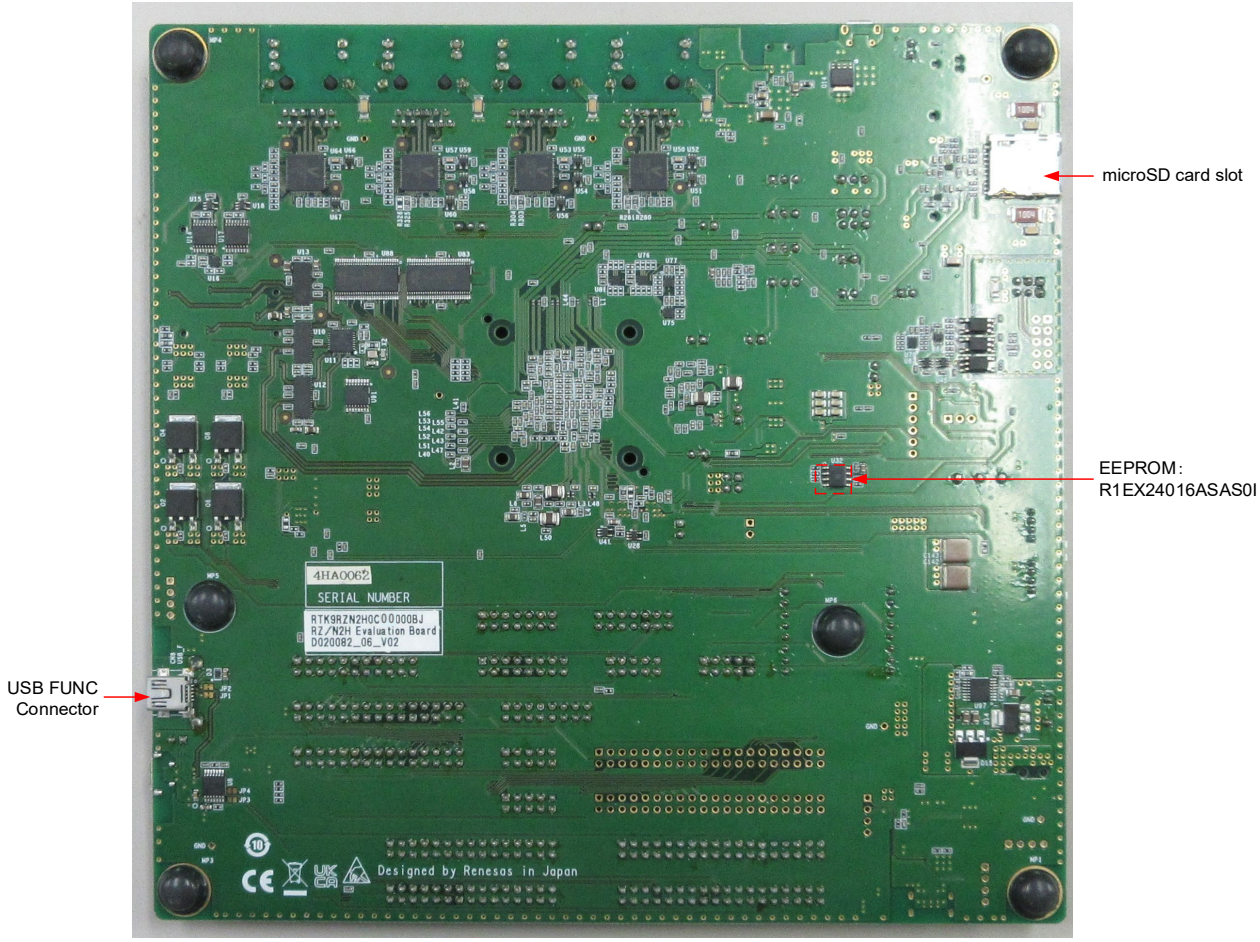
Figure 3-1 and Figure 3-2 show the component layouts on the top and on the soldered side of this board.



Notes: 1. For the details of each function, refer to chapter 7.

2. The MAC address shown in the figure is an example. Use a unique MAC address when running Ethernet software.

Figure 3-1 Board Layout (Top Side)



Note: The serial number (4HA0062) is an example.

Figure 3-2 Board Layout (Soldered Side)

3.2 Board Dimensions

Figure 3-3 shows the board dimensions and positions of connectors on this board. The through-hole connectors of pin headers are placed on a 2.54-mm pitch grid.

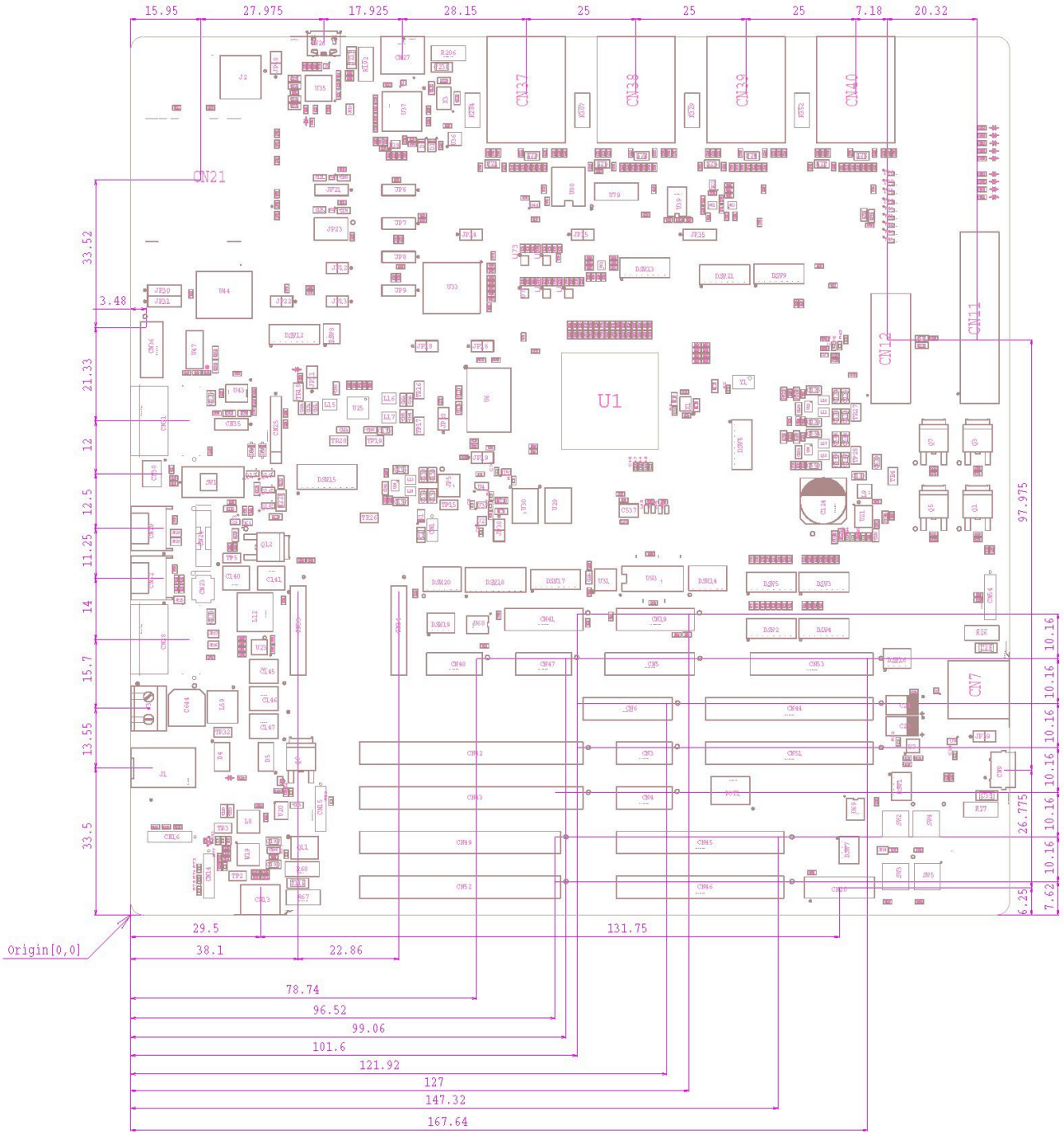


Figure 3-3 Board Dimensions (Unit: mm)

3.3 Arrangement of Components

For the arrangement of components on this board, refer to "11. Appendix".

4. Connections

4.1 Internal Connections of the Board

Figure 4-1 shows the connections between components of this board and the RZ/N2H.

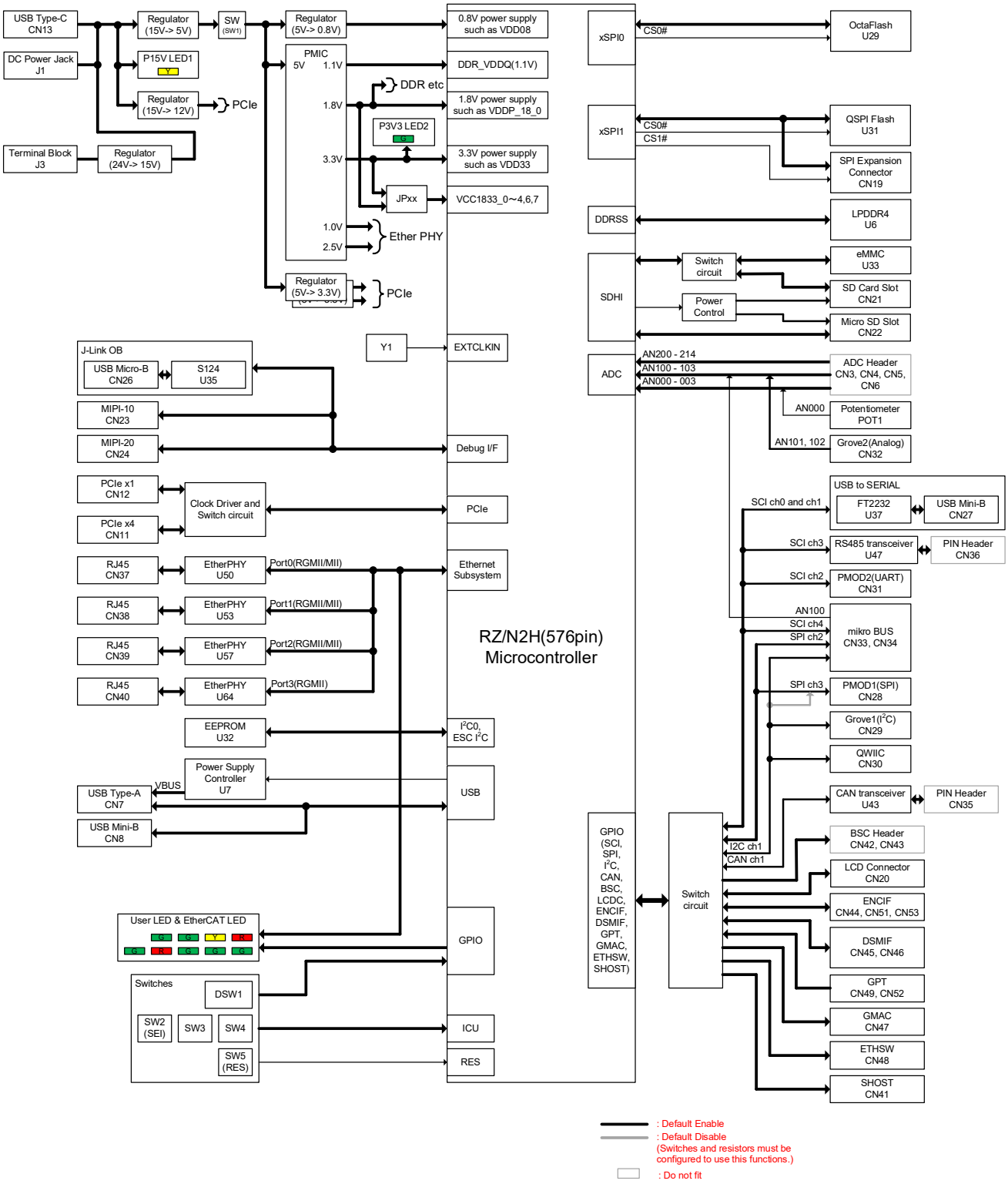


Figure 4-1 Internal Connections of the Board

4.2 Connections in the Debugging Environment

Figure 4-2 shows the connection between this board, the emulator, and the host PC. Figure 4-3 shows the connection between this board and the host PC when J-Link™ OB on this board is used.

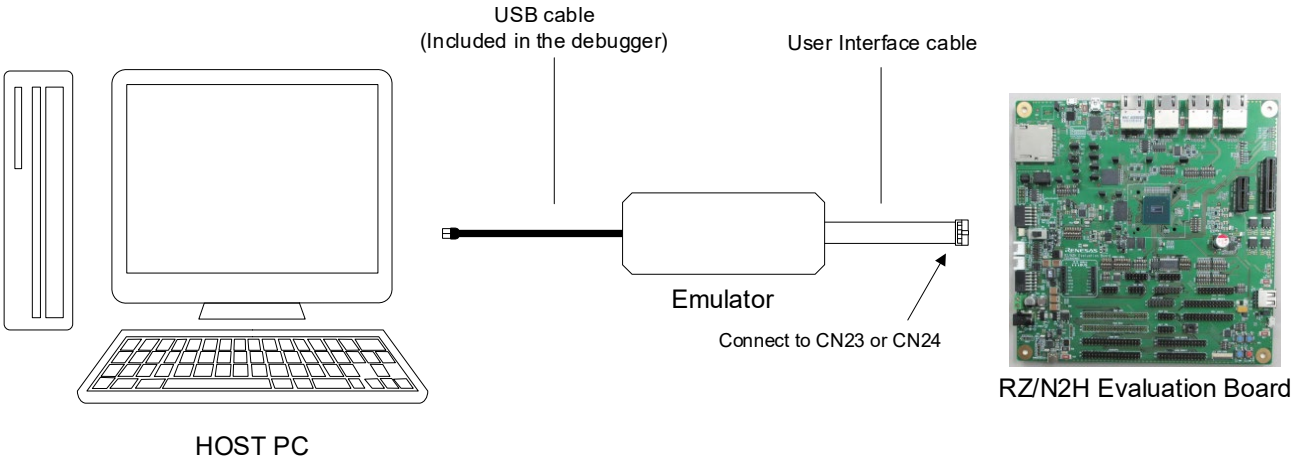


Figure 4-2 Connections in the Debugging Environment (with an Emulator)

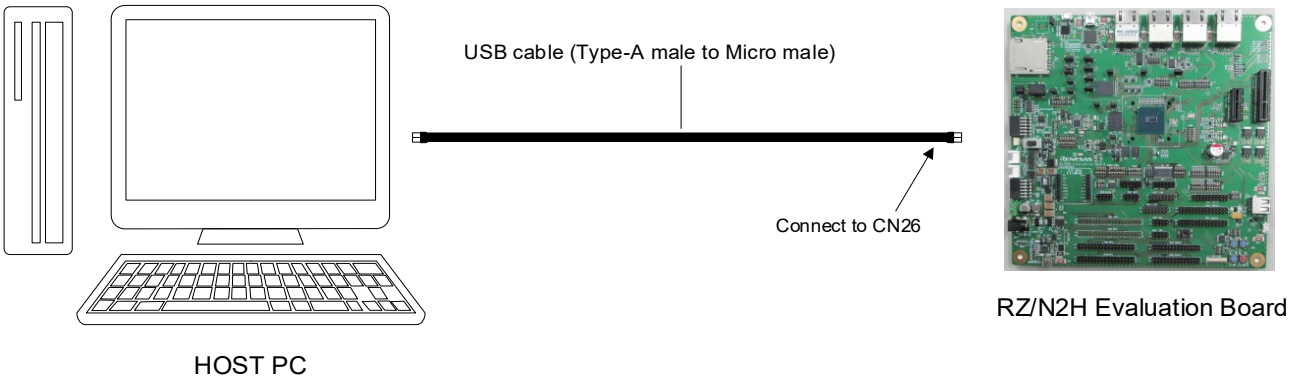


Figure 4-3 Connections in the Debugging Environment (with J-Link™ OB)

5. List of RZ/N2H Pin Functions

Table 5-1 to Table 5-24 are lists of the functions of RZ/N2H pins used on this board. **Text in bold blue type** in the tables indicates the settings at the time of shipment of the board and the functions available with those settings. However, a signal that is connected to multiple connectors can be used in only one of the connectors at a time.

Table 5-1 List of RZ/N2H Pin Function Selections (1)

Pin No.	Pin Name	Function	Description	Connector	Remarks
A1	VSS				
A2	P09_4/D13/MTIOC6B/GTIOC04_0A/GTIOC10_0A/MCLK70/DISP_CLK/DUEI13/HDSL07_MOSI1	**D13**	**D13 of external bus**	**CN43-31**	
		GTIOC04_0A	**Input capture / output compare / PWM output pin**	**CN52-15**	
		DISP_CLK	**Clock of Display**	**CN20-16**	
A3	P10_6/IRQ0/A3/MTIOC0B/GTIOC05_0A/DE0/MCLK21/DISP_DATAR6/HDSL08_MOSI1/POUTA	P10_6	CLKREQ output of PCIex1	CN12_B12	DSW4-2: OFF
		IRQ0	**PRSNT2 input of PCIex1**	**CN12_B17**	**DSW4-2: ON**
		A3	**A3 of external bus**	**CN42-7**	
		GTIOC05_0A	**Input capture / output compare / PWM output pin**	**CN52-27**	
		DISP_DATAR6	**Display data R6**	**CN20-35**	
A4	P10_7/IRQ9/A4/MTIC5U/GTIOC05_0B/GTIOC00_3A/SCK1/MDAT21/DISP_DATAR7/HDSL08_CLK2/POUTB	P10_7	CLKREQ output of PCIex4	CN11_B12	DSW4-1: OFF
		IRQ9	**PRSNT2 input of PCIex4**	**CN11_B17, B31**	**DSW4-1: ON**
		A4	**A4 of external bus**	**CN42-9**	
		GTIOC05_0B	**Input capture / output compare / PWM output pin**	**CN52-28**	
		DISP_DATAR7	**Display data R7**	**CN20-34**	
A5	P11_0/IRQ13/A5/GTIOC00_3B/ESC_RESETOUT#/RXD1/SCL1/MISO1/MCLK22/DISP_DATAG0/HDSL08_SEL2/POUTZ	A5	A5 of external bus	CN42-13	DSW12-3: ON, DSW12-4: OFF
		DISP_DATAG0	Display data G0	CN20-33	
		ESC_RESETOUT#	**ESC_RESETOUT# of Ethernet Port0, Port1**		**DSW12-3: OFF, DSW12-4: ON**
			ESC_RESETOUT# of Ethernet Port2		**DSW12-3: OFF, DSW12-4: ON,** DSW8-1: OFF, DSW8-2: ON
A6	P13_4/D28/GTIOC03_3B/RXD3/SCL3/MISO3/SPI_SSL31/MCLK40/ENCIFCK13/SCKE09/HDSL10_SEL2	D28	D28 of external bus	CN43-26	DSW2-4: ON
		MCLK40	Clock of DSMIF	CN46-17	
		RXD3	**RXD3 of RS485**		**DSW2-4: OFF**
A7	P13_7/IRQ14/D31/GTIOC06_4A/GTIOC04_3B/CTS3#/MDAT41/ENCIFDI13/RXDE09/HDSL11_LINK	**IRQ14**	**MDINT of Ethernet Port2**		**DSW13-7: OFF, DSW13-8: ON**
		D31	D31 of external bus	CN43-32	DSW13-7: ON, DSW13-8: OFF
		MDAT41	Data of DSMIF	CN46-16	
A8	P14_0/IRQ5/A0/GTIOC06_4B/ETHSW_PTPOUT2/ESC_SYNC0/DE3/MCLK42/HDSL11_SMPL	**IRQ5**	**IRQ of Display**	**CN20-4**	
		A0	**A0 of external bus**	**CN42-1**	
		MCLK42	**Clock of DSMIF**	**CN46-13**	
		ETHSW_PTPOUT2	**Timer pulse output of ETHSW**	**CN48-5**	
		DE3	**DE of RS485**		
A9	P14_7/IRQ9/POE11#/GTIOC09_3A/CMTW0_TOC1/ESC_I2CDATA/IIC_	ESC_I2CDATA/IIC_SDA0	SDA of EEPROM		DSW15-5: ON, DSW15-6: OFF

	SDA0/SD0_IOVS/MCLK32/SI02#/HDSL11_MISO2	**P14_7**	**Control of user LED1**		**DSW15-5: OFF, DSW15-6: ON**
A10	P14_6/IRQ8/POE10#/GTIOC06_2B/GTIOC09_2B/CMTW0_TIC1/ESC_I2CCLK/DE4/IIC_SCL0/SD0_PWEN/DISP_DATAG6/TST_OUT02/HDSL11_SEL2	ESC_I2CCLK/IIC_SCL0	SCL of EEPROM		**DSW15-8: OFF,** DSW15-9: ON, DSW15-10: OFF
		P14_6	**Control of user LED0**		**DSW15-8: OFF, DSW15-9: OFF, DSW15-10: ON**
		DISP_DATAG6	Display data G6	CN20-27	DSW15-8: ON, **DSW15-9: OFF,** DSW15-10: OFF
A11	P17_1/IRQ13/GTIOC03_2A/SD1_DATA2/DUEI06/HDSL13_CLK2	**SD1_DATA2**	**DAT2 of SD1**	**CN22-1**	
A12	P18_5/IRQ2/A13/GTIOC07_3B/GTADSM4_1/SS1#/CTS1#/RTS1#/CANTX1/MDAT11/DISP_DATAB6/ENCIFOE13/ENCIFOE14/DEE09/DEE10/HDSL14_MISO2	**A13**	**A13 of external bus**	**CN42-31**	
		MDAT11	**Data of DSMIF**	**CN45-16**	
		DISP_DATAB6	**Display data B6**	**CN20-19**	
A13	P18_3/IRQ0/A11/GTADSM03_1/RTCAT1HZ/ETH1_COL/GMAC1_MDIO/RXD1/SCL1/MISO1/CANTX0/SD1_IOVS/MDAT10/DISP_DATAB4/HDSL14_CLK2	**A11**	**A11 of external bus**	**CN42-25**	
		MDAT10	**Data of DSMIF**	**CN45-18**	
		DISP_DATAB4	**Display data B4**	**CN20-21**	
A14	P20_5/ETH0_TXEN/DUEI11/HDSL00_LINK	**ETH0_TXEN**	**TXEN of Ethernet Port0**		
A15	P20_1/MDV/ETH0_TXD0	**MDV**	**Input of MDV setting**		
		ETH0_TXD0	**TXD0 of Ethernet Port0**		
A16	P21_2/ETH0_RXD3/CANTXDP0/SI12#/HDSL00_MOSI1	**ETH0_RXD3**	**RXD3 of Ethernet Port0**		
A17	P21_3/ETH0_RXDV/DUEI13/HDSL00_CLK2	**ETH0_RXDV**	**RXDV of Ethernet Port0**		
A18	P22_4/IRQ6/A21/GTETRGD/ETH0_COL/SS5#/CTS5#/RTS5#/CANTXDP0/TST_OUT14/HDSL01_MOSI1	**ETH0_COL**	**COL of Ethernet Port0**		
A19	P24_5/ETH1_TXCLK/HDSL03_CLK1	**ETH1_TXCLK**	**TXCLK of Ethernet Port1**		
A20	P25_0/MD2/ETH1_TXD2/CANRXDP0	**MD2**	**Input of MD2 setting**		
		ETH1_TXD2	**TXD2 of Ethernet Port1**		
A21	P25_2/MDW1/ETH1_TXEN	**MDW1**	**Input of MDW1 setting**		
		ETH1_TXEN	**TXEN of Ethernet Port1**		
A22	P24_6/MD0/ETH1_TXD0	**MD0**	**Input of MD0 setting**		
		ETH1_TXD0	**TXD0 of Ethernet Port1**		
A23	P27_3/MTIOC2A/GTIOC08_3A/GTIOC02_1A/GMAC1_PTPTRG1/SCK0/CANRXDP1/SPI_MOSI0/HSPI_IO1/ENCIFCK14/SCKE10/HDSL04_MISO2	**P27_3**	**User DIPSW1**		**DSW2-3: ON**
		GMAC1_PTPTRG1	PTPTRG of GMAC1	CN47-4	DSW2-3: OFF
		ENCIFCK14	Clock of ENCIF	CN53-11	
		HSPI_IO1	IO1 of SHOSTIF	CN41-11	
A27	VSS				

Table 5-2 List of RZ/N2H Pin Function Selections (2)

Pin No.	Pin Name	Function	Description	Connector	Remarks
B1	P09_5/D14/MTIOC6D/GTIOC04_0B/GTIOC10_0B/MDAT70/DISP_HSYNC/TST_OUT13/HDSL07_CLK2	**D14**	**D14 of external bus**	**CN43-33**	
		GTIOC04_0B	**Input capture / output compare / PWM output pin**	**CN52-16**	
		DISP_HSYNC	**HSYNC of Display**	**CN20-14**	
B2	P10_1/IRQ7/WAIT#/MTIOC7D/GTIOC04_2B/GTIOC10_2B/SCK0/MDAT72/DISP_DATAR1/SI14#/HDSL08_LINK	**WAIT#**	**WAIT# of external bus**	**CN43-34**	
		MTIOC7D	**PWM of mikroBUS™**	**CN34-1**	
		GTIOC04_2B	**Input capture / output compare / PWM output pin**	**CN52-20**	
		DISP_DATAR1	**Display data R1**	**CN20-40**	
B3	P10_2/IRQ1/CS0#/MTCLKC/MTIOC2A/GTIOC04_3A/GTIOC10_3A/RXD0/SCL0/MISO0/MCLK10/MCLK00/DISP_DATAR2/ENCIFCK04/SCKE04/HDSL08_SMPL	**P10_1/IRQ1**	**WAKE# of PCIe x1**	**CN12-B11**	
		CS0#	**CS0# of external bus**	**CN42-32**	
		ENCIFCK04	**Input capture / output compare / PWM output pin**	**CN44-21**	
		DISP_DATAR2	**Display data R2**	**CN20-39**	
B4	P10_5/A2/MTIOC1B/MTIOC0A/GTIOC04_4B/CTS0#/MDAT11/MDAT01/DISP_DATAR5/ENCIFDI04/RXDE04/HDSL08_MISO1	**A2**	**A2 of external bus**	**CN42-5**	
		ENCIFDI04	**Data input of ENCIF**	**CN44-27**	
		DISP_DATAR5	**Display data R5**	**CN20-36**	
B5	VSS				
B6	P12_7/IRQ2/D23/GTIOC05_4B/CMTW1_TOC1/CTS2#/SD0_DATA5/MDAT10/ENCIFDI05/RXDE05/HDSL10_CLK1	P12_7/IRQ2	WAKE# of PCIe x4	CN11-B11	DSW5-1: OFF, DSW5-2: OFF
		D23	D23 of external bus	CN43-14	
		CTS2#	CTS of PMOD2	CN31-1	
		SD0_DATA5	**Data DAT5 of eMMC**		**DSW5-1: ON, DSW5-2: ON**
B7	P13_0/D24/GTIOC02_3A/DE2/SPI_RSPCK3/SD0_DATA6/MCLK00/ENCIFCK12/ENCIFCK03/SCKE08/SCKE03/HDSL10_SEL1	D24	D24 of external bus	CN43-16	DSW5-1: OFF, DSW5-2: OFF
		MCLK00	Clock of DSMIF	CN45-7	
		SPI_RSPCK3	SCK of PMOD1	CN28-4	DSW5-1: OFF, DSW5-2: OFF, **JP27: Short, JP29: Open**
		SD0_DATA6	**Data DAT6 of eMMC**		**DSW5-1: ON, DSW5-2: ON**
B8	P12_4/IRQ1/D20/GTIOC05_3A/CMTW1_TIC0/RXD2/SCL2/MISO2/SD0_DATA2/MCLK02/ENCIFCK05/SCKE05/HDSL09_MOSI2	D20	D20 of external bus	CN43-8	DSW5-1: OFF, DSW5-2: OFF
		MCLK02	Clock of DSMIF	CN45-3	
		RXD2	RXD2 of PMOD2	CN31-3	
		SD0_DATA2	**Data DAT2 of eMMC**		**DSW5-1: ON, DSW5-2: ON**
			Data DAT2 of SD0	CN21-9	DSW5-1: OFF, DSW2-2: ON
B9	P14_4/DACK/POE4#/GTIOC06_1B/GTIOC09_1B/GTIOC06_3A/CMTW0_TIC0/ESC_IRQ/SS4#/CTS4#/RTS4#/SD1_WP/DISP_DATAG4/MBX_HINT#/ENCIFDO00/TXDE00/HDSL11_MOSI1	**DACK**	**DACK of external bus**	**CN42-26**	**DSW20-3: ON, DSW20-4: OFF**
		DISP_DATAG4	**Display data G4**	**CN20-29**	
		MBX_HINT#	**HINT# of SHOSTIF**	**CN41-13**	
		ENCIFDO00	**Data output of ENCIF**	**CN44-7**	
B10	VSS				
B11	P17_2/IRQ14/GTIOC03_2B/SD1_DATA3/TST_OUT06/HDSL13_SEL2	**SD1_DATA3**	**Data DAT3 of SD1**	**CN22-2**	

B12	P18_1/IRQ15/A9/GTADSM2_1/GTIOC07_3A/ESC_LEDERR/CTS0#/CANTXDP0/SD1_IOVS/DISP_DATAB2/SI08#/HDSL14_MISO1	A9	A9 of external bus	CN42-21	DSW18-9: OFF, DSW18-10: ON
		DISP_DATAB2	Display data B2	CN20-23	
		ESC_LEDERR	**Control of LED5 ERR**		**DSW18-9: ON, DSW18-10: OFF**
B13	P18_4/IRQ1/A12/GTIOC07_3A/GTADSM4_0/ESC_LEDSTER/TXD1/SDA1/MOSI1/CANRX1/MCLK11/DISP_DATAB5/ENCIFCK13/ENCIFCK14/SCKE09/SCKE10/HDSL14_SEL2	**A12**	**A12 of external bus**	**CN42-27**	
		MCLK11	**Clock of DSMIF**	**CN45-15**	
		DISP_DATAB5	**Display data B5**	**CN20-20**	
B14	P20_0/ETH0_TXCLK/HDSL15_MOSI2	**ETH0_TXCLK**	**TXCLK of Ethernet Port0**		
B15	VSS				
B16	P20_4/ETH0_TXD3/CANTX0	**ETH0_TXD3**	**TXD3 of Ethernet Port0**		
B17	P22_2/A23/GTETRGB/ETH0_RXER/RXD5/SCL5/MISO5/CANRX0/HDSL01_SEL1	**ETH0_RXER**	**RXER of Ethernet Port0**		
B18	P22_5/IRQ7/A20/GTETRGSA/GMAC0_PTPTRG0/ESC_LATCH0/CTS5#/CANRX1/SD0_CD/SI14#/HDSL01_CLK2	GMAC0_PTPTRG0	PTPTRG0 of GMAC0	CN47-1	DSW15-3: ON, DSW15-4: OFF
		SD0_CD	**CD of SD0**	**CN21-10**	**DSW15-3: OFF, DSW15-4: ON**
B19	VSS				
B20	P25_1/MDW0/ETH1_TXD3/CANTXDP0	**MDW0**	**Input of MDW0 setting**		
		ETH1_TXD3	**TXD3 of Ethernet Port1**		
B21	P24_7/MD1/ETH1_TXD1	**MD1**	**Input of MD1 setting**		
		ETH1_TXD1	**TXD1 of Ethernet Port1**		
B22	P26_5/IRQ12/CANTX0/ENCIFCK01/SCKE01/HDSL04_CLK1	**IRQ12**	**Interrupt of Ethernet Port1**		
B23	P27_1/IRQ2/GTIOC02_0A/ETH1_COL/CANRX1/SPI_SSL03/HSPI_CS#/HDSL04_CLK2	**ETH1_COL**	**COL of Ethernet Port1**		**DSW13-5: ON, DSW13-6: OFF**
		HSPI_CS#	CS# of SHOSTIF	CN41-4	DSW13-5: OFF, DSW13-6: ON
B24	P27_2/IRQ3/GTIOC02_0B/GMAC1_PTPTRG0/ESC_LEDERR/CANTX1/SPI_RSPCK0/HSPI_IO0/HDSL04_SEL2	**P27_2**	**User DIPSW0**		**DSW2-3: ON**
		GMAC1_PTPTRG0	PTPTRG of GMAC1	CN47-3	DSW2-3: OFF
		HSPI_IO0	IO0 of SHOSTIF	CN41-12	

Table 5-3 List of RZ/N2H Pin Function Selections (3)

Pin No.	Pin Name	Function	Description	Connector	Remarks
C1	P09_6/D15/MTIOC7A/GTIOC04_1A/GTIOC10_1A/MCLK71/DISP_VSYNC/SI13#/HDSL07_SEL2	**P09_6**	**RESET of PMOD1**	**CN28-8**	
		D15	**D15 of external bus**	**CN43-35**	
		GTIOC04_1A	**Input capture / output compare / PWM output pin**	**CN52-17**	
		DISP_VSYNC	**VSYNC of Display**	**CN20-13**	
C2	P10_0/IRQ4/WE1#/MTIOC7B/GTIOC04_2A/GTIOC10_2A/MCLK72/DISP_DATAR0/TST_OUT14/HDSL07_MOSI2	**P10_0**	**RST of mikroBUS™**	**CN33-2**	
		WE1#	**WE1# of external bus**	**CN43-38**	
		GTIOC04_2A	**Input capture / output compare / PWM output pin**	**CN52-19**	
		DISP_DATAR0	**Display data R0**	**CN20-41**	
C3	P10_3/IRQ2/RD#/MTCLKD/MTIOC2B/GTIOC04_3B/GTIOC10_3B/TXD0/SDA0/MOSI0/MDAT10/MDAT00/DISP_DATAR3/ENCIFOE04/DEE04/HDSL08_CLK1	**RD#**	**RD# of external bus**	**CN42-39**	
		ENCIFOE04	**Output enable of ENCIF**	**CN44-23**	
		DISP_DATAR3	**Display data R3**	**CN20-38**	
C4	P09_7/WE0#/MTIOC7C/GTIOC04_1B/GTIOC10_1B/MDAT71/DISP_DE/DUEI14/HDSL07_MISO2	**P09_7**	**RESET of PMOD2**	**CN31-8**	
		WE0#	**WE0# of external bus**	**CN43-36**	
		GTIOC04_1B	**Input capture / output compare / PWM output pin**	**CN52-18**	
		DISP_DE	**DE of Display**	**CN20-12**	
C5	P10_4/IRQ3/A1/MTIOC1A/GTIOC04_4A/SS0#/CTS0#/RTS0#/MCLK11/MCLK01/DISP_DATAR4/ENCIFDO04/TXDE04/HDSL08_SEL1	**A1**	**A1 of external bus**	**CN42-3**	
		ENCIFDO04	**Data output of ENCIF**	**CN44-25**	
		DISP_DATAR4	**Display data R4**	**CN20-37**	
C6	P13_1/D25/GTIOC02_3B/SPI_MOSI3/SD0_DATA7/MDAT00/ENCIFOE12/ENCIFOE03/DEE08/DEE03/HDSL10_MISO1	D25	D25 of external bus	CN43-18	DSW5-1: OFF, DSW5-2: OFF
		SPI_MOSI3	MOSI of PMOD1	CN28-2	
		MDAT00	Data of DSMIF	CN45-8	
		SD0_DATA7	**Data DAT7 of eMMC**		**DSW5-1: ON, DSW5-2: ON**
C7	P13_5/IRQ4/D29/GTIOC06_3A/TXD3/SDA3/MOSI3/SPI_SSL32/MDAT40/ENCIFOE13/DEE09/HDSL10_MISO2	**D29**	**D29 of external bus**	**CN43-28**	
		TXD3	**TXD3 of RS485**		**DSW2-4: OFF**
		MDAT40	**Data of DSMIF**	**CN46-18**	
C8	P12_0/D16/MTIC5V/GTIOC05_1A/CMTW0_TIC0/CANRX1/SD0_CLK/DUEI01/HDSL09_MOSI1	D16	D16 of external bus	CN43-37	DSW5-1: OFF, DSW5-2: OFF
		GTIOC05_1A	Input capture / output compare / PWM output pin	CN52-29	
		CANRX1	RX of CAN interface		DSW5-1: ON, DSW5-2: OFF
		SD0_CLK	**Clock of eMMC**		**DSW5-1: ON, DSW5-2: ON**
			Clock of SD0	CN21-5	DSW5-1: OFF, DSW2-2: ON
C9	P14_1/RD/WR#/GTIOC06_0A/GTIOC09_0A/GTIOC05_3A/RTCAT1HZ/SCK4/SD0_CD/MDAT42/DISP_DATAG1/DUEI02/HDSL11_CLK1	**RD/WR#**	**RD/WR# of external bus**	**CN42-38**	
		MDAT42	**Data of DSMIF**	**CN46-14**	
		DISP_DATAG1	**Display data G1**	**CN20-32**	
C10	P14_3/IRQ6/DREQ/POE0#/GTIOC06_1A/GTIOC09_1A/ESC_LINKACT2/TXD4/SDA4/MOSI4/SD1_CD/DISP_	IRQ6	INT of PMOD1	CN28-7	**DSW19-3: OFF, DSW19-4 ON,** DSW18-5: OFF,
		TXD4	TX of mikroBUS™	CN34-4	
		DISP_DATAG3	Display data G3	CN20-30	

	DATAG3/ENCIFOE00/DEE00/HDSL11_MISO1	ENCIFOE00	Output enable of ENCIF	CN44-5	DSW18-6: ON
		DREQ	DREQ of external bus	CN42-28	**DSW19-3: OFF, DSW19-4 ON,** DSW18-5: OFF, DSW18-6: ON, **DSW20-1: ON, DSW20-2: OFF**
		ESC_LINKACT2	**Control of LED7 L/A2**		**DSW19-3: OFF, DSW19-4 ON, DSW18-5: ON, DSW18-6: OFF**
		SD1_CD	CD of SD1	CN22-9	DSW19-1: ON, DSW19-2: OFF, DSW19-3 ON, DSW19-4 OFF
C11	P17_0/IRQ12/GTIOC03_1B/SD1_DATA1/SI05#/HDSL13_MOSI1	**SD1_DATA1**	**Data DAT1 of SD1**	**CN22-8**	
C12	P18_2/SEI/A10/GTADSM03_0/GTIOC07_3B/ETH1_CRS/GMAC1_MDC/SCK1/CANRX0/SD1_PWEN/MCLK10/DISP_DATAB3/HDSL14_MOSI1	**SEI**	**SW2 for SEI switch**		
		A10	**A10 of external bus**	**CN42-23**	
		MCLK10	**Clock of DSMIF**	**CN45-17**	
		DISP_DATAB3	**Display data B3**	**CN20-22**	
C13	P18_6/IRQ3/A14/GTIOC07_4A/GTADSM5_0/CTS1#/CANRXDP1/MCLK12/DISP_DATAB7/ENCIFDO13/ENCIFDO14/TXDE09/TXDE10/HDSL14_MOSI2	**A14**	**A14 of external bus**	**CN42-33**	
		MCLK12	**Clock of DSMIF**	**CN45-13**	
		DISP_DATAB7	**Display data B7**	**CN20-18**	
C14	P21_6/ETHSW_PHYLINK0/ESC_PHYLINK0/CANRXDP1/HDSL00_MOSI2	**ETHSW_PHYLINK0/ESC_PHYLINK0**	**PHYLINK of Ethernet Port0**		
C15	P21_7/ETH0_REFCLK/RMII0_REFCLK/CANTXDP1/HDSL01_LINK	**ETH0_REFCLK**	**REFCLK of Ethernet Port0**		
C16	P21_1/ETH0_RXD2/CANRXDP0/TST_OUT12/HDSL00_MISO1	**ETH0_RXD2**	**RXD2 of Ethernet Port0**		
C17	P22_1/GTETRGA/ETH0_TXER/TXD5/SDA5/MOSI5/CANTX0/HDSL01_CLK1	**ETH0_TXER**	**TXER of Ethernet Port0**		
C18	P22_6/IRQ8/A19/GTETRGSB/GMAC0_PTPTRG1/ESC_LATCH1/DE5/CANTX1/SD0_WP/DUEI15/HDSL01_SEL2	IRQ8	INT of PMOD2	CN31-7	DSW15-1: ON, DSW15-2: OFF
		GMAC0_PTPTRG1	PTPTRG1 of GMAC0	CN47-2	
		SD0_WP	**WP of SD0**	**CN21-11**	**DSW15-1: OFF, DSW15-2: ON**
C19	P25_6/ETH1_RXD2/CANRX1/DUEI04/HDSL03_CLK2	**ETH1_RXD2**	**RXD2 of Ethernet Port1**		
C20	P26_2/GMAC1_MDIO/ETHSW_MDIO/ESC_MDIO/CANTXDP1/HDSL04_LINK	**GMAC1_MDIO/ETHSW_MDIO/ESC_MDIO**	**MDIO of Ethernet Port3**		
C21	P25_3/ETH1_RXCLK/DUEI03/HDSL03_SEL1	**ETH1_RXCLK**	**RXCLK of Ethernet Port1**		
C22	P26_6/SEI/CS2#/ETH1_TXER/ESC_RESETOUT#/CANRX0/ENCIFOE01/DEE01/HDSL04_SEL1	CS2#	CS2# of external bus	CN42-34	DSW21-1: OFF, DSW21-2: ON, DSW21-3: OFF
		ETH1_TXER	**TXER of Ethernet Port1**		**DSW21-1: ON, DSW21-2: OFF,**

					DSW21-3: ON
C23	P27_5/MTIOC1A/GTIOC08_4A/GTIOC02_2A/TXD0/SDA0/MOSI0/SPI_SSL00/HSPI_IO3/ENCIFDO14/TXDE10/HDSL05_LINK	**TXD0**	**TXD0 of USB-to-serial conversion**		**DSW9-3: ON, DSW9-4: OFF**
		HSPI_IO3	IO3 of SHOSTIF	CN41-9	DSW9-3: OFF, DSW9-4: ON
		ENCIFDO14	Data output of ENCIF	CN53-15	
C24	P27_6/MTIOC1B/GTIOC08_4B/GTIOC02_2B/HSPI_CK/ENCIFDI14/RXDE10/HDSL05_SMPL	**P27_6**	**User DIPSW2**		**DSW2-3: ON**
		HSPI_CKP	Clock of SHOSTIF	CN41-3	DSW2-3: OFF
		ENCIFDI14	Data input of ENCIF	CN53-17	

Table 5-4 List of RZ/N2H Pin Function Selections (4)

Pin No.	Pin Name	Function	Description	Connector	Remarks
D1	DDR_DQA12	**DDR_DQA12**	**Data DQ_A[3] of LPDDR4**		
D2	DDR_DQA9	**DDR_DQA9**	**Data DQ_A[1] of LPDDR4**		
D3	VSS				
D4	DDR_DQA13	**DDR_DQA13**	**Data DQ_A[0] of LPDDR4**		
D5	VSS				
D6	P12_6/D22/GTIOC05_4A/GTIOC01_3B/CMTW1_TIC1/SS2#/CTS2#/RTS2#/SD0_DATA4/MCLK10/ENCIFDO05/TXDE05/HDSL10_SMPL	D22	Data D22 of external bus	CN43-12	DSW5-1: OFF, DSW5-2: OFF
		RTS2#	RTS of PMOD2	CN31-4	
		SD0_DATA4	**Data DAT4 of eMMC**		**DSW5-1: ON, DSW5-2: ON**
D7	P12_5/D21/GTIOC05_3B/GTIOC01_3A/CMTW1_TOC0/TXD2/SDA2/MOSI2/SD0_DATA3/MDAT02/ENCIFOE05/DEE05/HDSL10_LINK	D21	D21 of external bus	CN43-10	DSW5-1: OFF, DSW5-2: OFF
		TXD2	TXD2 of PMOD2	CN31-2	
		MDAT02	Data of DSMIF	CN45-4	
		SD0_DATA3	**Data DAT3 of eMMC**		**DSW5-1: ON, DSW5-2: ON**
			Data DAT3 of SD0	CN21-1	DSW5-1: OFF, DSW2-2: ON
D8	VSS				
D9	P14_5/TEND/POE8#/GTIOC06_2A/GTIOC09_2A/GTIOC06_3B/CMTW0_TOC0/ESC_RESETOUT#/CTS4#/DISP_DATAG5/ENCIFDI00/RXDE00/HDSL11_CLK2	**TEND**	**TEND of external bus**	**CN42-40**	**DSW20-5: ON, DSW20-6: OFF**
		DISP_DATAG5	**Display data G5**	**CN20-28**	
		ENCIFDI00	**Data input of ENCIF**	**CN44-9**	
D10	P16_7/GTIOC03_1A/SD1_DATA0/TST_OUT05/HDSL13_MISO1	**SD1_DATA0**	**Data DAT0 of SD1**	**CN22-7**	
D11	P17_3/IRQ15/GTETRGA/SI06#/HDSL13_MISO2	**IRQ15**	**MDINT of Ethernet Port3**		
D12	P17_6/WE2#/GTADSM1_0/GTETRGD/CMTW1_TIC1/ETHSW_PTPOUT0/ESC_SYNC0/RXD0/SCL0/MISO0/SD1_PWEN/DISP_DATAG7/SI07#/HDSL14_SMPL	**WE2#**	**WE2# of external bus**	**CN43-20**	
		ETHSW_PTPOUT0	**PTPOUT of ETHSW**	**CN48-1**	
		DISP_DATAG7	**Display data G7**	**CN20-26**	
D13	VSS				
D14	P21_5/GMAC0_MDIO/ETHSW_MDIO/ESC_MDIO/CANTX1/SI13#/HDSL00_MISO2	**GMAC0_MDIO/ETHSW_MDIO/ESC_MDIO**	**MDIO of Ethernet Port0, Port1**		
			MDIO of Ethernet Port2		**DSW5-6: ON**
D15	P20_7/ETH0_RXD0/SI11#/HDSL00_CLK1	**ETH0_RXD0**	**RXD0 of Ethernet Port0**		
D16	P20_6/ETH0_RXCLK/TST_OUT11/HDSL00_SMPL	**ETH0_RXCLK**	**RXCLK of Ethernet Port0**		
D17	VSS				
D18	P22_7/IRQ9/A18/GTIOC06_0A/ETH1_CRS/ETHSW_TDMAOUT2/ESC_LINKACT0/CANRXDP1/TST_OUT15/HDSL01_MISO2	ETHSW_TDMAOUT2	TDMAOUT2 of ETHSW	CN48-8	DSW18-1: OFF, DSW18-2: ON
		ESC_LINKACT0	**Control of LED5 L/A0**		**DSW18-1: ON, DSW18-2: OFF**
D19	P26_3/ETHSW_PHYLINK1/ESC_PHYLINK1/HDSL04_SMPL	**ETHSW_PHYLINK1/ESC_PHYLINK1**	**PHYLINK of Ethernet Port1**		
D20	P25_5/ETH1_RXD1/SI03#/HDSL03_MOSI1	**ETH1_RXD1**	**RXD1 of Ethernet Port1**		

D21	VSS				
D22	P27_0/IRQ1/CS5#//ETH1_CRS/CANTXDP0/SPI_SSL02/HSPI_INT#/ENCIFDI01/RXDE01/HDSL04_MOSI1	**ETH1_CRS**	**CRS of Ethernet Port1**		**DSW13-3: ON, DSW13-4: OFF**
		CS5#	CS5# of external bus	CN42-20	DSW13-3: OFF, DSW13-4: ON, DSW21-6: ON, DSW21-7: OFF
		HSPI_INT#	INT# of SHOSTIF	CN41-2	DSW13-3: OFF, DSW13-4: ON
		ENCIFDI01	Data input of ENCIF	CN44-8	
D23	P27_4/MTIOC2B/GTIOC08_3B/GTIOC02_1B/RXD0/SCL0/MISO0/CANTXDP1/SPI_MISO0/HSPI_IO2/ENCIFOE14/DEE10/HDSL04_MOSI2	ENCIFOE14	Output enable of ENCIF	CN53-13	DSW9-1: OFF, DSW9-2: ON
		HSPI_IO2	IO2 of SHOSTIF	CN41-10	
		RXD0	**RXD0 of USB-to-serial conversion**		**DSW9-1: ON, DSW9-2: OFF**
D24	P30_4/GTIOC09_5B/ETH2_RXDV/ENCIFDI11/RXDE11/HDSL07_SEL1	**ETH2_RXDV**	**RXDV of Ethernet Port2**		**DSW5-7: ON**
		ENCIFDI11	Data input of ENCIF	CN51-26	DSW5-7: OFF

Table 5-5 List of RZ/N2H Pin Function Selections (5)

Pin No.	Pin Name	Function	Description	Connector	Remarks
E1	VSS				
E2	DDR_DQA8	**DDR_DQA8**	**Data DQ_A[7] of LPDDR4**		
E3	DDR_DQA11	**DDR_DQA11**	**Data DQ_A[2] of LPDDR4**		
E4	DDR_DQA14	**DDR_DQA14**	**Data DQ_A[4] of LPDDR4**		
E5	DDR_DQSA_C1	**DDR_DQSA_C1**	**DQS0_A_C of LPDDR4**		
E6	P13_6/D30/GTIOC06_3B/GTIOC04_3A/SS3#/CTS3#/RTS3#/SPI_SSL23/MCLK41/ENCIFDO13/TXDE09/HDSL10_MOSI2	**P13_6**	**GPIO of PMOD2**	**CN31-9**	
		D30	**D30 of external bus**	**CN43-30**	
		MCLK41	**Clock of DSMIF**	**CN46-15**	
E7	P12_1/D17/MTIC5W/GTIOC05_1B/CMTW0_TOC0/CANTX1/SD0_CMD/TST_OUT01/HDSL09_CLK2	D17	Data D17 of external bus	CN43-39	DSW5-1: OFF, DSW5-2: OFF
		GTIOC05_1B	Input capture / output compare / PWM output pin	CN52-30	
		CANTX1	TX of CAN interface		DSW5-1: ON, DSW5-2: OFF
		SD0_CMD	**CMD of eMMC**		**DSW5-1: ON, DSW5-2: ON**
			CMD of SD0	CN21-2	DSW5-1: OFF, DSW2-2: ON
E8	P12_2/D18/GTIOC05_2A/CMTW0_TIC1/CANRXDP1/SD0_DATA0/SI01#/HDSL09_SEL2	P12_2	GPIO.SSLA2 of PMOD1	CN28-9	DSW5-1: OFF, DSW5-2: OFF
		D18	D18 of external bus	CN43-4	
		GTIOC05_2A	Input capture / output compare / PWM output pin	CN52-31	
		SD0_DATA0	**Data DAT0 of eMMC**		**DSW5-1: ON, DSW5-2: ON**
			Data DAT0 of SD0	CN21-7	DSW5-1: OFF, DSW2-2: ON
E9	P14_2/BS#/GTIOC06_0B/GTIOC09_0B/GTIOC05_3B/RXD4/SCL4/MISO4/SD0_WP/DISP_DATAG2/ENCIFCK00/SCKE00/HDSL11_SEL1	**BS#**	**BS# of external bus**	**CN42-30**	
		RXD4	**RXD4 of RS485**	**CN34-3**	
		DISP_DATAG2	**Display data G2**	**CN20-31**	
		ENCIFCK00	**Clock of ENCIF**	**CN44-3**	
E10	P16_5/GTIOC03_0A/SD1_CLK/SI04#/HDSL13_CLK1	**SD1_CLK**	**CLK of SD1**	**CN22-5**	
E11	P16_6/GTIOC03_0B/SD1_CMD/DUEI05/HDSL13_SEL1	**SD1_CMD**	**CMD of SD1**	**CN22-3**	
E12	P17_7/WE3#/AH#/GTADSM1_1/CMTW1_TOC1/ETHSW_PTPOUT1/ESC_SYNC1/TXD0/SDA0/MOSI0/SD1_IOVS/DISP_DATAB0/DUEI08/HDSL14_CLK1	**WE3#**	**WE3# of external bus**	**CN43-40**	
		ETHSW_PTPOUT1	**Timer pulse output of ETHSW**	**CN48-3**	
		DISP_DATAB0	**Display data B0**	**CN20-25**	
E13	P17_4/A6/DREQ/GTADSM0_0/GTETRGB/CMTW1_TIC0/DE0/CANRX0/SD1_CD/DUEI07/HDSL13_MOSI2	A6	A6 of external bus	CN42-15	DSW5-3: OFF
		SD1_CD	**CD of SD1**	**CN22-9**	**DSW5-3: ON, DSW19-1: OFF, DSW19-2: ON**
E14	P20_3/ETH0_TXD2/CANRX0	**ETH0_TXD2**	**TXD2 of Ethernet Port0**		
E15	P21_0/ETH0_RXD1/DUEI12/HDSL00_SEL1	**ETH0_RXD1**	**RXD1 of Ethernet Port0**		
E16			**MDC of Ethernet Port0, Port1**		

	P21_4/GMAC0_MDC/ETHSW_MDC/ESC_MDC/CANRX1/TST_OUT13/HDSL00_SEL2	**GMAC0_MDC/ETHSW_MDC/ESC_MDC**	**MDC of Ethernet Port2**		**DSW5-6: ON**
E17	P22_3/IRQ5/A22/GTETRGC/ETH0_CRS/SCK5/CANRXDP0/DUEI14/HDSL01_MISO1	**ETH0_CRS**	**CRS of Ethernet Port0**		
E18	P26_1/GMAC1_MDC/ETHSW_MDC/ESC_MDC/CANRXDP1/HDSL03_MOSI2	**GMAC1_MDC/ETHSW_MDC/ESC_MDC**	**MDC of Ethernet Port3**		
E19	P25_4/ETH1_RXD0/TST_OUT03/HDSL03_MISO1	**ETH1_RXD0**	**RXD0 of Ethernet Port1**		
E20	P25_7/ETH1_RXD3/CANTX1/TST_OUT04/HDSL03_SEL2	**ETH1_RXD3**	**RXD3 of Ethernet Port1**		
E21	P26_4/ETH1_REFCLK/RMII1_REFCLK	**ETH1_REFCLK**	**REFCLK of Ethernet Port1**		
E22	P26_7/IRQ0/CS3#//ETH1_RXER/ESC_LEDSTER/CANRXDP0/SPI_SSL01/ENCIFDO01/TXDE01/HDSL04_MISO1	**ETH1_RXER**	**RXER of Ethernet Port1**		**DSW13-1: ON, DSW13-2: OFF**
		CS3#	CS3# of external bus	CN42-36	DSW13-1: OFF, DSW13-2: ON, DSW21-4: ON, DSW21-5: OFF
		ENCIFDO01	Data output of ENCIF	CN44-6	DSW13-1: OFF, DSW13-2: ON
E23	P29_1/GTIOC09_0A/ETH2_TXCLK/ENCIFCK09/SCKE09/HDSL06_CLK1	**ETH2_TXCLK**	**TXCLK of Ethernet Port2**		**DSW5-7: ON**
		ENCIFCK09	Clock of ENCIF	CN51-12	DSW5-7: OFF
E24	P30_2/IRQ10/GTIOC09_4B/ETH2_RXD2/SPI_MOSI2/ENCIFOE11/DEE11/HDSL07_SMPL	**ETH2_RXD2**	**RXD2 of Ethernet Port2**		**DSW5-7: ON**
		ENCIFOE11	Output enable of ENCIF	CN51-22	DSW5-7: OFF

Table 5-6 List of RZ/N2H Pin Function Selections (6)

Pin No.	Pin Name	Function	Description	Connector	Remarks
F1	DDR_DQA15	**DDR_DQA15**	**Data DQ_A[5] of LPDDR4**		
F2	VSS				
F3	DDR_DQA10	**DDR_DQA10**	**Data DQ_A[6] of LPDDR4**		
F4	DDR_DMIA1	**DDR_DMIA1**	**DMI_A[0] of LPDDR4**		
F5	DDR_DQSA_T1	**DDR_DQSA_T1**	**DQS0_A_T of LPDDR4**		
F6	DDR_VDDQ				
F7	P12_3/D19/GTIOC05_2B/CMTW0_TOC1/SCK2/CANTXDP1/SD0_DATA1/HDSL09_MISO2	P12_3	GPIO/SSLA3 of PMOD1	CN28-10	DSW5-1: OFF, DSW5-2: OFF
		D19	Data D19 of external bus	CN43-6	
		GTIOC05_2B	Input capture / output compare / PWM output pin	CN52-32	
		SD0_DATA1	**Data DAT1 of eMMC**		**DSW5-1: ON, DSW5-2: ON**
			Data DAT1 of SD0	CN21-8	DSW5-1: OFF, DSW2-2: ON
F8	P13_2/IRQ3/D26//SPI_MISO3/SD0_RST#/MCLK01/ENCIFDO12/ENCIFDO03/TXDE08/TXDE03/HDSL10_MOSI1	D26	Dats D26 of external bus	CN43-22	DSW5-1: OFF, DSW5-2: OFF
		MCLK01	Clock of DSMIF	CN45-5	
		SPI_MISO3	MISO of PMOD1	CN28-3	DSW5-1: OFF, DSW5-2: OFF, **JP26: Short JP28: Open**
		SD0_RST#	**Reset of eMMC**		**DSW5-1: ON, DSW5-2: ON**
F9	P13_3/D27/GTIOC03_3A/SCK3/SPI_SSL30/MDAT01/ENCIFDI12/ENCIFDI03/RXDE08/RXDE03/HDSL10_CLK2	**D27**	**D27 of external bus**	**CN43-24**	
		SPI_SSL30	**SS of PMOD1**	**CN28-1**	
		MDAT01	**Data of DSMIF**	**CN45-6**	
F10	VSS				
F11	P17_5/A7/DACK/GTADSM00_1/GTETRGC/CMTW1_TOC0/SCK0/CANTX0/SD1_WP/TST_OUT07/HDSL14_LINK	**A7**	**A7 of external bus**	**CN42-17**	
F12	P18_0/IRQ7/A8/TEND/GTADSM2_0/ESC_LEDRUN/SS0#/CTS0#/RTS0#/CANRXDP0/SD1_PWEN/DISP_DATAB1/TST_OUT08/HDSL14_SEL1	**IRQ7**	**Interrupt of SPI expansion connector**	**CN19-2**	
		A8	**A8 of external bus**	**CN42-19**	
		DISP_DATAB1	**Display data B1**	**CN20-24**	
F13	P18_7/IRQ4/A15/GTIOC07_4B/GTADSM5_1/ETHSW_PTPOUT3/ESC_SYNC1/DE1/CANTXDP1/MDAT12/ENCIFDI13/ENCIFDI14/RXDE09/RXDE10/HDSL15_LINK	**IRQ4**	**Interrupt of user SW4**		
		A15	**A15 of external bus**	**CN42-35**	
		ETHSW_PTPOUT3	**Timer pulse output of ETHSW**	**CN48-7**	
		MDAT12	**Data of DSMIF**	**CN45-14**	
F14	P20_2/ETH0_TXD1	**ETH0_TXD1**	**TXD1 of Ethernet Port0**		
F15	VSS				
F16	P22_0/IRQ11/HDSL01_SMPL	**IRQ11**	**MDINT of Ethernet Port0**		
F17	P23_0/IRQ10/A17/GTIOC06_0B/ETH1_COL/ETHSW_TDMAOUT3/ESC_LINKACT1/CANTXDP1/SI15#/HDSL01_MOSI2	IRQ10	INT of mikroBUS™	CN34-2	DSW18-3: OFF, DSW18-4: ON
		ETHSW_TDMAOUT3	TDMAOUT of ETHSW	CN48-10	
		ESC_LINKACT1	**Control of LED6 L/A1**		**DSW18-3: ON, DSW18-4: OFF**

F18	P26_0/ETH1_RXDV/SI04#/HDSL03_MISO2	**ETH1_RXDV**	**RXDV of Ethernet Port1**		
F19	VSS				
F20	P30_0/GTIOC09_3B/ETH2_RXD0/ENCIFDI10/RXDE10/HDSL06_MOSI2	**ETH2_RXD0**	**RXD0 of Ethernet Port2**		**DSW5-7: ON**
		ENCIFDI10	Data input of ENCIF	CN51-27	DSW5-7: OFF
F21	P29_6/GTIOC09_2B/ETH2_TXEN/SPI_SSL22/ENCIFOE10/DEE10/HDSL06_SEL2	**ETH2_TXEN**	**TXEN of Ethernet Port2**		**DSW5-7: ON**
		ENCIFOE10	Output enable of ENCIF	CN51-23	DSW5-7: OFF
F22	P29_4/IRQ8/GTIOC09_1B/ETH2_TXD2/SPI_SSL20/ENCIFDI09/RXDE09/HDSL06_MOSI1	**ETH2_TXD2**	**TXD2 of Ethernet Port2**		**DSW5-7: ON**
		ENCIFDI09	Data input of ENCIF	CN51-18	DSW5-7: OFF
F23	VSS				
F24	P30_7/IRQ14/ETHSW_PHYLINK2/ESC_PHYLINK2/SPI_MISO3/SD1_IOVS/MCLK30/SI07#/HDSL07_CLK2	**ETHSW_PHYLINK2/ESC_PHYLINK2**	**LINK of Ethernet Port2**		**DSW5-7: ON**
		MCLK30	Clock of DSMIF	CN46-7	DSW5-7: OFF

Table 5-7 List of RZ/N2H Pin Function Selections (7)

Pin No.	Pin Name	Function	Description	Connector	Remarks
G1	DDR_DQA6	**DDR_DQA6**	**Data DQ_A[9] of LPDDR4**		
G2	DDR_DQA5	**DDR_DQA5**	**Data DQ_A[15] of LPDDR4**		
G3	VSS				
G4	VSS				
G5	VSS				
G6	DDR_VDDQ				
G7	VDD33				
G8	VSS				
G9	VDDP_18_33				
G10	VDD33				
G11	VDD1833_6				
G12	VDD1833_7				
G13	VDD1833_0				
G14	VDD1833_0				
G15	VDDP_18_1				
G16	VSS_PLL0				
G17	VSS				
G18	VSS				
G19	P31_0/ETH2_REFCLK/RMII2_REFCLK/GTETRGSA/SPI_SSL30/HDSL07_SEL2	**ETH2_REFCLK**	**REFCLK of Ethernet Port2**		
G20	P30_5/GTIOC09_6A/GMAC2_MDC/ETHSW_MDC/ESC_MDC/SPI_RSPCK3/DUEI07/HDSL07_MISO1	GMAC2_MDC/ETHSW_MDC/ESC_MDC	MDC of Ethernet Port2		DSW5-6: OFF
G21	P29_5/IRQ9/GTIOC09_2A/ETH2_TXD3/SPI_SSL21/ENCIFCK10/SCKE10/HDSL06_CLK2	**ETH2_TXD3**	**TXD3 of Ethernet Port2**		**DSW5-7: ON**
		ENCIFCK10	Clock of ENCIF	CN51-21	DSW5-7: OFF
G22	P29_3/GTIOC09_1A/ETH2_TXD1/ENCIFDO09/TXDE09/HDSL06_MISO1	**ETH2_TXD1**	**TXD1 of Ethernet Port2**		**DSW5-7: ON**
		ENCIFDO09	Data output of ENCIF	CN51-16	DSW5-7: OFF
G23	P30_1/GTIOC09_4A/ETH2_RXD1/ENCIFCK11/SCKE11/HDSL07_LINK	**ETH2_RXD1**	**RXD1 of Ethernet Port2**		**DSW5-7: ON**
		ENCIFCK11	Clock of ENCIF	CN51-20	DSW5-7: OFF
G24	P31_1/IRQ13/GTETRGSB/ETH2_RXER/SPI_SSL31/HDSL07_MISO2	**ETH2_RXER**	**RXER of Ethernet Port2**		

Table 5-8 List of RZ/N2H Pin Function Selections (8)

Pin No.	Pin Name	Function	Description	Connector	Remarks
H1	DDR_DQA4	**DDR_DQA4**	**Data DQ_A[14] of LPDDR4**		
H2	VSS				
H3	DDR_DMIA0	**DDR_DMIA0**	**DMI_A[1] of LPDDR4**		
H4	DDR_DQA7	**DDR_DQA7**	**Data DQ_A[8] of LPDDR4**		
H5	DDR_DQSA_C0	**DDR_DQSA_C0**	**DQS1_A_C of LPDDR4**		
H6	DDR_VDDQ				
H7	VDD33				
H8	VSS_PLL2				
H9	DVDD08A_TSU				
H10	VDDP_18_33				
H11	VDDP_18_7				
H12	VDD18_PLL3				
H13	VSS_PLL3				
H14	VDDP_18_0				
H15	VDDP_18_33				
H16	VDD18_PLL0				
H17	VSS				
H18	VSS				
H19	VDD1833_1				
H20	P29_2/GTIOC09_0B/ETH2_TXD0/ENCIFOE09/DEE09/HDSL06_SEL1	**ETH2_TXD0**	**TXD0 of Ethernet Port2**		**DSW5-7: ON**
		ENCIFOE09	Data input of ENCIF	CN51-14	DSW5-7: OFF
H21	VSS				
H22	P29_7/GTIOC09_3A/ETH2_RXCLK/SPI_SSL23/ENCIFDO10/TXDE10/HDSL06_MISO2	**ETH2_RXCLK**	**RXCLK of Ethernet Port2**		**DSW5-7: ON**
		ENCIFDO10	Data output of ENCIF	CN51-25	DSW5-7: OFF
H23	P30_3/IRQ11/GTIOC09_5A/ETH2_RXD3/SPI_MISO2/ENCIFDO11/TXDE11/HDSL07_CLK1	**ETH2_RXD3**	**RXD3 of Ethernet Port2**		**DSW5-7: ON**
		ENCIFDO11	Data output of ENCIF	CN51-24	DSW5-7: OFF
H24	P30_6/GTIOC09_6B/GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/SPI_MOSI3/TST_OUT07/HDSL07_MOSI1	GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO	MDIO of Ethernet Port2		DSW5-6: OFF

Table 5-9 List of RZ/N2H Pin Function Selections (9)

Pin No.	Pin Name	Function	Description	Connector	Remarks
J1	DDR_DQA2	**DDR_DQA2**	**Data DQ_A[10] of LPDDR4**		
J2	DDR_DQA0	**DDR_DQA0**	**Data DQ_A[11] of LPDDR4**		
J3	DDR_DQA1	**DDR_DQA1**	**Data DQ_A[12] of LPDDR4**		
J4	DDR_DQA3	**DDR_DQA3**	**Data DQ_A[13] of LPDDR4**		
J5	DDR_DQSA_T0	**DDR_DQSA_T0**	**DQS1_A_T of LPDDR4**		
J6	VSS				
J7	VDD33				
J8	VDD18_PLL2				
J9	AVDD18A_TSU				
J10	VDDP_18_6				
J11	VDD08				
J12	VDD08_PLL3				
J13	VSS				
J14	VDD08				
J15	VSS				
J16	VDD08_PLL0				
J17	VDD33				
J18	VSS				
J19	VDD1833_1				
J20	P31_6/A16/TEND/POE11#/GMAC2_PTPTRG0/ETHSW_TDMAOUT0/ESC_LEDRUN/SPI_MISO0/MDAT32/ENCIFCK15/ENCIFCK01/SCKE11/SCKE01/HDSL08_SEL1	TEND	TEND of external bus	CN42-40	DSW18-7: OFF, DSW18-8: ON, DSW20-5: OFF, DSW20-6: ON
		GMAC2_PTPTRG0	PTPTRG0 of GMAC2	CN47-5	DSW18-7: OFF, DSW18-8: ON
		ETHSW_TDMAOUT0	TDMAOUT of ETHSW	CN48-4	
		MDAT32	Data of DSMIF	CN46-4	
		ESC_LEDRUN	**Control of LED3 ESC_LEDRUN**		**DSW18-7: ON, DSW18-8: OFF**
J21	P31_4/DREQ/POE8#/ETH2_CRS/ETHSW_PTPOUT2/ESC_SYNC0/SPI_RSPCK0/SPI_SSL30/MCLK81/MDAT31/HSPI_IO6/ENCIFDO09/TXDE09/HDSL08_SMPL/POUTB	**ETH2_CRS**	**CRS of Ethernet Port2**		**DSW5-7: ON**
		DREQ	DREQ of external bus	CN42-28	DSW5-7: OFF, DSW20-1: OFF, DSW20-2: ON
		MDAT31	Data of DSMIF	CN46-6	DSW5-7: OFF
		HSPI_IO6	IO6 of SHOSTIF	CN41-6	
J22	P31_3/POE4#/ETH2_RXER/ETHSW_TDMAOUT1/ESC_LEDERR/SPI_SSL33/MDAT80/MCLK31/HSPI_IO5/ENCIFOE09/DEE09/HDSL08_LINK	**P31_3**	**User DIPSW3**		**DSW2-3: ON**
		ETHSW_TDMAOUT1	TDMAOUT of ETHSW	CN48-6	DSW2-3: OFF
		MCLK31	Clock of DSMIF	CN46-5	
		HSPI_IO5	IO5 of SHOSTIF	CN41-7	
J23	P31_5/DACK/POE10#/ETH2_COL/ETHSW_PTPOUT3/ESC_SYNC1/SPI_MOSI0/SPI_SSL31/MDAT81/MCLK32/HSPI_IO7/ENCIFDI09/RXDE09/HDSL08_CLK1/POUTZ	**ETH2_COL**	**COL of Ethernet Port2**		**DSW5-7: ON**
		DACK	DACK of external bus	CN42-26	DSW5-7: OFF, DSW20-3: OFF, DSW20-4: ON
		MCLK32	Clock of DSMIF	CN46-3	DSW5-7: OFF
		HSPI_IO7	IO7 of SHOSTIF	CN41-5	
J24	P31_2/POE0#/ETH2_TXER/SPI_SSL32/MCLK80/MDAT30/HSPI_IO4/EN	**ETH2_TXER**	**TXER of Ethernet Port2**		**DSW5-7: ON**
		MDAT30	Data of DSMIF	CN46-8	DSW5-7: OFF

	CIFCK09/SCKE09/HDSL07_MOSI2/ POUTA	HSPI_IO4	IO4 of SHOSTIF	CN41-8	

Table 5-10 List of RZ/N2H Pin Function Selections (10)

Pin No.	Pin Name	Function	Description	Connector	Remarks
K1	VSS				
K2	DDR_CAA1	**DDR_CAA1**	**CA_A[0] of LPDDR4**		
K3	VSS				
K4	VSS				
K5	VSS				
K6	DDR_CKEA1	**DDR_CKEA1**	**CKE_A[1] of LPDDR4**		
K7	VSS				
K8	VDD08_PLL2				
K9	VDD08				
K10	VDD08				
K11	VSS				
K12	VDD08				
K13	VSS				
K14	VDD08				
K15	VSS				
K16	VDD08				
K17	VDDP_18_2				
K18	VDD1833_2				
K19	VDD1833_2				
K20	P34_1/A23/GTADSM3_1/GTIOC03_0B/ETH3_RXD0/SPI_MISO2/ENCIFDI06/RXDE06/HDSL10_CLK1	**ETH3_RXD0**	**RXD0 of Ethernet Port3**		**DSW5-8: ON**
		A23	A23 of external bus	CN42-18	DSW5-8: OFF
		GTIOC03_0B	Input capture / output compare / PWM output pin	CN52-4	
		SPI_MISO2	Data input of ENCIF	CN33-5	
K21	P34_5/CS3#/GTADSM5_1/GTIOC03_2B/ETH3_RXDV/ESC_I2CCLK/TXD3/SDA3/MOSI3/IIC_SCL1/SPI_SSL23/ADTRG1#/ENCIFDI07/RXDE07/HDSL10_CLK2	**ETH3_RXDV**	**RXDV of Ethernet Port3**		**DSW5-8: ON**
		CS3#	CS3# of external bus	CN42-36	DSW5-8: OFF, **DSW21-4: OFF, DSW21-5: ON**
		GTIOC03_2B	Data input of ENCIF	CN52-8	DSW5-8: OFF
K22	P34_2/A24/GTADSM4_0/GTIOC03_1A/ETH3_RXD1/SPI_SSL20/ENCIFCK07/SCKE07/HDSL10_SEL1	**ETH3_RXD1**	**RXD1 of Ethernet Port3**		**DSW5-8: ON**
		A24	A24 of external bus	CN42-22	DSW5-8: OFF
		GTIOC03_1A	Input capture / output compare / PWM output pin	CN52-5	
		SPI_SSL20	CS of mikroBUS™	CN33-3	
K23	P34_4/CS2#/GTADSM5_0/GTIOC03_2A/ETH3_RXD3/RXD3/SCL3/MISO3/SPI_SSL22/SD1_IOVS/ADTRG0#/ENCIFDO07/TXDE07/HDSL10_MOSI1	**ETH3_RXD3**	**RXD3 of Ethernet Port3**		**DSW5-8: ON**
		CS2#	CS2# of external bus	CN42-34	DSW5-8: OFF, **DSW21-1: ON, DSW21-2: OFF, DSW21-3: ON**
		GTIOC03_2A	Input capture / output compare / PWM output pin	CN52-7	DSW5-8: OFF
K24	P34_6/ETH3_REFCLK/RMII3_REFCLK/CS5#//ETH1_RXER/ESC_I2CDATA/IIC_SDA1/SPI_RSPCK3/ADTRG2#/DUEI08/HDSL10_SEL2	**ETH3_REFCLK**	**REFCLK of Ethernet Port3**		**DSW5-8: ON**
		CS5#	CS5# of external bus	CN42-20	DSW5-8: OFF, **DSW21-6: OFF, DSW21-7: ON**

Table 5-11 List of RZ/N2H Pin Function Selections (11)

Pin No.	Pin Name	Function	Description	Connector	Remarks
L1	DDR_CKA_C	**DDR_CKA_C**	**CK_A_C of LPDDR4**		
L2	DDR_CAA3	**DDR_CAA3**	**CA_A[1] of LPDDR4**		
L3	DDR_CAA4	**DDR_CAA4**	**CA_A[3] of LPDDR4**		
L4	DDR_CSA0	**DDR_CSA0**	**CS_A[0] of LPDDR4**		
L5	DDR_CSA1	**DDR_CSA1**	**CS_A[1] of LPDDR4**		
L6	DDR_CKEA0	**DDR_CKEA0**	**CKE_A[0] of LPDDR4**		
L7	VSS				
L8	VSS				
L9	VSS				
L10	VDD08				
L11	VSS				
L12	VDD08				
L13	VSS				
L14	VDD08				
L15	VSS				
L16	VDD08				
L17	VDDP_18_33				
L18	VSS				
L19	VSS				
L20	P33_2/A16/GTADSM0_0/ETH3_TXCLK/SCK1/SPI_RSPCK1/SPI_SSL30/MCLK50/ENCIFCK01/SCKE01/HDSL09_MOSI1	**ETH3_TXCLK**	**TXCLK of Ethernet Port3**		**DSW5-8: ON**
		A16	A16 of external bus	CN42-4	DSW5-8: OFF
		MCLK50	Clock of DSMIF	CN46-27	
L21	P34_3/A25/GTADSM4_1/GTIOC03_1B/ETH3_RXD2/SPI_SSL21/SD1_PWEN/ENCIFOE07/DEE07/HDSL10_MISO1	**ETH3_RXD2**	**RXD2 of Ethernet Port3**		**DSW5-8: ON**
		A25	A25 of external bus	CN42-24	DSW5-8: OFF
		GTIOC03_1B	Input capture / output compare / PWM output pin	CN52-6	
L22	P34_0/A22/GTADSM3_0/GTIOC03_0A/ETH3_RXCLK/SPI_MOSI2/ENCIFDO06/TXDE06/HDSL10_SMPL	**ETH3_RXCLK**	**RXCLK of Ethernet Port3**		**DSW5-8: ON**
		A22	A22 of external bus	CN42-16	DSW5-8: OFF
		GTIOC03_0A	Input capture / output compare / PWM output pin	CN52-3	
		SPI_MOSI2	MOSI of mikroBUS™	CN33-6	
L23	P33_7/A21/GTADSM2_1/ETH3_TXEN/SPI_RSPCK2/MDAT52/ENCIFOE06/DEE06/HDSL10_LINK	**ETH3_TXEN**	**TXEN of Ethernet Port3**		**DSW5-8: ON**
		A21	A21 of external bus	CN42-14	DSW5-8: OFF
		SPI_RSPCK2	SCK of mikroBUS™	CN33-4	
		MDAT52	Data of DSMIF	CN46-24	
L24	VSS				

Table 5-12 List of RZ/N2H Pin Function Selections (12)

Pin No.	Pin Name	Function	Description	Connector	Remarks
M1	DDR_CKA_T	**DDR_CKA_T**	**CK_A_T of LPDDR4**		
M2	VSS				
M3	DDR_CAA2	**DDR_CAA2**	**CA_A[2] of LPDDR4**		
M4	VSS				
M5	DDR_CAA5	**DDR_CAA5**	**CA_A[5] of LPDDR4**		
M6	VSS				
M7	DDR_VDDQ				
M8	DDR_VAA				
M9	VSS				
M10	VDD08				
M11	VSS				
M12	VDD08				
M13	VSS				
M14	VDD08				
M15	VSS				
M16	VDD08				
M17	VDD33				
M18	VSS				
M19	VSS				
M20	P33_3/IRQ12/A17/GTADSM00_1/ETH3_TXD0/RXD1/SCL1/MISO1/SPI_MOSI1/SPI_RSPCK0/MDAT50/PCIE_RSTOUT0B/ENCIFOE01/DEE01/HDSL09_CLK2	**ETH3_TXD0**	**TXD0 of Ethernet Port3**		**DSW5-8: ON**
		RXD1	RXD1 of USB-to-serial conversion		DSW5-8: OFF, **DSW9-5: ON, DSW9-6: OFF**
		A17	A17 of external bus	CN42-6	DSW5-8: OFF, DSW9-5: OFF, DSW9-6: ON
		MDAT50	Data of DSMIF	CN46-28	
		PCIE_RSTOUT0B	Reset output of PCIe x4	CN11-A11	DSW5-8: OFF, DSW9-5: OFF, DSW9-6: ON, **DSW4-1: ON**
M21	P33_6/IRQ15/A20/GTADSM2_0/ETH3_TXD3/TXD2/SDA2/MOSI2/SPI_SSL11/SPI_SSL00/MCLK52/ENCIFCK06/SCKE06/HDSL09_MOSI2	**ETH3_TXD3**	**TXD3 of Ethernet Port3**		**DSW5-8: ON**
		A20	A20 of external bus	CN42-12	DSW5-8: OFF
		MCLK52	Clock of DSMIF	CN46-23	
M22	VSS				
M23	VSS				
M24	EXTCLKIN	**EXTCLKIN**	**Connection of crystal oscillator**		**DSW2-1: ON**

Table 5-13 List of RZ/N2H Pin Function Selections (13)

Pin No.	Pin Name	Function	Description	Connector	Remarks
N1	VSS				
N2	DDR_CKEB1	**DDR_CKEB1**	**CKE_B[1] of LPDDR4**		
N3	DDR_CAB0	**DDR_CAB0**	**CA_B[2] of LPDDR4**		
N4	DDR_CAA0	**DDR_CAA0**	**CA_A[4] of LPDDR4**		
N5	DDR_VDDQ				
N6	VSS				
N7	DDR_RESET_N	**DDR_RESET_N**	**RESET_N of LPDDR4**		
N8	DDR_ATEST	**DDR_ATEST**			**NC**
N9	VSS				
N10	VDD08				
N11	VSS				
N12	VDD08				
N13	VSS				
N14	VDD08				
N15	VSS				
N16	VDD08				
N17	VDDP_18_33				
N18	VDD1833_3				
N19	VDD1833_3				
N20	P33_4/IRQ13/A18/GTADSM1_0/ETH3_TXD1/TXD1/SDA1/MOSI1/SPI_MISO1/SPI_MOSI0/MCLK51/PCIE_RSTOUT1B/ENCIFDO01/TXDE01/HDSL09_SEL2	**ETH3_TXD1**	**TXD1 of Ethernet Port3**		**DSW5-8: ON**
		TXD1	TXD1 of USB-to-serial conversion		DSW5-8: OFF, **DSW9-7: ON, DSW9-8: OFF**
		A18	A18 of external bus	CN42-8	DSW5-8: OFF, DSW9-7: OFF, DSW9-8: ON
		MCLK51	Clock of DSMIF	CN46-25	
		PCIE_RSTOUT1B	Reset out of PCIe x1	CN12-A11	DSW5-8: OFF, DSW9-7: OFF, DSW9-8: ON, **DSW4-2: ON**
N21	P33_5/IRQ14/A19/GTADSM1_1/ETH3_TXD2/RXD2/SCL2/MISO2/SPI_SSL10/SPI_MISO0/MDAT51/ENCIFDI01/RXDE01/HDSL09_MISO2	**ETH3_TXD2**	**TXD2 of Ethernet Port3**		**DSW5-8: ON**
		A19	A19 of external bus	CN42-10	DSW5-8: OFF
		MDAT51	Data of DSMIF	CN46-26	
N22	XTALSEL	**XTALSEL**	**EXTCLKIN/XTAL,EXTAL select**		
N23	XTAL	XTAL	Connection of crystal resonator		DSW2-1: OFF
N24	EXTAL	EXTAL	Connection of crystal resonator		DSW2-1: OFF

Table 5-14 List of RZ/N2H Pin Function Selections (14)

Pin No.	Pin Name	Function	Description	Connector	Remarks
P1	DDR_CKB_T	**DDR_CKB_T**	**CK_B_T of LPDDR4**		
P2	DDR_CKEB0	**DDR_CKEB0**	**CKE_B[0] of LPDDR4**		
P3	VSS				
P4	VSS				
P5	DDR_VDDQ				
P6	VSS				
P7	DDR_DTEST	**DDR_DTEST**			**NC**
P8	DDR_ZN	**DDR_ZN**			**120Ω PD**
P9	VDD08				
P10	VDD08				
P11	VSS				
P12	VDD08				
P13	VDD18_PLL4				
P14	VDD08				
P15	VSS				
P16	VSS				
P17	VDD33_X				
P18	VDDP_18_X				
P19	OTPVDD08				
P20	OTPVDD18				
P21	VSS				
P22	VSS				
P23	VSS				
P24	VSS				

Table 5-15 List of RZ/N2H Pin Function Selections (15)

Pin No.	Pin Name	Function	Description	Connector	Remarks
R1	DDR_CKB_C	**DDR_CKB_C**	**CK_B_C of LPDDR4**		
R2	DDR_CAB1	**DDR_CAB1**	**CA_B[0] of LPDDR4**		
R3	DDR_VDDQ				
R4	DDR_CAB2	**DDR_CAB2**	**CA_B[3] of LPDDR4**		
R5	DDR_CAB5	**DDR_CAB5**	**CA_B[1] of LPDDR4**		
R6	DDR_CSB0	**DDR_CSB0**	**CS_B[0] of LPDDR4**		
R7	VSS				
R8	VSS				
R9	VDD08				
R10	VDD08				
R11	VSS				
R12	VSS				
R13	VSS_PLL4				
R14	PCIE_VDD08A_L1				
R15	PCIE_VDD08A_L0				
R16	VSS				
R17	VSS				
R18	VSS				
R19	VSS				
R20	VSS				
R21	AVSSIO_ADC0				
R22	AVDDREF_ADC0				
R23	AN002	**AN002**	**ADC input (AN002)**	**CN3-6**	
R24	AN000	**AN000**	ADC input (AN000)	CN3-2	DSW6-1: ON, DSW6-2: OFF
			Input of potentiometer		**DSW6-1: OFF, DSW6-2: ON**

Table 5-16 List of RZ/N2H Pin Function Selections (16)

Pin No.	Pin Name	Function	Description	Connector	Remarks
T1	DDR_CAB3	**DDR_CAB3**	**CA_B[4] of LPDDR4**		
T2	VSS				
T3	DDR_CAB4	**DDR_CAB4**	**CA_B[5] of LPDDR4**		
T4	DDR_DQB0	**DDR_DQB0**	**Data DQ_B[12] of LPDDR4**		
T5	VSS				
T6	DDR_CSB1	**DDR_CSB1**	**CS_B[1] of LPDDR4**		
T7	VSS				
T8	VSS				
T9	VSS				
T10	VSS_PLL1				
T11	VDD18_PLL1				
T12	VDD08_PLL1				
T13	VDD08_PLL4				
T14	PCIE_VDD08A_L1				
T15	PCIE_VDD08A_L0				
T16	PCIE_VDD18A_L1				
T17	PCIE_VDD18A_L0				
T18	VSS				
T19	VSS				
T20	AVDD_ADC0				
T21	AVSSIO_ADC0				
T22	AVDDIO_ADC0				
T23	AN003	**AN003**	**ADC input (AN003)**	**CN3-8**	
T24	AN001	**AN001**	**ADC input (AN001)**	**CN3-4**	

Table 5-17 List of RZ/N2H Pin Function Selections (17)

Pin No.	Pin Name	Function	Description	Connector	Remarks
U1	DDR_DQB2	**DDR_DQB2**	**Data DQ_B[11] of LPDDR4**		
U2	DDR_DQB1	**DDR_DQB1**	**Data DQ_B[13] of LPDDR4**		
U3	VSS				
U4	DDR_DQB3	**DDR_DQB3**	**Data DQ_B[14] of LPDDR4**		
U5	DDR_DQSB_T0	**DDR_DQSB_T0**	**DQS1_B_T of LPDDR4**		
U6	VSS				
U7	VSS				
U8	VSS				
U9	VSS				
U10	VDDP_18_33				
U11	VDD1833_4				
U12	VSS				
U13	VDDP_18_5				
U14	VSS				
U15	USB_USVDD18				
U16	PCIE_VDD18A_L1				
U17	PCIE_VDD18A_L0				
U18	VSS				
U19	VSS				
U20	AVSS_ADC0				
U21	AVDDIO_ADC1				
U22	AVDDREF_ADC1				
U23	AN100	**AN100**	ADC input (AN100)	CN4-2	DSW6-3: ON, DSW6-4: OFF
			ADC input of mikroBUS™	**CN33-1**	**DSW6-3: OFF, DSW6-4: ON**
U24	AN103	**AN103**	**ADC input (AN103)**	**CN4-8**	

Table 5-18 List of RZ/N2H Pin Function Selections (18)

Pin No.	Pin Name	Function	Description	Connector	Remarks
V1	VSS				
V2	DDR_DQB4	**DDR_DQB4**	**Data DQ_B[10] of LPDDR4**		
V3	DDR_DQB7	**DDR_DQB7**	**Data DQ_B[9] of LPDDR4**		
V4	DDR_DMIB0	**DDR_DMIB0**	**DMI_B[1] of LPDDR4**		
V5	DDR_DQSB_C0	**DDR_DQSB_C0**	**DQS1_B_C of LPDDR4**		
V6	VSS				
V7	TRST#	**TRST#**	**TRST of debug interface**		
V8	VDD33				
V9	VDD33				
V10	VDDP_18_4				
V11	VDD1833_4				
V12	VDDP_18_33				
V13	VDD1833_5				
V14	VSS				
V15	USB_USVDD18				
V16	USB_USVDD33				
V17	USB_USVDD33				
V18	VSS				
V19	VSS				
V20	AVSS_ADC1				
V21	AVSSIO_ADC1				
V22	AVSSIO_ADC1				
V23	AN102	**AN102**	ADC input (AN102)	CN4-6	DSW6-7: ON, DSW6-8: OFF
			ADC input (AN102) of Grove2	**CN32-2**	**DSW6-7: OFF, DSW6-8: ON**
V24	AN101	**AN101**	ADC input (AN101)	CN4-4	DSW6-5: ON, DSW6-6: OFF
			ADC input (AN101) of Grove2	**CN32-1**	**DSW6-5: OFF, DSW6-6: ON**

Table 5-19 List of RZ/N2H Pin Function Selections (19)

Pin No.	Pin Name	Function	Description	Connector	Remarks
W1	DDR_DQB6	**DDR_DQB6**	**Data DQ_B[15] of LPDDR4**		
W2	DDR_VDDQ				
W3	DDR_DQB5	**DDR_DQB5**	**Data DQ_B[8] of LPDDR4**		
W4	VSS				
W5	VSS				
W6	VSS				
W7	P06_5/IRQ11/GTETRGC/IIC_SDA1/XSPI0_IO7/HDSL05_SEL1	**XSPI0_IO7**	**Data IO7 of XSPI0**		
W8	P06_3/IRQ9/GTETRGA/IIC_SDA0/XSPI0_IO5/TST_OUT09/HDSL05_SMPL	**XSPI0_IO5**	**Data IO5 of XSPI0**		
W9	P03_4/IRQ14/D12/MTCLKB/MTIOC8D/GTIOC02_3B/GTADSM9_1/CMTW1_TOC1/RTCAT1HZ/IIC_SDA1/ENCIFOE02/DEE02/HDSL02_MISO2	D12	**D12 of external bus**	CN43-27	DSW7-3: OFF, DSW7-4: ON
		IIC_SDA1	**SDA of PCIe clock driver and some connectors**	**CN20-1, CN29-2, CN30-3, CN34-6**	**DSW7-3: ON, DSW7-4: OFF**
			SDA of PMOD1	CN28-4	**DSW7-3: ON, DSW7-4: OFF,** JP27: Open, JP29: Short
W10	VSS				
W11	P01_0/IRQ6/MTIOC3A/MTIOC1A/GTIOC00_4A/GTIOC00_2B/IIC_SCL1/XSPI1_CKP/ENCIFDO00/ENCIFDO04/TXDE00/TXDE04/HDSL00_MISO2	GTIOC00_2B	Input capture / output compare / PWM output pin	CN49-8	DSW2-6: OFF
		XSPI1_CKP	**Clock of QSPI and SPI expansion connector**	**CN19-3**	**DSW2-6: ON**
W12	P00_2/IRQ1/D2/MTIOC4A/GTIOC00_1A/ETH3_CRS/ADTRG0#/USB_EXICEN/SI00#/HDSL00_CLK1	**ETH3_CRS**	**CRS of Ethernet Port3**		**DSW5-8: ON**
		D2	D2 of external bus	CN43-5	DSW5-8: OFF, DSW2-5: OFF
		GTIOC00_1A	Input capture / output compare / PWM output pin	CN49-5	
W13	VDD1833_5				
W14	USB_USDVDD				
W15	USB_USDVDD				
W16	VSS				
W17	VSS				
W18	PCIE_VDD18A_CMN				
W19	VSS				
W20	AVDD_ADC1				
W21	AVSSIO_ADC2				
W22	AVSSIO_ADC2				
W23	AN206	**AN206**	**ADC input (AN206)**	**CN5-13**	
W24	AN210	**AN210**	**ADC input (AN210)**	**CN6-5**	

Table 5-20 List of RZ/N2H Pin Function Selections (20)

Pin No.	Pin Name	Function	Description	Connector	Remarks
Y1	DDR_DQB8	**DDR_DQB8**	**Data DQ_B[5] of LPDDR4**		
Y2	VSS				
Y3	DDR_DQB15	**DDR_DQB15**	**Data DQ_B[4] of LPDDR4**		
Y4	VSS				
Y5	DDR_DQSB_T1	**DDR_DQSB_T1**	**DQS0_B_T of LPDDR4**		
Y6	VSS				
Y7	P06_2/IRQ8/IIC_SCL0/XSPI0_IO4/DUEI09/HDSL05_LINK	**XSPI0_IO4**	**Data IO4 of XSPI0**		
Y8	P06_4/IRQ10/GTETRGB/IIC_SCL1/XSPI0_IO6/SI09#/HDSL05_CLK1	**XSPI0_IO6**	**Data IO6 of XSPI0**		
Y9	P03_1/D9/MTIOC4B/MTIOC1B/GTIOC02_2A/GTADSM8_0/CMTW1_TIC0/ENCIFDO02/TXDE02/HDSL02_MOSI1	**P03_1**	**GMAC_RESETOUT2# of Ethernet Port2**		**DSW12-7: OFF, DSW12-8: ON, DSW8-1:ON, DSW8-2: OFF**
		D9	D9 of external bus	CN43-21	DSW12-7: ON, DSW12-8: OFF
		GTIOC02_2A	Input capture / output compare / PWM output pin	CN49-31	
Y10	P02_3/IRQ10/MTIOC6C/MTIOC1B/GTIOC01_4B/ETH3_COL/IIC_SCL0/IIC_SCL2/XSPI1_IO7/MDAT22/USB_OVRCUR/ENCIFDI01/RXDE01/HDSL01_MOSI2	**XSPI1_IO7**	**IO7 of SPI expansion connector**	**CN19-5**	**DSW2-6: ON**
		USB_OVRCUR	OVRCUR input of USB Host		DSW2-6: OFF, DSW14-1: OFF, DSW14-2: ON
Y11	P02_4/IRQ11/POE0#/IIC_SDA0/MDAT20/USB_EXICEN/MBX_HINT#/HDSL02_LINK		Unused		
Y12	P01_2/MTIOC6B/MTIOC8B/GTIOC01_0A/GTIOC04_0A/XSPI1_CS1#/DUEI02/HDSL01_LINK	**XSPI1_CS1#**	**CS1# of SPI expansion connector**	**CN19-4**	**DSW2-6: ON**
		GTIOC01_0A	Input capture / output compare / PWM output pin	CN49-15	DSW2-6: OFF
Y13	VDD33				
Y14	USB_VUBUSIN	**USB_VUBUSIN**	**VBUSIN of USB function**	**CN8-1**	**DSW16-1: OFF, DSW16-2: ON**
Y15	USB_TXRTUNE	**USB_TXRTUNE**	**200Ω P,D,**		
Y16	PCIE_REFCLK_N1	**PCIE_REFCLK_N1**	**REFCLK of PCIe ch1**		
Y17	PCIE_REFCLK_P0	**PCIE_REFCLK_P0**	**REFCLK of PCIe ch0**		
Y18	PCIE_VDD18A_CMN				
Y19	VSS				
Y20	AVDD_ADC2				
Y21	AVDDIO_ADC2				
Y22	AN209	**AN209**	**ADC input (AN209)**	**CN6-3**	
Y23	AN208	**AN208**	**ADC input (AN208)**	**CN6-1**	
Y24	AN202	**AN202**	**ADC input (AN202)**	**CN5-5**	

Table 5-21 List of RZ/N2H Pin Function Selections (21)

Pin No.	Pin Name	Function	Description	Connector	Remarks
AA1	DDR_DQB14	**DDR_DQB14**	**Data DQ_B[6] of LPDDR4**		
AA2	DDR_DQB9	**DDR_DQB9**	**Data DQ_B[1] of LPDDR4**		
AA3	DDR_DMIB1	**DDR_DMIB1**	**DMI_B[0] of LPDDR4**		
AA4	DDR_DQB10	**DDR_DQB10**	**Data DQ_B[0] of LPDDR4**		
AA5	DDR_DQSB_C1	**DDR_DQSB_C1**	**DQS0_B_C of LPDDR4**		
AA6	BSCANP	**BSCANP**	**Boundary scan enable**		
AA7	P05_1/IRQ3/XSPI0_CKP/DUEI06/HDSL04_SMPL	**XSPI0_CKP**	**Clock CKP of XSPI0**		
AA8	VSS				
AA9	P03_3/IRQ13/D11/MTCLKA/MTIOC8C/GTIOC02_3A/GTADSM9_0/CMTW1_TIC1/IIC_SCL1/ENCIFCK02/SCKE02/HDSL02_SEL2	IRQ13	IRQ13 of SPI expansion connector	CN19-13	DSW7-1: OFF, DSW7-2: ON
		D11	D11 of external bus	CN43-25	
		IIC_SCL1	**SCL of I2C**	**CN20-2, CN29-1, CN30-4, CN34-5**	**DSW7-1: ON, DSW7-2: OFF**
				CN28-3	**DSW7-1: ON, DSW7-2: OFF,** JP26: Open, JP28: Short
AA10	P02_1/IRQ8/MTCLKD/MTIOC0D/GTIOC01_3B/ETH3_RXER/IIC_SCL2/XSPI1_IO5/MDAT21/ENCIFOE01/DEE01/HDSL01_SEL2	**XSPI1_IO5**	**IO5 of SPI expansion connector**	**CN19-7**	**DSW2-6: ON**
		ENCIFOE01	Data input of ENCIF	CN44-4	DSW2-6: OFF
AA11	P02_2/IRQ9/MTIOC6A/MTIOC1A/GTIOC01_4A/ETH3_CRS/IIC_SDA2/XSPI1_IO6/MCLK22/USB_VBUSEN/ENCIFDO01/TXDE01/HDSL01_MISO2	**XSPI1_IO6**	**IO6 of SPI expansion connector**	**CN19-6**	**DSW2-6: ON**
AA12	P02_0/IRQ7/MTCLKC/MTIOC0C/GTIOC01_3A/ETH3_TXER/IIC_SDA1/XSPI1_IO4/MCLK21/ENCIFCK01/SCKE01/HDSL01_CLK2	**XSPI1_IO4**	**IO4 of SPI expansion connector**	**CN19-8**	**DSW2-6: ON**
		ENCIFCK01	Clock of ENCIF	CN44-2	DSW2-6: OFF
AA13	P00_1/IRQ0/D1/MTIOC3D/GTIOC00_0B/ETH3_RXER/USB_OVRCUR/TST_OUT00/HDSL00_SMPL	D1	D1 of external bus	CN43-3	DSW5-8: OFF, DSW2-5: OFF
		GTIOC00_0B	Input capture / output compare / PWM output pin	CN49-4	
		USB_OVRCUR	OVRCUR input of USB Host		DSW5-8: OFF, **DSW2-5: ON, DSW14-1: ON, DSW14-2: OFF**
		ETH3_RXER	**RXER of Ethernet Port3**		**DSW5-8: ON**
AA14	USB_OTG_ID	**USB_OTG_ID**	**ID of USB_OTG**	**CN9-4**	
AA15	VSS				
AA16	PCIE_REFCLK_P1	**PCIE_REFCLK_P1**	**REFCLK of PCIe ch1**		
AA17	PCIE_REFCLK_N0	**PCIE_REFCLK_N0**	**REFCLK of PCIe ch0**		
AA18	VSS				
AA19	VSS				
AA20	AVSS_ADC2				
AA21	AVDDREF_ADC2				

AA22	AN213	**AN213**	**ADC input (AN213)**	**CN6-11**	
AA23	AN201	**AN201**	**ADC input (AN201)**	**CN5-3**	
AA24	AN200	**AN200**	**ADC input (AN200)**	**CN5-1**	

Table 5-22 List of RZ/N2H Pin Function Selections (22)

Pin No.	Pin Name	Function	Description	Connector	Remarks
AB1	DDR_DQB12	**DDR_DQB12**	**Data DQ_B[3] of LPDDR4**		
AB2	VSS				
AB3	DDR_DQB13	**DDR_DQB13**	**Data DQ_B[2] of LPDDR4**		
AB4	DDR_DQB11	**DDR_DQB11**	**Data DQ_B[7] of LPDDR4**		
AB5	VSS				
AB6	P05_2/IRQ4/IIC_SCL2/XSPI0_CKN/TST_OUT06/HDSL04_CLK1	**XSPI0_CKN**	**Clock CKN of XSPI0**		
AB7	P06_1/XSPI0_IO3/SI08#/HDSL04_MOSI2	**XSPI0_IO3**	**Data IO3 of XSPI0**		
AB8	P05_4/IRQ6/IIC_SDA2/XSPI0_CS1#/DUEI07/HDSL04_MISO1	**XSPI0_CS1#**	**CS# of HyperRAM**		
AB9	P03_2/IRQ12/D10/MTIOC4D/MTIOC1A/GTIOC02_2B/GTADSM8_1/CMTW1_TOC0/ENCIFDI02/RXDE02/HDSL02_CLK2	**P03_2**	**GMAC_RESETOUT3# of Ethernet Port3**		**DSW12-5: OFF, DSW12-6: ON**
		D10	D10 of external bus	CN43-23	DSW12-5: ON, DSW12-6: OFF
		GTIOC02_2B	Input capture / output compare / PWM output pin	CN49-32	
AB10	P02_6/D6/MTIOC3D/MTIOC8B/GTIOC02_0B/GTADSM6_1/CMTW0_TOC0/SD0_IOVS/MDAT00/HDSL02_CLK1/POUTB	**SD0_IOVS**	**Voltage select of SD0**		**DSW17-5: OFF, DSW17-6: ON**
		D6	D6 of external bus	CN43-15	DSW17-5: ON, DSW17-6: OFF
		GTIOC02_0B	Input capture / output compare / PWM output pin	CN49-28	
AB11	P01_1/MTIOC3C/MTIOC8A/GTIOC00_4B/XSPI1_CS0#/MCLK20/ENCIFDI00/ENCIFDI04/RXDE00/RXDE04/HDSL00_MOSI2	**XSPI1_CS0#**	**CS# of QSPI**		
AB12	P01_7/MTIOC7D/MTIOC0B/GTIOC01_2B/GTIOC04_2B/XSPI1_IO3/SI03#/HDSL01_MOSI1	**XSPI1_IO3**	**IO3 of QSPI snd SPI expansion connector**	**CN19-9**	**DSW2-6: ON**
		GTIOC01_2B	Input capture / output compare / PWM output pin	CN49-20	DSW2-6: OFF
AB13	P00_0/SEI/D0/MTIOC3B/GTIOC00_0A/ETH3_TXER/USB_VBUSEN/DUEI00/HDSL00_LINK	**ETH3_TXER**	**TXER of Ethernet Port3**		**DSW5-8: ON**
		D0	D0 of external bus	CN43-1	DSW5-8: OFF, DSW2-5: OFF
		GTIOC00_0A	Input capture / output compare / PWM output pin	CN49-3	
		USB_VBUSEN	VBUS control of USB Host		DSW5-8: OFF, DSW2-5: ON, **DSW14-5: ON, DSW14-6: OFF, DSW16-3: OFF, DSW16-4: ON**
AB14	VSS				
AB15	VSS				
AB16	VSS				
AB17	VSS				
AB18	VSS				
AB19	VSS				
AB20	VSS				
AB21	VSS				
AB22	AN203	**AN203**	**ADC input (AN203)**	**CN5-7**	

AB23	AVSSIO_ADC2				
AB24	AN212	**AN212**	**ADC input (AN212)**	**CN6-9**	

Table 5-23 List of RZ/N2H Pin Function Selections (23)

Pin No.	Pin Name	Function	Description	Connector	Remarks
AC1	MDX	**MDX**	**Input of MDX setting**		
AC2	P08_5/IRQ8/RSTOUT#/GTETRGSA/IIC_SCL1/SD1_PWEN/MCLK02/HDSL06_MISO2	**SD1_PWEN**	**Power enable of SD1**		
AC3	P08_4/TDO/HDSL06_SEL2	**TDO**	**TDO of debug interface**	**CN23-6, CN24-6**	
AC4	RES#	**RES#**	**Reset input**		
AC5	P08_3/TCK/SI10#/HDSL06_CLK2	**TCK**	**TCK of debug interface**	**CN23-4 CN24-4**	
AC6	P06_0/XSPI0_IO2/TST_OUT08/HDSL04_MISO2	**XSPI0_IO2**	**Data IO2 of XSPI0**		
AC7	P05_7/XSPI0_IO1/DUEI08/HDSL04_SEL2	**XSPI0_IO1**	**Data IO1 of XSPI0**		
AC8	P06_7/IRQ12/POE4#/GTETRGD/GMAC1_MDC/IIC_SCL2/HDSL05_MISO1	**P06_7**	**GPIO of PMOD2**	**CN31-10**	
AC9	P02_7/D7/MTIOC4A/MTIC5U/GTIOC02_1A/GTADSM7_0/CMTW0_TIC1/MCLK01/HDSL02_SEL1/POUTZ	**P02_7**	**Control of user LED2**		**DSW17-3: OFF, DSW17-4: ON**
		D7	D7 of external bus	CN43-17	DSW17-3: ON, DSW17-4: OFF
		GTIOC02_1A	Input capture / output compare / PWM output pin	CN49-29	
AC10	VSS				
AC11	P01_5/MTIOC7C/MTIC5W/GTIOC01_1B/GTIOC04_1B/XSPI1_IO1/DUEI03/HDSL01_SEL1	**XSPI1_IO1**	**IO1 of QSPI and SPI expansion connector**	**CN19-11**	**DSW2-6: ON**
		GTIOC01_1B	Input capture / output compare / PWM output pin	CN49-18	DSW2-6: OFF
AC12	P01_3/MTIOC6D/MTIC5U/GTIOC01_0B/GTIOC04_0B/XSPI1_DS/TST_OUT02/HDSL01_SMPL	**GTIOC01_0B**	**Input capture / output compare / PWM output pin**	**CN49-16**	
AC13	P00_4/IRQ3/D4/MTIOC4B/GTIOC00_2A/ADTRG2#/TST_OUT01/HDSL00_MISO1	**IRQ3**	**Interrupt of user SW3**		
		D4	**D4 of external bus**	**CN17-9**	
		GTIOC00_2A	**Input capture / output compare / PWM output pin**	**CN24-7**	
AC14	USB_QDP	**USB_QDP**	**USB DP data I/O**		
AC15	VSS				
AF16	PCIE_RXDN_L1	**PCIE_RXDN_L1**	Data input (x1) of PCIe ch1	CN12-A17	DSW4-3: ON
			Data input (x4) of PCIe ch1	**CN11-A22**	**DSW4-3: OFF**
AC17	PCIE_RXDN_L0	**PCIE_RXDN_L0**	**Data input (x4) of PCIe ch0**	**CN11-A17**	
AC18	VSS				
AC19	PCIE_TXDN_L1	**PCIE_TXDN_L1**	Data output (x1) of PCIe ch1	CN12-B15	DSW4-3: ON
			Data output (x4) of PCIe ch1	**CN11-B20**	**DSW4-3: OFF**
AC20	PCIE_TXDN_L0	**PCIE_TXDN_L0**	**Data output (x4) of PCIe ch0**	**CN32-B15**	
AC21	VSS				
AC22	AN211	**AN211**	**ADC input (AN211)**	**CN6-7**	
AC23	AN204	**AN204**	**ADC input (AN204)**	**CN5-9**	
AC24	AN207	**AN207**	**ADC input (AN207)**	**CN5-15**	

Table 5-24 List of RZ/N2H Pin Function Selections (24)

Pin No.	Pin Name	Function	Description	Connector	Remarks
AD1	VSS				
AD2	P08_6/SEI/CKIO/GTIOC08_3A/GTETRGSB/IIC_SDA1/SD1_IOVS/MDAT02/MCLK11/DUEI11/HDSL06_MOSI2	CKIO	CKIO of external bus	CN43-2	DSW5-3: OFF
		SD1_IOVS	**Voltage select of SD1**		**DSW5-3: ON**
AD3	P08_1/TMS/DUEI10/HDSL06_MISO1	**TMS**	**TMS of debug interface**	**CN23-2, CN24-2**	
AD4	P08_2/TDI/TST_OUT10/HDSL06_MOSI1	**TDI**	**TDI of debug interface**	**CN23-8 CN24-8**	
AD5	P05_6/XSPI0_IO0/SI07#/HDSL04_CLK2	**XSPI0_IO0**	**Data IO0 of XSPI0**		
AD6	P05_5/XSPI0_DS/TST_OUT07/HDSL04_MOSI1	**XSPI0_DS**	**DS of XSPI0**		
AD7	P06_6/MDD/XSPI0_RESET0#	**MDD**	**Input of MDD setting**		
		XSPI0_RESET0#	**RESET# of OctaFlash**		
AD8	P05_3/IRQ5/XSPI0_CS0#/SI06#/HDSL04_SEL1	**XSPI0_CS0#**	**CS# of OctaFlash**		
AD9	P03_0/D8/MTIOC4C/MTIC5V/GTIOC02_1B/GTADSM7_1/CMTW0_TOC1/MDAT01/HDSL02_MISO1	**P03_0**	**Control of user LED3**		**DSW17-1: OFF, DSW17-2: ON**
		D8	D8 of external bus	CN43-19	DSW17-1: ON, DSW17-2: OFF
		GTIOC02_1B	Input capture / output compare / PWM output pin	CN49-30	
AD10	P02_5/D5/MTIOC3B/MTIOC8A/GTIOC02_0A/GTADSM6_0/CMTW0_TIC0/IIC_SCL0/SD0_PWEN/MCLK00/HDSL02_SMPL/POUTA	**SD0_PWEN**	**Power enable of SD0**		**DSW17-7: OFF, DSW17-8: ON**
		D5	D5 of external bus	CN43-13	DSW17-7: ON, DSW17-8: OFF
		GTIOC02_0A	Input capture / output compare / PWM output pin	CN49-27	
AD11	P01_6/MTIOC7B/MTIOC0A/GTIOC01_2A/GTIOC04_2A/XSPI1_IO2/TST_OUT03/HDSL01_MISO1	GTIOC01_2A	Input capture / output compare / PWM output pin	CN49-19	DSW2-6: OFF
		XSPI1_IO2	**IO2 of QSPI and SPI expansion connector**	**CN19-10**	**DSW2-6: ON**
AD12	P01_4/MTIOC7A/MTIC5V/GTIOC01_1A/GTIOC04_1A/XSPI1_IO0/SI02#/HDSL01_CLK1	GTIOC01_1A	Input capture / output compare / PWM output pin	CN49-17	DSW2-6: OFF
		XSPI1_IO0	**IO0 of QSPI and SPI expansion connector**	**CN19-12**	**DSW2-6: ON**
AD13	P00_3/IRQ2/D3/MTIOC4C/GTIOC00_1B/ETH3_COL/ADTRG1#/DUEI01/HDSL00_SEL1	D3	D3 of external bus	CN43-7	DSW12-1: ON, DSW12-2: OFF
		GTIOC00_1B	Input capture / output compare / PWM output pin	CN49-6	
		ETH3_COL	**COL of Ethernet Port3**		**DSW12-1: OFF, DSW12-2: ON**
AD14	USB_QDM	**USB_QDM**	**USB DM data I/O**		
AD15	VSS				
AD16	PCIE_RXDP_L1	**PCIE_RXDP_L1**	Data input (x1) of PCIe ch1	CN12-A16	SW4-3: ON
			Data input (x4) of PCIe ch1	**CN11-A21**	**SW4-3: OFF**
AD17	PCIE_RXDP_L0	**PCIE_RXDP_L0**	**Data input (x4) of PCIe ch0**	**CN32-A16**	
AD18	VSS				
AD19	PCIE_TXDP_L1	**PCIE_TXDP_L1**	Data output (x1) of PCIe ch1	CN8-B13	SW4-3: ON
			Data output (x4) of PCIe ch1	**CN32-B19**	**SW4-3: OFF**

AD20	PCIE_TXDP_L0	**PCIE_TXDP_L0**	**Data output (x4) of PCIe ch0**	**CN32-B14**	
AD21	VSS				
AD22	AN205	**AN205**	**ADC input (AN205)**	**CN5-11**	
AD23	AN214	**AN214**	**ADC input (AN214)**	**CN6-13**	
AD24	AVSSIO_ADC2				

6. Circuitry for Configuration

6.1 Types of Configuration Circuits

Since multiple functions are assigned to single pins and each function has to be selected for use in the RZ/N2H, the functions to be used should be selected through the following methods on this board.

(1) Switches

DIP switches DSW2 to DSW9 and DSW12 to DSW21 are mounted for selecting functions.

(2) Jumper blocks

JP5 to JP9, JP11 to JP23, JP30 to JP36, and JP38 to JP40 are mounted for selecting functions.

(3) Option links

The option links are as follows:

— Solder bridges and trace cuts

A solder bridge consists of two pads, which are insulated from each other at the time of shipment. Conduction can be set up for such pads by connecting them with solder or the like. A trace cut is a thin copper trace that connects two pads and sets up conduction between them. Such pads can be insulated from each other by cutting the trace between the pads.

Figure 6-1 Solder Bridge and Trace Cut

— 0-Ω and other resistors

A different function can be selected by switching the factory state of a 0-Ω resistor or other resistor between mounted and not mounted.

The subsequent sections describe which peripheral functions of the multi-functional RZ/N2H signals are enabled or disabled through the settings of switches, jumper blocks, and option links. The connection information for ICs and headers other than the RZ/N2H will also be shown. **Text in bold blue type** in the tables indicates the initial state of the configuration on the board as shipped. For the positions of switches, jumper blocks, and option links, refer to "3.3 Arrangement of Components".

The settings of switches or jumper blocks should be changed only when the power is turned off.

When removing soldered components, do not apply a soldering iron to the board for more than 5 seconds. This time restriction is to avoid any damage to components mounted nearby on the board.

When modifying an option link, always check the related option links to ensure that no signal contention or short circuit has occurred. Most of the RZ/N2H pins have multiplexed functions and some of the peripheral functions must be used exclusively of each other. Refer to the RZ/T2H and RZ/N2H Groups User's Manual: Hardware and this board's schematics for further information.

6.2 Configuration at Shipment

Figure 6-2 shows the state of switch settings and jumper block settings for the configuration at the time of shipment.

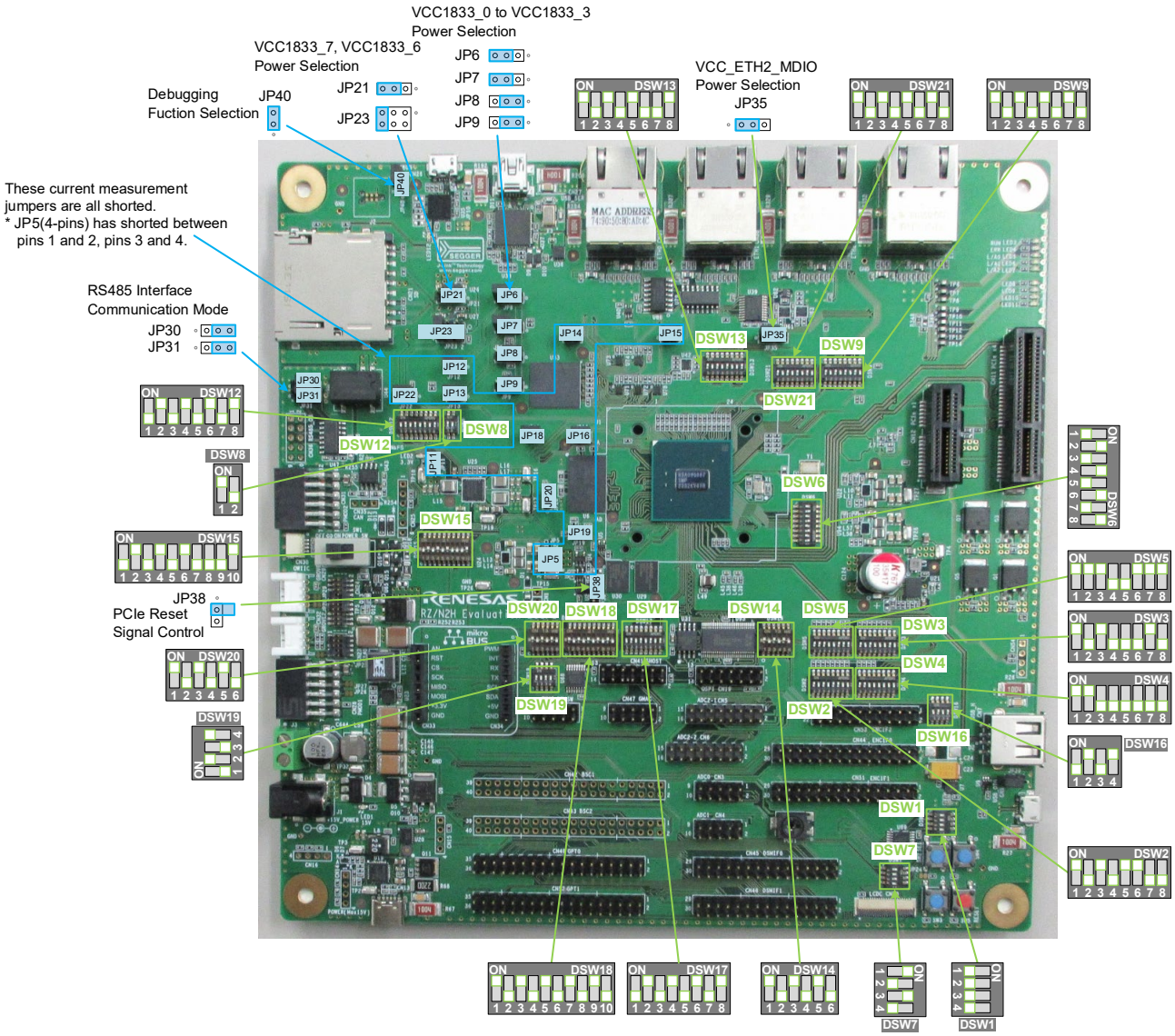


Figure 6-2 Switch Settings and Jumper Block Settings at Shipment

6.3 Configuration by Switches

This board is equipped with DIP switches DSW2 to DSW9 and DSW12 to DSW21 for selecting functions. The functions set by individual switches are explained below.

6.3.1 Mode Setting Switch DSW3

DSW3 is used to set the mode pins of the RZ/N2H. Table 6-1 lists the settings of DSW3.

Table 6-1 Functions of Mode Setting Switch DSW3

No.	Setting		Function
DSW3-1 MD0	OFF	MD0 = H	The operating mode of the RZ/N2H is selected with the combination of DSW3-1, DSW3-2, and DSW3-3 (MD0, MD1, and MD2). DSW3-6 (MDV) should be selected according to these settings. For details, see Table 6-2.
	ON	**MD0 = L**	
DSW3-2 MD1	**OFF**	**MD1 = H**	
	ON	MD1 = L	
DSW3-3 MD2	OFF	MD2 = H	
	ON	**MD2 = L**	
DSW3-4 MDW0	**OFF**	**MDW0 = H**	**The number of ATCM wait cycles of CPU0 in the Cortex-R52 is 1 wait cycle.**
	ON	MDW0 = L	The number of ATCM wait cycles of CPU0 in the Cortex-R52 is 0 wait cycles.
DSW3-5 MDW1	**OFF**	**MDW1 = H**	**The number of ATCM wait cycles of CPU1 in the Cortex-R52 is 1 wait cycle.**
	ON	MDW1 = L	The number of ATCM wait cycles of CPU1 in the Cortex-R52 is 0 wait cycles.
DSW3-6 MDV*	**OFF**	**MDV = H**	**The power-supply voltage of the boot peripheral is 3.3 V.**
	ON	MDV = L	The power-supply voltage of the boot peripheral is 1.8 V.
DSW3-7 MDD	OFF	MDD = H	JTAG mode = JTAG authentication in hash mode
	ON	**MDD = L**	**JTAG mode = Normal mode**
DSW3-8	Unused		**— (At the time of shipment = OFF)**

Note: This setting may have to be changed to suit the operating mode. It is “Don’t care” in SCI (UART) boot mode and USB boot mode.

Table 6-2 DSW3-1, DSW3-2, DSW3-3, and DSW3-6 (MD0, MD1, MD2, and MDV) and RZ/N2H Operating Mode

DSW3-3 (MD2)	DSW3-2 (MD1)	DSW3-1 (MD0)	DSW3-6 (MDV)	Operating Mode
ON	ON	ON	OFF (3.3 V)	xSPI0 boot mode (x1 boot serial flash)
ON	ON	OFF	OFF (3.3 V)	xSPI0 boot mode (x8 boot serial flash)*
ON	**OFF**	**ON**	**OFF (3.3 V)**	**xSPI1 boot mode (x1 boot serial flash)**
ON	OFF	OFF	OFF (3.3 V)	eSD boot mode
OFF	ON	ON	ON (1.8 V)	eMMC boot mode
OFF	ON	OFF	—	SCI (UART) boot mode
OFF	OFF	ON	—	USB boot mode
OFF	OFF	OFF	—	Reserved (setting prohibited)

Note: This setting is prohibited because OctaFlash is mounted.

6.3.2 Signal Function Selection Switches DSW2, DSW4 to DSW9, DSW12 to DSW21

DSW2, DSW4 to DSW9, and DSW12 to DSW21 are used to select the functions of the signal lines. Table 6-3 to Table 6-19 list the settings of DSW2, DSW4 to DSW9, and DSW12 to DSW21.

Table 6-3 Signal Function Selection Switch DSW2

No.	Setting	Function
DSW2-1	OFF	XTALSEL = H The resonator is selected as the clock input to the RZ/N2H.
	ON	**XTALSEL = L** **The oscillator is selected as the clock input to the RZ/N2H.**
DSW2-2	Unused	**— (At the time of shipment = OFF)**
DSW2-3	OFF	P27_2, P27_3, P27_6, and P31_3 are connected to Serial HOST(CN41), DSMIF1(CN46), GMAC(CN47), ETHSW(CN48), and ENCIF2(CN53).
	ON	**P27_2, P27_3, P27_6, and P31_3 are used as inputs to user DIP switches.**
DSW2-4	**OFF**	**P13_4, P13_5, and P14_0 are used as RXD3, TXD3, and DE3 of the RS485.**
	ON	P13_4, P13_5, and P14_0 are connected to LCDC(CN20), BSC1,2(CN42 and CN43), DSMIF1(CN46), and ETHSW(CN48).
DSW2-5	OFF	P00_0 to P00_2 are connected to BSC2(CN43) and GPT0(CN49).
	ON	**P00_0 to P00_2 are used as control signals for the USB power-supply IC.** **In this case, set DSW14-1, DSW14-3, and DSW14-5 to ON and DSW14-2, DSW14-4, and DSW14-6 to OFF.**
DSW2-6	OFF	P01_0, P01_2, P01_4 to P01_7, and P02_0 to P02_3 are connected to ENCIF0(CN44) and GPT0(CN49), and used as control signals for the USB power-supply IC. In case that P02_2 and P02_3 used as control signals for the USB power-supply IC, set DSW14-2 and DSW14-6 to ON and DSW14-1 and DSW14-5 to OFF.
	ON	**P01_0, P01_2, P01_4 to P01_7, and P02_0 to P02_3 are used as XSPI1 signals.**
DSW2-7	Unused	**— (At the time of shipment = OFF)**
DSW2-8	Unused	**— (At the time of shipment = OFF)**

Table 6-4 Signal Function Selection Switch DSW4

No.	Setting	Function
DSW4-1	OFF	PCIe L0 functions is used as Endpoint.
	ON	**PCIe L0 functions is used as Root Complex.**
DSW4-2	OFF	PCIe L1 functions is used as Endpoint.
	ON	**PCIe L1functions is used as Root Complex.**
DSW4-3	**OFF**	**The PCIe function is used in a configuration of 2 lanes × 1 port.**
	ON	The PCIe function is used in a configuration of 1 lane × 2 ports.
DSW4-4	Unused	**— (At the time of shipment = OFF)**
DSW4-5	**OFF**	**The 12-V power supply of the PCIe x1 connector CN12 is OFF.**
	ON	The 12-V power supply of the PCIe x1 connector CN12 is ON (when the x1 connector CN12 is used for the root complex).
DSW4-6	**OFF**	**The 3.3-V power supply of the PCIe x1 connector CN12 is OFF.**
	ON	The 3.3-V power supply of the PCIe x1 connector CN12 is ON (when the x1 connector CN12 is used for the root complex).
DSW4-7	**OFF**	**The 12-V power supply of the PCIe x4 connector CN11 is OFF.**
	ON	The 12-V power supply of the PCIe x4 connector CN11 is ON (when the x4 connector CN11 is used for the root complex).
DSW4-8	**OFF**	**The 3.3-V power supply of the PCIe x4 connector CN11 is OFF.**
	ON	The 3.3-V power supply of the PCIe x4 connector CN11 is ON (when the x4 connector CN11 is used for the root complex).

Table 6-5 Signal Function Selection Switch DSW5

No.	Setting		Function
DSW5-1, DSW5-2	-1	-2	
	OFF	OFF	P12_0 to P12_7 and P13_0 to 2 are connected to PCIe x4(CN11), PMOD1(CN28), PMOD2(CN31), BSC2(CN43), DSMIF0(CN45), and GPT1(CN52).
	OFF	ON	P12_0 to P12_5 are connected to SD card slot (CN21).
	ON	OFF	P12_0 and P12_1 are used as CAN I/F signals.
	ON	**ON**	**P12_0 to P12_7 and P13_0 to P13_2 are connected to eMMC.**
DSW5-3	OFF		P08_6 and P17_4 are connected to BSC1,2(CN42 and CN43).
	ON		**P08_6 and P17_4 are used as SD1 control signal.**
DSW5-4	Unused		**— (At the time of shipment = OFF)**
DSW5-5	Unused		**— (At the time of shipment = OFF)**
DSW5-6	OFF		MDC and MDIO of Ethernet port 2 are connected to GMAC2 (P30_5 and P30_6).
	ON		**MDC and MDIO of Ethernet port 2 are connected to GMAC0 (P21_4 and P21_5).**
DSW5-7	OFF		P29_1 to P29_7, P30_0 to P30_4, P30_7, P31_2, P31_4, and P31_5 are connected to Serial HOST(CN41), BSC1(CN42), DSMIF1(CN46), and ENCIF1(CN51).
	ON		**P29_1 to P29_7, P30_0 to P30_4, P30_7, P31_2, P31_4, and P31_5 are used as control signals for Ethernet Port 2.**
DSW5-8	OFF		P00_0 to P00_2, P33_2 to P33_7, and P34_0 to P34_6 are connected to mikroBUS™(CN33), BSC1,2(CN42 and CN43), DSMIF1(CN46), and GPT0,1(CN49 and CN52) and used as control signals for USB power supply IC, USB-to-Serial conversion signal, and PCIE_RSTOUT signal.
	ON		**P00_0 to P00_2, P33_2 to P33_7, and P34_0 to P34_6 are used as control signals for Ethernet Port 3.**

Table 6-6 Signal Function Selection Switch DSW6

No.	Setting		Function
DSW6-1, DSW6-2	-1	-2	
	ON	OFF	AN000 is connected to ADC0(CN3).
	OFF	**ON**	**AN000 is connected to the potentiometer.**
DSW6-3, DSW6-4	-3	-4	
	ON	OFF	AN100 is connected to ADC1(CN4).
	OFF	**ON**	**AN100 is connected to mikroBUS™(CN33).**
DSW6-5, DSW6-6	-5	-6	
	ON	OFF	AN101 is connected to ADC1(CN4).
	OFF	**ON**	**AN101 is connected to Grove(Analog)(CN32).**
DSW6-7, DSW6-8	-7	-8	
	ON	OFF	AN102 is connected to ADC1(CN4).
	OFF	**ON**	**AN102 is connected to Grove(Analog)(CN32).**

Table 6-7 Signal Function Selection Switch DSW7

No.	Setting		Function
DSW7-1, DSW7-2	-1	-2	
	ON	**OFF**	**P03_3 is used as I2C_SCL of U11, LCDC(CN20), Grove(I2C)(CN29), QWIIC(CN30), and mikroBUS™(CN34).**
	OFF	ON	P03_3 is used as IRQ13 of XSPI(CN19) or D11 of BSC2(CN43).
DSW7-3, DSW7-4	-3	-4	
	ON	**OFF**	**P03_4 is used as I2C_SDA of U11, LCDC(CN20), Grove(I2C)(CN29), QWIIC(CN30), and mikroBUS™(CN34).**
	OFF	ON	P03_4 is used as D12 of BSC2(CN43).

Table 6-8 Signal Function Selection Switch DSW8

No.	Setting		Function
DSW8-1, DSW8-2	-1	-2	
	ON	**OFF**	**P03_1_GMAC_RESETOUT2# is used as RESET for Ethernet Port 2.**
	OFF	ON	P11_0_ESC_RESETOUT# is used as RESET for Ethernet Port 2 as same as Ethernet Port 0 and 1.

Table 6-9 Signal Function Selection Switch DSW9

No.	Setting		Function
DSW9-1, DSW9-2	-1	-2	
	ON	**OFF**	**P27_4 is used as RXD0 of the USB-to-serial conversion.**
	OFF	ON	P27_4 is used as HSPI_IO2 of Serial HOST(CN41) or ENCIFOE14 of ENCIF2(CN53).
DSW9-3, DSW9-4	-3	-4	
	ON	**OFF**	**P27_5 is used as TXD0 of the USB-to-serial conversion.**
	OFF	ON	P27_5 is used as HSPI_IO3 of Serial HOST(CN41) or ENCIFDO14 of ENCIF2(CN53).
DSW9-5, DSW9-6	-5	-6	
	ON	**OFF**	**P33_3 is used as RXD1 of the USB-to-serial conversion.**
	OFF	ON	P33_3 is used as PCIEx4_PERST#, A17 of BSC1(CN42) or MDAT50 of DSMIF1(CN46).
DSW9-7, DSW9-8	-7	-8	
	ON	**OFF**	**P33_4 is used as TXD1 of the USB-to-serial conversion.**
	OFF	ON	P27_5 is used as PCIEx1_PERST#, A18 of BSC1(CN42) or MCLK51 of DSMIF1(CN46).

Table 6-10 Signal Function Selection Switch DSW12

No.	Setting		Function
DSW12-1, DSW12-2	-1	-2	
	ON	OFF	P00_3 is used as D3 of BSC2(CN43) or GTIOC00_1B of GPT0(CN49).
	OFF	**ON**	**P00_3 is used as P00_3_ETH3_COL of Ethernet Port 3.**
DSW12-3, DSW12-4	-3	-4	
	ON	OFF	P11_0 is used as DATG0 of LCDC(CN20) or A5 of BSC1(CN42).
	OFF	**ON**	**P11_0 is used as P11_0_ESC_RESETOUT# of Ethernet Port 0 and 1.**
DSW12-5, DSW12-6	-5	-6	
	ON	OFF	P03_2 is used as D10 of BSC2(CN43) or GTIOC02_2B of GPT0(CN49).
	OFF	**ON**	**P03_2 is used as P03_2_GMAC_RESETOUT3# of Ethernet Port 3.**
DSW12-7, DSW12-8	-7	-8	
	ON	OFF	P03_1 is used as D9 of BSC2(CN43) or GTIOC02_2A of GPT0(CN49).
	OFF	**ON**	**P03_1 is used as P03_1_GMAC_RESETOUT2# of Ethernet Port 2.** **In this case, set DSW8-1 to ON and DSW8-2 to OFF.**

Table 6-11 Signal Function Selection Switch DSW13

No.	Setting		Function
DSW13-1, DSW13-2	-1	-2	
	ON	**OFF**	**P26_7 is used as P26_7_ETH1_RXER of Ethernet Port 1.**
	OFF	ON	P26_7 is used as ENCIFDO01 of ENCIF0(CN44) or CS3# of BSC1(CN42).
DSW13-3, DSW13-4	-3	-4	
	ON	**OFF**	**P27_0 is used as P27_0_ETH1_CRS of Ethernet Port 1.**
	OFF	ON	P27_0 is used as HSPI_INT# of Serial HOST(CN41) or CS5# of BSC1(CN42).
DSW13-5, DSW13-6	-5	-6	
	ON	**OFF**	**P27_1 is used as P27_1_ETH1_COL of Ethernet Port 1.**
	OFF	ON	P27_1 is used as HSPI_CS# of Serial HOST(CN41).
DSW13-7, DSW13-8	-7	-8	
	ON	OFF	P13_7 is used as D31 of BSC2(CN43) or MDAT41 of DSMIF1(CN46).
	OFF	**ON**	**P13_7 is used as MDINT of Ethernet Port 2.**

Table 6-12 Signal Function Selection Switch DSW14

No.	Setting		Function
DSW14-1, DSW14-2	-1	-2	
	ON	**OFF**	**P00_1 is used as USB_OVRCUR.** **In this case, set DSW2-5 to ON.**
	OFF	ON	P02_3 is used as USB_OVRCUR. In this case, set DSW2-6 to OFF.
DSW14-3, DSW14-4	-3	-4	
	ON	**OFF**	**Setting fixed**
	OFF	ON	Setting prohibited
DSW14-5, DSW14-6	-5	-6	
	ON	**OFF**	**P00_0 is used as VBUSEN.** **In this case, set DSW2-5 to ON.**
	OFF	ON	P02_2 is used as VBUSEN. In this case, set DSW2-6 to OFF.

Table 6-13 Signal Function Selection Switch DSW15

No.	Setting		Function
DSW15-1, DSW15-2	-1	-2	
	ON	OFF	P22_6 is used as INT of PMOD2(CN31) or GMAC0_PTPTRG1 of GMAC(CN47).
	OFF	**ON**	**P22_6 is used as P22_6_SD0_WP.**
DSW15-3, DSW15-4	-3	-4	
	ON	OFF	P22_5 is used as P22_5_GMAC0_PTPTRG0 of GMAC(CN47).
	OFF	**ON**	**P22_5 is used as P22_5_SD0_CD.**
DSW15-5, DSW15-6	-5	-6	
	ON	OFF	P14_7 is used as SDA of I2C for EEPROM access.
	OFF	**ON**	**P14_7 is used as P14_7_USER_LED1(LED9).**
DSW15-7	Unused		**— (At the time of shipment = OFF)**

No.	Setting			Function
DSW15-8 to DSW15-10	-8	-9	-10	
	ON	OFF	OFF	P14_6 is used as P14_6_LCDC_DATG6 of LCDC(CN20)
	OFF	ON	OFF	P14_6 is used as SCK of I2C for EEPROM access.
	OFF	**OFF**	**ON**	**P14_6 is used as P14_6_USER_LED0(LED8).**

Table 6-14 Signal Function Selection Switch DSW16

No.	Setting		Function
DSW16-1, DSW16-2	-1	-2	
	ON	OFF	Setting prohibited
	OFF	**ON**	**USB_VUBUSIN is connected to VBUS of CN8 for Function.**
DSW16-3, DSW16-4	-3	-4	
	ON	OFF	Setting prohibited
	OFF	**ON**	**USB_VBUSEN is used as USB_HF_VBUSEN.**

Table 6-15 Signal Function Selection Switch DSW17

No.	Setting		Function
DSW17-1, DSW17-2	-1	-2	
	ON	OFF	P03_0 is used as D8 of BSC2(CN43) or GTIOC02_1B of GPT0(CN49).
	OFF	**ON**	**P03_0 is used as USER_LED3(LED11).**
DSW17-3, DSW17-4	-3	-4	
	ON	OFF	P02_7 is used as D7 of BSC2(CN43) or GTIOC02_1A of GPT0(CN49).
	OFF	**ON**	**P02_7 is used as USER_LED2(LED10).**
DSW17-5, DSW17-6	-5	-6	
	ON	OFF	P02_6 is used as D6 of BSC2(CN43) or GTIOC02_0B of GPT0(CN49).
	OFF	**ON**	**P02_6 is used as P02_6_SD0_IOVS.**
DSW17-7, DSW17-8	-7	-8	
	ON	OFF	P02_5 is used as D5 of BSC2(CN43) or GTIOC02_0A of GPT0(CN49).
	OFF	**ON**	**P02_5 is used as P02_5_SD0_PWEN.**

Table 6-16 Signal Function Selection Switch DSW18

No.	Setting		Function
DSW18-1, DSW18-2	-1	-2	
	ON	**OFF**	**P22_7 is used as ESC_LINKACT0(LED5).**
	OFF	ON	P22_7 is used as ETHSW_TDMAOUT0 of ETHSW(CN48).
DSW18-3, DSW18-4	-3	-4	
	ON	**OFF**	**P23_0 is used as ESC_LINKACT1(LED6).**
	OFF	ON	P23_0 is used as INT of mikroBUS™(CN34) or ETHSW_TDMAOUT3 of ETHSW(CN48).
DSW18-5, DSW18-6	-5	-6	
	ON	**OFF**	**P14_3 is used as ESC_LINKACT2(LED7).**
	OFF	ON	P14_3 is used as DATG3 of LCDC(CN20), INT of PMOD1(CN28), TX of mikroBUS™(CN34), DREQ of BSC1(CN42), or ENCIFOE00 of ENCIF0(CN44).
DSW18-7, DSW18-8	-7	-8	
	ON	**OFF**	**P31_6 is used as ESC_LEDRUN(LED3).**
	OFF	ON	P31_6 is used as TEND of BSC1(CN42) or GMAC2_PTPTRG0 of GMAC(CN47).
DSW18-9, DSW18-10	-9	-10	
	ON	**OFF**	**P18_1 is used as ESC_LEDERR(LED4).**
	OFF	ON	P18_1 is used as DATB2 of LCDC(CN20) or A9 of BSC1(CN42).

Table 6-17 Signal Function Selection Switch DSW19

No.	Setting				Function
DSW19-1, DSW19-2, DSW19-3, DSW19-4	-1	-2	-3	-4	
	ON	OFF	ON	OFF	P14_3 is used as SD1_CD.
	OFF	**ON**	-	-	**P17_4 is used as SD1_CD.**
	-	-	**OFF**	**ON**	**P14_3 is used as DATG3 of LCDC(CN20), INT of PMOD1(CN28), TX of mikroBUS™(CN34), DREQ of BSC1(CN42), ENCIFOE00 of ENCIF0(CN44), or LED7 of LINKACT2.**

Table 6-18 Signal Function Selection Switch DSW20

No.	Setting		Function
DSW20-1, DSW20-2	-1	-2	
	ON	**OFF**	**P14_3 is used as DREQ of BSC1(CN42)** **In this case, set DSW18-5 to OFF, DSW18-6 to ON, DSW19-3 to OFF, and DSW19-4 to ON.**
	OFF	ON	P31_4 is used as DREQ of BSC1(CN42) In this case, set DSW5-7 to OFF.
DSW20-3, DSW20-4	-3	-4	
	ON	**OFF**	**P14_4 is used as DACK of BSC1(CN42).**
	OFF	ON	P31_5 is used as DACK of BSC1(CN42). In this case, set DSW5-7 to OFF.
DSW20-5, DSW20-6	-5	-6	
	ON	**OFF**	**P14_5 is used as TEND of BSC1(CN42).**
	OFF	ON	P31_6 is used as TEND of BSC1(CN42).

Table 6-19 Signal Function Selection Switch DSW21

No.	Setting			Function
DSW21-1 to DSW21-3	-1	-2	-3	
	ON	**OFF**	**ON**	**P26_6 is used as P26_6_ETH1_TXER of Ethernet Port1 and P34_4 is used as CS2# of BSC1(CN42).** **In this case, set DSW5-8 to OFF.**
	OFF	ON	OFF	P26_6 is used as CS2# of BSC1(CN42).
DSW21-4, DSW21-5	-4	-5		
	ON	OFF		P26_7 is used as CS3# of BSC1(CN42). In this case, set DSW13-1 to OFF and DSW13-2 to ON.
	OFF	**ON**		**P34_5 is used as CS3# of BSC1(CN42).** **In this case, set DSW5-8 to OFF.**
DSW21-6, DSW21-7	-6	-7		
	ON	OFF		P27_0 is used as CS5# of BSC1(CN42). In this case, set DSW13-3 to OFF and DSW13-4 to ON.
	OFF	**ON**		**P34_6 is used as CS5# of BSC1(CN42).** **In this case, set DSW5-8 to OFF.**
DSW21-8	Unused			**— (At the time of shipment = OFF)**

6.4 Configuration by Jumper Blocks

This board is equipped with jumper blocks JP5 to JP9, JP11 to JP23, JP30 to JP36, and JP38 to JP40 for selecting functions. The functions set by individual jumper blocks are explained below.

6.4.1 I/O Power Selection Jumper Blocks JP6 to JP9, JP21, JP23 and JP35

JP6 to JP9, JP21, JP23, and JP35 are used to select the power supply to the I/O power domain of the RZ/N2H and Ethernet Phy. The supply of voltage to each power supply selected by JP6 to JP9, JP21, JP23, and JP35 must comply with the standards or usage methods of the I/O devices connected to that power domain. Otherwise, malfunctions of the device may occur or permanent damages may be caused.

Table 6-20 I/O Power Selection Jumper Blocks JP6 to JP9, JP21, JP23, and JP35

No.	Setting	Function
JP6	1-2 are short-circuit	1.8-V power is supplied to VCC1833_0. (for Ethernet Port 0)
	2-3 are short-circuit	**3.3-V power is supplied to VCC1833_0. (for Ethernet Port 0)**
JP7	1-2 are short-circuit	1.8-V power is supplied to VCC1833_1. (for Ethernet Port 1)
	2-3 are short-circuit	**3.3-V power is supplied to VCC1833_1. (for Ethernet Port 1)**
JP8	**1-2 are short-circuit**	**1.8-V power is supplied to VCC1833_2. (for Ethernet Port 2)**
	2-3 are short-circuit	3.3-V power is supplied to VCC1833_2. (for Ethernet Port 2)
JP9	**1-2 are short-circuit**	**1.8-V power is supplied to VCC1833_3. (for Ethernet Port 3)**
	2-3 are short-circuit	3.3-V power is supplied to VCC1833_3. (for Ethernet Port 3)
JP21	1-2 are short-circuit	3.3-V power is supplied to VCC1833_7. (for SD1)
	2-3 are short-circuit	**Power control IC output for SD1 is supplied to VCC1833_7. (for SD1)**
JP23	1-2 are short-circuit	3.3-V power is supplied to VCC1833_6. (for SD0)
	3-4 are short-circuit	The output from the power-supply control IC for SD0 is supplied to VCC1833_6 (for SD0).
	5-6 are short-circuit	**1.8-V power is supplied to VCC1833_6. (for SD0)**
JP35	**1-2 are short-circuit**	**VCC1833_0 is supplied to VCC_ETH2_MDIO (DSW5-6 is ON: When P21_4 and P21_5 are selected for MDIO).**
	2-3 are short-circuit	VCC1833_2 is supplied to VCC_ETH2_MDIO. (DSW5-6 is OFF: When P30_5 and P30_6 are selected for MDIO)

6.4.2 Debugging Function Selection Jumper Block JP40

JP40 is used to enable or disable the on-board debugging function J-Link™ OB.

Table 6-21 Debugging Function Selection Jumper Block JP40

No.	Setting	Function
JP40	Open-circuit	The on-board debugging function J-Link™ OB is enabled.
	Short-circuit	**The on-board debugging function J-Link™ OB is disabled.** **Connect an external emulator to CN23 or CN24 at debugging.**

6.4.3 RS485 Interface Communication Mode Selection Jumper Blocks JP30 and JP31

JP30 and JP31 are used to select the communication mode of the RS485 interface.

Table 6-22 RS485 Interface Communication Mode Selection Jumper Blocks JP30 and JP31

No.	Setting	Function
JP30, JP31	1-2 are short-circuit	Full-duplex communication
	2-3 are short-circuit	**Half-duplex communication**

6.4.4 PCIe Reset Signal Control Jumper Block JP38

JP38 is used to select whether the reset signal of the PCIe is included in the system reset factors.

Table 6-23 PCIe Reset Signal Control Jumper Block JP38

No.	Setting	Function
JP38	**Open-circuit**	**A PCIe reset is not included in the system reset factors.**
	Short-circuit	A PCIe reset is included in the system reset factors.

6.4.5 Current Measurement Jumper Blocks JP5, JP11 to JP16, JP18 to JP20, and JP22

JP5, JP11 to JP16, JP18 to JP20, and JP22 are jumper blocks for measuring the current drawn by the target device (RZ/N2H). When measuring the current, insert an ammeter between pins 1-2 of the corresponding jumper block (pins 1-2 and 3-4 in JP5).

Table 6-24 Current Measurement Jumper Blocks JP5, JP11 to JP16, JP18 to JP20, and JP22

No.	Function	Description
JP5	Current of CPU0V8 is measured.	**The jumper blocks are short-circuit at the time of shipment.** To measure the current, make the relevant jumper block open-circuit and insert an ammeter between pins 1-2 (pins 1-2 and 3-4 for JP5).
JP11	Current of CPU3V3 is measured.	
JP12	Current of VCC1833_0 is measured.	
JP13	Current of VCC1833_1 is measured.	
JP14	Current of VCC1833_2 is measured.	
JP15	Current of VCC1833_3 is measured.	
JP16	Current of CPU1V1 is measured.	
JP18	Current of CPU1V8 is measured.	
JP19	Current of VCC1833_4 is measured.	
JP20	Current of VCC1833_5 is measured.	
JP22	Current of VCC1833_6 is measured.	

6.5 Configuration by Option Links

6.5.1 Settings by Solder Bridges and Trace Cuts

This board is equipped with solder bridges JP28 and JP29, and trace cuts JP10, JP24, JP25, JP26, and JP27 for selecting functions. Table 6-25 lists the settings of each solder bridge and trace cut.

Table 6-25 Settings of Solder Bridges and Trace Cuts

No.	Setting	Function
JP10	Open-circuit	Setting prohibited.
	Short-circuit	**3.3-V power is supplied to the J-Link™ OB circuit.**
JP24	Open-circuit	SW2 (SEI) is not input to P18_2.
	Short-circuit	**SW2 (SEI) is input to P18_2.**
JP25	Open-circuit	Setting prohibited.
	Short-circuit	**Pin 9 of CN23 (MIPI-10) is connected to the ground.**
JP26	Open-circuit	PMOD1 (CN28) is not used with the SPI interface.
	Short-circuit	**PMOD1 (CN28) is used with the SPI interface.** **(In this case, JP28 should be left open-circuit.)**
JP27	Open-circuit	PMOD1 (CN28) is not used with the SPI interface.
	Short-circuit	**PMOD1 (CN28) is used with the SPI interface.** **(In this case, JP29 should be left open-circuit.)**
JP28	**Open-circuit**	**PMOD1 (CN28) is not used with the I^2C interface.**
	Short-circuit	PMOD1 (CN28) is used with the I^2C interface. (In this case, JP26 should be left open-circuit.)
JP29	**Open-circuit**	**PMOD1 (CN28) is not used with the I^2C interface.**
	Short-circuit	PMOD1 (CN28) is used with the I^2C interface. (In this case, JP27 should be left open-circuit.)

6.5.2 Settings by 0-Ω and other Resistors

The following 0-Ω and other resistors are or can be placed on this board, and the function to be used can be selected by changing the Fit/DNF state from the state as shipped. Table 6-26 lists the settings of 0-Ω and other resistors.

Table 6-26 Settings of 0-Ω and other Resistors

No.	Setting	Function
R254 (0Ω)	**Fit**	**The termination resistor for CAN_H is enabled.**
	DNF	The termination resistor for CAN_H is disabled.
R255 (0Ω)	**Fit**	**The termination resistor for CAN_L is enabled.**
	DNF	The termination resistor for CAN_L is disabled.
R268 (0Ω)	**Fit**	**The DE signal is used in the RE control of the RS485.**
	DNF	The DE signal is not used in the RE control of the RS485. In this case, install R183 (10-kΩ) and fix the RE signal to the low level.
R263 (0Ω)	**Fit**	**The 130-Ω termination resistor of RS485 A-B is enabled.**
	DNF	The 130-Ω termination resistor of RS485 A-B is disabled.
R281 (33Ω)	**Fit**	**MII is used for the MAC-PHY interface of Ethernet Port 0.**
	DNF	RGMII is used for the MAC-PHY interface of Ethernet Port 0.
R304 (33Ω)	**Fit**	**MII is used for the MAC-PHY interface of Ethernet Port 1.**
	DNF	RGMII is used for the MAC-PHY interface of Ethernet Port 1.
R326 (33Ω)*	Fit	MII is used for the MAC-PHY interface of Ethernet Port 2.
	DNF	**RGMII is used for the MAC-PHY interface of Ethernet Port 2.**
R349 (33Ω)*	Fit	MII is used for the MAC-PHY interface of Ethernet Port 3.
	DNF	**RGMII is used for the MAC-PHY interface of Ethernet Port 3.**

Note: When installing a resistor, use a 1608-size (mm) chip resistor.

7. User Circuits

This chapter describes the circuits on the board for each of its functions.

The initial state of this board at the time of shipment is indicated by the **text in bold blue type** in the "Settings of Configuration Circuits" column of each of the signal connection tables. Refer to the details on the configuration circuits in chapter 6.

7.1 Reset Circuit

A reset signal can be generated by the power-on reset IC and RES switch on the board. Figure 7-1 shows the configuration of the reset circuit.

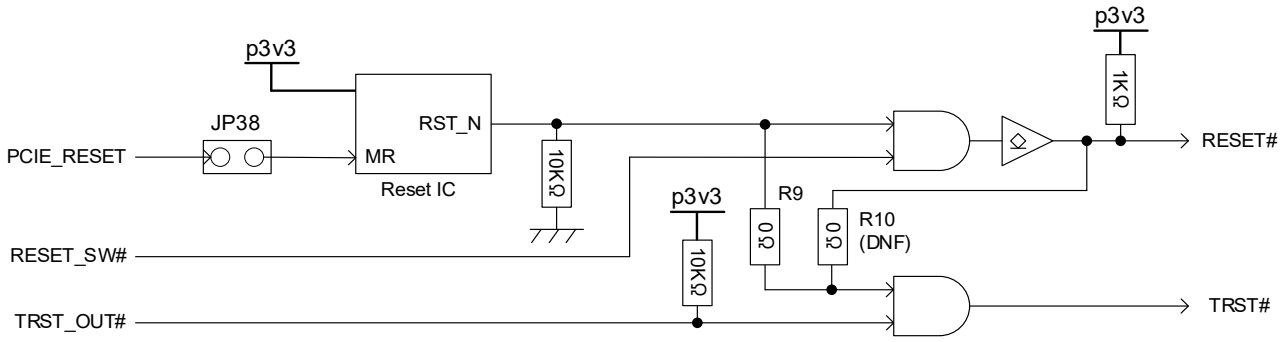


Figure 7-1 Configuration of Reset Circuit

7.2 Clock Circuit

Figure 7-2 shows the clock circuit for the RZ/N2H on this board. Table 7-1 lists the resonators.

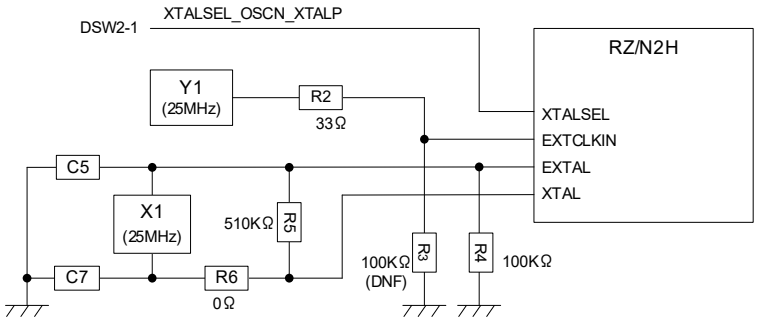


Figure 7-2 Configuration of Clock Circuit

Table 7-1 List of Resonators

Oscillator	Function or Intended Use	State as Shipped	Frequency
Y1	Clock for the RZ/N2H (oscillator)	Mounted	25 MHz
X1	Clock for the RZ/N2H	Mounted (Disabled)	25 MHz
X2	Clock for PCIe function	Mounted	25 MHz
X3	Clock for the USB-to-serial conversion IC	Mounted	12 MHz

7.3 Switches

This board is equipped with four push switches and nineteen DIP switches in addition to the power switch described in section 2.2. Table 7-2 lists the functions and signal connections of the four push switches. Table 7-3 lists the functions and signal connections of user DIP switch DSW1.

Among the DIP switches, DSW3 is used for setting the mode of the RZ/N2H, and DSW2, DSW4 to DSW9, and DSW12 to DSW21 are used for selecting the functions of the signal lines. Refer to section 6.2 in which the switches are explained as part of the configuration circuitry of this board.

Table 7-2 Signal Connections of Push Switches

Switch	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
RES (SW5)	Reset switch	RES#*	AC4	—
SEI (SW2)	Switch for user control. Connected to SEI.	P18_2	C12	—
SW3	Switch for user control. Connected to IRQ3.	P00_4	AC13	—
SW4	Switch for user control. Connected to IRQ4.	P18_7	F13	—

Note: Connected via the reset circuit.

Table 7-3 Signal Connections of DIP Switch DSW1 for User Control

Switch	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
DSW1-1	Connected to P27_2 for user control	P27_2*	B24	**DSW2-3: ON**
DSW1-2	Connected to P27_3 for user control	P27_3*	A23	
DSW1-3	Connected to P27_6 for user control	P27_6*	C24	
DSW1-4	Connected to P31_3 for user control	P31_3*	J22	

Note: Connected via the bus switch IC.

7.4 LEDs

This board is equipped with 20 LEDs. Table 7-4 lists the functions, colors, and signal connections of LEDs.

Table 7-4 Signal Connections of LEDs

LED	Color	Function or Intended Use	MPU		Settings of Configuration Circuits
			Port	Pin	
LED1 (P15V)	Yellow	Indicator of the 15-V power-supply line	—	—	—
LED2 (P3V3)	Green	Indicator of the 3.3-V power-supply line	—	—	—
LED3 (ESC_RUN)	Green	User LED or ESC_LEDRUN, also connected to TP6	P31_6*1	J20	**DSW18-7: ON, DSW18-8: OFF**
LED4 (ESC_ERR)	Red	User LED or ESC_LEDERR, also connected to TP7	P18_1*1	B12	**DSW18-9: ON, DSW18-10: OFF**
LED5 (ESC_L/A0)	Green	User LED or ESC_LINKACT0, also connected to TP8	P22_7*1	D18	**DSW18-1: ON, DSW18-2: OFF**
LED6 (ESC_L/A1)	Green	User LED or ESC_LINKACT1, also connected to TP9	P23_0*1	F17	**DSW18-3: ON, DSW18-4: OFF**
LED7 (ESC_L/A2)	Green	User LED or ESC_LINKACT2, also connected to TP10	P14_3*2	C10	**DSW18-5: ON, DSW18-6: OFF, DSW19-3: OFF, DSW19-4: ON**
LED8 (USER_LED0)	Green	User LED, also connected to TP11	P14_6*1	A10	**DSW15-8: OFF, DSW15-9: OFF, DSW15-10: ON**
LED9 (USER_LED1)	Green	User LED, also connected to TP12	P14_7*1	A9	**DSW15-5: OFF, DSW16-6: ON**
LED10 (USER_LED2)	Yellow	User LED, also connected to TP13	P02_7*1	AC9	**DSW17-3: OFF, DSW17-4: ON**
LED11 (USER_LED3)	Red	User LED, also connected to TP14	P03_0*1	AD9	**DSW17-1: OFF, DSW17-2: ON**
LED12	Yellow	Indicator of J-Link™ OB	—	—	—
LED built in CN37	Green	Ethernet port 0 LED (Link)	—	—	—
LED built in CN37	Yellow	Ethernet port 0 LED (Activity)	—	—	—
LED built in CN38	Green	Ethernet port 1 LED (Link)	—	—	—
LED built in CN38	Yellow	Ethernet port 1 LED (Activity)	—	—	—
LED built in CN39	Green	Ethernet port 2 LED (Link)	—	—	—
LED built in CN39	Yellow	Ethernet port 2 LED (Activity)	—	—	—
LED built in CN40	Green	Ethernet port 3 LED (Link)	—	—	—
LED built in CN40	Yellow	Ethernet port 3 LED (Activity)	—	—	—

Notes: 1. Connected via DIP switches. If the factory settings are used, they can be used for controlling LEDs.
2. Connected via the bus switch IC and DIP switch. If the factory settings are used, they can be used for controlling LEDs.

7.5 Potentiometer

On this board, a 10-kΩ single-rotation potentiometer for evaluating the ADC is connected to AN000 (pin R24) of the RZ/N2H. Figure 7-3 shows the configuration of the potentiometer circuit.

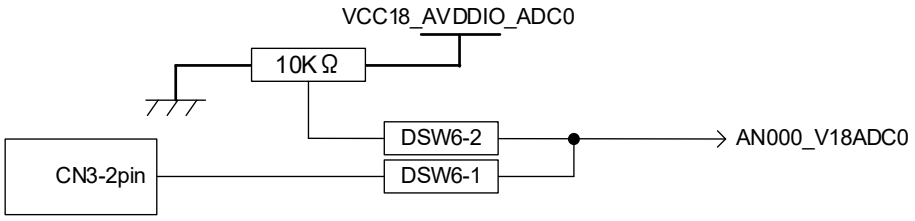


Figure 7-3 Configuration of Potentiometer Circuit

A potentiometer is installed to provide an easy way of supplying a variable analog input to the microprocessor. Note in advance that it will not guarantee the accuracy of the A/D converter.

7.6 Pmod™

This board is equipped with two connectors for Digilent Pmod™ interfaces so that compatible Pmod™ modules can be connected and evaluated. PMOD1 (CN28) supports the type 2A and 6A Pmod™ interfaces and PMOD2 (CN31) supports type 3A. Figure 7-4 shows the configuration of the Pmod™ interface circuits. Table 7-5 and Table 7-6 list the signal connections. Figure 7-5 shows the switch settings when using PMOD1 and PMOD2.

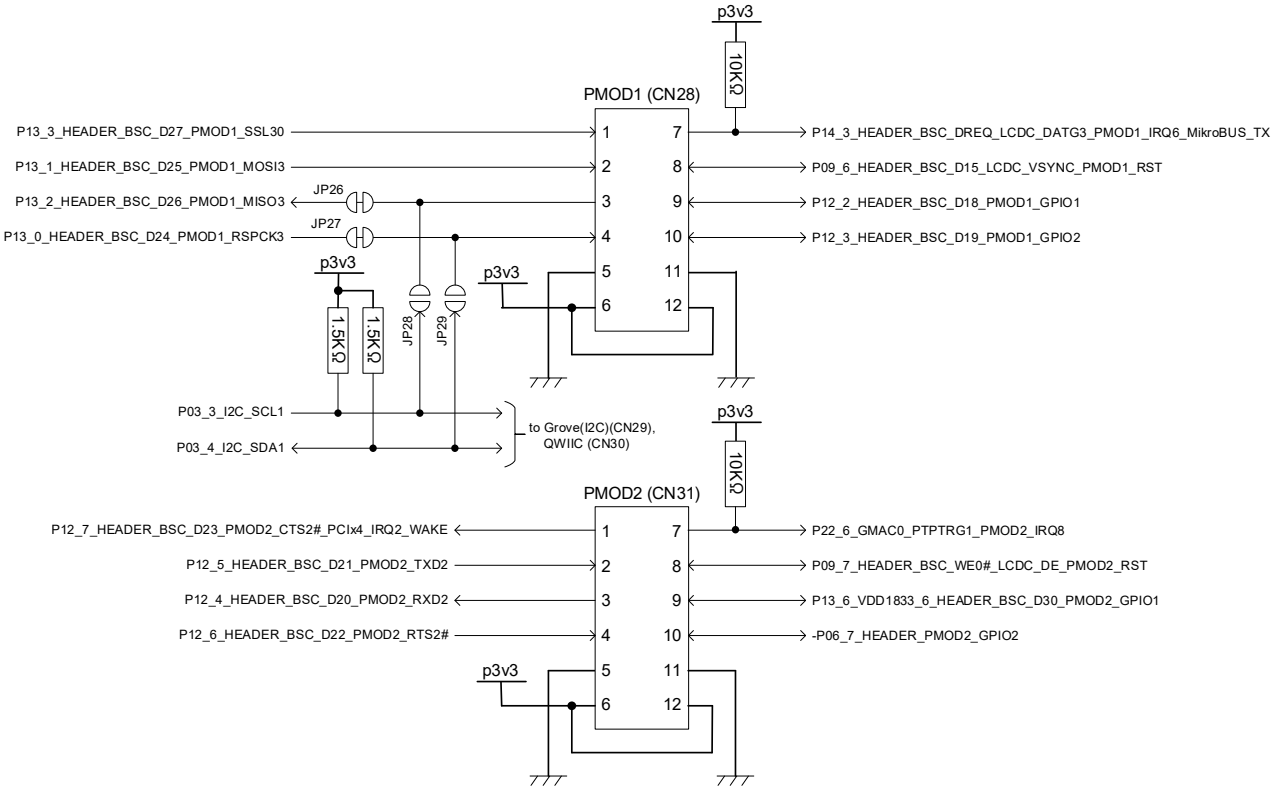


Figure 7-4 Configuration of Pmod™ Interface Circuits

Table 7-5 Signal Connections of PMOD1 Connector (CN28)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P13_3_HEADER_BSC_D27_PMOD1_SSL30	P13_3*1	F9	—
2	P13_1_HEADER_BSC_D25_PMOD1_MOSI3	P13_1*2	C6	DSW5-1: OFF, DSW5-2: OFF
3	P13_2_HEADER_BSC_D26_PMOD1_MISO3	P13_2*2	F8	DSW5-1: OFF, DSW5-2: OFF, **JP26: Short, JP28: Open**
	P03_3_I2C_SCL1	P03_3*3	AA9	**DSW7-1: ON, DSW7-2: OFF,** JP26: Open, JP28: Short
4	P13_0_HEADER_BSC_D24_PMOD1_RSPCK3	P13_0*2	B7	DSW5-1: OFF, DSW5-2: OFF, **JP27: Short, JP29: Open**
	P03_4_I2C_SDA1	P03_4*3	W9	**DSW7-3: ON, DSW7-4: OFF,** JP27: Open, JP29: Short
5	GROUND	-	—	—
6	p3v3	-	—	—
7	P14_3_HEADER_BSC_DREQ_LCDC_DATG3_PMOD1_IRQ6_MikroBUS_TX	P14_3*4	C10	DSW5-3: OFF, DSW18-5: OFF, DSW18-6: ON
8	P09_6_HEADER_BSC_D15_LCDC_VSYNC_PMOD1_RST	P09_6	C1	—
9	P12_2_HEADER_BSC_D18_PMOD1_GPIO1	P12_2*2	E8	DSW5-1: OFF, DSW5-2: OFF
10	P12_3_HEADER_BSC_D19_PMOD1_GPIO2	P12_3*2	F7	
11	GROUND	—	—	—
12	p3v3	—	—	—

Notes: 1. Connected via the level shifter IC.
2. Connected via the level shifter IC with an enable function.
3. Connected via the DIP switch and the setting of a solder bridge jumper has to be changed.
4. Connected via the bus switch IC and DIP switches.

Table 7-6 Signal Connections of PMOD2 Connector (CN31)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P12_7_HEADER_BSC_D23_PMOD2_CTS2#_PCIx4_IRQ2_WAKE	P12_7*1	B6	DSW5-1: OFF, DSW5-2: OFF
2	P12_5_HEADER_BSC_D21_PMOD2_TXD2	P12_5*1	D7	
3	P12_4_HEADER_BSC_D20_PMOD2_RXD2	P12_4*1	B8	
4	P12_6_HEADER_BSC_D22_PMOD2_RTS2#	P12_6*1	D6	
5	GROUND	—	—	—
6	p3v3	—	—	—
7	P22_6_GMAC0_PTPTRG1_PMOD2_IRQ8	P22_6*2	C18	DSW15-1: ON, DSW15-2: OFF
8	P09_7_HEADER_BSC_WE0#_LCDC_DE_PMOD2_RST	P09_7	C4	—
9	P13_6_VDD1833_6_HEADER_BSC_D30_PMOD2_GPIO1	P13_6*3	E6	—
10	P06_7_HEADER_PMOD2_GPIO2	P06_7	AC8	—
11	GROUND	—	—	—
12	p3v3	—	—	—

Notes: 1. Connected via the level shifter IC with an enable function.
2. Connected via the DIP switch.
3. Connected via the level shifter IC.

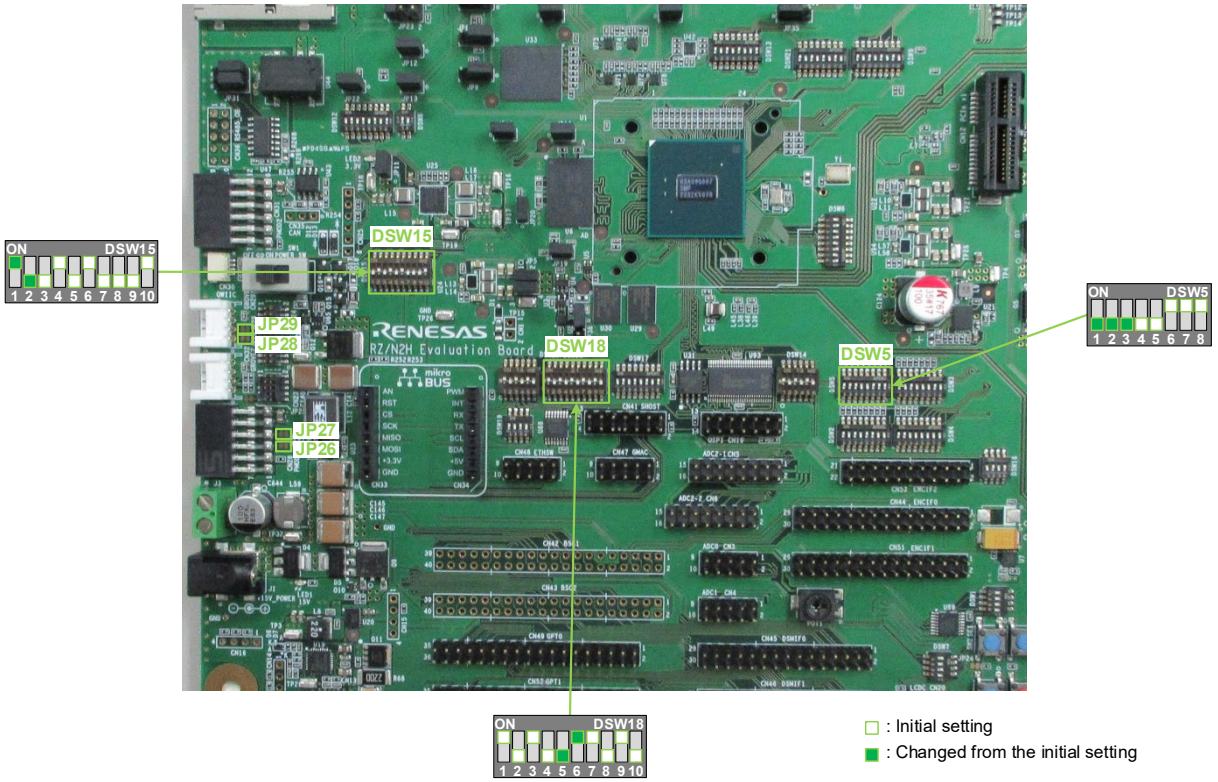


Figure 7-5 Switch Settings When Using PMOD1 and PMOD2

Note that the pin assignment for a Digilent Pmod™ connector differs in terms of numbering from that for a typical connector. Figure 7-6 shows the pin assignment for a Pmod™ connector. For details, refer to the Digilent Pmod™ Interface Specification.

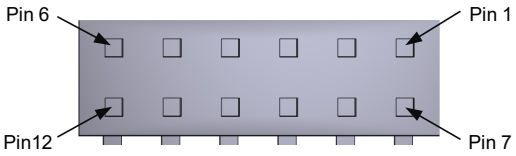


Figure 7-6 Pin Assignment for a Digilent Pmod™ Connector (Viewed from the Direction of Insertion)

7.7 Grove

This board is equipped with two connectors for Grove interfaces so that compatible Grove modules can be connected and evaluated. Figure 7-7 shows the configuration of the Grove interface circuits and Figure 7-8 shows the pin assignment for a Grove connector. Table 7-7 and Table 7-8 list the signal connections.

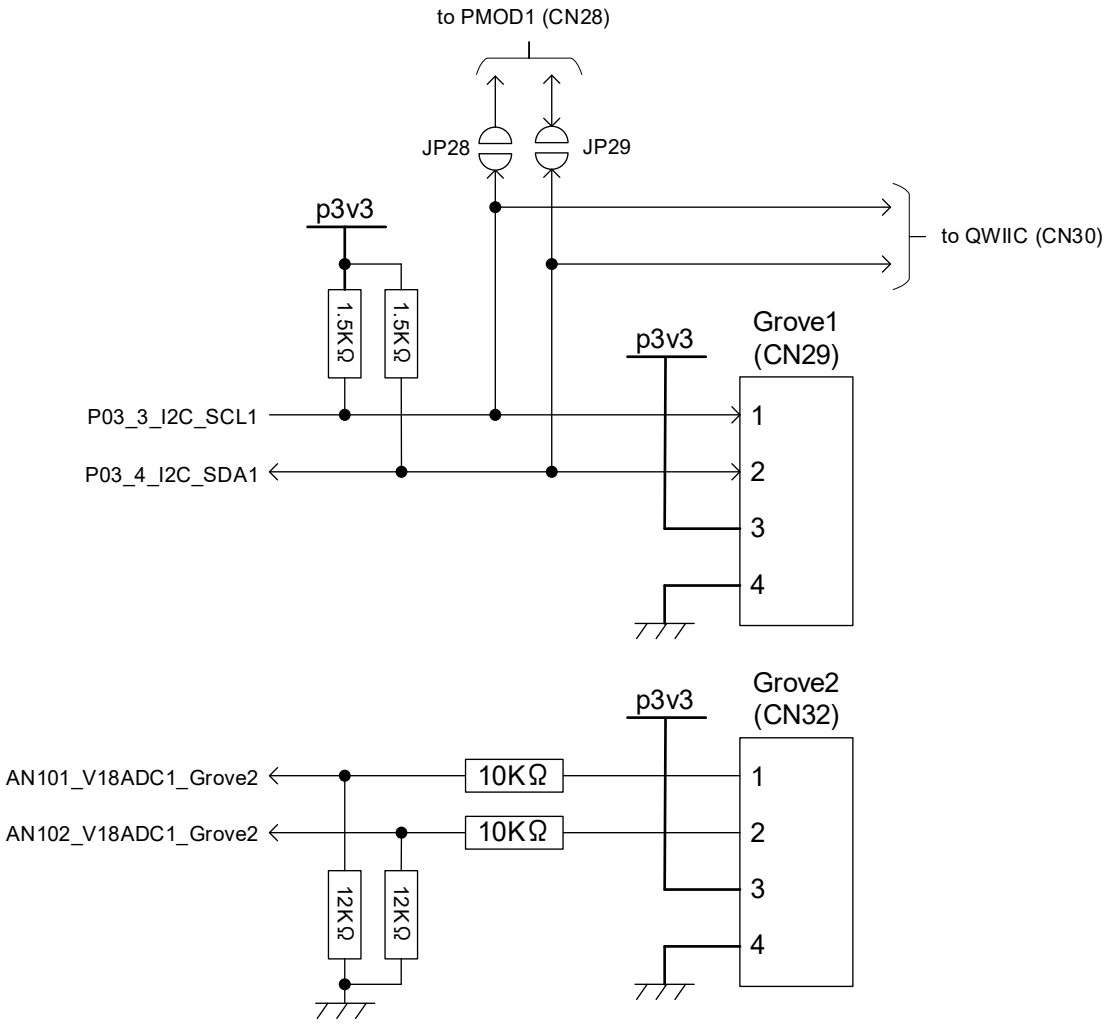


Figure 7-7 Configuration of Grove Interface Circuits

Table 7-7 Signal Connections of Grove1 Connector (CN29)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P03_3_I2C_SCL1	P03_3*	AA9	DSW7-1: ON, DSW7-2: OFF
2	P03_4_I2C_SDA1	P03_4*	W9	DSW7-3: ON, DSW7-4: OFF
3	p3v3	—	—	—
4	GROUND	—	—	—

Note: Connected via the DIP switch.

Table 7-8 Signal Connections of Grove2 Connector (CN32)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	AN101_V18ADC1_Grove2	AN101*	V24	DSW6-5: OFF, DSW6-6: ON
2	AN102_V18ADC1_Grove2	AN102*	V23	DSW6-7: OFF, DSW6-8: ON
3	p3v3	—	—	—
4	GROUND	—	—	—

Note: Connected via the DIP switch.

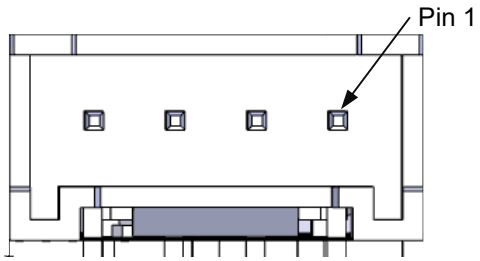


Figure 7-8 Pin Assignment for a Grove Connector (Viewed from the Direction of Insertion)

7.8 QWIIC

This board is equipped with a connector for the QWIIC interface so that a compatible QWIIC module can be connected and evaluated. Figure 7-9 shows the pin assignment for a QWIIC connector, and Table 7-9 lists the signal connections.

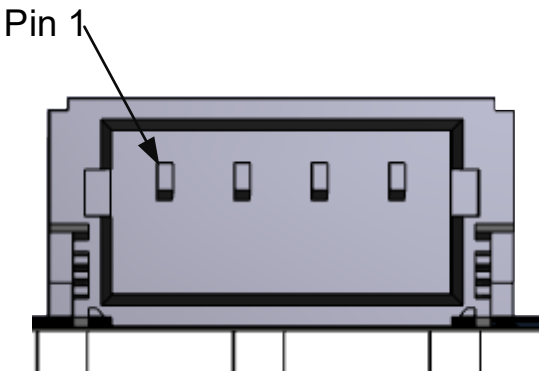


Figure 7-9 Pin Assignment for a QWIIC Connector (Viewed from the Direction of Insertion)

Table 7-9 Signal Connections of QWIIC Connector (CN30)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	GROUND	—	—	—
2	p3v3	—	—	—
3	P03_3_I2C_SCL1	P03_3*	AA9	**DSW7-1: ON, DSW7-2: OFF**
4	P03_4_I2C_SDA1	P03_4*	W9	**DSW7-3: ON, DSW7-4: OFF**

Note: Connected via the DIP switch.

7.9 mikroBUS™

This board is equipped with two connectors for mikroBUS™ interfaces so that compatible mikroBUS™ modules can be connected and evaluated. Figure 7-10 shows the configuration of the mikroBUS™ interface circuits, and Table 7-10 and Table 7-11 list the signal connections. Figure 7-11 shows the switch settings when using mikroBUS™.

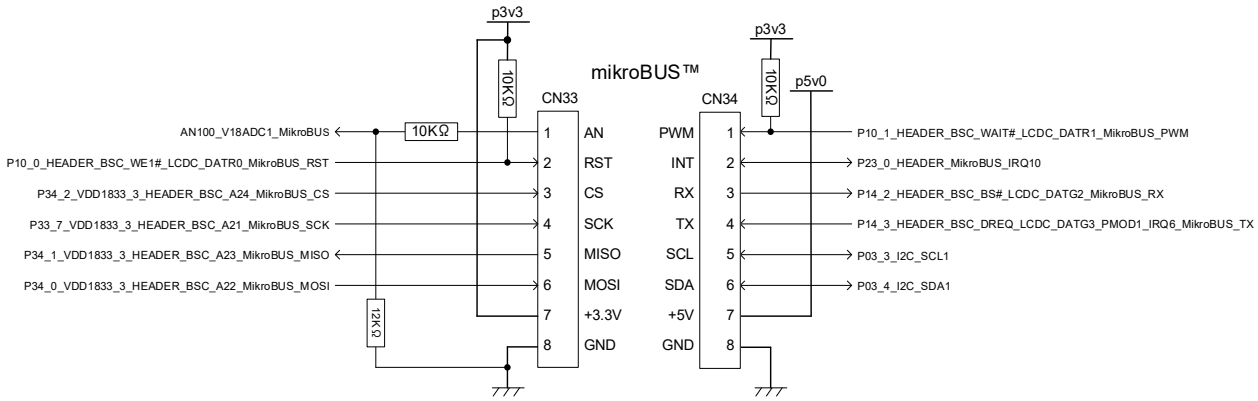


Figure 7-10 Configuration of mikroBUS™ Interface Circuits

Table 7-10 Signal Connections of mikroBUS™ Connector (CN33)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	AN100_V18ADC1_MikroBUS	AN100*1	U23	**DSW6-3: OFF, DSW6-4: ON**
2	P10_0_HEADER_BSC_WE1#_LCDC_DATR0_MikroBUS_RST	P10_0	C2	—
3	P34_2_VDD1833_3_HEADER_BSC_A24_MikroBUS_CS	P34_2*2	K22	DSW5-8: OFF
4	P33_7_VDD1833_3_HEADER_BSC_A21_MikroBUS_SCK	P33_7*2	L23	
5	P34_1_VDD1833_3_HEADER_BSC_A23_MikroBUS_MISO	P34_1*2	K20	
6	P34_0_VDD1833_3_HEADER_BSC_A22_MikroBUS_MOSI	P34_0*2	L22	
7	p3v3	—	—	—
8	GROUND	—	—	—

Notes: 1. Connected via the DIP switch.
2. Connected via the bus switch IC.

Table 7-11 Signal Connections of mikroBUS™ Connector (CN34)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P10_1_HEADER_BSC_WAIT#_LCDC_DATR1_MikroBUS_PWM	P10_1	B2	—
2	P23_0_HEADER_MikroBUS_IRQ10	P23_0*1	F17	DSW18-3: OFF, DSW18-4: ON
3	P14_2_HEADER_BSC_BS#_LCDC_DATG2_MikroBUS_RX	P14_2	E9	—
4	P14_3_HEADER_BSC_DREQ_LCDC_DATG3_PMOD1_IRQ6_MikroBUS_TX	P14_3*2	C10	DSW5-3: OFF, DSW18-5: OFF, DSW18-6: ON
5	P03_3_I2C_SCL1	P03_3*1	AA9	**DSW7-1: ON, DSW7-2: OFF**
6	P03_4_I2C_SDA1	P03_4*1	W9	**DSW7-3: ON, DSW7-4: OFF**
7	p5v0	—	—	—
8	GROUND	—	—	—

Notes: 1. Connected via the DIP switch.
2. Connected via the bus switch IC and DIP switch.

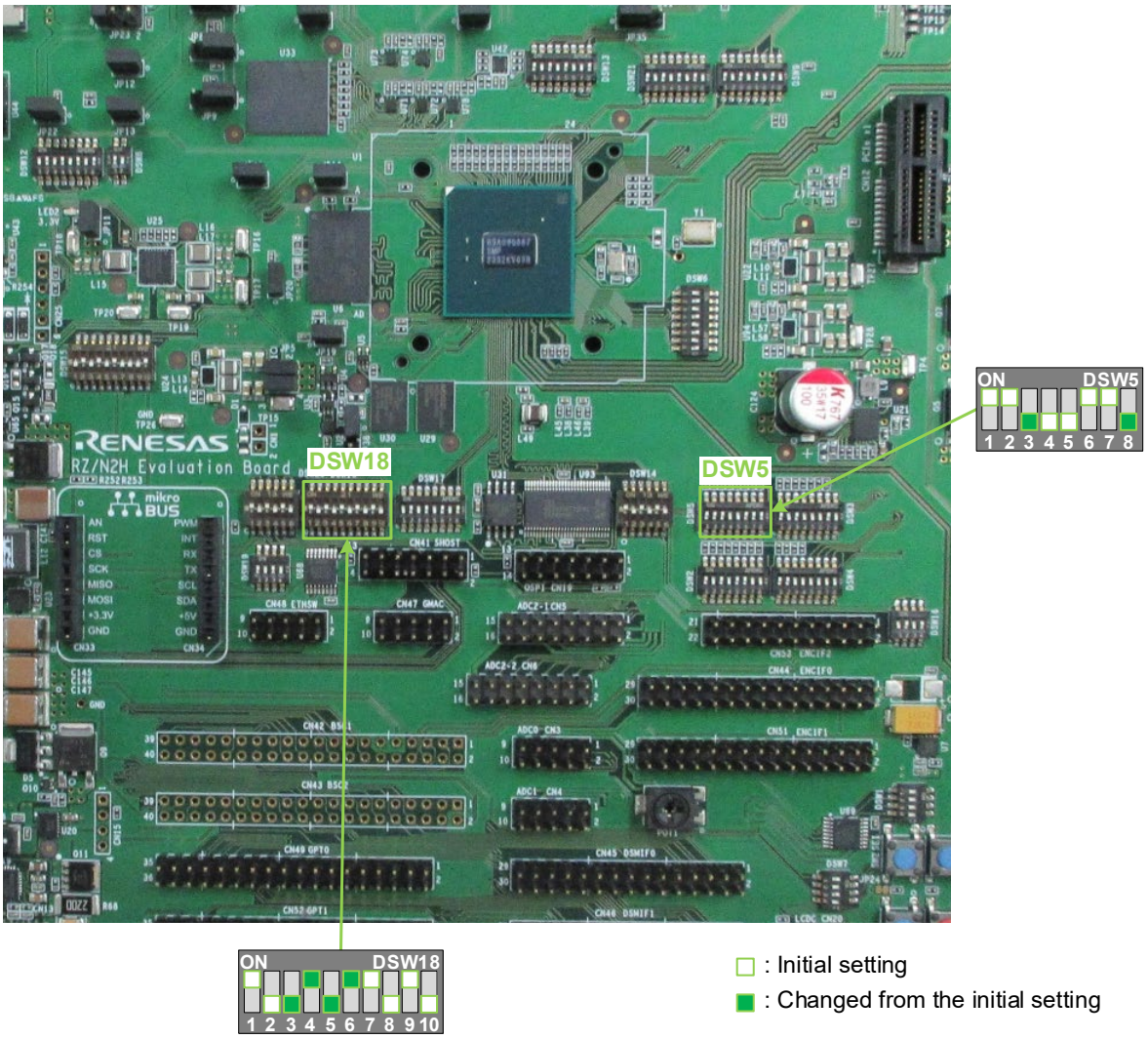


Figure 7-11 Switch Settings When Using mikroBUS™

7.10 USB-to-Serial Conversion

This board is equipped with a USB connector (CN27) for terminal output and a FT2232 for USB-to-serial conversion. Figure 7-12 shows the configuration of the USB-to-serial conversion circuit, and Table 7-12 lists the signal connections. Figure 7-13 shows the switch settings when using USB-to-Serial Conversion Circuit.

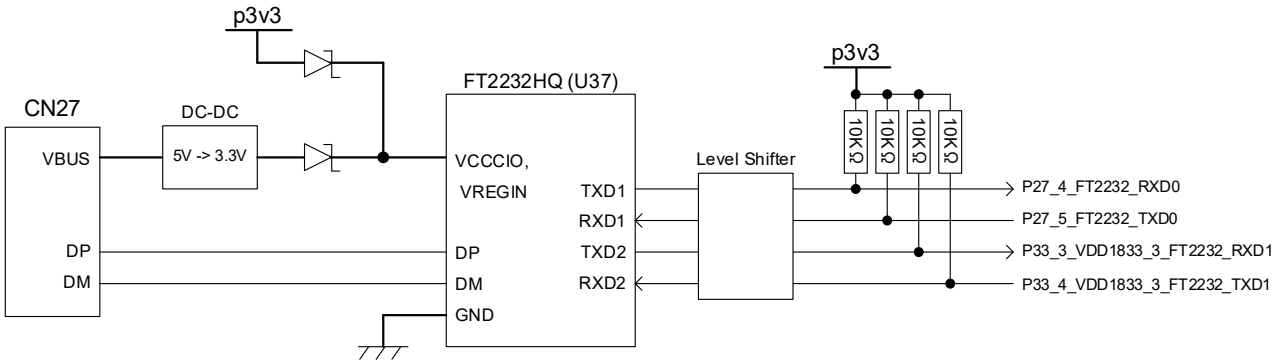
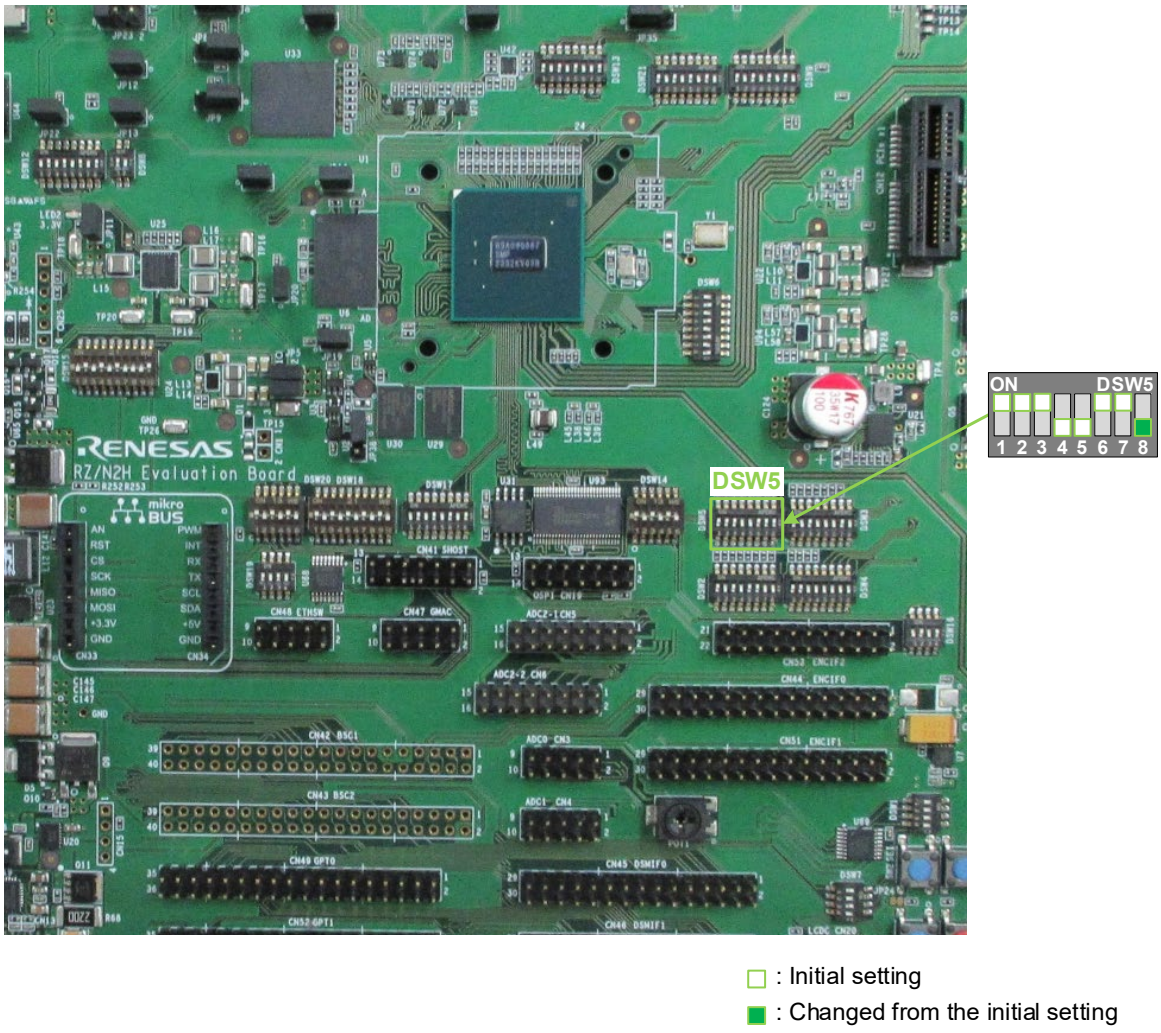


Figure 7-12 Configuration of USB-to-Serial Conversion Circuit

Table 7-12 Signal Connections of USB-to-Serial Conversion

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P27_4_FT2232_RXD0	Reception of UART data 1 for USB-to-serial conversion	P27_4*1	D23	**DSW9-1: ON, DSW9-2: OFF**
P27_5_FT2232_TXD0	Transmission of UART data 1 for USB-to-serial conversion	P27_5*1	C23	**DSW9-3: ON, DSW9-4: OFF**
P33_3_VDD1833_3_FT2232_RXD1	Reception of UART data 2 for USB-to-serial conversion	P33_3*2	M20	DSW5-8: OFF, **DSW9-5: ON, DSW9-6: OFF**
P33_4_VDD1833_3_FT2232_TXD1	Transmission of UART data 2 for USB-to-serial conversion	P33_4*2	N20	DSW5-8: OFF, **DSW9-7: ON, DSW9-8: OFF**

Notes: 1. Connected via the level shifter IC and DIP switch.
2. Connected via the level shifter IC, bus switch IC, and DIP switch.



□ : Initial setting
■ : Changed from the initial setting

Figure 7-13 Switch Settings When Using USB-to-Serial Conversion Circuit

When the USB connector (CN27) for terminal output is first connected to a PC, the PC will search for a driver. A driver with the standard specification that has been installed on the PC should be used.

7.11 SPI Memory

This board has OctaFlash, Quad SPI flash memory, and EEPROM as SPI memory. An SPI expansion connector (CN19) is also connected to SPI1.

Figure 7-14 shows the configuration of SPI memory circuits, and Table 7-13 lists the SPI memories. Table 7-14, Table 7-15, and Table 7-16 list the signal connections for each memory. Table 7-17 lists the signal connections for the SPI expansion connector. Figure 7-15 and Figure 7-16 show the switch settings when using EEPROM and SPI memory.

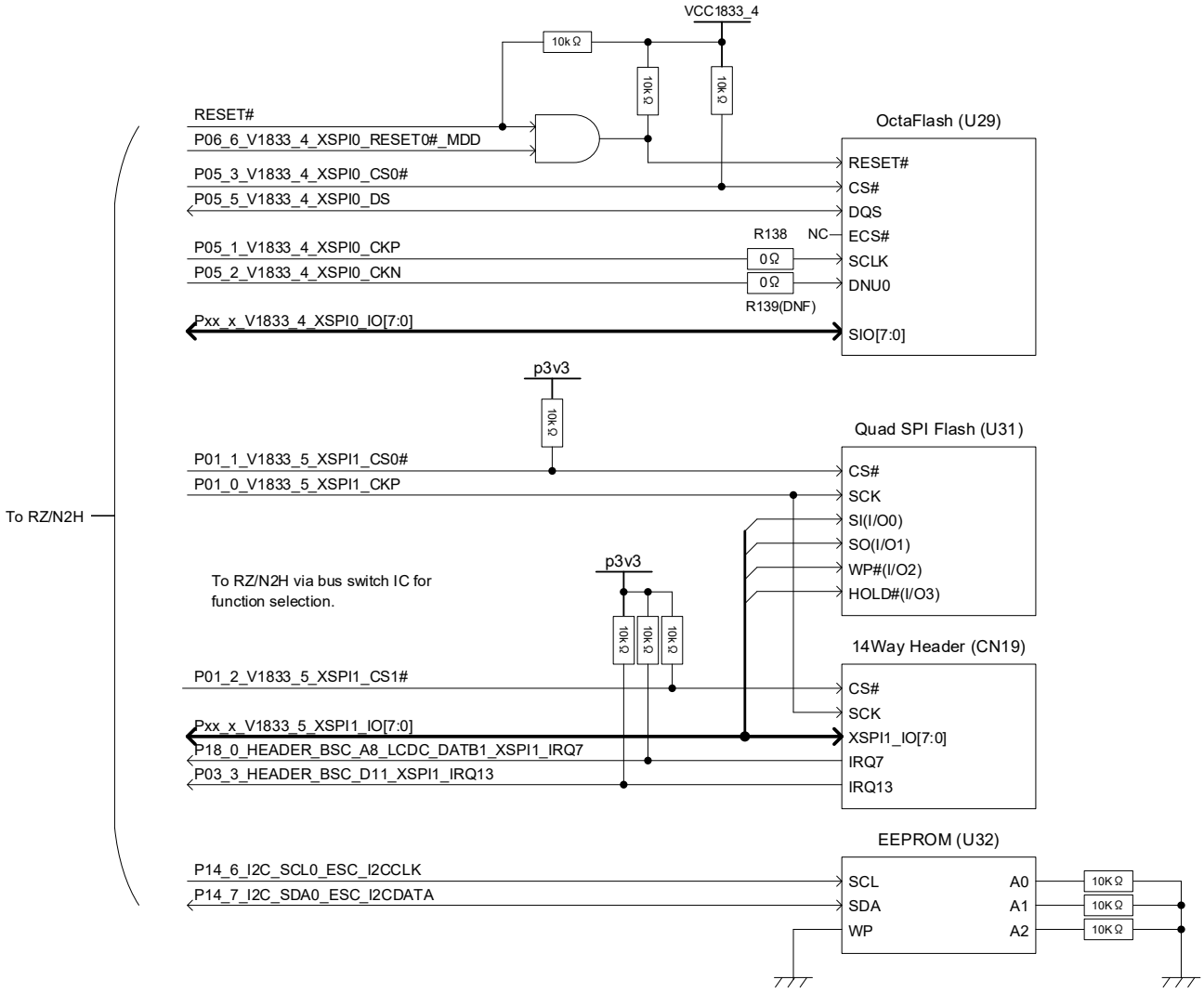


Figure 7-14 Configuration of SPI Memory Circuits

Table 7-13 List of SPI Memories

Device	Location	Controller	Address Space
OctaFlash (512 Mbits)	U29	XSPI0_CS0	40000000h - 43FFFFFFh (64Mbyte)
Quad SPI flash memory (128 Mbits)	U31	XSPI1_CS0	50000000h - 50FFFFFFh (16Mbyte)
EEPROM (16 Kbits)	U32	I2C or EtherCAT	—

Table 7-14 Signal Connections of OctaFlash

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P06_6_V1833_4_XSPI0_RESET0#_MDD	Reset for CS0	P06_6	AD7	—
P05_3_V1833_4_XSPI0_CS0#	CS0#	P05_3	AD8	—
P05_5_V1833_4_XSPI0_DS	DS	P05_5	AD6	—
P05_1_V1833_4_XSPI0_CKP	CKP	P05_1	AA7	—
P05_2_V1833_4_XSPI0_CKN	CKN	P05_2	AB6	—
P06_5_V1833_4_XSPI0_IO7	Data 7	P06_5	W7	—
P06_4_V1833_4_XSPI0_IO6	Data 6	P06_4	Y8	—
P06_3_V1833_4_XSPI0_IO5	Data 5	P06_3	W8	—
P06_2_V1833_4_XSPI0_IO4	Data 4	P06_2	Y7	—
P06_1_V1833_4_XSPI0_IO3	Data 3	P06_1	AB7	—
P06_0_V1833_4_XSPI0_IO2	Data 2	P06_0	AC6	—
P05_7_V1833_4_XSPI0_IO1	Data 1	P05_7	AC7	—
P05_6_V1833_4_XSPI0_IO0	Data 0	P05_6	AD5	—

Table 7-15 Signal Connections of Quad SPI Flash Memory

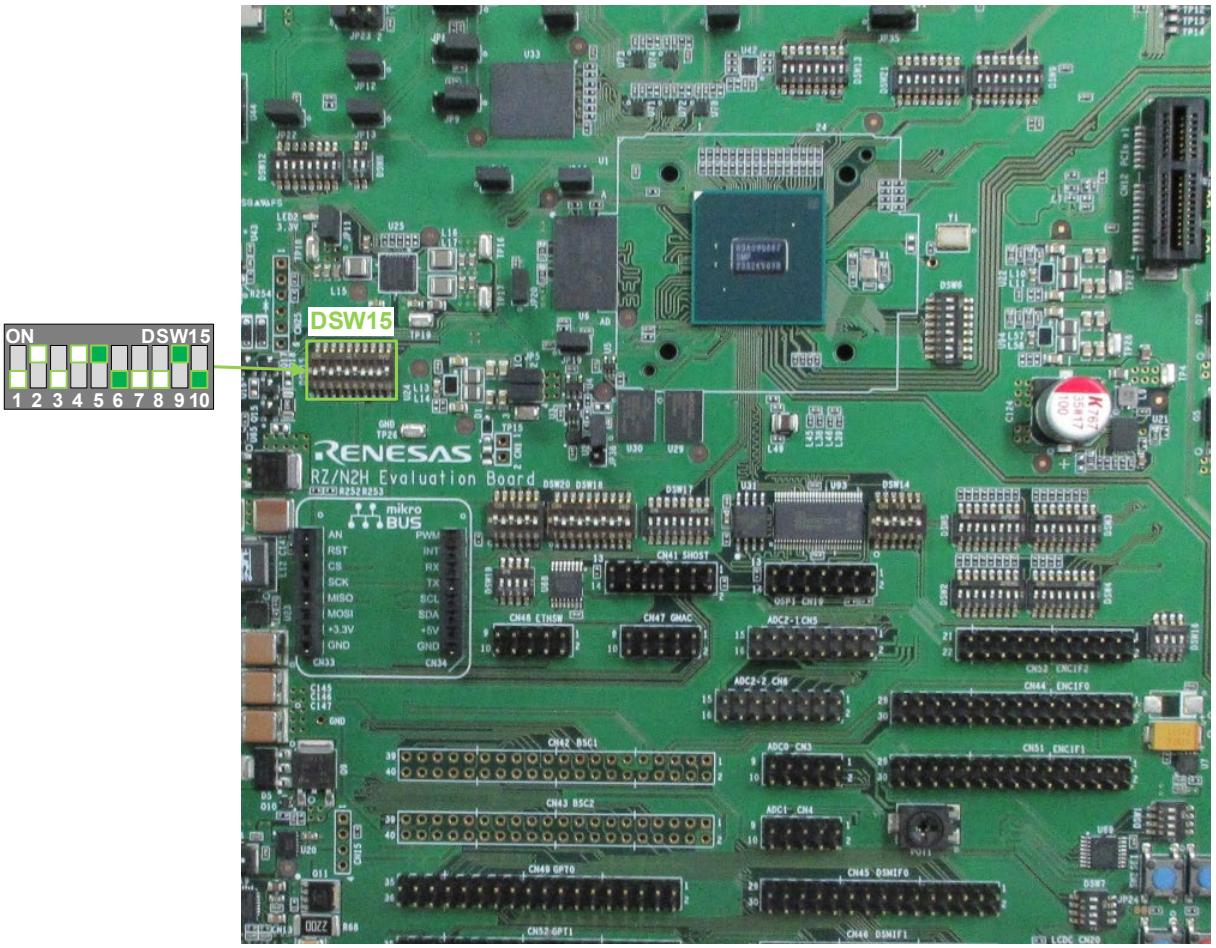
Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P01_1_V1833_5_XSPI1_CS0#	CS0#	P01_1	AG12	**DSW2-6: ON**
P01_0_V1833_5_XSPI1_CKP	CKP	P01_0*	AF13	
P01_7_V1833_5_XSPI1_IO3	Data 3	P01_7*	AC13	
P01_6_V1833_5_XSPI1_IO2	Data 2	P01_6*	AD13	
P01_5_V1833_5_XSPI1_IO1	Data 1	P01_5*	AE13	
P01_4_V1833_5_XSPI1_IO0	Data 0	P01_4*	AG13	

Note: Connected via the bus switch IC.

Table 7-16 Signal Connections of EEPROM

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P14_6_I2C_SCL0_ESC_I2CCLK	I2C CLK	P14_6*	A10	**DSW15-8: OFF,** DSW15-9: ON, DSW15-10: OFF
P14_7_I2C_SDA0_ESC_I2CDATA	I2C DATA	P14_7*	A9	DSW15-5: ON, DSW15-6: OFF

Note: Connected via the DIP switch.



□ : Initial setting
■ : Changed from the initial setting

Figure 7-15 Switch Settings When Using EEPROM

Table 7-17 Signal Connections of SPI Expansion Connector (CN19)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	GROUND	—	—	—
2	P18_0_HEADER_BSC_A8_LCDC_DATB1_XSPI1_IRQ7	P18_0	F12	—
3	P01_0_V1833_5_XSPI1_CKP	P01_0*1	W11	**DSW2-6: ON**
4	P01_2_V1833_5_XSPI1_CS1#	P01_2*1	Y12	
5	P02_3_V1833_5_XSPI1_IO7	P02_3*1	Y10	
6	P02_2_V1833_5_XSPI1_IO6	P02_2*1	AA11	
7	P02_1_V1833_5_XSPI1_IO5	P02_1*1	AA10	
8	P02_0_V1833_5_XSPI1_IO4	P02_0*1	AA12	
9	P01_7_V1833_5_XSPI1_IO3	P01_7*1	AB12	
10	P01_6_V1833_5_XSPI1_IO2	P01_6*1	AD11	
11	P01_5_V1833_5_XSPI1_IO1	P01_5*1	AC11	
12	P01_4_V1833_5_XSPI1_IO0	P01_4*1	AD12	
13	P03_3_HEADER_BSC_D11_XSPI1_IRQ13	P03_3*2	AA9	DSW7-1: OFF, DSW7-2: ON
14	p3v3	—	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via the DIP switch.

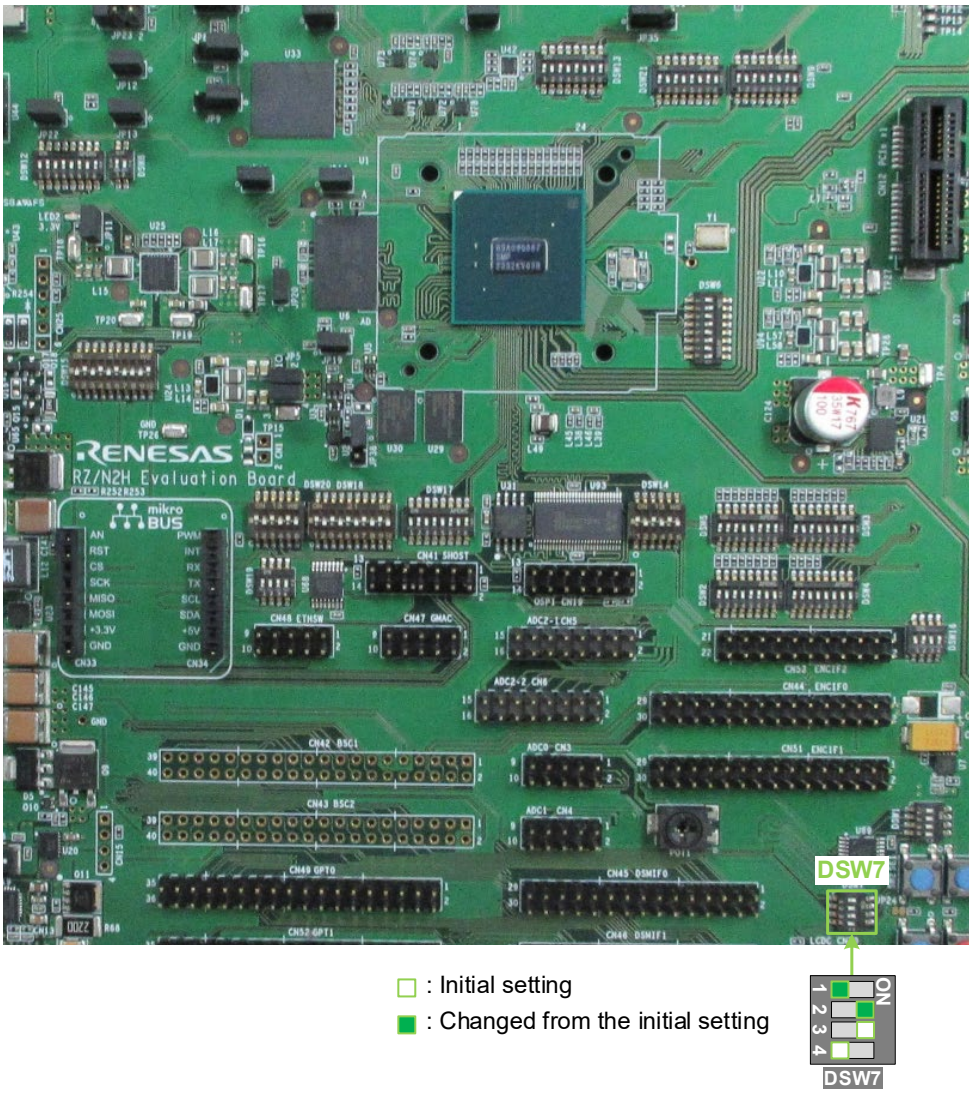


Figure 7-16 Switch Settings When Using SPI Memory

7.12 LPDDR4

This board has LPDDR4. Figure 7-17 shows the signal connections for LPDDR4.

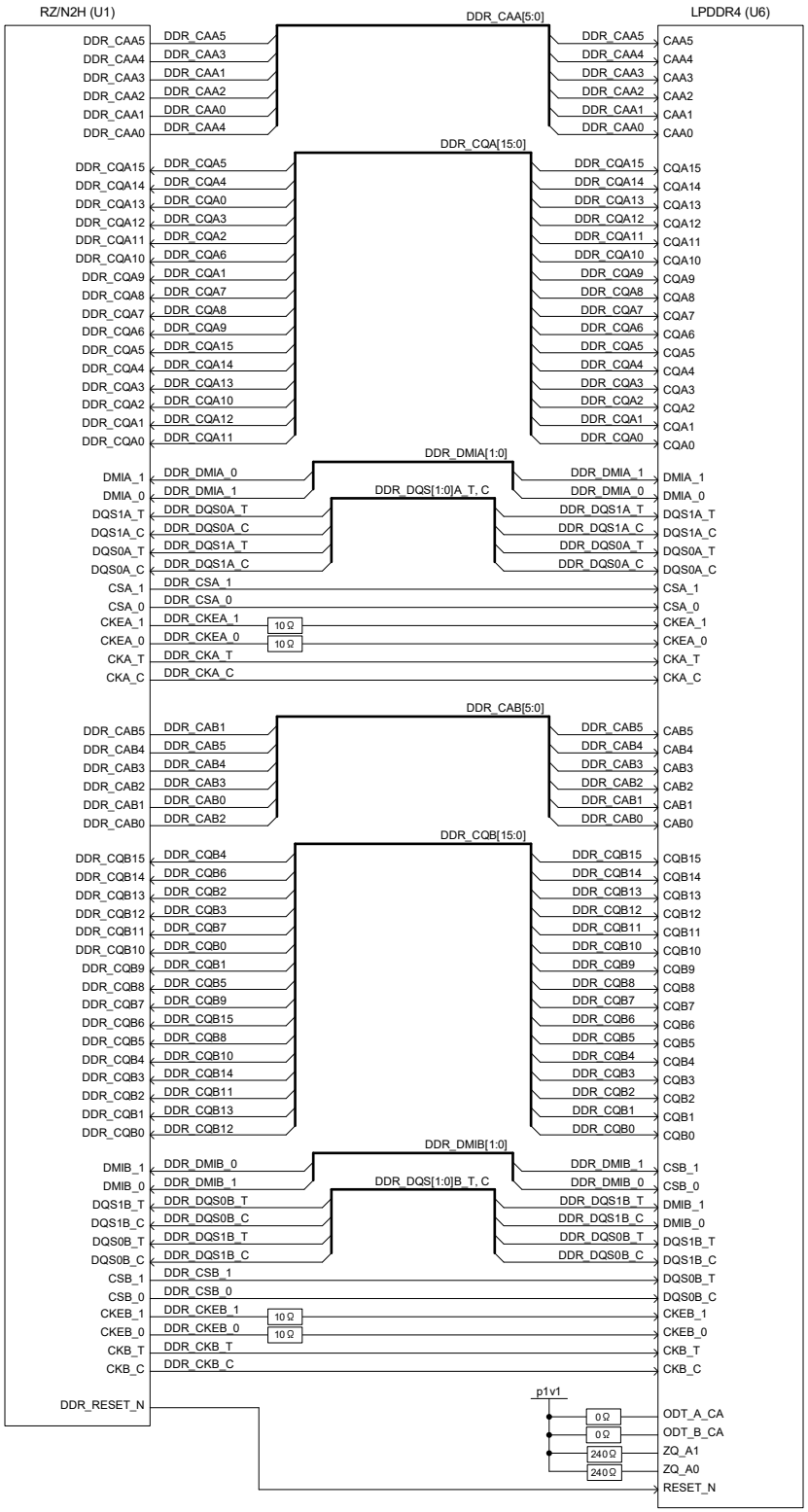


Figure 7-17 Signal Connections for LPDDR4

7.13 SD and eMMC

This board is equipped with an SD card slot (CN21), a MicroSD card slot (CN22), and eMMC (U33). Figure 7-18 shows the configuration of the SD and eMMC, and Table 7-18, Table 7-19 and Table 7-20 list the signal connections. Figure 7-19 shows the switch settings when using the SD card slot (CN21).

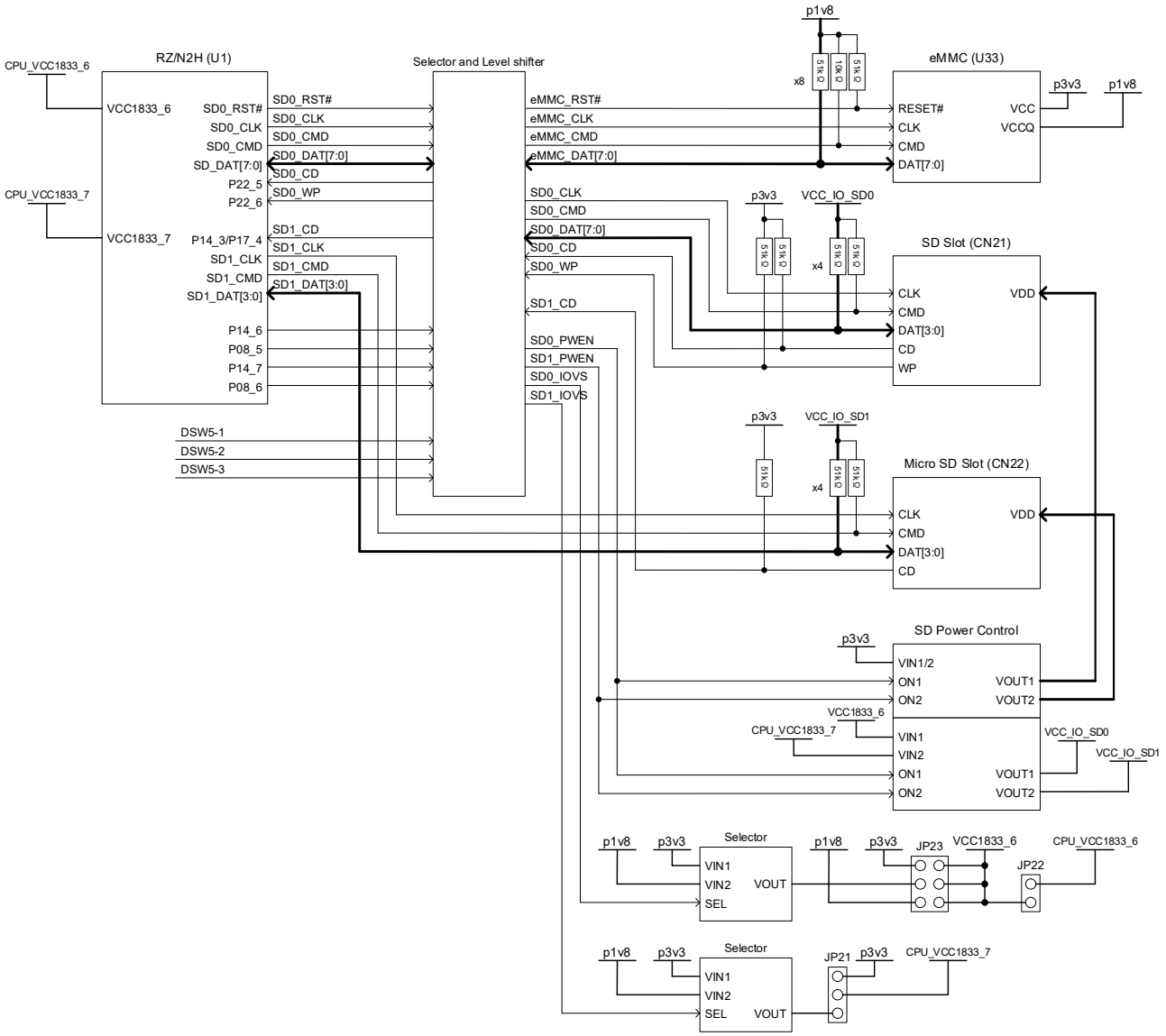


Figure 7-18 Configuration of SD, eMMC Circuits

Table 7-18 Signal Connections of eMMC

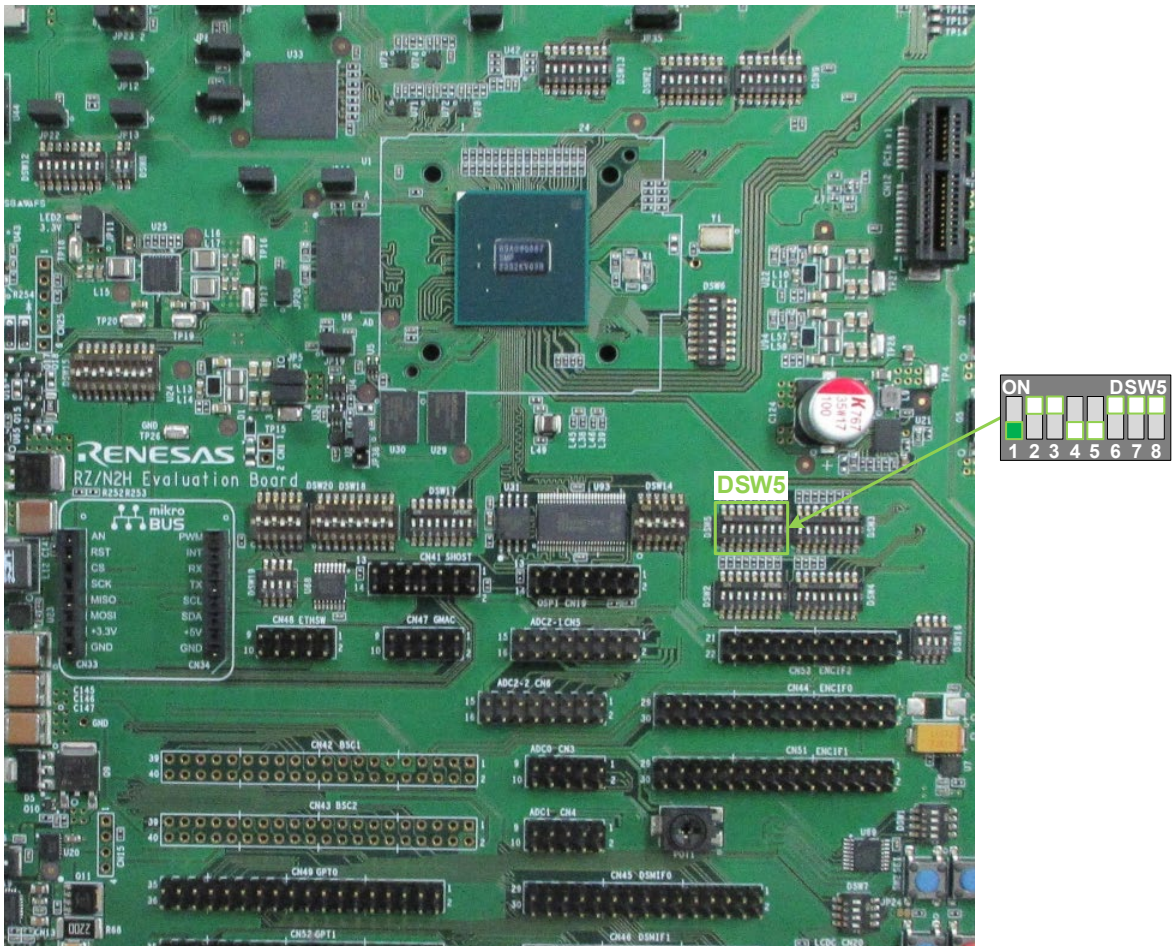
Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P13_2_P1V8_eMMC_RST#	Reset	P13_2 *	F8	**DSW5-1: ON, DSW5-2: ON**
P12_1_P1V8_eMMC_CMD	Command	P12_1 *	E7	
P12_0_P1V8_eMMC_CLK	Clock	P12_0 *	C8	
P12_2_P1V8_eMMC_DAT0	Data 0	P12_2 *	E8	
P12_3_P1V8_eMMC_DAT1	Data 1	P12_3 *	F7	
P12_4_P1V8_eMMC_DAT2	Data 2	P12_4 *	B8	
P12_5_P1V8_eMMC_DAT3	Data 3	P12_5 *	D7	
P12_6_P1V8_eMMC_DAT4	Data 4	P12_6 *	D6	
P12_7_P1V8_eMMC_DAT5	Data 5	P12_7 *	B6	
P13_0_P1V8_eMMC_DAT6	Data 6	P13_0 *	B7	
P13_1_P1V8_eMMC_DAT7	Data 7	P13_1 *	C6	

Note: Connected via the level shifter IC with an enable function.

Table 7-19 Signal Connections of SD Card Slot

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P12_1_VCC1833_6_SD0_CMD	Command	P12_1*1	E7	DSW5-1: OFF, **DSW5-2: ON**
P12_0_VCC1833_6_SD0_CLK	Clock	P12_0*1	C8	
P12_2_VCC1833_6_SD0_DAT0	Data 0	P12_2*1	E8	
P12_3_VCC1833_6_SD0_DAT1	Data 1	P12_3*1	F7	
P12_4_VCC1833_6_SD0_DAT2	Data 2	P12_4*1	B8	
P12_5_VCC1833_6_SD0_DAT3	Data 3	P12_5*1	D7	
P22_5_SD0_CD	Card Detection	P22_5*2	B18	**DSW15-3: OFF, DSW15-4: ON**
P22_6_SD0_WP	Write Protection	P22_6*2	C18	**DSW15-1: OFF, DSW15-2: ON**
P02_5_SD0_PWEN	Power supply control	P02_5*2	AD10	**DSW17-7: OFF, DSW17-8: ON**
P02_6_SD0_IOVS	IO voltage selection of SD0	P02_6*2	AB10	**DSW17-5: OFF, DSW17-6: ON**

Notes: 1. Connected via the level shifter IC with an enable function.
2. Connected via the DIP switch.



□ : Initial setting
■ : Changed from the initial setting

Figure 7-19 Switch Settings When Using the SD Card Slot (CN21)

Table 7-20 Signal Connections of MicroSD Card Slot

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P16_6_VDD1833_7_SD1_CMD	Command	P16_6	E11	—
P16_5_VDD1833_7_SD1_CLK	Clock	P16_5	E10	—
P16_7_VDD1833_7_SD1_DATA0	Data 0	P16_7	D10	—
P17_0_VDD1833_7_SD1_DATA1	Data 1	P17_0	C11	—
P17_1_VDD1833_7_SD1_DATA2	Data 2	P17_1	A11	—
P17_2_VDD1833_7_SD1_DATA3	Data 3	P17_2	B11	—
P14_3_P17_4_SD1_CD	Card Detection	P14_3*3	C10	DSW19-1: ON, DSW19-2: OFF, DSW19-3: ON, DSW19-4: OFF
		P17_4*1	E13	**DSW5-3: ON, DSW19-1: OFF, DSW19-2: ON**
P08_5_SD1_PWEN	Power supply control	P08_5	AC2	—
P08_6_SD1_IOVS	IO voltage selection of SD1	P08_6*2	AD2	**DSW5-3: ON**

Notes: 1. Connected via the bus switch IC and DIP switch.
2. Connected via the bus switch IC.
3. Connected via the DIP switch.

7.14 CAN

This board is equipped with a CAN transceiver (U43) and a CAN interface connector (CN35) so that the CAN module of the RZ/N2H can be evaluated. Figure 7-20 shows the configuration of the CAN interface circuit, and Table 7-21 lists the signal connections.

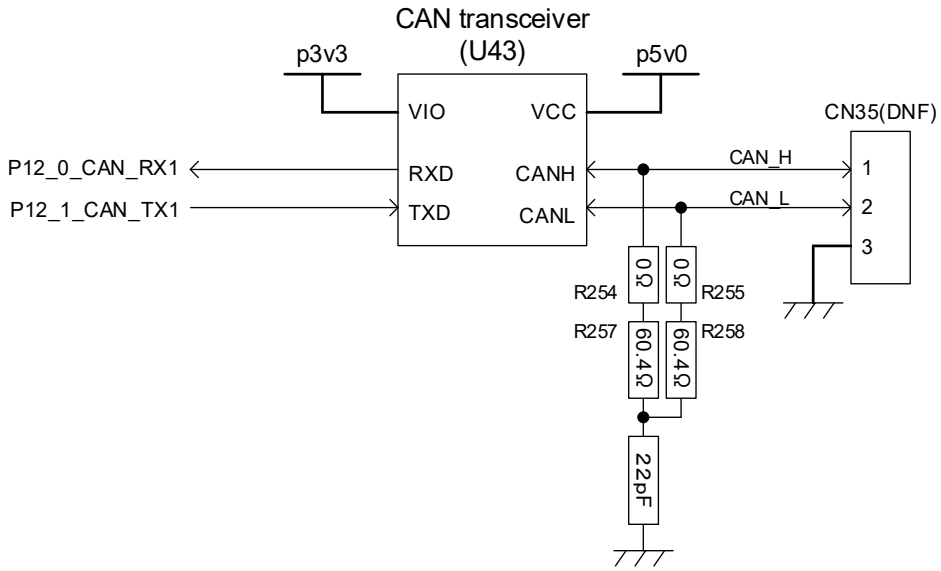
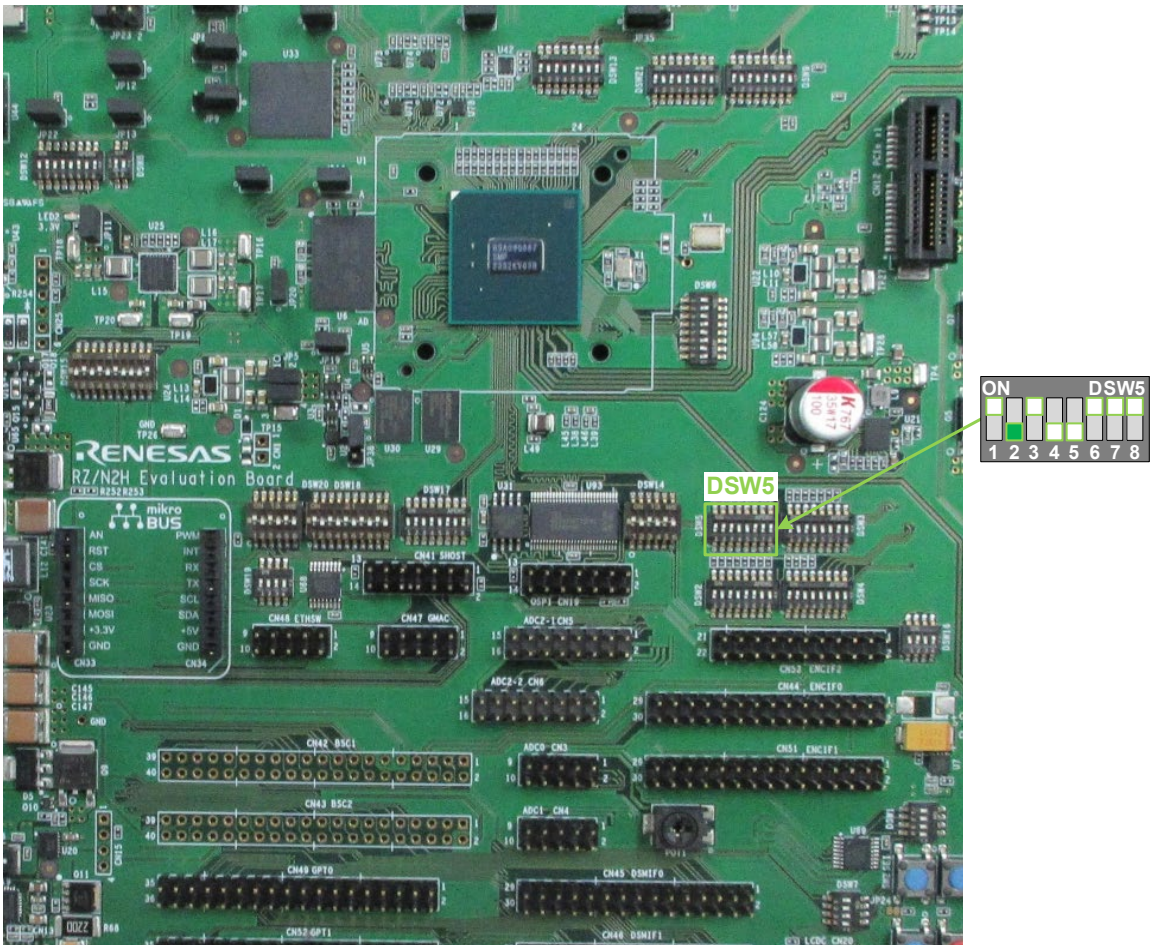


Figure 7-20 Configuration of CAN Interface Circuit

Table 7-21 Signal Connections of CAN

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P12_0_CAN_RX1	Reception of CAN data	P12_0*	C8	**DSW5-1: ON,** DSW5-2: OFF
P12_1_CAN_TX1	Transmission of CAN data	P12_1*	E7	

Note: Connected via the level shifter IC with an enable function.



□ : Initial setting
■ : Changed from the initial setting

Figure 7-21 Switch Settings When Using CAN Interface Circuit

7.15 RS485 Interface

This board is equipped with an RS485 transceiver (U47), an RS485 interface connector (CN36). Figure 7-22 shows the configuration of the RS485 interface circuit, Table 7-22 lists the signal connections of the connector, and Table 7-23 lists the ports to be used.

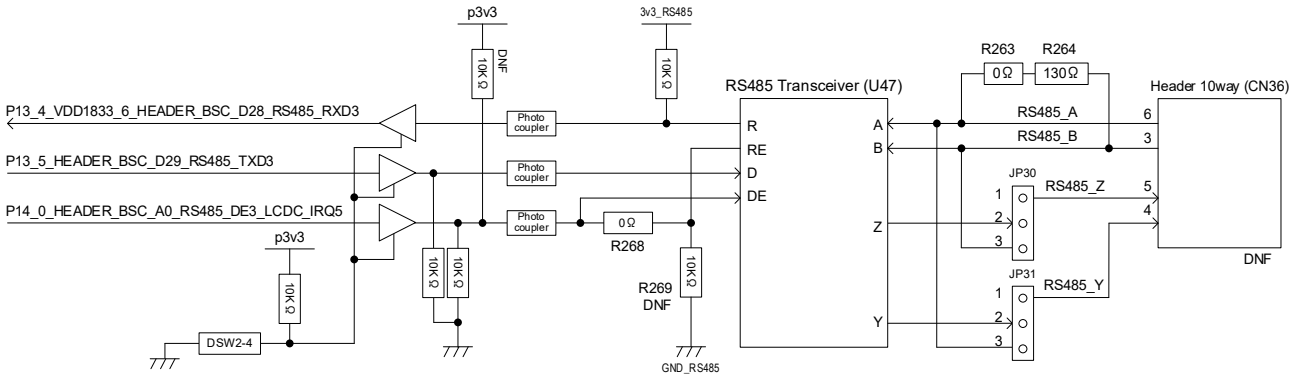


Figure 7-22 Configuration of RS485 Interface Circuit

Table 7-22 Signal Connections of RS485 Interface Connector (CN36)

Pin	Signal Name	Pin	Signal Name
1	GND_RS485	2	GND_RS485
3	RS485_B	4	RS485_Y
5	RS485_Z	6	RS485_A
7	GND_RS485	8	GND_RS485
9	GND_RS485	10	GND_RS485

Table 7-23 Ports Used with the RS485 Interface

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P13_4_VDD1833_6_HEADER_BSC_D28_RS485_RXD3	Reception data	P13_4*1	A6	**DSW2-4: OFF**
P14_0_HEADER_BSC_A0_RS485_DE3_LCDC_IRQ5	Driver enable	P14_0	A8	—
P13_5_HEADER_BSC_D29_RS485_TXD3	Transmission data	P13_5*2	C7	**DSW2-4: OFF**

Notes: 1. Connected via the buffer IC.
2. Connected via the buffer IC and level shifter IC.

7.16 USB

This board is equipped with a USB type-A connector (CN7) and a mini-B connector (CN8). The USB function of the RZ/N2H can be used as either a USB host interface or a USB function interface (both cannot be used at the same time). The USB micro-AB connector (CN9) cannot be used.

Figure 7-23 shows the configuration of the USB circuit, Table 7-24 lists the signal connections. Figure 7-24 and Figure 7-25 show the configuration of the USB circuit.

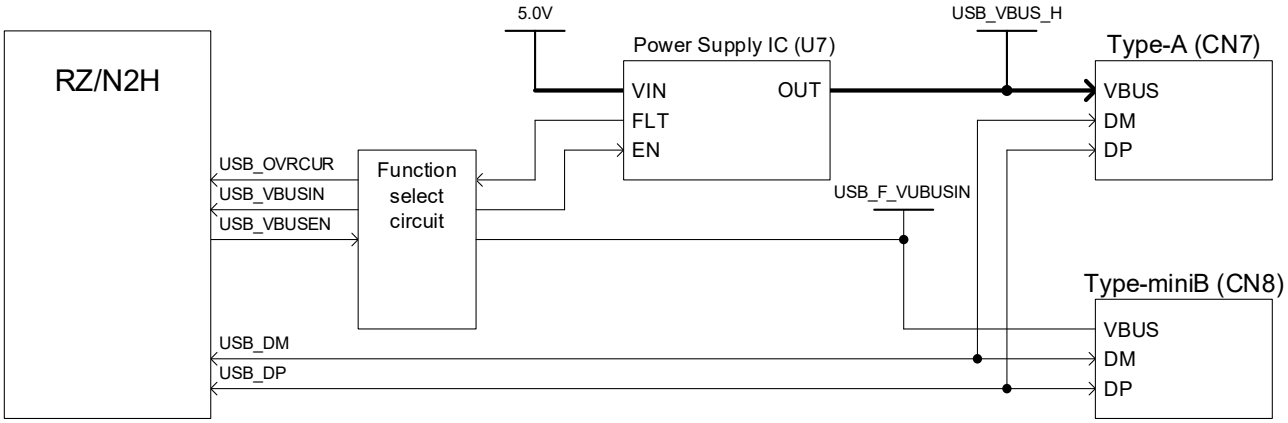
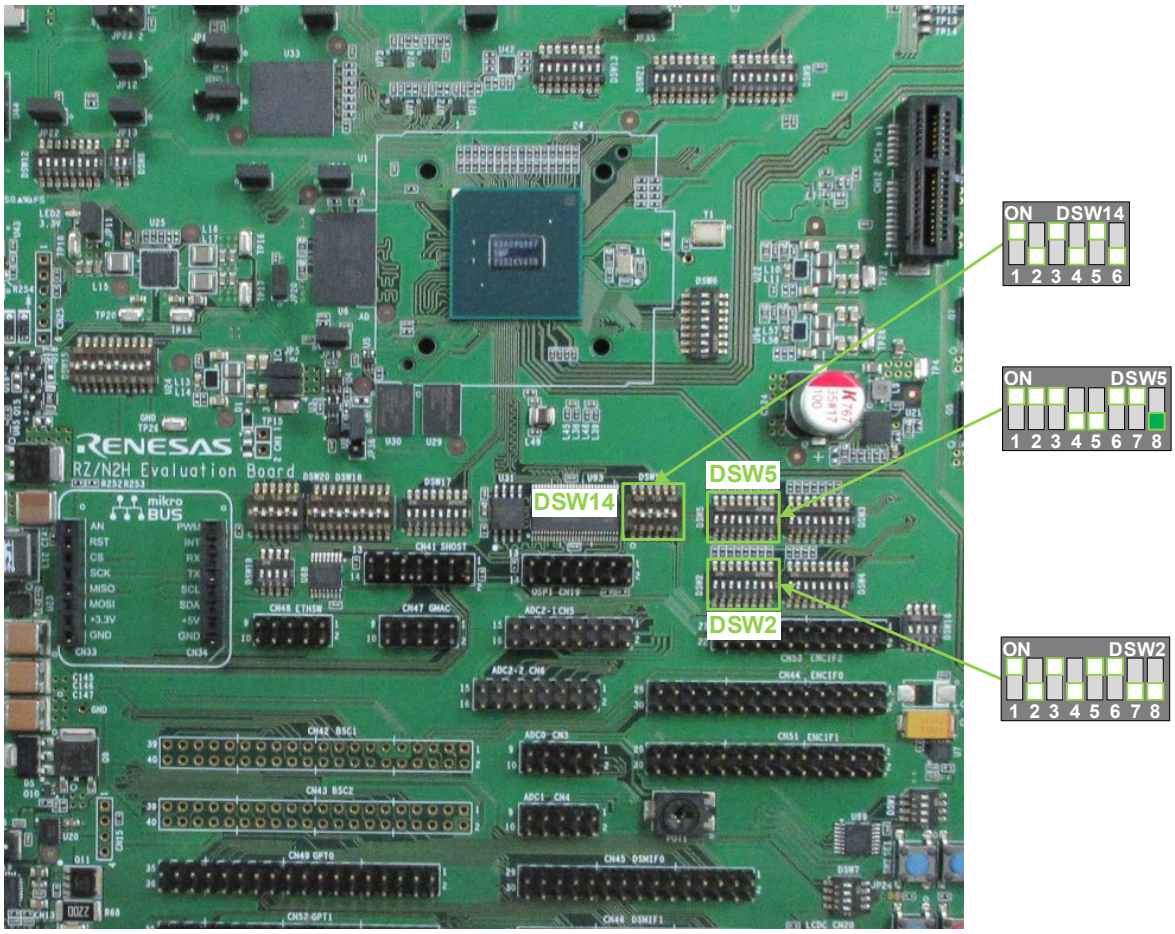


Figure 7-23 Configuration of USB Circuit

Table 7-24 Signal Connections of USB

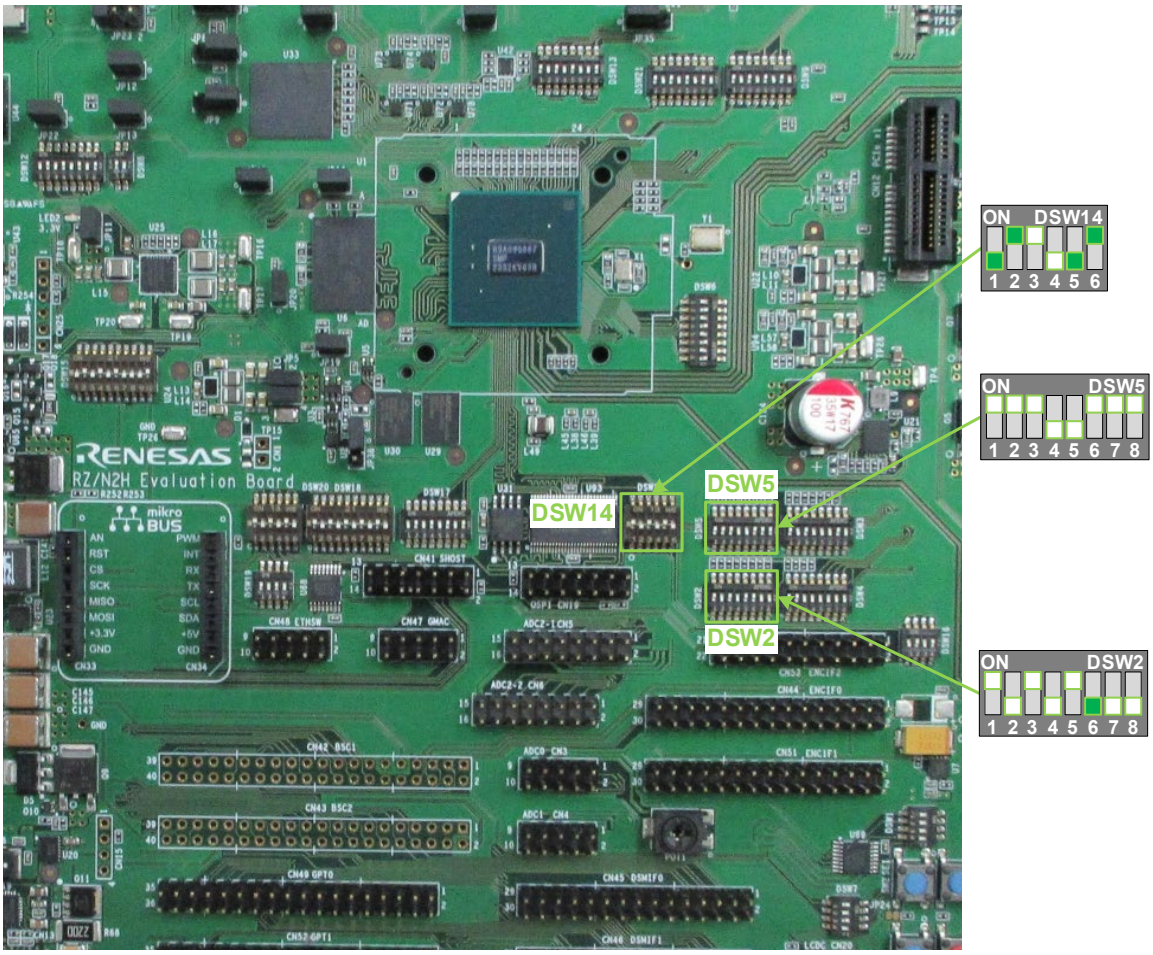
Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
USB_DP	Input/output of D+ data	USB_QDP	AC14	—
USB_DM	Input/output of D- data	USB_QDM	AD14	—
VUBUSIN	VBUS detection	USB_VUBUSIN	Y14	**DSW16-1: OFF, DSW16-2: ON**
USB_HF_VBUSEN	VBUS enable signal	P00_0*1	AB13	DSW5-8: OFF, **DSW2-5: ON, DSW14-5: ON, DSW14-6: OFF, DSW16-3: OFF, DSW16-4: ON**
		P02_2*1	AA11	DSW2-6: OFF, DSW14-5: OFF, DSW14-6: ON, **DSW16-3: OFF, DSW16-4: ON**
P00_1_P02_3_V1833_5_USB_OVRCUR	Overcurrent	P00_1*2	AA13	DSW5-8: OFF, **DSW2-5: ON, DSW14-1: ON, DSW14-2: OFF**
		P02_3*2	Y10	DSW2-6: OFF, DSW14-1: OFF, DSW14-2: ON

Notes: 1. Connected via the bus switch IC.
2. Connected via the bus switch IC and DIP switch.



□ : Initial setting
■ : Changed from the initial setting

Figure 7-24 Switch Settings When Using USB Circuit (Port 00)



□ : Initial setting
■ : Changed from the initial setting

Figure 7-25 Switch Settings When Using USB Circuit (Port 02)

7.17 Ethernet System

When running any Ethernet software, do so with the use of a unique MAC address. A sticker indicating the unique MAC address that was assigned by Renesas is affixed to this board (top side) to ensure full compatibility in the case of connection to other Renesas hardware modules.

An EtherCAT ID number is required to execute the EtherCAT slave controller software. Please use DSW1 as required.

This board is equipped with four Ethernet PHY devices and Ethernet connectors (CN37, CN38, CN39, and CN40) so that the Ethernet system of the RZ/N2H can be evaluated. Figure 7-26 shows the configuration of the Ethernet system circuits. Table 7-25 to Table 7-28 list the signal connections. Table 7-29 shows initial settings by hardware strapping of the PHY devices.

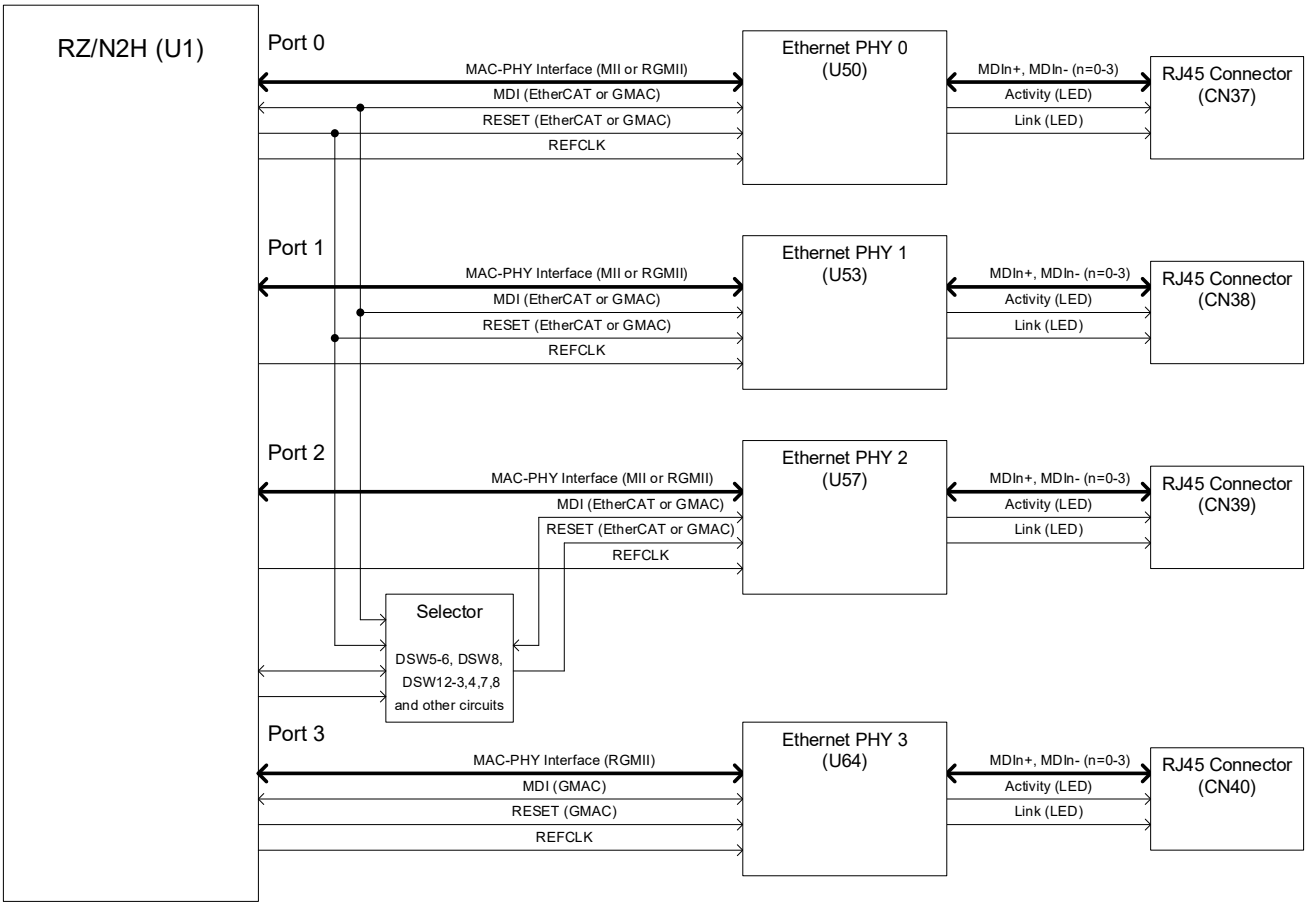


Figure 7-26 Configuration of Ethernet System Circuits

Table 7-25 Signal Connections of Ethernet Port 0 (ETH0)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P20_0_VDD1833_0_ETH0_TXCLK	Transmit clock	P20_0	B14	—
P20_1_VDD1833_0_ETH0_TXD0_MDV	Transmit data 0	P20_1	A15	—
P20_2_VDD1833_0_ETH0_TXD1	Transmit data 1	P20_2	F14	—
P20_3_VDD1833_0_ETH0_TXD2	Transmit data 2	P20_3	E14	—
P20_4_VDD1833_0_ETH0_TXD3	Transmit data 3	P20_4	B16	—
P20_5_VDD1833_0_ETH0_TXEN	Transmit data enable / error	P20_5	A14	—
P22_1_ETH0_TXER	Transmit data error	P22_1	C17	—
P20_6_VDD1833_0_ETH0_RXCLK	Receive clock	P20_6	D16	—
P20_7_VDD1833_0_ETH0_RXD0	Receive data 0	P20_7	D15	—
P21_0_VDD1833_0_ETH0_RXD1	Receive data 1	P21_0	E15	—
P21_1_VDD1833_0_ETH0_RXD2	Receive data 2	P21_1	C16	—
P21_2_VDD1833_0_ETH0_RXD3	Receive data 3	P21_2	A16	—
P21_3_VDD1833_0_ETH0_RXDV	Receive data valid / error / carrier sense	P21_3	A17	—
P22_2_ETH0_RXER	Receive data error	P22_2	B17	—
P22_3_ETH0_CRS	Carrier sense	P22_3	E17	—
P22_4_ETH0_COL	Collision detection	P22_4	A18	—
P21_4_VDD1833_0_ETH0_GMAC0_MDC	MDI Clock	P21_4	E16	—
P21_5_VDD1833_0_ETH0_GMAC0_MDIO	MDI Data	P21_5	D14	—
P22_0_VDD1833_0_PHY0_IRQ11	MDI interrupt input	P22_0	F16	—
P21_6_VDD1833_0_ETHSW_PHYLINK0	Link status	P21_6	C14	—
P21_7_VDD1833_0_ETH0_REFCLK	Clock output (25 MHz)	P21_7	C15	—
P11_0_ESC_RESETOUT#	Reset output	P11_0*	A5	**DSW12-3: OFF, DSW12-4: ON**

Note: Connected via the DIP switch.

Table 7-26 Signal Connections of Ethernet Port 1 (ETH1)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P24_5_VDD1833_1_ETH1_TXCLK	Transmit clock	P24_5	A19	—
P24_6_VDD1833_1_ETH1_TXD0_MD0	Transmit data 0	P24_6	A22	—
P24_7_VDD1833_1_ETH1_TXD1_MD1	Transmit data 1	P24_7	B21	—
P25_0_VDD1833_1_ETH1_TXD2_MD2	Transmit data 2	P25_0	A20	—
P25_1_VDD1833_1_ETH1_TXD3_MDW0	Transmit data 3	P25_1	B20	—
P25_2_VDD1833_1_ETH1_TXEN_MDW1	Transmit data enable / error	P25_2	A21	—
P26_6_ETH1_TXER	Transmit data error	P26_6*	C22	**DSW21-1: ON, DSW21-2: OFF, DSW21-3: ON**
P25_3_VDD1833_1_ETH1_RXCLK	Receive clock	P25_3	C21	—
P25_4_VDD1833_1_ETH1_RXD0	Receive data 0	P25_4	E19	—
P25_5_VDD1833_1_ETH1_RXD1	Receive data 1	P25_5	D20	—
P25_6_VDD1833_1_ETH1_RXD2	Receive data 2	P25_6	C19	—
P25_7_VDD1833_1_ETH1_RXD3	Receive data 3	P25_7	E20	—
P26_0_VDD1833_1_ETH1_RXDV	Receive data valid / error / carrier sense	P26_0	F18	—
P26_7_ETH1_RXER	Receive data error	P26_7*	E22	**DSW13-1: ON, DSW13-2: OFF**
P27_0_ETH1_CRS	Carrier sense	P27_0*	D22	**DSW13-3: ON, DSW13-4: OFF**
P27_1_ETH1_COL	Collision detection	P27_1*	B23	**DSW13-5: ON, DSW13-6: OFF**
P21_4_VDD1833_0_ETH0_GMAC0_MDC	MDI Clock	P21_4	E16	—
P21_5_VDD1833_0_ETH0_GMAC0_MDIO	MDI Data	P21_5	D14	—
P26_5_VDD1833_1_PHY1_IRQ12	MDI interrupt input	P26_5	B22	—
P26_3_VDD1833_1_ETHSW_PHYLINK1	Link status	P26_3	D19	—
P26_4_VDD1833_1_ETH1_REFCLK	Clock output (25 MHz)	P26_4	E21	—
P11_0_ESC_RESETOUT#	Reset output	P11_0*	A5	**DSW12-3: OFF, DSW12-4: ON**

Note: Connected via the DIP switch.

Table 7-27 Signal Connections of Ethernet Port2 (ETH2)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P29_1_VDD1833_2_ETH2_TXCLK	Transmit clock	P29_1*1	E23	**DSW5-7: ON**
P29_2_VDD1833_2_ETH2_TXD0	Transmit data 0	P29_2*1	H20	
P29_3_VDD1833_2_ETH2_TXD1	Transmit data 1	P29_3*1	G22	
P29_4_VDD1833_2_ETH2_TXD2	Transmit data 2	P29_4*1	F22	
P29_5_VDD1833_2_ETH2_TXD3	Transmit data 3	P29_5*1	G21	
P29_6_VDD1833_2_ETH2_TXEN	Transmit data enable / error	P29_6*1	F21	
P31_2_ETH2_TXER	Transmit data error	P31_2*1	J24	
P29_7_VDD1833_2_ETH2_RXCLK	Receive clock	P29_7*1	H22	
P30_0_VDD1833_2_ETH2_RXD0	Receive data 0	P30_0*1	F20	
P30_1_VDD1833_2_ETH2_RXD1	Receive data 1	P30_1*1	G23	
P30_2_VDD1833_2_ETH2_RXD2	Receive data 2	P30_2*1	E24	
P30_3_VDD1833_2_ETH2_RXD3	Receive data 3	P30_3*1	H23	
P30_4_VDD1833_2_ETH2_RXDV	Receive data valid / error / carrier sense	P30_4*1	D24	
P31_1_VDD1833_2_ETH2_RXER	Receive data error	P31_1	G24	—
P31_4_ETH2_CRS	Carrier sense	P31_4*1	J21	**DSW5-7: ON**
P31_5_ETH2_COL	Collision detection	P31_5*1	J23	
ETH2_MDC	MDI Clock	P21_4*2	E16	**DSW5-6: ON**
		P30_5*2	G20	DSW5-6: OFF
ETH2_MDIO	MDI Data	P21_5*2	D14	**DSW5-6: ON**
		P30_6*2	H24	DSW5-6: OFF
P13_7_VDD1833_6_PHY2_IRQ14	MDI interrupt input	P13_7*3	A7	**DSW13-7: OFF, DSW13-8: ON**
P30_7_VDD1833_2_ETHSW_PHYLINK2	Link status	P30_7*1	F24	**DSW5-7: ON**
P31_0_VDD1833_2_ETH2_REFCLK	Clock output (25 MHz)	P31_0	G19	—
P11_0_ESC_RESETOUT#_P03_1_GMAC_RESETOUT2#	Reset output	P11_0*3	A5	**DSW12-3: OFF, DSW12-4: ON**, DSW8-1: OFF, DSW8-2: ON
		P03_1*3	Y9	**DSW12-7: OFF, DSW12-8: ON, DSW8-1: ON, DSW8-2: OFF**

Notes: 1. Connected via the bus switch IC.
2. Connected via the level shifter IC with an enable function.
3. Connected via the DIP switch.

Table 7-28 Signal Connections of Ethernet Port3 (ETH3)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P33_2_VDD1833_3_ETH3_TXCLK	Transmit clock	P33_2*1	L20	DSW5-8: ON
P33_3_VDD1833_3_ETH3_TXD0	Transmit data 0	P33_3*1	M20	
P33_4_VDD1833_3_ETH3_TXD1	Transmit data 1	P33_4*1	N20	
P33_5_VDD1833_3_ETH3_TXD2	Transmit data 2	P33_5*1	N21	
P33_6_VDD1833_3_ETH3_TXD3	Transmit data 3	P33_6*1	M21	
P33_7_VDD1833_3_ETH3_TXEN	Transmit data enable / error	P33_7*1	L23	
P00_0_ETH3_TXER	Transmit data error	P00_0*1	AB13	
P34_0_VDD1833_3_ETH3_RXCLK	Receive clock	P34_0*1	L22	
P34_1_VDD1833_3_ETH3_RXD0	Receive data 0	P34_1*1	K20	
P34_2_VDD1833_3_ETH3_RXD1	Receive data 1	P34_2*1	K22	
P34_3_VDD1833_3_ETH3_RXD2	Receive data 2	P34_3*1	L21	
P34_4_VDD1833_3_ETH3_RXD3	Receive data 3	P34_4*1	K23	
P34_5_VDD1833_3_ETH3_RXDV	Receive data valid / error / carrier sense	P34_5*1	K21	
P00_1_ETH3_RXER	Receive data error	P00_1*1	AA13	
P00_2_ETH3_CRS	Carrier sense	P00_2*1	W12	
P00_3_ETH3_COL	Collision detection	P00_3*2	AD13	DSW12-1: OFF, DSW12-2: ON
P26_1_VDD1833_1_GMAC1_MDC	MDI Clock	P26_1	E18	—
P26_2_VDD1833_1_GMAC1_MDIO	MDI Data	P26_2	C20	—
P17_3_VDD1833_7_PHY3_IRQ15	MDI interrupt input	P17_3	D11	—
P34_6_VDD1833_3_ETH3_REFCLK	Clock output (25 MHz)	P34_6*1	K24	DSW5-8: ON
P03_2_GMAC_RESETOUT3#	Reset output	P03_2*2	AB9	DSW12-5: OFF, DSW12-6: ON

Notes: 1. Connected via the bus switch IC.
2. Connected via the DIP switch.

Table 7-29 Initial Settings by Hardware Strapping of the PHY Devices

Items of PHY Initial Settings	Contents of PHY Initial Settings
CLKOUT	Disabled
Managed or unmanaged	Unmanaged mode
CLK delay	2.0 ns
Link advertisement	Default mode of operation, 10/100/1000 FDX/HDX, auto-nego is ON
MAC interface	RGMII mode
Selection of GMII/MII or RGMII/RMII	PHY0(U50), PHY1(U53): GMII or MII mode (when R281 or R304 is Fit) PHY2(U57), PHY3(U64): RGMII mode (when R326 or R349 is DNF)
PHY address	PHY0 (U50): 0 PHY1 (U53): 1 PHY2 (U57): 2 PHY3 (U64): 3
Enabling of forced 1000-BT mode	Not set

On the board as shipped, Ethernet ports 0 and 1 are set to the 3.3-V/MII mode (JP6, JP7: 2-3 are short-circuit. R281, R304: Fit.) and Ethernet ports 2 and 3 are set to the 1.8-V/RGMII mode (JP8, JP9: 1-2 are short-circuit. R326, R349: DNF.). When switching the MII and RGMII modes, change the settings with reference to Table 6-20 and Table 6-26.

7.18 PCIe

This board is equipped with a clock driver, power-supply IC, and connectors (CN11 and CN12) for the PCIe so that the PCIe function of the RZ/N2H can be evaluated. Figure 7-27 shows the configuration of the PCIe circuit.

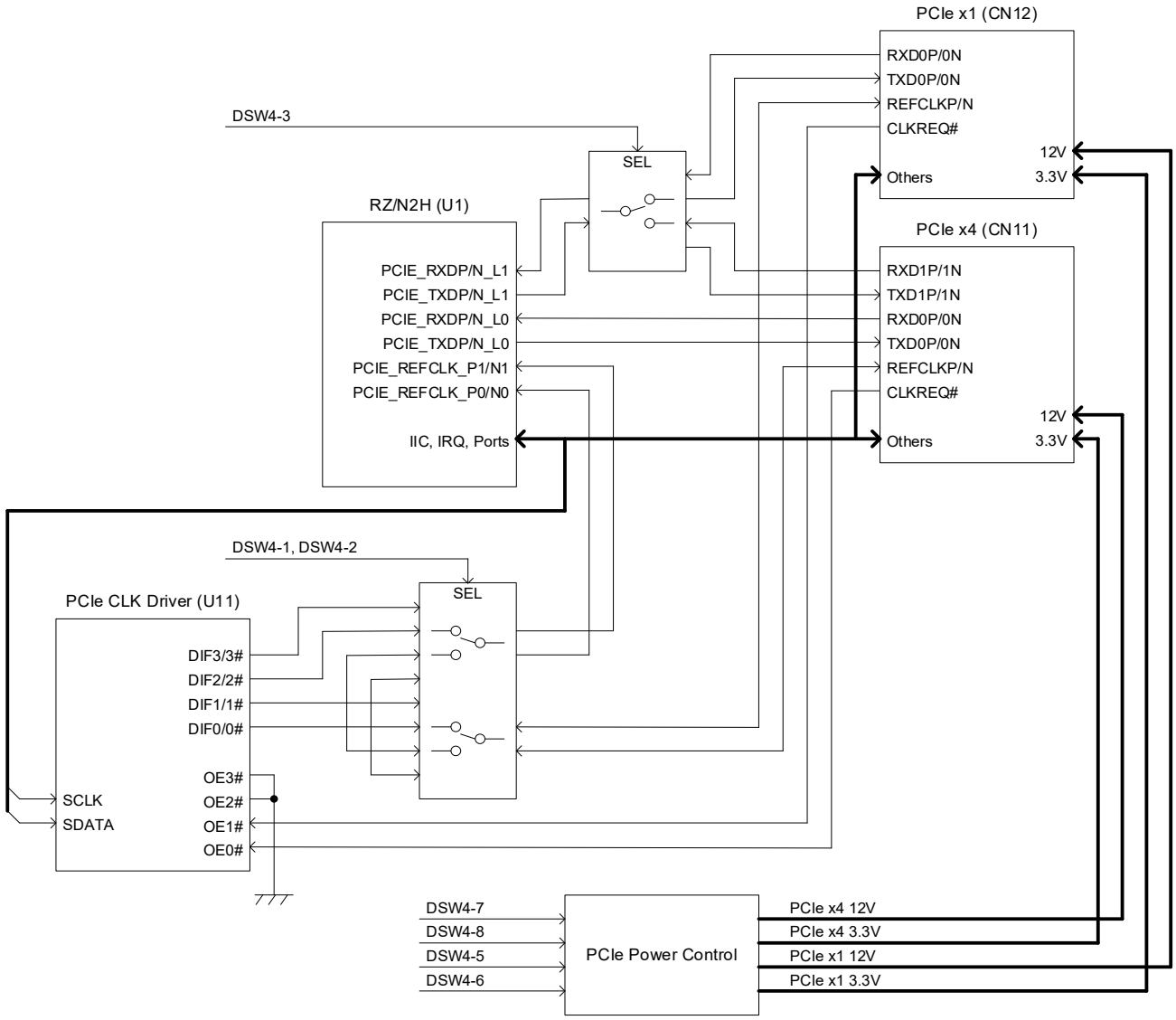


Figure 7-27 Configuration of PCIe Circuit

The configurations of root complex or endpoint, and 2 lanes × 1 port or 1 lane × 2 ports can be selected by setting DSW4-1 to DSW4-3. In addition, the supply of power to each connector can be controlled by setting DSW4-5 to DSW4-8. However, since the connection of data signals to the connector is the same for an endpoint setting as for a root complex setting, a crossover cable should be used when performing evaluation. Table 7-30 and Figure 7-28 show the PCIe configurations and associated switch settings.

Table 7-30 PCIe Configurations and Associated Switch Settings (Excluding Signal Function Selection Switches)

Configuration No.	Description of Configuration	Settings of Switches
Configuration 1	Root complex and 2 lane x 1 port (CN11)	**DSW4-1: ON, DSW4-2: ON, DSW4-3: OFF, DSW4-5, 6: OFF**, DSW4-7, 8: ON
Configuration 2	Root complex and 1 lane x 2 port	**DSW4-1: ON, DSW4-2: ON**, DSW4-3: ON, DSW4-5 to 8: ON
Configuration 3	Endpoint and 2 lane x 1 port (CN11)	DSW4-1: OFF, DSW4-2: OFF, **DSW4-3: OFF, DSW4-5 to 8: OFF**
Configuration 4	Endpoint and 1 lane x 2 port	DSW4-1: OFF, DSW4-2: OFF, DSW4-3: ON, **DSW4-5 to 8: OFF**
Configuration 5	Root complex and 1 lane x 1 port (CN11), Endpoint and 1 lane x 1 port (CN12)	**DSW4-1: ON**, DSW4-2: OFF, DSW4-3: ON, **DSW4-5, 6: OFF**, DSW4-7, 8: ON
Configuration 6	Root complex and 1 lane x 1 port (CN12), Endpoint and 1 lane x 1 port (CN11)	DSW4-1: OFF, **DSW4-2: ON**, DSW4-3: ON, DSW4-5, 6: ON, **DSW4-7, 8: OFF**

Table 7-31 and Table 7-32 list the signal connections of the PCIe x4 connector (CN11) and PCIe x1 connector (CN12), respectively.

Table 7-31 Signal Connections of PCIe x4 Connector (CN11)

Pin*1	Function name	Connection	MPU		Settings of Configuration Circuits
			Port	Pin	
A1	PRSNT1#	For a root complex: Fixed to the low level For an endpoint: Connected to PRSNT2#, PRSNT3#	— —	— —	— —
A5	TCK	Pull-Down	—	—	—
A6	TDI	Pull-Up	—	—	—
A7	TDO	NC	—	—	—
A8	TMS	Pull-Up	—	—	—
A11	PERST#	For a root complex: Connected to P33_3 (PCIE_RSTOUT0B) of the RZ/N2H For an endpoint: Input to the reset IC via JP38	P33_3*2 —	M20 —	DSW5-8: OFF, DSW9-5: OFF, DSW9-6: ON, **DSW4-1: ON** —
A13	REFCLK+	For a root complex: Clock driver output For an endpoint: Input to PCIE_REFCLK_P0 of the RZ/N2H	— —	— —	— —
A14	REFCLK-	For a root complex: Clock driver output For an endpoint: Input to PCIE_REFCLK_N0 of the RZ/N2H	— —	— —	— —
A16	HSIP0	Connected to PCIE_RXDP_L0 of the RZ/N2H	—	AD17	—
A17	HSIN0	Connected to PCIE_RXDN_L0 of the RZ/N2H	—	AC17	—
A21	HSIP1	For 1 Port: Connected to PCIE_RXDP_L1 of the RZ/N2H For 2 ports: NC	— —	AG19 —	— —
A22	HSIN1	For 1 Port: Connect to PCIE_RXDN_L1 of the RZ/N2H For 2 ports: NC	— —	AF19 —	— —
A21	HSIP1	NC	—	—	—
A22	HSIN1	NC	—	—	—
A25	HSIP2	NC	—	—	—
A26	HSIN2	NC	—	—	—
A29	HSIP3	NC	—	—	—
A30	HSIN3	NC	—	—	—
B5	SMCLK	Pull-Up	—	—	—
B6	SMDAT	Pull-Up	—	—	—
B9	TRST#	Pull-Down	—	—	—
B10	3V3AUX	Connected to the 3.3-V power supply for the PCIe x4 connector (only supplied for a root complex)	—	—	—
B11	WAKE#	Connected to P12_7 of the RZ/N2H	P12_7*3	E21	DSW5-1: OFF, DSW5-2: OFF
B12	CLKREQ#	For a root complex: Clock driver input For an endpoint: Connected to P10_7 (PCIEx4_CLKREQ) of the RZ/N2H	— P10_7	— A4	— DSW4-1: OFF
B14	HSOP0	Connected to PCIE_TXDP_L0 of the RZ/N2H	—	AD20	—
B15	HSON0	Connected to PCIE_TXDN_L0 of the RZ/N2H	—	AC20	—

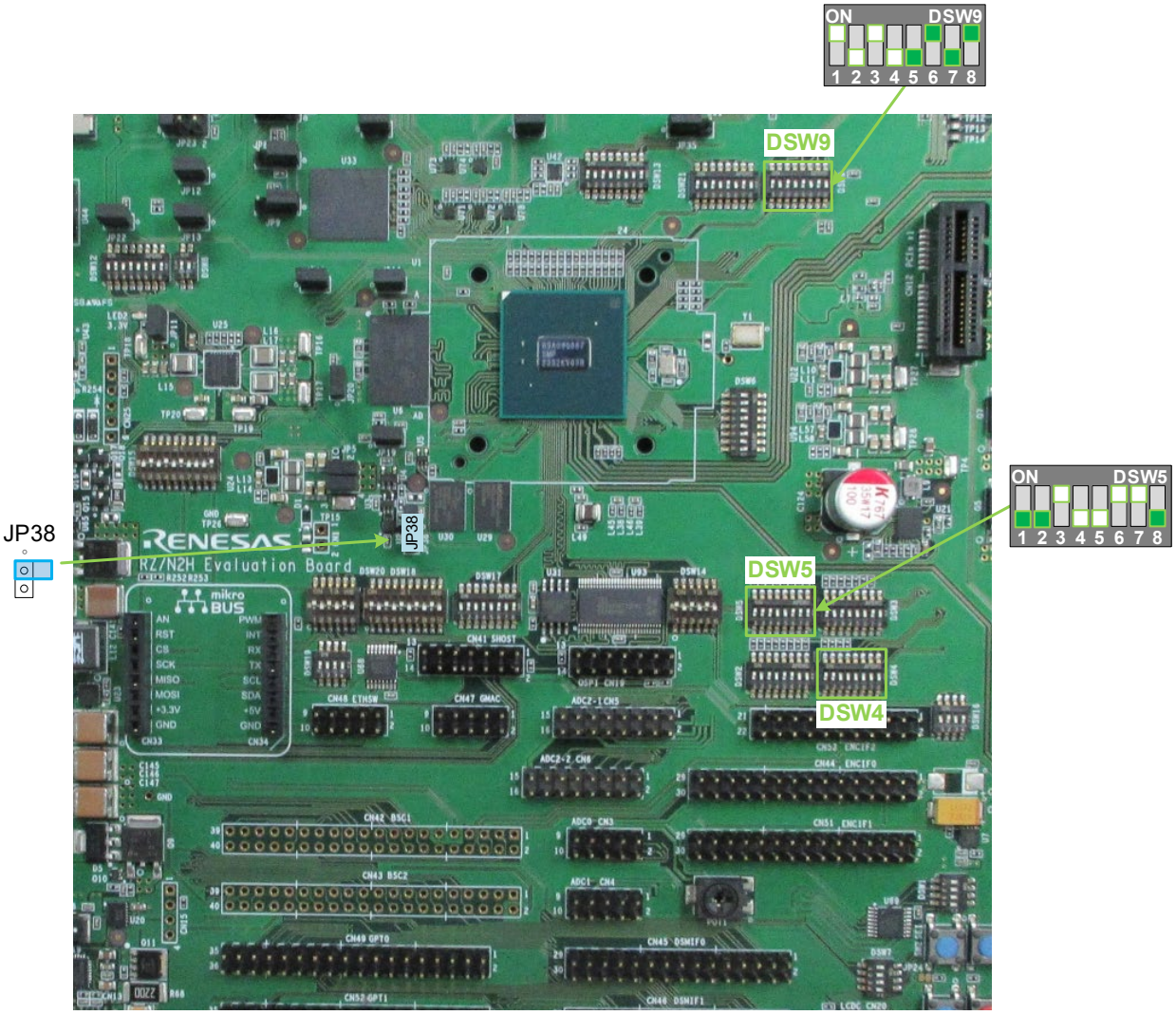
B17	PRSNT2#	For a root complex: Connected to P10_7 of the RZ/N2H (same as B31) For an endpoint: Connected to PRSNT1#	P10_7 —	A4 —	**DSW4-1: ON** —
B19	HSOP1	For 1 port: Connected to PCIE_TXDP_L1 of the RZ/N2H For 2 ports: NC	— —	AD19 —	— —
B20	HSON1	For 1 port: Connected to PCIE_TXDN_L1 of the RZ/N2H For 2 ports: NC	— —	AC19 —	— —
B23	HSOP2	NC	—	—	—
B24	HSON2	NC	—	—	—
B27	HSOP3	NC	—	—	—
B28	HSON3	NC	—	—	—
B31	PRSNT3#	For a root complex: Connect to P10_7 of RZ/N2H (same as B17) For an endpoint: Connected to PRSNT1#	P10_7 —	A4 —	**DSW4-1: ON** —

Notes: 1. The pins for power supplies (12 V, 3.3 V, and GROUND) and reserved pins are omitted.
2. Connected via the bus switch IC and DIP switch.
3. Connected via the level shifter IC with an enable function.

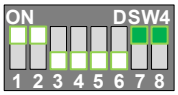
Table 7-32 Signal Connections of PCIe x1 Connector (CN12) (Only for a Configuration 1 of Lane x 2 Ports)

Pin*1	Function name	Connection	MPU		Settings of Configuration Circuits
			Port	Pin	
A1	PRSNT1#	For a root complex: Fixed to the low level For an endpoint: Connected to PRSNT2#	— —	— —	— —
A5	TCK	Pull-Down	—	—	—
A6	TDI	Pull-Up	—	—	—
A7	TDO	NC	—	—	—
A8	TMS	Pull-Up	—	—	—
A11	PERST#	For a root complex: Connected to P33_4 (PCIE_RSTOUT1B) of the RZ/N2H For an endpoint: Input to the reset IC via JP38	P33_4*2 —	N20 —	DSW5-8: OFF, DSW9-7: OFF, DSW9-8: ON, **DSW4-2: ON** —
A13	REFCLK+	For a root complex: Clock driver output For an endpoint: Input to PCIE_REFCLK_P1 of the RZ/N2H	— —	— AA16	— —
A14	REFCLK-	For a root complex: Clock driver output For an endpoint: Input to PCIE_REFCLK_N1 of the RZ/N2H	— —	— Y16	— —
A16	HSIP0	Connected to PCIE_RXDP_L1 of the RZ/N2H	—	AD16	—
A17	HSIN0	Connected to PCIE_RXDN_L1 of the RZ/N2H	—	AC16	—
B5	SMCLK	Pull-Up	—	—	—
B6	SMDAT	Pull-Up	—	—	—
B9	TRST#	Pull-Down	—	—	—
B10	3V3AUX	Connected to the 3.3-V power supply for the PCIe x1 connector (only supplied for a root complex)	—	—	—
B11	WAKE#	Connected to P10_2 of the RZ/N2H	P10_2	B3	—
B12	CLKREQ#	For a root complex: Clock driver input For an endpoint: Connected to P10_6 of the RZ/N2H	— P10_6	— A3	— DSW4-2: OFF
B14	HSOP0	Connected to PCIE_TXDP_L1 of the RZ/N2H	—	AD19	—
B15	HSON0	Connected to PCIE_TXDN_L1 of the RZ/N2H	—	AC19	—
B17	PRSNT2#	For a root complex: Connected to P10_6 of the RZ/N2H For an endpoint: Connected to PRSNT1#	P10_6 —	A3 —	**DSW4-2: ON** —

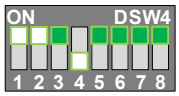
Notes: 1. The pins for power supplies (12 V, 3.3 V, and GROUND) and reserved pins are omitted.
2. Connected via the bus switch IC and DIP switch.



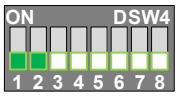
Configuration 1
Root complex, 2 lane 1 port



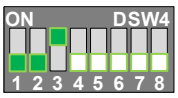
Configuration 2
Root complex, 1 lane 2 port



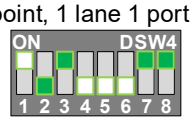
Configuration 3
Endpoint, 2 lane 1 port



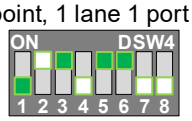
Configuration 4
Endpoint, 1 lane 2 port



Configuration 5
Root complex, 1 lane 1 port (CN11)
Endpoint, 1 lane 1 port (CN12)



Configuration 6
Endpoint, 1 lane 1port (CN12)
Endpoint, 1 lane 1 port (CN11)



□ : Initial setting
■ : Changed from the initial setting

Figure 7-28 Switch Settings When Using PCIe

When endpoint mode is selected, the PCIe reset signal can be included in the system reset factors by short-circuiting JP38. On the board as shipped, JP38 is open-circuit.

7.19 LCD Interface

This board is equipped with an LCD interface connector (CN20). Figure 7-29 shows the configuration of the LCD interface circuit, and Table 7-33 lists the signal connections. Figure 7-30 shows the switch settings when using the LCD interface.

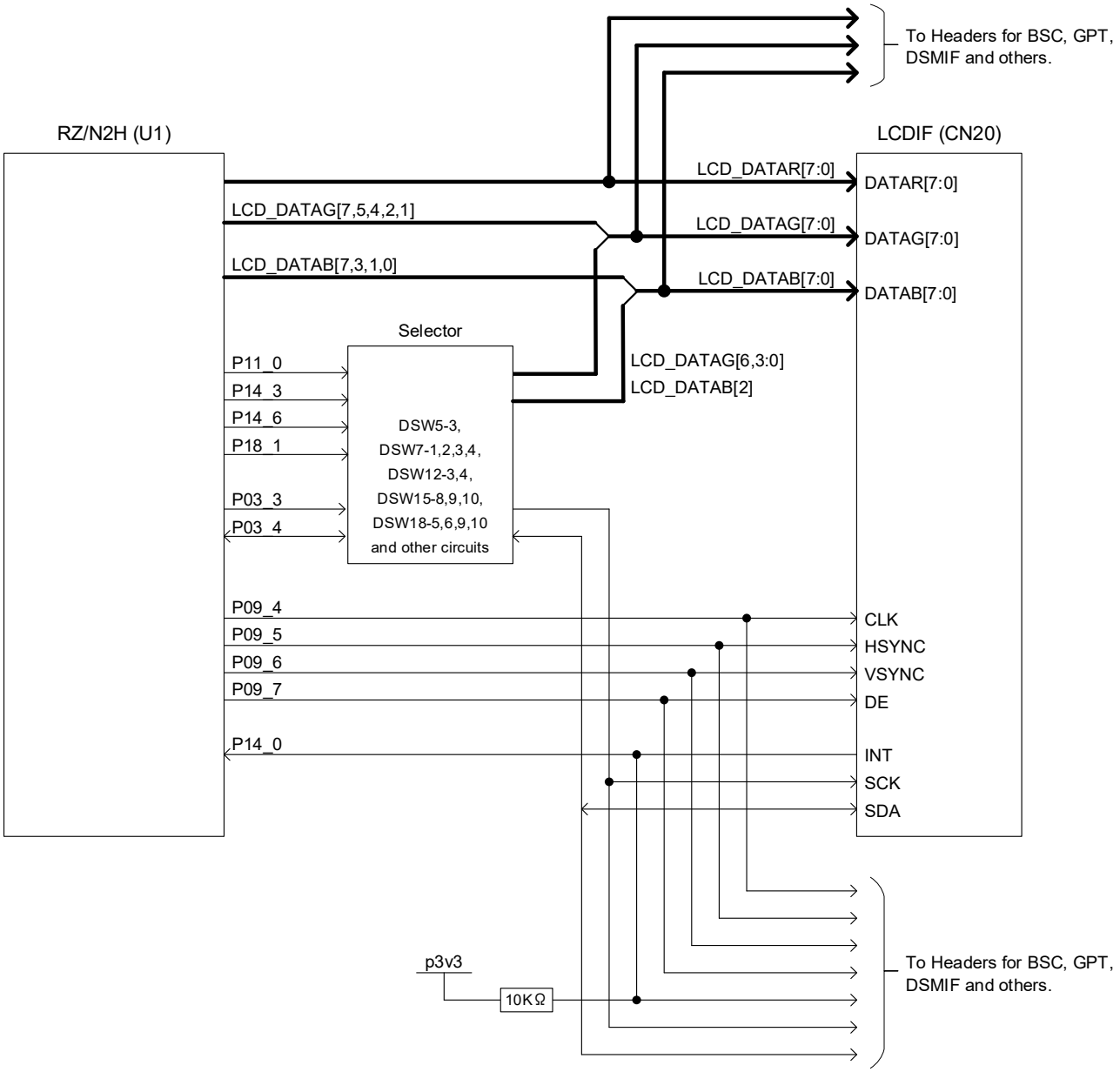


Figure 7-29 Configuration of LCD Interface Circuit

Table 7-33 Signal Connections of LCD Interface Connector (CN20)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P03_4_I2C_SDA1	P03_4*1	W9	**DSW7-3: ON, DSW7-4: OFF**
2	P03_3_I2C_SCL1	P03_3*1	AA9	**DSW7-1: ON, DSW7-2: OFF**
3	p5v0	—	—	—
4	P14_0_HEADER_BSC_A0_RS485_DE3_LCDC_IRQ5	P14_0	A8	
5	GROUND	—	—	
6	p1v8			
7	p1v8			
8	p1v8			
9	p1v8			
10	GROUND			
11	p3v3			
12	P09_7_HEADER_BSC_WE0#_LCDC_DE_PMOD2_RST	P09_7	C4	
13	P09_6_HEADER_BSC_D15_LCDC_VSYNC_PMOD1_RST	P09_6	C1	
14	P09_5_HEADER_BSC_D14_LCDC_HSYNC	P09_5	B1	
15	GROUND	—	—	
16	P09_4_HEADER_BSC_D13_LCDC_CLK	P09_4	A2	
17	GROUND	—	—	
18	P18_6_HEADER_BSC_A14_LCDC_DATB7	P18_6	C13	
19	P18_5_HEADER_BSC_A13_LCDC_DATB6	P18_5	A12	
20	P18_4_HEADER_BSC_A12_LCDC_DATB5	P18_4	B13	
21	P18_3_HEADER_BSC_A11_LCDC_DATB4	P18_3	A13	
22	P18_2_HEADER_BSC_A10_LCDC_DATB3_SEI	P18_2	C12	
23	P18_1_HEADER_BSC_A9_LCDC_DATB2	P18_1*1	B12	DSW18-9: OFF, DSW18-10: ON
24	P18_0_HEADER_BSC_A8_LCDC_DATB1_XSPI1_IRQ7	P18_0	F12	—
25	P17_7_HEADER_BSC_WE3#/AH#_LCDC_DATB0_ETHSW_PTPOUT1	P17_7	E12	
26	P17_6_HEADER_BSC_WE2#_LCDC_DATG7_ETHSW_PTPOUT0	P17_6	D12	
27	P14_6_LCDC_DATG6	P14_6*1	A10	DSW15-8: ON, **DSW15-9: OFF,** DSW15-10: OFF
28	P14_5_HEADER_BSC_TEND_LCDC_DATG5	P14_5	D9	—
29	P14_4_HEADER_BSC_DACK_LCDC_DATG4_MBX_HINT#	P14_4	B9	—
30	P14_3_HEADER_BSC_DREQ_LCDC_DATG3_PMOD1_IRQ6_MikroBUS_TX	P14_3*2	C10	DSW5-3: OFF, DSW18-5: OFF, DSW18-6: ON
31	P14_2_HEADER_BSC_BS#_LCDC_DATG2_MikroBUS_RX	P14_2	E9	—
32	P14_1_HEADER_BSC_RD/WR#_LCDC_DATG1	P14_1	C9	
33	P11_0_HEADER_BSC_A5_LCDC_DATG0	P11_0*1	A5	DSW12-3: ON, DSW12-4: OFF
34	P10_7_HEADER_BSC_A4_LCDC_DATR7_PCIx4_PRSNT_IRQ	P10_7	A4	—

	9_CLKREQ			
35	P10_6_HEADER_BSC_A3_LCDC_DATR6_PCIEx1_PRSNT_IRQ0_CLKREQ	P10_6	A3	
36	P10_5_HEADER_BSC_A2_LCDC_DATR5	P10_5	B4	
37	P10_4_HEADER_BSC_A1_LCDC_DATR4	P10_4	C5	
38	P10_3_HEADER_BSC_RD#_LCDC_DATR3	P10_3	C3	
39	P10_2_HEADER_BSC_CS0#_LCDC_DATR2_PCIEx1_IRQ1_WAKE	P10_2	B3	
40	P10_1_HEADER_BSC_WAIT#_LCDC_DATR1_MikroBUS_PWM	P10_1	B2	
41	P10_0_HEADER_BSC_WE1#_LCDC_DATR0_MikroBUS_RST	P10_0	C2	
42	p3v3	—	—	
43	p3v3	—	—	—
44	GROUND			
45	GROUND			

Notes: 1. Connected via the DIP switch.
2. Connected via the bus switch IC and DIP switch.

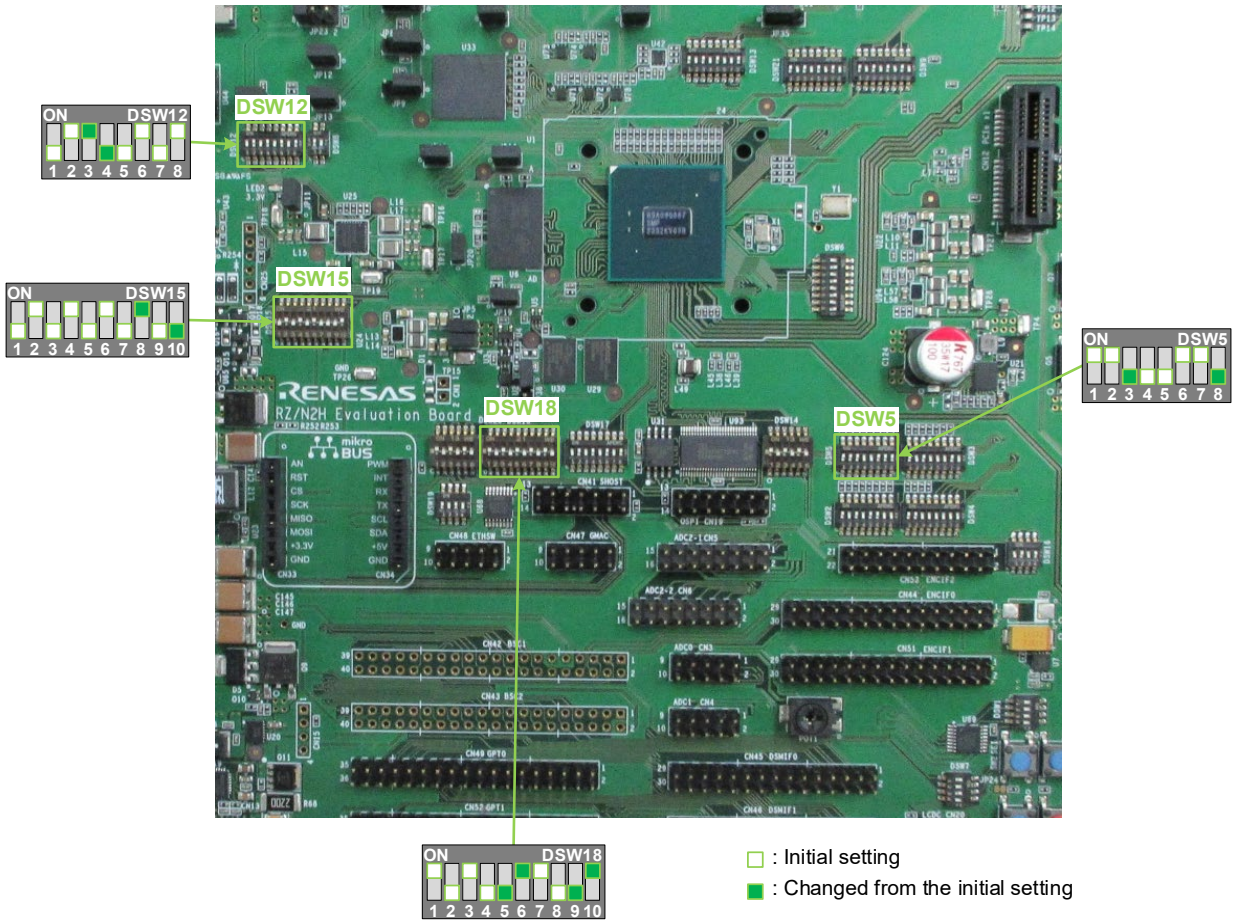


Figure 7-30 Switch Settings When Using the LCD Interface

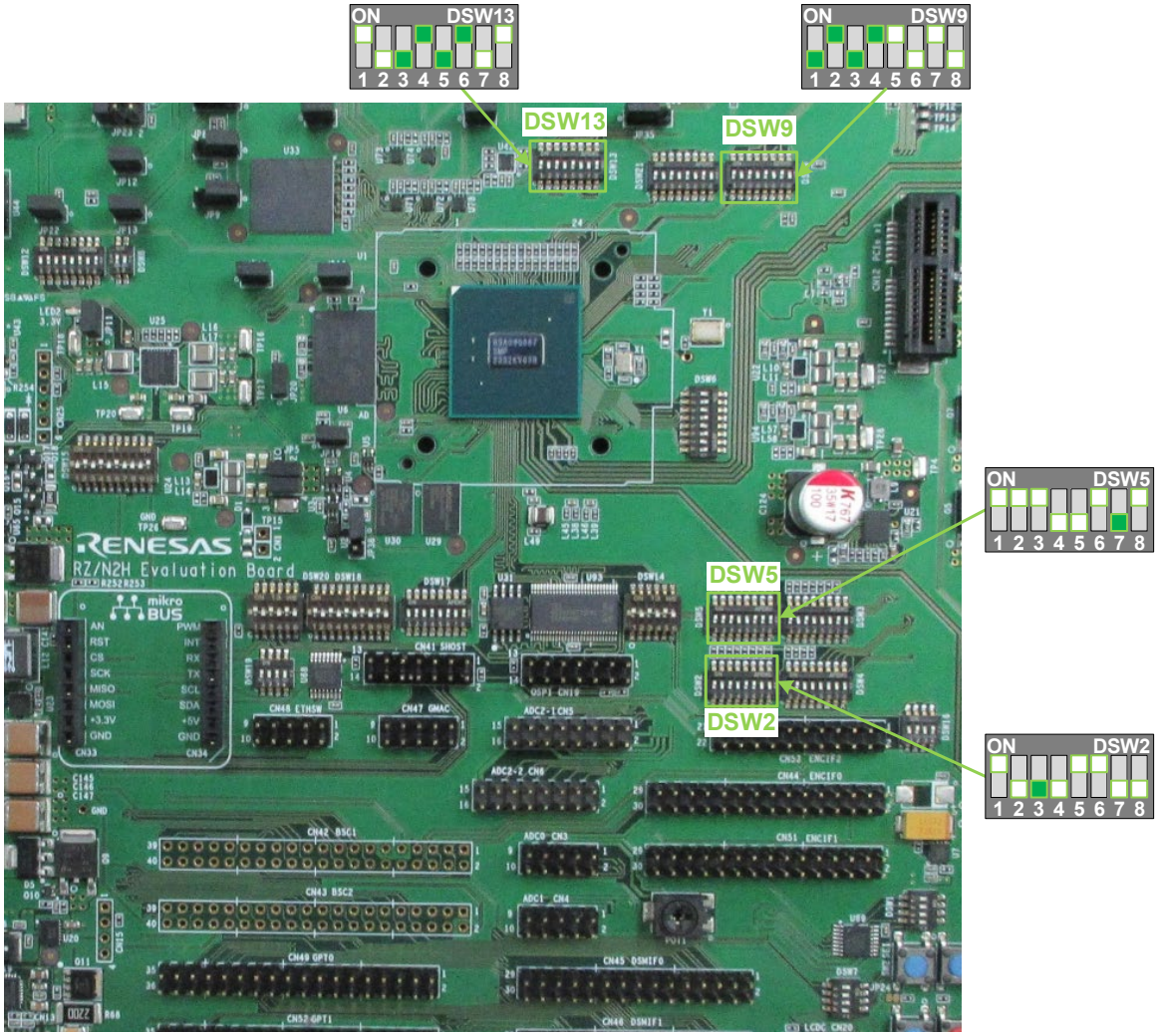
7.20 Serial Host Interface

This board is equipped with a connector (CN41) for the serial host interface, and the serial host interface of the RZ/N2H can be evaluated by connecting the connector to an external host CPU. Table 7-34 lists the signal connections of the serial host interface connector (CN41). Figure 7-31 shows the switch settings when using the serial host interface.

Table 7-34 Signal Connections of Serial Host Interface Connector (CN41)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	GROUND	—	—	—
2	P27_0_HEADER_BSC_CS5# (HSPI_INT#)	P27_0*1	D22	DSW13-3: OFF, DSW13-4: ON
3	P27_6_HEADER (HSPI_CK)	P27_6*2	C24	DSW2-3: OFF
4	P27_1_HEADER (HSPI_CS#)	P27_1*1	B23	DSW13-5: OFF, DSW13-6: ON
5	P31_5_HEADER_BSC_DACK (HSPI_IO7)	P31_5*2	J23	DSW5-7: OFF
6	P31_4_HEADER_BSC_DREQ (HSPI_IO6)	P31_4*2	J21	
7	P31_3_HEADER (HSPI_IO5)	P31_3*2	J22	DSW2-3: OFF
8	P31_2_HEADER (HSPI_IO4)	P31_2*2	J24	DSW5-7: OFF
9	P27_5_HEADER (HSPI_IO3)	P27_5*1	C23	DSW9-3: OFF, DSW9-4: ON
10	P27_4_HEADER (HSPI_IO2)	P27_4*1	D23	DSW9-1: OFF, DSW9-2: ON
11	P27_3_HEADER (HSPI_IO1)	P27_3*2	A23	DSW2-3: OFF
12	P27_2_HEADER_IRQ3 (HSPI_IO0)	P27_2*2	B24	
13	P14_4_HEADER_BSC_DACK_LCDC_DATG4_MBX_HINT# (MBX_HINT#)	P14_4	B9	—
14	p3v3	—	—	—

Notes: 1. Connected via the DIP switch.
2. Connected via the bus switch IC.



□ : Initial setting
■ : Changed from the initial setting

Figure 7-31 Switch Settings When Using the Serial Host Interface

7.21 Pin Headers

This board is equipped with the 2.54-mm pitch pin headers listed in Table 7-35. Table 7-36 to Table 7-50 list the signal connections of the pin headers. Figure 7-32 to Figure 7-38 show the switch settings when using the pin headers.

Table 7-35 List of Pin Headers

Function	Reference	Number of pins	Description
ENCIF Interface	CN44	30 (15 × 2)	For ENCIF0 (unit 0, 1, and 4)
	CN51	30 (15 × 2)	For ENCIF1 (unit 9 to 11)
	CN53	22 (11 × 2)	For ENCIF2 (for unit 14)
DSMIF Interface	CN45	30 (15 × 2)	For DSMIF0 (unit 0 to 1)
	CN46	30 (15 × 2)	For DSMIF1 (unit 3 to 5)
GPT Interface	CN49	36 (18 × 2)	For GPT0 (unit 0 to 2)
	CN52	36 (18 × 2)	For GPT1 (unit 3 to 5)
ETHSW signal monitor	CN48	10 (5 × 2)	For monitoring the PTPOUT and TDMAOUT signals
GMAC signal monitor	CN47	10 (5 × 2)	For monitoring the PTPTRG signals
Bus Interface	CN42	40 (20 × 2)	For the address line and others
	CN43	40 (20 × 2)	For the data line and others
ADC	CN3	10 (5 × 2)	For ADC0
	CN4	10 (5 × 2)	For ADC1
	CN5	16 (8 × 2)	For ADC2_1
	CN6	16 (8 × 2)	For ADC2_2

Table 7-36 Signal Connections of ENCIF0 (CN44)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	ENCIFCK01	P02_0_V1833_5_HEADER	P02_0*1	AA12	DSW2-6: OFF
3	ENCIFCK00	P14_2_HEADER_BSC_BS#_LCDC_DATG2_MikroBUS_RX	P14_2	E9	—
4	ENCIFOE01	P02_1_V1833_5_HEADER	P02_1*1	AA10	DSW2-6: OFF
5	ENCIFOE00	P14_3_HEADER_BSC_DREQ_LCDC_DATG3_PMOD1_IRQ6_MikroBUS_TX	P14_3*2	C10	DSW5-3: OFF, DSW18-5: OFF, DSW18-6: ON
6	ENCIFDO01	P26_7_HEADER_BSC_CS3#	P26_7*3	E22	DSW13-1: OFF, DSW13-2: ON
7	ENCIFDO00	P14_4_HEADER_BSC_DACK_LCDC_DATG4_MBX_HINT#	P14_4	B9	—
8	ENCIFDI01	P27_0_HEADER_BSC_CS5#	P27_0*3	D22	DSW13-3: OFF, DSW13-4: ON
9	ENCIFDI00	P14_5_HEADER_BSC_TEND_LCDC_DATG5	P14_5	D9	—
10	GROUND	GROUND	—	—	—
11	ENCIFCK02	NC	—	—	—
12	ENCIFCK03	NC	—	—	—
13	ENCIFOE02	NC	—	—	—
14	ENCIFOE03	NC	—	—	—
15	ENCIFDO02	NC	—	—	—
16	ENCIFDO03	NC	—	—	—
17	ENCIFDI02	NC	—	—	—
18	ENCIFDI03	NC	—	—	—
19	GROUND	GROUND	—	—	—
20	ENCIFCK05	NC	—	—	—
21	ENCIFCK04	P10_2_HEADER_BSC_CS0#_LCDC_DATR2_PCIEx1_IRQ1_WAKE	P10_2	B3	—
22	ENCIFOE05	NC	—	—	—
23	ENCIFOE04	P10_3_HEADER_BSC_RD#_LCDC_DATR3	P10_3	C3	—
24	ENCIFDO05	NC	—	—	—
25	ENCIFDO04	P10_4_HEADER_BSC_A1_LCDC_DATR4	P10_4	C5	—
26	ENCIFDI05	NC	—	—	—
27	ENCIFDI04	P10_5_HEADER_BSC_A2_LCDC_DATR5	P10_5	B4	—
28	GROUND	GROUND	—	—	—
29	p5v0	p5v0	—	—	—
30	p3v3	p3v3	—	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via the bus switch IC and DIP switch.
3. Connected via the DIP switch.

Table 7-37 Signal Connections of ENCIF1 (CN51)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	ENCIFCK07	NC	—	—	—
3	ENCIFCK06	NC	—	—	—
4	ENCIFOE07	NC	—	—	—
5	ENCIFOE06	NC	—	—	—
6	ENCIFDO07	NC	—	—	—
7	ENCIFDO06	NC	—	—	—
8	ENCIFDI07	NC	—	—	—
9	ENCIFDI06	NC	—	—	—
10	GROUND	GROUND	—	—	—
11	ENCIFCK08	NC	—	—	—
12	ENCIFCK09	P29_1_VDD1833_2_HEADER	P29_1*	E23	DSW5-7: OFF
13	ENCIFOE08	NC	—	—	—
14	ENCIFOE09	P29_2_VDD1833_2_HEADER	P29_2*	H20	DSW5-7: OFF
15	ENCIFDO08	NC	—	—	—
16	ENCIFDO09	P29_3_VDD1833_2_HEADER	P29_3*	G22	DSW5-7: OFF
17	ENCIFDI08	NC	—	—	—
18	ENCIFDI09	P29_4_VDD1833_2_HEADER	P29_4*	F22	DSW5-7: OFF
19	GROUND	GROUND	—	—	—
20	ENCIFCK11	P30_1_VDD1833_2_HEADER	P30_1*	G23	DSW5-7: OFF
21	ENCIFCK10	P29_5_VDD1833_2_HEADER	P29_5*	G21	
22	ENCIFOE11	P30_2_VDD1833_2_HEADER	P30_2*	E24	
23	ENCIFOE10	P29_6_VDD1833_2_HEADER	P29_6*	F21	
24	ENCIFDO11	P30_3_VDD1833_2_HEADER	P30_3*	H23	
25	ENCIFDO10	P29_7_VDD1833_2_HEADER	P29_7*	H22	
26	ENCIFDI11	P30_4_VDD1833_2_HEADER	P30_4*	D24	
27	ENCIFDI10	P30_0_VDD1833_2_HEADER	P30_0*	F20	
28	GROUND	GROUND	—	—	—
29	p5v0	p5v0	—	—	—
30	p3v3	p3v3	—	—	—

Note: Connected via the bus switch IC.

Table 7-38 Signal Connections of ENCIF2 (CN53)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	ENCIFCK13	NC	—	—	—
3	ENCIFCK12	NC	—	—	—
4	ENCIFOE13	NC	—	—	—
5	ENCIFOE12	NC	—	—	—
6	ENCIFDO13	NC	—	—	—
7	ENCIFDO12	NC	—	—	—
8	ENCIFDI13	NC	—	—	—
9	ENCIFDI12	NC	—	—	—
10	GROUND	GROUND	—	—	—
11	ENCIFCK14	P27_3_HEADER	P27_3*1	A23	DSW2-3: OFF
12	ENCIFCK15	NC	—	—	—
13	ENCIFOE14	P27_4_HEADER	P27_4*2	D23	DSW9-1: OFF, DSW9-2: ON
14	ENCIFOE15	NC	—	—	—
15	ENCIFDO14	P27_5_HEADER	P27_5*2	C23	DSW9-3: OFF, DSW9-4: ON
16	ENCIFDO15	NC	—	—	—
17	ENCIFDI14	P27_6_HEADER	P27_6*1	C24	DSW2-3: OFF
18	ENCIFDI15	NC	—	—	—
19	NC	NC	—	—	—
20	GROUND	GROUND	—	—	—
21	p5v0	p5v0	—	—	—
22	p3v3	p3v3	—	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via the DIP switch.

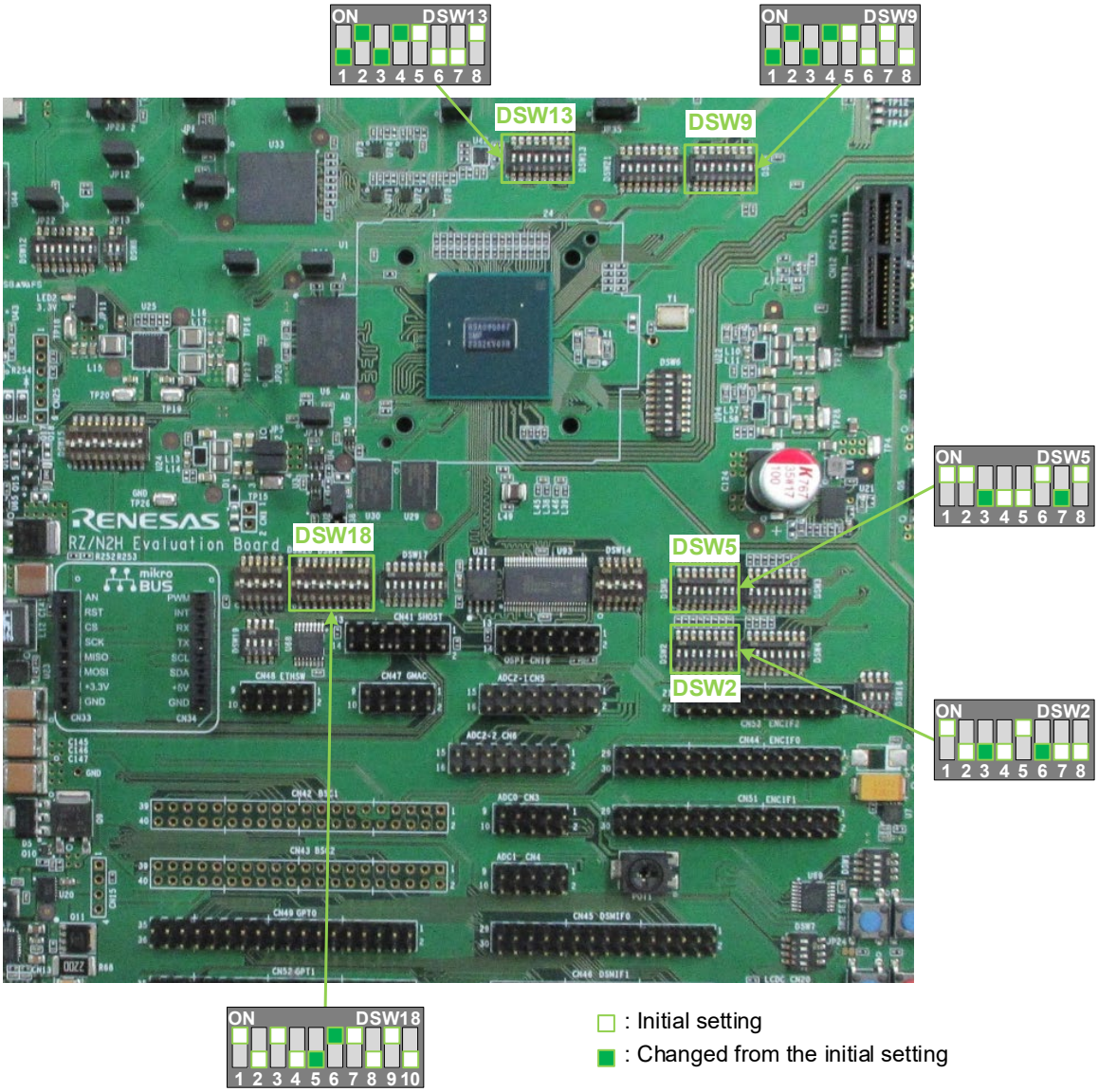


Figure 7-32 Switch Settings When Using ENCIF0 (CN44), ENCIF1 (CN51), and ENCIF2 (CN53)

Table 7-39 Signal Connections of DSMIF0 (CN45)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	p5v0	p5v0	—	—	—
2	p3v3	p3v3	—	—	—
3	MCLK02	P12_4_HEADER_BSC_D20_PMOD2_RXD2	P12_4*	B8	DSW5-1: OFF, DSW5-2: OFF
4	MDAT02	P12_5_HEADER_BSC_D21_PMOD2_TXD2	P12_5*	D7	
5	MCLK01	P13_2_HEADER_BSC_D26_PMOD1_MISO3	P13_2*	F8	
6	MDAT01	P13_3_HEADER_BSC_D27_PMOD1_SSL30	P13_3	F9	—
7	MCLK00	P13_0_HEADER_BSC_D24_PMOD1_RSPCK3	P13_0*	B7	DSW5-1: OFF, DSW5-2: OFF
8	MDAT00	P13_1_HEADER_BSC_D25_PMOD1_MOSI3	P13_1*	C6	
9	GROUND	GROUND	—	—	—
10	GROUND	GROUND	—	—	—
11	p5v0	p5v0	—	—	—
12	p3v3	p3v3	—	—	—
13	MCLK12	P18_6_HEADER_BSC_A14_LCDC_DATB7	P18_6	C13	—
14	MDAT12	P18_7_PSW_IRQ4_HEADER_BSC_A15_ETHSW_PTPOUT3	P18_7	F13	—
15	MCLK11	P18_4_HEADER_BSC_A12_LCDC_DATB5	P18_4	B13	—
16	MDAT11	P18_5_HEADER_BSC_A13_LCDC_DATB6	P18_5	A12	—
17	MCLK10	P18_2_HEADER_BSC_A10_LCDC_DATB3_SEI	P18_2	C12	—
18	MDAT10	P18_3_HEADER_BSC_A11_LCDC_DATB4	P18_3	A13	—
19	GROUND	GROUND	—	—	—
20	GROUND	GROUND	—	—	—
21	p5v0	p5v0	—	—	—
22	p3v3	p3v3	—	—	—
23	MCLK22	NC	—	—	—
24	MDAT22	NC	—	—	—
25	MCLK21	NC	—	—	—
26	MDAT21	NC	—	—	—
27	MCLK20	NC	—	—	—
28	MDAT20	NC	—	—	—
29	GROUND	GROUND	—	—	—
30	GROUND	GROUND	—	—	—

Note: Connected via the level shifter IC with an enable function.

Table 7-40 Signal Connections of DSMIF1 (CN46)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	p5v0	p5v0	—	—	—
2	p3v3	p3v3	—	—	—
3	MCLK32	P31_5_HEADER_BSC_DACK	P31_5*1	J23	DSW5-7: OFF
4	MDAT32	P31_6_HEADER_BSC_TEND	P31_6*2	J20	DSW18-7: OFF, DSW18-8: ON
5	MCLK31	P31_3_HEADER	P31_3*1	J22	DSW2-3: OFF
6	MDAT31	P31_4_HEADER_BSC_DREQ	P31_4*1	J21	DSW5-7: OFF
7	MCLK30	P30_7_VDD1833_2_HEADER	P30_7*1	F24	
8	MDAT30	P31_2_HEADER	P31_2*1	J24	
9	GROUND	GROUND	-	-	-
10	GROUND	GROUND	-	-	-
11	p5v0	p5v0	-	-	-
12	p3v3	p3v3	-	-	-
13	MCLK42	P14_0_HEADER_BSC_A0_RS485_DE3_LCDC_IRQ5	P14_0	A8	-
14	MDAT42	P14_1_HEADER_BSC_RD/WR#_LCDC_DATG1	P14_1	C9	-
15	MCLK41	P13_6_HEADER_BSC_D30_PMOD2_GPIO1	P13_6	E6	-
16	MDAT41	P13_7_HEADER_BSC_D31	P13_7*2	A7	DSW13-7: ON, DSW13-8: OFF
17	MCLK40	P13_4_HEADER_BSC_D28	P13_4*3	A6	DSW2-4: ON
18	MDAT40	P13_5_HEADER_BSC_D29_RS485_TXD3	P13_5	C7	-
19	GROUND	GROUND	-	-	-
20	GROUND	GROUND	-	-	-
21	p5v0	p5v0	-	-	-
22	p3v3	p3v3	-	-	-
23	MCLK52	P33_6_VDD1833_3_HEADER_BSC_A20	P33_6*1	M21	DSW5-8: OFF
24	MDAT52	P33_7_VDD1833_3_HEADER_BSC_A21_MikroBUS_SCK	P33_7*1	L23	
25	MCLK51	P33_4_VDD1833_3_HEADER_BSC_A18_PCIE_RSTOUT1B	P33_4*4	N20	DSW5-8: OFF, DSW9-7: OFF, DSW9-8: ON
26	MDAT51	P33_5_VDD1833_3_HEADER_BSC_A19	P33_5*1	N21	DSW5-8: OFF
27	MCLK50	P33_2_VDD1833_3_HEADER_BSC_A16	P33_2*1	L20	
28	MDAT50	P33_3_VDD1833_3_HEADER_BSC_A17_PCIE_RSTOUT0B	P33_3*4	M20	DSW5-8: OFF, DSW9-5: OFF, DSW9-6: ON
29	GROUND	GROUND	—	—	—
30	GROUND	GROUND	—	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via the DIP switch.
3. Connected via the level shifter IC.
4. Connected via the bus switch IC and DIP switch.

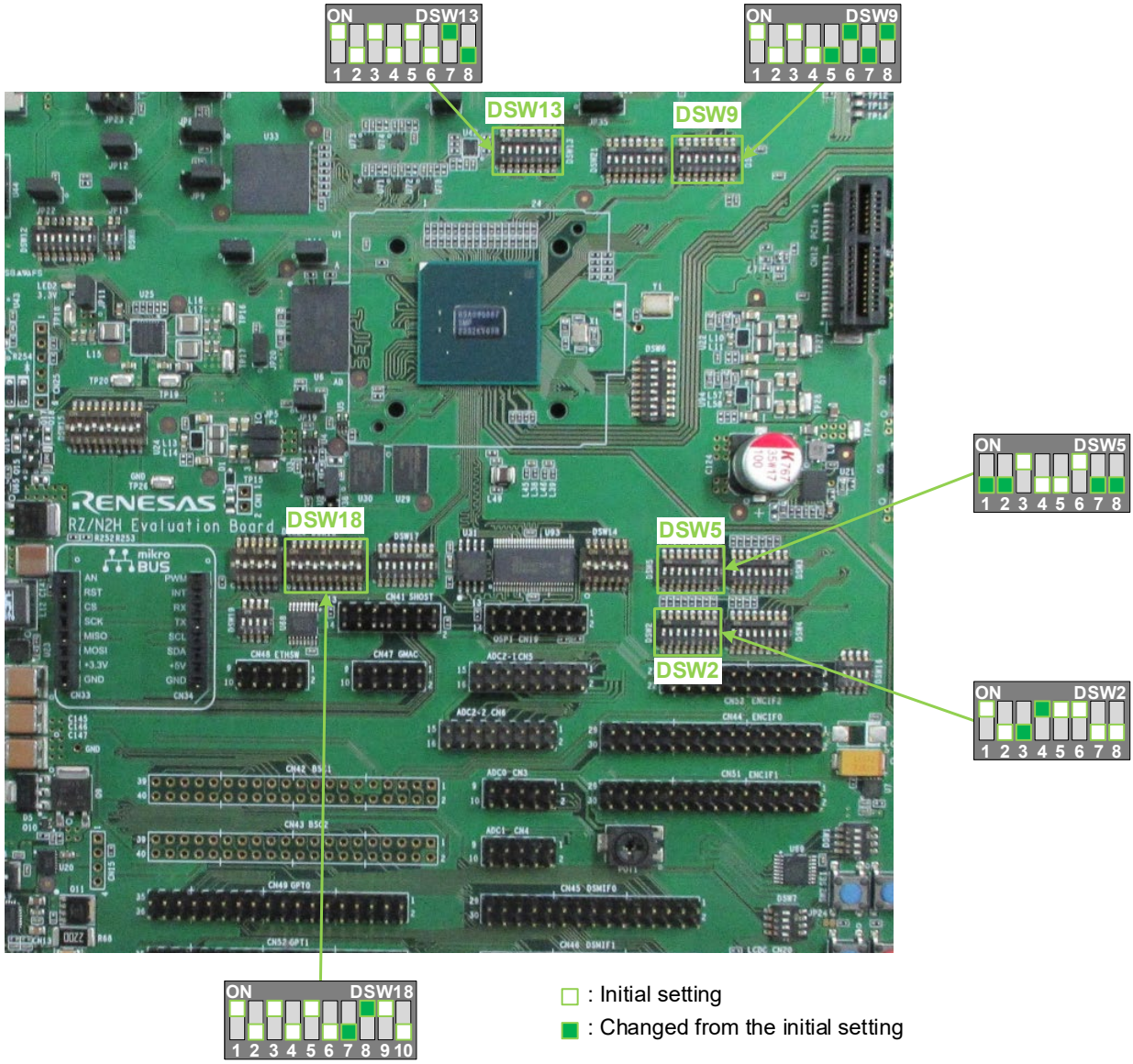


Figure 7-33 Switch Settings When Using DSMIF0 (CN45) and DSMIF1 (CN46)

Table 7-41 Signal Connections of GPT0 (CN49)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	GROUND	GROUND	—	—	—
3	GTIOC00_0A	P00_0_HEADER_BSC_D0	P00_0*1	AB13	DSW5-8: OFF, DSW2-5: OFF
4	GTIOC00_0B	P00_1_HEADER_BSC_D1	P00_1*1	AA13	
5	GTIOC00_1A	P00_2_HEADER_BSC_D2	P00_2*1	W12	
6	GTIOC00_1B	P00_3_HEADER_BSC_D3	P00_3*2	AD13	DSW12-1: ON, DSW12-2: OFF
7	GTIOC00_2A	P00_4_PSW_IRQ3_HEADER_BSC_D4	P00_4	AC13	—
8	GTIOC00_2B	P01_0_V1833_5_HEADER	P01_0*1	W11	DSW2-6: OFF
9	GTIOC00_3A	NC	—	—	—
10	GTIOC00_3B	NC	—	—	—
11	GTIOC00_4A	NC	—	—	—
12	GTIOC00_4B	NC	—	—	—
13	GROUND	GROUND	—	—	—
14	GROUND	GROUND	—	—	—
15	GTIOC01_0A	P01_2_V1833_5_HEADER	P01_2*1	Y12	DSW2-6: OFF
16	GTIOC01_0B	P01_3_V1833_5_HEADER	P01_3	AC12	—
17	GTIOC01_1A	P01_4_V1833_5_HEADER	P01_4*1	AD12	DSW2-6: OFF
18	GTIOC01_1B	P01_5_V1833_5_HEADER	P01_5*1	AC11	
19	GTIOC01_2A	P01_6_V1833_5_HEADER	P01_6*1	AD11	
20	GTIOC01_2B	P01_7_V1833_5_HEADER	P01_7*1	AB12	
21	GTIOC01_3A	NC	—	—	—
22	GTIOC01_3B	NC	—	—	—
23	GTIOC01_4A	NC	—	—	—
24	GTIOC01_4B	NC	—	—	—
25	GROUND	GROUND	—	—	—
26	GROUND	GROUND	—	—	—
27	GTIOC02_0A	P02_5_HEADER_BSC_D5	P02_5*2	AD10	DSW17-7: ON, DSW17-8: OFF
28	GTIOC02_0B	P02_6_HEADER_BSC_D6	P02_6*2	AB10	DSW17-5: ON, DSW17-6: OFF
29	GTIOC02_1A	P02_7_HEADER_BSC_D7	P02_7*2	AC9	DSW17-3: ON, DSW17-4: OFF
30	GTIOC02_1B	P03_0_HEADER_BSC_D8	P03_0*2	AD9	DSW17-1: ON, DSW17-2: OFF
31	GTIOC02_2A	P03_1_HEADER_BSC_D9	P03_1*2	Y9	DSW12-7: ON, DSW12-8: OFF
32	GTIOC02_2B	P03_2_HEADER_BSC_D10	P03_2*2	AB9	DSW12-5: ON, DSW12-6: OFF
33	GTIOC02_3A	NC	—	—	—
34	GTIOC02_3B	NC	—	—	—
35	GTIOC02_4A	NC	—	—	—
36	GTIOC02_4B	NC	—	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via the DIP switch.

Table 7-42 Signal Connections of GPT1 (CN52)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	GROUND	GROUND	—	—	—
3	GTIOC03_0A	P34_0_VDD1833_3_HEADER_BSC_A22_MikroBUS_MOSI	P34_0*1	L20	DSW5-8: OFF
4	GTIOC03_0B	P34_1_VDD1833_3_HEADER_BSC_A23_MikroBUS_MISO	P34_1*1	K20	
5	GTIOC03_1A	P34_2_VDD1833_3_HEADER_BSC_A24_MikroBUS_CS	P34_2*1	K22	
6	GTIOC03_1B	P34_3_VDD1833_3_HEADER_BSC_A25	P34_3*1	L21	
7	GTIOC03_2A	P34_4_VDD1833_3_HEADER_BSC_CS2#	P34_4*1	K23	
8	GTIOC03_2B	P34_5_VDD1833_3_HEADER_BSC_CS3#	P34_5*1	K21	
9	GTIOC03_3A	NC	—	—	—
10	GTIOC03_3B	NC	—	—	—
11	GTIOC03_4A	NC	—	—	—
12	GTIOC03_4B	NC	—	—	—
13	GROUND	GROUND	—	—	—
14	GROUND	GROUND	—	—	—
15	GTIOC04_0A	P09_4_HEADER_BSC_D13_LCDC_CLK	P09_4	A2	—
16	GTIOC04_0B	P09_5_HEADER_BSC_D14_LCDC_HSYNC	P09_5	B1	—
17	GTIOC04_1A	P09_6_HEADER_BSC_D15_LCDC_VSYNC_PMOD1_RST	P09_6	C1	—
18	GTIOC04_1B	P09_7_HEADER_BSC_WE0#_LCDC_DE_PMOD2_RST	P09_7	C4	—
19	GTIOC04_2A	P10_0_HEADER_BSC_WE1#_LCDC_DATR0_MikroBUS_RST	P10_0	C2	—
20	GTIOC04_2B	P10_1_HEADER_BSC_WAIT#_LCDC_DATR1_MikroBUS_PWM	P10_1	B2	—
21	GTIOC04_3A	NC	—	—	—
22	GTIOC04_3B	NC	—	—	—
23	GTIOC04_4A	NC	—	—	—
24	GTIOC04_4B	NC	—	—	—
25	GROUND	GROUND	—	—	—
26	GROUND	GROUND	—	—	—
27	GTIOC05_0A	P10_6_HEADER_BSC_A3_LCDC_DATR6_PCIEx1_PRSNT_IRQ0_CLKREQ	P10_6	A3	—
28	GTIOC05_0B	P10_7_HEADER_BSC_A4_LCDC_DATR7_PCIx4_PRSNT_IRQ9_CLKREQ	P10_7	A4	—
29	GTIOC05_1A	P12_0_HEADER_BSC_D16	P12_0*2	C8	DSW5-1: OFF, DSW5-2: OFF
30	GTIOC05_1B	P12_1_HEADER_BSC_D17	P12_1*2	E7	
31	GTIOC05_2A	P12_2_HEADER_BSC_D18_PMOD1_GPIO1	P12_2*2	E8	
32	GTIOC05_2B	P12_3_HEADER_BSC_D19_PMOD1_GPIO2	P12_3*2	F8	

33	GTIOC05_3A	NC	—	—	—
34	GTIOC05_3B	NC	—	—	—
35	GTIOC05_4A	NC	—	—	—
36	GTIOC05_4B	NC	—	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via the level shifter IC with an enable function.

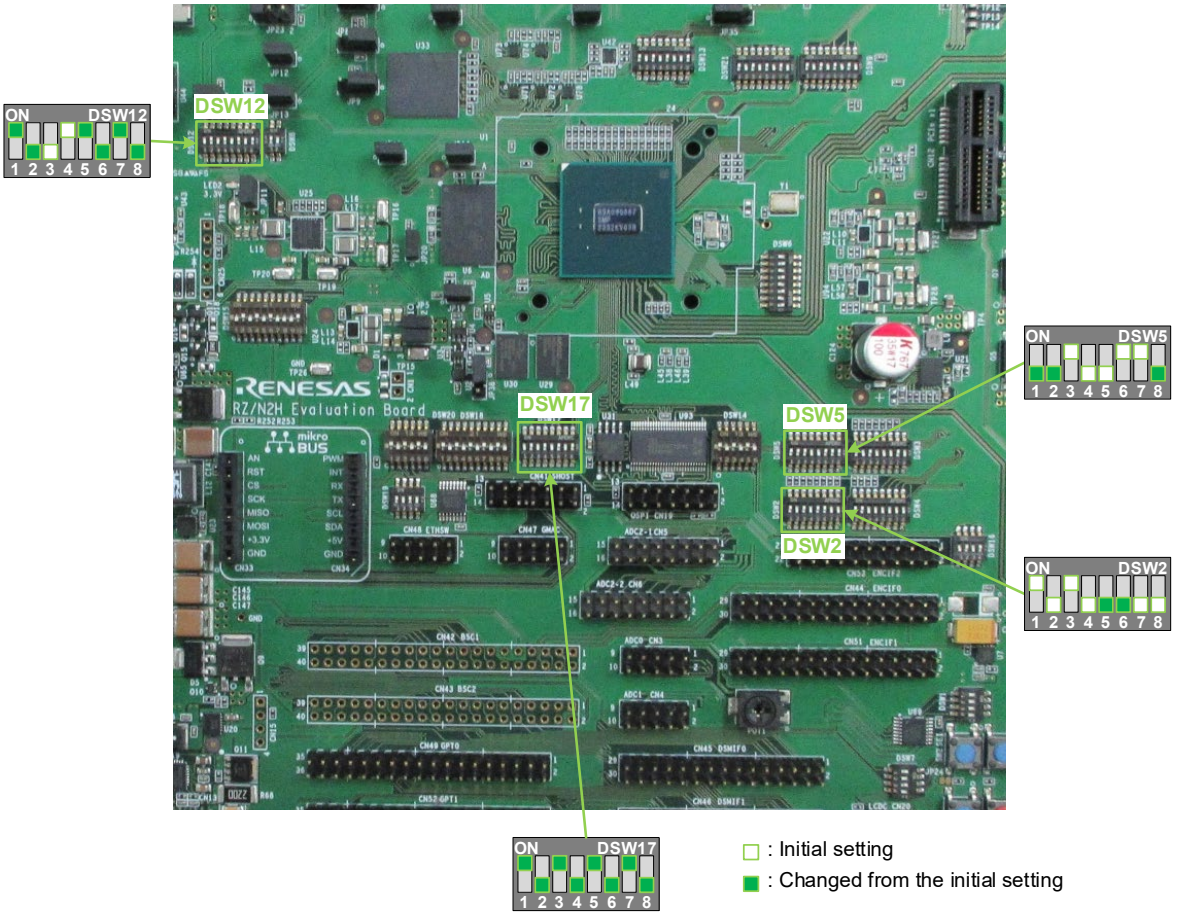


Figure 7-34 Switch Settings When Using GPT0 (CN49) and GPT1 (CN52)

Table 7-43 Signal Connections of ETHSW (CN48)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	ETHSW_PTPOUT0	P17_6_HEADER_BSC_WE2#_LCDC_DATG7_ETHSW_PTPOUT0	P17_6	D12	—
2	GROUND	GROUND	—	—	—
3	ETHSW_PTPOUT1	P17_7_HEADER_BSC_WE3#/AH#_LCDC_DATB0_ETHSW_PTPOUT1	P17_7	E12	—
4	ETHSW_TDMAOUT0	P31_6_HEADER_BSC_TEND	P31_6*1	J20	DSW18-7: OFF, DSW18-8: ON
5	ETHSW_PTPOUT2	P14_0_HEADER_BSC_A0_RS485_DE3_LCDC_IRQ5	P14_0	A8	—
6	ETHSW_TDMAOUT1	P31_3_HEADER	P31_3*2	J22	DSW2-3: OFF
7	ETHSW_PTPOUT3	P18_7_PSW_IRQ4_HEADER_BSC_A15_ETHSW_PTPOUT3	P18_7	F13	—
8	ETHSW_TDMAOUT2	P22_7_HEADER	P22_7*1	D18	DSW18-1: OFF, DSW18-2: ON
9	GROUND	GROUND	—	—	—
10	ETHSW_TDMAOUT3	P23_0_HEADER_MikroBUS_IRQ10	P23_0*1	F17	DSW18-3: OFF, DSW18-4: ON

Notes: 1. Connected via the DIP switch.
2. Connected via the bus switch IC.

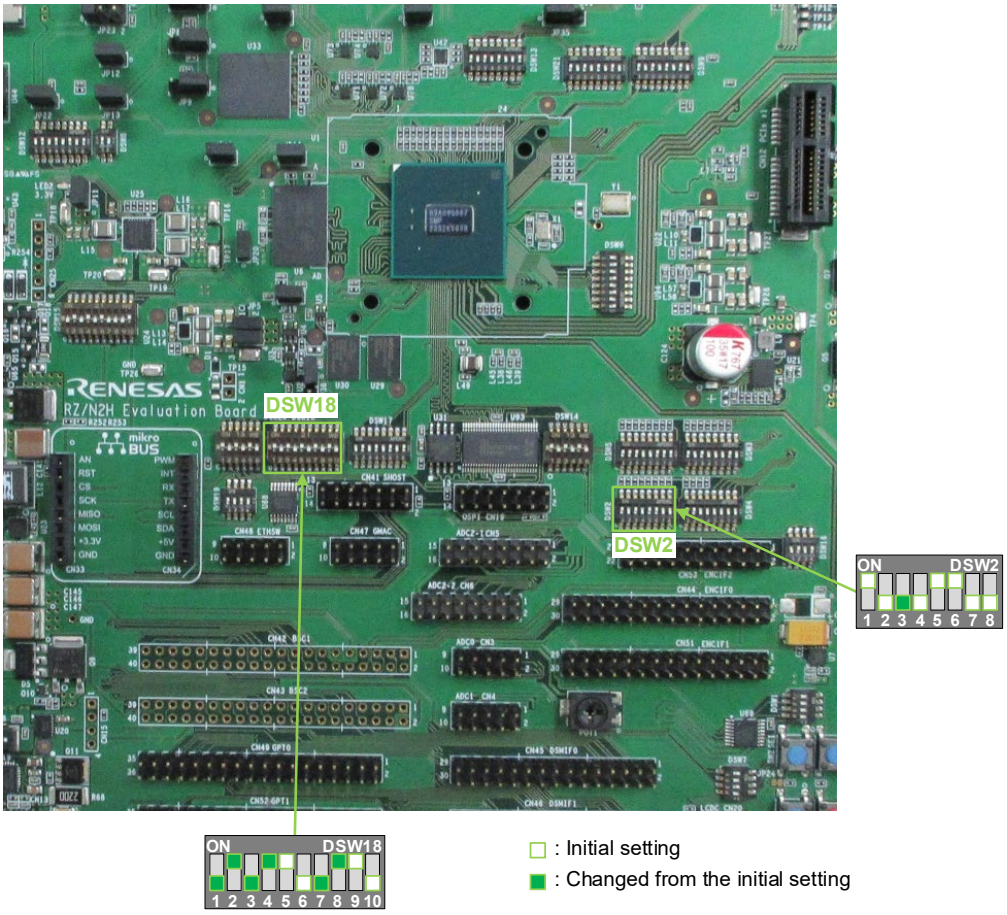


Figure 7-35 Switch Settings When Using ETHSW (CN48)

Table 7-44 Signal Connections of GMAC (CN47)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GMAC0_PTPTRG0	P22_5_GMAC0_PTPTRG0	P22_5*1	B18	DSW15-3: ON, DSW15-4: OFF
2	GMAC0_PTPTRG1	P22_6_GMAC0_PTPTRG1_PMOD2_IRQ8	P22_6*1	C18	DSW15-1: ON, DSW15-2: OFF
3	GMAC1_PTPTRG0	P27_2_HEADER	P27_2*2	B24	DSW2-3: OFF
4	GMAC1_PTPTRG1	P27_3_HEADER	P27_3*2	A23	
5	GMAC2_PTPTRG0	P31_6_HEADER_BSC_TEND	P31_6*1	J20	DSW18-7: OFF, DSW18-8: ON
6	GMAC2_PTPTRG1	NC	—	—	—
7	—	NC	—	—	—
8	—	NC	—	—	—
9	—	NC	—	—	—
10	—	NC	—	—	—

Notes: 1. Connected via the DIP switch.
2. Connected via the bus switch IC.

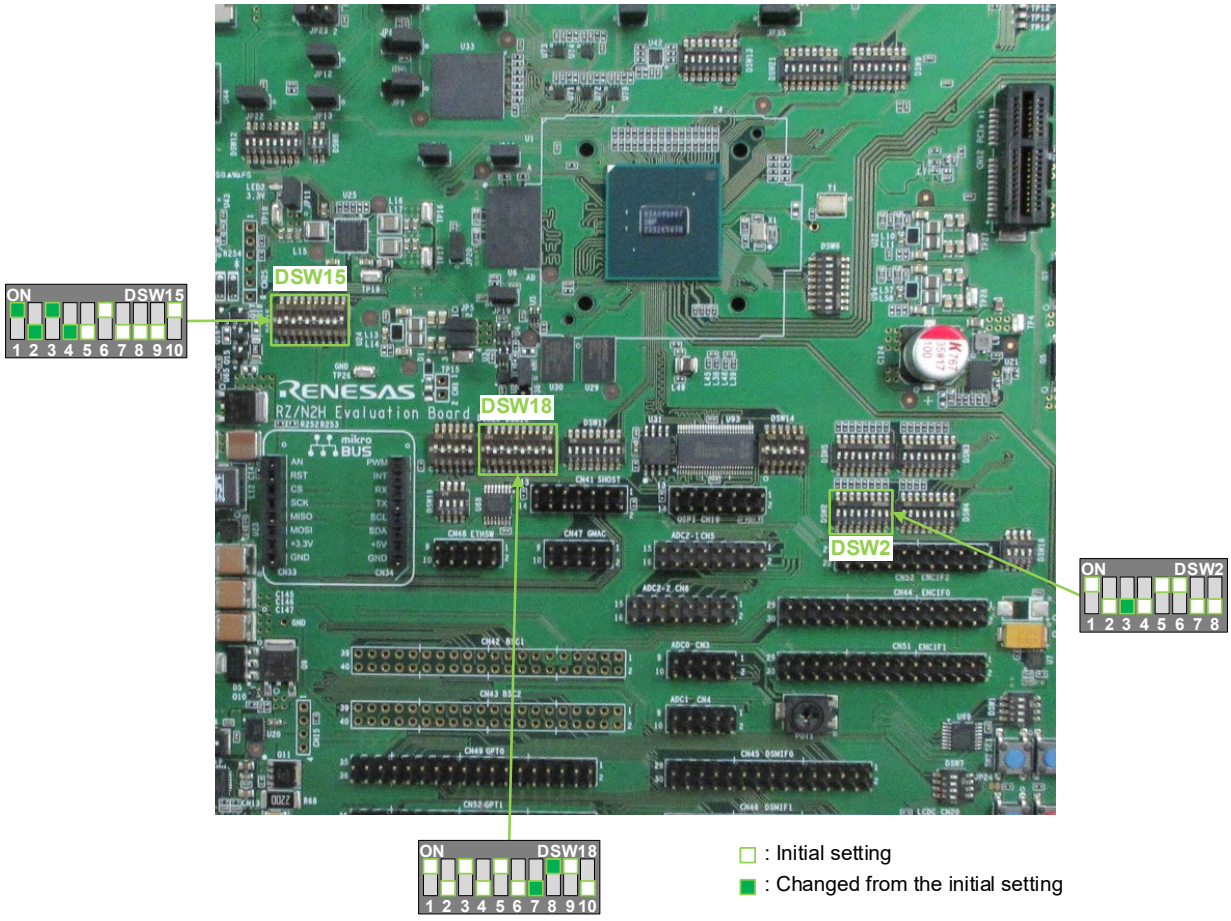


Figure 7-36 Switch Settings When Using GMAC (CN47)

Table 7-45 Signal Connections of BSC1 (CN42)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P14_0_HEADER_BSC_A0_RS485_DE3_LCDC_IRQ5	P14_0	A8	—
2	p3v3	—	—	—
3	P10_4_HEADER_BSC_A1_LCDC_DATR4	P10_4	C5	—
4	P33_2_VDD1833_3_HEADER_BSC_A16	P33_2*1	L20	DSW5-8: OFF
5	P10_5_HEADER_BSC_A2_LCDC_DATR5	P10_5	B4	—
6	P33_3_VDD1833_3_HEADER_BSC_A17_PCIE_RST OUT0B	P33_3*2	M20	DSW5-8: OFF, DSW9-5: OFF, DSW9-6: ON
7	P10_6_HEADER_BSC_A3_LCDC_DATR6_PCIEx1_P RSNT_IRQ0_CLKREQ	P10_6	A3	—
8	P33_4_VDD1833_3_HEADER_BSC_A18_PCIE_RST OUT1B	P33_4*2	N20	DSW5-8: OFF, DSW9-7: OFF, DSW9-8: ON
9	P10_7_HEADER_BSC_A4_LCDC_DATR7_PCIx4_PR SNT_IRQ9_CLKREQ	P10_7	A4	—
10	P33_5_VDD1833_3_HEADER_BSC_A19	P33_5*1	N21	DSW5-8: OFF
11	GROUND	—	—	—
12	P33_6_VDD1833_3_HEADER_BSC_A20	P33_6*1	M21	DSW5-8: OFF
13	P11_0_HEADER_BSC_A5_LCDC_DATG0	P11_0*3	A5	DSW12-3: ON, DSW12-4: OFF
14	P33_7_VDD1833_3_HEADER_BSC_A21_MikroBUS_ SCK	P33_7*1	L23	DSW5-8: OFF
15	P17_4_HEADER_BSC_A6	P17_4*1	E13	DSW5-3: OFF
16	P34_0_VDD1833_3_HEADER_BSC_A22_MikroBUS_ MOSI	P34_0*1	L22	DSW5-8: OFF
17	P17_5_HEADER_BSC_A7	P17_5	F11	—
18	P34_1_VDD1833_3_HEADER_BSC_A23_MikroBUS_ MISO	P34_1*1	K20	DSW5-8: OFF
19	P18_0_HEADER_BSC_A8_LCDC_DATB1_XSPI1_IR Q7	P18_0	F12	—
20	P27_0_P34_6_BSC_CS5#	P27_0*3	D22	DSW13-3: OFF, DSW13-4: ON, DSW21-6: ON, DSW21-7: OFF
		P34_6*2	K24	DSW5-8: OFF, **DSW21-6: OFF, DSW21-7: ON**
21	P18_1_HEADER_BSC_A9_LCDC_DATB2	P18_1*3	B12	DSW18-9: OFF, DSW18-10: ON
22	P34_2_VDD1833_3_HEADER_BSC_A24_MikroBUS_ CS	P34_2*1	K22	DSW5-8: OFF
23	P18_2_HEADER_BSC_A10_LCDC_DATB3_SEI	P18_2	C12	—
24	P34_3_VDD1833_3_HEADER_BSC_A25	P34_3*1	L21	DSW5-8: OFF
25	P18_3_HEADER_BSC_A11_LCDC_DATB4	P18_3	A13	—
26	P14_4_P31_5_BSC_DACK	P14_4*3	B9	**DSW20-3: ON, DSW20-4: OFF**
		P31_5*2	J23	DSW5-7: OFF, DSW20-3: OFF, DSW20-4: ON
27	P18_4_HEADER_BSC_A12_LCDC_DATB5	P18_4	B13	—
28	P14_3_P31_4_BSC_DREQ	P14_3*2	C10	DSW5-3: OFF, DSW18-5: OFF, DSW18-6: ON, **DSW20-1: ON, DSW20-2: OFF**
		P31_4*2	J21	DSW5-7: OFF, DSW20-1: OFF, DSW20-2: ON
29	GROUND	—	—	—

30	P14_2_HEADER_BSC_BS#_LCDC_DATG2_MikroBUS_RX	P14_2	E9	—
31	P18_5_HEADER_BSC_A13_LCDC_DATB6	P18_5	A12	—
32	P10_2_HEADER_BSC_CS0#_LCDC_DATR2_PCIEx1_IRQ1_WAKE	P10_2	B3	—
33	P18_6_HEADER_BSC_A14_LCDC_DATB7	P18_6	C13	—
34	P26_6_P34_4_BSC_CS2#	P26_6*3	C22	DSW21-1: OFF, DSW21-2: ON, DSW21-3: OFF
		P34_4*2	K23	DSW5-8: OFF, **DSW21-1: ON, DSW21-2: OFF, DSW21-3: ON**
35	P18_7_PSW_IRQ4_HEADER_BSC_A15_ETHSW_PTPOUT3	P18_7	F13	—
36	P26_7_P34_5_BSC_CS3#	P26_7*3	E22	DSW13-1: OFF, DSW13-2: ON, DSW21-4: ON, DSW21-5: OFF
		P34_5*2	K21	DSW5-8: OFF, **DSW21-4: OFF, DSW21-5: ON**
37	NC	—	—	—
38	P14_1_HEADER_BSC_RD/WR#_LCDC_DATG1	P14_1	C9	—
39	P10_3_HEADER_BSC_RD#_LCDC_DATR3	P10_3	C3	—
40	P14_5_P31_6_BSC_TEND	P14_5*3	D9	**DSW20-5: ON, DSW20-6: OFF**
		P31_6*3	J20	DSW18-7: OFF, DSW18-8: ON, DSW20-5: OFF, DSW20-6: ON

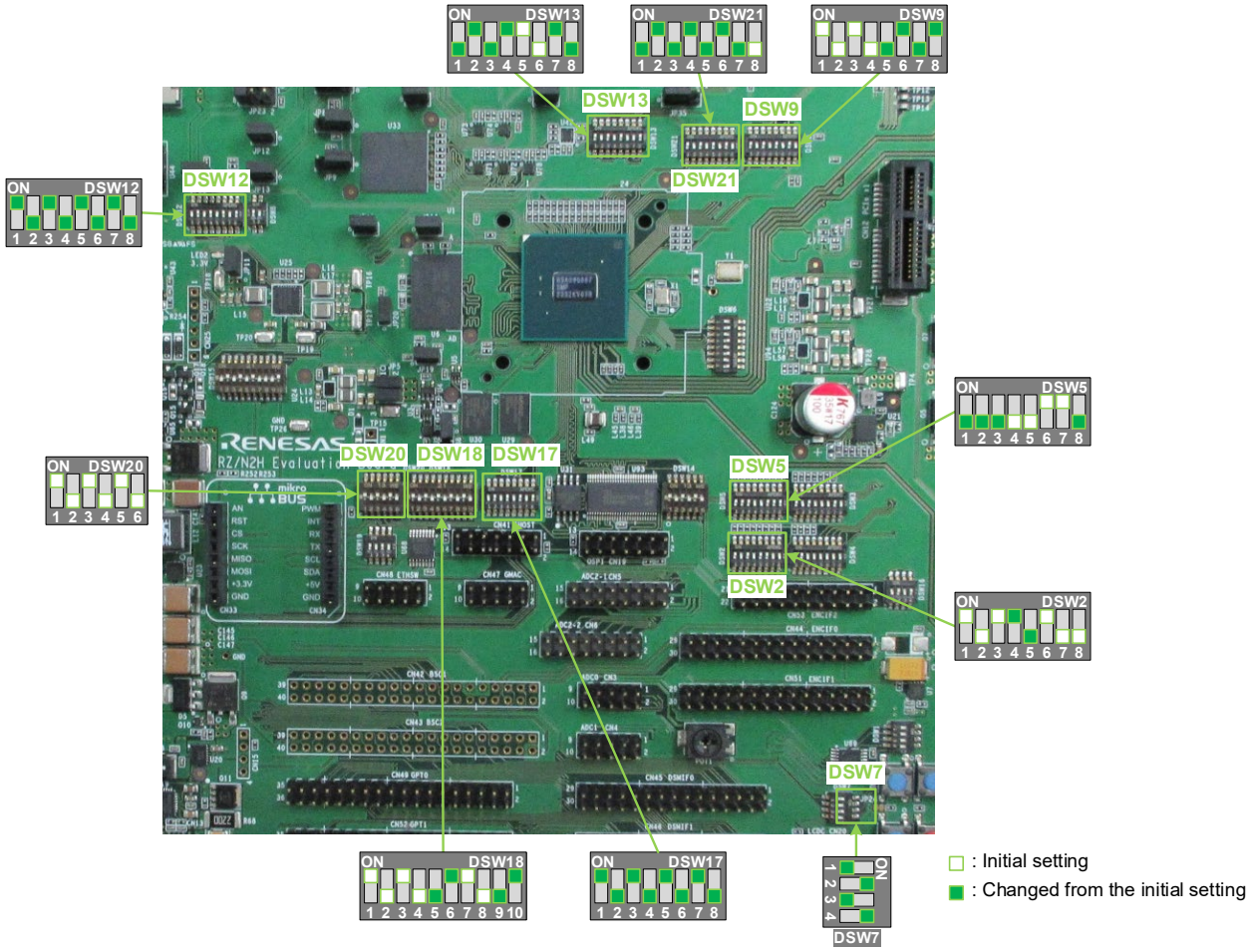
Notes: 1. Connected via the bus switch IC.
2. Connected via the bus switch IC and DIP switch.
3. Connected via the DIP switch.

Table 7-46 Signal Connections of BSC2 (CN43)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P00_0_HEADER_BSC_D0	P00_0*1	AB13	DSW5-8: OFF, DSW2-5: OFF
2	P08_6_HEADER_BSC_CKIO	P08_6*2	AD2	DSW5-3: OFF
3	P00_1_HEADER_BSC_D1	P00_1*1	AA13	DSW5-8: OFF, DSW2-5: OFF
4	P12_2_HEADER_BSC_D18_PMOD1_GPIO1	P12_2*3	E8	DSW5-1: OFF, DSW5-2: OFF
5	P00_2_HEADER_BSC_D2	P00_2*1	W12	DSW5-8: OFF, DSW2-5: OFF
6	P12_3_HEADER_BSC_D19_PMOD1_GPIO2	P12_3*3	F7	DSW5-1: OFF, DSW5-2: OFF
7	P00_3_HEADER_BSC_D3	P00_3*4	AD13	DSW12-1: ON, DSW12-2: OFF
8	P12_4_HEADER_BSC_D20_PMOD2_RXD2	P12_4*3	B8	DSW5-1: OFF, DSW5-2: OFF
9	P00_4_PSW_IRQ3_HEADER_BSC_D4	P00_4	AC13	—
10	P12_5_HEADER_BSC_D21_PMOD2_TXD2	P12_5*3	D7	DSW5-1: OFF, DSW5-2: OFF
11	GROUND	—	—	—
12	P12_6_HEADER_BSC_D22_PMOD2_RTS2#	P12_6*3	D6	DSW5-1: OFF, DSW5-2: OFF
13	P02_5_HEADER_BSC_D5	P02_5*4	AD10	DSW17-7: ON, DSW17-8: OFF
14	P12_7_HEADER_BSC_D23_PMOD2_CTS2#_PCIx4_IRQ2_WAKE	P12_7*3	B6	DSW5-1: OFF, DSW5-2: OFF
15	P02_6_HEADER_BSC_D6	P02_6*4	AB10	DSW17-5: ON, DSW17-6: OFF
16	P13_0_HEADER_BSC_D24_PMOD1_RSPCK3	P13_0*3	B7	DSW5-1: OFF, DSW5-2: OFF
17	P02_7_HEADER_BSC_D7	P02_7*4	AC9	DSW17-3: ON, DSW17-4: OFF
18	P13_1_HEADER_BSC_D25_PMOD1_MOSI3	P13_1*3	C6	DSW5-1: OFF, DSW5-2: OFF
19	P03_0_HEADER_BSC_D8	P03_0*4	AD9	DSW17-1: ON, DSW17-2: OFF
20	P17_6_HEADER_BSC_WE2#_LCDC_DATG7_ETHSW_PTPOUT0	P17_6	D12	—
21	P03_1_HEADER_BSC_D9	P03_1*4	Y9	DSW12-7: ON, DSW12-8: OFF
22	P13_2_HEADER_BSC_D26_PMOD1_MISO3	P13_2*3	F8	DSW5-1: OFF, DSW5-2: OFF
23	P03_2_HEADER_BSC_D10	P03_2*4	AB9	DSW12-5: ON, DSW12-6: OFF
24	P13_3_HEADER_BSC_D27_PMOD1_SSL30	P13_3	F9	—
25	P03_3_HEADER_BSC_D11_XSPI1_IRQ13	P03_3*4	AA9	DSW7-1: OFF, DSW7-2: ON
26	P13_4_HEADER_BSC_D28	P13_4*5	A6	DSW2-4: ON
27	P03_4_HEADER_BSC_D12	P03_4*4	W9	DSW7-3: OFF, DSW7-4: ON
28	P13_5_HEADER_BSC_D29_RS485_TXD3	P13_5	C7	—
29	GROUND	—	—	—
30	P13_6_HEADER_BSC_D30_PMOD2_GPIO1	P13_6	E6	—
31	P09_4_HEADER_BSC_D13_LCDC_CLK	P09_4	A2	—
32	P13_7_HEADER_BSC_D31	P13_7*4	A7	DSW13-7: ON, DSW13-8: OFF
33	P09_5_HEADER_BSC_D14_LCDC_HSYNC	P09_5	B1	—
34	P10_1_HEADER_BSC_WAIT#_LCDC_DATR1_MikroBUS_PWM	P10_1	B2	—
35	P09_6_HEADER_BSC_D15_LCDC_VSYNC_PMOD1_RST	P09_6	C1	—
36	P09_7_HEADER_BSC_WE0#_LCDC_DE_PMOD2_RST	P09_7	C4	—
37	P12_0_HEADER_BSC_D16	P12_0*3	C8	DSW5-1: OFF, DSW5-2: OFF
38	P10_0_HEADER_BSC_WE1#_LCDC_DATR0_MikroBUS_RST	P10_0	C2	—
39	P12_1_HEADER_BSC_D17	P12_1*3	E7	DSW5-1: OFF, DSW5-2: OFF

40	P17_7_HEADER_BSC_WE3#/AH#_LCDC_DATA TB0_ETHSW_PTPOUT1	P17_7	E12	—

Notes: 1. Connected via the bus switch IC.
2. Connected via the bus switch IC and option link.
3. Connected via the level shifter IC with an enable function.
4. Connected via the DIP switch.
5. Connected via the level shifter IC.



- Using P27_0 as P27_0_P34_6_BSC_CS5#
- Using P14_4 as P14_4_P31_5_BSC_DACK
- Using P14_3 as P14_3_P31_4_BSC_DREQ
- Using P26_6 as P26_6_P34_4_BSC_CS2#
- Using P26_7 as P26_7_P34_5_BSC_CS3#
- Using P14_5 as P14_5_P31_6_BSC_TEND

Figure 7-37 Switch Settings When Using BSC1 (CN42) and BSC2 (CN43)

Table 7-47 Signal Connections of ADC0 (CN3)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	VCC08_AVDD_ADC0	—	—	—
2	AN000_V18ADC0_AD_HEADER	—	R24*	DSW6-1: ON, DSW6-2: OFF
3	AVSS_ADC0	—	—	—
4	AN001_V18ADC0_AD_HEADER	—	T24	—
5	AVSSIO_ADC0	—	—	—
6	AN002_V18ADC0_AD_HEADER	—	R23	—
7	VCC18_AVDDIO_ADC0	—	—	—
8	AN003_V18ADC0_AD_HEADER	—	T23	—
9	VCC18_AVDDREF_ADC0	—	—	—
10	AVSS_ADC0	—	—	—

Note: Connected via the DIP switch.

Table 7-48 Signal Connections of ADC1 (CN4)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	VCC08_AVDD_ADC1	—	—	—
2	AN100_V18ADC1_AD_HEADER	—	U23*	DSW6-3: ON, DSW6-4: OFF
3	AVSS_ADC1	—	—	—
4	AN101_V18ADC1_AD_HEADER	—	V24*	DSW6-5: ON, DSW6-6: OFF
5	AVSSIO_ADC1	—	—	—
6	AN102_V18ADC1_AD_HEADER	—	V23*	DSW6-7: ON, DSW6-8: OFF
7	VCC18_AVDDIO_ADC1	—	—	—
8	AN103_V18ADC1_AD_HEADER	—	U24	—
9	VCC18_AVDDREF_ADC1	—	—	—
10	AVSS_ADC1	—	—	—

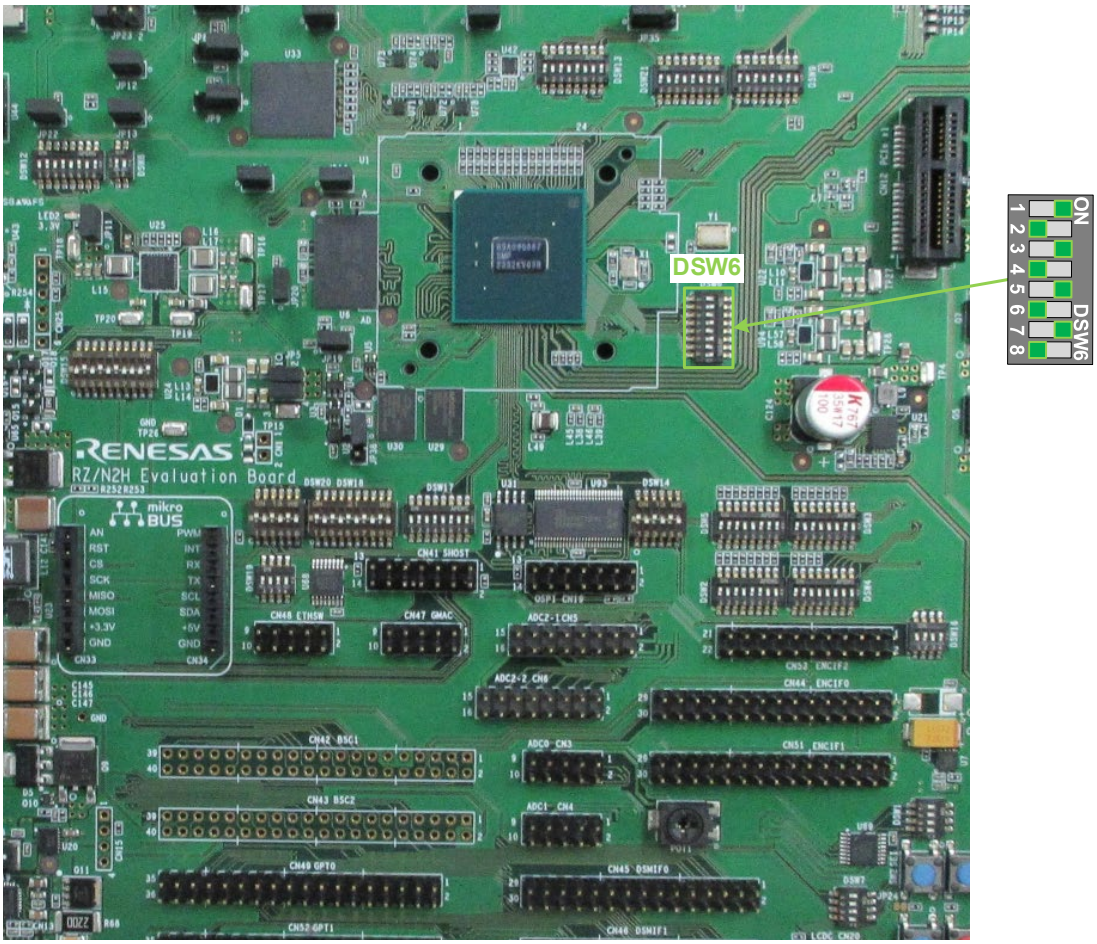
Note: Connected via the DIP switch.

Table 7-49 Signal Connections of ADC2_1 (CN5)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	AN200_V18ADC2_AD_HEADER	—	AA24	—
2	VCC08_AVDD_ADC2	—	—	—
3	AN201_V18ADC2_AD_HEADER	—	AA23	—
4	AVSS_ADC2	—	—	—
5	AN202_V18ADC2_AD_HEADER	—	Y24	—
6	AVSSIO_ADC2	—	—	—
7	AN203_V18ADC2_AD_HEADER	—	AB22	—
8	VCC18_AVDDIO_ADC2	—	—	—
9	AN204_V18ADC2_AD_HEADER	—	AC23	—
10	VCC18_AVDDREF_ADC2	—	—	—
11	AN205_V18ADC2_AD_HEADER	—	AD22	—
12	AVSS_ADC2	—	—	—
13	AN206_V18ADC2_AD_HEADER	—	W23	—
14	AVSS_ADC2	—	—	—
15	AN207_V18ADC2_AD_HEADER	—	AC24	—
16	AVSS_ADC2	—	—	—

Table 7-50 Signal Connections of ADC2_2 (CN6)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	AN208_V18ADC2_AD_HEADER	—	Y23	—
2	VCC08_AVDD_ADC2	—	—	—
3	AN209_V18ADC2_AD_HEADER	—	Y22	—
4	AVSS_ADC2	—	—	—
5	AN210_V18ADC2_AD_HEADER	—	W24	—
6	AVSSIO_ADC2	—	—	—
7	AN211_V18ADC2_AD_HEADER	—	AC22	—
8	VCC18_AVDDIO_ADC2	—	—	—
9	AN212_V18ADC2_AD_HEADER	—	AB24	—
10	VCC18_AVDDREF_ADC2	—	—	—
11	AN213_V18ADC2_AD_HEADER	—	AA22	—
12	AVSS_ADC2	—	—	—
13	AN214_V18ADC2_AD_HEADER	—	AD23	—
14	AVSS_ADC2	—	—	—
15	AVSS_ADC2	—	—	—
16	AVSS_ADC2	—	—	—



□ : Initial setting
■ : Changed from the initial setting

Figure 7-38 Switch Settings When Using ADC0 (CN3) and ADC1 (CN4)

7.22 Test Pins

This board is equipped with the test pins listed in Table 7-51 and Figure 7-39.

Table 7-51 List of Test Pins

Reference	Description	Reference	Description
TP1	For monitoring EXTCLKIN (DNF)	TP16	For monitoring the p1v1 power supply
TP2	For monitoring the cVBUS power supply	TP17	For monitoring the p1v8 power supply
TP3	For monitoring the P3V3_USB_PD power supply	TP18	For monitoring the p3v3 power supply
TP4	For monitoring the P12V power supply	TP19	For monitoring the ETH_VDD10 power supply
TP5	For monitoring the p5v0s power supply	TP20	For monitoring the ETH_VDD25 power supply
TP6	For monitoring the P31_6_ESC_LEDRUN signal	TP21	GROUND (DNF)
TP7	For monitoring the P18_1_ESC_LEDERR signal	TP22	GROUND (DNF)
TP8	For monitoring the P22_7_ESC_LINKACT0 signal	TP23	GROUND (DNF)
TP9	For monitoring the P23_0_ESC_LINKACT1 signal	TP24	GROUND (DNF)
TP10	For monitoring the P14_3_ESC_LINKACT2 signal	TP25	GROUND (DNF)
TP11	For monitoring the P14_6_USER_LED0 signal	TP26	GROUND
TP12	For monitoring the P14_7_USER_LED1 signal	TP27	For monitoring the PCIE3V3_x4 power supply
TP13	For monitoring the P02_7_USER_LED2 signal	TP28	For monitoring the PCIE3V3_x1 power supply
TP14	For monitoring the P03_0_USER_LED3 signal	TP29	GROUND (DNF)
TP15	For monitoring the p0v8 power supply	TP32	For monitoring the 15V power supply

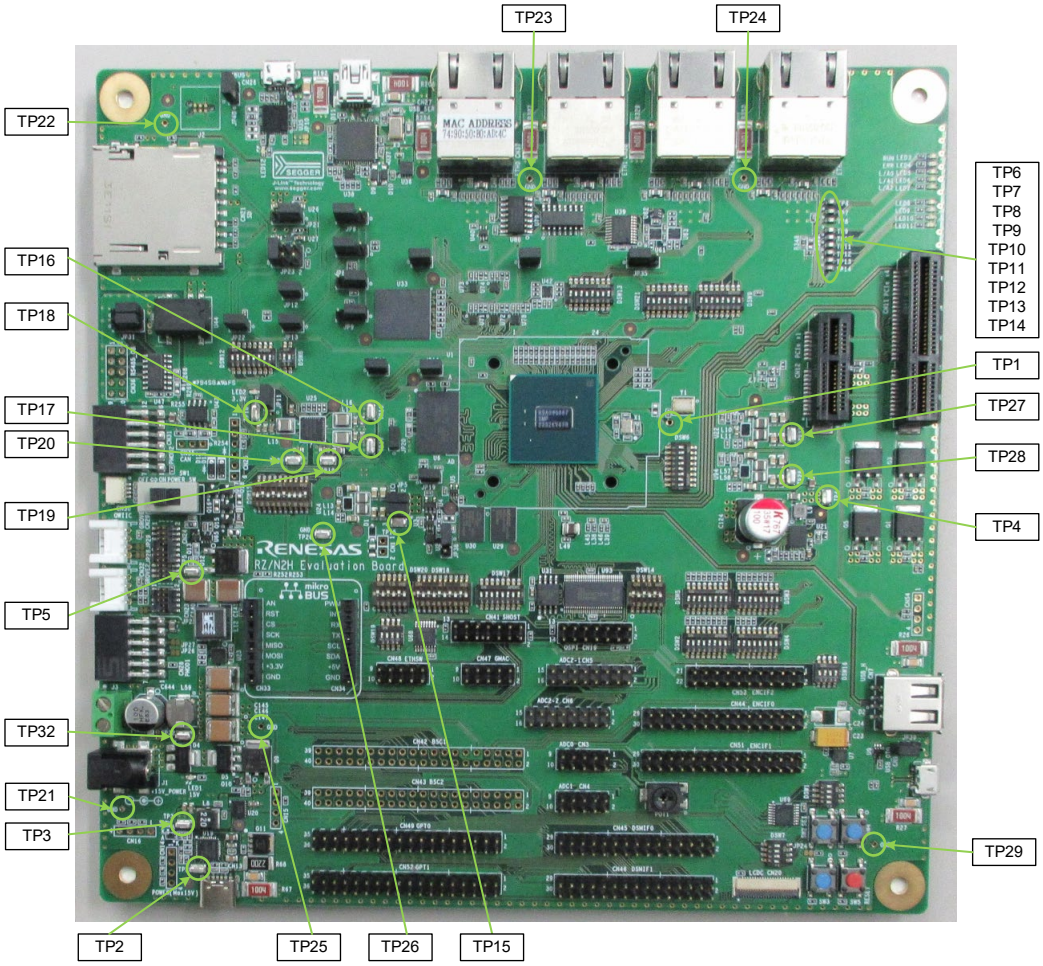


Figure 7-39 Arrangement of Test Pins

8. Developing Code

8.1 Overview

The following methods for debugging code for this device are available.

- Connect this board to a PC via J-Link™ OB, which is a development tool from Segger and mounted on this board.
- Connect this board to a PC via an emulator from a given company.

For more details on individual emulators, refer to the Web sites of the manufacturers.

8.2 Supported Modes

This board supports a variety of boot modes. The possible mode settings are shown in section 6.3.1. For detailed information on the microprocessor, such as operating modes and registers, refer to the RZ/T2H and RZ/N2H Groups User's Manual: Hardware.

Mode settings should only be changed while the power is turned off to avoid causing damage to the microprocessor.

8.3 Address Spaces

For details on the usable address spaces determined by the operating mode of the microprocessor, refer to the RZ/T2H and RZ/N2H Groups User's Manual: Hardware.

9. Usage Notes

9.1 Handling of the XTALSEL Pin

Though the circuitry of this board is configured so that XTALSEL does not pass through any resistor when it is at the low level because it is to be switched by a switch during evaluation, operation with this circuit configuration is not guaranteed. When XTALSEL is to be set to the low level (selecting EXTCLKIN as the main clock source) on a customer’s board, connect it to VSS via a resistor according to the descriptions in the RZ/T2H and RZ/N2H Groups User’s Manual: Hardware (R01UH1039EJ).

9.2 Use of the RGB-HDMI Conversion Board

Warning

When this board is used with an RGB-HDMI conversion board connected to the LCD interface, the EMC emission may exceed the restriction on class A equipment according to EN55032:2015. Therefore, special care must be taken, such as keeping this board away from EMC-sensitive equipment. If interference does occur, separation by a longer distance may be required. In such cases, additional appropriate measures should be taken on the responsibility of the user and operator of the equipment.

10. Support

For details on the RZ/N2H microprocessors, refer to the RZ/T2H and RZ/N2H Groups User's Manual: Hardware (R01UH1039EJ).

Online technical support and information are available from this Web page: https://www.renesas.com/.

Technical Contact Details

America: techsupport.america@renesas.com

Europe: https://www.renesas.com/en-eu/support/contact.html

Global & Japan: https://www.renesas.com/support/contact.html

General information on Renesas microprocessors can be found on the Renesas website at: https://www.renesas.com/

Design and Manufacturing Information

The design and manufacturing information for this board "RZ/N2H Evaluation Board Design Package" can be obtained from https://www.renesas.com/rzn2h-evkit.

- File Name：rzn2h-evaluation-board-v1-designpackage.zip
- File Contents

Table 10-1 Contents of the RZ/N2H Evaluation Board Design Package

File Type	Content	File/Folder Name
File (txt)	Readme	Readme for schematic.txt
File (PDF)	Schematics	rzn2h-evaluation-board-v1-schematic.pdf
File (PDF)	Mechanical Drawing	rzn2h-evaluation-board-v1-mechdwg.pdf
File (PDF)	3D Drawing	rzn2h-evaluation-board-v1-3d.pdf
File (xlsx)	Bill of materials (BOM)	rzn2h-evaluation-board-v1-BOM.xlsx
Folder	Manufacturing Files	rzn2h-evaluation-board-Manufacturing Files
Folder	Design Files	rzn2h-evaluation-board-Design Files

11. Appendix

The arrangements of individual components on this board are shown in this appendix.

CN26
CN27
R206
J2
JP10
U35
U37
X3
R192
R284
CN37
CN38
CN39
CN40
R307
R329
R352
CN21
JP21
JP23
JP6
JP7
JP8
JP9
U80
U79
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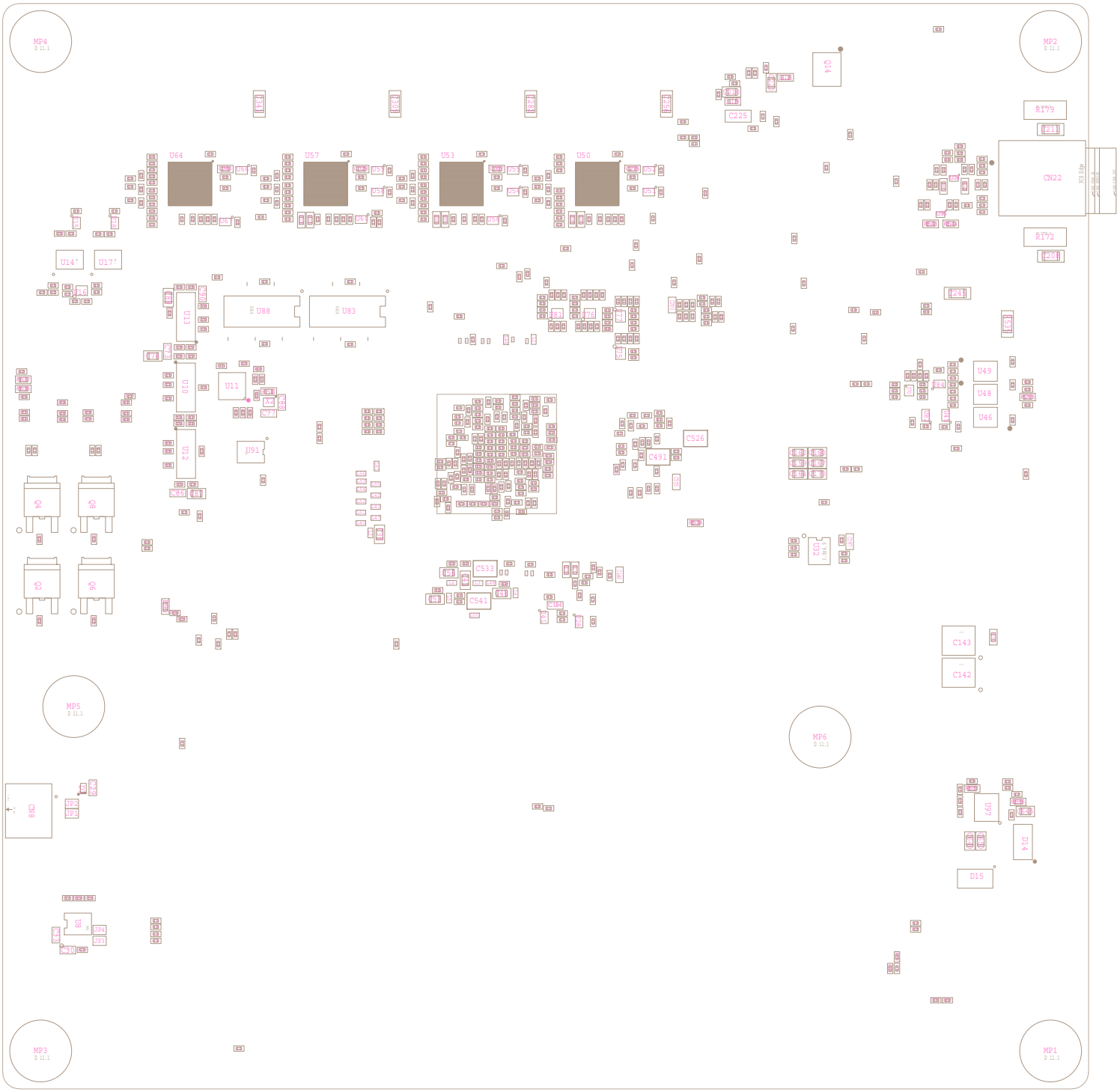
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