User's Manual

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RZ/T2H Group

RZ/T2H Evaluation Board User's Manual

RZ/T Series for Real-Time Control

RZ Family

64-Bit & 32-Bit Arm®-Based High-End MPUs

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Precautions

This product is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

• Ensure attached cables do not lie across the equipment.

• Reorient the receiving antenna.

• Increase the distance between the equipment and the receiver.

• Connect the equipment into an outlet on a circuit different from that which the receiver is connected.

• Power down the equipment when not in use.

• Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

• The user is advised that mobile phones should not be used within 10 m of the product when in use.

• The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

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How to Use This Manual

1. Purpose and Target Readers

The intention of this manual is to assist users in understanding the hardware functionality and electrical characteristics of the evaluation board in overview. The target users of this manual are engineers designing sample code that runs on the platform of the evaluation board, with the use of various peripheral devices.

Though this manual includes an overview of the functionality of the evaluation board, it is not intended to be a guide for embedded programming or hardware design.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Handling Precautions section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/T2H Evaluation Board. Be sure to refer to the latest versions of these documents. The newest versions of the listed documents are available on the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual	Explanation of the hardware specifications of the evaluation board	RZ/T2H Evaluation Board User's Manual	R20UT5405EJ0100 (this manual)
Quick start guide	Explanation of the flow from turning on the power to confirming initial operation	RZ/T2H Evaluation Board Quick Start Guide	R20QS0055EJ
User's manual for the hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and descriptions of operation	RZ/T2H and RZ/N2H Groups User's Manual: Hardware	R01UH1039EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DIP	Dual In-line Package
DNF	Do Not Fit
EEPROM	Electronically Erasable Programmable Read Only Memory
ESC	EtherCAT Slave Controller
ESD	Electrostatic Discharge
EtherCAT	Ethernet for Control Automation Technology
GPT	General PWM Timer
I^2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
J-Link™	SEGGER debug probe
J-Link™ OB	SEGGER On-board debug probe
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MAC	Media Access Control
MCU	Micro Controller Unit
MPU	Micro Processor Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
PC	Personal Computer
PCB	Printed Circuit Board
POE	Port Output Enable
POEG	Port Output Enable for GPT
PWM	Pulse Width Modulation
RAM	Random Access Memory
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
ROM	Read Only Memory
SCI	Serial Communications Interface
SEI	System Error Interrupt
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Table of Contents

1. Overview

1.1 Purpose

This evaluation board (hereafter referred to as this board) is an evaluation tool for a Renesas microprocessor. This manual describes the technical elements of the hardware of this board in detail. The method for installing software and the debugging environment are explained in the quick start guide.

1.2 Features

This board has the following features.

- Programming of a Renesas microprocessor
- Debugging of user code
- User circuits for switches, LEDs, and potentiometers

This board is equipped with all of the circuits that are required for operating the microprocessor.

1.3 Board Specifications

Table 1-1 and Table 1-2 list the board specifications.

Table 1-1 Board Specifications (1)

Item	Specification
Microprocessor	Part No.: R9A09G077M44GBG*1
	Package: 729-pin FCBGA
	On-chip memory: 2 Mbytes of RAM
On-board memory	OctaFlash: 512 Mbits
	QSPI serial flash memory: 128 Mbits
	I^2C EEPROM: 16 Kbits
	LPDDR4: 8 Gbytes
	eMMC: 32 Gbytes
Input clocks	RZ/T2H main: 25 MHz
	PCIe: 25 MHz
	USB-to-serial conversion IC: 12 MHz
Power supplies	Power inputs: 15-V/3-A USB PD supporting type-C connector (CN46) 15-V/3-A power jack (CN47) for the AC adapter 24-V/3-A bipolar terminal block (CN90)
	Power-supply IC: 24-V input, 15-V output
	Power-supply IC: 15-V input, 12-V output
	Power-supply IC: 15-V input, 5-V output
	Power-supply IC: 5-V input, 3.3-V output
	Power-supply IC: 5-V input, 1.8-V output
	Power-supply IC: 5-V input, 1.1-V output
	Power-supply IC: 5-V input, 0.8-V output
	Power-supply IC: 5-V input, 2.5-V output (for Ethernet PHY)
	Power-supply IC: 5-V input, 1.0-V output (for Ethernet PHY)
Debugging interfaces	MIPI-10: 1.27-mm pitch, 10-pin box header (CN60)
	MIPI-20: 1.27-mm pitch, 20-pin box header (CN61)
	J-Link™ OB: USB micro-B (CN14)
Slide switch	Power-supply switch: Single-pole double-throw type × 1 (SW16)
DIP switches	Mode setting: 8 switches × 1
	Signal selection: 10 switches × 4, 8 switches × 4, 6 switches × 1, and 2 switches × 1
	User switch: 4 switches × 1
Push switches	Reset switch × 1
	User switch × 3
Potentiometer (for A/D conversion)	Single-turn type (10 kΩ)

LEDs	For the power supply: (yellow) × 1 and (green) × 1
	For the user: (green) × 6, (yellow) × 1, and (red) × 2 Among the above, (green) × 4 and (red) × 1 are also used for indicating the EtherCAT status.
	Ethernet status: (green) × 4 and (yellow) × 4 (built in to each RJ-45)
	J-Link™ OB status: (yellow) × 1
Ethernet ports	Connectors: RJ-45 × 4 (CN1, CN44, CN45, and CN59)
	PHY: Single-channel PHY × 4
USB	USB function: USB mini-B (CN79)
	USB host: USB type-A (CN80)
	USB micro-AB (CN33)*2

Notes: 1. Evaluation of the one-time programmable memory (OTP) is not possible with the device mounted on this product.
2. Cannot be used in this product.

Table 1-2 Board Specifications (2)

Item	Specification
CAN	Connector*: 2.54-mm pitch, 3 pins × 1 (CN55)
	CAN transceiver × 1
RS485	Connector*: 10 pins × 1 (CN58)
	RS485 transceiver × 1
	External RS485 expansion connector: 2.54-mm pitch, 8 pins × 1 (CN12)
USB-to-serial conversion interface	Connector: USB mini-B (CN34)
	Driver: FT2232HQ
Pmod™	PMOD-2A, 6A: 12-pin connector (CN50)
	PMOD-3A: 12-pin connector (CN49)
mikroBUS™	2.54-mm pitch, 8 pins × 2 (CN53 and CN54)
Grove	2.00-mm pitch, 4 pins × 2 (CN48 and CN51)
QWIIC	1.00-mm pitch, 4 pins × 1 (CN52)
Serial host interface	2.54-mm pitch, 14 pins × 1 (CN64)
LCDC	45-pin FPC connector × 1 (CN15)
SD	SD card slot × 1 (CN31) and microSD card slot × 1 (CN16)
PCIe	The selectable configurations are 1 lane × 2 ports or 2 lanes × 1 port and root complex or endpoint.
	Connectors: 1 lane × 1 (CN8), 4 lanes × 1 (CN32, with only 2 lanes actually in use)
Pin headers (2.54-mm pitch)	ENCIF: 30 pins × 2 (CN2 and CN3), 22 pins × 1 (CN10)
	DSMIF: 30 pins × 3 (CN18, CN21, and CN22), 10 pins × 1 (CN19)
	GPT: 36 pins × 3 (CN24, CN25, and CN26)
	ETHSW: 10 pins × 1 (CN20)
	GMAC: 6 pins × 1 (CN23)
	External bus*: 40 pins × 2 (CN13 and CN17)
	ADC: 10 pins × 2 (CN41 and CN42), 12 pins × 1 (CN43)

Note: The connector is not mounted on the product as shipped.

2. Power Supply

2.1 Specifications of Power Supply

This board has a USB type-C connector (CN46), a power jack (CN47), and a bipolar terminal block (CN90). Power can be supplied from any one of these. Table 2-1 lists the specifications of power supply.

Table 2-1 Specifications of Power Supply

Connector	Specifications and Supply Voltage
CN46	USB power delivery (USB PD) supporting type-C, 15-V/3-A DC*1
CN47	2.0-mm center-positive power jack, 15-V/3-A DC*2
CN90	5.08-mm pitch bipolar terminal block, 24-V/3-A DC*3

Notes: 1. When supplying power through CN46, always use an AC adapter for USB supporting 15 V/3 A.
2. Though some of our boards, such as Renesas Starter Kit, require a 12-V or 5-V power supply, in the case of supplying power to this board through CN47, always use a 15-V/3-A power supply and do not connect a 12-V or 5-V power supply.
3. When supplying power through CN90, always use a stabilized power source that is capable of supplying 24 V/3 A.

2.2 Methods for Turning the Power On and Off

This board is equipped with a power switch (POWER_SW slide switch). When turning the power on, connect the power to CN46, CN47, or CN90 with the power switch turned off, and then turn the power switch on to start the power supply. To end the supply of power, turn the power switch off and then disconnect the power cable from CN46, CN47, or CN90. Figure 2-1 shows the arrangement and manipulation method of the power switch.

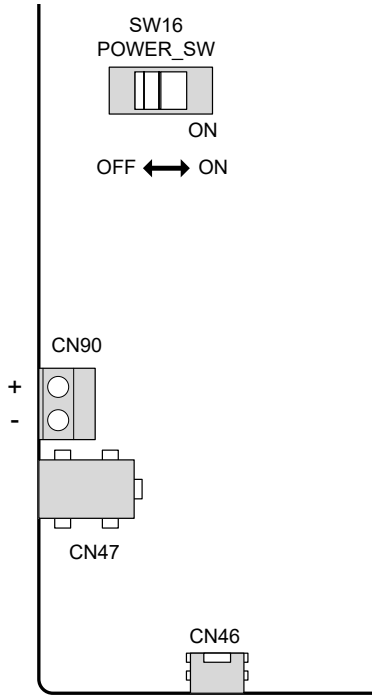


Figure 2-1 Arrangement and Method of Manipulating the Power Switch

2.3 Connectors for Current Measurement

This board has connectors for measuring currents, and each current value can be measured by inserting an ammeter between pins 1-2 of the given connector. Table 2-2 is a list of the connectors for measuring currents.

Table 2-2 List of Connectors for Current Measurement

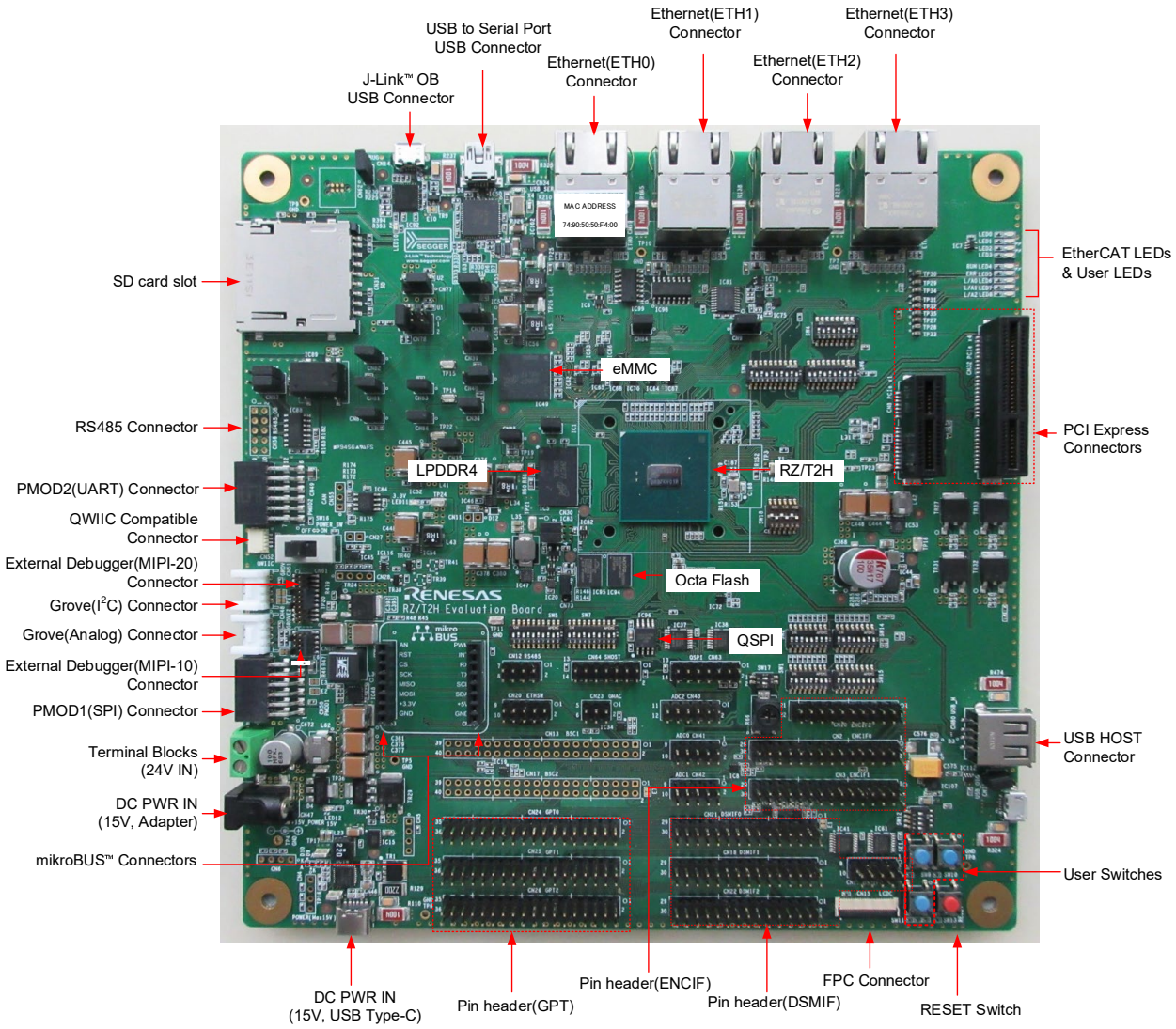
Connector	Purpose
CN30*	For measuring the current of the power supply (CPU0V8) line input to the 0.8-V power supply of the RZ/T2H
CN29	For measuring the current of the power supply (CPU1V1) line input to the 1.1-V power supply of the RZ/T2H
CN35	For measuring the current of the power supply (CPU1V8) line input to the 1.8-V power supply of the RZ/T2H
CN36	For measuring the current of the power supply (CPU3V3) line input to the 3.3-V power supply of the RZ/T2H
CN81	For measuring the current of the power supply (CPU_VCC1833_0) line input to the VCC1833_0 power supply of the RZ/T2H
CN82	For measuring the current of the power supply (CPU_VCC1833_1) line input to the VCC1833_1 power supply of the RZ/T2H
CN83	For measuring the current of the power supply (CPU_VCC1833_2) line input to the VCC1833_2 power supply of the RZ/T2H
CN84	For measuring the current of the power supply (CPU_VCC1833_3) line input to the VCC1833_3 power supply of the RZ/T2H
CN85	For measuring the current of the power supply (CPU_VCC1833_4) line input to the VCC1833_4 power supply of the RZ/T2H
CN86	For measuring the current of the power supply (CPU_VCC1833_5) line input to the VCC1833_5 power supply of the RZ/T2H
CN87	For measuring the current of the power supply (CPU_VCC1833_6) line input to the VCC1833_6 power supply of the RZ/T2H

Note: This is a 4-pin connector. To measure the current, insert an ammeter between pins 1-3 and 2-4.

3. Board Layout

3.1 Component Layouts

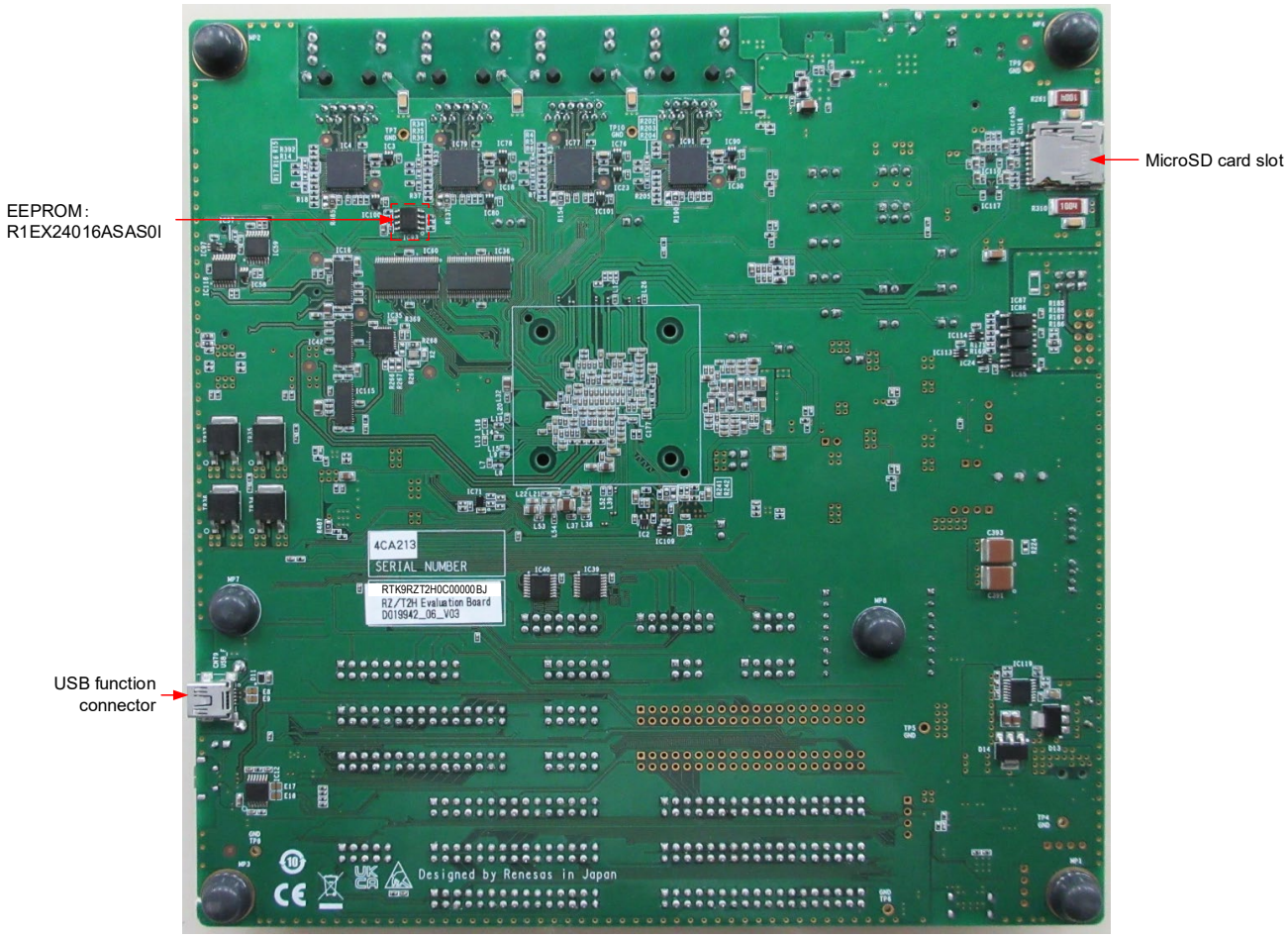
Figure 3-1 and Figure 3-2 show the component layouts on the top and on the soldered side of this board.



Notes: 1. For the details of each function, refer to chapter 7.

2. The MAC address shown in the figure is an example. Use a unique MAC address when running Ethernet software.

Figure 3-1 Board Layout (Top Side)



Note: The serial number (3KA0162) is an example.

Figure 3-2 Board Layout (Soldered Side)

3.2 Board Dimensions

Figure 3-3 shows the board dimensions and positions of connectors on this board. The through-hole connectors of pin headers are placed on a 2.54-mm pitch grid.

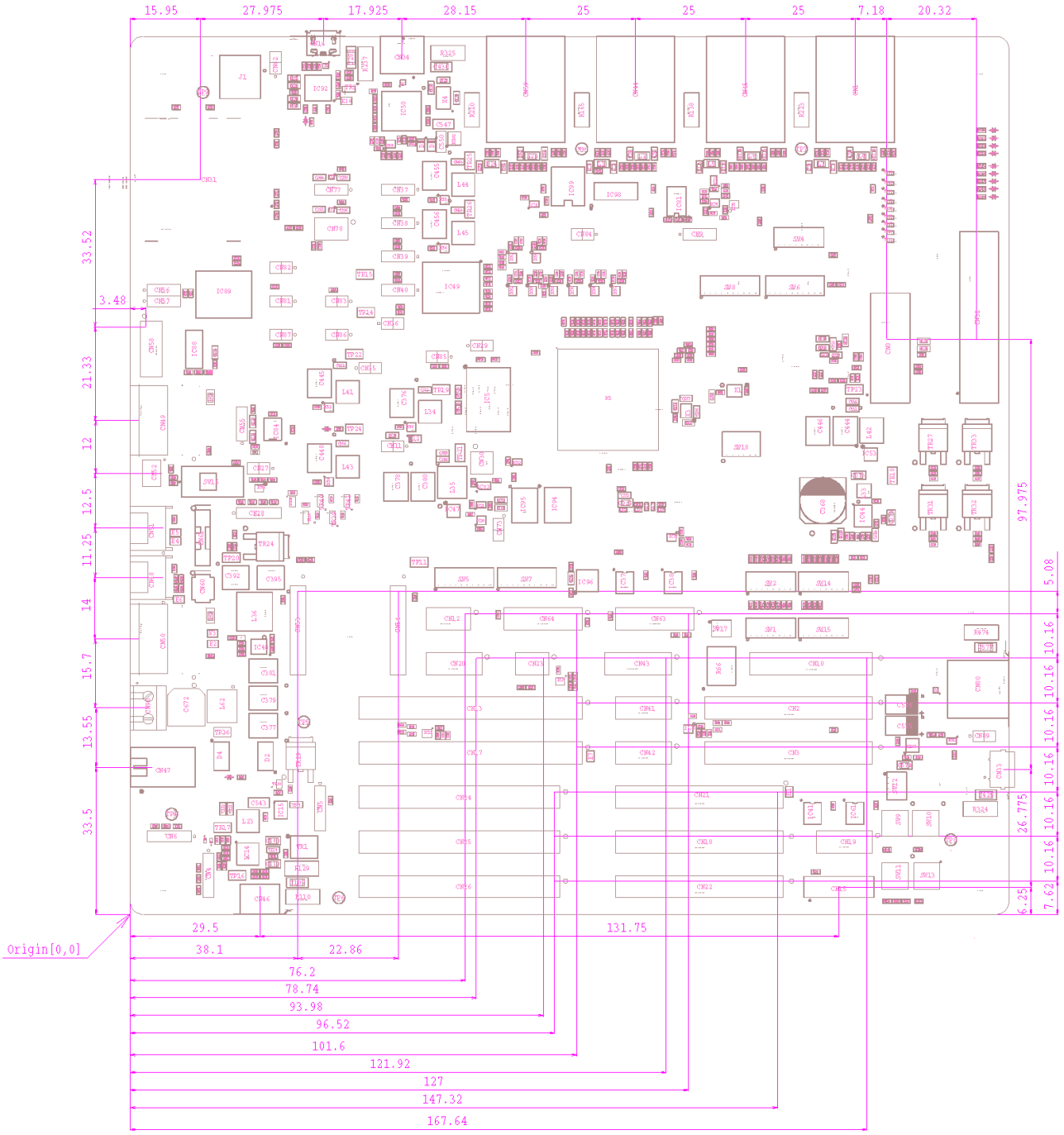


Figure 3-3 Board Dimensions (Unit: mm)

3.3 Arrangement of Components

For the arrangement of components on this board, refer to "11. Appendix".

4. Connections

4.1 Internal Connections of the Board

Figure 4-1 shows the connections between components of this board and the RZ/T2H.

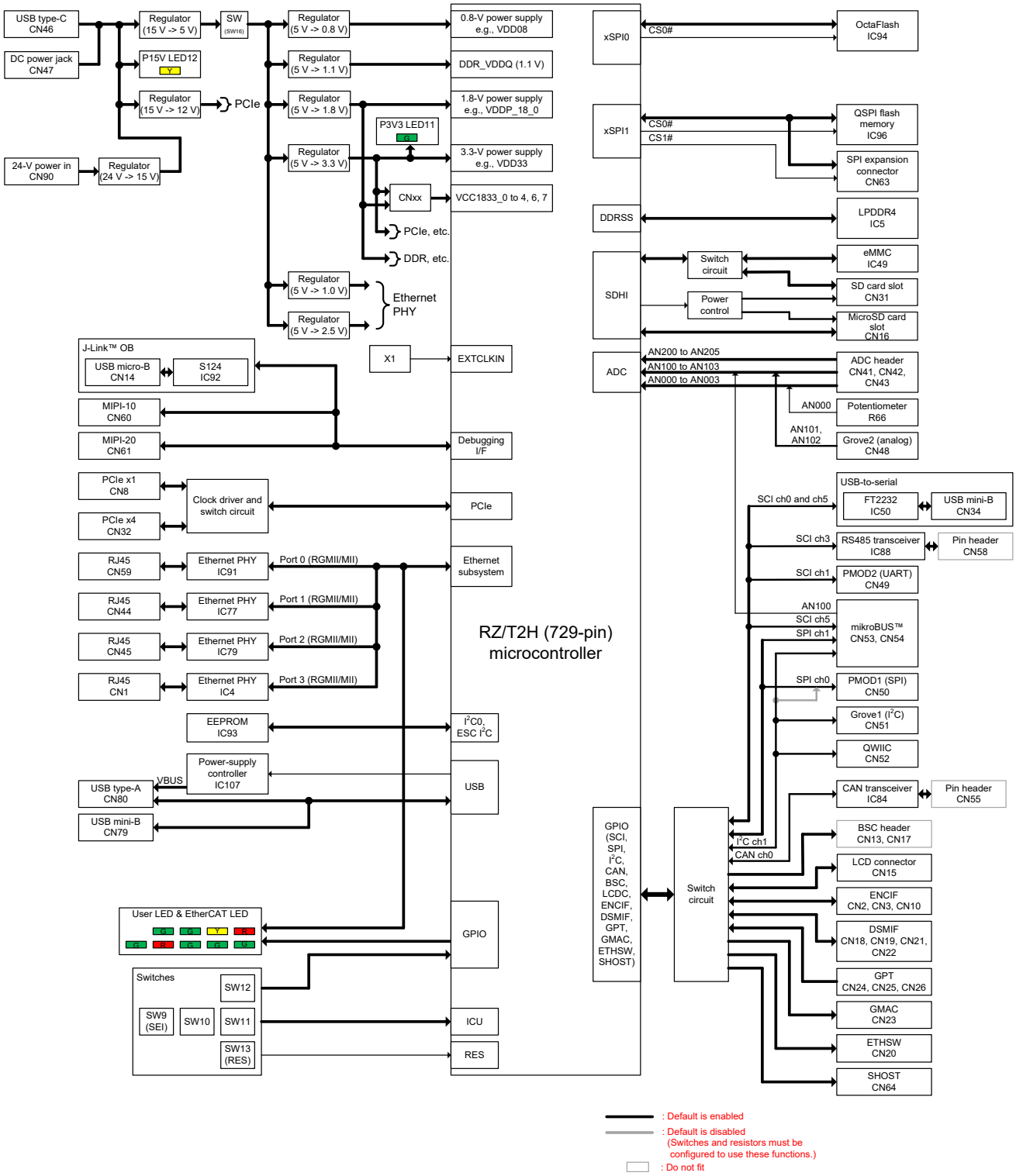


Figure 4-1 Internal Connections of the Board

4.2 Connections in the Debugging Environment

Figure 4-2 shows the connection between this board, the emulator, and the host PC. Figure 4-3 shows the connection between this board and the host PC when J-Link™ OB on this board is used.

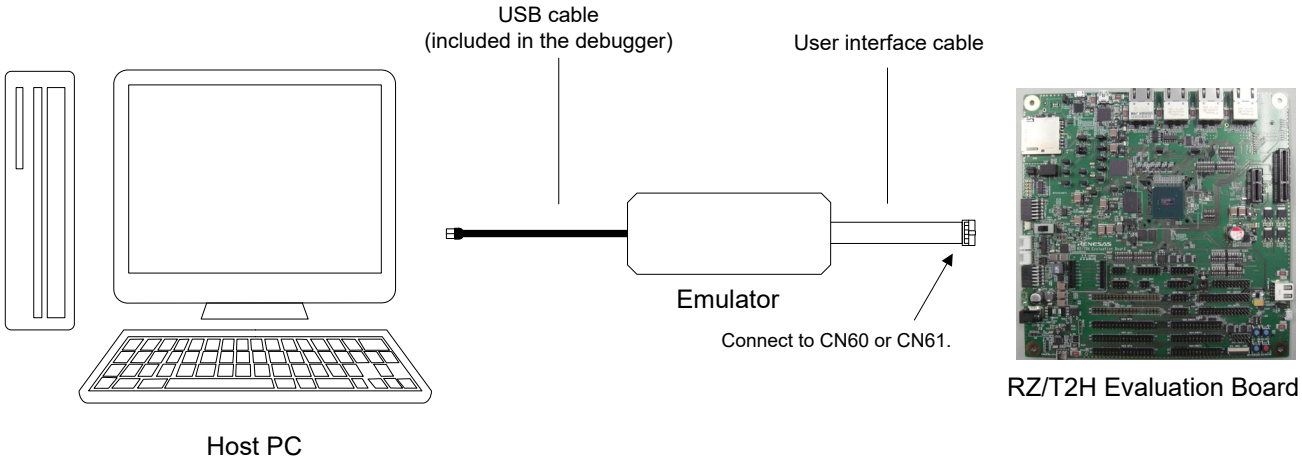


Figure 4-2 Connections in the Debugging Environment (with an Emulator)

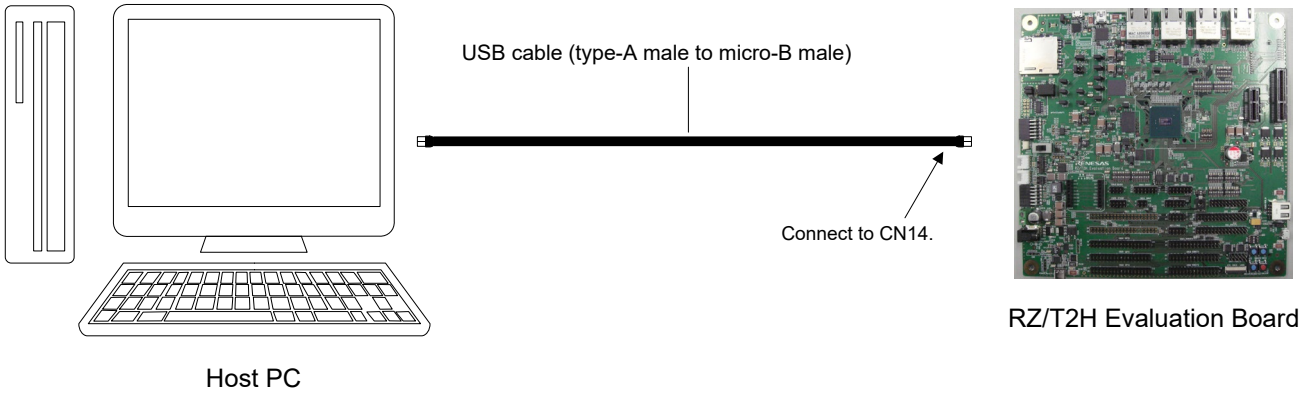


Figure 4-3 Connections in the Debugging Environment (with J-Link™ OB)

5. List of RZ/T2H Pin Functions

Table 5-1 to Table 5-27 are lists of the functions of RZ/T2H pins used on this board. **Text in bold blue type** in the tables indicates the settings at the time of shipment of the board and the functions available with those settings. However, a signal that is connected to multiple connectors can be used in only one of the connectors at a time.

Table 5-1 List of RZ/T2H Pin Function Selections (1)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
A1	VSS				
A2	P11_4/IRQ7/DE1/MCLK31/HDSL09_SMPL	**MCLK31**	**Clock of DSMIF**	**CN18-5**	
A3	P11_6/GTIOC05_0A/TST_OUT00/HDSL09_SEL1	**P11_6**	**GPIO/SSL for use with PMOD1**	**CN50-10**	
		GTIOC05_0A	**Input capture/output compare/PWM output pin**	**CN25-27**	
A4	P11_7/GTIOC05_0B/SI00#/HDSL09_MISO1	**GTIOC05_0B**	**Input capture/output compare/PWM output pin**	**CN25-28**	
A5	P10_1/IRQ7/WAIT#/MTIOC7D/GTIOC04_2B/GTIOC10_2B/SCK0/MDAT72/DISP_DATAR1/SI14#/HDSL08_LINK	**WAIT#**	**Wait signal of external bus**	**CN17-34**	
		MDAT72	**Data of DSMIF**	**CN22-14**	
		DISP_DATAR1	**Display data R1**	**CN15-40**	
A6	P10_6/IRQ0/A3/MTIOC0B/GTIOC05_0A/DE0/MCLK21/DISP_DATAR6/HDSL08_MOSI1/POUTA	**A3**	**Address A3 of external bus**	**CN13-7**	
		MCLK21	**Clock of DSMIF**	**CN21-25**	
		DISP_DATAR6	**Display data R6**	**CN15-35**	
A7	P14_0/IRQ5/A0/GTIOC06_4B/ETHSW_PTPOUT2/ESC_SYNC0/DE3/MCLK42/HDSL11_SMPL	**A0**	**Address A0 of external bus**	**CN13-1**	
		GTIOC06_4B	**Input capture/output compare/PWM output pin**	**CN26-12**	
		ETHSW_PTPOUT2	**Timer pulse output from ETHSW**	**CN20-5**	
		DE3	**DE of RS485**		**SW1-4: OFF**
A8	P13_6/D30/GTIOC06_3B/GTIOC04_3A/SS3#/CTS3#/RTS3#/SPI_SSL23/MCLK41/ENCIFDO13/TXDE09/HDSL10_MOSI2	**D30**	**Data D30 of external bus**	**CN17-30**	
		GTIOC06_3B	**Input capture/output compare/PWM output pin**	**CN26-10**	
		ENCIFDO13	**Data output from ENCIF**	**CN10-6**	
A9	P14_4/DACK/POE4#/GTIOC06_1B/GTIOC09_1B/GTIOC06_3A/CMTW0_TIC0/ESC_IRQ/SS4#/CTS4#/RTS4#/SD1_WP/DISP_DATAG4/MBX_HINT#/ENCIFDO00/TXDE00/HDSL11_MOSI1	**DACK**	**DMA acknowledge**	**CN13-26**	
		DISP_DATAG4	**Display data G4**	**CN15-29**	
		ENCIFDO00	**Data output from ENCIF**	**CN2-7**	
A10	P14_7/IRQ9/POE11#/GTIOC09_3A/CMTW0_TOC1/ESC_I2CDATA/IIC_SDA0/SD0_IOVS/MCLK32/SI02#/HDSL11_MISO2	**MCLK32**	**Clock of DSMIF**	**CN18-3**	
A11	P16_2/SCK5/MDAT51/SI03#/HDSL12_MOSI2	**MDAT51**	**Data of DSMIF**	**CN18-26**	

A12	P16_4/IRQ11/GTETRGSB/ESC_LINKACT1/TXD5/SDA5/MOSI5/TST_OUT04/HDSL13_SMPL	**TXD5**	**TXD5 of USB-to-serial conversion**		**SW8-7: ON, SW8-8: OFF**
		TXD5	TX for use with mikroBUS™	CN54-4	SW8-7: OFF, SW8-8: ON
A13	P17_0/IRQ12/GTIOC03_1B/SD1_DATA1/SI05#/HDSL13_MOSI1	**SD1_DATA1**	**Data DAT1 of SD1**	**CN16-8**	
A14	P17_5/A7/DACK/GTADSM00_1/GTETRGC/CMTW1_TOC0/SCK0/CANTX0/SD1_WP/TST_OUT07/HDSL14_LINK	P17_5	GMAC reset of Ethernet port 2		SW6-1: OFF, SW6-2: ON, SW6-3: OFF
		A7	Address A7 of external bus	CN13-17	SW6-1: ON, SW6-2: OFF
A15	P19_4/GTIOC07_2A/TST_OUT10/HDSL15_MOSI1	**GTIOC07_2A**	**Input capture/output compare/PWM output pin**	**CN26-19**	
A16	P19_5/GTIOC07_2B/SI10#/HDSL15_CLK2	**GTIOC07_2B**	**Input capture/output compare/PWM output pin**	**CN26-20**	
A17	P20_1/MDV/ETH0_TXD0	**MDV**	**MDV setting input**		
		ETH0_TXD0	**TXD0 of Ethernet port 0**		
A18	P20_0/ETH0_TXCLK/HDSL15_MOSI2	**ETH0_TXCLK**	**TXCLK of Ethernet port 0**		
A19	P21_3/ETH0_RXDV/DUEI13/HDSL00_CLK2	**ETH0_RXDV**	**RXDV of Ethernet port 0**		
A20	P23_1/GTIOC06_1A/ESC_IRQ/DUEI00/HDSL02_LINK	**P23_1**	**Control of user LED0**		**SW8-9: ON, SW8-10: OFF**
		GTIOC06_1A	Input capture/output compare/PWM output pin	CN26-5	SW8-9: OFF, SW8-10: ON
A21	P23_3/GTIOC06_2A/ESC_I2CCLK/IIC_SCL0/SI00#/HDSL02_CLK1	GTIOC06_2A	Input capture/output compare/PWM output pin	CN26-7	SW6-7: OFF, SW6-8: ON
		ESC_I2CCLK	**SCL of EEPROM**		**SW6-7: ON, SW6-8: OFF**
A22	P23_2/GTIOC06_1B/ESC_RESETOUT#/TST_OUT00/HDSL02_SMPL	**GTIOC06_1B**	**Input capture/output compare/PWM output pin**	**CN26-6**	
A23	P24_6/MD0/ETH1_TXD0	**MD0**	**MD0 setting input**		
		ETH1_TXD0	**TXD0 of Ethernet port 1**		
A24	P25_2/MDW1/ETH1_TXEN	**MDW1**	**MDW1 setting input**		
		ETH1_TXEN	**TXEN of Ethernet port 1**		
A25	P26_3/ETHSW_PHYLINK1/ESC_PHYLINK1/HDSL04_SMPL	**ETHSW_PHYLINK1/ESC_PHYLINK1**	**PHYLINK of Ethernet port 1**		
A26	P25_1/MDW0/ETH1_TXD3/CANTXDP0	**MDW0**	**MDW1 setting input**		
		ETH1_TXD3	**TXD3 of Ethernet port 1**		
A27	VSS				

Table 5-2 List of RZ/T2H Pin Function Selections (2)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
B1	P10_3/IRQ2/RD#/MTCLKD/MTIOC2B/GTIOC04_3B/GTIOC10_3B/TXD0/SDA0/MOSI0/MDAT10/MDAT00/DISP_DATAR3/ENCIFOE04/DEE04/HDSL08_CLK1	**RD#**	**RD# of external bus**	**CN13-39**	
		GTIOC04_3B	**Input capture/output compare/PWM output pin**	**CN25-22**	
		DISP_DATAR3	**Display data R3**	**CN15-38**	
B2	P10_2/IRQ1/CS0#/MTCLKC/MTIOC2A/GTIOC04_3A/GTIOC10_3A/RXD0/SCL0/MISO0/MCLK10/MCLK00/DISP_DATAR2/ENCIFCK04/SCKE04/HDSL08_SMPL	**CS0#**	**CS0# of external bus**	**CN13-32**	
		GTIOC04_3A	**Input capture/output compare/PWM output pin**	**CN25-21**	
		DISP_DATAR2	**Display data R2**	**CN15-39**	
B3	P10_5/A2/MTIOC1B/MTIOC0A/GTIOC04_4B/CTS0#/MDAT11/MDAT01/DISP_DATAR5/ENCIFDI04/RXDE04/HDSL08_MISO1	**A2**	**Address A2 of external bus**	**CN13-5**	
		GTIOC04_4B	**Input capture/output compare/PWM output pin**	**CN25-24**	
		DISP_DATAR5	**Display data R5**	**CN15-36**	
B4	P11_5/MDAT31/DUEI00/HDSL09_CLK1	**MDAT31**	**Data of DSMIF**	**CN18-6**	
B5	P10_4/IRQ3/A1/MTIOC1A/GTIOC04_4A/SS0#/CTS0#/RTS0#/MCLK11/MCLK01/DISP_DATAR4/ENCIFDO04/TXDE04/HDSL08_SEL1	**A1**	**Address A1 of external bus**	**CN13-3**	
		GTIOC04_4A	**Input capture/output compare/PWM output pin**	**CN25-23**	
		DISP_DATAR4	**Display data R4**	**CN15-37**	
B6	P12_4/IRQ1/D20/GTIOC05_3A/CMTW1_TIC0/RXD2/SCL2/MISO2/SD0_DATA2/MCLK02/ENCIFCK05/SCKE05/HDSL09_MOSI2	D20	Data D20 of external bus	CN17-8	SW2-1: ON, SW2-2: OFF
		GTIOC05_3A	Input capture/output compare/PWM output pin	CN25-33	
		RXD2	RXD2 of RS485	CN12-3	
		ENCIFCK05	Clock of ENCIF	CN2-20	
		SD0_DATA2	**Data DAT2 of eMMC**		**SW2-1: ON, SW2-2: ON**
		SD0_DATA2	Data DAT2 of SD0	CN31-9	SW2-1: OFF, SW2-2: ON
B7	P13_5/IRQ4/D29/GTIOC06_3A/TXD3/SDA3/MOSI3/SPI_SSL32/MDAT40/ENCIFOE13/DEE09/HDSL10_MISO2	**D29**	**Data D29 of external bus**	**CN17-28**	
		GTIOC06_3A	**Input capture/output compare/PWM output pin**	**CN26-9**	
		TXD3	**TXD3 of RS485**		**SW1-4: OFF**
		ENCIFOE13	**ENCIF output enable**	**CN10-4**	
B8	P13_4/D28/GTIOC03_3B/RXD3/SCL3/MISO3/SPI_SSL31/MCLK40/ENCIFCK13/SCKE09/HDSL10_SEL2	D28	Data D28 of external bus	CN17-26	SW1-4: ON
		ENCIFCK13	Clock of ENCIF	CN10-2	
		RXD3	**RXD3 of RS485**		**SW1-4: OFF**
B9	P14_6/IRQ8/POE10#/GTIOC06_2B/GTIOC09_2B/CMTW0_TIC1/ESC_I2CCLK/DE4/IIC_SCL0/SD0_PWEN/DISP_DATAG6/TST_OUT02/HDSL11_SEL2	**DE4**	**DE4 of RS485**	**CN12-8**	
		DISP_DATAG6	**Display data G6**	**CN15-27**	
B10	VSS				
B11	P16_1/DE5/MCLK51/TST_OUT03/HDSL12_MISO2	**MCLK51**	**Clock of DSMIF**	**CN18-25**	

B12	P16_3/IRQ10/GTETRGSA/ESC_LINKACT0/RXD5/SCL5/MISO5/DUEI04/HDSL13_LINK	P16_3/IRQ10	WAKE# of PCIe x1 connector	CN8-B11	SW8-5: OFF, SW8-6: ON
		IRQ10	INT for use with PMOD2	CN49-7	
		RXD5	RX for use with mikroBUS™	CN54-3	
		RXD5	**RXD5 of USB-to-serial conversion**		**SW8-5: ON, SW8-6: OFF**
B13	P17_1/IRQ13/GTIOC03_2A/SD1_DATA2/DUEI06/HDSL13_CLK2	**SD1_DATA2**	**Data DAT2 of SD1**	**CN16-1**	
B14	VSS				
B15	P18_2/SEI/A10/GTADSM03_0/GTIOC07_3B/ETH1_CRS/GMAC1_MDC/SCK1/CANRX0/SD1_PWEN/MCLK10/DISP_DATAB3/HDSL14_MOSI1	**A10**	**Address A10 of external bus**	**CN13-23**	
		DISP_DATAB3	**Display data B3**	**CN15-22**	
B16	P18_6/IRQ3/A14/GTIOC07_4A/GTADSM05_0/CTS1#/CANRXDP1/MCLK12/DISP_DATAB7/ENCIFDO13/ENCIFDO14/TXDE09/TXDE10/HDSL14_MOSI2	**A14**	**Address A14 of external bus**	**CN13-33**	
		GTIOC07_4A	**Input capture/output compare/PWM output pin**	**CN26-23**	
		DISP_DATAB7	**Display data B7**	**CN15-18**	
		ENCIFDO14	**Data output from ENCIF**	**CN10-15**	
B17	P20_5/ETH0_TXEN/DUEI11/HDSL00_LINK	**ETH0_TXEN**	**TXEN of Ethernet port 0**		
B18	VSS				
B19	P21_2/ETH0_RXD3/CANTXDP0/SI12#/HDSL00_MOSI1	**ETH0_RXD3**	**RXD3 of Ethernet port 0**		
B20	P24_3/IRQ14/ESC_I2CCLK/IIC_SCL1/CANRX0/MCLK70/HDSL03_LINK	**CANRX0**	**RX of CAN interface**		**SW7-3: OFF, SW7-4: ON**
		MCLK70	Clock of DSMIF	CN22-17	SW7-3: ON, SW7-4: OFF
B21	P23_6/ETHSW_LPI0/MDAT60/SI01#/HDSL02_MOSI1	**MDAT60**	**Data of DSMIF**	**CN22-8**	
B22	VSS				
B23	P26_1/GMAC1_MDC/ETHSW_MDC/ESC_MDC/CANRXDP1/HDSL03_MOSI2	**GMAC1_MDC/ETHSW_MDC/ESC_MDC**	**MDC of Ethernet port 3**		
B24	P26_2/GMAC1_MDIO/ETHSW_MDIO/ESC_MDIO/CANTXDP1/HDSL04_LINK	**GMAC1_MDIO/ETHSW_MDIO/ESC_MDIO**	**MDIO of Ethernet port 3**		
B25	P25_0/MD2/ETH1_TXD2/CANRXDP0	**MD2**	**MD2 setting input**		
		ETH1_TXD2	**TXD2 of Ethernet port 1**		
B26	P25_3/ETH1_RXCLK/DUEI03/HDSL03_SEL1	**ETH1_RXCLK**	**RXCLK of Ethernet port 1**		
B27	P28_3/GTIOC08_2A/SPI_SSL11/TST_OUT06/HDSL05_CLK2	**GTIOC08_2A**	**Input capture/output compare/PWM output pin**	**CN26-31**	

Table 5-3 List of RZ/T2H Pin Function Selections (3)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
C1	P11_1/IRQ4/ESC_LEDRUN/TXD1/SDA1/MOSI1/MDAT22/DUEI15/HDSL08_MISO2	**TXD1**	**TXD for use with PMOD2**	**CN49-2**	
		MDAT22	**Data of DSMIF**	**CN21-24**	
C2	P09_5/D14/MTIOC6D/GTIOC04_0B/GTIOC10_0B/MDAT70/DISP_HSYNC/TST_OUT13/HDSL07_CLK2	**D14**	**Data D14 of external bus**	**CN17-33**	
		GTIOC04_0B	**Input capture/output compare/PWM output pin**	**CN25-16**	
		DISP_HSYNC	**HSYNC of display output**	**CN15-14**	
C3	P11_2/IRQ5/SS1#/CTS1#/RTS1#/MCLK30/TST_OUT15/HDSL08_MOSI2	**RTS1#**	**RTS for use with PMOD2**	**CN49-4**	
		MCLK30	**Clock of DSMIF**	**CN18-7**	
C4	P10_7/IRQ9/A4/MTIC5U/GTIOC05_0B/GTIOC00_3A/SCK1/MDAT21/DISP_DATAR7/HDSL08_CLK2/POUTB	**IRQ9**	**IRQ of SPI expansion connector**	**CN63-13**	
		A4	**Address A4 of external bus**	**CN13-9**	
		MDAT21	**Data of DSMIF**	**CN21-26**	
		DISP_DATAR7	**Display data R7**	**CN15-34**	
C5	P11_0/IRQ13/A5/GTIOC00_3B/ESC_RESETOUT#/RXD1/SCL1/MISO1/MCLK22/DISP_DATAG0/HDSL08_SEL2/POUTZ	A5	Address A5 of external bus	CN13-13	SW6-3: OFF, SW6-4: ON, SW6-5: OFF
		RXD1	RXD for use with PMOD2	CN49-3	
		DISP_DATAG0	Display data G0	CN15-33	
		ESC_RESETOUT#	ESC_RESETOUT# of Ethernet port 0 or port 1		SW6-3: OFF, SW6-4: OFF, SW6-5: ON
			ESC_RESETOUT# of Ethernet port 2		SW6-2: OFF, SW6-3: ON, SW6-4: OFF, SW6-5: OFF
			ESC_RESETOUT# of Ethernet port 0, port 1, or port 2		**SW6-2: OFF, SW6-3: ON, SW6-4: OFF, SW6-5: ON**
C6	VSS				
C7	P13_0/D24/GTIOC02_3A/DE2/SPI_RSPCK3/SD0_DATA6/MCLK00/ENCIFCK12/ENCIFCK03/SCKE08/SCKE03/HDSL10_SEL1	D24	Data D24 of external bus	CN17-16	SW2-1: ON, SW2-2: OFF
		GTIOC02_3A	Input capture/output compare/PWM output pin	CN24-33	
		DE2	DE2 of RS485	CN12-7	
		ENCIFCK12	Clock of ENCIF	CN10-3	
		SD0_DATA6	**Data DAT6 of eMMC**		**SW2-1: ON, SW2-2: ON**
C8	P13_7/IRQ14/D31/GTIOC06_4A/GTIOC04_3B/CTS3#/MDAT41/ENCIFDI13/RXDE09/HDSL11_LINK	**D31**	**Data D31 of external bus**	**CN17-32**	
		GTIOC06_4A	**Input capture/output compare/PWM output pin**	**CN26-11**	
		ENCIFDI13	**Data input to ENCIF**	**CN10-8**	
C9	P14_1/RD/WR#/GTIOC06_0A/GTIOC09_0A/GTIOC05_3A/RTCAT1HZ/SCK4/SD0_CD/MDAT42/DISP_DATAG1/DUEI02/HDSL11_CLK1	**RD/WR#**	**RD/WR# of external bus**	**CN13-38**	
		DISP_DATAG1	**Display data G1**	**CN15-32**	

C10	P14_2/BS#/GTIOC06_0B/GTIOC09_0B/GTIOC05_3B/RXD4/SCL4/MISO4/SD0_WP/DISP_DATAG2/ENCIFCK00/SCKE00/HDSL11_SEL1	**BS#**	**BS# of external bus**	**CN13-30**	
		RXD4	**RXD4 of RS485**	**CN12-4**	
		DISP_DATAG2	**Display data G2**	**CN15-31**	
		ENCIFCK00	**Clock of ENCIF**	**CN2-3**	
C11	P14_5/TEND/POE8#/GTIOC06_2A/GTIOC09_2A/GTIOC06_3B/CMTW0_TOC0/ESC_RESETOUT#/CTS4#/DISP_DATAG5/ENCIFDI00/RXDE00/HDSL11_CLK2	**TEND**	**End of DMA transfer**	**CN13-40**	
		DISP_DATAG5	**Display data G5**	**CN15-28**	
		ENCIFDI00	**Data input to ENCIF**	**CN2-9**	
C12	P16_6/GTIOC03_0B/SD1_CMD/DUEI05/HDSL13_SEL1	**SD1_CMD**	**CMD of SD1**	**CN16-3**	
C13	P17_3/IRQ15/GTETRGA/SI06#/HDSL13_MISO2	P17_3	CLKREQ output from PCIe x4 connector	CN32-B12	SW15-1: OFF
		IRQ15	**PRSNT2 input to PCIe x4 connector**	**CN32-B17, CN32-B31**	**SW15-1: ON**
C14	P19_2/GTIOC07_1A/SI09#/HDSL15_SEL1	**GTIOC07_1A**	**Input capture/output compare/PWM output pin**	**CN26-17**	
C15	P19_3/GTIOC07_1B/DUEI10/HDSL15_MISO1	**GTIOC07_1B**	**Input capture/output compare/PWM output pin**	**CN26-18**	
C16	P18_7/IRQ4/A15/GTIOC07_4B/GTADSM05_1/ETHSW_PTPOUT3/ESC_SYNC1/DE1/CANTXDP1/MDAT12/ENCIFDI13/ENCIFDI14/RXDE09/RXDE10/HDSL15_LINK	**A15**	**Address A15 of external bus**	**CN13-35**	
		GTIOC07_4B	**Input capture/output compare/PWM output pin**	**CN26-24**	
		ETHSW_PTPOUT3	**Timer pulse output from ETHSW**	**CN20-7**	
		ENCIFDI14	**Data input to ENCIF**	**CN10-17**	
C17	P20_3/ETH0_TXD2/CANRX0	**ETH0_TXD2**	**TXD2 of Ethernet port 0**		
C18	P20_6/ETH0_RXCLK/TST_OUT11/HDSL00_SMPL	**ETH0_RXCLK**	**RXCLK of Ethernet port 0**		
C19	P21_4/GMAC0_MDC/ETHSW_MDC/ESC_MDC/CANRX1/TST_OUT13/HDSL00_SEL2	**GMAC0_MDC/ETHSW_MDC/ESC_MDC**	**MDC of Ethernet port 0 or port 1**		
			MDC of Ethernet port 2		**SW2-6: ON**
C20	P23_4/GTIOC06_2B/ESC_I2CDATA/IIC_SDA0/DUEI01/HDSL02_SEL1	GTIOC06_2B	Input capture/output compare/PWM output pin		SW6-9: OFF, SW6-10: ON
		ESC_I2CDATA	**SDA of EEPROM**		**SW6-9: ON, SW6-10: OFF**
C21	P23_5/ESC_LINKACT2/MCLK60/TST_OUT01/HDSL02_MISO1	**ESC_LINKACT2**	**LINKACT2 control of LED8**		**SW7-5: OFF, SW7-6 :ON**
		MCLK60	Clock of DSMIF	CN22-7	SW7-5: ON, SW7-6 :OFF
C22	P22_6/IRQ8/A19/GTETRGSB/GMAC0_PTPTRG1/ESC_LATCH1/DE5/CANTX1/SD0_WP/DUEI15/HDSL01_SEL2	IRQ8	IRQ of display output unit	CN15-4	SW2-1: ON, SW2-2: OFF
		GMAC0_PTPTRG1	PTPTRG1 of GMAC0	CN23-2	
		SD0_WP	WP of SD0	CN31-WP	SW2-1: OFF, SW2-2: ON
C23	P24_7/MD1/ETH1_TXD1	**MD1**	**MD1 setting input**		
		ETH1_TXD1	**TXD1 of Ethernet port 1**		
C24	P24_5/ETH1_TXCLK/HDSL03_CLK1	**ETH1_TXCLK**	**TXCLK of Ethernet port 1**		

C25	P26_4/ETH1_REFCLK/RMII1_REFCLK	**ETH1_REFCLK**	**REFCLK of Ethernet port 1**		
C26	P26_5/IRQ12/CANTX0/ENCIFCK01/SCKE01/HDSL04_CLK1	**IRQ12**	**Interrupt of Ethernet port 1**		
C27	P27_7/IRQ4/GTIOC08_0A/ETHSW_TDMAOUT0/SPI_RSPCK1/DUEI05/HDSL05_CLK1	**GTIOC08_0A**	**Input capture/output compare/PWM output pin**	**CN26-27**	
		ETHSW_TDMAOUT0	**TDMA timer output from ETHSW**	**CN20-4**	

Table 5-4 List of RZ/T2H Pin Function Selections (4)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
D1	P11_3/IRQ6/CTS1#/MDAT30/SI15#/HDSL09_LINK	**CTS1#**	**CTS for use with PMOD2**	**CN49-1**	
		MDAT30	**Data of DSMIF**	**CN18-8**	
D2	P09_4/D13/MTIOC6B/GTIOC04_0A/GTIOC10_0A/MCLK70/DISP_CLK/DUEI13/HDSL07_MOSI1	**D13**	**Data D13 of external bus**	**CN17-31**	
		GTIOC04_0A	**Input capture/output compare/PWM output pin**	**CN25-15**	
		DISP_CLK	**Clock of display output**	**CN15-16**	
D3	P09_6/D15/MTIOC7A/GTIOC04_1A/GTIOC10_1A/MCLK71/DISP_VSYNC/SI13#/HDSL07_SEL2	**D15**	**Data D15 of external bus**	**CN17-35**	
		MCLK71	**Clock of DSMIF**	**CN22-15**	
		DISP_VSYNC	**VSYNC of display output**	**CN15-13**	
D4	P10_0/IRQ4/WE1#/MTIOC7B/GTIOC04_2A/GTIOC10_2A/MCLK72/DISP_DATAR0/TST_OUT14/HDSL07_MOSI2	**WE1#**	**WE1# of external bus**	**CN17-38**	
		MCLK72	**Clock of DSMIF**	**CN22-13**	
		DISP_DATAR0	**Display data R0**	**CN15-41**	
D5	P09_7/WE0#/MTIOC7C/GTIOC04_1B/GTIOC10_1B/MDAT71/DISP_DE/DUEI14/HDSL07_MISO2	**WE0#**	**WE0# of external bus**	**CN17-36**	
		MDAT71	**Data of DSMIF**	**CN22-16**	
		DISP_DE	**DE of display output**	**CN15-12**	
D6	P12_6/D22/GTIOC05_4A/GTIOC01_3B/CMTW1_TIC1/SS2#/CTS2#/RTS2#/SD0_DATA4/MCLK10/ENCIFDO05/TXDE05/HDSL10_SMPL	D22	Data D22 of external bus	CN17-12	SW2-1: ON, SW2-2: OFF
		GTIOC05_4A	Input capture/output compare/PWM output pin	CN25-35	
		ENCIFDO05	Data output from ENCIF	CN2-24	
		SD0_DATA4	**Data DAT4 of eMMC**		**SW2-1: ON, SW2-2: ON**
D7	P12_0/D16/MTIC5V/GTIOC05_1A/CMTW0_TIC0/CANRX1/SD0_CLK/DUEI01/HDSL09_MOSI1	D16	Data D16 of external bus	CN17-37	SW2-1: ON, SW2-2: OFF
		GTIOC05_1A	Input capture/output compare/PWM output pin	CN25-29	
		SD0_CLK	**CLK of eMMC**		**SW2-1: ON, SW2-2: ON**
			CLK of SD0	CN31-5	SW2-1: OFF, SW2-2: ON
D8	VSS				
D9	P14_3/IRQ6/DREQ/POE0#/GTIOC06_1A/GTIOC09_1A/ESC_LINKACT2/TXD4/SDA4/MOSI4/SD1_CD/DISP_DATAG3/ENCIFOE00/DEE00/HDSL11_MISO1	**DREQ**	**DMA request**	**CN13-28**	
		DISP_DATAG3	**Display data G3**	**CN15-30**	
		ENCIFOE00	**ENCIF output enable**	**CN2-5**	
		TXD4	**TXD4 of RS485**	**CN12-6**	
D10	P15_6/IRQ1/GTIOC09_6B/MDAT42/ENCIFDO07/TXDE07/HDSL12_MOSI1	**IRQ1**	**INT for use with mikroBUS™**	**CN54-2**	
		MDAT42	**Data of DSMIF**	**CN18-14**	
D11	P16_0/IRQ2/CTS5#/MDAT50/TXDE07/DUEI03/HDSL12_SEL2	**MDAT50**	**Data of DSMIF**	**CN18-28**	
D12	VSS				

D13	P18_3/IRQ0/A11/GTADSM03_1/RTCAT1HZ/ETH1_COL/GMAC1_MDIO/RXD1/SCL1/MISO1/CANTX0/SD1_IOVS/MDAT10/DISP_DATAB4/HDSL14_CLK2	**A11**	**Address A11 of external bus**	**CN13-25**	
		DISP_DATAB4	**Display data B4**	**CN15-21**	
D14	P19_0/GTIOC07_0A/DUEI09/HDSL15_SMPL	**GTIOC07_0A**	**Input capture/output compare/PWM output pin**	**CN26-15**	
D15	P18_0/IRQ7/A8/TEND/GTADSM02_0/ESC_LEDRUN/SS0#/CTS0#/RTS0#/CANRXDP0/SD1_PWEN/DISP_DATAB1/TST_OUT08/HDSL14_SEL1	A8	Address A8 of external bus	CN13-19	SW8-3: OFF, SW8-4: ON
		DISP_DATAB1	Display data B1	CN15-24	
		ESC_LEDRUN	**LEDRUN control of LED4**		**SW8-3: ON, SW8-4: OFF**
D16	VSS				
D17	P21_7/ETH0_REFCLK/RMII0_REFCLK/CANTXDP1/HDSL01_LINK	**ETH0_REFCLK**	**REFCLK of Ethernet port 0**		
D18	P20_7/ETH0_RXD0/SI11#/HDSL00_CLK1	**ETH0_RXD0**	**RXD0 of Ethernet port 0**		
D19	P21_6/ETHSW_PHYLINK0/ESC_PHYLINK0/CANRXDP1/HDSL00_MOSI2	**ETHSW_PHYLINK0/ESC_PHYLINK0**	**PHYLINK of Ethernet port 0**		
D20	VSS				
D21	P22_1/GTETRGA/ETH0_TXER/TXD5/SDA5/MOSI5/CANTX0/HDSL01_CLK1	**ETH0_TXER**	**TXER of Ethernet port 0**		
D22	P24_1/IRQ12/MCLK62/SI02#/HDSL02_MISO2	**MCLK62**	**Clock of DSMIF**	**CN22-3**	
D23	P25_6/ETH1_RXD2/CANRX1/DUEI04/HDSL03_CLK2	**ETH1_RXD2**	**RXD2 of Ethernet port 1**		
D24	VSS				
D25	P26_0/ETH1_RXDV/SI04#/HDSL03_MISO2	**ETH1_RXDV**	**RXDV of Ethernet port 1**		
D26	P26_6/SEI/CS2#/ETH1_TXER/ESC_RESETOUT#/CANRX0/ENCIFOE01/DEE01/HDSL04_SEL1	**ETH1_TXER**	**TXER of Ethernet port 1**		
D27	P28_5/CANRX0/SPI_SSL13/MCLK71/ENCIFCK08/ENCIFCK00/SCKE08/SCKE00/HDSL05_MISO2	**ENCIFCK08**	**Clock of ENCIF**	**CN3-11**	

Table 5-5 List of RZ/T2H Pin Function Selections (5)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
E1	DDR_DQA12	**DDR_DQA12**	**Data DQ_A[3] of LPDDR4**		
E2	DDR_DQA9	**DDR_DQA9**	**Data DQ_A[1] of LPDDR4**		
E3	VSS				
E4	DDR_DQA13	**DDR_DQA13**	**Data DQ_A[0] of LPDDR4**		
E5	VSS				
E6	P12_7/IRQ2/D23/GTIOC05_4B/CMTW1_TOC1/CTS2#/SD0_DATA5/MDAT10/ENCIFDI05/RXDE05/HDSL10_CLK1	D23	Data D23 of external bus	CN17-14	SW2-1: ON, SW2-2: OFF
		GTIOC05_4B	Input capture/output compare/PWM output pin	CN25-36	
		ENCIFDI05	Data input to ENCIF	CN2-26	
		SD0_DATA5	**Data DAT5 of eMMC**		**SW2-1: ON, SW2-2: ON**
E7	P12_3/D19/GTIOC05_2B/CMTW0_TOC1/SCK2/CANTXDP1/SD0_DATA1/HDSL09_MISO2	D19	Data D19 of external bus	CN17-6	SW2-1: ON, SW2-2: OFF
		GTIOC05_2B	Input capture/output compare/PWM output pin	CN25-32	
		SD0_DATA1	**Data DAT1 of eMMC**		**SW2-1: ON, SW2-2: ON**
			Data DAT1 of SD0	CN31-8	SW2-1: OFF, SW2-2: ON
E8	P12_2/D18/GTIOC05_2A/CMTW0_TIC1/CANRXDP1/SD0_DATA0/SI01#/HDSL09_SEL2	D18	Data D18 of external bus	CN17-4	SW2-1: ON, SW2-2: OFF
		GTIOC05_2A	Input capture/output compare/PWM output pin	CN25-31	
		SD0_DATA0	**Data DAT0 of eMMC**		**SW2-1: ON, SW2-2: ON**
			Data DAT0 of SD0	CN31-7	SW2-1: OFF, SW2-2: ON
E9	P15_7/SS5#/CTS5#/RTS5#/MCLK50/ENCIFDI07/RXDE07/HDSL12_CLK2	**MCLK50**	**Clock of DSMIF**	**CN18-27**	
E10	P15_1/GTIOC09_4A/MCLK40/ENCIFOE06/DEE06/HDSL12_LINK	**MCLK40**	**Clock of DSMIF**	**CN18-17**	
E11	P15_5/IRQ0/GTIOC09_6A/MCLK42/ENCIFOE07/DEE07/HDSL12_MISO1	**MCLK42**	**Clock of DSMIF**	**CN18-13**	
E12	P17_2/IRQ14/GTIOC03_2B/SD1_DATA3/TST_OUT06/HDSL13_SEL2	**SD1_DATA3**	**Data DAT3 of SD1**	**CN16-2**	
E13	P18_1/IRQ15/A9/GTADSM02_1/GTIOC07_3A/ESC_LEDERR/CTS0#/CANTXDP0/SD1_IOVS/DISP_DATAB2/SI08#/HDSL14_MISO1	A9	Address A9 of external bus	CN13-21	SW8-1: OFF, SW8-2: ON
		DISP_DATAB2	Display data B2	CN15-23	
		ESC_LEDERR	**LEDERR control of LED5**		**SW8-1: ON, SW8-2: OFF**
E14	P19_1/GTIOC07_0B/TST_OUT09/HDSL15_CLK1	**GTIOC07_0B**	**Input capture/output compare/PWM output pin**	**CN26-16**	

E15	P17_7/WE3#/AH#/GTADSM01_1/CMTW1_TOC1/ETHSW_PTPOUT1/ESC_SYNC1/TXD0/SDA0/MOSI0/SD1_IOVS/DISP_DATAB0/DUEI08/HDSL14_CLK1	**WE3#**	**WE3 of external bus**	**CN17-40**	
		ETHSW_PTPOUT1	**Timer pulse output from ETHSW**	**CN20-3**	
		DISP_DATAB0	**Display data B0**	**CN15-25**	
E16	P19_6/MCLK52/HDSL15_SEL2	**MCLK52**	**Clock of DSMIF**	**CN18-23**	
E17	P20_2/ETH0_TXD1	**ETH0_TXD1**	**TXD1 of Ethernet port 0**		
E18	P21_0/ETH0_RXD1/DUEI12/HDSL00_SEL1	**ETH0_RXD1**	**RXD1 of Ethernet port 0**		
E19	P22_0/IRQ11/HDSL01_SMPL	**IRQ11**	**MDINT of Ethernet port 0**		
E20	P22_4/IRQ6/A21/GTETRGD/ETH0_COL/SS5#/CTS5#/RTS5#/CANTXDP0/TST_OUT14/HDSL01_MOSI1	**ETH0_COL**	**COL of Ethernet port 0**		
E21	P22_5/IRQ7/A20/GTETRGSA/GMAC0_PTPTRG0/ESC_LATCH0/CTS5#/CANRX1/SD0_CD/SI14#/HDSL01_CLK2	P22_5/IRQ7	WAKE# of PCIe x4 connector	CN32-B11	SW2-1: ON, SW2-2: OFF
		IRQ7	Interrupt of SPI expansion connector	CN63-2	
		GMAC0_PTPTRG0	PTPTRG0 of GMAC0	CN23-1	
		SD0_CD	CD of SD0	CN31-CD	SW2-1: OFF, SW2-2: ON
E22	P22_2/A23/GTETRGB/ETH0_RXER/RXD5/SCL5/MISO5/CANRX0/HDSL01_SEL1	**ETH0_RXER**	**RXER of Ethernet port 0**		
E23	P25_4/ETH1_RXD0/TST_OUT03/HDSL03_MISO1	**ETH1_RXD0**	**RXD0 of Ethernet port 1**		
E24	P25_7/ETH1_RXD3/CANTX1/TST_OUT04/HDSL03_SEL2	**ETH1_RXD3**	**RXD3 of Ethernet port 1**		
E25	P28_4/GTIOC08_2B/SPI_SSL12/SI06#/HDSL05_SEL2	**GTIOC08_2B**	**Input capture/output compare/PWM output pin**	**CN26-32**	
E26	P28_1/IRQ6/GTIOC08_1A/ETHSW_TDMAOUT2/SPI_MISO1/SI05#/HDSL05_MISO1	**GTIOC08_1A**	**Input capture/output compare/PWM output pin**	**CN26-29**	
		ETHSW_TDMAOUT2	**TDMA timer output from ETHSW**	**CN20-8**	
E27	P28_6/CANTX0/MDAT71/ENCIFOE08/ENCIFOE00/DEE08/DEE00/HDSL05_MOSI2	**ENCIFOE08**	**ENCIF output enable**	**CN3-13**	

Table 5-6 List of RZ/T2H Pin Function Selections (6)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
F1	VSS				
F2	DDR_DQA8	**DDR_DQA8**	**Data DQ_A[7] of LPDDR4**		
F3	DDR_DQA11	**DDR_DQA11**	**Data DQ_A[2] of LPDDR4**		
F4	DDR_DQA14	**DDR_DQA14**	**Data DQ_A[4] of LPDDR4**		
F5	DDR_DQSA_C1	**DDR_DQSA_C1**	**DQS0_A_C of LPDDR4**		
F6	P13_3/D27/GTIOC03_3A/SCK3/SPI_SSL30/MDAT01/ENCIFDI12/ENCIFDI03/RXDE08/RXDE03/HDSL10_CLK2	**D27**	**Data D27 of external bus**	**CN17-24**	
		ENCIFDI12	**Data input to ENCIF**	**CN10-9**	
F7	P13_1/D25/GTIOC02_3B/SPI_MOSI3/SD0_DATA7/MDAT00/ENCIFOE12/ENCIFOE03/DEE08/DEE03/HDSL10_MISO1	D25	Data D25 of external bus	CN17-18	SW2-1: ON, SW2-2: OFF
		GTIOC02_3B	Input capture/output compare/PWM output pin	CN24-34	
		ENCIFOE12	ENCIF output enable	CN10-5	
		SD0_DATA7	**Data DAT7 of eMMC**		**SW2-1: ON, SW2-2: ON**
F8	P13_2/IRQ3/D26/SPI_MISO3/SD0_RST#/MCLK01/ENCIFDO12/ENCIFDO03/TXDE08/TXDE03/HDSL10_MOSI1	D26	Data D26 of external bus	CN17-22	SW2-1: ON, SW2-2: OFF
		ENCIFDO12	Data output from ENCIF	CN10-7	
		SD0_RST#	**Reset of eMMC**		**SW2-1: ON, SW2-2: ON**
F9	P15_4/GTIOC09_5B/MDAT41/ENCIFCK07/SCKE07/HDSL12_SEL1	**MDAT41**	**Data of DSMIF**	**CN18-16**	
F10	VSS				
F11	P15_2/GTIOC09_4B/MDAT40/ENCIFDO06/TXDE06/HDSL12_SMPL	**MDAT40**	**Data of DSMIF**	**CN18-18**	
F12	P16_7/GTIOC03_1A/SD1_DATA0/TST_OUT05/HDSL13_MISO1	**SD1_DATA0**	**Data DAT0 of SD1**	**CN16-7**	
F13	P17_6/WE2#/GTADSM01_0/GTETRGD/CMTW1_TIC1/ETHSW_PTPOUT0/ESC_SYNC0/RXD0/SCL0/MISO0/SD1_PWEN/DISP_DATAG7/SI07#/HDSL14_SMPL	**WE2#**	**WE2# of external bus**	**CN17-20**	
		ETHSW_PTPOUT0	**Timer pulse output from ETHSW**	**CN20-1**	
		DISP_DATAG7	**Display data G7**	**CN15-26**	
F14	VSS				
F15	P18_4/IRQ1/A12/GTIOC07_3A/GTADSM04_0/ESC_LEDSTER/TXD1/SDA1/MOSI1/CANRX1/MCLK11/DISP_DATAB5/ENCIFCK13/ENCIFCK14/SCKE09/SCKE10/HDSL14_SEL2	**A12**	**Address A12 of external bus**	**CN13-27**	
		GTIOC07_3A	**Input capture/output compare/PWM output pin**	**CN26-21**	
		DISP_DATAB5	**Display data B5**	**CN15-20**	
		ENCIFCK14	**Clock of ENCIF**	**CN10-11**	
F16	P19_7/MDAT52/HDSL15_MISO2	**MDAT52**	**Data of DSMIF**	**CN18-24**	
F17	P20_4/ETH0_TXD3/CANTX0	**ETH0_TXD3**	**TXD3 of Ethernet port 0**		
F18	VSS				
F19	P24_0/IRQ11/ETHSW_LPI2/MDAT61/TST_OUT02/HDSL02_SEL2	**MDAT61**	**Data of DSMIF**	**CN22-6**	

F20	P22_3/IRQ5/A22/GTETRGC/ETH0_CRS/SCK5/CANRXDP0/DUEI14/HDSL01_MISO1	**ETH0_CRS**	**CRS of Ethernet port 0**		
F21	P24_2/IRQ13/MDAT62/HDSL02_MOSI2	**MDAT62**	**Data of DSMIF**	**CN22-4**	
F22	VSS				
F23	P25_5/ETH1_RXD1/SI03#/HDSL03_MOSI1	**ETH1_RXD1**	**RXD1 of Ethernet port 1**		
F24	P28_0/IRQ5/GTIOC08_0B/ETHSW_TDMAOUT1/SPI_MOSI1/TST_OUT05/HDSL05_SEL1	**ETHSW_TDMAOUT1**	**TDMA timer output from ETHSW**	**CN20-6**	
		GTIOC08_0B	**Input capture/output compare/PWM output pin**	**CN26-28**	
F25	P27_5/MTIOC1A/GTIOC08_4A/GTIOC02_2A/TXD0/SDA0/MOSI0/SPI_SSL00/HSPI_IO3/ENCIFDO14/TXDE10/HDSL05_LINK	GTIOC08_4A	Input capture/output compare/PWM output pin	CN26-35	SW4-7: OFF, SW4-8: ON
		HSPI_IO3	IO3 of SHOSTIF	CN64-9	
		TXD0	**TXD0 of USB-to-serial conversion**		**SW4-7: ON, SW4-8: OFF**
F26	VSS				
F27	P27_3/MTIOC2A/GTIOC08_3A/GTIOC02_1A/GMAC1_PTPTRG1/SCK0/CANRXDP1/SPI_MOSI0/HSPI_IO1/ENCIFCK14/SCKE10/HDSL04_MISO2	**GTIOC08_3A**	**Input capture/output compare/PWM output pin**	**CN26-33**	
		GMAC1_PTPTRG1	**PTPTRG1 of GMAC1**	**CN23-4**	
		HSPI_IO1	**IO1 of SHOSTIF**	**CN64-11**	

Table 5-7 List of RZ/T2H Pin Function Selections (7)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
G1	DDR_DQA15	**DDR_DQA15**	**Data DQ_A[5] of LPDDR4**		
G2	VSS				
G3	DDR_DQA10	**DDR_DQA10**	**Data DQ_A[6] of LPDDR4**		
G4	DDR_DMIA1	**DDR_DMIA1**	**DMI_A[0] of LPDDR4**		
G5	DDR_DQSA_T1	**DDR_DQSA_T1**	**DQS0_A_T of LPDDR4**		
G6	DDR_VDDQ				
G7	P12_5/D21/GTIOC05_3B/GTIOC01_3A/CMTW1_TOC0/TXD2/SDA2/MOSI2/SD0_DATA3/MDAT02/ENCIFOE05/DEE05/HDSL10_LINK	D21	Data D21 of external bus	CN17-10	SW2-1: ON, SW2-2: OFF
		GTIOC05_3B	Input capture/output compare/PWM output pin	CN25-34	
		TXD2	TXD2 of RS485	CN12-5	
		ENCIFOE05	ENCIF output enable	CN2-22	
		SD0_DATA3	**Data DAT3 of eMMC**		**SW2-1: ON, SW2-2: ON**
			Data DAT3 of SD0	CN31-1	SW2-1: OFF, SW2-2: ON
G8	P12_1/D17/MTIC5W/GTIOC05_1B/CMTW0_TOC0/CANTX1/SD0_CMD/TST_OUT01/HDSL09_CLK2	D17	Data D17 of external bus	CN17-39	SW2-1: ON, SW2-2: OFF
		GTIOC05_1B	Input capture/output compare/PWM output pin	CN25-30	
		SD0_CMD	**CMD of eMMC**		**SW2-1: ON, SW2-2: ON**
			CMD of SD0	CN31-2	SW2-1: OFF, SW2-2: ON
G9	P15_0/GTIOC09_3B/MDAT32/ENCIFCK06/SCKE06/HDSL11_MOSI2	**MDAT32**	**Data of DSMIF**	**CN18-4**	
G10	VSS				
G11	P15_3/GTIOC09_5A/MCLK41/ENCIFDI06/RXDE06/HDSL12_CLK1	**MCLK41**	**Clock of DSMIF**	**CN18-15**	
G12	P16_5/GTIOC03_0A/SD1_CLK/SI04#/HDSL13_CLK1	**SD1_CLK**	**CLK of SD1**	**CN16-5**	
G13	P17_4/A6/DREQ/GTADSM00_0/GTETRGB/CMTW1_TIC0/DE0/CANRX0/SD1_CD/DUEI07/HDSL13_MOSI2	A6	Address A6 of external bus	CN13-15	SW2-3: OFF
		SD1_CD	**CD of SD1**	**CN16-9**	**SW2-3: ON**
G14	VSS				
G15	P18_5/IRQ2/A13/GTIOC07_3B/GTADSM04_1/SS1#/CTS1#/RTS1#/CANTX1/MDAT11/DISP_DATAB6/ENCIFOE13/ENCIFOE14/DEE09/DEE10/HDSL14_MISO2	**A13**	**Address A13 of external bus**	**CN13-31**	
		GTIOC07_3B	**Input capture/output compare/PWM output pin**	**CN26-22**	
		DISP_DATAB6	**Display data B6**	**CN15-19**	
		ENCIFOE14	**ENCIF output enable**	**CN10-13**	
G16	P21_5/GMAC0_MDIO/ETHSW_MDIO/ESC_MDIO/CANTX1/SI13#/HDSL00_MISO2	**GMAC0_MDIO/ ETHSW_MDIO/ ESC_MDIO**	**MDIO of Ethernet port 0 or port 1**		
			MDIO of Ethernet port 2		**SW2-6: ON**
G17	P21_1/ETH0_RXD2/CANRXDP0/TST_OUT12/HDSL00_MISO1	**ETH0_RXD2**	**RXD2 of Ethernet port 0**		

G18	VSS				
G19	P23_7/ETHSW_LPI1/MCLK61/DUEI02/HDSL02_CLK2	**MCLK61**	**Clock of DSMIF**	**CN22-5**	
G20	P23_0/IRQ10/A17/GTIOC06_0B/ETH1_COL/ETHSW_TDMAOUT3/ESC_LINKACT1/CANTXDP1/SI15#/HDSL01_MOSI2	GTIOC06_0B	Input capture/output compare/PWM output pin	CN26-4	SW5-7: ON, SW5-8: OFF
		ESC_LINKACT1	**LINKACT1 control of LED7**		**SW5-7: OFF, SW5-8: ON**
G21	P22_7/IRQ9/A18/GTIOC06_0A/ETH1_CRS/ETHSW_TDMAOUT2/ESC_LINKACT0/CANRXDP1/TST_OUT15/HDSL01_MISO2	GTIOC06_0A	Input capture/output compare/PWM output pin	CN26-3	SW5-9: ON, SW5-10: OFF
		ESC_LINKACT0	**LINKACT0 control of LED6**		**SW5-9: OFF, SW5-10: ON**
G22	P24_4/IRQ15/ESC_I2CDATA/IIC_SDA1/CANTX0/MDAT70/HDSL03_SMPL	**CANTX0**	**TX of CAN interface**		**SW7-1: OFF, SW7-2: ON**
		MDAT70	Data of DSMIF	CN22-18	SW7-1: ON, SW7-2: OFF
G23	P27_0/IRQ1/CS5#/ETH1_CRS/CANTXDP0/SPI_SSL02/HSPI_INT#/ENCIFDI01/RXDE01/HDSL04_MOSI1	**ETH1_CRS**	**CRS of Ethernet port 1**		**SW4-1: ON, SW4-2: OFF**
		CS5#	CS5# of external bus	CN13-20	SW4-1: OFF, SW4-2: ON
		HSPI_INT#	INT# of SHOSTIF	CN64-2	
G24	P27_1/IRQ2/GTIOC02_0A/ETH1_COL/CANRX1/SPI_SSL03/HSPI_CS#/HDSL04_CLK2	**ETH1_COL**	**COL of Ethernet port 1**		**SW4-3: ON, SW4-4: OFF**
		HSPI_CS#	CS# of SHOSTIF	CN64-4	SW4-3: OFF, SW4-4: ON
G25	P28_2/IRQ7/GTIOC08_1B/ETHSW_TDMAOUT3/SPI_SSL10/DUEI06/HDSL05_MOSI1	**GTIOC08_1B**	**Input capture/output compare/PWM output pin**	**CN26-30**	
		ETHSW_TDMAOUT3	**TDMA timer output from ETHSW**	**CN20-10**	
G26	P27_2/IRQ3/GTIOC02_0B/GMAC1_PTPTRG0/ESC_LEDERR/CANTX1/SPI_RSPCK0/HSPI_IO0/HDSL04_SEL2	**IRQ3**	**MDINT of Ethernet port 3**		
		GMAC1_PTPTRG0	**PTPTRG0 of GMAC1**	**CN23-3**	
		HSPI_IO0	**IO0 of SHOSTIF**	**CN64-12**	
G27	P27_6/MTIOC1B/GTIOC08_4B/GTIOC02_2B/HSPI_CK/ENCIFDI14/RXDE10/HDSL05_SMPL	**GTIOC08_4B**	**Input capture/output compare/PWM output pin**	**CN26-36**	
		HSPI_CKP	**Clock of SHOSTIF**	**CN64-3**	

Table 5-8 List of RZ/T2H Pin Function Selections (8)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
H1	DDR_DQA6	**DDR_DQA6**	**Data DQ_A[9] of LPDDR4**		
H2	DDR_DQA5	**DDR_DQA5**	**Data DQ_A[15] of LPDDR4**		
H3	VSS				
H4	VSS				
H5	VSS				
H6	DDR_VDDQ				
H7	VSS				
H8	VSS				
H9	VDDP_18_33				
H10	VSS				
H11	VDDP_18_6				
H12	VDDP_18_33				
H13	VSS				
H14	VDDP_18_7				
H15	VSS				
H16	VDDP_18_33				
H17	VSS				
H18	VDDP_18_0				
H19	VSS				
H20	VDDP_18_1				
H21	VDD1833_1				
H22	P26_7/IRQ0/CS3#/ETH1_RXER/ESC_LEDSTER/CANRXDP0/SPI_SSL01/ENCIFDO01/TXDE01/HDSL04_MISO1	**ETH1_RXER**	**RXER of Ethernet port 1**		
H23	P28_7/CANRXDP0/MCLK72/ENCIFDO08/ENCIFDO00/TXDE08/TXDE00/HDSL06_LINK	**ENCIFDO08**	**Data output from ENCIF**	**CN3-15**	
H24	VSS				
H25	P29_0/CANTXDP0/MDAT72/ENCIFDI08/ENCIFDI00/RXDE08/RXDE00/HDSL06_SMPL	**ENCIFDI08**	**Data input to ENCIF**	**CN3-17**	
H26	P27_4/MTIOC2B/GTIOC08_3B/GTIOC02_1B/RXD0/SCL0/MISO0/CANTXDP1/SPI_MISO0/HSPI_IO2/ENCIFOE14/DEE10/HDSL04_MOSI2	GTIOC08_3B	Input capture/output compare/PWM output pin	CN26-34	SW4-5: OFF, SW4-6: ON
		HSPI_IO2	IO2 of SHOSTIF	CN64-10	
		RXD0	**RXD0 of USB-to-serial conversion**		**SW4-5: ON, SW4-6: OFF**
H27	P29_3/GTIOC09_1A/ETH2_TXD1/ENCIFDO09/TXDE09/HDSL06_MISO1	**ETH2_TXD1**	**TXD1 of Ethernet port 2**		**SW2-7: ON**
		ENCIFDO09	Data output from ENCIF	CN3-16	SW2-7: OFF

Table 5-9 List of RZ/T2H Pin Function Selections (9)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
J1	DDR_DQA4	**DDR_DQA4**	**Data DQ_A[14] of LPDDR4**		
J2	VSS				
J3	DDR_DMIA0	**DDR_DMIA0**	**DMI_A[1] of LPDDR4**		
J4	DDR_DQA7	**DDR_DQA7**	**Data DQ_A[8] of LPDDR4**		
J5	DDR_DQSA_C0	**DDR_DQSA_C0**	**DQS1_A_C of LPDDR4**		
J6	DDR_VDDQ				
J7	VDD33				
J8	VSS				
J9	VDD1833_6				
J10	AVDD18A_TSU				
J11	VDD33				
J12	VSS				
J13	VDD1833_7				
J14	VSS				
J15	VDD33				
J16	VSS				
J17	VDD1833_0				
J18	VSS				
J19	VDDP_18_33				
J20	VSS				
J21	VDD1833_1				
J22	P30_5/GTIOC09_6A/GMAC2_MDC/ETHSW_MDC/ESC_MDC/SPI_RSPCK3/DUEI07/HDSL07_MISO1	GMAC2_MDC/ETHSW_MDC/ESC_MDC	MDC of Ethernet port 2		SW2-6: OFF
J23	P29_6/GTIOC09_2B/ETH2_TXEN/SPI_SSL22/ENCIFOE10/DEE10/HDSL06_SEL2	**ETH2_TXEN**	**TXEN of Ethernet port 2**		**SW2-7: ON**
		ENCIFOE10	ENCIF output enable	CN3-23	SW2-7: OFF
J24	P30_7/IRQ14/ETHSW_PHYLINK2/ESC_PHYLINK2/SPI_MISO3/SD1_IOVS/MCLK30/SI07#/HDSL07_CLK2	**ETHSW_PHYLINK2/ESC_PHYLINK2**	**LINK of Ethernet port 2**		
J25	P29_1/GTIOC09_0A/ETH2_TXCLK/ENCIFCK09/SCKE09/HDSL06_CLK1	**ETH2_TXCLK**	**TXCLK of Ethernet port 2**		**SW2-7: ON**
		ENCIFCK09	Clock of ENCIF	CN3-12	SW2-7: OFF
J26	P31_1/IRQ13/GTETRGSB/ETH2_RXER/SPI_SSL31/HDSL07_MISO2	**IRQ13**	**MDINT of Ethernet port 2**		
J27	P30_3/IRQ11/GTIOC09_5A/ETH2_RXD3/SPI_MISO2/ENCIFDO11/TXDE11/HDSL07_CLK1	**ETH2_RXD3**	**RXD3 of Ethernet port 2**		**SW2-7: ON**
		ENCIFDO11	Data output from ENCIF	CN3-24	SW2-7: OFF

Table 5-10 List of RZ/T2H Pin Function Selections (10)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
K1	DDR_DQA2	**DDR_DQA2**	**Data DQ_A[10] of LPDDR4**		
K2	DDR_DQA0	**DDR_DQA0**	**Data DQ_A[11] of LPDDR4**		
K3	DDR_DQA1	**DDR_DQA1**	**Data DQ_A[12] of LPDDR4**		
K4	DDR_DQA3	**DDR_DQA3**	**Data DQ_A[13] of LPDDR4**		
K5	DDR_DQSA_T0	**DDR_DQSA_T0**	**DQS1_A_T of LPDDR4**		
K6	VSS				
K7	VDD33				
K8	VSS				
K9	VDD1833_6				
K10	DVDD08A_TSU				
K11	VDD33				
K12	VSS				
K13	VDD1833_7				
K14	VSS				
K15	VDD33				
K16	VSS				
K17	VDD1833_0				
K18	VDD33				
K19	VDD33				
K20	VDDP_18_2				
K21	P30_6/GTIOC09_6B/GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/SPI_MOSI3/TST_OUT07/HDSL07_MOSI1	GMAC2_MDIO/ ETHSW_MDIO/ ESC_MDIO	MDIO of Ethernet port 2		SW2-6: OFF
K22	VSS				
K23	P29_2/GTIOC09_0B/ETH2_TXD0/ENCIFOE09/DEE09/HDSL06_SEL1	**ETH2_TXD0**	**TXD0 of Ethernet port 2**		**SW2-7: ON**
		ENCIFOE09	ENCIF output enable	CN3-14	SW2-7: OFF
K24	P30_4/GTIOC09_5B/ETH2_RXDV/ENCIFDI11/RXDE11/HDSL07_SEL1	**ETH2_RXDV**	**RXDV of Ethernet port 2**		**SW2-7: ON**
		ENCIFDI11	Data input to ENCIF	CN3-26	SW2-7: OFF
K25	P30_1/GTIOC09_4A/ETH2_RXD1/ENCIFCK11/SCKE11/HDSL07_LINK	**ETH2_RXD1**	**RXD1 of Ethernet port 2**		**SW2-7: ON**
		ENCIFCK11	Clock of ENCIF	CN30-20	SW2-7: OFF
K26	VSS				
K27	P30_0/GTIOC09_3B/ETH2_RXD0/ENCIFDI10/RXDE10/HDSL06_MOSI2	**ETH2_RXD0**	**RXD0 of Ethernet port 2**		**SW2-7: ON**
		ENCIFDI10	Data input to ENCIF	CN30-27	SW2-7: OFF

Table 5-11 List of RZ/T2H Pin Function Selections (11)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
L1	VSS				
L2	DDR_CAA1	**DDR_CAA1**	**CA_A[0] of LPDDR4**		
L3	VSS				
L4	VSS				
L5	VSS				
L6	DDR_CKEA1	**DDR_CKEA1**	**CKE_A[1] of LPDDR4**		
L7	VSS				
L8	VDD18_PLL2				
L9	VDD08_PLL2				
L10	VSS				
L11	VDD18_PLL3				
L12	VSS_PLL3				
L13	VDD08_PLL3				
L14	VSS				
L15	VSS				
L16	VSS				
L17	VSS				
L18	VSS				
L19	VSS				
L20	VDD1833_2				
L21	VDD1833_2				
L22	P29_4/IRQ8/GTIOC09_1B/ETH2_TXD2/SPI_SSL20/ENCIFDI09/RXDE09/HDSL06_MOSI1	**ETH2_TXD2**	**TXD2 of Ethernet port 2**		**SW2-7: ON**
		ENCIFDI09	Data input to ENCIF	CN3-18	SW2-7: OFF
L23	P29_5/IRQ9/GTIOC09_2A/ETH2_TXD3/SPI_SSL21/ENCIFCK10/SCKE10/HDSL06_CLK2	**ETH2_TXD3**	**TXD3 of Ethernet port 2**		**SW2-7: ON**
		ENCIFCK10	Clock of ENCIF	CN3-21	SW2-7: OFF
L24	P31_0/ETH2_REFCLK/RMII2_REFCLK/GTETRGSA/SPI_SSL30/HDSL07_SEL2	**ETH2_REFCLK**	**REFCLK of Ethernet port 2**		
L25	P29_7/GTIOC09_3A/ETH2_RXCLK/SPI_SSL23/ENCIFDO10/TXDE10/HDSL06_MISO2	**ETH2_RXCLK**	**RXCLK of Ethernet port 2**		**SW2-7: ON**
		ENCIFDO10	Data output from ENCIF	CN3-25	SW2-7: OFF
L26	P30_2/IRQ10/GTIOC09_4B/ETH2_RXD2/SPI_MOSI2/ENCIFOE11/DEE11/HDSL07_SMPL	**ETH2_RXD2**	**RXD2 of Ethernet port 2**		**SW2-7: ON**
		ENCIFOE11	ENCIF output enable	CN3-22	SW2-7: OFF
L27	P32_6/GTIOC10_2A/GTIOC01_2A/SPI_SSL10/ENCIFCK11/SCKE11/HDSL09_SMPL	**GTIOC01_2A**	**Input capture/output compare/PWM output pin**	**CN24-19**	
		SPI_SSL10	**CS for use with mikroBUS™**	**CN53-3**	

Table 5-12 List of RZ/T2H Pin Function Selections (12)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
M1	DDR_CKA_C	**DDR_CKA_C**	**CK_A_C of LPDDR4**		
M2	DDR_CAA3	**DDR_CAA3**	**CA_A[1] of LPDDR4**		
M3	DDR_CAA4	**DDR_CAA4**	**CA_A[3] of LPDDR4**		
M4	DDR_CSA0	**DDR_CSA0**	**CS_A[0] of LPDDR4**		
M5	DDR_CSA1	**DDR_CSA1**	**CS_A[1] of LPDDR4**		
M6	DDR_CKEA0	**DDR_CKEA0**	**CKE_A[0] of LPDDR4**		
M7	VSS				
M8	VSS_PLL2				
M9	VDD08				
M10	VSS				
M11	VDD08				
M12	VSS				
M13	VDD08				
M14	VSS				
M15	VDD08				
M16	VSS				
M17	VDD08				
M18	VSS				
M19	VDD08_PLL0				
M20	VSS				
M21	VSS				
M22	P32_2/GTIOC10_0A/GTIOC01_0A/SPI_SSL03/ENCIFCK10/SCKE10/HDSL08_SEL2	**P32_2**	**Control of user LED1**		**SW5-1: OFF, SW5-2: ON**
			SD1 power selection		SW5-1: ON, SW5-2: OFF, SW5-3: ON, SW5-4: OFF
M23	P32_1/SPI_SSL02/ENCIFDI15/ENCIFDI01/RXDE11/RXDE01/HDSL08_CLK2	**ENCIFDI15**	**Data input to ENCIF**	**CN10-18**	
M24	VSS				
M25	P32_0/SPI_SSL01/ENCIFDO15/ENCIFDO01/TXDE11/TXDE01/HDSL08_MOSI1	**ENCIFDO15**	**Data output from ENCIF**	**CN10-16**	
M26	P31_7/GMAC2_PTPTRG1/SPI_SSL00/ENCIFOE15/ENCIFOE01/DEE11/DEE01/HDSL08_MISO1	**GMAC2_PTPTRG1**	**PTPTRG1 of GMAC2**	**CN23-6**	
		SPI_SSL00	**SSL for use with PMOD1**	**CN50-1**	
		ENCIFOE15	**ENCIF output enable**	**CN10-14**	
M27	P32_5/GTIOC10_1B/GTIOC01_1B/SPI_MISO1/ENCIFDI10/RXDE10/HDSL09_LINK	**GTIOC01_1B**	**Input capture/output compare/PWM output pin**	**CN24-18**	
		SPI_MISO1	**MISO for use with mikroBUS™**	**CN53-5**	

Table 5-13 List of RZ/T2H Pin Function Selections (13)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
N1	DDR_CKA_T	**DDR_CKA_T**	**CK_A_T of LPDDR4**		
N2	VSS				
N3	DDR_CAA2	**DDR_CAA2**	**CA_A[2] of LPDDR4**		
N4	VSS				
N5	DDR_CAA5	**DDR_CAA5**	**CA_A[5] of LPDDR4**		
N6	VSS				
N7	DDR_VDDQ				
N8	DDR_VAA				
N9	VSS				
N10	VDD08				
N11	VSS				
N12	VDD08				
N13	VSS				
N14	VDD08				
N15	VSS				
N16	VDD08				
N17	VSS				
N18	VDD08				
N19	VSS_PLL0				
N20	VDD18_PLL0				
N21	VSS				
N22	P32_4/GTIOC10_1A/GTIOC01_1A/ SPI_MOSI1/ENCIFDO10/TXDE10/H DSL08_MOSI2	**GTIOC01_1A**	**Input capture/output compare/PWM output pin**	**CN24-17**	
		SPI_MOSI1	**MOSI for use with mikroBUS™**	**CN53-6**	
N23	P32_3/GTIOC10_0B/GTIOC01_0B/ SPI_RSPCK1/ENCIFOE10/DEE10/ HDSL08_MISO2	**P32_3**	**GMAC_RESETOUT3# of Ethernet port 3**		
		SPI_RSPCK1	**SCK for use with mikroBUS™**	**CN53-4**	
N24	P32_7/GTIOC10_2B/GTIOC01_2B/ SPI_SSL11/ENCIFOE11/DEE11/HD SL09_CLK1	**GTIOC01_2B**	**Input capture/output compare/PWM output pin**	**CN24-20**	
N25	P31_4/DREQ/POE8#/ETH2_CRS/E THSW_PTPOUT2/ESC_SYNC0/SPI _RSPCK0/SPI_SSL30/MCLK81/MD AT31/HSPI_IO6/ENCIFDO09/TXDE 09/HDSL08_SMPL/POUTB	**ETH2_CRS**	**CRS of Ethernet port 2**		**SW2-7: ON**
		MCLK81	Clock of DSMIF	CN22-25	SW2-7: OFF
		HSPI_IO6	IO6 of SHOSTIF	CN64-6	
		SPI_RSPCK0	SCK for use with PMOD1	CN50-4	SW2-7: OFF E3: Short-circuit, E5: Open-circuit

N26	P31_3/POE4#/ETH2_RXER/ETHSW_TDMAOUT1/ESC_LEDERR/SPI_SSL33/MDAT80/MCLK31/HSPI_IO5/ENCIFOE09/DEE09/HDSL08_LINK	**ETH2_RXER**	**RXER of Ethernet port 2**		**SW2-7: ON**
		MDAT80	Data of DSMIF	CN22-28	SW2-7: OFF
		HSPI_IO5	IO5 of SHOSTIF	CN64-7	
N27	P31_2/POE0#/ETH2_TXER/SPI_SSL32/MCLK80/MDAT30/HSPI_IO4/ENCIFCK09/SCKE09/HDSL07_MOSI2/POUTA	**ETH2_TXER**	**TXER of Ethernet port 2**		**SW2-7: ON**
		MCLK80	Clock of DSMIF	CN22-27	SW2-7: OFF
		HSPI_IO4	IO4 of SHOSTIF	CN64-8	

Table 5-14 List of RZ/T2H Pin Function Selections (14)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
P1	VSS				
P2	DDR_CKEB1	**DDR_CKEB1**	**CKE_B[1] of LPDDR4**		
P3	DDR_CAB0	**DDR_CAB0**	**CA_B[2] of LPDDR4**		
P4	DDR_CAA0	**DDR_CAA0**	**CA_A[4] of LPDDR4**		
P5	DDR_VDDQ				
P6	VSS				
P7	DDR_RESET_N	**DDR_RESET_N**	**RESET_N of LPDDR4**		
P8	DDR_ATEST	**DDR_ATEST**			**NC**
P9	VDD08				
P10	VSS				
P11	VDD08				
P12	VSS				
P13	VDD08				
P14	VSS				
P15	VDD08				
P16	VSS				
P17	VDD08				
P18	VSS				
P19	VSS				
P20	VSS				
P21	VDDP_18_33				
P22	VSS				
P23	P33_1/GTIOC10_3B/SPI_SSL13/MDAT82/ENCIFDI11/RXDE11/HDSL09_MISO1	**MDAT82**	**Data of DSMIF**	**CN22-24**	
P24	P33_0/GTIOC10_3A/SPI_SSL12/MCLK82/ENCIFDO11/TXDE11/HDSL09_SEL1	**MCLK82**	**Clock of DSMIF**	**CN22-23**	
P25	P31_6/A16/TEND/POE11#/GMAC2_PTPTRG0/ETHSW_TDMAOUT0/ESC_LEDRUN/SPI_MISO0/MDAT32/ENCIFCK15/ENCIFCK01/SCKE11/SCKE01/HDSL08_SEL1	**GMAC2_PTPTRG0**	**PTPTRG0 of GMAC2**	**CN23-5**	
		ENCIFCK15	**Clock of ENCIF**	**CN10-12**	
		SPI_MISO0	**MISO for use with PMOD1**	**CN50-3**	**E2: Short-circuit,** **E4: Open-circuit**
P26	P31_5/DACK/POE10#/ETH2_COL/ETHSW_PTPOUT3/ESC_SYNC1/SPI_MOSI0/SPI_SSL31/MDAT81/MCLK32/HSPI_IO7/ENCIFDI09/RXDE09/HDSL08_CLK1/POUTZ	**ETH2_COL**	**COL of Ethernet port 2**		**SW2-7: ON**
		SPI_MOSI0	MOSI for use with PMOD1	CN50-2	SW2-7: OFF
		MDAT81	Data of DSMIF	CN22-26	
		HSPI_IO7	IO7 of SHOSTIF	CN64-5	
P27	P34_4/CS2#/GTADSM05_0/GTIOC03_2A/ETH3_RXD3/RXD3/SCL3/MISO3/SPI_SSL22/SD1_IOVS/ADTRG0#/ENCIFDO07/TXDE07/HDSL10_MOSI1	**ETH3_RXD3**	**RXD3 of Ethernet port 3**		**SW2-8: ON**
		CS2#	CS2# of external bus	CN13-34	SW2-8: OFF
		ENCIFDO07	Data output from ENCIF	CN3-6	

Table 5-15 List of RZ/T2H Pin Function Selections (15)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
R1	DDR_CKB_T	**DDR_CKB_T**	**CK_B_T of LPDDR4**		
R2	DDR_CKEB0	**DDR_CKEB0**	**CKE_B[0] of LPDDR4**		
R3	VSS				
R4	VSS				
R5	DDR_VDDQ				
R6	VSS				
R7	DDR_DTEST	**DDR_DTEST**			**NC**
R8	DDR_ZN	**DDR_ZN**			**120-Ω pull-down**
R9	VSS				
R10	VDD08				
R11	VSS				
R12	VDD08				
R13	VSS				
R14	VDD08				
R15	VSS				
R16	VDD08				
R17	VSS				
R18	VDD08				
R19	VDDP_18_X				
R20	VDD33				
R21	VSS				
R22	P34_1/A23/GTADSM03_1/GTIOC03_0B/ETH3_RXD0/SPI_MISO2/ENCIFDI06/RXDE06/HDSL10_CLK1	**ETH3_RXD0**	**RXD0 of Ethernet port 3**		**SW2-8: ON**
		A23	Address A23 of external bus	CN13-18	SW2-8: OFF
		ENCIFDI06	Data input to ENCIF	CN3-9	
R23	P34_6/ETH3_REFCLK/RMII3_REFCLK/CS5#/ETH1_RXER/ESC_I2CDATA/IIC_SDA1/SPI_RSPCK3/ADTRG2#/DUEI08/HDSL10_SEL2	**ETH3_REFCLK**	**REFCLK of Ethernet port 3**		
R24	P33_2/A16/GTADSM00_0/ETH3_TXCLK/SCK1/SPI_RSPCK1/SPI_SSL30/MCLK50/ENCIFCK01/SCKE01/HDSL09_MOSI1	**ETH3_TXCLK**	**TXCLK of Ethernet port 3**		**SW2-8: ON**
		A16	Address A16 of external bus	CN13-4	SW2-8: OFF
		ENCIFCK01	Clock of ENCIF	CN2-2	
R25	P33_6/IRQ15/A20/GTADSM02_0/ETH3_TXD3/TXD2/SDA2/MOSI2/SPI_SSL11/SPI_SSL00/MCLK52/ENCIFCK06/SCKE06/HDSL09_MOSI2	**ETH3_TXD3**	**TXD3 of Ethernet port 3**		**SW2-8: ON**
		A20	Address A20 of external bus	CN13-12	SW2-8: OFF
		ENCIFCK06	Clock of ENCIF	CN3-3	
R26	P33_7/A21/GTADSM02_1/ETH3_TXEN/SPI_RSPCK2/MDAT52/ENCIFOE06/DEE06/HDSL10_LINK	**ETH3_TXEN**	**TXEN of Ethernet port 3**		**SW2-8: ON**
		A21	Address A21 of external bus	CN13-14	SW2-8: OFF
		ENCIFOE06	ENCIF output enable	CN3-5	
R27	P34_5/CS3#/GTADSM05_1/GTIOC03_2B/ETH3_RXDV/ESC_I2CCLK/TXD3/SDA3/MOSI3/IIC_SCL1/SPI_SSL23/ADTRG1#/ENCIFDI07/RXDE07/HDSL10_CLK2	**ETH3_RXDV**	**RXDV of Ethernet port 3**		**SW2-8: ON**
		CS3#	CS3# of external bus	CN13-36	SW2-8: OFF
		ENCIFDI07	Data input to ENCIF	CN3-8	

Table 5-16 List of RZ/T2H Pin Function Selections (16)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
T1	DDR_CKB_C	**DDR_CKB_C**	**CK_B_C of LPDDR4**		
T2	DDR_CAB1	**DDR_CAB1**	**CA_B[0] of LPDDR4**		
T3	DDR_VDDQ				
T4	DDR_CAB2	**DDR_CAB2**	**CA_B[3] of LPDDR4**		
T5	DDR_CAB5	**DDR_CAB5**	**CA_B[1] of LPDDR4**		
T6	DDR_CSB0	**DDR_CSB0**	**CS_B[0] of LPDDR4**		
T7	VSS				
T8	VSS				
T9	VDD08				
T10	VSS				
T11	VDD08				
T12	VSS				
T13	VDD08				
T14	VSS				
T15	VDD08				
T16	VSS				
T17	VDD08				
T18	VSS				
T19	VDD33_X				
T20	VSS				
T21	VDD1833_3				
T22	VDDP_18_3				
T23	P34_2/A24/GTADSM04_0/GTIOC03_1A/ETH3_RXD1/SPI_SSL20/ENCIFCK07/SCKE07/HDSL10_SEL1	**ETH3_RXD1**	**RXD1 of Ethernet port 3**		**SW2-8: ON**
		A24	Address A24 of external bus	CN13-22	SW2-8: OFF
		ENCIFCK07	Clock of ENCIF	CN3-2	
T24	VSS				
T25	P33_5/IRQ14/A19/GTADSM01_1/ETH3_TXD2/RXD2/SCL2/MISO2/SPI_SSL10/SPI_MISO0/MDAT51/ENCIFDI01/RXDE01/HDSL09_MISO2	**ETH3_TXD2**	**TXD2 of Ethernet port 3**		**SW2-8: ON**
		A19	Address A19 of external bus	CN13-10	SW2-8: OFF
		ENCIFDI01	Data input to ENCIF	CN2-8	
T26	P35_1/TEND/GTADSM07_0/ETH3_CRS/SPI_SSL30/SPI_MISO1/MCLK90/DUEI09/HDSL11_LINK	**ETH3_CRS**	**CRS of Ethernet port 3**		**SW2-8: ON**
		MCLK90	Clock of DSMIF	CN19-7	SW2-8: OFF
T27	XTALSEL	**XTALSEL**	**Selection of EXTCLKIN or XTAL and EXTAL**		

Table 5-17 List of RZ/T2H Pin Function Selections (17)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
U1	DDR_CAB3	**DDR_CAB3**	**CA_B[4] of LPDDR4**		
U2	VSS				
U3	DDR_CAB4	**DDR_CAB4**	**CA_B[5] of LPDDR4**		
U4	DDR_DQB0	**DDR_DQB0**	**DQ_B[12] of LPDDR4**		
U5	VSS				
U6	DDR_CSB1	**DDR_CSB1**	**CS_B[1] of LPDDR4**		
U7	VSS				
U8	VSS				
U9	VSS				
U10	VDD08				
U11	VSS				
U12	VDD08				
U13	VSS_PLL1				
U14	VSS_PLL4				
U15	VSS				
U16	VDD08				
U17	VSS				
U18	VSS				
U19	VSS				
U20	VSS				
U21	VDD1833_3				
U22	P35_6/GTADSM09_1/TXD4/SDA4/MOSI4/SPI_SSL12/MDAT92/SI10#/HDSL11_MOSI1	**P35_6**	**User DIP switch SW3**		**SW1-3: ON**
		MDAT92	Data of DSMIF	CN19-4	SW1-3: OFF
U23	P34_3/A25/GTADSM04_1/GTIOC03_1B/ETH3_RXD2/SPI_SSL21/SD1_PWEN/ENCIFOE07/DEE07/HDSL10_MISO1	**ETH3_RXD2**	**RXD2 of Ethernet port 3**		**SW2-8: ON**
		A25	Address A25 of external bus	CN13-24	SW2-8: OFF
		ENCIFOE07	ENCIF output enable	CN3-4	
U24	P33_4/IRQ13/A18/GTADSM01_0/ETH3_TXD1/TXD1/SDA1/MOSI1/SPI_MISO1/SPI_MOSI0/MCLK51/PCIE_RSTOUT1B/ENCIFDO01/TXDE01/HDSL09_SEL2	**ETH3_TXD1**	**TXD1 of Ethernet port 3**		**SW2-8: ON**
		A18	Address A18 of external bus	CN13-8	SW2-8: OFF
		ENCIFDO01	Data output from ENCIF	CN2-6	
		PCIE_RSTOUT1B	Reset output from PCIe x1 connector	CN8-A11	SW2-8: OFF, **SW15-2: ON**
U25	P33_3/IRQ12/A17/GTADSM00_1/ETH3_TXD0/RXD1/SCL1/MISO1/SPI_MOSI1/SPI_RSPCK0/MDAT50/PCIE_RSTOUT0B/ENCIFOE01/DEE01/HDSL09_CLK2	**ETH3_TXD0**	**TXD0 of Ethernet port 3**		**SW2-8: ON**
		A17	Address A17 of external bus	CN13-6	SW2-8: OFF
		ENCIFOE01	ENCIF output enable	CN2-4	
		PCIE_RSTOUT0B	Reset output from PCIe x4 connector	CN32-A11	SW2-8: OFF, **SW15-1: ON**
U26	VSS				
U27	EXTCLKIN	**EXTCLKIN**	**Connection of crystal oscillator**		**SW1-1: ON**

Table 5-18 List of RZ/T2H Pin Function Selections (18)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
V1	DDR_DQB2	**DDR_DQB2**	**DQ_B[11] of LPDDR4**		
V2	DDR_DQB1	**DDR_DQB1**	**DQ_B[13] of LPDDR4**		
V3	VSS				
V4	DDR_DQB3	**DDR_DQB3**	**DQ_B[14] of LPDDR4**		
V5	DDR_DQSB_T0	**DDR_DQSB_T0**	**DQS1_B_T of LPDDR4**		
V6	VSS				
V7	VSS				
V8	VSS				
V9	VDD1833_4				
V10	VDD33				
V11	VDDP_18_4				
V12	VDDP_18_5				
V13	VDD18_PLL1				
V14	VDD18_PLL4				
V15	VDD08				
V16	VSS				
V17	OTPVDD08				
V18	VSS				
V19	PCIE_VDD08A_L0				
V20	VSS				
V21	VSS				
V22	P35_3/GTADSM08_0/SPI_SSL32/SPI_MOSI1/MCLK91/ADTRG0#/SI09#/HDSL11_CLK1	**P35_3**	**User DIP switch SW0**		**SW1-3: ON**
		MCLK91	Clock of DSMIF	CN19-5	SW1-3: OFF
V23	P34_0/A22/GTADSM03_0/GTIOC03_0A/ETH3_RXCLK/SPI_MOSI2/ENCIFDO06/TXDE06/HDSL10_SMPL	**ETH3_RXCLK**	**RXCLK of Ethernet port 3**		**SW2-8: ON**
		A22	Address A22 of external bus	CN13-16	SW2-8: OFF
		ENCIFDO06	Data output from ENCIF	CN3-7	
V24	P35_5/GTADSM09_0/RXD4/SCL4/MISO4/SPI_RSPCK1/MCLK92/TST_OUT10/HDSL11_MISO1	**P35_5**	**User DIP switch SW2**		**SW1-3: ON**
		MCLK92	Clock of DSMIF	CN19-3	SW1-3: OFF
V25	P35_0/DACK/GTADSM06_1/ETH3_RXER/SPI_MISO3/SI08#/HDSL10_MOSI2	**ETH3_RXER**	**RXER of Ethernet port 3**		**SW2-8: ON**
V26	VSS				
V27	XTAL	XTAL	Connection of crystal resonator		SW1-1: OFF

Table 5-19 List of RZ/T2H Pin Function Selections (19)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
W1	VSS				
W2	DDR_DQB4	**DDR_DQB4**	**DQ_B[10] of LPDDR4**		
W3	DDR_DQB7	**DDR_DQB7**	**DQ_B[9] of LPDDR4**		
W4	DDR_DMIB0	**DDR_DMIB0**	**DMI_B[1] of LPDDR4**		
W5	DDR_DQSB_C0	**DDR_DQSB_C0**	**DQS1_B_C of LPDDR4**		
W6	VSS				
W7	VSS				
W8	VSS				
W9	VDD1833_4				
W10	VDD33				
W11	VDDP_18_33				
W12	VDDP_18_33				
W13	VDD08_PLL1				
W14	VDD08_PLL4				
W15	VSS				
W16	VSS				
W17	OTPVDD18				
W18	VSS				
W19	PCIE_VDD08A_L0				
W20	VSS				
W21	VSS				
W22	VSS				
W23	P34_7/IRQ14/DREQ/GTADSM06_0/ETH3_TXER/ESC_RESETOUT#/SPI_MOSI3/TST_OUT08/HDSL10_MISO2	**ETH3_TXER**	**TXER of Ethernet port 3**		**SW2-8: ON**
W24	P35_4/GTADSM08_1/SPI_SSL33/SPI_SSL11/MDAT91/ADTRG1#/DUEI10/HDSL11_SEL1	**P35_4**	**User DIP switch SW1**		**SW1-3: ON**
		MDAT91	Data of DSMIF	CN19-6	SW1-3: OFF
W25	P35_2/GTADSM07_1/ETH3_COL/SPI_SSL31/SPI_SSL10/MDAT90/ADTRG2#/TST_OUT09/HDSL11_SMPL	**ETH3_COL**	**COL of Ethernet port 3**		**SW2-8: ON**
		MDAT90	Data of DSMIF	CN19-8	SW2-8: OFF
W26	VSS				
W27	EXTAL	EXTAL	Connection of crystal resonator		SW1-1: OFF

Table 5-20 List of RZ/T2H Pin Function Selections (20)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
Y1	DDR_DQB6	DDR_DQB6	DQ_B[15] of LPDDR4		
Y2	DDR_VDDQ				
Y3	DDR_DQB5	DDR_DQB5	DQ_B[8] of LPDDR4		
Y4	VSS				
Y5	VSS				
Y6	VSS				
Y7	VSS				
Y8	VSS				
Y9	VSS				
Y10	VSS				
Y11	VSS				
Y12	VDD33				
Y13	VDD33				
Y14	VDD1833_5				
Y15	VDD1833_5				
Y16	VSS				
Y17	USB_USVDD18				
Y18	USB_USVDD33				
Y19	PCIE_VDD08A_L1				
Y20	PCIE_VDD18A_L1				
Y21	PCIE_VDD18A_L0				
Y22	VSS				
Y23	VSS				
Y24	VSS				
Y25	VSS				
Y26	VSS				
Y27	VSS				

Table 5-21 List of RZ/T2H Pin Function Selections (21)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
AA1	DDR_DQB8	**DDR_DQB8**	**DQ_B[5] of LPDDR4**		
AA2	VSS				
AA3	DDR_DQB15	**DDR_DQB15**	**DQ_B[4] of LPDDR4**		
AA4	VSS				
AA5	DDR_DQSB_T1	**DDR_DQSB_T1**	**DQS0_B_T of LPDDR4**		
AA6	VSS				
AA7	P06_5/IRQ11/GTETRGC/IIC_SDA1/ XSPI0_IO7/HDSL05_SEL1	**XSPI0_IO7**	**Data IO7 of XSPI0**		
AA8	P05_1/IRQ3/XSPI0_CKP/DUEI06/H DSL04_SMPL	**XSPI0_CKP**	**Clock CKP of XSPI0**		
AA9	P05_2/IRQ4/IIC_SCL2/XSPI0_CKN/ TST_OUT06/HDSL04_CLK1	P05_2	CLKREQ of PCIe x1 connector		SW15-2: OFF, **E20: Short-circuit**
		IRQ4	**PRSNT of PCIe x1 connector**		**SW15-2: ON**, **E20: Short-circuit**
		XSPI0_CKN	**Clock CKN of XSPI0**		
AA10	P05_0/IRQ2/MTIOC6C/MTIOC0B/G TIOC03_4B/IIC_SDA1/ENCIFDI03/ RXDE03/HDSL04_LINK	**GTIOC03_4B**	**Input capture/output compare/PWM output pin**	**CN25-12**	
		IIC_SDA1	**SDA of I2C**	**CN15-1, CN51-2, CN52-3, CN54-6**	
				CN50-4	E3: Open-circuit, E5: Short-circuit
		ENCIFDI03	**Data input to ENCIF**	**CN2-18**	
AA11	VSS				
AA12	P04_2/MTIOC7C/GTIOC03_1B/CM TW0_TOC1/DUEI05/HDSL03_MISO 1	**MTIOC7C**	**PWM for use with mikroBUS™**	**CN54-1**	
		GTIOC03_1B	**Input capture/output compare/PWM output pin**	**CN25-6**	
AA13	P02_2/IRQ9/MTIOC6A/MTIOC1A/G TIOC01_4A/ETH3_CRS/IIC_SDA2/ XSPI1_IO6/MCLK22/USB_VBUSEN /ENCIFDO01/TXDE01/HDSL01_MI SO2	GTIOC01_4A	Input capture/output compare/PWM output pin	CN24-23	SW1-6: OFF
		MCLK22	Clock of DSMIF	CN21-23	
		XSPI1_IO6	**IO6 of SPI expansion connector**	**CN63-6**	**SW1-6: ON**
AA14	VSS				
AA15	VSS				
AA16	USB_USDVDD				
AA17	USB_USVDD18				
AA18	USB_USVDD33				
AA19	PCIE_VDD08A_L1				

AA20	PCIE_VDD18A_L1				
AA21	PCIE_VDD18A_L0				
AA22	AVSS_ADC0				
AA23	AVDD_ADC0				
AA24	AVSSIO_ADC0				
AA25	AVSSIO_ADC0				
AA26	AN002	**AN002**	**Input to A/D converter (AN002)**	**CN41-6**	
AA27	AN000	**AN000**	**Input to potentiometer**		**SW17-1: ON, SW17-2: OFF**
			Input to A/D converter (AN000)	CN41-2	SW17-1: OFF, SW17-2: ON

Table 5-22 List of RZ/T2H Pin Function Selections (22)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
AB1	DDR_DQB14	**DDR_DQB14**	**DQ_B[6] of LPDDR4**		
AB2	DDR_DQB9	**DDR_DQB9**	**DQ_B[1] of LPDDR4**		
AB3	DDR_DMIB1	**DDR_DMIB1**	**DMI_B[0] of LPDDR4**		
AB4	DDR_DQB10	**DDR_DQB10**	**DQ_B[0] of LPDDR4**		
AB5	DDR_DQSB_C1	**DDR_DQSB_C1**	**DQS0_B_C of LPDDR4**		
AB6	BSCANP	**BSCANP**	**Boundary scan enable**		
AB7	P06_3/IRQ9/GTETRGA/IIC_SDA0/XSPI0_IO5/TST_OUT09/HDSL05_SMPL	**XSPI0_IO5**	**Data IO5 of XSPI0**		
AB8	P06_4/IRQ10/GTETRGB/IIC_SCL1/XSPI0_IO6/SI09#/HDSL05_CLK1	**XSPI0_IO6**	**Data IO6 of XSPI0**		
AB9	P07_7/IIC_SCL0/XSPI0_WP0#/MCLK10/ENCIFDO05/TXDE05/HDSL06_CLK1	**MCLK10**	**Clock of DSMIF**	**CN21-17**	
AB10	P03_4/IRQ14/D12/MTCLKB/MTIOC8D/GTIOC02_3B/GTADSM09_1/CMTW1_TOC1/RTCAT1HZ/IIC_SDA1/ENCIFOE02/DEE02/HDSL02_MISO2	**D12**	**Data D12 of external bus**	**CN17-27**	
		ENCIFOE02	**ENCIF output enable**	**CN2-13**	
AB11	P03_3/IRQ13/D11/MTCLKA/MTIOC8C/GTIOC02_3A/GTADSM09_0/CMTW1_TIC1/IIC_SCL1/ENCIFCK02/SCKE02/HDSL02_SEL2	**D11**	**Data D11 of external bus**	**CN17-25**	
		ENCIFCK02	**Clock of ENCIF**	**CN2-11**	
AB12	P03_7/MTIOC6B/MTIOC1B/GTIOC03_0A/CMTW0_TIC0/DUEI04/HDSL03_SMPL	**GTIOC03_0A**	**Input capture/output compare/PWM output pin**	**CN25-3**	
AB13	P02_1/IRQ8/MTCLKD/MTIOC0D/GTIOC01_3B/ETH3_RXER/IIC_SCL2/XSPI1_IO5/MDAT21/ENCIFOE01/DEE01/HDSL01_SEL2	**XSPI1_IO5**	**IO5 of SPI expansion connector**	**CN63-7**	**SW1-6: ON**
		GTIOC01_3B	Input capture/output compare/PWM output pin	CN24-22	SW1-6: OFF
AB14	P01_3/MTIOC6D/MTIC5U/GTIOC01_0B/GTIOC04_0B/XSPI1_DS/TST_OUT02/HDSL01_SMPL	**GTIOC01_0B**	**Input capture/output compare/PWM output pin**	**CN24-16**	
AB15	P00_5/MTIOC4D/MTIOC8C/GTIOC00_2B/USB_VBUSEN/SI01#/HDSL00_MOSI1	**GTIOC00_2B**	**Input capture/output compare/PWM output pin**	**CN24-8**	
AB16	USB_USDVDD				
AB17	VSS				
AB18	VSS				
AB19	VSS				
AB20	VSS				
AB21	PCIE_VDD18A_CMN				
AB22	AVSS_ADC1				
AB23	AVDD_ADC1				
AB24	AVDDIO_ADC0				

AB25	AVDDREF_ADC0				
AB26	AN001	**AN001**	**Input to A/D converter (AN001)**	**CN41-4**	
AB27	AN003	**AN003**	**Input to A/D converter (AN003)**	**CN41-8**	

Table 5-23 List of RZ/T2H Pin Function Selections (23)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
AC1	DDR_DQB12	**DDR_DQB12**	**DQ_B[3] of LPDDR4**		
AC2	VSS				
AC3	DDR_DQB13	**DDR_DQB13**	**DQ_B[2] of LPDDR4**		
AC4	DDR_DQB11	**DDR_DQB11**	**DQ_B[7] of LPDDR4**		
AC5	VSS				
AC6	P06_1/XSPI0_IO3/SI08#/HDSL04_MOSI2	**XSPI0_IO3**	**Data IO3 of XSPI0**		
AC7	P07_6/IIC_SDA2/XSPI0_ECS1#/MDAT02/ENCIFOE05/DEE05/HDSL06_SMPL	**MDAT02**	**Data of DSMIF**	**CN21-4**	
AC8	P07_4/IIC_SDA1/XSPI0_INT1#/MDAT01/ENCIFDI04/ENCIFDI12/RXDE04/RXDE08/HDSL05_MOSI2	**MDAT01**	**Data of DSMIF**	**CN21-6**	
AC9	P03_2/IRQ12/D10/MTIOC4D/MTIOC1A/GTIOC02_2B/GTADSM08_1/CMTW1_TOC0/ENCIFDI02/RXDE02/HDSL02_CLK2	**D10**	**Data D10 of external bus**	**CN17-23**	
		GTIOC02_2B	**Input capture/output compare/PWM output pin**	**CN24-32**	
AC10	P03_1/D9/MTIOC4B/MTIOC1B/GTIOC02_2A/GTADSM08_0/CMTW1_TIC0/ENCIFDO02/TXDE02/HDSL02_MOSI1	**D9**	**Data D9 of external bus**	**CN17-21**	
		GTIOC02_2A	**Input capture/output compare/PWM output pin**	**CN24-31**	
AC11	P04_7/IRQ1/MTIOC6A/MTIOC0A/GTIOC03_4A/IIC_SCL1/ENCIFDO03/TXDE03/HDSL03_MOSI2	**GTIOC03_4A**	**Input capture/output compare/PWM output pin**	**CN25-11**	
		IIC_SCL1	**SCL of I2C**	**CN15-2, CN51-1, CN52-4, CN54-5**	
				CN50-3	E2: Open-circuit, E4: Short-circuit
		ENCIFDO03	**Data output from ENCIF**	**CN2-16**	
AC12	P03_5/IRQ15/MTIOC3A/MTIC5W/GTIOC02_4A/IIC_SCL2/ENCIFDO02/TXDE02/HDSL02_MOSI2	**GTIOC02_4A**	**Input capture/output compare/PWM output pin**	**CN24-35**	
		ENCIFDO02	**Data output from ENCIF**	**CN2-15**	
AC13	P01_7/MTIOC7D/MTIOC0B/GTIOC01_2B/GTIOC04_2B/XSPI1_IO3/SI03#/HDSL01_MOSI1	**XSPI1_IO3**	**IO3 of QSPI and SPI expansion connector**	**CN63-9**	**SW1-6: ON**
		GTIOC04_2B	Input capture/output compare/PWM output pin	CN25-20	SW1-6: OFF
AC14	P02_0/IRQ7/MTCLKC/MTIOC0C/GTIOC01_3A/ETH3_TXER/IIC_SDA1/XSPI1_IO4/MCLK21/ENCIFCK01/SCKE01/HDSL01_CLK2	**XSPI1_IO4**	**IO4 of SPI expansion connector**	**CN63-8**	**SW1-6: ON**
		GTIOC01_3A	Input capture/output compare/PWM output pin	CN24-21	SW1-6: OFF
AC15	P00_2/IRQ1/D2/MTIOC4A/GTIOC00_1A/ETH3_CRS/ADTRG0#/USB_EXICEN/SI00#/HDSL00_CLK1	D2	Data D2 of external bus	CN17-5	SW1-5: OFF
		GTIOC00_1A	Input capture/output compare/PWM output pin	CN24-5	

AC16	VSS				
AC17	USB_TXRTUNE	**USB_TXRTUNE**	**200-Ω pull-down**		
AC18	VSS				
AC19	PCIE_REFCLK_N1	**PCIE_REFCLK_N1**	**Reference clock of PCIe ch1**		
AC20	PCIE_REFCLK_P0	**PCIE_REFCLK_P0**	**Reference clock of PCIe ch0**		
AC21	PCIE_VDD18A_CMN				
AC22	AVDD_ADC2				
AC23	AVDDIO_ADC2				
AC24	AVDDIO_ADC1				
AC25	AVDDREF_ADC1				
AC26	AN103	**AN103**	**Input to A/D converter (AN103)**	**CN42-8**	
AC27	AN100	**AN100**	Input to A/D converter (AN100)	CN42-2	SW18-1: ON, SW18-2: OFF
			Input to A/D converter for use with mikroBUS™	**CN53-1**	**SW18-1: OFF, SW18-2: ON**

Table 5-24 List of RZ/T2H Pin Function Selections (24)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
AD1	MDX	**MDX**	**MDX setting input**		
AD2	P08_6/SEI/CKIO/GTIOC08_3A/GTETRGSB/IIC_SDA1/SD1_IOVS/MDAT02/MCLK11/DUEI11/HDSL06_MOSI2	SEI	Switch SW9 of SEI		SW2-3: OFF, **E1: Short-circuit, E7: Short-circuit**
		CKIO	CKIO of external bus	CN17-2	SW2-3: OFF
		MCLK11	Clock of DSMIF	CN21-15	SW2-3: OFF, **E7: Short-circuit**
		SD1_IOVS	**SD1 power selection**		**SW2-3: ON, SW5-3: OFF, SW5-4: ON**
AD3	P08_3/TCK/SI10#/HDSL06_CLK2	**TCK**	**TCK of debugging interface**	**CN60-4 CN61-4**	
AD4	RESN	**RESN**	**Reset input**		
AD5	P08_2/TDI/TST_OUT10/HDSL06_MOSI1	**TDI**	**TDI of debugging interface**	**CN60-8 CN61-8**	
AD6	P05_6/XSPI0_IO0/SI07#/HDSL04_CLK2	**XSPI0_IO0**	**Data IO0 of XSPI0**		
AD7	P08_0/RTCAT1HZ/IIC_SDA0/XSPI0_WP1#/MDAT10/MBX_HINT#/ENCIFDI05/RXDE05/HDSL06_SEL1	**MDAT10**	**Data of DSMIF**	**CN21-18**	
AD8	VSS				
AD9	P02_6/D6/MTIOC3D/MTIOC8B/GTIOC02_0B/GTADSM06_1/CMTW0_TOC0/SD0_IOVS/MDAT00/HDSL02_CLK1/POUTB	D6	Data D6 of external bus	CN17-15	SW2-1: ON, SW2-2: OFF
		GTIOC02_0B	Input capture/output compare/PWM output pin	CN24-28	
		SD0_IOVS	SD0 power selection		SW2-1: OFF, SW2-2: ON
AD10	P04_6/IRQ0/MTCLKD/MTIOC0D/GTIOC03_3B/CMTW1_TOC1/IIC_SDA0/ADTRG2#/MBX_HINT#/ENCIFOE03/DEE03/HDSL03_MISO2	**ENCIFOE03**	**ENCIF output enable**	**CN2-14**	
		GTIOC03_3B	**Input capture/output compare/PWM output pin**	**CN25-10**	
AD11	P02_5/D5/MTIOC3B/MTIOC8A/GTIOC02_0A/GTADSM06_0/CMTW0_TIC0/IIC_SCL0/SD0_PWEN/MCLK00/HDSL02_SMPL/POUTA	D5	Data D5 of external bus	CN17-13	SW2-1: ON, SW2-2: OFF
		GTIOC02_0A	Input capture/output compare/PWM output pin	CN24-27	
		SD0_PWEN	SD0 power enable		SW2-1: OFF, SW2-2: ON
AD12	VSS				
AD13	P01_6/MTIOC7B/MTIOC0A/GTIOC01_2A/GTIOC04_2A/XSPI1_IO2/TST_OUT03/HDSL01_MISO1	**XSPI1_IO2**	**IO2 of QSPI and SPI expansion connector**	**CN63-10**	**SW1-6: ON**
		GTIOC04_2A	Input capture/output compare/PWM output pin	CN25-19	SW1-6: OFF
AD14	P01_2/MTIOC6B/MTIOC8B/GTIOC01_0A/GTIOC04_0A/XSPI1_CS1#/DUEI02/HDSL01_LINK	**XSPI1_CS1#**	**CS1# of SPI expansion connector**	**CN63-4**	**SW1-6: ON**
		GTIOC01_0A	Input capture/output compare/PWM output pin	CN24-15	SW1-6: OFF

AD15	P00_1/IRQ0/D1/MTIOC3D/GTIOC00_0B/ETH3_RXER/USB_OVRCUR/TST_OUT00/HDSL00_SMPL	D1	Data D1 of external bus	CN17-3	SW1-5: OFF
		GTIOC00_0B	Input capture/output compare/PWM output pin	CN24-4	
		USB_OVRCUR	**OVRCUR input for USB host interface**		**SW1-5: ON**
AD16	USB_VUBUSIN	**USB_VUBUSIN**	**VBUSIN of USB function interface**	**CN79-1**	**SW7-7: OFF, SW7-8: ON**
AD17	USB_OTG_ID	**USB_OTG_ID**	**ID of USB_OTG**	**CN33-4**	
AD18	VSS				
AD19	PCIE_REFCLK_P1	**PCIE_REFCLK_P1**	**Reference clock of PCIe ch1**		
AD20	PCIE_REFCLK_N0	**PCIE_REFCLK_N0**	**Reference clock of PCIe ch0**		
AD21	VSS				
AD22	AVSS_ADC2				
AD23	AVSSIO_ADC2				
AD24	AVSSIO_ADC1				
AD25	AVSSIO_ADC1				
AD26	AN102	**AN102**	Input to A/D converter (AN102)	CN42-6	SW18-5: ON, SW18-6: OFF
			Input to A/D converter (AN102) of Grove2	**CN48-2**	**SW18-5: OFF, SW18-6: ON**
AD27	AN101	**AN101**	Input to A/D converter (AN101)	CN42-4	SW18-3: ON, SW18-4: OFF
			Input to A/D converter (AN101) of Grove2	**CN48-1**	**SW18-3: OFF, SW18-4: ON**

Table 5-25 List of RZ/T2H Pin Function Selections (25)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
AE1	P09_0/IIC_SDA2/MCLK12/SI11#/HDSL07_SMPL	**P09_0**	**GPIO for use with PMOD2**	**CN49-9**	
		MCLK12	**Clock of DSMIF**	**CN21-13**	
AE2	P09_2/MCLK20/TST_OUT12/HDSL07_SEL1	**MCLK20**	**Clock of DSMIF**	**CN21-27**	
AE3	P08_5/IRQ8/RSTOUT#/GTETRGSA/IIC_SCL1/SD1_PWEN/MCLK02/HDSL06_MISO2	P08_5	Control of user LED3		SW2-3: OFF
		SD1_PWEN	**SD1 power enable**		**SW2-3: ON**
AE4	P08_4/TDO/HDSL06_SEL2	**TDO**	**TDO of debugging interface**	**CN60-6, CN61-6**	
AE5	P06_0/XSPI0_IO2/TST_OUT08/HDSL04_MISO2	**XSPI0_IO2**	**Data IO2 of XSPI0**		
AE6	P06_2/IRQ8/IIC_SCL0/XSPI0_IO4/DUEI09/HDSL05_LINK	**XSPI0_IO4**	**Data IO4 of XSPI0**		
AE7	P05_7/XSPI0_IO1/DUEI08/HDSL04_SEL2	**XSPI0_IO1**	**Data IO1 of XSPI0**		
AE8	P07_3/POE11#/IIC_SCL1/XSPI0_INT0#/MCLK01/ENCIFDO04/ENCIFDO12/TXDE04/TXDE08/HDSL05_MISO2	**MCLK01**	**Clock of DSMIF**	**CN21-5**	
AE9	P02_7/D7/MTIOC4A/MTIC5U/GTIOC02_1A/GTADSM07_0/CMTW0_TIC1/MCLK01/HDSL02_SEL1/POUTZ	**D7**	**Data D7 of external bus**	**CN17-17**	
		GTIOC02_1A	**Input capture/output compare/PWM output pin**	**CN24-29**	
AE10	P03_0/D8/MTIOC4C/MTIC5V/GTIOC02_1B/GTADSM07_1/CMTW0_TOC1/MDAT01/HDSL02_MISO1	**D8**	**Data D8 of external bus**	**CN17-19**	
		GTIOC02_1B	**Input capture/output compare/PWM output pin**	**CN24-30**	
AE11	P04_0/MTIOC6D/GTIOC03_0B/CMTW0_TOC0/TST_OUT04/HDSL03_CLK1	**P04_0**	**IRQOUT# of external bus**	**CN13-37**	
		GTIOC03_0B	**Input capture/output compare/PWM output pin**	**CN25-4**	
AE12	P02_4/IRQ11/POE0#/IIC_SDA0/MDAT20/USB_EXICEN/MBX_HINT#/HDSL02_LINK	**MBX_HINT#**	**HINT# of SHOSTIF**	**CN64-13**	
AE13	P01_5/MTIOC7C/MTIC5W/GTIOC01_1B/GTIOC04_1B/XSPI1_IO1/DUEI03/HDSL01_SEL1	**XSPI1_IO1**	**IO1 of QSPI and SPI expansion connector**	**CN63-11**	**SW1-6: ON**
		GTIOC04_1B	Input capture/output compare/PWM output pin	CN25-18	SW1-6: OFF
AE14	P00_7/IRQ5/MTCLKB/MTIOC1B/GTIOC00_3B/IIC_SDA0/USB_EXICEN/ENCIFOE00/ENCIFOE04/DEE00/DEE04/HDSL00_SEL2	**IRQ5**	**INT for use with PMOD1**	**CN50-7**	
		GTIOC00_3B	**Input capture/output compare/PWM output pin**	**CN24-10**	
		ENCIFOE04	**ENCIF output enable**	**CN2-23**	

AE15	P00_0/SEI/D0/MTIOC3B/GTIOC00_0A/ETH3_TXER/USB_VBUSEN/DUEI00/HDSL00_LINK	D0	Data D0 of external bus	CN17-1	SW1-5: OFF
		GTIOC00_0A	Input capture/output compare/PWM output pin	CN24-3	
		USB_VBUSEN	**VBUS control for USB host interface**		**SW1-5: ON, SW7-9: OFF, SW7-10: ON**
AE16	VSS				
AE17	VSS				
AE18	VSS				
AE19	VSS				
AE20	VSS				
AE21	VSS				
AE22	VSS				
AE23	VSS				
AE24	VSS				
AE25	AVSSIO_ADC2				
AE26	AN202	**AN202**	**Input to A/D converter (AN202)**	**CN43-5**	
AE27	AN201	**AN201**	**Input to A/D converter (AN201)**	**CN43-3**	

Table 5-26 List of RZ/T2H Pin Function Selections (26)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
AF1	P09_3/MDAT20/SI12#/HDSL07_MISO1	**MDAT20**	**Data of DSMIF**	**CN21-28**	
AF2	P08_7/IRQ0/A0/GTIOC08_3B/IIC_SCL2/IIC_SCL1/MDAT11/TST_OUT11/HDSL07_LINK	**P08_7**	**RESET for use with PMOD2**	**CN49-8**	
		IRQ0	**Interrupt of user SW11**		
		MDAT11	**Data of DSMIF**	**CN21-16**	
AF3	TRST#	**TRSTN**	**TRST of debugging interface**		
AF4	P07_1/IRQ14/POE8#/IIC_SCL0/XSPI0_RSTO0#/MCLK00/ENCIFCK04/ENCIFCK12/SCKE04/SCKE08/HDSL05_CLK2	**MCLK00**	**Clock of DSMIF**	**CN21-7**	
AF5	P05_5/XSPI0_DS/TST_OUT07/HDSL04_MOSI1	**XSPI0_DS**	**DS of XSPI0**		
AF6	VSS				
AF7	P06_7/IRQ12/POE4#/GTETRGD/GMAC1_MDC/IIC_SCL2/HDSL05_MISO1	**P06_7**	**Control of user LED2**		
AF8	P07_0/IRQ13/GMAC1_MDIO/IIC_SDA2/XSPI0_RESET1#/HDSL05_MOSI1	**XSPI0_RESET1#**	**RESET1# of XSPI0**		
AF9	P04_5/SEI/MTCLKC/MTIOC0C/GTIOC03_3A/CMTW1_TIC1/IIC_SCL0/ADTRG1#/ENCIFCK03/SCKE03/HDSL03_SEL2	**GTIOC03_3A**	**Input capture/output compare/PWM output pin**	**CN25-9**	
		ENCIFCK03	**Clock of ENCIF**	**CN2-12**	
AF10	VSS				
AF11	P04_1/MTIOC7A/GTIOC03_1A/CMTW0_TIC1/SI04#/HDSL03_SEL1	**P04_1**	**RST for use with mikroBUS™**	**CN53-2**	
		GTIOC03_1A	**Input capture/output compare/PWM output pin**	**CN25-5**	
AF12	P02_3/IRQ10/MTIOC6C/MTIOC1B/GTIOC01_4B/ETH3_COL/IIC_SCL0/IIC_SCL2/XSPI1_IO7/MDAT22/USB_OVRCUR/ENCIFDI01/RXDE01/HDSL01_MOSI2	GTIOC01_4B	Input capture/output compare/PWM output pin	CN24-24	SW1-6: OFF
		XSPI1_IO7	**IO7 of SPI expansion connector**	**CN63-5**	**SW1-6: ON**
AF13	P01_0/IRQ6/MTIOC3A/MTIOC1A/GTIOC00_4A/GTIOC00_2B/IIC_SCL1/XSPI1_CKP/ENCIFDO00/ENCIFDO04/TXDE00/TXDE04/HDSL00_MISO2	GTIOC00_4A	Input capture/output compare/PWM output pin	CN24-11	SW1-6: OFF
		ENCIFDO04	Data output from ENCIF	CN2-25	
		XSPI1_CKP	**CKP of QSPI and SPI expansion connector**	**CN63-3**	**SW1-6: ON**
AF14	VSS				
AF15	P00_4/IRQ3/D4/MTIOC4B/GTIOC00_2A/ADTRG2#/TST_OUT01/HDSL00_MISO1	**D4**	**Data D4 of external bus**	**CN17-9**	
		GTIOC00_2A	**Input capture/output compare/PWM output pin**	**CN24-7**	
AF16	VSS				
AF17	USB_QDP	**USB_QDP**	**Input/output of USB DP**		
AF18	VSS				

AF19	PCIE_RXDN_L1	**PCIE_RXDN_L1**	Receive data of PCIe ch1 (x1)	CN8-A17	SW15-2: ON
			Receive data of PCIe ch1 (x4)	**CN32-A22**	**SW15-2: OFF**
AF20	PCIE_RXDN_L0	**PCIE_RXDN_L0**	**Receive data of PCIe ch0 (x4)**	**CN32-A17**	
AF21	VSS				
AF22	PCIE_TXDN_L1	**PCIE_TXDN_L1**	Transmit data of PCIe ch1 (x1)	CN8-B15	SW15-2: ON
			Transmit data of PCIe ch1 (x4)	**CN32-B20**	**SW15-2: OFF**
AF23	PCIE_TXDN_L0	**PCIE_TXDN_L0**	**Transmit data of PCIe ch0 (x4)**	**CN32-B15**	
AF24	VSS				
AF25	AVDDREF_ADC2				
AF26	AN204	**AN204**	**Input to A/D converter (AN204)**	**CN43-9**	
AF27	AN200	**AN200**	**Input to A/D converter (AN200)**	**CN43-1**	

Table 5-27 List of RZ/T2H Pin Function Selections (27)

Pin No.	Pin Name	Pin Function	Description	Connector	Remarks
AG1	VSS				
AG2	P09_1/MDAT12/DUEI12/HDSL07_CLK1	**P09_1**	**GPIO for use with PMOD2**	**CN49-10**	
		MDAT12	**Data of DSMIF**	**CN21-14**	
AG3	P08_1/TMS/DUEI10/HDSL06_MISO1	**TMS**	**TMS of debugging interface**	**CN60-2, CN61-2**	
AG4	P05_3/IRQ5/XSPI0_CS0#/SI06#/HDSL04_SEL1	**XSPI0_CS0#**	**CS# of OctaFlash**		
AG5	P07_2/IRQ15/POE10#/IIC_SDA0/XSPI0_RSTO1#/MDAT00/ENCIFOE04/ENCIFOE12/DEE04/DEE08/HDSL05_SEL2	**MDAT00**	**Data of DSMIF**	**CN21-8**	
AG6	P07_5/IIC_SCL2/XSPI0_ECS0#/MCLK02/ENCIFCK05/SCKE05/HDSL06_LINK	MCLK02	Clock of DSMIF	CN21-3	SW5-5: ON, SW5-6: OFF
		XSPI0_ECS0#	**ECS# of OctaFlash**		**SW5-5: OFF, SW5-6: ON**
AG7	P05_4/IRQ6/IIC_SDA2/XSPI0_CS1#/DUEI07/HDSL04_MISO1	**XSPI0_CS1#**	**CS# to HyperRAM**		
AG8	P06_6/MDD/XSPI0_RESET0#	**MDD**	**MDD setting**		
		XSPI0_RESET0#	**RESET# to OctaFlash**		
AG9	P03_6/MTIOC3C/MTIOC1A/GTIOC02_4B/IIC_SDA2/ENCIFDI02/RXDE02/HDSL03_LINK	**GTIOC02_4B**	**Input capture/output compare/PWM output pin**	**CN24-36**	
		ENCIFDI02	**Data input to ENCIF**	**CN2-17**	
AG10	P04_3/MTIOC7B/GTIOC03_2A/CMTW1_TIC0/TST_OUT05/HDSL03_MOSI1	**P04_3**	**RESET for use with PMOD1**	**CN50-8**	
		GTIOC03_2A	**Input capture/output compare/PWM output pin**	**CN25-7**	
AG11	P04_4/MTIOC7D/GTIOC03_2B/CMTW1_TOC0/ADTRG0#/SI05#/HDSL03_CLK2	**P04_4**	**GPIO for use with PMOD1**	**CN50-9**	
		GTIOC03_2B	**Input capture/output compare/PWM output pin**	**CN25-8**	
AG12	P01_1/MTIOC3C/MTIOC8A/GTIOC00_4B/XSPI1_CS0#/MCLK20/ENCIFDI00/ENCIFDI04/RXDE00/RXDE04/HDSL00_MOSI2	GTIOC00_4B	Input capture/output compare/PWM output pin	CN24-12	SW1-6: OFF
		ENCIFDI04	Data input to ENCIF	CN2-27	
		XSPI1_CS0#	**CS# of QSPI**		**SW1-6: ON**
AG13	P01_4/MTIOC7A/MTIC5V/GTIOC01_1A/GTIOC04_1A/XSPI1_IO0/SI02#/HDSL01_CLK1	GTIOC04_1AB	Input capture/output compare/PWM output pin	CN25-17	SW1-6: OFF
		XSPI1_IO0	**IO0 of QSPI and SPI expansion connector**	**CN63-12**	**SW1-6: ON**
AG14	P00_6/IRQ4/MTCLKA/MTIOC8D/GTIOC00_3A/IIC_SCL0/USB_OVRCUR/ENCIFCK00/ENCIFCK04/SCKE00/SCKE04/HDSL00_CLK2	**GTIOC00_3A**	**Input capture/output compare/PWM output pin**	**CN24-9**	
		ENCIFCK04	**Clock of ENCIF**	**CN2-21**	

AG15	P00_3/IRQ2/D3/MTIOC4C/GTIOC00_1B/ETH3_COL/ADTRG1#/DUEI01/HDSL00_SEL1	**IRQ2/ADTRG1#**	**User switch SW10/ ADTRG switch**		
		D3	**Data D3 of external bus**	**CN17-7**	
		GTIOC00_1B	**Input capture/output compare/PWM output pin**	**CN24-6**	
AG16	VSS				
AG17	USB_QDM	**USB_QDM**	**Input/output of USB DM**		
AG18	VSS				
AG19	PCIE_RXDP_L1	**PCIE_RXDP_L1**	Receive data of PCIe ch1 (x1)	CN8-A16	SW15-2: ON
			Receive data of PCIe ch1 (x4)	**CN32-A21**	**SW15-2: OFF**
AG20	PCIE_RXDP_L0	**PCIE_RXDP_L0**	**Receive data of PCIe ch0 (x4)**	**CN32-A16**	
AG21	VSS				
AG22	PCIE_TXDP_L1	**PCIE_TXDP_L1**	Transmit data of PCIe ch1 (x1)	CN8-B14	SW15-2: ON
			Transmit data of PCIe ch1 (x4)	**CN32-B19**	**SW15-2: OFF**
AG23	PCIE_TXDP_L0	**PCIE_TXDP_L0**	**Transmit data of PCIe ch0 (x4)**	**CN32-B14**	
AG24	VSS				
AG25	AN205	**AN205**	**Input to A/D converter (AN205)**	**CN43-11**	
AG26	AN203	**AN203**	**Input to A/D converter (AN203)**	**CN43-7**	
AG27	VSS				

6. Circuitry for Configuration

6.1 Types of Configuration Circuits

Since multiple functions are assigned to single pins and each function has to be selected for use in the RZ/T2H, the functions to be used should be selected through the following methods on this board.

(1) Switches

DIP switches SW1, SW2, SW4 to SW8, SW14, SW15, SW17, and SW18 are mounted for selecting functions.

(2) Jumper blocks

CN9, CN29, CN30, CN35 to CN40, CN56, CN57, CN62, CN73, CN77, CN78, and CN81 to CN87 are mounted for selecting functions.

(3) Option links

The option links are as follows:

— Solder bridges and trace cuts

A solder bridge consists of two pads, which are insulated from each other at the time of shipment. Conduction can be set up for such pads by connecting them with solder or the like. A trace cut is a thin copper trace that connects two pads and sets up conduction between them. Such pads can be insulated from each other by cutting the trace between the pads.

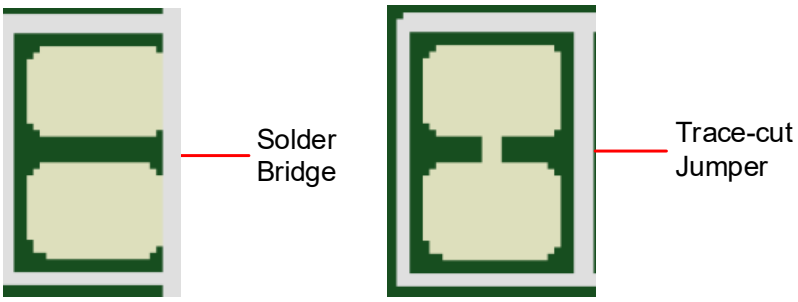


Figure 6-1 Solder Bridge and Trace Cut

— 0-Ω and other resistors

A different function can be selected by switching the factory state of a 0-Ω resistor or other resistor between mounted and not mounted.

The subsequent sections describe which peripheral functions of the multi-functional RZ/T2H signals are enabled or disabled through the settings of switches, jumper blocks, and option links. The connection information for ICs and headers other than the RZ/T2H will also be shown. **Text in bold blue type** in the tables indicates the initial state of the configuration on the board as shipped. For the positions of switches, jumper blocks, and option links, refer to "3.3 Arrangement of Components".

The settings of switches or jumper blocks should be changed only when the power is turned off.

When removing soldered components, do not apply a soldering iron to the board for more than 5 seconds. This time restriction is to avoid any damage to components mounted nearby on the board.

When modifying an option link, always check the related option links to ensure that no signal contention or short circuit has occurred. Most of the RZ/T2H pins have multiplexed functions and some of the peripheral functions must be used exclusively of each other. Refer to the RZ/T2H and RZ/N2H Groups User's Manual: Hardware and this board's schematics for further information.

6.2 Configuration at Shipment

Figure 6-2 shows the state of switch settings and jumper block settings for the configuration at the time of shipment.

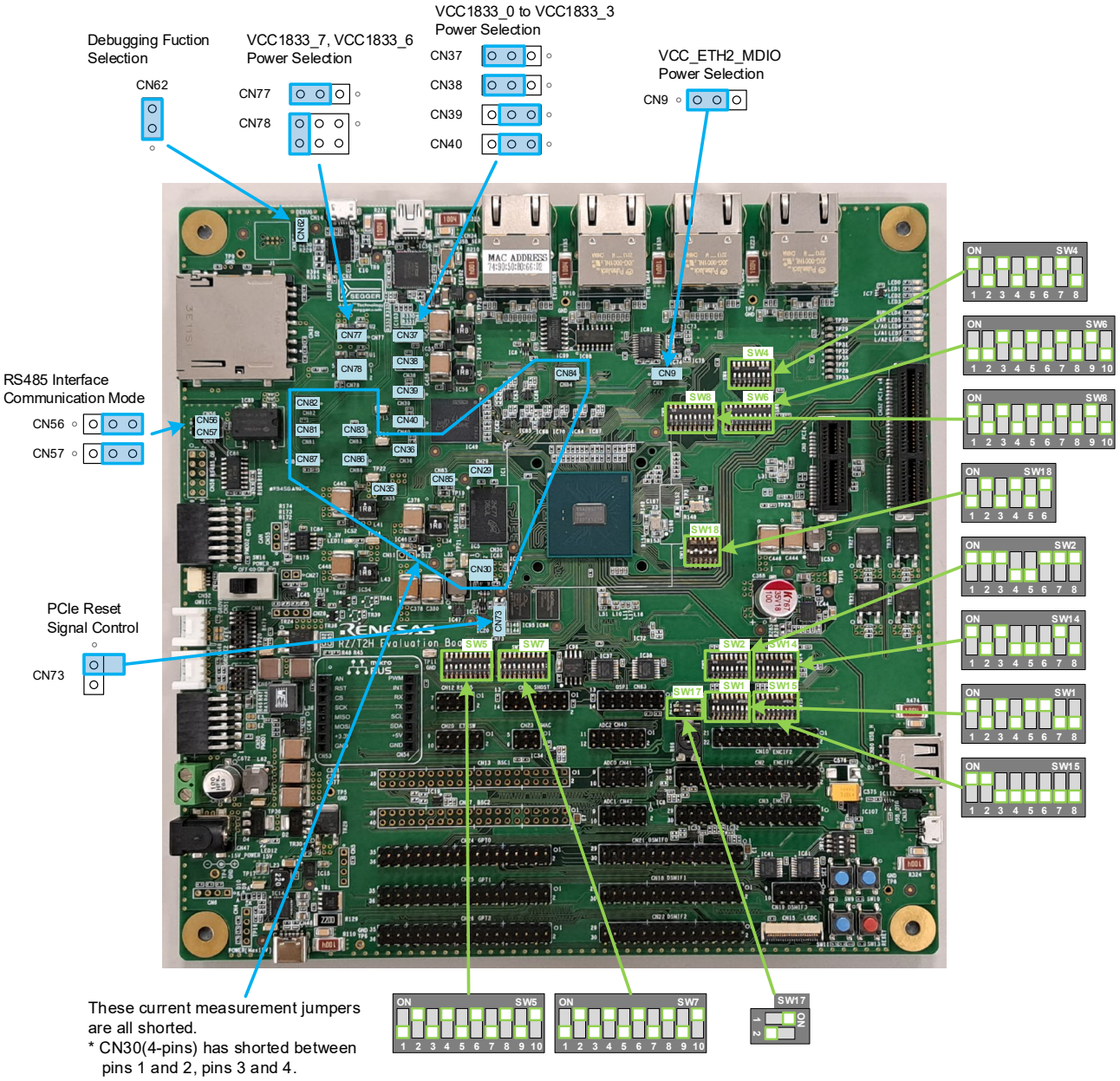


Figure 6-2 Switch Settings and Jumper Block Settings at Shipment

6.3 Configuration by Switches

This board is equipped with DIP switches SW1, SW2, SW4 to SW8, SW14, SW15, SW17, and SW18 for selecting functions. The functions set by individual switches are explained below.

6.3.1 Mode Setting Switch SW14

SW14 is used to set the mode pins of the RZ/T2H. Table 6-1 lists the settings of SW14.

Table 6-1 Functions of Mode Setting Switch SW14

No.	Setting		Function
SW14-1 MD0	OFF	MD0 = H	The operating mode of the RZ/T2H is selected with the combination of SW14-1, SW14-2, and SW14-3 (MD0, MD1, and MD2). SW14-6 (MDV) should be selected according to these settings. For details, see Table 6-2.
	ON	**MD0 = L**	
SW14-2 MD1	**OFF**	**MD1 = H**	
	ON	MD1 = L	
SW14-3 MD2	OFF	MD2 = H	
	ON	**MD2 = L**	
SW14-4 MDW0	**OFF**	**MDW0 = H**	**The number of ATCM wait cycles of CPU0 in the Cortex-R52 is 1 wait cycle.**
	ON	MDW0 = L	The number of ATCM wait cycles of CPU0 in the Cortex-R52 is 0 wait cycles.
SW14-5 MDW1	**OFF**	**MDW1 = H**	**The number of ATCM wait cycles of CPU1 in the Cortex-R52 is 1 wait cycle.**
	ON	MDW1 = L	The number of ATCM wait cycles of CPU1 in the Cortex-R52 is 0 wait cycles.
SW14-6 MDV*	**OFF**	**MDV = H**	**The power-supply voltage of the boot peripheral is 3.3 V.**
	ON	MDV = L	The power-supply voltage of the boot peripheral is 1.8 V.
SW14-7 MDD	OFF	MDD = H	JTAG mode = JTAG authentication in hash mode
	ON	**MDD = L**	**JTAG mode = Normal mode**
SW14-8	Unused		**— (At the time of shipment = OFF)**

Note: This setting may have to be changed to suit the operating mode. It is “Don’t care” in SCI (UART) boot mode and USB boot mode.

Table 6-2 SW14-1, SW14-2, SW14-3, and SW14-6 (MD0, MD1, MD2, and MDV) and RZ/T2H Operating Mode

SW14-3 (MD2)	SW14-2 (MD1)	SW14-1 (MD0)	SW14-6 (MDV)	Operating Mode
ON	ON	ON	OFF (3.3 V)	xSPI0 boot mode (x1 boot serial flash)
ON	ON	OFF	OFF (3.3 V)	xSPI0 boot mode (x8 boot serial flash)*
ON	**OFF**	**ON**	**OFF (3.3 V)**	**xSPI1 boot mode (x1 boot serial flash)**
ON	OFF	OFF	OFF (3.3 V)	eSD boot mode
OFF	ON	ON	ON (1.8 V)	eMMC boot mode
OFF	ON	OFF	—	SCI (UART) boot mode
OFF	OFF	ON	—	USB boot mode
OFF	OFF	OFF	—	Reserved (setting prohibited)

Note: This setting is prohibited because OctaFlash is mounted.

6.3.2 Signal Function Selection Switches SW1, SW2, SW4 to SW8, SW15, SW17, and SW18

SW1, SW2, SW4 to SW8, SW15, SW17, and SW18 are used to select the functions of the signal lines. Table 6-3 to Table 6-12 list the settings of SW1, SW2, SW4 to SW8, SW15, SW17, and SW18.

Table 6-3 Signal Function Selection Switch SW1

No.	Setting	Function
SW1-1	OFF	XTALSEL = H The resonator is selected as the clock input to the RZ/T2H.
	ON	**XTALSEL = L** **The oscillator is selected as the clock input to the RZ/T2H.**
SW1-2	Unused	**— (At the time of shipment = OFF)**
SW1-3	OFF	P35_3 to P35_6 are connected to DSMIF3 (CN19).
	ON	**P35_3 to P35_6 are used as inputs to user DIP switches.**
SW1-4	**OFF**	**P13_4, P13_5, and P14_0 are used as RXD3, TXD3, and DE3 of the RS485.**
	ON	P13_4, P13_5, and P14_0 are connected to ENCIF2 (CN10), GPT2 (CN26), BSC1 (CN13), BSC2 (CN17), and ETHSW (CN20).
SW1-5	OFF	P00_0 to P00_2 are connected to GPT0 (CN24) and BSC2 (CN17).
	ON	**P00_0 to P00_2 are used as control signals for the USB power-supply IC.**
SW1-6	OFF	P01_0 to P01_2, P01_4 to P01_7, and P02_0 to P02_3 are connected to ENCIF0 (CN2), GPT0 (CN24), GPT1 (CN25), and DSMIF0 (CN21).
	ON	**P01_0 to P01_2, P01_4 to P01_7, and P02_0 to P02_3 are used as XSPI1 signals.**
SW1-7	Unused	**— (At the time of shipment = OFF)**
SW1-8	Unused	**— (At the time of shipment = OFF)**

Table 6-4 Signal Function Selection Switch SW2

No.	Setting		Function
SW2-1, SW2-2	-1	-2	
	OFF	OFF	Setting prohibited
	OFF	ON	P12_0 to P12_5, P22_5, and P22_6 are connected to the SD card slot (CN31). P02_5 and P02_6 are used for controlling the power supply of the SD card.
	ON	OFF	P12_0 to P12_7, P13_0 to P13_2, P22_5, P22_6, P02_5, and P02_6 are connected to BSC2 (CN17), ENCIF0 (CN2), GPT1 (CN25), and the pin header (CN12) of the off-board RS485.
	ON	**ON**	**P12_0 to P12_7 and P13_0 to P13_2 are connected to eMMC.**
SW2-3	OFF		P17_4, P08_5, and P08_6 are connected to BSC1 (CN13), BSC2 (CN17), DSMIF0 (CN21), SEI (SW9), and LED3.
	ON		**P17_4, P08_5, and P08_6 are used as SD1 control signals.**
SW2-4	Unused		**— (At the time of shipment = OFF)**
SW2-5	Unused		**— (At the time of shipment = OFF)**
SW2-6	OFF		MDC and MDIO of Ethernet port 2 are connected to GMAC2 (P30_5 and P30_6).
	ON		**MDC and MDIO of Ethernet port 2 are connected to GMAC0 (P21_4 and P21_5).**
SW2-7	OFF		P29_1 to P29_7, P30_0 to P30_4, and P31_2 to P31_5 are connected to INCIF1 (CN3), SHOST (CN64), DSMIF2 (CN22), and PMOD1 (CN50).
	ON		**P29_1 to P29_7, P30_0 to P30_4, and P31_2 to P31_5 are used as control signals for Ethernet port 2.**
SW2-8	OFF		P27_2, P33_2 to P33_7, P34_0 to P34_5, P34_7, and P35_0 to P35_2 are used as GMAC (CN23), Serial Host Interface (CN64), ENCIF0 (CN2), BSC1 (CN13), DSMIF3 (CN19) and PCIE_RSTOUT.
	ON		**P27_2, P33_2 to P33_7, P34_0 to P34_5, P34_7, and P35_0 to P35_2 are used as control signals for Ethernet port 3.**

Table 6-5 Signal Function Selection Switch SW4

No.	Setting		Function
SW4-1, SW4-2	-1	-2	
	ON	**OFF**	**P27_0 is used as ETH1_CRS.**
	OFF	ON	P27_0 is used as HSPI_INT# of SHOST (CN64) or CS5# of CN13.
SW4-3, SW4-4	-3	-4	
	ON	**OFF**	**P27_1 is used as ETH1_COL.**
	OFF	ON	P27_1 is used as HSPI_CS# of SHOST (CN64).
SW4-5, SW4-6	-5	-6	
	ON	**OFF**	**P27_4 is used as RXD0 of the USB-to-serial conversion.**
	OFF	ON	P27_4 is used as HSPI_IO2 of SHOST (CN64) or GTIOC08_3B of GPT2 (CN26).
SW4-7, SW4-8	-7	-8	
	ON	**OFF**	**P27_5 is used as TXD0 of the USB-to-serial conversion.**
	OFF	ON	P27_5 is used as HSPI_IO3 of SHOST (CN64) or GTIOC08_4A of GPT2 (CN26).

Table 6-6 Signal Function Selection Switch SW5

No.	Setting		Function
SW5-1, SW5-2	-1	-2	
	ON	OFF	P32_2 is used as SD1_IOVS (SW5-3 needs to be set to ON).
	OFF	**ON**	**P32_2 is used as USER_LED1.**
SW5-3, SW5-4	-3	-4	
	ON	OFF	P32_2 is used as SD1_IOVS (SW5-1 needs to be set to ON).
	OFF	**ON**	**When SW2-3=ON, P08_6 is used as SD1_IOVS.**
SW5-5, SW5-6	-5	-6	
	ON	OFF	P07_5 is used as MCLK02 of DSMIF0 (CN21).
	OFF	**ON**	**P07_5 is used as XSPI0_ECS# of OctaFlash.**
SW5-7, SW5-8	-7	-8	
	ON	OFF	P23_0 is used as GTIOC06_0B of GPT2 (CN26).
	OFF	**ON**	**P23_0 is used as ESC_LINKACT1.**
SW5-9, SW5-10	-9	-10	
	ON	OFF	P22_7 is used as GTIOC06_0A of GPT2 (CN26).
	OFF	**ON**	**P22_7 is used as ESC_LINKACT0.**

Table 6-7 Signal Function Selection Switch SW6

No.	Setting			Function
SW6-1 to SW6-3	-1	-2	-3	
	ON	OFF	OFF	P17_5 is used as BSC_A7.
	OFF	ON	OFF	P17_5 is used as GMAC_RESETOUT2#.
	OFF	**OFF**	**ON**	**P11_0 is used as ESC_RESETOUT2#.**
SW6-4, SW6-5	-4	-5		
	ON	OFF		P11_0 is used as BSC_A5/LCDC_DATG0/PMOD2_RXD1.
	OFF	**ON**		**P11_0 is used as ESC_RESETOUT01#.**
SW6-6	Unused			**— (At the time of shipment = OFF)**
SW6-7, SW6-8	-7	-8		
	ON	**OFF**		**P23_3 is used as ESC_I2CCLK.**
	OFF	ON		P23_3 is used as GTIOC06_2A of GPT2 (CN26).
SW6-9, SW6-10	-9	-10		
	ON	**OFF**		**P23_4 is used as ESC_I2CDATA.**
	OFF	ON		P23_4 is used as GTIOC06_2B of GPT2 (CN26).

Table 6-8 Signal Function Selection Switch SW7

No.	Setting		Function
SW7-1, SW7-2	-1	-2	
	ON	OFF	P24_4 is used as MDAT70 of DSMIF2 (CN22).
	OFF	**ON**	**P24_4 is used as CAN_TX.**
SW7-3, SW7-4	-3	-4	
	ON	OFF	P24_3 is used as MCLK70 of DSMIF2 (CN22).
	OFF	**ON**	**P24_3 is used as CAN_RX.**
SW7-5, SW7-6	-5	-6	
	ON	OFF	P23_5 is used as MCLK60 of DSMIF2 (CN22).
	OFF	**ON**	**P23_5 is used as ESC_LINKACT2.**
SW7-7, SW7-8	-7	-8	
	ON	OFF	Setting prohibited
	OFF	**ON**	**VUBUSIN is used as USB_Function.**
SW7-9, SW7-10	-9	-10	
	ON	OFF	Setting prohibited
	OFF	**ON**	**P00_0 is used as USB_HF_VBUSEN.**

Table 6-9 Signal Function Selection Switch SW8

No.	Setting		Function
SW8-1, SW8-2	-1	-2	
	ON	**OFF**	**P18_1 is used as ESC_LED_ERR.**
	OFF	ON	P18_1 is used as BSC_A9/LCDC_DATB2.
SW8-3, SW8-4	-3	-4	
	ON	**OFF**	**P18_0 is used as ESC_LED_RUN.**
	OFF	ON	P18_0 is used as BSC_A8/LCDC_DATB1.
SW8-5, SW8-6	-5	-6	
	ON	**OFF**	**P16_3 is used as RXD5 of the USB-to-serial conversion.**
	OFF	ON	P16_3 is used as MikroBUS_RXD5/IRQ10_D(PMOD)/PCIex1_WAKE_GPIO.
SW8-7, SW8-8	-7	-8	
	ON	**OFF**	**P16_4 is used as TXD5 of the USB-to-serial conversion.**
	OFF	ON	P16_4 is used as MikroBUS_TXD5.
SW8-9, SW8-10	-9	-10	
	ON	**OFF**	**P23_1 is used as USER_LED0.**
	OFF	ON	P23_1 is used as GTIOC06_1A of GPT2 (CN26).

Table 6-10 Signal Function Selection Switch SW15

No.	Setting	Function
SW15-1	OFF	PCIe L0 is used as an endpoint.
	ON	**PCIe L0 is used as a root complex.**
SW15-2	OFF	PCIe L1 is used as an endpoint.
	ON	**PCIe L1 is used as a root complex.**
SW15-3	**OFF**	**The PCIe function is used in a configuration of 2 lanes × 1 port.**
	ON	The PCIe function is used in a configuration of 1 lane × 2 ports.
SW15-4	Unused	**— (At the time of shipment = OFF)**
SW15-5	**OFF**	**The 12-V power supply of the PCIe x4 connector CN32 is OFF.**
	ON	The 12-V power supply of the PCIe x4 connector CN32 is ON (when the x4 connector CN32 is used for the root complex).
SW15-6	**OFF**	**The 3.3-V power supply of the PCIe x4 connector CN32 is OFF.**
	ON	The 3.3-V power supply of the PCIe x4 connector CN32 is ON (when the x4 connector CN32 is used for the root complex).
SW15-7	**OFF**	**The 3.3-V power supply of the PCIe x1 connector CN8 is OFF.**
	ON	The 3.3-V power supply of the PCIe x1 connector CN8 is ON (when the x1 connector CN8 is used for the root complex).
SW15-8	**OFF**	**The 12-V power supply of the PCIe x1 connector CN8 is OFF.**
	ON	The 12-V power supply of the PCIe x1 connector CN8 is ON (when the x1 connector CN8 is used for the root complex).

Table 6-11 Signal Function Selection Switch SW17

No.	Setting		Function
SW17-1, SW17-2	-1	-2	
	ON	**OFF**	**AN000 is connected to the potentiometer.**
	OFF	ON	AN000 is connected to CN41.

Table 6-12 Signal Function Selection Switch SW18

No.	Setting		Function
SW18-1, SW18-2	-1	-2	
	ON	OFF	AN100 is connected to CN42.
	OFF	**ON**	**AN100 is connected to mikroBUS™.**
SW18-3, SW18-4	-3	-4	
	ON	OFF	AN101 is connected to CN42.
	OFF	**ON**	**AN101 is connected to Grove2.**
SW18-5, SW18-6	-5	-6	
	ON	OFF	AN102 is connected to CN42.
	OFF	**ON**	**AN102 is connected to Grove2.**

6.4 Configuration by Jumper Blocks

This board is equipped with jumper blocks CN9, CN29, CN30, CN35 to CN40, CN56, CN57, CN62, CN73, CN77, CN78, and CN81 to CN87 for selecting functions. The functions set by individual jumper blocks are explained below.

6.4.1 I/O Power Selection Jumper Blocks CN9, CN37 to CN40, CN77, and CN78

CN9, CN37 to CN40, CN77, and CN78 are used to select the power supply to the I/O power domain of the RZ/T2H and Ethernet PHY. The supply of voltage to each power supply selected by CN9, CN37 to CN40, CN77, or CN78 must comply with the standards or usage methods of the I/O devices connected to that power domain. Otherwise, malfunctions of the device may occur or permanent damages may be caused.

Table 6-13 I/O Power Selection Jumper Blocks CN9, CN37 to CN40, CN77, and CN78

No.	Setting	Function
CN9	**1-2 are short-circuit**	**VCC1833_0 is supplied to VCC_ETH2_MDIO (SW2-6 is ON: When P21_4 and P21_5 are selected for MDIO).**
	2-3 are short-circuit	VCC1833_2 is supplied to VCC_ETH2_MDIO (SW2-6 is OFF: When P30_5 and P30_6 are selected for MDIO).
CN37	1-2 are short-circuit	1.8-V power is supplied to VCC1833_0 (for Ethernet port 0).
	2-3 are short-circuit	**3.3-V power is supplied to VCC1833_0 (for Ethernet port 0).**
CN38	1-2 are short-circuit	1.8-V power is supplied to VCC1833_1 (for Ethernet port 1).
	2-3 are short-circuit	**3.3-V power is supplied to VCC1833_1 (for Ethernet port 1).**
CN39	**1-2 are short-circuit**	**1.8-V power is supplied to VCC1833_2 (for Ethernet port 2).**
	2-3 are short-circuit	3.3-V power is supplied to VCC1833_2 (for Ethernet port 2).
CN40	**1-2 are short-circuit**	**1.8-V power is supplied to VCC1833_3 (for Ethernet port 3).**
	2-3 are short-circuit	3.3-V power is supplied to VCC1833_3 (for Ethernet port 3).
CN77	1-2 are short-circuit	3.3-V power is supplied to VCC1833_7 (for SD1).
	2-3 are short-circuit	**The output from the power-supply control IC for SD1 is supplied to VCC1833_7 (for SD1).**
CN78	1-2 are short-circuit	3.3-V power is supplied to VCC1833_6 (for SD0).
	3-4 are short-circuit	The output from the power-supply control IC for SD0 is supplied to VCC1833_6 (for SD0).
	5-6 are short-circuit	**1.8-V power is supplied to VCC1833_6 (for SD0).**

6.4.2 Debugging Function Selection Jumper Block CN62

CN62 is used to enable or disable the on-board debugging function J-Link™ OB.

Table 6-14 Debugging Function Selection Jumper Block CN62

No.	Setting	Function
CN62	Open-circuit	The on-board debugging function J-Link™ OB is enabled.
	Short-circuit	**The on-board debugging function J-Link™ OB is disabled.** **Connect an external emulator to either CN60 or CN61 at debugging.**

6.4.3 RS485 Interface Communication Mode Selection Jumper Blocks CN56 and CN57

CN56 and CN57 are used to select the communication mode of the RS485 interface.

Table 6-15 RS485 Interface Communication Mode Selection Jumper Blocks CN56 and CN57

No.	Setting	Function
CN56, CN57	1-2 are short-circuit	Full-duplex communication
	2-3 are short-circuit	**Half-duplex communication**

6.4.4 PCIe Reset Signal Control Jumper Block CN73

CN73 is used to select whether the reset signal of the PCIe is included in the system reset factors.

Table 6-16 PCIe Reset Signal Control Jumper Block CN73

No.	Setting	Function
CN73	Open-circuit	**A PCIe reset is not included in the system reset factors.**
	Short-circuit	A PCIe reset is included in the system reset factors.

6.4.5 Current Measurement Jumper Blocks CN29, CN30, CN35, CN36, and CN81 to CN87

CN29, CN30, CN35, CN36, and CN81 to CN87 are jumper blocks for measuring the current drawn by the target device (RZ/T2H). When measuring the current, insert an ammeter between pins 1-2 of the corresponding jumper block (pins 1-2 and 3-4 in CN30).

Table 6-17 Current Measurement Jumper Blocks CN29, CN30, CN35, CN36, and CN81 to CN87

No.	Function	Function
CN29	Current of CPU1V1 is measured.	**The jumper blocks are short-circuit at the time of shipment.** To measure the current, make the relevant jumper block open-circuit and insert an ammeter between pins 1-2 (pins 1-2 and 3-4 for CN30).
CN30	Current of CPU0V8 is measured.	
CN35	Current of CPU1V8 is measured.	
CN36	Current of CPU3V3 is measured.	
CN81	Current of CPU_VCC1833_0 is measured.	
CN82	Current of CPU_VCC1833_1 is measured.	
CN83	Current of CPU_VCC1833_2 is measured.	
CN84	Current of CPU_VCC1833_3 is measured.	
CN85	Current of CPU_VCC1833_4 is measured.	
CN86	Current of CPU_VCC1833_5 is measured.	
CN87	Current of CPU_VCC1833_6 is measured.	

6.5 Configuration by Option Links

6.5.1 Settings by Solder Bridges and Trace Cuts

This board is equipped with solder bridges E4 and E5, and trace cuts E1 to E3, E6, E7, E10, and E20 for selecting functions. Table 6-18 lists the settings of each solder bridge and trace cut.

Table 6-18 Settings of Solder Bridges and Trace Cuts

No.	Setting	Function
E1	Open-circuit	SEI (SW9) is not input to P08_6.
	Short-circuit	**SEI (SW9) is input to P08_6.**
E2	Open-circuit	PMOD1 (CN50) is not used with the SPI interface.
	Short-circuit	**PMOD1 (CN50) is used with the SPI interface.** **(In this case, E4 should be left open-circuit.)**
E3	Open-circuit	PMOD1 (CN50) is not used with the SPI interface.
	Short-circuit	**PMOD1 (CN50) is used with the SPI interface.** **(In this case, E5 should be left open-circuit.)**
E4	**Open-circuit**	**PMOD1 (CN50) is not used with the I^2C interface.**
	Short-circuit	PMOD1 (CN50) is used with the I^2C interface. (In this case, E2 should be left open-circuit.)
E5	**Open-circuit**	**PMOD1 (CN50) is not to be used with the I^2C interface.**
	Short-circuit	PMOD1 (CN50) is used with the I^2C interface. (In this case, E3 should be left open-circuit.)
E6	Open-circuit	Setting prohibited
	Short-circuit	**Pin 9 of CN60 (MIPI-10) is connected to the ground.**
E7	Open-circuit	P08_6 is not connected to DSMIF0 (CN21) and SEI (SW9) (not used as a DSMIF signal or SEI).
	Short-circuit	**P08_6 is connected to DSMIF0 (CN21) and SEI (SW9) (used as a DSMIF signal and SEI).**
E10	Open-circuit	Setting prohibited
	Short-circuit	**3.3-V power is supplied to the J-Link™ OB circuit.**
E20	Open-circuit	P05_2 is not connected to CN8 (not used as a PCIe-related signal).
	Short-circuit	**P05_2 is connected to CN8 (used as a PCIe-related signal).**

6.5.2 Settings by 0-Ω and Other Resistors

The following 0-Ω and other resistors are or can be placed on this board, and the function to be used can be selected by changing the Fit/DNF state from the state as shipped. Table 6-19 lists the settings of 0-Ω and other resistors.

Table 6-19 Settings by 0-Ω and Other Resistors

No.	Setting	Function
R172 (0 Ω)	**Fit**	**The termination resistor for CAN_H is enabled.**
	DNF	The termination resistor for CAN_H is disabled.
R173 (0 Ω)	**Fit**	**The termination resistor for CAN_L is enabled.**
	DNF	The termination resistor for CAN_L is disabled.
R182 (0 Ω)	**Fit**	**The DE signal is used in the RE control of the RS485.**
	DNF	The DE signal is not used in the RE control of the RS485. In this case, install R183 (10-kΩ) and fix the RE signal to the low level.
R187 (0 Ω)	**Fit**	**The 130-Ω termination resistor of RS485 A-B is enabled.**
	DNF	The 130-Ω termination resistor of RS485 A-B is disabled.
R191 (33 Ω)	**Fit**	**MII is used for the MAC-PHY interface of Ethernet port 0.**
	DNF	RGMII is used for the MAC-PHY interface of Ethernet port 0.
R155 (33 Ω)	**Fit**	**MII is used for the MAC-PHY interface of Ethernet port 1.**
	DNF	RGMII is used for the MAC-PHY interface of Ethernet port 1.
R23 (33 Ω)*	Fit	MII is used for the MAC-PHY interface of Ethernet port 2.
	DNF	**RGMII is used for the MAC-PHY interface of Ethernet port 2.**
R486 (33 Ω)*	Fit	MII is used for the MAC-PHY interface of Ethernet port 3.
	DNF	**RGMII is used for the MAC-PHY interface of Ethernet port 3.**

Note: When installing a resistor, use a 1608-size (mm) chip resistor.

7. User Circuits

This chapter describes the circuits on the board for each of its functions.

The initial state of this board at the time of shipment is indicated by the **text in bold blue type** in the "Settings of Configuration Circuits" column of each of the signal connection tables. Refer to the details on the configuration circuits in chapter 6.

7.1 Reset Circuit

A reset signal can be generated by the power-on reset IC and RES switch on the board. Figure 7-1 shows the configuration of the reset circuit.

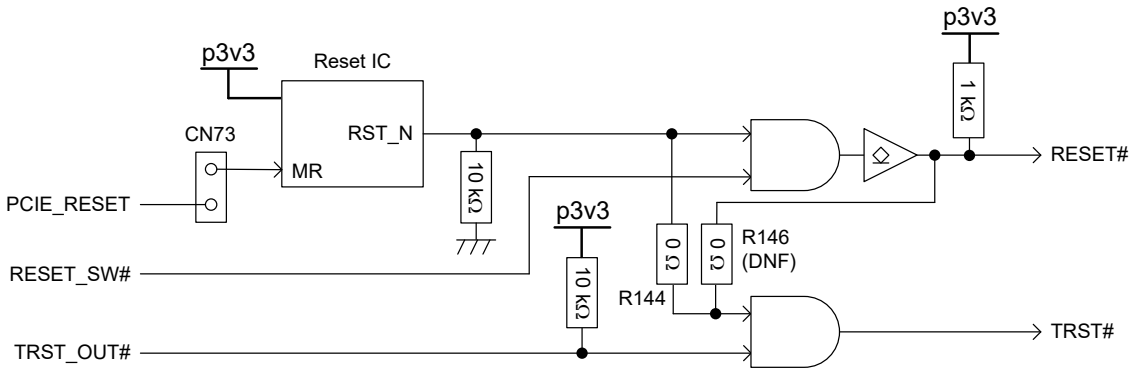


Figure 7-1 Configuration of Reset Circuit

7.2 Clock Circuit

Figure 7-2 shows the clock circuit for the RZ/T2H on this board. Table 7-1 lists the resonators.

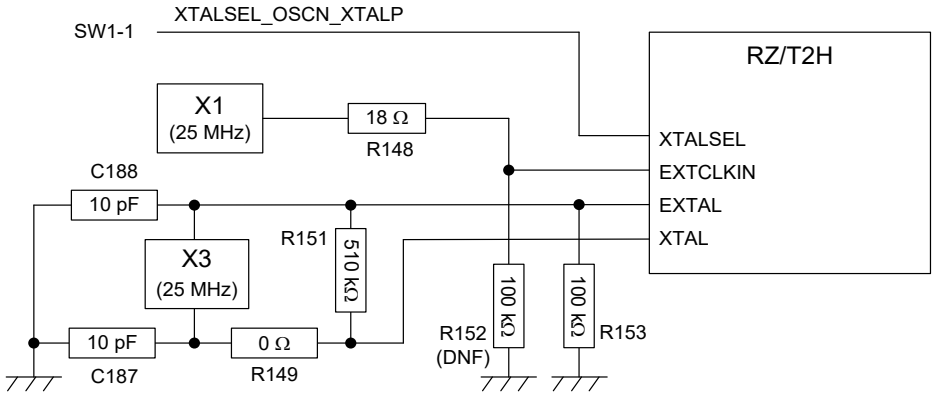


Figure 7-2 Configuration of Clock Circuit

Table 7-1 List of Resonators

Resonator	Function or Intended Use	State as Shipped	Frequency
X1	Clock for the RZ/T2H (oscillator)	Mounted	25 MHz
X2	Clock for the PCIe	Mounted	25 MHz
X3	Clock for the RZ/T2H	Mounted (disabled state)	25 MHz
X4	Clock for the USB-to-serial conversion IC	Mounted	12 MHz

7.3 Switches

This board is equipped with four push switches and 12 DIP switches in addition to the power switch described in section 2.2. Table 7-2 lists the functions and signal connections of the four push switches. Table 7-3 lists the functions and signal connections of user DIP switch SW12.

Among the DIP switches, SW14 is used for setting the mode of the RZ/T2H, and SW1, SW2, SW4 to SW8, SW15, SW17, and SW18 are used for selecting the functions of the signal lines. Refer to section 6.2 in which the switches are explained as part of the configuration circuitry of this board.

Table 7-2 Signal Connections of Push Switches

Switch	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
RES (SW13)	Reset switch	RES#*	AD4	—
SEI (SW9)	User push switch, connected to SEI.	P08_6	AD2	SW2-3: OFF, **E1: Short-circuit,** **E7: Short-circuit**
SW10	User push switch, connected to IRQ2.	P00_3	AG15	—
SW11	User push switch, connected to IRQ0.	P08_7	AF2	—

Note: Connected via the reset circuit.

Table 7-3 Signal Connections of DIP Switch SW12 for User Control

Switch	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
SW12-1	Connected to P35_3 for user control.	P35_3*	V22	**SW1-3: ON**
SW12-2	Connected to P35_4 for user control.	P35_4*	W24	**SW1-3: ON**
SW12-3	Connected to P35_5 for user control.	P35_5*	V24	**SW1-3: ON**
SW12-4	Connected to P35_6 for user control.	P35_6*	U22	**SW1-3: ON**

Note: Connected via the bus switch IC.

7.4 LEDs

This board is equipped with 20 LEDs. Table 7-4 lists the functions, colors, and signal connections of LEDs.

Table 7-4 Signal Connections of LEDs

LED	Color	Function or Intended Use	MPU		Settings of Configuration Circuits
			Port	Pin	
P15V (LED12)	Yellow	Indicator of the 15-V power-supply line	—	—	—
P3V3 (LED11)	Green	Indicator of the 3.3-V power-supply line	—	—	—
LED0	Green	User LED	P23_1*1	A20	**SW8-9: ON, SW8-10: OFF**
LED1	Green	User LED	P32_2*1	M22	**SW5-1: OFF, SW5-2: ON**
LED2	Yellow	User LED	P06_7	AF8	—
LED3	Red	User LED	P08_5*2	AE3	SW2-3: OFF
LED4_ESC_RUN	Green	User LED or ESC_LEDRUN	P18_0*1	D15	**SW8-3: ON, SW8-4: OFF**
LED5_ESC_ERR	Red	User LED or ESC_LEDERR	P18_1*1	E13	**SW8-1: ON, SW8-2: OFF**
LED6_ESC_L/A0	Green	User LED or ESC_LINKACT0	P22_7*1	G21	**SW5-9: OFF, SW5-10: ON**
LED7_ESC_L/A1	Green	User LED or ESC_LINKACT1	P23_0*1	G20	**SW5-7: OFF, SW5-8: ON**
LED8_ESC_L/A2	Green	User LED or ESC_LINKACT2	P23_5*1	C21	**SW7-5: OFF, SW7-6: ON**
LED10	Yellow	Indicator of J-Link™ OB	—	—	—
LED built in CN59	Green	Ethernet port 0 LED (Link)	—	—	—
LED built in CN59	Yellow	Ethernet port 0 LED (Activity)	—	—	—
LED built in CN44	Green	Ethernet port 1 LED (Link)	—	—	—
LED built in CN44	Yellow	Ethernet port 1 LED (Activity)	—	—	—
LED built in CN45	Green	Ethernet port 2 LED (Link)	—	—	—
LED built in CN45	Yellow	Ethernet port 2 LED (Activity)	—	—	—
LED built in CN1	Green	Ethernet port 3 LED (Link)	—	—	—
LED built in CN1	Yellow	Ethernet port 3 LED (Activity)	—	—	—

Notes: 1. Connected via DIP switches. If the factory settings are used, they can be used for controlling LEDs.
2. Connected via the bus switch IC.

7.5 Potentiometer

On this board, a 10-kΩ single-rotation potentiometer for evaluating the ADC is connected to AN000 (pin AA27) of the RZ/T2H. Figure 7-3 shows the configuration of the potentiometer circuit.

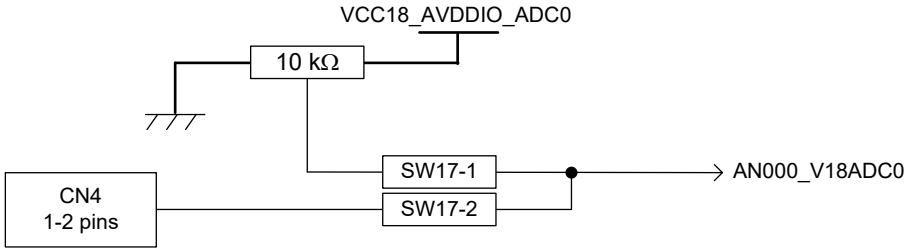


Figure 7-3 Configuration of Potentiometer Circuit

A potentiometer is installed to provide an easy way of supplying a variable analog input to the microprocessor. Note in advance that it will not guarantee the accuracy of the A/D converter.

7.6 Pmod™

This board is equipped with two connectors for Digilent Pmod™ interfaces so that compatible Pmod™ modules can be connected and evaluated. PMOD1 (CN50) supports the type 2A and 6A Pmod™ interfaces and PMOD2 (CN49) supports type 3A. Figure 7-4 shows the configuration of the Pmod™ interface circuits. Table 7-5 and Table 7-6 list the signal connections. Figure 7-5 shows the switch settings when using PMOD1 and PMOD2.

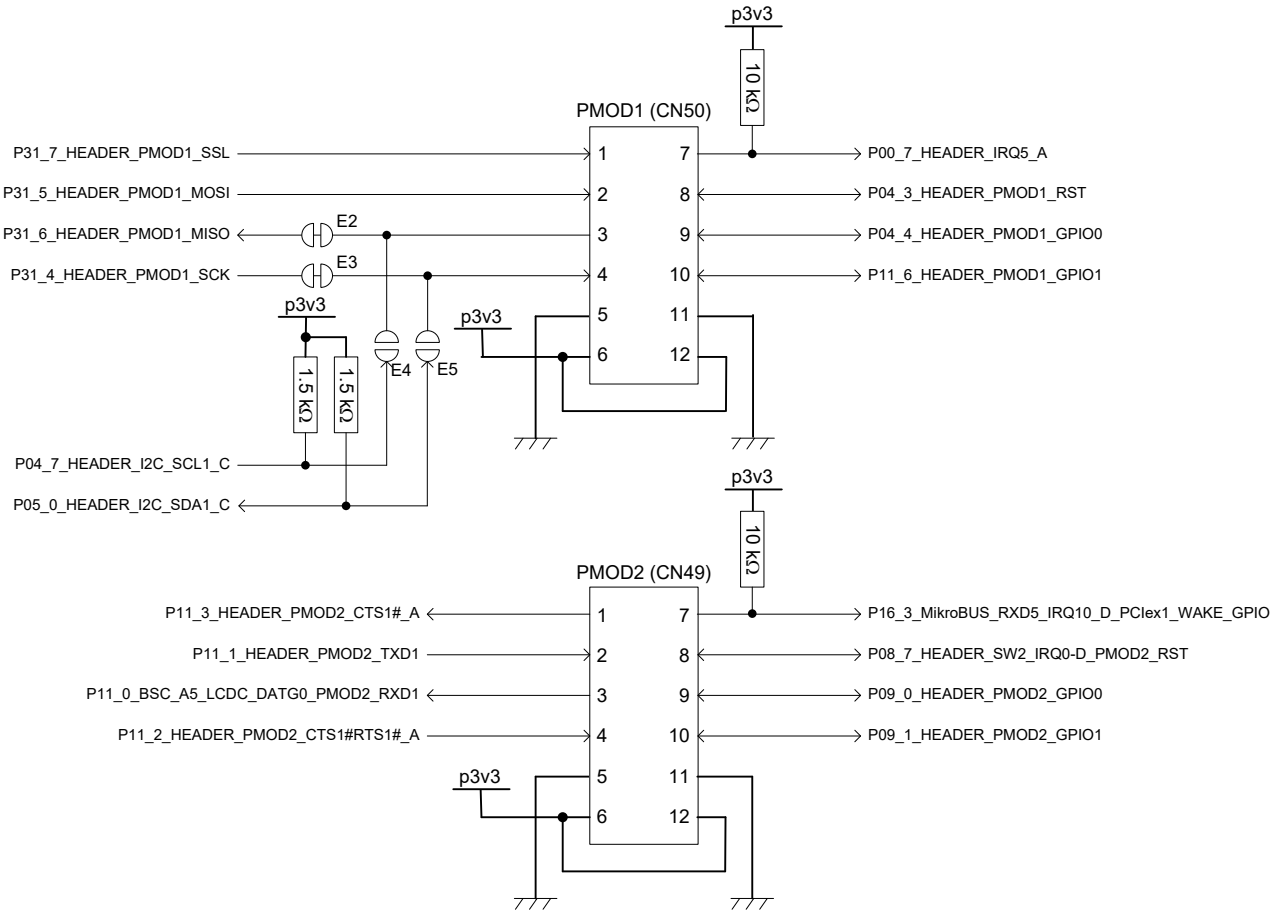


Figure 7-4 Configuration of Pmod™ Interface Circuits

Table 7-5 Signal Connections of PMOD1 Connector (CN50)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P31_7_HEADER_PMOD1_SSL	P31_7	M26	—
2	P31_5_HEADER_PMOD1_MOSI	P31_5*1	P26	SW2-7: OFF
3	P31_6_HEADER_PMOD1_MISO	P31_6	P25	**E2: Short-circuit, E4: Open-circuit**
	P04_7_HEADER_I2C_SCL1_C	P04_7*2	AC11	E2: Open-circuit, E4: Short-circuit
4	P31_4_HEADER_PMOD1_SCK	P31_4*1	N25	SW2-7: OFF, **E3: Short-circuit, E5: Open-circuit**
	P05_0_HEADER_I2C_SDA1_C	P05_0*2	AA10	E3: Open-circuit, E5: Short-circuit
5	GROUND	—	—	—
6	p3v3	—	—	—
7	P00_7_HEADER_IRQ5_A	P00_7	AE14	—
8	P04_3_HEADER_PMOD1_RST	P04_3	AG10	—
9	P04_4_HEADER_PMOD1_GPIO0	P04_4	AG11	—
10	P11_6_HEADER_PMOD1_GPIO1	P11_6	A3	—
11	GROUND	—	—	—
12	p3v3	—	—	—

Notes: 1. Connected via the bus switch IC.
2. To change the function, the setting of a solder bridge jumper has to be changed.

Table 7-6 Signal Connections of PMOD2 Connector (CN49)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P11_3_HEADER_PMOD2_CTS1#_A	P11_3	D1	—
2	P11_1_HEADER_PMOD2_TXD1	P11_1	C1	—
3	P11_0_BSC_A5_LCDC_DATG0_PMOD2_RXD1	P11_0*	C5	SW6-3: OFF, SW6-4: ON, SW6-5: OFF
4	P11_2_HEADER_PMOD2_CTS1#RTS1#_A	P11_2	C3	—
5	GROUND	—	—	—
6	p3v3	—	—	—
7	P16_3_MikroBUS_RXD5_IRQ10_D_PCIex1_WAKE_GPIO	P16_3*	B12	SW8-5: OFF, SW8-6: ON
8	P08_7_HEADER_SW2_IRQ0-D_PMOD2_RST	P08_7	AF2	—
9	P09_0_HEADER_PMOD2_GPIO0	P09_0	AE1	—
10	P09_1_HEADER_PMOD2_GPIO1	P09_1	AG2	—
11	GROUND	—	—	—
12	p3v3	—	—	—

Note: Connected via SW6 or SW8.

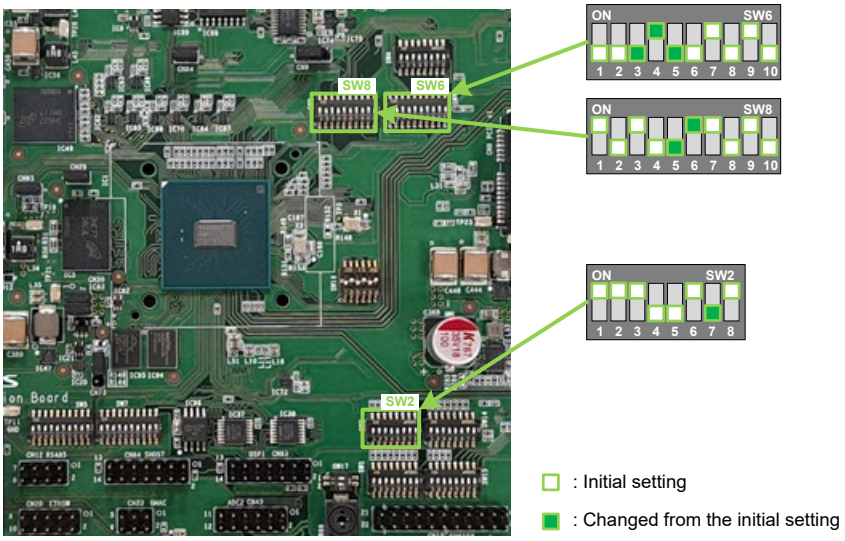


Figure 7-5 Switch Settings When Using PMOD1 and PMOD2

Note that the pin assignment for a Digilent Pmod™ connector differs in terms of numbering from that for a typical connector. Figure 7-6 shows the pin assignment for a Pmod™ connector. For details, refer to the Digilent Pmod™ Interface Specification.

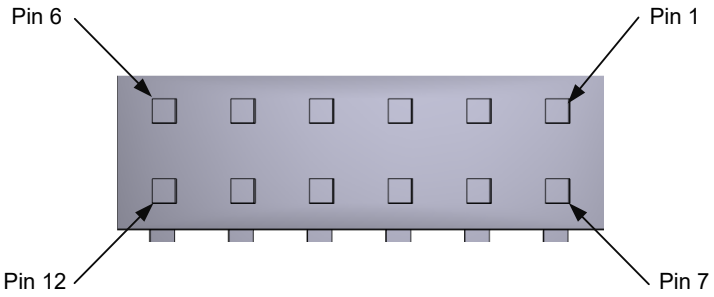


Figure 7-6 Pin Assignment for a Digilent Pmod™ Connector (Viewed from the Direction of Insertion)

7.7 Grove

This board is equipped with two connectors for Grove interfaces so that compatible Grove modules can be connected and evaluated. Figure 7-7 shows the configuration of the Grove interface circuits. Figure 7-8 shows the pin assignment for a Grove connector. Table 7-7 and Table 7-8 list the signal connections.

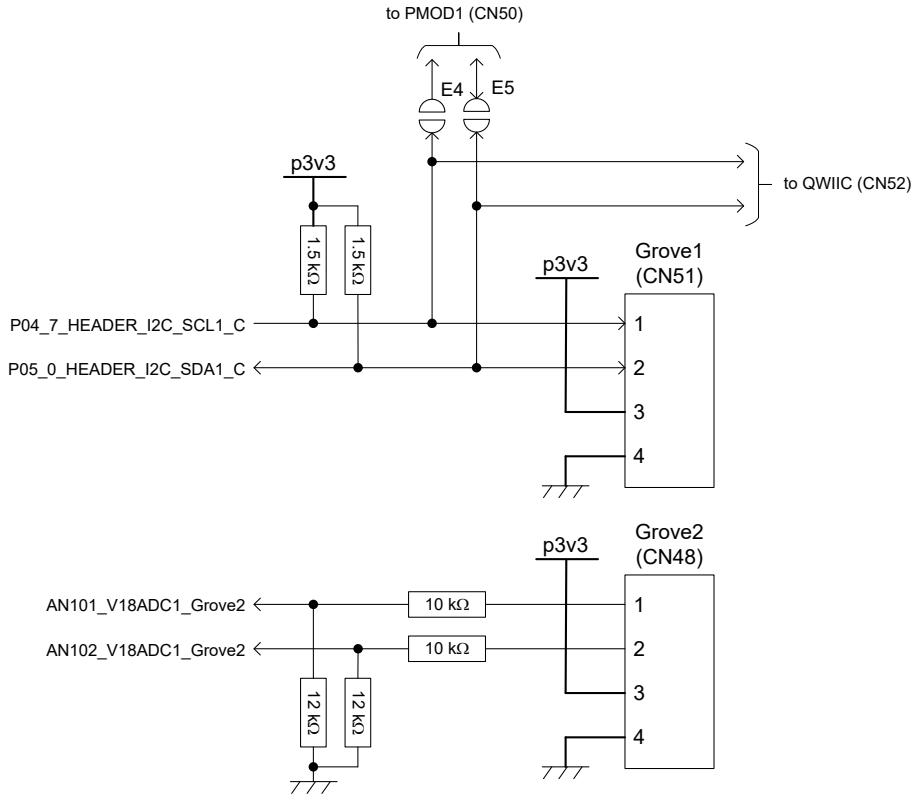


Figure 7-7 Configuration of Grove Interface Circuits

Table 7-7 Signal Connections of Grove1 Connector (CN51)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P04_7_HEADER_I2C_SCL1_C	P04_7*	AC11	—
2	P05_0_HEADER_I2C_SDA1_C	P05_0*	AA10	—
3	p3v3	—	—	—
4	GROUND	—	—	—

Note: Shared with QWIIC and other interfaces.

Table 7-8 Signal Connections of Grove2 Connector (CN48)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	AN101_V18ADC1_Grove2	AN101*	AD27	**SW18-3: OFF, SW18-4: ON**
2	AN102_V18ADC1_Grove2	AN102*	AD26	**SW18-5: OFF, SW18-6: ON**
3	p3v3	—	—	—
4	GROUND	—	—	—

Note: Connected via SW18.

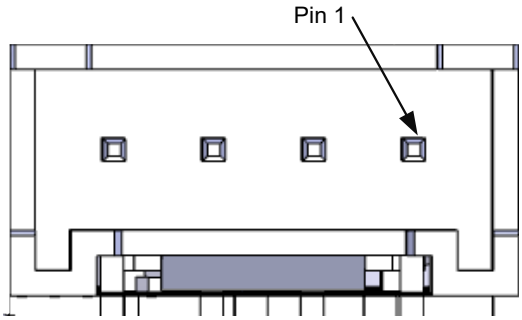


Figure 7-8 Pin Assignment for a Grove Connector (Viewed from the Direction of Insertion)

7.8 QWIIC

This board is equipped with a connector for the QWIIC interface so that a compatible QWIIC module can be connected and evaluated. Figure 7-9 shows the pin assignment for a QWIIC connector. Table 7-9 lists the signal connections.

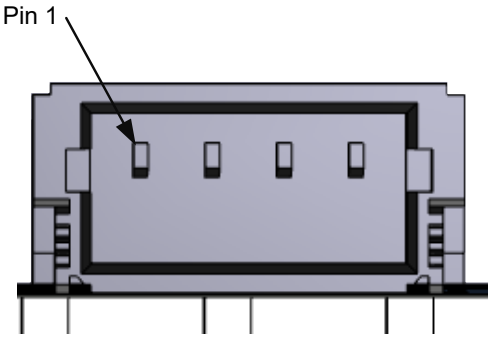


Figure 7-9 Pin Assignment for a QWIIC Connector (Viewed from the Direction of Insertion)

Table 7-9 Signal Connections of QWIIC Connector (CN52)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	GROUND	—	—	—
2	p3v3	—	—	—
3	P05_0_HEADER_I2C_SDA1_C	P05_0*	AA10	—
4	P04_7_HEADER_I2C_SCL1_C	P04_7*	AC11	—

Note: Shared with Grove2 and other interfaces.

7.9 mikroBUS™

This board is equipped with two connectors for mikroBUS™ interfaces so that compatible mikroBUS™ modules can be connected and evaluated. Figure 7-10 shows the configuration of the mikroBUS™ interface circuits. Table 7-10 and Table 7-11 list the signal connections. Figure 7-11 shows the switch settings when using mikroBUS™.

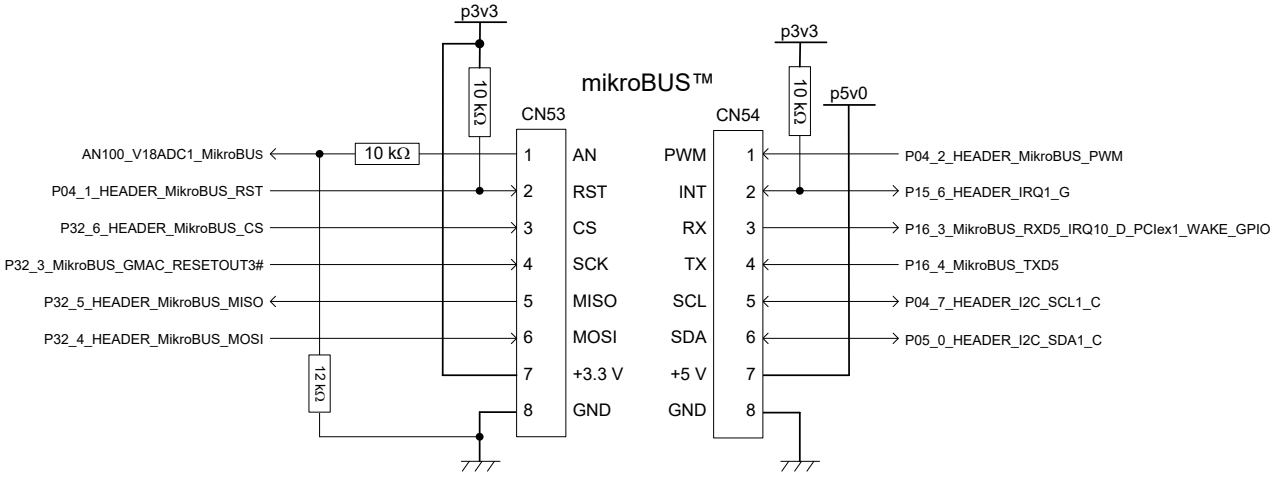


Figure 7-10 Configuration of mikroBUS™ Interface Circuits

Table 7-10 Signal Connections of mikroBUS™ Connector (CN53)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	AN100_V18ADC1_MikroBUS	AN100*	AC27	**SW18-1: OFF, SW18-2: ON**
2	P04_1_HEADER_MikroBUS_RST	P04_1	AF11	—
3	P32_6_HEADER_MikroBUS_CS	P32_6	L27	—
4	P32_3_MikroBUS_GMAC_RESETOUT3#	P32_3	N23	—
5	P32_5_HEADER_MikroBUS_MISO	P32_5	M27	—
6	P32_4_HEADER_MikroBUS_MOSI	P32_4	N22	—
7	p3v3	—	—	—
8	GROUND	—	—	—

Note: Connected via SW18.

Table 7-11 Signal Connections of mikroBUS™ Connector (CN54)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P04_2_HEADER_MikroBUS_PWM	P04_2	AA12	—
2	P15_6_HEADER_IRQ1_G	P15_6	D10	—
3	P16_3_MikroBUS_RXD5_IRQ10_D_PCIex1_WAKE_GPIO	P16_3*1	B12	SW8-5: OFF, SW8-6: ON
4	P16_4_MikroBUS_TXD5	P16_4*1	A12	SW8-7: OFF, SW8-8: ON
5	P04_7_HEADER_I2C_SCL1_C	P04_7*2	AC11	—
6	P05_0_HEADER_I2C_SDA1_C	P05_0*2	AA10	—
7	p5v0	—	—	—
8	GROUND	—	—	—

Notes: 1. Connected via SW8.
2. Shared with Grove2 and other interfaces.

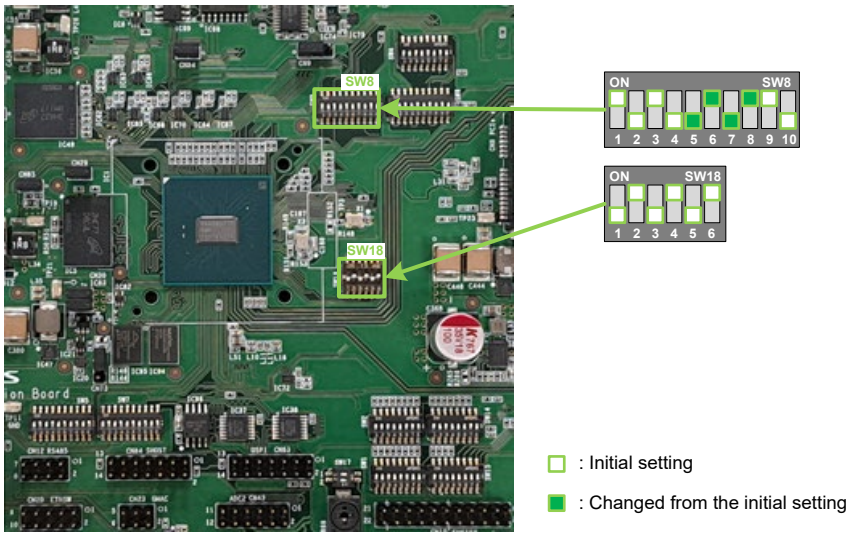


Figure 7-11 Switch Settings When Using mikroBUS™

7.10 USB-to-Serial Conversion

This board is equipped with a USB connector (CN34) for terminal output and an FT2232 for USB-to-serial conversion. Figure 7-12 shows the configuration of the USB-to-serial conversion circuit. Table 7-12 lists the signal connections.

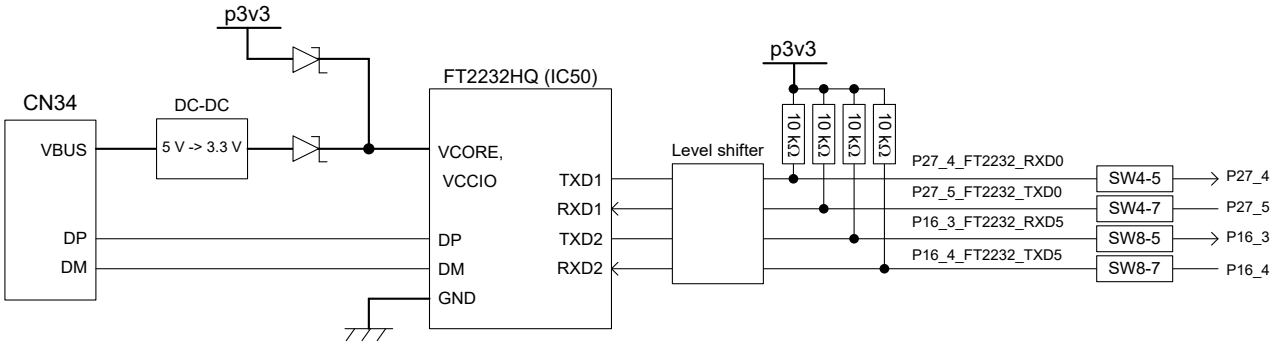


Figure 7-12 Configuration of USB-to-Serial Conversion Circuit

Table 7-12 Signal Connections of USB-to-Serial Conversion

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P27_4_FT2232_RXD0	UART data reception 1 for USB-to-serial conversion	P27_4*	H26	**SW4-5: ON, SW4-6: OFF**
P27_5_FT2232_TXD0	UART data transmission 1 for USB-to-serial conversion	P27_5*	F25	**SW4-7: ON, SW4-8: OFF**
P16_3_FT2232_RXD5	UART data reception 2 for USB-to-serial conversion	P16_3*	B12	**SW8-5: ON, SW8-6: OFF**
P16_4_FT2232_TXD5	UART data transmission 2 for USB-to-serial conversion	P16_4*	A12	**SW8-7: ON, SW8-8: OFF**

Note: Connected via SW4 or SW8.

When the USB connector (CN34) for terminal output is first connected to a PC, the PC will search for a driver. A driver with the standard specification that has been installed on the PC should be used.

7.11 SPI Memory

This board has OctaFlash, Quad SPI flash memory, and EEPROM as SPI memory. An SPI expansion connector (CN63) is also connected to SPI1.

Figure 7-13 shows the configuration of the SPI memory circuits, and Table 7-13 lists the SPI memories. Table 7-14, Table 7-15, and Table 7-16 list the signal connections for each memory. Table 7-17 lists the signal connections for the SPI expansion connector. Figure 7-14 shows the switch settings when using SPI memory.

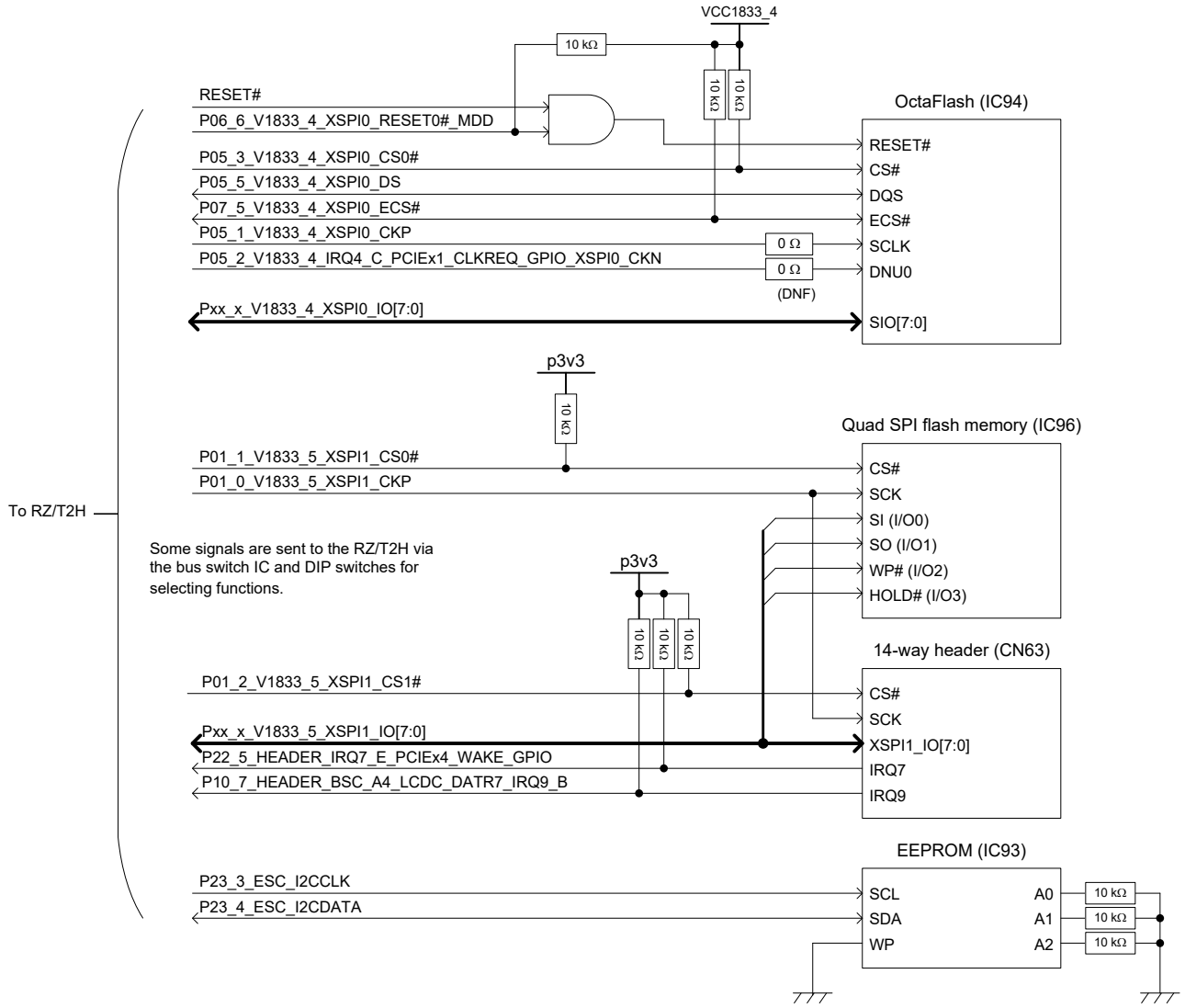


Figure 7-13 Configuration of SPI Memory Circuits

Table 7-13 List of SPI Memories

SPI Memory	Reference	Controller	Address Space
OctaFlash (512 Mbits)	IC94	XSPI0_CS0	40000000h to 43FFFFFFh (64 Mbytes)
Quad SPI flash memory (128 Mbits)	IC96	XSPI1_CS0	50000000h to 50FFFFFFh (16 Mbytes)
EEPROM (16 Kbits)	IC93	I2C or EtherCAT	—

Table 7-14 Signal Connections of OctaFlash

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P06_6_V1833_4_XSPI0_RESET0#_MDD	Reset for CS0	P06_6	AG8	—
P05_3_V1833_4_XSPI0_CS0#	CS0#	P05_3	AG4	—
P05_5_V1833_4_XSPI0_DS	DS	P05_5	AF5	—
P07_5_V1833_4_XSPI0_ECS#	ECS#	P07_5*	AG6	SW5-5: OFF, SW5-6: ON
P05_1_V1833_4_XSPI0_CKP	CKP	P05_1	AA8	—
P05_2_V1833_4_IRQ4_C_PCIEx1_CLKREQ_GPIO_XSPI0_CKN	CKN	P05_2	AA9	—
P06_5_V1833_4_XSPI0_IO7	Data 7	P06_5	AA7	—
P06_4_V1833_4_XSPI0_IO6	Data 6	P06_4	AB8	—
P06_3_V1833_4_XSPI0_IO5	Data 5	P06_3	AB7	—
P06_2_V1833_4_XSPI0_IO4	Data 4	P06_2	AE6	—
P06_1_V1833_4_XSPI0_IO3	Data 3	P06_1	AC6	—
P06_0_V1833_4_XSPI0_IO2	Data 2	P06_0	AE5	—
P05_7_V1833_4_XSPI0_IO1	Data 1	P05_7	AE7	—
P05_6_V1833_4_XSPI0_IO0	Data 0	P05_6	AD6	—

Note: Connected via SW5.

Table 7-15 Signal Connections of Quad SPI Flash Memory

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P01_1_V1833_5_XSPI1_CS0#	CS0#	P01_1*	AG12	SW1-6: ON
P01_0_V1833_5_XSPI1_CKP	CKP	P01_0*	AF13	SW1-6: ON
P01_7_V1833_5_XSPI1_IO3	Data 3	P01_7*	AC13	SW1-6: ON
P01_6_V1833_5_XSPI1_IO2	Data 2	P01_6*	AD13	SW1-6: ON
P01_5_V1833_5_XSPI1_IO1	Data 1	P01_5*	AE13	SW1-6: ON
P01_4_V1833_5_XSPI1_IO0	Data 0	P01_4*	AG13	SW1-6: ON

Note: Connected via the bus switch IC.

Table 7-16 Signal Connections of EEPROM

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P23_3_ESC_I2CCLK	EtherCAT I2CCLK	P23_3*	A21	SW6-7: ON, SW6-8: OFF
P23_4_ESC_I2CDATA	EtherCAT I2CDATA	P23_4*	C20	SW6-9: ON, SW6-10: OFF

Note: Connected via SW6.

Table 7-17 Signal Connections of SPI Expansion Connector (CN63)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	GROUND	—	—	—
2	P22_5_HEADER_IRQ7_E_PCIEx4_WAKE_GPIO	P22_5*1	E21	SW2-1: ON, SW2-2: OFF
3	P01_0_V1833_5_XSPI1_CKP	P01_0*2	AF13	**SW1-6: ON**
4	P01_2_V1833_5_XSPI1_CS1#	P01_2*2	AD14	**SW1-6: ON**
5	P02_3_V1833_5_XSPI1_IO7	P02_3*2	AF12	**SW1-6: ON**
6	P02_2_V1833_5_XSPI1_IO6	P02_2*2	AA13	**SW1-6: ON**
7	P02_1_V1833_5_XSPI1_IO5	P02_1*2	AB13	**SW1-6: ON**
8	P02_0_V1833_5_XSPI1_IO4	P02_0*2	AC14	**SW1-6: ON**
9	P01_7_V1833_5_XSPI1_IO3	P01_7*2	AC13	**SW1-6: ON**
10	P01_6_V1833_5_XSPI1_IO2	P01_6*2	AD13	**SW1-6: ON**
11	P01_5_V1833_5_XSPI1_IO1	P01_5*2	AE13	**SW1-6: ON**
12	P01_4_V1833_5_XSPI1_IO0	P01_4*2	AG13	**SW1-6: ON**
13	P10_7_HEADER_BSC_A4_LCDC_DATR7_IRQ9_B	P10_7	C4	—
14	p3v3	—	—	—

Notes: 1. Connected via the level shifter IC with an enable function.
2. Connected via the bus switch IC.

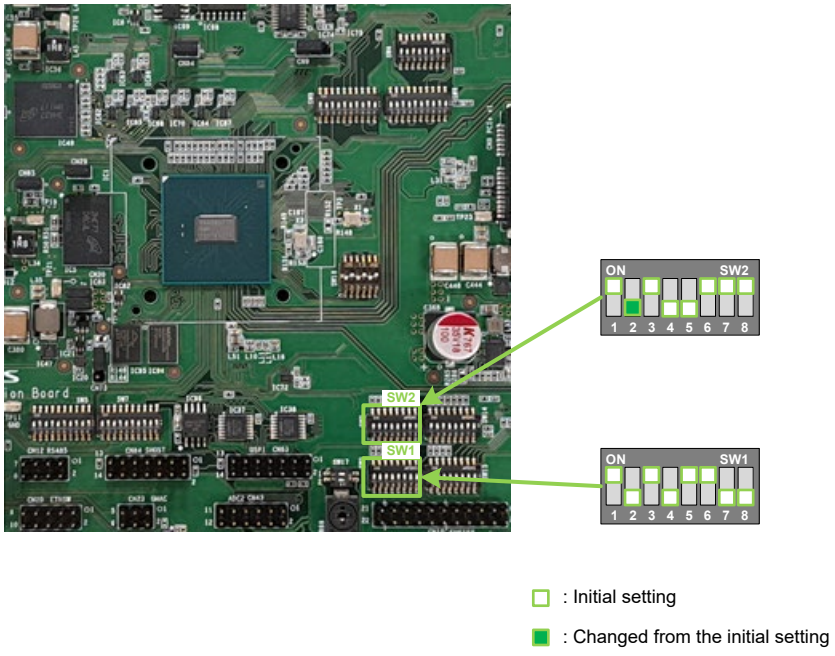


Figure 7-14 Switch Settings When Using SPI Memory

7.12 LPDDR4

This board is equipped with LPDDR4. Figure 7-15 shows the signal connections of LPDDR4.

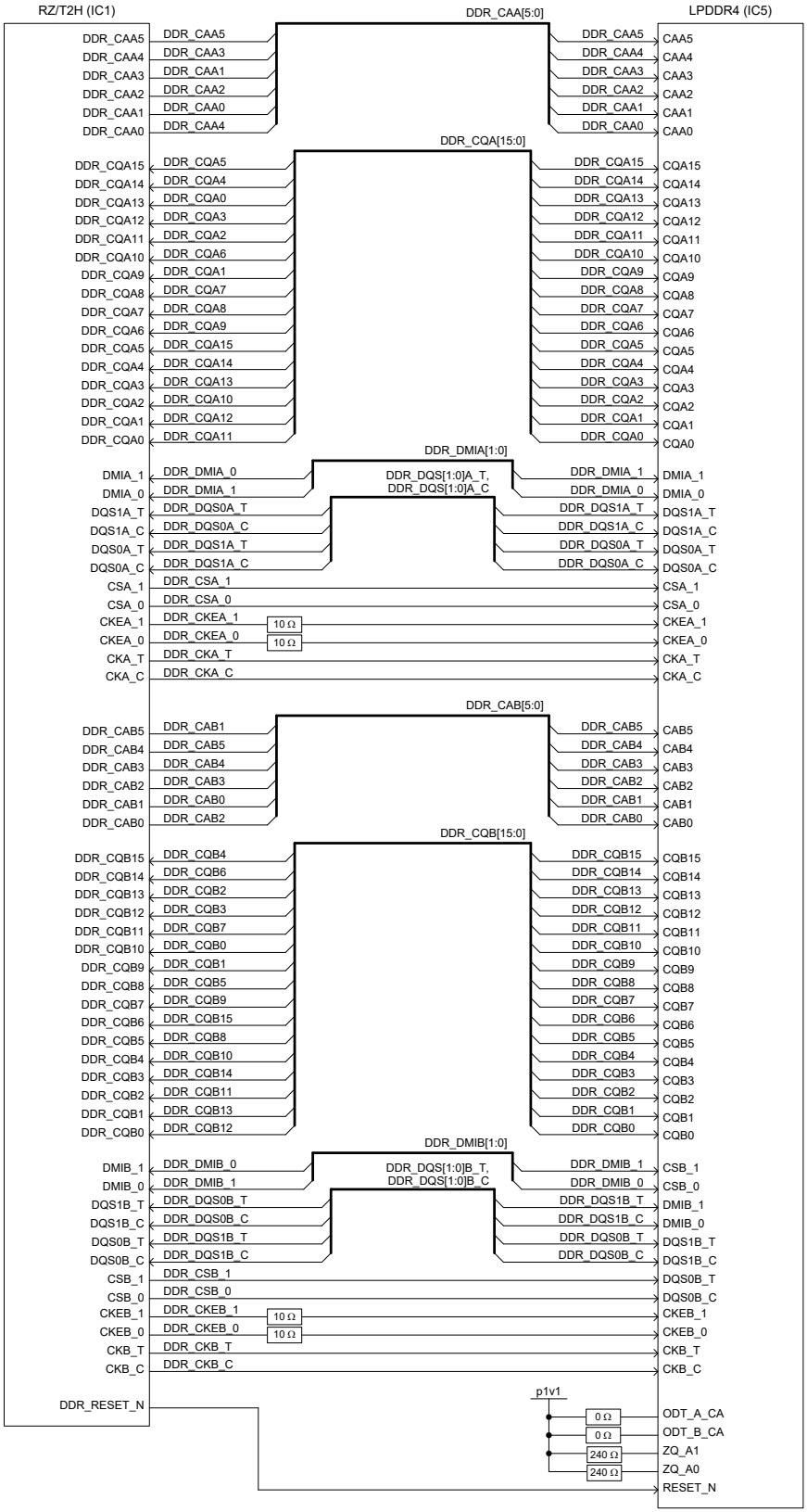


Figure 7-15 Signal Connections of LPDDR4

7.13 SD and eMMC

This board is equipped with an SD card slot (CN31), a microSD card slot (CN16), and eMMC (IC49). Figure 7-16 shows the configuration of the SD and eMMC circuit. Table 7-18, Table 7-19, and Table 7-20 list the signal connections. Figure 7-17 shows the switch settings when using the SD card slot (CN31).

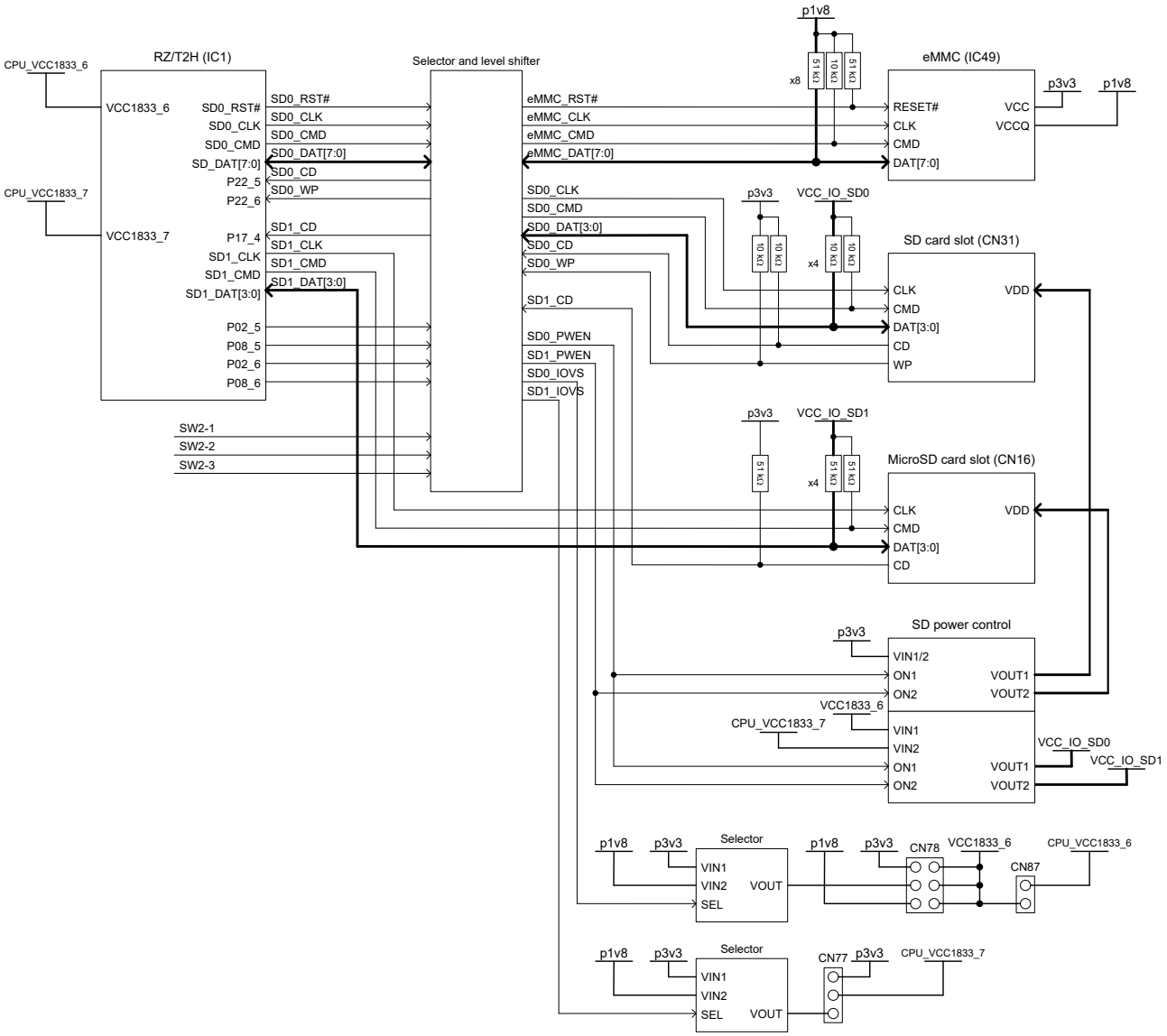


Figure 7-16 Configuration of SD and eMMC Circuit

Table 7-18 Signal Connections of eMMC

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P13_2_P1V8_eMMC_RST#	Reset	P13_2*	F8	**SW2-1: ON, SW2-2: ON**
P12_1_P1V8_eMMC_CMD	Command	P12_1*	G8	**SW2-1: ON, SW2-2: ON**
P12_0_P1V8_eMMC_CLK	Clock	P12_0*	D7	**SW2-1: ON, SW2-2: ON**
P12_2_P1V8_eMMC_DAT0	Data 0	P12_2*	E8	**SW2-1: ON, SW2-2: ON**
P12_3_P1V8_eMMC_DAT1	Data 1	P12_3*	E7	**SW2-1: ON, SW2-2: ON**
P12_4_P1V8_eMMC_DAT2	Data 2	P12_4*	B6	**SW2-1: ON, SW2-2: ON**
P12_5_P1V8_eMMC_DAT3	Data 3	P12_5*	G7	**SW2-1: ON, SW2-2: ON**
P12_6_P1V8_eMMC_DAT4	Data 4	P12_6*	D6	**SW2-1: ON, SW2-2: ON**
P12_7_P1V8_eMMC_DAT5	Data 5	P12_7*	E6	**SW2-1: ON, SW2-2: ON**
P13_0_P1V8_eMMC_DAT6	Data 6	P13_0*	C7	**SW2-1: ON, SW2-2: ON**
P13_1_P1V8_eMMC_DAT7	Data 7	P13_1*	F7	**SW2-1: ON, SW2-2: ON**

Note: Connected via the level shifter IC with an enable function.

Table 7-19 Signal Connections of SD Card Slot

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P12_1_VCC_SD0_CMD	Command	P12_1*	G8	SW2-1: OFF, SW2-2: ON
P12_0_VCC_SD0_CLK	Clock	P12_0*	D7	SW2-1: OFF, SW2-2: ON
P12_2_VCC_SD0_DAT0	Data 0	P12_2*	E8	SW2-1: OFF, SW2-2: ON
P12_3_VCC_SD0_DAT1	Data 1	P12_3*	E7	SW2-1: OFF, SW2-2: ON
P12_4_VCC_SD0_DAT2	Data 2	P12_4*	B6	SW2-1: OFF, SW2-2: ON
P12_5_VCC_SD0_DAT3	Data 3	P12_5*	G7	SW2-1: OFF, SW2-2: ON
P22_5_SD0_CD_A	Card detection	P22_5*	E21	SW2-1: OFF, SW2-2: ON
P22_6_SD0_WP_A	Write protection	P22_6*	C22	SW2-1: OFF, SW2-2: ON
P02_5_SD0_PWEN_A	Power supply control	P02_5*	AD11	SW2-1: OFF, SW2-2: ON
P02_6_SD0_IOVS_A	IO voltage selection of SD0	P02_6*	AD9	SW2-1: OFF, SW2-2: ON

Note: Connected via the level shifter IC with an enable function.

Table 7-20 Signal Connections of MicroSD Card Slot

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P16_6_V1833_7_SD1_CMD	Command	P16_6	C12	—
P16_5_V1833_7_SD1_CLK	Clock	P16_5	G12	—
P16_7_V1833_7_SD1_DAT0	Data 0	P16_7	F12	—
P17_0_V1833_7_SD1_DAT1	Data 1	P17_0	A13	—
P17_1_V1833_7_SD1_DAT2	Data 2	P17_1	B13	—
P17_2_V1833_7_SD1_DAT3	Data 3	P17_2	E12	—
P17_4_SD1_CD_A	Card detection	P17_4*1	G13	**SW2-3: ON**
P08_5_SD1_PWEN_A	Power supply control	P08_5*1	AE3	**SW2-3: ON**
P08_6_SD1_IOVS_A_P32_2_GPIO	IO voltage selection of SD1	P08_6*1, *2	AD2	**SW2-3: ON, SW5-3: OFF, SW5-4: ON**
		P32_2*2	M22	SW5-1: ON, SW5-2: OFF, SW5-3: ON, SW5-4: OFF

Notes: 1. Connected via the bus switch IC.
2. Connected via SW5.

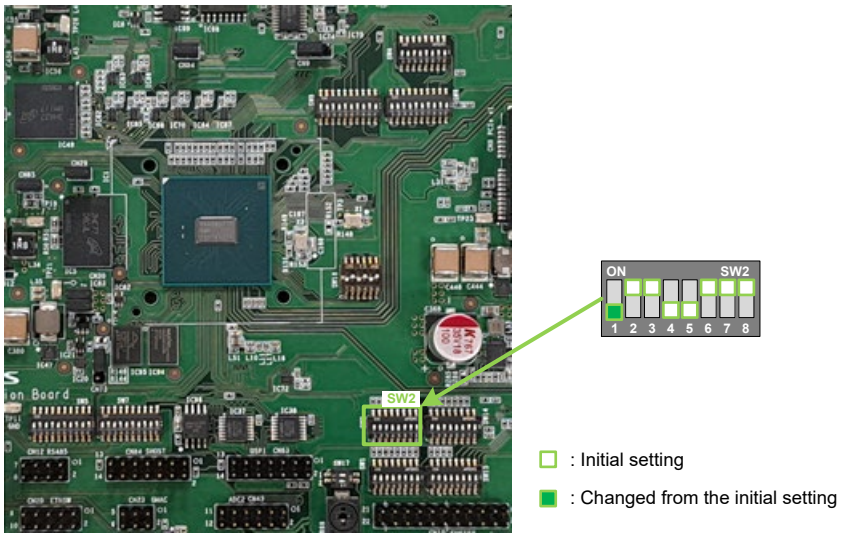


Figure 7-17 Switch Settings When Using the SD Card Slot (CN31)

7.14 CAN

This board is equipped with a CAN transceiver (IC84) and a CAN interface connector (CN55) so that the CAN module of the RZ/T2H can be evaluated. Figure 7-18 shows the configuration of the CAN interface circuit, and Table 7-21 lists the signal connections.

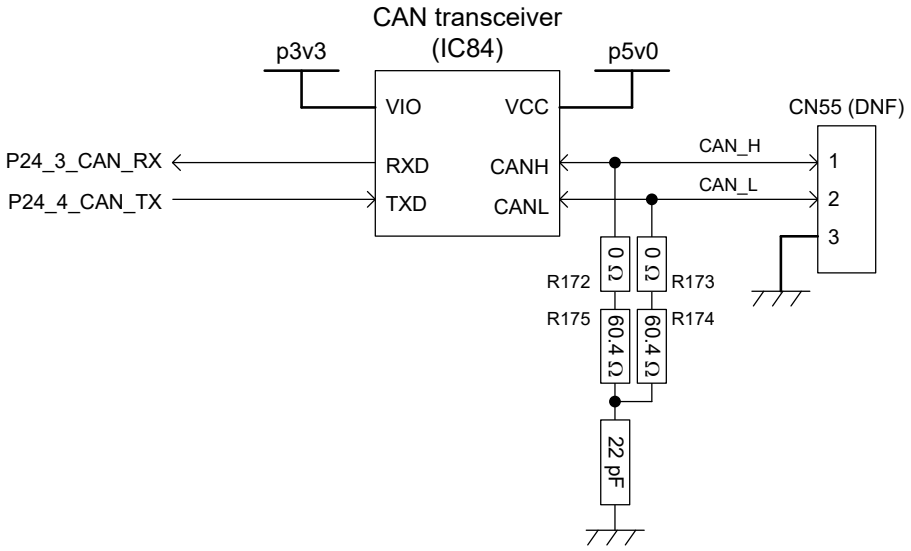


Figure 7-18 Configuration of CAN Interface Circuit

Table 7-21 Signal Connections of CAN

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P24_3_CAN_RX	Reception of CAN data	P24_3*	B20	**SW7-3: OFF, SW7-4: ON**
P24_4_CAN_TX	Transmission of CAN data	P24_4*	G22	**SW7-1: OFF, SW7-2: ON**

Note: Connected via SW7.

7.15 RS485 Interface

This board is equipped with an RS485 transceiver (IC88), an RS485 interface connector (CN58), and an RS485 external expansion connector (CN12). Figure 7-19 shows the configuration of the RS485 interface circuits, Table 7-22 lists the signal connections of the connector, and Table 7-23 lists the ports to be used.

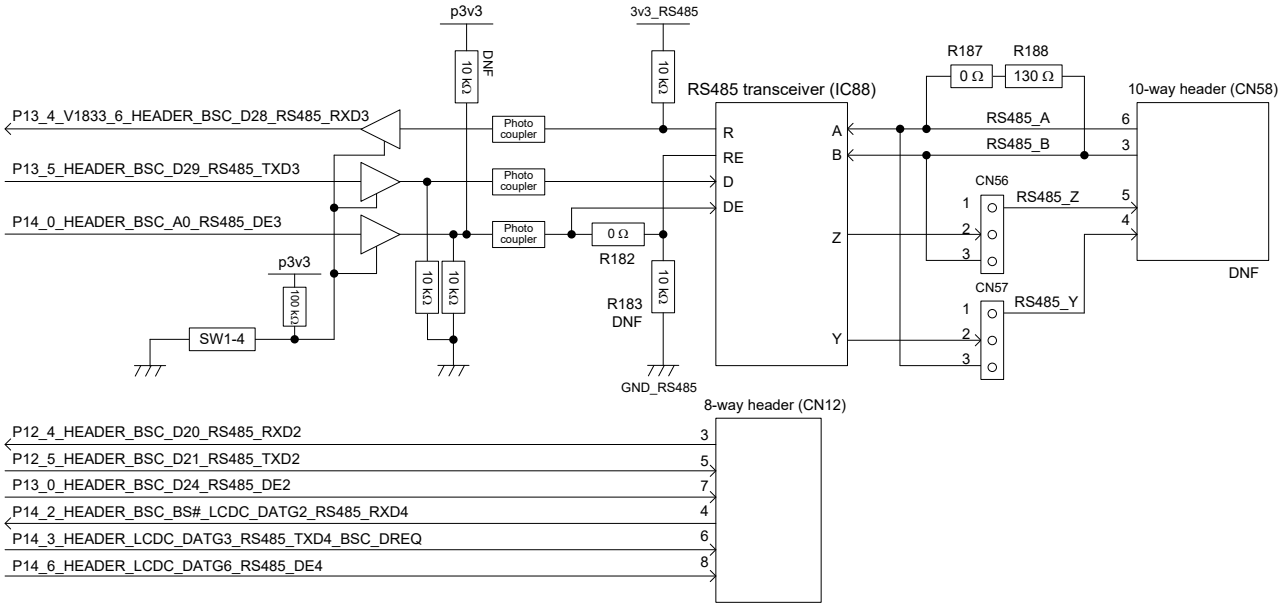


Figure 7-19 Configuration of RS485 Interface Circuits

Table 7-22 Signal Connections of RS485 Interface Connector (CN58)

Pin	Signal Name	Pin	Signal Name
1	GROUND	2	GROUND
3	RS485_B	4	RS485_Y
5	RS485_Z	6	RS485_A
7	GROUND	8	GROUND
9	GROUND	10	GROUND

Table 7-23 Ports Used with the RS485 Interface

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P13_4_V1833_6_HEADER_BSC_D28_RS485_RXD3	Reception of data	P13_4*	B8	SW1-4: OFF
P14_0_HEADER_BSC_A0_RS485_DE3	Driver enable signal	P14_0*	A7	SW1-4: OFF
P13_5_HEADER_BSC_D29_RS485_TXD3	Transmission of data	P13_5*	B7	SW1-4: OFF

Note: Connected via the buffer IC.

7.16 USB

This board is equipped with a USB type-A connector (CN80) and a mini-B connector (CN79). The USB function of the RZ/T2H can be used for either a USB host interface or a USB function interface (both cannot be used at the same time). The USB micro-AB connector (CN33) cannot be used.

Figure 7-20 shows the configuration of the USB circuit, and Table 7-24 lists the signal connections.

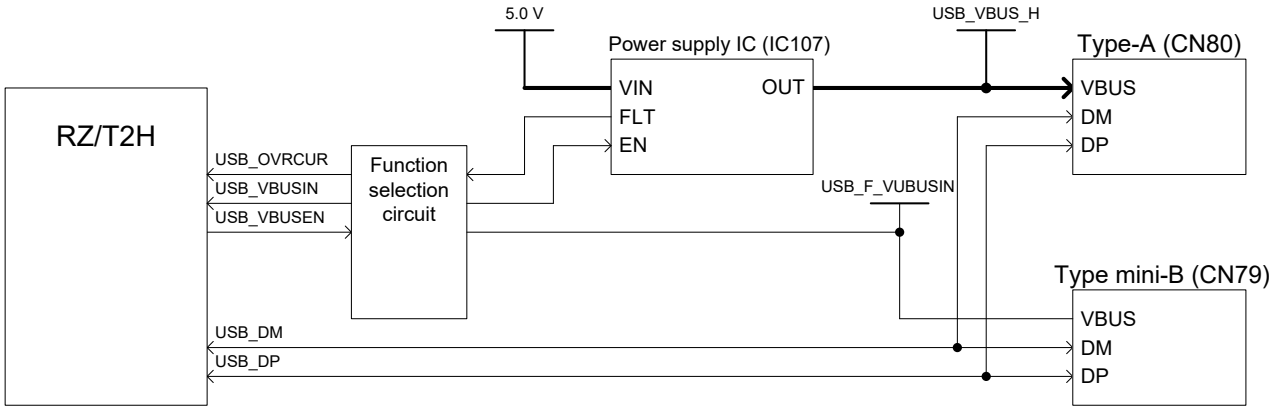


Figure 7-20 Configuration of USB Circuit

Table 7-24 Signal Connections of USB

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
USB_DP	Input/output of D+ data	USB_DP	AF17	—
USB_DM	Input/output of D- data	USB_DM	AG17	—
VUBUSIN	VBUS detection	USB_VUBUSIN*2	AD16	**SW7-7: OFF, SW7-8: ON**
P00_0_USB_VBUSEN_A	VBUS enable signal	P00_0*1, *3	AE15	**SW1-5: ON, SW7-9: OFF, SW7-10: ON**
P00_1_USB_OVRCUR_A	Overcurrent	P00_1*1	AD15	**SW1-5: ON**

Notes: 1. Connected via the bus switch IC.
2. Connected via SW7. When USB_Function is used, set SW7-7 to OFF and SW7-8 to ON.
3. Connected via SW7. When USB_Host is used, set SW7-9 to OFF and SW7-10 to ON.

7.17 Ethernet System

When running any Ethernet software, do so with the use of a unique MAC address. A sticker indicating the unique MAC address that was assigned by Renesas is affixed to this board (top side) to ensure full compatibility in the case of connection to other Renesas hardware modules.

An EtherCAT ID number is required to execute the EtherCAT slave controller software. Please use SW12 as required.

This board is equipped with four Ethernet PHY devices and Ethernet connectors (CN59, CN44, CN45, and CN1) so that the Ethernet system of the RZ/T2H can be evaluated. Figure 7-21 shows the configuration of the Ethernet system circuit. Table 7-25 to Table 7-28 list the signal connections. Table 7-29 shows initial settings by hardware strapping of the PHY devices.

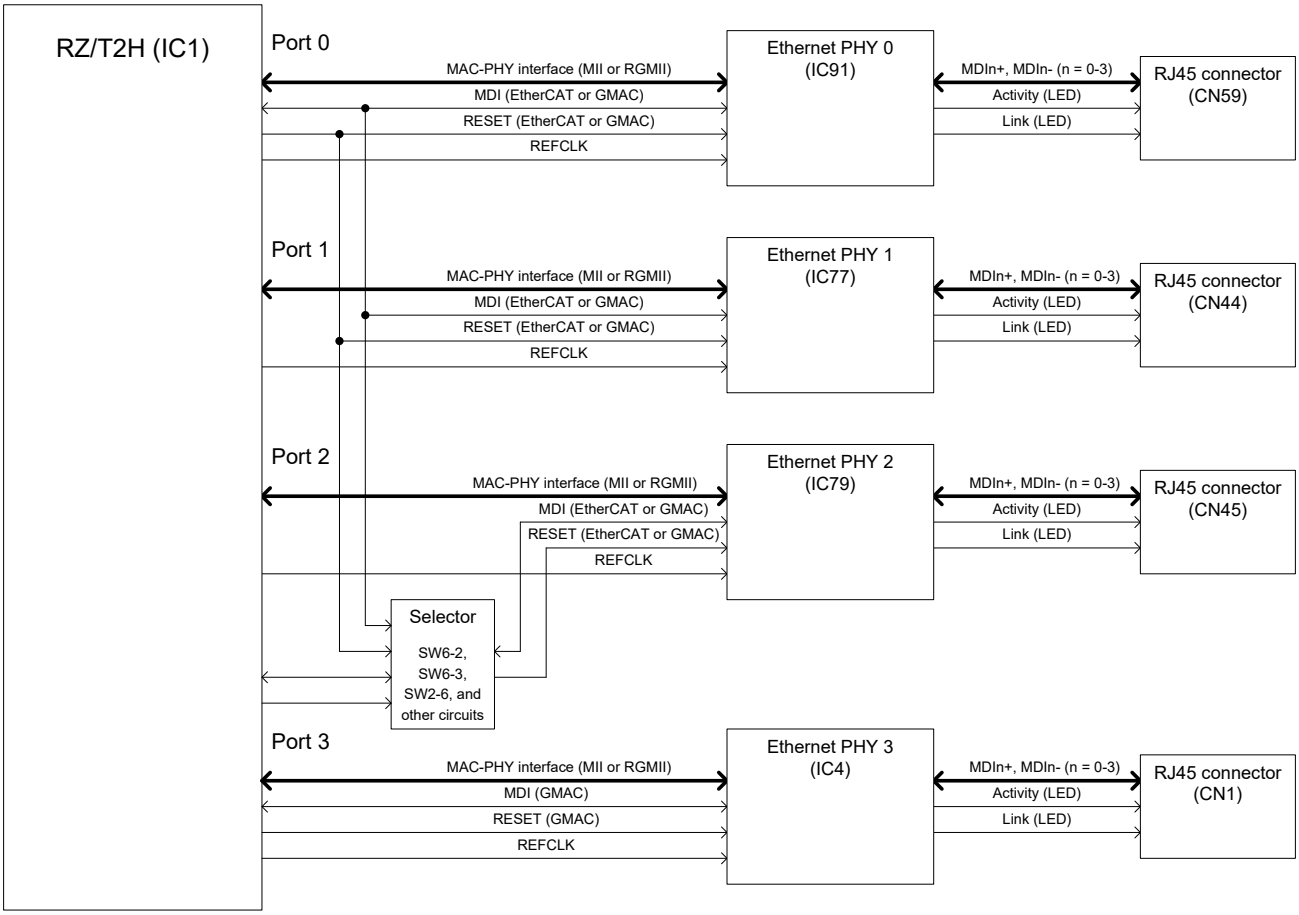


Figure 7-21 Configuration of Ethernet System Circuit

Table 7-25 Signal Connections of Ethernet Port 0 (ETH0)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P20_0_V1833_0_ETH0_TXCLK	Transmit clock	P20_0	A18	—
P20_1_V1833_0_ETH0_TXD0_MDV	Transmit data 0	P20_1	A17	—
P20_2_V1833_0_ETH0_TXD1	Transmit data 1	P20_2	E17	—
P20_3_V1833_0_ETH0_TXD2	Transmit data 2	P20_3	C17	—
P20_4_V1833_0_ETH0_TXD3	Transmit data 3	P20_4	F17	—
P20_5_V1833_0_ETH0_TXEN	Transmit data enable/error	P20_5	B17	—
P22_1_ETH0_TXER	Transmit data error	P22_1	D21	—
P20_6_V1833_0_ETH0_RXCLK	Receive clock	P20_6	C18	—
P20_7_V1833_0_ETH0_RXD0	Receive data 0	P20_7	D18	—
P21_0_V1833_0_ETH0_RXD1	Receive data 1	P21_0	E18	—
P21_1_V1833_0_ETH0_RXD2	Receive data 2	P21_1	G17	—
P21_2_V1833_0_ETH0_RXD3	Receive data 3	P21_2	B19	—
P21_3_V1833_0_ETH0_RXDV	Receive data valid/error/carrier sense	P21_3	A19	—
P22_2_ETH0_RXER	Receive data error	P22_2	E22	—
P22_3_ETH0_CRS	Carrier sense	P22_3	F20	—
P22_4_ETH0_COL	Collision detection	P22_4	E20	—
P21_4_V1833_0_ESC_GMAC_ETHSW_MDC	MDI clock	P21_4	C19	—
P21_5_V1833_0_ESC_GMAC_ETHSW_MDIO	MDI data	P21_5	G16	—
P22_0_V1833_0_IRQ11G	MDI interrupt input	P22_0	E19	—
P21_6_V1833_0_ETH0_LINK	Link status	P21_6	D19	—
P21_7_V1833_0_ETH0_REFCLK	Clock output (25 MHz)	P21_7	D17	—
P11_0_ESC_RESETOUT01#	Reset output	P11_0*	C5	**SW6-2: OFF, SW6-3: ON, SW6-4: OFF, SW6-5: ON**

Note: Connected via SW6.

Table 7-26 Signal Connections of Ethernet Port 1 (ETH1)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P24_5_V1833_1_ETH1_TXCLK	Transmit clock	P24_5	C24	—
P24_6_V1833_1_ETH1_TXD0_MD0	Transmit data 0	P24_6	A23	—
P24_7_V1833_1_ETH1_TXD1_MD1	Transmit data 1	P24_7	C23	—
P25_0_V1833_1_ETH1_TXD2_MD2	Transmit data 2	P25_0	B25	—
P25_1_V1833_1_ETH1_TXD3_MDW0	Transmit data 3	P25_1	A26	—
P25_2_V1833_1_ETH1_TXEN_MDW1	Transmit data enable/error	P25_2	A24	—
P26_6_ETH1_TXER	Transmit data error	P26_6	D26	—
P25_3_V1833_1_ETH1_RXCLK	Receive clock	P25_3	B26	—
P25_4_V1833_1_ETH1_RXD0	Receive data 0	P25_4	E23	—
P25_5_V1833_1_ETH1_RXD1	Receive data 1	P25_5	F23	—
P25_6_V1833_1_ETH1_RXD2	Receive data 2	P25_6	D23	—
P25_7_V1833_1_ETH1_RXD3	Receive data 3	P25_7	E24	—
P26_0_V1833_1_ETH1_RXDV	Receive data valid/error/carrier sense	P26_0	D25	—
P26_7_ETH1_RXER	Receive data error	P26_7	H22	—
P27_0_ETH1_CRS	Carrier sense	P27_0*	G23	**SW4-1: ON, SW4-2: OFF**
P27_1_ETH1_COL	Collision detection	P27_1*	G24	**SW4-3: ON, SW4-4: OFF**
P21_4_V1833_0_ESC_GMAC_ETHSW_MDC	MDI clock	P21_4	C19	—
P21_5_V1833_0_ESC_GMAC_ETHSW_MDIO	MDI data	P21_5	G16	—
P26_5_V1833_1_ETH1_INT#	MDI interrupt input	P26_5	C26	—
P26_3_V1833_1_ETH1_LINK	Link status	P26_3	A25	—
P26_4_ETH1_REFCLK	Clock output (25 MHz)	P26_4	C25	—
P11_0_ESC_RESETOUT01#	Reset output	P11_0*	C5	**SW6-2: OFF, SW6-3: ON, SW6-4: OFF, SW6-5: ON**

Note: Connected via SW4 or SW6.

Table 7-27 Signal Connections of Ethernet Port 2 (ETH2)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P29_1_V1833_2_ETH2_TXCLK	Transmit clock	P29_1*1	J25	**SW2-7: ON**
P29_2_V1833_2_ETH2_TXD0	Transmit data 0	P29_2*1	K23	**SW2-7: ON**
P29_3_V1833_2_ETH2_TXD1	Transmit data 1	P29_3*1	H27	**SW2-7: ON**
P29_4_V1833_2_ETH2_TXD2	Transmit data 2	P29_4*1	L22	**SW2-7: ON**
P29_5_V1833_2_ETH2_TXD3	Transmit data 3	P29_5*1	L23	**SW2-7: ON**
P29_6_V1833_2_ETH2_TXEN	Transmit data enable/error	P29_6*1	J23	**SW2-7: ON**
P31_2_ETH2_TXER	Transmit data error	P31_2*1	N27	**SW2-7: ON**
P29_7_V1833_2_ETH2_RXCLK	Receive clock	P29_7*1	L25	**SW2-7: ON**
P30_0_V1833_2_ETH2_RXD0	Receive data 0	P30_0*1	K27	**SW2-7: ON**
P30_1_V1833_2_ETH2_RXD1	Receive data 1	P30_1*1	K25	**SW2-7: ON**
P30_2_V1833_2_ETH2_RXD2	Receive data 2	P30_2*1	L26	**SW2-7: ON**
P30_3_V1833_2_ETH2_RXD3	Receive data 3	P30_3*1	J27	**SW2-7: ON**
P30_4_V1833_2_ETH2_RXDV	Receive data valid/error/carrier sense	P30_4*1	K24	**SW2-7: ON**
P31_3_ETH2_RXER	Receive data error	P31_3*1	N26	**SW2-7: ON**
P31_4_ETH2_CRS	Carrier sense	P31_4*1	N25	**SW2-7: ON**
P31_5_ETH2_COL	Collision detection	P31_5*1	P26	**SW2-7: ON**
P21_4_P30_5_VCC_ETH2_MDC	MDI clock	P21_4*2	C19	**SW2-6: ON**
		P30_5*2	J22	SW2-6: OFF
P21_5_P30_6_VCC_ETH2_MDIO	MDI data	P21_5*2	G16	**SW2-6: ON**
		P30_6*2	K21	SW2-6: OFF
P31_1_V1833_2_IRQ13	MDI interrupt input	P31_1	J26	—
P30_7_V1833_2_ETH2_LINK	Link status	P30_7	J24	—
P31_0_V1833_2_ETH2_REFCLK	Clock output (25 MHz)	P31_0	L24	—
P11_0_ESC_RESETOUT2#_P17_5_GMAC_RESETOUT2#	Reset output	P11_0*3	C5	**SW6-2: OFF, SW6-3: ON, SW6-4: OFF, SW6-5: ON**
		P17_5*3	A14	SW6-1: OFF, SW6-2: ON, SW6-3: OFF

Notes: 1. Connected via the bus switch IC.
2. Connected via the selector IC.
3. Connected via SW6.

Table 7-28 Signal Connections of Ethernet Port 3 (ETH3)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
P33_2_V1833_3_ETH3_TXCLK	Transmit clock	P33_2*	R24	SW2-8: ON
P33_3_V1833_3_ETH3_TXD0	Transmit data 0	P33_3*	U25	SW2-8: ON
P33_4_V1833_3_ETH3_TXD1	Transmit data 1	P33_4*	U24	SW2-8: ON
P33_5_V1833_3_ETH3_TXD2	Transmit data 2	P33_5*	T25	SW2-8: ON
P33_6_V1833_3_ETH3_TXD3	Transmit data 3	P33_6*	R25	SW2-8: ON
P33_7_V1833_3_ETH3_TXEN	Transmit data enable/error	P33_7*	R26	SW2-8: ON
P34_7_ETH3_TXER	Transmit data error	P34_7*	W23	SW2-8: ON
P34_0_V1833_3_ETH3_RXCLK	Receive clock	P34_0*	V23	SW2-8: ON
P34_1_V1833_3_ETH3_RXD0	Receive data 0	P34_1*	R22	SW2-8: ON
P34_2_V1833_3_ETH3_RXD1	Receive data 1	P34_2*	T23	SW2-8: ON
P34_3_V1833_3_ETH3_RXD2	Receive data 2	P34_3*	U23	SW2-8: ON
P34_4_V1833_3_ETH3_RXD3	Receive data 3	P34_4*	P27	SW2-8: ON
P34_5_V1833_3_ETH3_RXDV	Receive data valid/error/carrier sense	P34_5*	R27	SW2-8: ON
P35_0_ETH3_RXER	Receive data error	P35_0*	V25	SW2-8: ON
P35_1_ETH3_CRS	Carrier sense	P35_1*	T26	SW2-8: ON
P35_2_ETH3_COL	Collision detection	P35_2*	W25	SW2-8: ON
P26_1_V1833_1_GMACMDC_A	MDI clock	P26_1	B23	—
P26_2_V1833_1_GMACMDIO_A	MDI interrupt input	P26_2	B24	—
P27_2_HEADER_IRQ3	Link status	P27_2	G26	—
P34_6_V1833_3_ETH3_REFCLK	Clock output (25 MHz)	P34_6	R23	—
P32_3_MikroBUS_GMAC_RESETOUT3#	Reset output	P32_3	N23	—

Note: Connected via the bus switch IC.

Table 7-29 Initial Settings by Hardware Strapping of the PHY Devices

Items of PHY Initial Settings	Contents of PHY Initial Settings
CLKOUT	Disabled
Managed or unmanaged	Unmanaged mode
CLK delay	2.0 ns
Link advertisement	Default operating mode, 10, 100, or 1000 FDX/HDX, auto-nego is ON
MAC interface	RGMII mode
Selection of GMII/MII or RGMII/RMII	PHY0 (IC91), PHY1 (IC77): GMII or MII mode (when R191 or R155 is Fit) PHY2 (IC79), PHY3 (IC4): RGMII mode (when R23 or R486 is DNF)
PHY address	PHY0 (IC91): 0 PHY1 (IC77): 1 PHY2 (IC79): 2 PHY3 (IC4): 3
Enabling of forced 1000-BT mode	Not set

On the board as shipped, Ethernet ports 0 and 1 are set to the 3.3-V/MII mode (CN37, CN38: 2-3 are short-circuit. R191, R155: Fit.) and Ethernet ports 2 and 3 are set to the 1.8-V/RGMII mode (CN39, CN40: 1-2 are short-circuit. R23, R486: DNF.). When switching the MII and RGMII modes, change the settings with reference to Table 6-13 and Table 6-19.

7.18 PCIe

This board is equipped with a clock driver, power-supply IC, and connectors (CN8 and CN32) for the PCIe so that the PCIe function of the RZ/T2H can be evaluated. Figure 7-22 shows the configuration of the PCIe circuit.

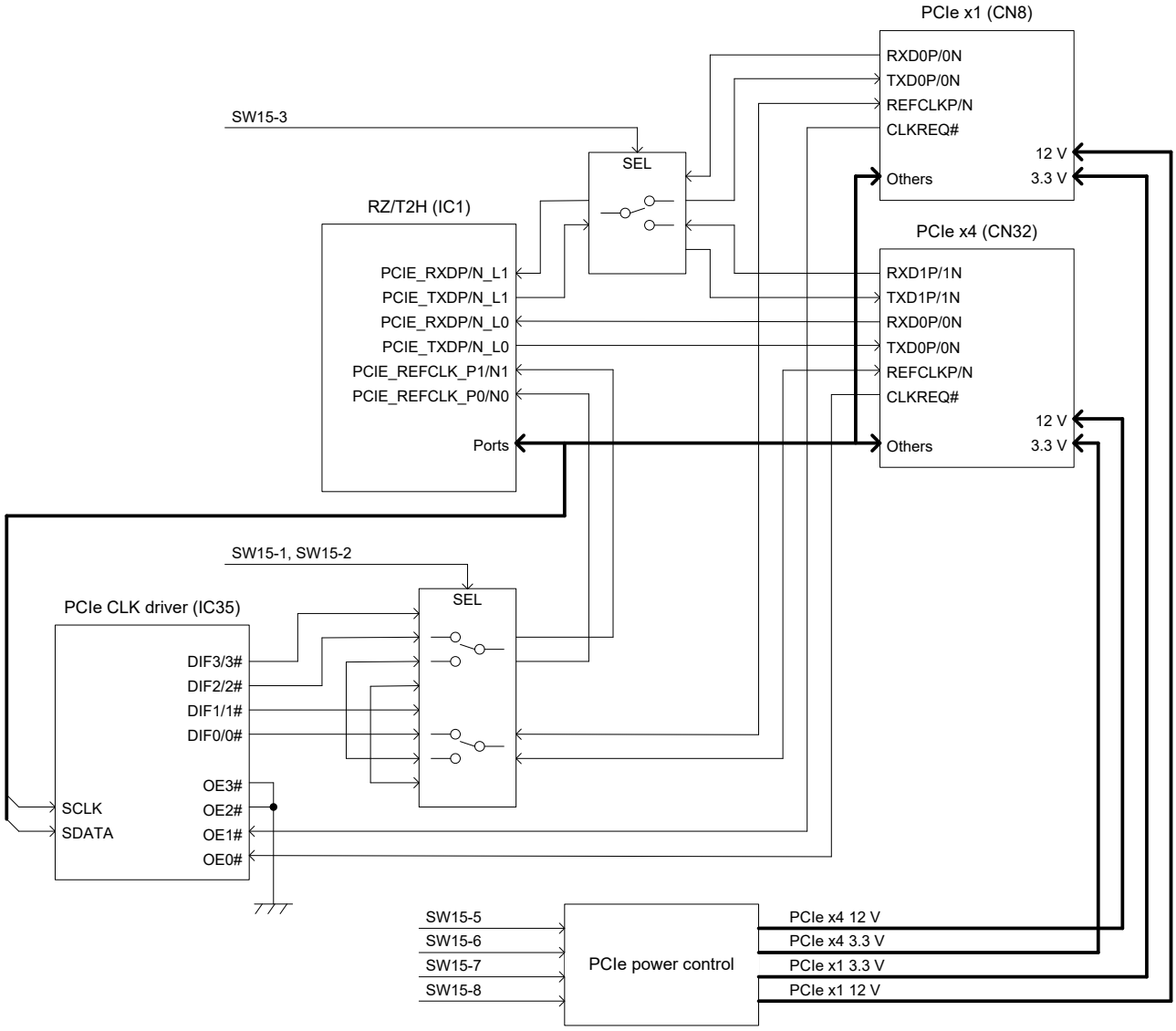


Figure 7-22 Configuration of PCIe Circuit

The configurations of root complex or endpoint, and 2 lanes × 1 port or 1 lane × 2 ports can be selected by setting SW15-1 to SW15-3. In addition, the supply of power to each connector can be controlled by setting SW15-5 to SW15-8. However, since the connection of data signals to the connector is the same for an endpoint setting as for a root complex setting, a crossover cable should be used when performing evaluation. Table 7-30 and Figure 7-23 show the PCIe configurations and associated switch settings.

Table 7-30 PCIe Configurations and Associated Switch Settings (Excluding Signal Function Selection Switches)

Configuration No.	Description of Configuration	Settings of Switches
1	Root complex and 2 lanes × 1 port (CN32)	**SW15-1 and SW15-2: ON, SW15-3: OFF**, SW15-5 and SW15-6: ON, **SW15-7 and SW15-8: OFF**
2	Root complex and 1 lane × 2 ports	**SW15-1 and SW15-2: ON**, SW15-3: ON, SW15-5 to SW15-8: ON
3	Endpoint and 2 lanes × 1 port (CN32)	SW15-1 and SW15-2: OFF, **SW15-3: OFF**, **SW15-5 to SW15-8: OFF**
4	Endpoint and 1 lane × 2 ports	SW15-1 and SW15-2: OFF, SW15-3: ON, **SW15-5 to SW15-8: OFF**
5	Root complex and 1 lane × 1 port (CN32), endpoint and 1 lane × 1 port (CN8)	**SW15-1: ON**, SW15-2: OFF, SW15-3: ON, SW15-5 and SW15-6: ON, **SW15-7 and SW15-8: OFF**
6	Root complex and 1 lane × 1 port (CN8), endpoint and 1 lane × 1 port (CN32)	SW15-1: OFF, **SW15-2: ON**, SW15-3: ON, **SW15-5 and SW15-6: OFF**, SW15-7 and SW15-8: ON

Table 7-31 and Table 7-32 list the signal connections of the PCIe x4 connector (CN32) and PCIe x1 connector (CN8), respectively.

Table 7-31 Signal Connections of PCIe x4 Connector (CN32)

Pin*1	Function Name	Connection	MPU		Settings of Configuration Circuits
			Port	Pin	
A1	PRSNT1#	For a root complex: Fixed to the low level For an endpoint: Connected to PRSNT2#, PRSNT3#	— —	— —	— —
A5	TCK	Pull-down	—	—	—
A6	TDI	Pull-up	—	—	—
A7	TDO	NC	—	—	—
A8	TMS	Pull-up	—	—	—
A11	PERST#	For a root complex: Connected to P33_3 (PCIE_RSTOUT0B) of the RZ/T2H For an endpoint: Input to the reset IC via CN73	P33_3*2 —	U25 —	SW2-8: OFF, **SW15-1: ON** —
A13	REFCLK+	For a root complex: Clock driver output For an endpoint: Input to PCIE_REFCLK_P0 of the RZ/T2H	— —	— —	— —
A14	REFCLK-	For a root complex: Clock driver output For an endpoint: Input to PCIE_REFCLK_N0 of the RZ/T2H	— —	— —	— —
A16	HSIP0	Connected to PCIE_RXDP_L0 of the RZ/T2H	—	AG20	—
A17	HSIN0	Connected to PCIE_RXDN_L0 of the RZ/T2H	—	AF20	—
A21	HSIP1	For 1 port: Connected to PCIE_RXDP_L1 of the RZ/T2H For 2 ports: NC	— —	AG19 —	— —
A22	HSIN1	For 1 port: Connected to PCIE_RXDN_L1 of the RZ/T2H For 2 ports: NC	— —	AF19 —	— —
A21	HSIP1	NC	—	—	—
A22	HSIN1	NC	—	—	—
A25	HSIP2	NC	—	—	—
A26	HSIN2	NC	—	—	—
A29	HSIP3	NC	—	—	—
A30	HSIN3	NC	—	—	—
B5	SMCLK	Pull-up	—	—	—
B6	SMDAT	Pull-up	—	—	—
B9	TRST#	Pull-down	—	—	—
B10	3V3AUX	Connected to the 3.3-V power supply for the PCIe x4 connector (only supplied for a root complex)	—	—	—
B11	WAKE#	Connected to P22_5 of the RZ/T2H	P22_5*3	E21	SW2-1: ON, SW2-2: OFF
B12	CLKREQ#	For a root complex: Clock driver input For an endpoint: Connected to P17_3 (PCIEx4_CLKREQ) of the RZ/T2H	— P17_3	— C13	— SW15-1: OFF
B14	HSOP0	Connected to PCIE_TXDP_L0 of the RZ/T2H	—	AG23	—
B15	HSON0	Connected to PCIE_TXDN_L0 of the RZ/T2H	—	AF23	—

B17	PRSNT2#	For a root complex: Connected to P17_3 of the RZ/T2H (same as B31) For an endpoint: Connected to PRSNT1#	P17_3 —	C13 —	**SW15-1: ON** —
B19	HSOP1	For 1 port: Connected to PCIE_TXDP_L1 of the RZ/T2H For 2 ports: NC	— —	AG22 —	— —
B20	HSON1	For 1 port: Connected to PCIE_TXDN_L1 of the RZ/T2H For 2 ports: NC	— —	AF22 —	— —
B23	HSOP2	NC	—	—	—
B24	HSON2	NC	—	—	—
B27	HSOP3	NC	—	—	—
B28	HSON3	NC	—	—	—
B31	PRSNT3#	For a root complex: Connected to P17_3 of the RZ/T2H (same as B17) For an endpoint: Connected to PRSNT1#	P17_3 —	C13 —	**SW15-1: ON** —

Notes: 1. The pins for power supplies (12 V, 3.3 V, and GROUND) and reserved pins are omitted.
2. Connected via the bus switch IC.
3. Connected via the level shifter IC with an enable function.

Table 7-32 Signal Connections of PCIe x1 Connector (CN8) (Only for a Configuration of 1 Lane × 2 Ports)

Pin*1	Function Name	Connection	MPU		Settings of Configuration Circuits
			Port	Pin	
A1	PRSNT1#	For a root complex: Fixed to the low level For an endpoint: Connected to PRSNT2#	— —	— —	— —
A5	TCK	Pull-down	—	—	—
A6	TDI	Pull-up	—	—	—
A7	TDO	NC	—	—	—
A8	TMS	Pull-up	—	—	—
A11	PERST#	For a root complex: Connected to P33_4 (PCIE_RSTOUT1B) of the RZ/T2H For an endpoint: Input to the reset IC via CN73	P33_4*2 —	U24 —	SW2-8: OFF, **SW15-2: ON** —
A13	REFCLK+	For a root complex: Clock driver output For an endpoint: Input to PCIE_REFCLK_P1 of the RZ/T2H	— —	— AD9	— —
A14	REFCLK-	For a root complex: Clock driver output For an endpoint: Input to PCIE_REFCLK_N1 of the RZ/T2H	— —	— AC9	— —
A16	HSIP0	Connected to PCIE_RXDP_L1 of the RZ/T2H	—	AG19	—
A17	HSIN0	Connected to PCIE_RXDN_L1 of the RZ/T2H	—	AF19	—
B5	SMCLK	Pull-up	—	—	—
B6	SMDAT	Pull-up	—	—	—
B9	TRST#	Pull-down	—	—	—
B10	3V3AUX	Connected to the 3.3-V power supply for the PCIe x1 connector (only supplied for a root complex)	—	—	—
B11	WAKE#	Connected to P16_3 of the RZ/T2H	P16_3*3	B12	SW8-5: OFF, SW8-6: ON
B12	CLKREQ#	For a root complex: Clock driver input For an endpoint: Connected to P05_2 of the RZ/T2H	— P05_2	— AA9	— SW15-2: OFF, **E20: Short-circuit**
B14	HSOP0	Connected to PCIE_TXDP_L1 of the RZ/T2H	—	AG22	—
B15	HSON0	Connected to PCIE_TXDN_L1 of the RZ/T2H	—	AF22	—
B17	PRSNT2#	For a root complex: Connected to P05_2 of the RZ/T2H For an endpoint: Connected to PRSNT1#	P05_2 —	AA9 —	**SW15-2: ON, E20: Short-circuit** —

Notes: 1. The pins for power supplies (12 V, 3.3 V, and GROUND) and reserved pins are omitted.
2. Connected via the bus switch IC.
3. Connected via SW8.

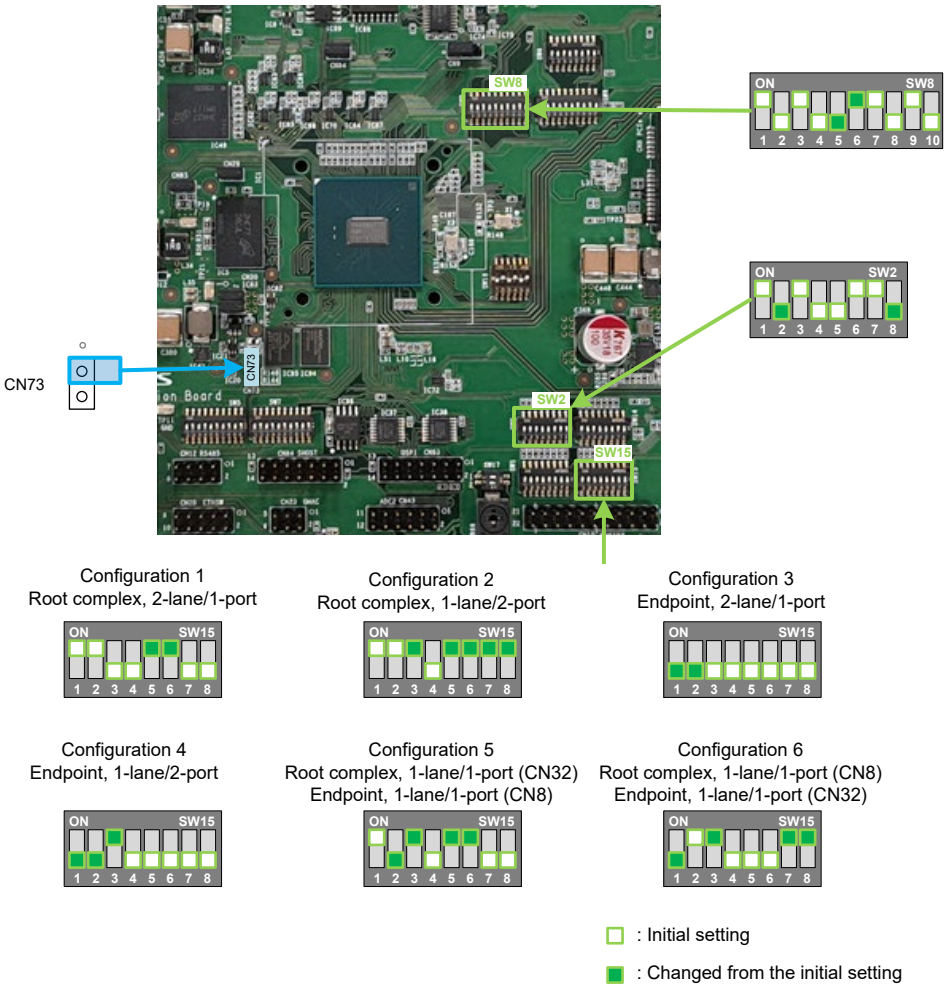


Figure 7-23 Switch Settings When Using PCIe

When endpoint mode is selected, the PCIe reset signal can be included in the system reset factors by short-circuiting CN73. On the board as shipped, CN73 is open-circuit.

7.19 LCD Interface

This board is equipped with an LCD interface connector (CN15). Figure 7-24 shows the configuration of the LCD interface circuit. Table 7-33 lists the signal connections. Figure 7-25 shows the switch settings when using the LCD interface.

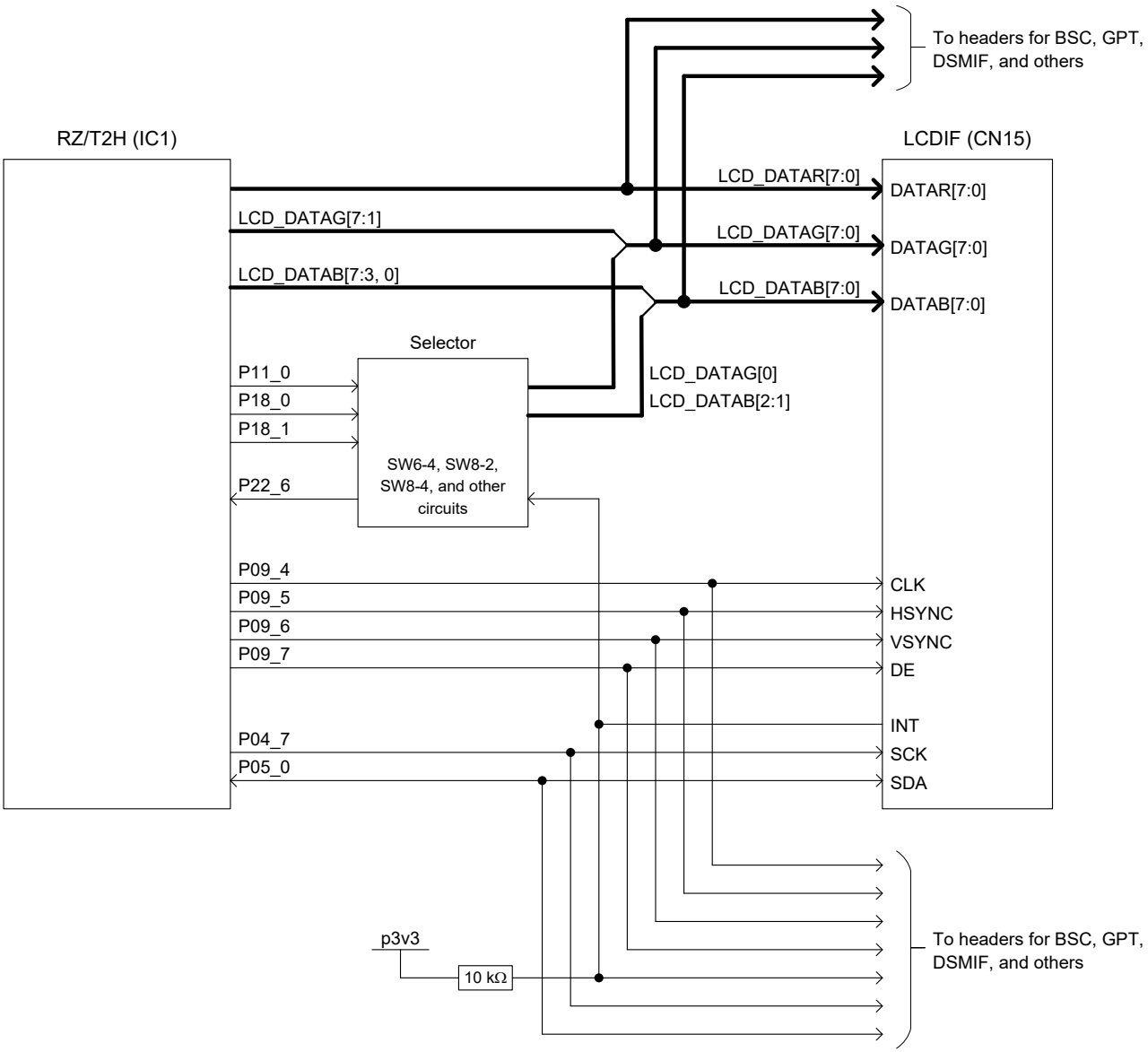


Figure 7-24 Configuration of LCD Interface Circuit

Table 7-33 Signal Connections of LCD Interface Connector (CN15)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P05_0_HEADER_I2C_SDA1_C	P05_0	AA10	—
2	P04_7_HEADER_I2C_SCL1_C	P04_7	AC11	—
3	p5v0	—	—	—
4	P22_6_HEADER_IRQ8_E	P22_6*1	C22	SW2-1: ON, SW2-2: OFF
5	GROUND	—	—	—
6	p1v8	—	—	—
7	p1v8	—	—	—
8	p1v8	—	—	—
9	p1v8	—	—	—
10	GROUND	—	—	—
11	p3v3	—	—	—
12	P09_7_HEADER_BSC_WE0#_LCDC_DE	P09_7	D5	—
13	P09_6_HEADER_BSC_D15_LCDC_VSYNC	P09_6	D3	—
14	P09_5_HEADER_BSC_D14_LCDC_HSYNC	P09_5	C2	—
15	GROUND	—	—	—
16	P09_4_HEADER_BSC_D13_LCDC_CLK	P09_4	D2	—
17	GROUND	—	—	—
18	P18_6_HEADER_BSC_A14_LCDC_DATB7	P18_6	B16	—
19	P18_5_HEADER_BSC_A13_LCDC_DATB6	P18_5	G15	—
20	P18_4_HEADER_BSC_A12_LCDC_DATB5	P18_4	F15	—
21	P18_3_BSC_A11_LCDC_DATB4	P18_3	D13	—
22	P18_2_BSC_A10_LCDC_DATB3	P18_2	B15	—
23	P18_1_BSC_A9_LCDC_DATB2	P18_1*2	E13	SW8-1: OFF, SW8-2: ON
24	P18_0_BSC_A8_LCDC_DATB1	P18_0*2	D15	SW8-3: OFF, SW8-4: ON
25	P17_7_HEADER_BSC_WE3#_AH_LCDC_DATB0	P17_7	E15	—
26	P17_6_HEADER_LCDC_DATG7	P17_6	F13	—
27	P14_6_HEADER_LCDC_DATG6_RS485_DE4	P14_6	B9	—
28	P14_5_HEADER_LCDC_DATG5_BSC_TEND	P14_5	C11	—
29	P14_4_HEADER_LCDC_DATG4_BSC_DACK	P14_4	A9	—
30	P14_3_HEADER_LCDC_DATG3_RS485_TXD4_BSC_DREQ	P14_3	D9	—
31	P14_2_HEADER_BSC_BS#_LCDC_DATG2_RS485_RXD4	P14_2	C10	—
32	P14_1_HEADER_BSC_RD/WR#_LCDC_DATG1	P14_1	C9	—
33	P11_0_BSC_A5_LCDC_DATG0_PMOD2_RXD1	P11_0*3	C5	SW6-3: OFF, SW6-4: ON, SW6-5: OFF
34	P10_7_HEADER_BSC_A4_LCDC_DATR7_IRQ9_B	P10_7	C4	—
35	P10_6_HEADER_BSC_A3_LCDC_DATR6	P10_6	A6	—
36	P10_5_HEADER_BSC_A2_LCDC_DATR5	P10_5	B3	—
37	P10_4_HEADER_BSC_A1_LCDC_DATR4	P10_4	B5	—

38	P10_3_HEADER_BSC_RD#_LCDC_DATR3	P10_3	B1	—
39	P10_2_HEADER_BSC_CS0#_LCDC_DATR2	P10_2	B2	—
40	P10_1_HEADER_BSC_WAIT#_LCDC_DATR1	P10_1	A5	—
41	P10_0_HEADER_BSC_WE1#_LCDC_DATR0	P10_0	D4	—
42	p3v3	—	—	—
43	p3v3	—	—	—
44	GROUND	—	—	—
45	GROUND	—	—	—

Notes: 1. Connected via the level shifter IC with an enable function.
2. Connected via SW8.
3. Connected via SW6.

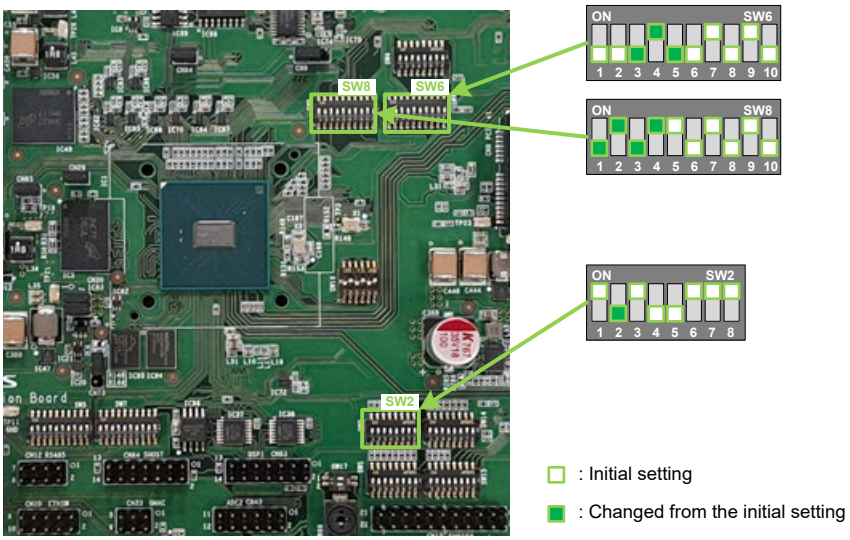


Figure 7-25 Switch Settings When Using the LCD Interface

7.20 Serial Host Interface

This board is equipped with a connector (CN64) for the serial host interface, and the serial host interface of the RZ/T2H can be evaluated by connecting the connector to an external host CPU. Table 7-34 lists the signal connections of the serial host interface connector (CN64). Figure 7-26 shows the switch settings when using the serial host interface.

Table 7-34 Signal Connections of Serial Host Interface Connector (CN64)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	GROUND	—	—	—
2	P27_0_HEADER_BSC_CS5# (HSPI_INT#)	P27_0*1	G23	SW4-1: OFF, SW4-2: ON
3	P27_6_HEADER (HSPI_CKP)	P27_6	G27	—
4	P27_1_HEADER (HSPI_CS#)	P27_1*1	G24	SW4-3: OFF, SW4-4: ON
5	P31_5_HEADER_PMOD1_MOSI (HSPI_IO7)	P31_5*2	P26	SW2-7: OFF
6	P31_4_HEADER_PMOD1_SCK (HSPI_IO6)	P31_4*2	N25	SW2-7: OFF
7	P31_3_HEADER (HSPI_IO5)	P31_3*2	N26	SW2-7: OFF
8	P31_2_HEADER (HSPI_IO4)	P31_2*2	N27	SW2-7: OFF
9	P27_5_HEADER (HSPI_IO3)	P27_5*1	F25	SW4-7: OFF, SW4-8: ON
10	P27_4_HEADER (HSPI_IO2)	P27_4*1	H26	SW4-5: OFF, SW4-6: ON
11	P27_3_HEADER (HSPI_IO1)	P27_3	F27	—
12	P27_2_HEADER_IRQ3 (HSPI_IO0)	P27_2	G26	SW2-8: OFF
13	P02_4_V1833_5_MBX_HINT# (MBX_HINT#)	P02_4	AE12	—
14	p3v3	—	—	—

Notes: 1. Connected via SW4.
2. Connected via the bus switch IC.

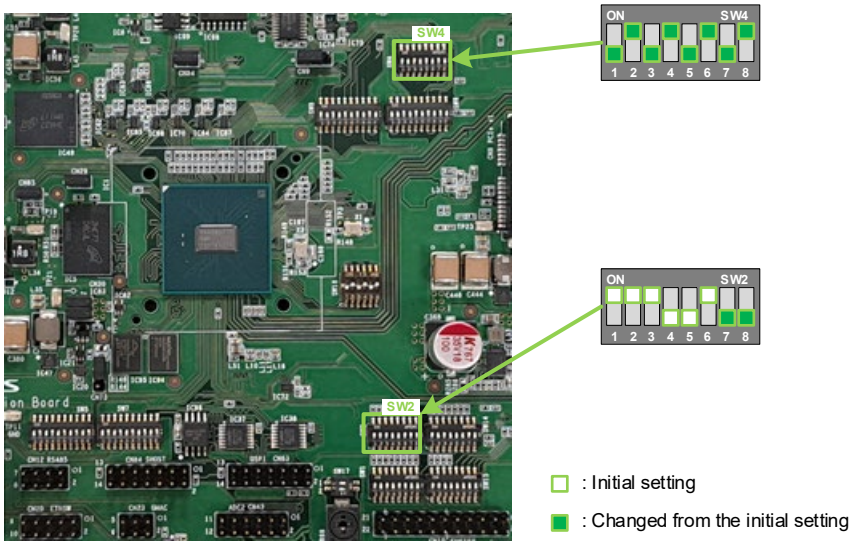


Figure 7-26 Switch Settings When Using the Serial Host Interface

7.21 Pin Headers

This board is equipped with the 2.54-mm pitch pin headers listed in Table 7-35. Table 7-36 to Table 7-52 list the signal connections of the pin headers. Figure 7-27 to Figure 7-32 show the switch settings when using the pin headers.

Table 7-35 List of Pin Headers

Function	Reference	Number of Pins	Description
ENCIF interface	CN2	30 (15 × 2)	For ENCIF0 (units 0 to 5)
	CN3	30 (15 × 2)	For ENCIF1 (units 6 to 11)
	CN10	22 (11 × 2)	For ENCIF2 (units 12 to 15)
DSMIF interface	CN21	30 (15 × 2)	For DSMIF0 (units 0 to 2)
	CN18	30 (15 × 2)	For DSMIF1 (units 3 to 5)
	CN22	30 (15 × 2)	For DSMIF2 (units 6 to 8)
	CN19	10 (5 × 2)	For DSMIF3 (unit 9)
GPT interface	CN24	36 (18 × 2)	For GPT0 (units 0 to 2)
	CN25	36 (18 × 2)	For GPT1 (units 3 to 5)
	CN26	36 (18 × 2)	For GPT2 (units 6 to 8)
ETHSW signal monitoring	CN20	10 (5 × 2)	For monitoring the PTPOUT and TDMAOUT signals
GMAC signal monitoring	CN23	6 (3 × 2)	For monitoring the PTPTRG signals
Bus interface	CN13	40 (20 × 2)	For the address line and others
	CN17	40 (20 × 2)	For the data line and others
ADC	CN41	10 (5 × 2)	For ADC0
	CN42	10 (5 × 2)	For ADC1
	CN43	12 (6 × 2)	For ADC2

Table 7-36 Signal Connections of ENCIF0 (CN2)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	ENCIFCK01	P33_2_V1833_3_HEADER_BSC_A16	P33_2*1	R24	SW2-8: OFF
3	ENCIFCK00	P14_2_HEADER_BSC_BS#_LCDC_DATG2_RS485_RXD4	P14_2	C10	—
4	ENCIFOE01	P33_3_V1833_3_HEADER_BSC_A17_PCIe_RSTOUT0B	P33_3*1	U25	SW2-8: OFF
5	ENCIFOE00	P14_3_HEADER_LCDC_DATG3_RS485_TXD4_BSC_DREQ	P14_3	D9	—
6	ENCIFDO01	P33_4_V1833_3_HEADER_BSC_A18_PCIe_RSTOUT1B	P33_4*1	U24	SW2-8: OFF
7	ENCIFDO00	P14_4_HEADER_LCDC_DATG4_BSC_DACK	P14_4	A9	—
8	ENCIFDI01	P33_5_V1833_3_HEADER_BSC_A19	P33_5*1	T25	SW2-8: OFF
9	ENCIFDI00	P14_5_HEADER_LCDC_DATG5_BSC_TEND	P14_5	C11	—
10	GROUND	GROUND	—	—	—
11	ENCIFCK02	P03_3_HEADER_BSC_D11	P03_3	AB11	—
12	ENCIFCK03	P04_5_HEADER	P04_5	AF9	—
13	ENCIFOE02	P03_4_HEADER_BSC_D12	P03_4	AB10	—
14	ENCIFOE03	P04_6_HEADER	P04_6	AD10	—
15	ENCIFDO02	P03_5_HEADER	P03_5	AC12	—
16	ENCIFDO03	P04_7_HEADER_I2C_SCL1_C	P04_7	AC11	—
17	ENCIFDI02	P03_6_HEADER	P03_6	AG9	—
18	ENCIFDI03	P05_0_HEADER_I2C_SDA1_C	P05_0	AA10	—
19	GROUND	GROUND	—	—	—
20	ENCIFCK05	P12_4_HEADER_BSC_D20_RS485_RXD2	P12_4*2	B6	SW2-1: ON, SW2-2: OFF
21	ENCIFCK04	P00_6_HEADER	P00_6	AG14	—
22	ENCIFOE05	P12_5_HEADER_BSC_D21_RS485_TXD2	P12_5*2	G7	SW2-1: ON, SW2-2: OFF
23	ENCIFOE04	P00_7_HEADER_IRQ5_A	P00_7	AE14	—
24	ENCIFDO05	P12_6_HEADER_BSC_D22	P12_6*2	D6	SW2-1: ON, SW2-2: OFF
25	ENCIFDO04	P01_0_V1833_5_HEADER	P01_0*1	AF13	SW1-6: OFF
26	ENCIFDI05	P12_7_HEADER_BSC_D23	P12_7*2	E6	SW2-1: ON, SW2-2: OFF
27	ENCIFDI04	P01_1_V1833_5_HEADER	P01_1*1	AG12	SW1-6: OFF
28	GROUND	GROUND	—	—	—
29	p5v0	p5v0	—	—	—
30	p3v3	p3v3	—	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via the level shifter IC with an enable function.

Table 7-37 Signal Connections of ENCIF1 (CN3)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	ENCIFCK07	P34_2_V1833_3_HEADER_BSC_A24	P34_2*	T23	SW2-8: OFF
3	ENCIFCK06	P33_6_V1833_3_HEADER_BSC_A20	P33_6*	R25	SW2-8: OFF
4	ENCIFOE07	P34_3_V1833_3_HEADER_BSC_A25	P34_3*	U23	SW2-8: OFF
5	ENCIFOE06	P33_7_V1833_3_HEADER_BSC_A21	P33_7*	R26	SW2-8: OFF
6	ENCIFDO07	P34_4_V1833_3_HEADER_BSC_CS2#	P34_4*	P27	SW2-8: OFF
7	ENCIFDO06	P34_0_V1833_3_HEADER_BSC_A22	P34_0*	V23	SW2-8: OFF
8	ENCIFDI07	P34_5_V1833_3_HEADER_BSC_CS3#	P34_5*	R27	SW2-8: OFF
9	ENCIFDI06	P34_1_V1833_3_HEADER_BSC_A23	P34_1*	R22	SW2-8: OFF
10	GROUND	GROUND	—	—	—
11	ENCIFCK08	P28_5_HEADER	P28_5	D27	—
12	ENCIFCK09	P29_1_V1833_2_HEADER	P29_1*	J25	SW2-7: OFF
13	ENCIFOE08	P28_6_HEADER	P28_6	E27	—
14	ENCIFOE09	P29_2_V1833_2_HEADER	P29_2*	K23	SW2-7: OFF
15	ENCIFDO08	P28_7_HEADER	P28_7	H23	—
16	ENCIFDO09	P29_3_V1833_2_HEADER	P29_3*	H27	SW2-7: OFF
17	ENCIFDI08	P29_0_HEADER	P29_0	H25	—
18	ENCIFDI09	P29_4_V1833_2_HEADER	P29_4*	L22	SW2-7: OFF
19	GROUND	GROUND	—	—	—
20	ENCIFCK11	P30_1_V1833_2_HEADER	P30_1*	K25	SW2-7: OFF
21	ENCIFCK10	P29_5_V1833_2_HEADER	P29_5*	L23	SW2-7: OFF
22	ENCIFOE11	P30_2_V1833_2_HEADER	P30_2*	L26	SW2-7: OFF
23	ENCIFOE10	P29_6_V1833_2_HEADER	P29_6*	J23	SW2-7: OFF
24	ENCIFDO11	P30_3_V1833_2_HEADER	P30_3*	J27	SW2-7: OFF
25	ENCIFDO10	P29_7_V1833_2_HEADER	P29_7*	L25	SW2-7: OFF
26	ENCIFDI11	P30_4_V1833_2_HEADER	P30_4*	K24	SW2-7: OFF
27	ENCIFDI10	P30_0_V1833_2_HEADER	P30_0*	K27	SW2-7: OFF
28	GROUND	GROUND	—	—	—
29	p5v0	p5v0	—	—	—
30	p3v3	p3v3	—	—	—

Note: Connected via the bus switch IC.

Table 7-38 Signal Connections of ENCIF2 (CN10)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	ENCIFCK13	P13_4_HEADER_BSC_D28_RS485_RXD3	P13_4*1	B8	SW1-4: ON
3	ENCIFCK12	P13_0_HEADER_BSC_D24_RS485_DE2	P13_0*2	C7	SW2-1: ON, SW2-2: OFF
4	ENCIFOE13	P13_5_HEADER_BSC_D29_RS485_TXD3	P13_5	B7	—
5	ENCIFOE12	P13_1_HEADER_BSC_D25	P13_1*2	F7	SW2-1: ON, SW2-2: OFF
6	ENCIFDO13	P13_6_HEADER_BSC_D30	P13_6	A8	—
7	ENCIFDO12	P13_2_HEADER_BSC_D26	P13_2*2	F8	SW2-1: ON, SW2-2: OFF
8	ENCIFDI13	P13_7_HEADER_BSC_D31	P13_7	C8	—
9	ENCIFDI12	P13_3_V1833_6_HEADER_BSC_D27	P13_3	F6	—
10	GROUND	GROUND	—	—	—
11	ENCIFCK14	P18_4_HEADER_BSC_A12_LCDC_DATB5	P18_4	F15	—
12	ENCIFCK15	P31_6_HEADER_PMOD1_MISO	P31_6	P25	—
13	ENCIFOE14	P18_5_HEADER_BSC_A13_LCDC_DATB6	P18_5	G15	—
14	ENCIFOE15	P31_7_HEADER_PMOD1_SSL	P31_7	M26	—
15	ENCIFDO14	P18_6_HEADER_BSC_A14_LCDC_DATB7	P18_6	B16	—
16	ENCIFDO15	P32_0_HEADER	P32_0	M25	—
17	ENCIFDI14	P18_7_HEADER_BSC_A15	P18_7	C16	—
18	ENCIFDI15	P32_1_HEADER	P32_1	M23	—
19	NC	NC	—	—	—
20	GROUND	GROUND	—	—	—
21	p5v0	p5v0	—	—	—
22	p3v3	p3v3	—	—	—

Notes: 1. SW1-4 has to be set to ON, and RXD of the RS485 has to be disabled.
2. Connected via the level shifter IC with an enable function.

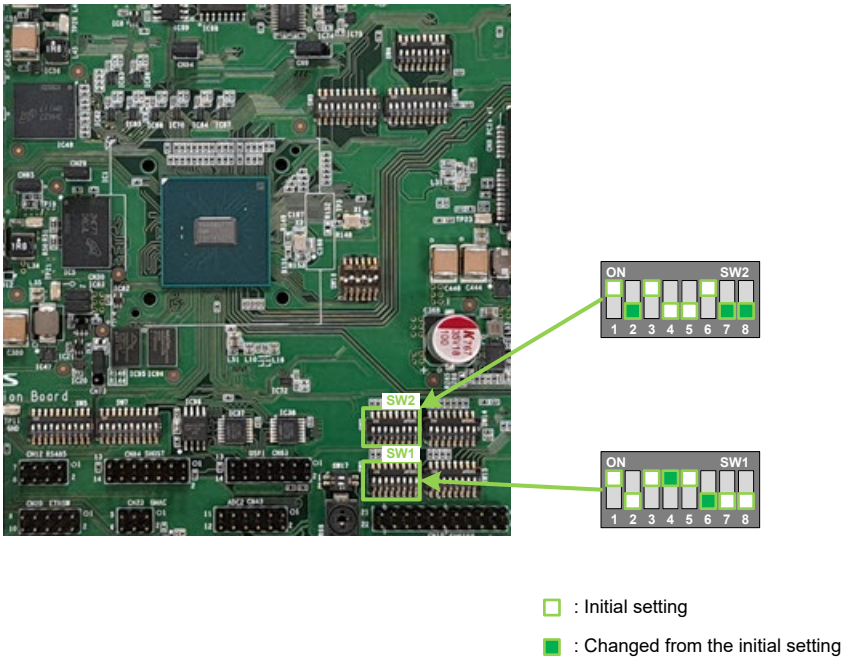


Figure 7-27 Switch Settings When Using ENCIF0 (CN2), ENCIF1 (CN3), and ENCIF2 (CN10)

Table 7-39 Signal Connections of DSMIF0 (CN21)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	p5v0	p5v0	—	—	—
2	p3v3	p3v3	—	—	—
3	MCLK02	P07_5_V1833_4_HEADER	P07_5*1	AG6	SW5-5: ON, SW5-6: OFF
4	MDAT02	P07_6_V1833_4_HEADER	P07_6	AC7	—
5	MCLK01	P07_3_V1833_4_HEADER	P07_3	AE8	—
6	MDAT01	P07_4_V1833_4_HEADER	P07_4	AC8	—
7	MCLK00	P07_1_V1833_4_HEADER	P07_1	AF4	—
8	MDAT00	P07_2_V1833_4_HEADER	P07_2	AG5	—
9	GROUND	GROUND	—	—	—
10	GROUND	GROUND	—	—	—
11	p5v0	p5v0	—	—	—
12	p3v3	p3v3	—	—	—
13	MCLK12	P09_0_HEADER_PMOD2_GPIO0	P09_0	AE1	—
14	MDAT12	P09_1_HEADER_PMOD2_GPIO1	P09_1	AG2	—
15	MCLK11	P08_6_HEADER_SW_SEI	P08_6*2	AD2	SW2-3: OFF, E7: Short-circuit
16	MDAT11	P08_7_HEADER_SW2_IRQ0-D_PMOD2_RST	P08_7	AF2	—
17	MCLK10	P07_7_V1833_4_HEADER	P07_7	AB9	—
18	MDAT10	P08_0_V1833_4_HEADER	P08_0	AD7	—
19	GROUND	GROUND	—	—	—
20	GROUND	GROUND	—	—	—
21	p5v0	p5v0	—	—	—
22	p3v3	p3v3	—	—	—
23	MCLK22	P02_2_V1833_5_HEADER	P02_2*3	AA13	SW1-6: OFF
24	MDAT22	P11_1_HEADER_PMOD2_TXD1	P11_1	C1	—
25	MCLK21	P10_6_HEADER_BSC_A3_LCDC_DATR6	P10_6	A6	—
26	MDAT21	P10_7_HEADER_BSC_A4_LCDC_DATR7_IRQ9_B	P10_7	C4	—
27	MCLK20	P09_2_HEADER	P09_2	AE2	—
28	MDAT20	P09_3_HEADER	P09_3	AF1	—
29	GROUND	GROUND	—	—	—
30	GROUND	GROUND	—	—	—

Notes: 1. Connected via SW5.
2. Connected via the bus switch IC and option link E7.
3. Connected via the bus switch IC.

Table 7-40 Signal Connections of DSMIF1 (CN18)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	p5v0	p5v0	—	—	—
2	p3v3	p3v3	—	—	—
3	MCLK32	P14_7_HEADER	P14_7	A10	—
4	MDAT32	P15_0_HEADER	P15_0	G9	—
5	MCLK31	P11_4_HEADER	P11_4	A2	—
6	MDAT31	P11_5_HEADER	P11_5	B4	—
7	MCLK30	P11_2_HEADER_PMOD2_CTS1#RTS1#_A	P11_2	C3	—
8	MDAT30	P11_3_HEADER_PMOD2_CTS1#_A	P11_3	D1	—
9	GROUND	GROUND	—	—	—
10	GROUND	GROUND	—	—	—
11	p5v0	p5v0	—	—	—
12	p3v3	p3v3	—	—	—
13	MCLK42	P15_5_HEADER	P15_5	E11	—
14	MDAT42	P15_6_HEADER_IRQ1_G	P15_6	D10	—
15	MCLK41	P15_3_HEADER	P15_3	G11	—
16	MDAT41	P15_4_HEADER	P15_4	F9	—
17	MCLK40	P15_1_HEADER	P15_1	E10	—
18	MDAT40	P15_2_HEADER	P15_2	F11	—
19	GROUND	GROUND	—	—	—
20	GROUND	GROUND	—	—	—
21	p5v0	p5v0	—	—	—
22	p3v3	p3v3	—	—	—
23	MCLK52	P19_6_HEADER	P19_6*2	E16	—
24	MDAT52	P19_7_HEADER	P19_7	F16	—
25	MCLK51	P16_1_HEADER	P16_1	B11	—
26	MDAT51	P16_2_HEADER	P16_2	A11	—
27	MCLK50	P15_7_HEADER	P15_7	E9	—
28	MDAT50	P16_0_HEADER	P16_0	D11	—
29	GROUND	GROUND	—	—	—
30	GROUND	GROUND	—	—	—

Table 7-41 Signal Connections of DSMIF2 (CN22)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	p5v0	p5v0	—	—	—
2	p3v3	p3v3	—	—	—
3	MCLK62	P24_1_HEADER	P24_1	D22	—
4	MDAT62	P24_2_HEADER	P24_2	F21	—
5	MCLK61	P23_7_HEADER	P23_7	G19	—
6	MDAT61	P24_0_HEADER	P24_0	F19	—
7	MCLK60	P23_5_HEADER	P23_5*1	C21	SW7-5: ON, SW7-6: OFF
8	MDAT60	P23_6_HEADER	P23_6	B21	—
9	GROUND	GROUND	—	—	—
10	GROUND	GROUND	—	—	—
11	p5v0	p5v0	—	—	—
12	p3v3	p3v3	—	—	—
13	MCLK72	P10_0_HEADER_BSC_WE1#_LCDC_DATR0	P10_0	D4	—
14	MDAT72	P10_1_HEADER_BSC_WAIT#_LCDC_DATR1	P10_1	A5	—
15	MCLK71	P09_6_HEADER_BSC_D15_LCDC_VSYNC	P09_6	D3	—
16	MDAT71	P09_7_HEADER_BSC_WE0#_LCDC_DE	P09_7	D5	—
17	MCLK70	P24_3_HEADER	P24_3*1	B20	SW7-3: ON, SW7-4: OFF
18	MDAT70	P24_4_HEADER	P24_4*1	G22	SW7-1: ON, SW7-2: OFF
19	GROUND	GROUND	—	—	—
20	GROUND	GROUND	—	—	—
21	p5v0	p5v0	—	—	—
22	p3v3	p3v3	—	—	—
23	MCLK82	P33_0_HEADER	P33_0	P24	—
24	MDAT82	P33_1_HEADER	P33_1	P23	—
25	MCLK81	P31_4_HEADER_PMOD1_SCK	P31_4*2	N25	SW2-7: OFF
26	MDAT81	P31_5_HEADER_PMOD1_MOSI	P31_5	P26	—
27	MCLK80	P31_2_HEADER	P31_2*2	N27	SW2-7: OFF
28	MDAT80	P31_3_HEADER	P31_3*2	N26	SW2-7: OFF
29	GROUND	GROUND	—	—	—
30	GROUND	GROUND	—	—	—

Notes: 1. Connected via SW7.
2. Connected via the bus switch IC.

Table 7-42 Signal Connections of DSMIF3 (CN19)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	p5v0	p5v0	—	—	—
2	p3v3	p3v3	—	—	—
3	MCLK92	P35_5_HEADER	P35_5*	V24	SW1-3: OFF,
4	MDAT92	P35_6_HEADER	P35_6*	U22	SW1-3: OFF,
5	MCLK91	P35_3_HEADER	P35_3*	V22	SW1-3: OFF,
6	MDAT91	P35_4_HEADER	P35_4*	W24	SW1-3: OFF,
7	MCLK90	P35_1_HEADER	P35_1*	T26	SW2-8: OFF,
8	MDAT90	P35_2_HEADER	P35_2*	W25	SW2-8: OFF,
9	GROUND	GROUND	—	—	—
10	GROUND	GROUND	—	—	—

Note: Connected via the bus switch IC.

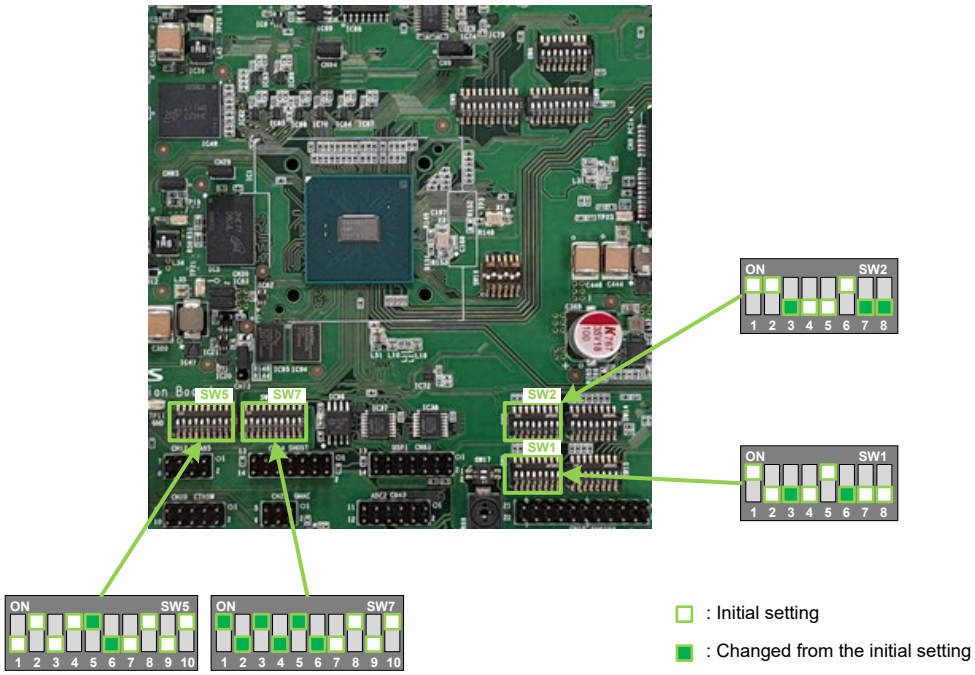


Figure 7-28 Switch Settings When Using DSMIF0 (CN21), DSMIF1 (CN18), DSMIF2 (CN22), and DSMIF3 (CN19)

Table 7-43 Signal Connections of GPT0 (CN24)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	GROUND	GROUND	—	—	—
3	GTIOC00_0A	P00_0_HEADER_BSC_D0	P00_0*1	AE15	SW1-5: OFF
4	GTIOC00_0B	P00_1_HEADER_BSC_D1	P00_1*1	AD15	SW1-5: OFF
5	GTIOC00_1A	P00_2_HEADER_BSC_D2	P00_2*1	AC15	SW1-5: OFF
6	GTIOC00_1B	P00_3_HEADER_BSC_D3_SW1_IRQ2_A_ADTRG1	P00_3	AG15	—
7	GTIOC00_2A	P00_4_HEADER_BSC_D4	P00_4	AF15	—
8	GTIOC00_2B	P00_5_HEADER	P00_5	AB15	—
9	GTIOC00_3A	P00_6_HEADER	P00_6	AG14	—
10	GTIOC00_3B	P00_7_HEADER_IRQ5_A	P00_7	AE14	—
11	GTIOC00_4A	P01_0_V1833_5_HEADER	P01_0*1	AF13	SW1-6: OFF
12	GTIOC00_4B	P01_1_V1833_5_HEADER	P01_1*1	AG12	SW1-6: OFF
13	GROUND	GROUND	—	—	—
14	GROUND	GROUND	—	—	—
15	GTIOC01_0A	P01_2_V1833_5_HEADER	P01_2*1	AD14	SW1-6: OFF
16	GTIOC01_0B	P01_3_V1833_5_HEADER	P01_3	AB14	—
17	GTIOC01_1A	P32_4_HEADER_MikroBUS_MOSI	P32_4	N22	—
18	GTIOC01_1B	P32_5_HEADER_MikroBUS_MISO	P32_5	M27	—
19	GTIOC01_2A	P32_6_HEADER_MikroBUS_CS	P32_6	L27	—
20	GTIOC01_2B	P32_7_HEADER	P32_7	N24	—
21	GTIOC01_3A	P02_0_V1833_5_HEADER	P02_0*1	AC14	SW1-6: OFF
22	GTIOC01_3B	P02_1_V1833_5_HEADER	P02_1*1	AB13	SW1-6: OFF
23	GTIOC01_4A	P02_2_V1833_5_HEADER	P02_2*1	AA13	SW1-6: OFF
24	GTIOC01_4B	P02_3_V1833_5_HEADER	P02_3*1	AF12	SW1-6: OFF
25	GROUND	GROUND	—	—	—
26	GROUND	GROUND	—	—	—
27	GTIOC02_0A	P02_5_HEADER_BSC_D5	P02_5*2	AD11	SW2-1: ON, SW2-2: OFF
28	GTIOC02_0B	P02_6_HEADER_BSC_D6	P02_6*2	AD9	SW2-1: ON, SW2-2: OFF
29	GTIOC02_1A	P02_7_HEADER_BSC_D7	P02_7	AE9	—
30	GTIOC02_1B	P03_0_HEADER_BSC_D8	P03_0	AE10	—
31	GTIOC02_2A	P03_1_HEADER_BSC_D9	P03_1	AC10	—
32	GTIOC02_2B	P03_2_HEADER_BSC_D10	P03_2	AC9	—
33	GTIOC02_3A	P13_0_HEADER_BSC_D24_RS485_DE2	P13_0*2	C7	SW2-1: ON, SW2-2: OFF
34	GTIOC02_3B	P13_1_HEADER_BSC_D25	P13_1*2	F7	SW2-1: ON, SW2-2: OFF
35	GTIOC02_4A	P03_5_HEADER	P03_5	AC12	—
36	GTIOC02_4B	P03_6_HEADER	P03_6	AG9	—

Notes: 1. Connected via the bus switch IC.
2. Connected via the level shifter IC with an enable function.

Table 7-44 Signal Connections of GPT1 (CN25)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	GROUND	GROUND	—	—	—
3	GTIOC03_0A	P03_7_HEADER	P03_7	AB12	—
4	GTIOC03_0B	P04_0_HEADER_BSC_IRQOUT#	P04_0	AE11	—
5	GTIOC03_1A	P04_1_HEADER_MikroBUS_RST	P04_1	AF11	—
6	GTIOC03_1B	P04_2_HEADER_MikroBUS_PWM	P04_2	AA12	—
7	GTIOC03_2A	P04_3_HEADER_PMOD1_RST	P04_3	AG10	—
8	GTIOC03_2B	P04_4_HEADER_PMOD1_GPIO0	P04_4	AG11	—
9	GTIOC03_3A	P04_5_HEADER	P04_5	AF9	—
10	GTIOC03_3B	P04_6_HEADER	P04_6	AD10	—
11	GTIOC03_4A	P04_7_HEADER_I2C_SCL1_C	P04_7	AC11	—
12	GTIOC03_4B	P05_0_HEADER_I2C_SDA1_C	P05_0	AA10	—
13	GROUND	GROUND	—	—	—
14	GROUND	GROUND	—	—	—
15	GTIOC04_0A	P09_4_HEADER_BSC_D13_LCDC_CLK	P09_4	D2	—
16	GTIOC04_0B	P09_5_HEADER_BSC_D14_LCDC_HSYNC	P09_5	C2	—
17	GTIOC04_1A	P01_4_V1833_5_HEADER	P01_4*1	AG13	SW1-6: OFF
18	GTIOC04_1B	P01_5_V1833_5_HEADER	P01_5*1	AE13	SW1-6: OFF
19	GTIOC04_2A	P01_6_V1833_5_HEADER	P01_6*1	AD13	SW1-6: OFF
20	GTIOC04_2B	P01_7_V1833_5_HEADER	P01_7*1	AC13	SW1-6: OFF
21	GTIOC04_3A	P10_2_HEADER_BSC_CS0#_LCDC_DATR2	P10_2	B2	—
22	GTIOC04_3B	P10_3_HEADER_BSC_RD#_LCDC_DATR3	P10_3	B1	—
23	GTIOC04_4A	P10_4_HEADER_BSC_A1_LCDC_DATR4	P10_4	B5	—
24	GTIOC04_4B	P10_5_HEADER_BSC_A2_LCDC_DATR5	P10_5	B3	—
25	GROUND	GROUND	—	—	—
26	GROUND	GROUND	—	—	—
27	GTIOC05_0A	P11_6_HEADER_PMOD1_GPIO1	P11_6	A3	—
28	GTIOC05_0B	P11_7_HEADER	P11_7	A4	—
29	GTIOC05_1A	P12_0_HEADER_BSC_D16	P12_0*2	D7	SW2-1: ON, SW2-2: OFF
30	GTIOC05_1B	P12_1_HEADER_BSC_D17	P12_1*2	G8	SW2-1: ON, SW2-2: OFF
31	GTIOC05_2A	P12_2_HEADER_BSC_D18	P12_2*2	E8	SW2-1: ON, SW2-2: OFF
32	GTIOC05_2B	P12_3_HEADER_BSC_D19	P12_3*2	E7	SW2-1: ON, SW2-2: OFF
33	GTIOC05_3A	P12_4_HEADER_BSC_D20_RS485_RXD2	P12_4*2	B6	SW2-1: ON, SW2-2: OFF
34	GTIOC05_3B	P12_5_HEADER_BSC_D21_RS485_TXD2	P12_5*2	G7	SW2-1: ON, SW2-2: OFF
35	GTIOC05_4A	P12_6_HEADER_BSC_D22	P12_6*2	D6	SW2-1: ON, SW2-2: OFF
36	GTIOC05_4B	P12_7_HEADER_BSC_D23	P12_7*2	E6	SW2-1: ON, SW2-2: OFF

Notes: 1. Connected via the bus switch IC.
2. Connected via the level shifter IC with an enable function.

Table 7-45 Signal Connections of GPT2 (CN26)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GROUND	GROUND	—	—	—
2	GROUND	GROUND	—	—	—
3	GTIOC06_0A	P22_7_HEADER	P22_7*	G21	SW5-9: ON, SW5-10: OFF
4	GTIOC06_0B	P23_0_HEADER	P23_0*	G20	SW5-7: ON, SW5-8: OFF
5	GTIOC06_1A	P23_1_HEADER	P23_1*	A20	SW8-9: OFF, SW8-10: ON
6	GTIOC06_1B	P23_2_HEADER	P23_2	A22	—
7	GTIOC06_2A	P23_3_HEADER	P23_3*	A21	SW6-7: OFF, SW6-8: ON
8	GTIOC06_2B	P23_4_HEADER	P23_4*	C20	SW6-9: OFF, SW6-10: ON
9	GTIOC06_3A	P13_5_HEADER_BSC_D29_RS485_TXD3	P13_5	B7	—
10	GTIOC06_3B	P13_6_HEADER_BSC_D30	P13_6	A8	—
11	GTIOC06_4A	P13_7_HEADER_BSC_D31	P13_7	C8	—
12	GTIOC06_4B	P14_0_HEADER_BSC_A0_RS485_DE3	P14_0	A7	—
13	GROUND	GROUND	—	—	—
14	GROUND	GROUND	—	—	—
15	GTIOC07_0A	P19_0_HEADER	P19_0	D14	—
16	GTIOC07_0B	P19_1_HEADER	P19_1	E14	—
17	GTIOC07_1A	P19_2_HEADER	P19_2	C14	—
18	GTIOC07_1B	P19_3_HEADER	P19_3	C15	—
19	GTIOC07_2A	P19_4_HEADER	P19_4	A15	—
20	GTIOC07_2B	P19_5_HEADER	P19_5	A16	—
21	GTIOC07_3A	P18_4_HEADER_BSC_A12_LCDC_DATB5	P18_4	F15	—
22	GTIOC07_3B	P18_5_HEADER_BSC_A13_LCDC_DATB6	P18_5	G15	—
23	GTIOC07_4A	P18_6_HEADER_BSC_A14_LCDC_DATB7	P18_6	B16	—
24	GTIOC07_4B	P18_7_HEADER_BSC_A15	P18_7	C16	—
25	GROUND	GROUND	—	—	—
26	GROUND	GROUND	—	—	—
27	GTIOC08_0A	P27_7_HEADER	P27_7	C27	—
28	GTIOC08_0B	P28_0_HEADER	P28_0	F24	—
29	GTIOC08_1A	P28_1_HEADER	P28_1	E26	—
30	GTIOC08_1B	P28_2_HEADER	P28_2	G25	—
31	GTIOC08_2A	P28_3_HEADER	P28_3	B27	—
32	GTIOC08_2B	P28_4_HEADER	P28_4	E25	—
33	GTIOC08_3A	P27_3_HEADER	P27_3	F27	—
34	GTIOC08_3B	P27_4_HEADER	P27_4*	H26	SW4-5: OFF, SW4-6: ON
35	GTIOC08_4A	P27_5_HEADER	P27_5*	F25	SW4-7: OFF, SW4-8: ON
36	GTIOC08_4B	P27_6_HEADER	P27_6	G27	—

Note: Connected via SW4, SW5, SW6, or SW8.

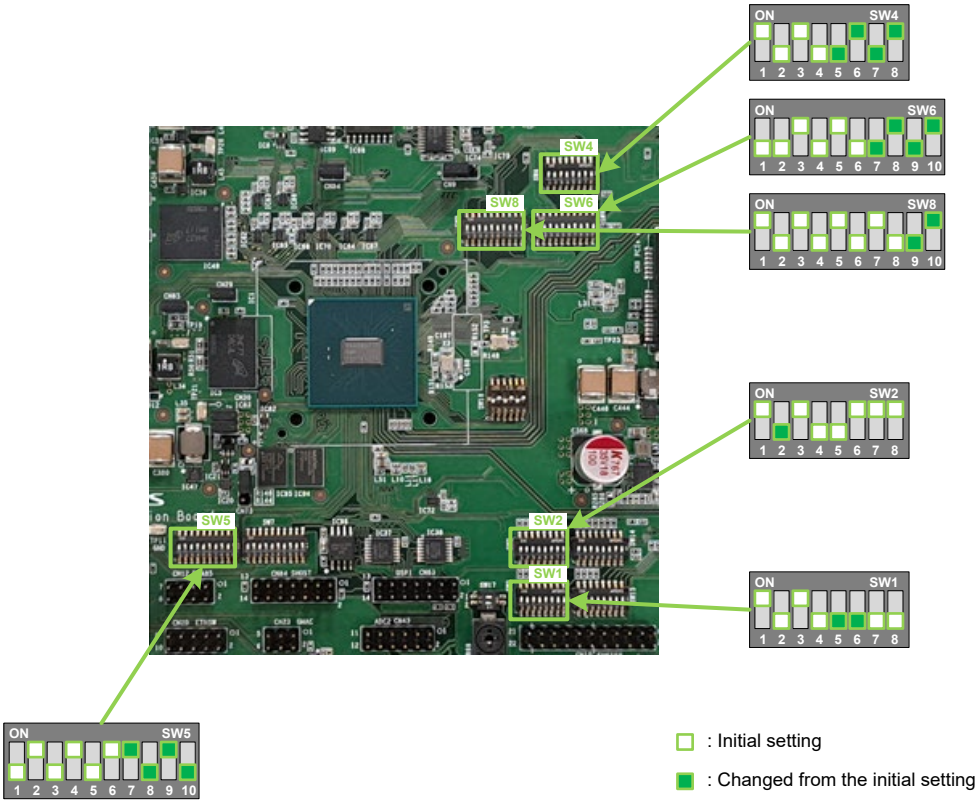


Figure 7-29 Switch Settings When Using GPT0 (CN24), GPT1 (CN25), and GPT2 (CN26)

Table 7-46 Signal Connections of ETHSW (CN20)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	ETHSW_PTPOUT0	P17_6_HEADER_LCDC_DATG7	P17_6	F13	—
2	GROUND	GROUND	—	—	—
3	ETHSW_PTPOUT1	P17_7_HEADER_BSC_WE3#_AH_LCDC_DATB0	P17_7	E15	—
4	ETHSW_TDMAOUT0	P27_7_HEADER	P27_7	C27	—
5	ETHSW_PTPOUT2	P14_0_HEADER_BSC_A0_RS485_DE3	P14_0	A7	—
6	ETHSW_TDMAOUT1	P28_0_HEADER	P28_0	F24	—
7	ETHSW_PTPOUT3	P18_7_HEADER_BSC_A15	P18_7	C16	—
8	ETHSW_TDMAOUT2	P28_1_HEADER	P28_1	E26	—
9	GROUND	GROUND	—	—	—
10	ETHSW_TDMAOUT3	P28_2_HEADER	P28_2	G25	—

Table 7-47 Signal Connections of GMAC (CN23)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	GMAC0_PTPTRG0	P22_5_HEADER_IRQ7_E_PCIEx4_WAKE_GPIO	P22_5*	E21	SW2-1: ON, SW2-2: OFF
2	GMAC0_PTPTRG1	P22_6_HEADER_IRQ8_E	P22_6*	C22	SW2-1: ON, SW2-2: OFF
3	GMAC1_PTPTRG0	P27_2_HEADER_IRQ3	P27_2	G26	SW2-8: OFF
4	GMAC1_PTPTRG1	P27_3_HEADER	P27_3	F27	—
5	GMAC2_PTPTRG0	P31_6_HEADER_PMOD1_MISO	P31_6	P25	—
6	GMAC2_PTPTRG1	P31_7_HEADER_PMOD1_SSL	P31_7	M26	—

Note: Connected via the level shifter IC with an enable function.

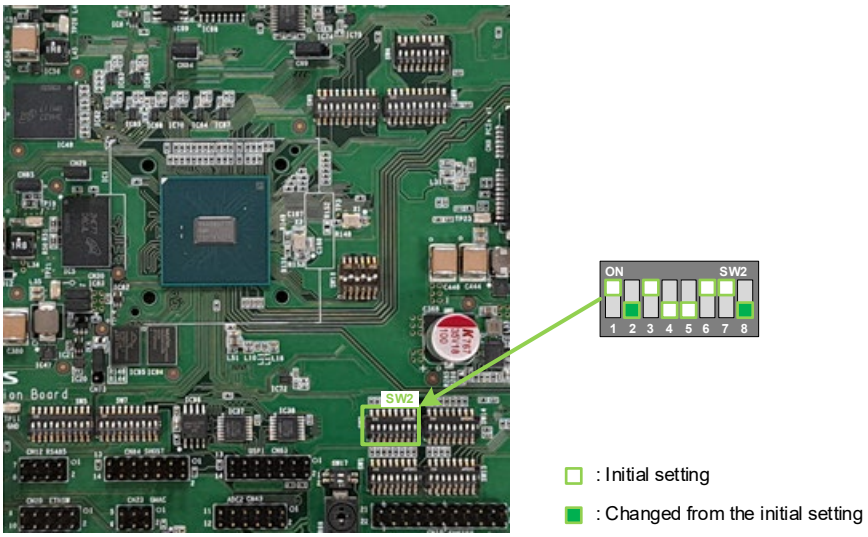


Figure 7-30 Switch Settings When Using GMAC (CN23)

Table 7-48 Signal Connections of BSC1 (CN13)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P14_0_HEADER_BSC_A0_RS485_DE3	P14_0	A7	—
2	p3v3	—	—	—
3	P10_4_HEADER_BSC_A1_LCDC_DATR4	P10_4	B5	—
4	P33_2_V1833_3_HEADER_BSC_A16	P33_2*1	R24	SW2-8: OFF
5	P10_5_HEADER_BSC_A2_LCDC_DATR5	P10_5	B3	—
6	P33_3_V1833_3_HEADER_BSC_A17_PCIe_RSTOUT0B	P33_3*1	U25	SW2-8: OFF
7	P10_6_HEADER_BSC_A3_LCDC_DATR6	P10_6	A6	—
8	P33_4_V1833_3_HEADER_BSC_A18_PCIe_RSTOUT1B	P33_4*1	U24	SW2-8: OFF
9	P10_7_HEADER_BSC_A4_LCDC_DATR7_IRQ9_B	P10_7	C4	—
10	P33_5_V1833_3_HEADER_BSC_A19	P33_5*1	T25	SW2-8: OFF
11	GROUND	—	—	—
12	P33_6_V1833_3_HEADER_BSC_A20	P33_6*1	R25	SW2-8: OFF
13	P11_0_BSC_A5_LCDC_DATG0_PMOD2_RXD1	P11_0*2	C5	SW6-3: OFF, SW6-4: ON, SW6-5: OFF
14	P33_7_V1833_3_HEADER_BSC_A21	P33_7*1	R26	SW2-8: OFF
15	P17_4_BSC_A6	P17_4*1	G13	SW2-3: OFF
16	P34_0_V1833_3_HEADER_BSC_A22	P34_0*1	V23	SW2-8: OFF
17	P17_5_BSC_A7	P17_5*2	A14	SW6-1: ON, SW6-2: OFF
18	P34_1_V1833_3_HEADER_BSC_A23	P34_1*1	R22	SW2-8: OFF
19	P18_0_BSC_A8_LCDC_DATB1	P18_0*2	D15	SW8-3: OFF, SW8-4: ON
20	P27_0_HEADER_BSC_CS5#	P27_0	G23	SW4-1: OFF, SW4-2: ON
21	P18_1_BSC_A9_LCDC_DATB2	P18_1*2	E13	SW8-1: OFF, SW8-2: ON
22	P34_2_V1833_3_HEADER_BSC_A24	P34_2*1	T23	SW2-8: OFF
23	P18_2_BSC_A10_LCDC_DATB3	P18_2	B15	—
24	P34_3_V1833_3_HEADER_BSC_A25	P34_3*1	U23	SW2-8: OFF
25	P18_3_BSC_A11_LCDC_DATB4	P18_3	D13	—
26	P14_4_HEADER_LCDC_DATG4_BSC_DACK	P14_4	A9	—
27	P18_4_HEADER_BSC_A12_LCDC_DATB5	P18_4	F15	—
28	P14_3_HEADER_LCDC_DATG3_RS485_TXD4_BSC_DREQ	P14_3	D9	—
29	GROUND	—	—	—
30	P14_2_HEADER_BSC_BS#_LCDC_DATG2_RS485_RXD4	P14_2	C10	—
31	P18_5_HEADER_BSC_A13_LCDC_DATB6	P18_5	G15	—
32	P10_2_HEADER_BSC_CS0#_LCDC_DATR2	P10_2	B2	—
33	P18_6_HEADER_BSC_A14_LCDC_DATB7	P18_6	B16	—
34	P34_4_V1833_3_HEADER_BSC_CS2#	P34_4*1	P27	SW2-8: OFF
35	P18_7_HEADER_BSC_A15	P18_7	C16	—
36	P34_5_V1833_3_HEADER_BSC_CS3#	P34_5*1	R27	SW2-8: OFF
37	P04_0_HEADER_BSC_IRQOUT#	P04_0	AE11	—
38	P14_1_HEADER_BSC_RD/WR#_LCDC_DATG1	P14_1	C9	—
39	P10_3_HEADER_BSC_RD#_LCDC_DATR3	P10_3	B1	—
40	P14_5_HEADER_LCDC_DATG5_BSC_TEND	P14_5	C11	—

Notes: 1. Connected via the bus switch IC.
2. Connected via SW6 or SW8.

Table 7-49 Signal Connections of BSC2 (CN17)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	P00_0_HEADER_BSC_D0	P00_0*1	AE15	SW1-5: OFF
2	P08_6_HEADER_SW_SEI_BSC_CKIO	P08_6*1	AD2	SW2-3: OFF
3	P00_1_HEADER_BSC_D1	P00_1*1	AD15	SW1-5: OFF
4	P12_2_HEADER_BSC_D18	P12_2*2	E8	SW2-1: ON, SW2-2: OFF
5	P00_2_HEADER_BSC_D2	P00_2*1	AC15	SW1-5: OFF
6	P12_3_HEADER_BSC_D19	P12_3*2	E7	SW2-1: ON, SW2-2: OFF
7	P00_3_HEADER_BSC_D3_SW1_IRQ2_A_ADTRG1	P00_3	AG15	—
8	P12_4_HEADER_BSC_D20_RS485_RXD2	P12_4*2	B6	SW2-1: ON, SW2-2: OFF
9	P00_4_HEADER_BSC_D4	P00_4	AF15	—
10	P12_5_HEADER_BSC_D21_RS485_TXD2	P12_5*2	G7	SW2-1: ON, SW2-2: OFF
11	GROUND	—	—	—
12	P12_6_HEADER_BSC_D22	P12_6*2	D6	SW2-1: ON, SW2-2: OFF
13	P02_5_HEADER_BSC_D5	P02_5*2	AD11	SW2-1: ON, SW2-2: OFF
14	P12_7_HEADER_BSC_D23	P12_7*2	E6	SW2-1: ON, SW2-2: OFF
15	P02_6_HEADER_BSC_D6	P02_6*2	AD9	SW2-1: ON, SW2-2: OFF
16	P13_0_HEADER_BSC_D24_RS485_DE2	P13_0*2	C7	SW2-1: ON, SW2-2: OFF
17	P02_7_HEADER_BSC_D7	P02_7	AE9	—
18	P13_1_HEADER_BSC_D25	P13_1*2	F7	SW2-1: ON, SW2-2: OFF
19	P03_0_HEADER_BSC_D8	P03_0	AE10	—
20	P17_6_HEADER_BSC_WE2#_LCDC_DATG7	P17_6	F13	—
21	P03_1_HEADER_BSC_D9	P03_1	AC10	—
22	P13_2_HEADER_BSC_D26	P13_2*2	F8	SW2-1: ON, SW2-2: OFF
23	P03_2_HEADER_BSC_D10	P03_2	AC9	—
24	P13_3_V1833_6_HEADER_BSC_D27	P13_3	F6	—
25	P03_3_HEADER_BSC_D11	P03_3	AB11	—
26	P13_4_HEADER_BSC_D28_RS485_RXD3	P13_4*3	B8	SW1-4: ON
27	P03_4_HEADER_BSC_D12	P03_4	AB10	—
28	P13_5_HEADER_BSC_D29_RS485_TXD3	P13_5	B7	—
29	GROUND	—	—	—
30	P13_6_HEADER_BSC_D30	P13_6	A8	—
31	P09_4_HEADER_BSC_D13_LCDC_CLK	P09_4	D2	—
32	P13_7_HEADER_BSC_D31	P13_7	C8	—
33	P09_5_HEADER_BSC_D14_LCDC_HSYNC	P09_5	C2	—
34	P10_1_HEADER_BSC_WAIT#_LCDC_DATR1	P10_1	A5	—
35	P09_6_HEADER_BSC_D15_LCDC_VSYNC	P09_6	D3	—
36	P09_7_HEADER_BSC_WE0#_LCDC_DE	P09_7	D5	—
37	P12_0_HEADER_BSC_D16	P12_0*2	D7	SW2-1: ON, SW2-2: OFF
38	P10_0_HEADER_BSC_WE1#_LCDC_DATR0	P10_0	D4	—
39	P12_1_HEADER_BSC_D17	P12_1*2	G8	SW2-1: ON, SW2-2: OFF
40	P17_7_HEADER_BSC_WE3#_AH_LCDC_DATB0	P17_7	E15	—

Notes: 1. Connected via the bus switch IC.
2. Connected via the level shifter IC with an enable function.
3. SW1-4 has to be set to ON and RXD of the RS485 has to be disabled.

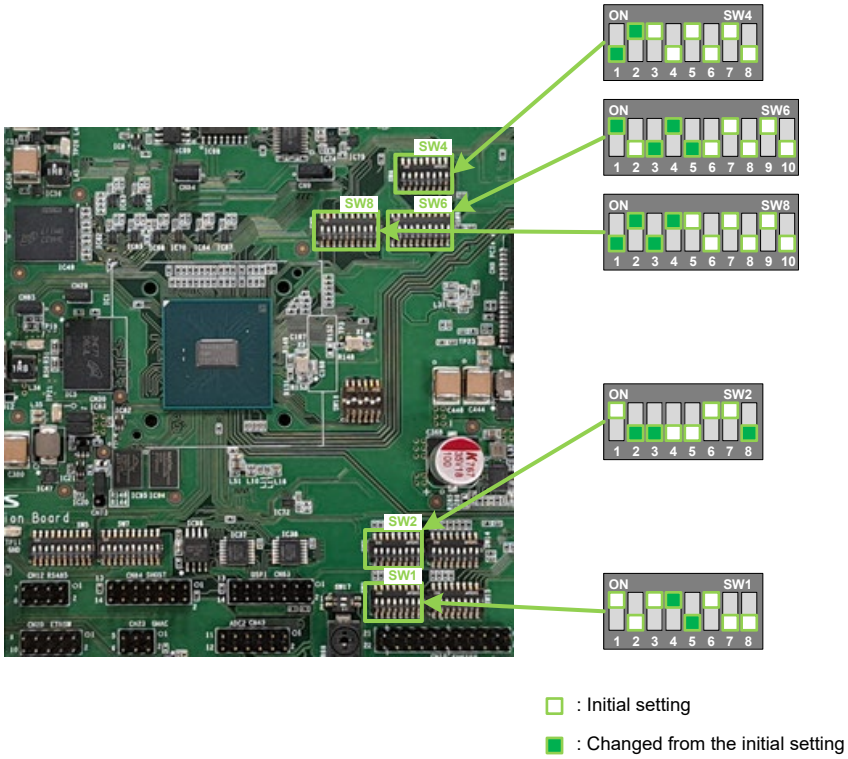


Figure 7-31 Switch Settings When Using BSC1 (CN13) and BSC2 (CN17)

Table 7-50 Signal Connections of ADC0 (CN41)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	VCC08_AVDD_ADC0	—	—	—
2	AN000_V18ADC0_AD_HEADER	—	AA27*	SW17-1: OFF, SW17-2: ON
3	AVSS_ADC0	—	—	—
4	AN001_V18ADC0_AD_HEADER	—	AB26	—
5	AVSSIO_ADC0	—	—	—
6	AN002_V18ADC0_AD_HEADER	—	AA26	—
7	VCC18_AVDDIO_ADC0	—	—	—
8	AN003_V18ADC0_AD_HEADER	—	AB27	—
9	VCC18_AVDDREF_ADC0	—	—	—
10	AVSS_ADC0	—	—	—

Note: Connected via SW17.

Table 7-51 Signal Connections of ADC1 (CN42)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	VCC08_AVDD_ADC1	—	—	—
2	AN100_V18ADC1_AD_HEADER	—	AC27*	SW18-1: ON, SW18-2: OFF
3	AVSS_ADC1	—	—	—
4	AN101_V18ADC1_AD_HEADER	—	AD27*	SW18-3: ON, SW18-4: OFF
5	AVSSIO_ADC1	—	—	—
6	AN102_V18ADC1_AD_HEADER	—	AD26*	SW18-5: ON, SW18-6: OFF
7	VCC18_AVDDIO_ADC1	—	—	—
8	AN103_V18ADC1_AD_HEADER	—	AC26	—
9	VCC18_AVDDREF_ADC1	—	—	—
10	AVSS_ADC1	—	—	—

Note: Connected via SW18.

Table 7-52 Signal Connections of ADC2 (CN43)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	AN200_V18ADC2_AD_HEADER	—	AF27	—
2	VCC08_AVDD_ADC2	—	—	—
3	AN201_V18ADC2_AD_HEADER	—	AE27	—
4	AVSS_ADC2	—	—	—
5	AN202_V18ADC2_AD_HEADER	—	AE26	—
6	AVSSIO_ADC2	—	—	—
7	AN203_V18ADC2_AD_HEADER	—	AG26	—
8	VCC18_AVDDIO_ADC2	—	—	—
9	AN204_V18ADC2_AD_HEADER	—	AF26	—
10	VCC18_AVDDREF_ADC2	—	—	—
11	AN205_V18ADC2_AD_HEADER	—	AG25	—
12	AVSS_ADC2	—	—	—

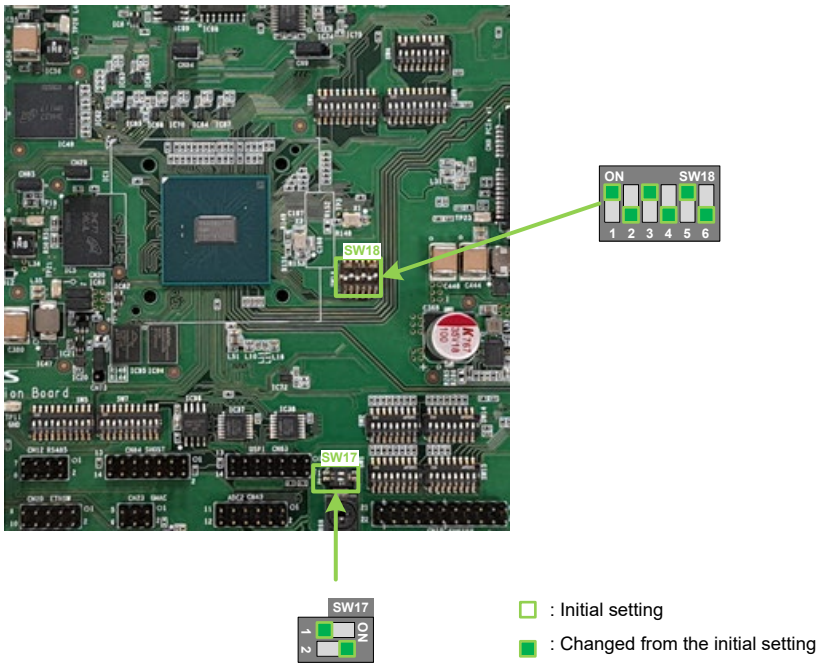


Figure 7-32 Switch Settings When Using ADC0 (CN41) and ADC1 (CN42)

7.22 Test Pins

This board is equipped with the test pins listed in Table 7-53 and Figure 7-33.

Table 7-53 List of Test Pins

Reference	Description	Reference	Description
TP3	For monitoring EXTCLKIN (DNF)	TP21	For monitoring the p0v8 power supply
TP4	GROUND (DNF)	TP22	For monitoring the p1v8 power supply
TP5	GROUND (DNF)	TP23	For monitoring the PCIE3V3 power supply
TP6	GROUND (DNF)	TP24	For monitoring the p3v3 power supply
TP7	GROUND (DNF)	TP25	For monitoring the ETH_VDD25 power supply
TP8	GROUND (DNF)	TP26	For monitoring the ETH_VDD10 power supply
TP9	GROUND (DNF)	TP27	For monitoring the P06_7_V1833_4_USER_LED2 signal
TP10	GROUND (DNF)	TP28	For monitoring the P08_5_USER_LED3 signal
TP11	GROUND	TP29	For monitoring the P18_0_ESC_LED_RUN signal
TP14	For monitoring the CPU3V3 power supply	TP30	For monitoring the P18_1_ESC_LED_ERR signal
TP15	GROUND	TP31	For monitoring the P22_7_ESC_LINKACT0 signal
TP16	For monitoring the cVBUS power supply	TP32	For monitoring the P23_0_ESC_LINKACT1 signal
TP17	For monitoring the P3V3_USB_PD power supply	TP33	For monitoring the P23_5_ESC_LINKACT2 signal
TP18	For monitoring the P12V power supply	TP34	For monitoring the P23_1_USER_LED0 signal
TP19	For monitoring the p1v1 power supply	TP35	For monitoring the P32_2_USER_LED1 signal
TP20	For monitoring the p5v0s power supply	TP36	For monitoring the 15-V power generation unit

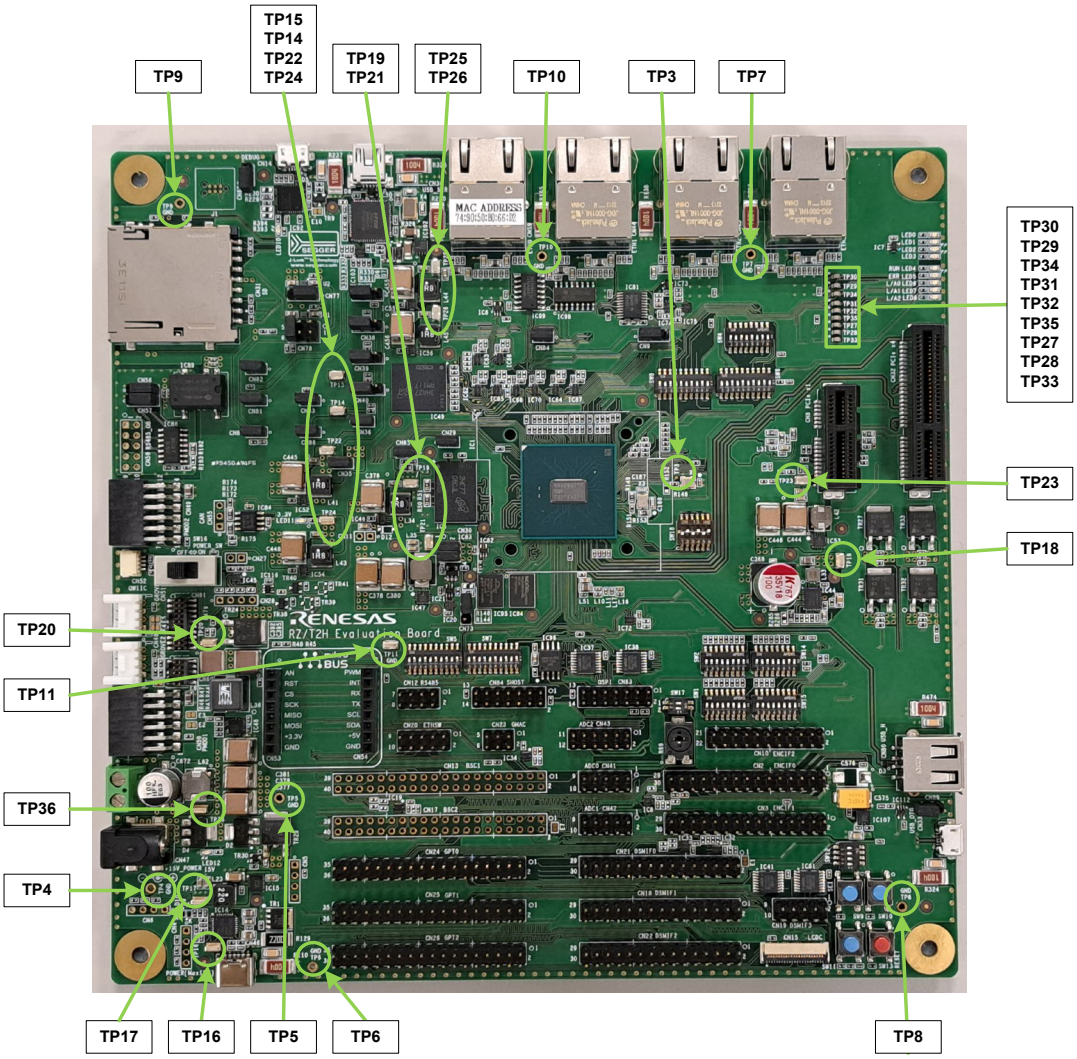


Figure 7-33 Arrangement of Test Pins

8. Developing Code

8.1 Overview

The following methods for debugging code for this device are available.

- Connect this board to a PC via J-Link™ OB, which is a development tool from Segger and mounted on this board.
- Connect this board to a PC via an emulator from a given company.

For more details on individual emulators, refer to the Web sites of the manufacturers.

8.2 Supported Modes

This board supports a variety of boot modes. The possible mode settings are shown in section 6.3.1. For detailed information on the microprocessor, such as operating modes and registers, refer to the RZ/T2H and RZ/N2H Groups User's Manual: Hardware.

Mode settings should only be changed while the power is turned off to avoid causing damage to the microprocessor.

8.3 Address Spaces

For details on the usable address spaces determined by the operating mode of the microprocessor, refer to the RZ/T2H and RZ/N2H Groups User's Manual: Hardware.

9. Usage Notes

9.1 Handling of the XTALSEL Pin

Though the circuitry of this board is configured so that XTALSEL does not pass through any resistor when it is at the low level because it is to be switched by a switch during evaluation, operation with this circuit configuration is not guaranteed. When XTALSEL is to be set to the low level (selecting EXTCLKIN as the main clock source) on a customer’s board, connect it to VSS via a resistor according to the descriptions in the RZ/T2H and RZ/N2H Groups User’s Manual: Hardware (R01UH1039EJ).

9.2 Use of the RGB-HDMI Conversion Board

Warning

When this board is used with an RGB-HDMI conversion board connected to the LCD interface, the EMC emission may exceed the restriction on class A equipment according to EN55032:2015. Therefore, special care must be taken, such as keeping this board away from EMC-sensitive equipment. If interference does occur, separation by a longer distance may be required. In such cases, additional appropriate measures should be taken on the responsibility of the user and operator of the equipment.

10. Support

For details on the RZ/T2H microprocessors, refer to the RZ/T2H and RZ/N2H Groups User's Manual: Hardware (R01UH1039EJ).

Online technical support and information are available from this Web page: https://www.renesas.com/.

Technical Contact Details

America: techsupport.america@renesas.com

Europe: https://www.renesas.com/en-eu/support/contact.html

Global & Japan: https://www.renesas.com/support/contact.html

General information on Renesas microprocessors can be found on the Renesas website at: https://www.renesas.com/.

Design and Manufacturing Information

The design and manufacturing information on this board "RZ/T2H Evaluation Board Design Package" can be obtained from: https://www.renesas.com/rzt2h-evkit.

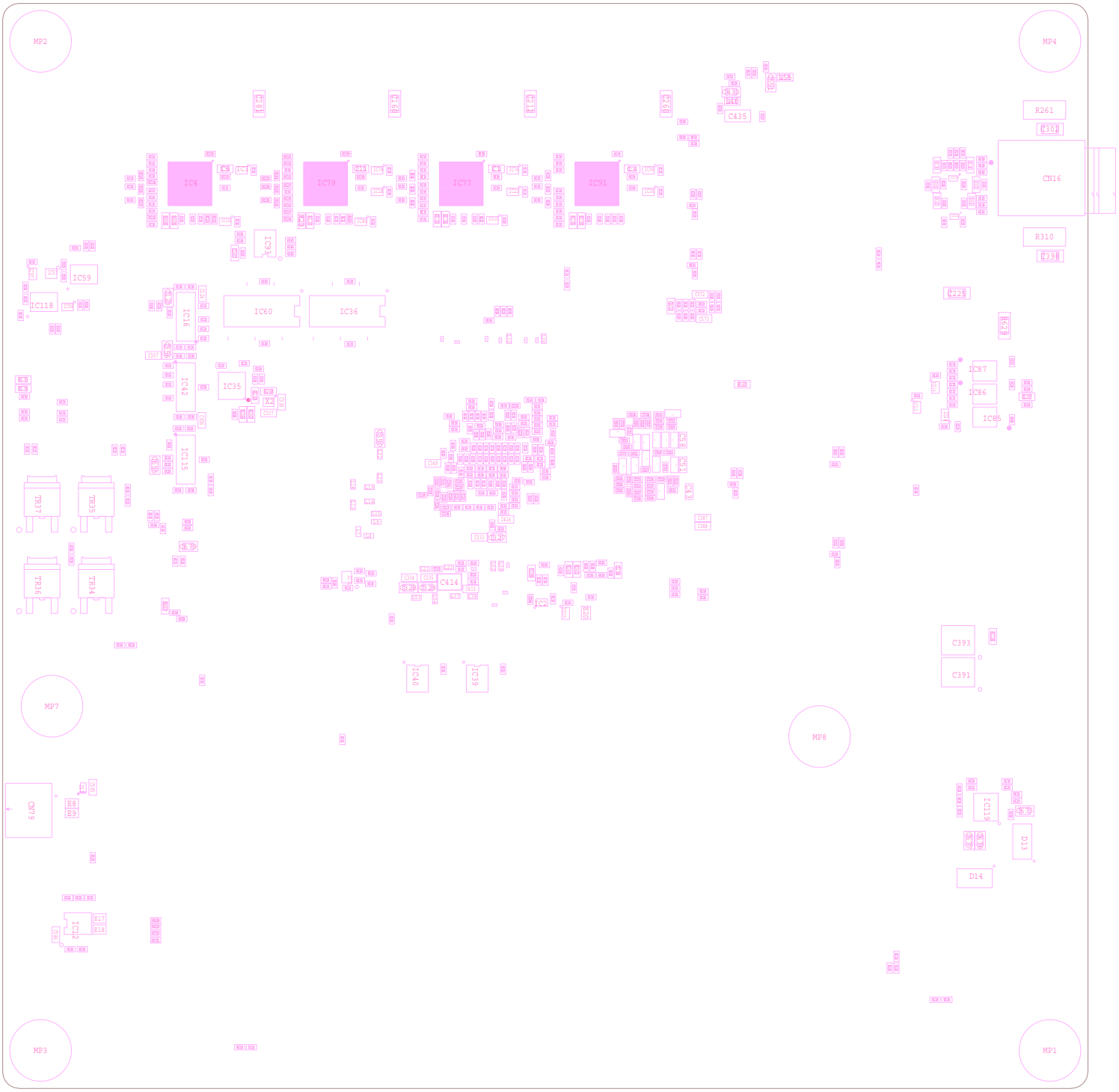
- File name: rzt2h-evaluation-board-v1-designpackage.zip
- File contents

Table 10-1 Contents of the RZ/T2H Evaluation Board Design Package

File Type	Description	File Name or Folder Name
File (txt)	Readme	Readme for schematic.txt
File (PDF)	Schematics	rzt2h-evaluation-board-v1-schematic.pdf
File (PDF)	Mechanical drawings	rzt2h-evaluation-board-v1-mechdwg.pdf
File (PDF)	3D drawings	rzt2h-evaluation-board-v1-3d.pdf
File (xlsx)	Bill of materials (BOM)	rzt2h-evaluation-board-v1-BOM.xlsx
Folder	Manufacturing files	rzt2h-evaluation-board-Manufacturing Files
Folder	Design files	rzt2h-evaluation-board-Design Files

11. Appendix

The arrangements of individual components on this board are shown in this appendix.


MP2
MP4
MP7
MP8
MP3
MP1
IC4
IC79
IC77
IC91
IC60
IC36
IC59
IC118
IC35
IC87
IC86
IC85
IC2
IC12
IC19
CN16
CN76
R261
R310
C435
C393
C391
C414
D13
D14

Revision History	RZ/T2H Group RZ/T2H Evaluation Board User's Manual

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		Page	Summary
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