User's Manual

32

SH7267 CPU Board

R0K572670C000BR

User's Manual

Renesas 32-bit RISC Microcomputer
SuperH™ RISC engine Family / SH7260 Series

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Chapter 1
Overview

1.1 Introduction

The SH7267 CPU board and its optional boards are designed for evaluating the features and performance of the SH7267 Group of Renesas Electronics original microcomputers (MCUs), as well as for developing and evaluating application software for these MCUs. Following are features of the SH7267 CPU board and optional boards.

1.1.1 SH7267 CPU board (Part number: R0K572670C000BR)

The R0K572670C000BR comes standard with 4-MB NOR flash memory (16-bit bus width), 16-MB SDRAM (16-bit bus width), 256-MB NAND flash memory and 2-MB serial flash memory as its external memory. The R0K572670C000BR has three boot options;

- Boot from NOR flash memory
- Boot from NAND flash memory
- Boot from serial flash memory

The R0K572670C000BR comes standard with an RS-232C connector and a USB connector as the SH7267 peripheral interfaces.

The USB connector on the R0K572670C000BR is a Series-A receptacle. The wiring pattern on the R0K572670C000BR allows for connecting a Mini-B receptacle to evaluate the USB host and function modules.

The SH7267 data bus, address bus and internal peripheral pins are connected to expansion connectors on the R0K572670C000BR to allow for timing evaluation with peripherals using measurement instruments, and the development of the optional board according to its application.

The Renesas Electronics E10A-USB on-chip emulator (AUD trace enabled: 36-pin, AUB trace disabled: 14-pin) can be connected to the R0K572670C000BR.

1.1.2 Optional board for audio (Part number: M3A-HS64G01)

The M3A-HS64G01 is an evaluation board suitable for advance development of the audio system, which comes standard with an audio interface, CD deck interface and character LCD module connector.

Also, it comes with two channels of a D/A converter for audio output, and one channel of a D/A converter and an A/D converter for audio input and output as its audio interfaces.

It also comes standard with an LCD module interface connector, a UART interface connector, a CAN (Controller Area Network) connector, an IEBus™ connector, an IIC connector, and an SD card connector.

Note: Some of the functions cannot be used with the R0K572670C000BR.

1.1.3 Optional board for graphic display (Part number: M3A-HS64G02)

The M3A-HS64G02 is an evaluation board, which comes standard with a video input interface, an audio interface and an LCD module interface for developing the video processing or music-playing applications.

All PWM output pins and timer output pins are inserted into connectors to allow for developing the automotive meter or brightness-control applications.

It comes standard with a CAN connector, an IEBus™ connector, an IIC connector and an SD card connector.

Note: Some of the functions cannot be used with the R0K572670C000BR.

1.2 R0K572670C000BR Configuration

The following figure shows an example of the system configuration using the R0K572670C000BR.

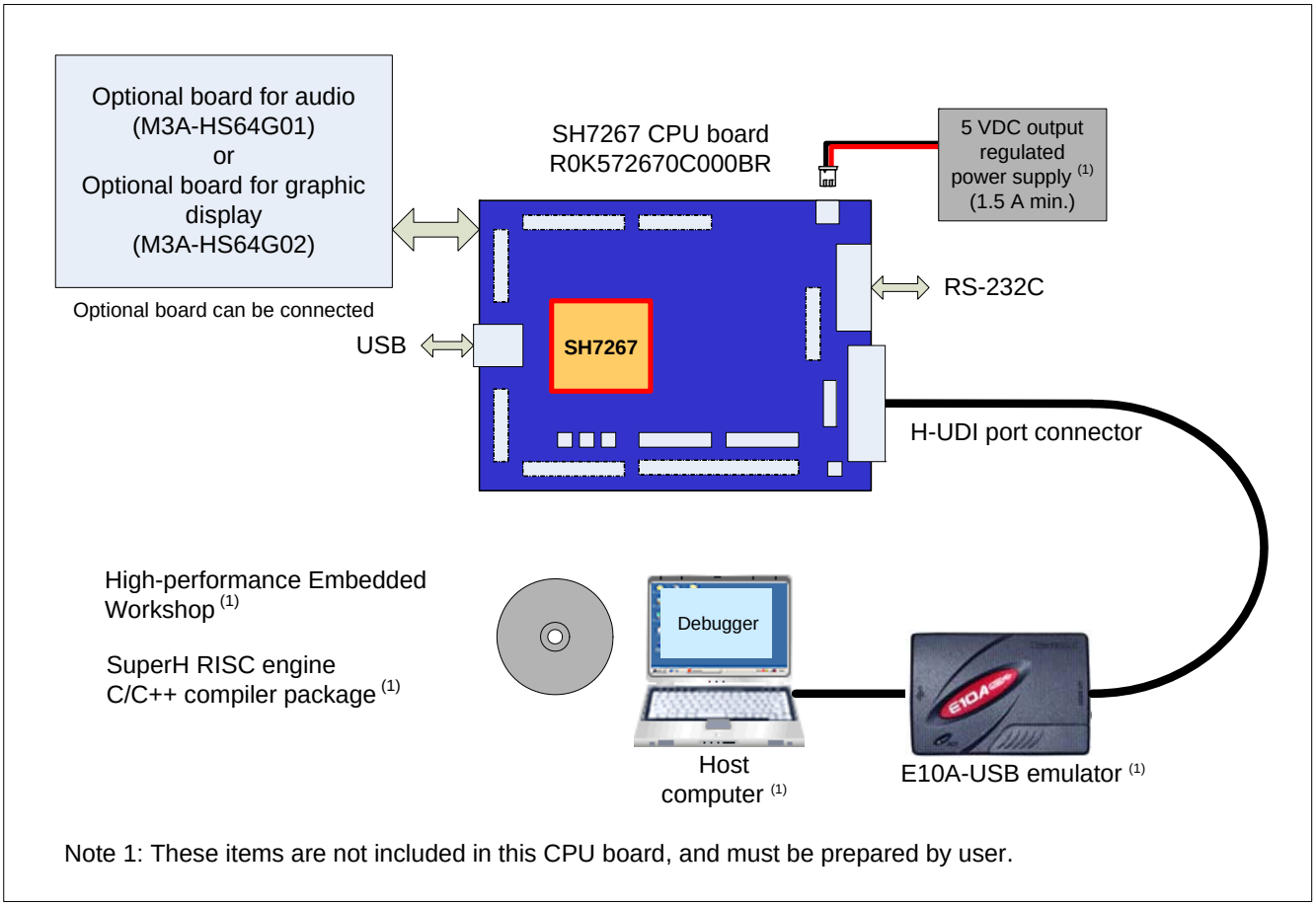


Figure 1.2.1 R0K572670C000BR System Configuration Example

1.3 R0K572670C000BR Board Specifications

Table 1.3.1 and Table 1.3.2 describe the board specifications of the R0K572670C000BR.

Table 1.3.1 Board Specifications (1/2)

No.	Item	Description
1	CPU	• SH7267 ・Input (XIN) clock: 12 MHz ・Bus clock: 72 MHz at maximum ・CPU clock: 144 MHz at maximum ・Internal memory Hi-speed internal RAM: 64 KB Large-capacity internal RAM: 1.5 MB Instruction cache: 8 KB Operand cache: 8 KB ・Power supply voltage: internal - 1.25 V, I/O - 3.3 V ・176-pin QFP, 0.5 mm pitch (package code: PLQP0176KB-A)
2	External memory	• SDRAM: 16 MB ・EDS1216AATA-75E: 1 (Elpida) • NOR flash memory: 4 MB ・S29GL032N90TFI030: 1 (SPANSION) • NAND flash memory: 256 MB ・K9F2G08U0A-PCB0: 1 (Samsung) • Serial flash memory: 2 MB ・SST25VF016B-75: 1 (SST) • EEPROM: 16 KB ・R1EX24128ASA00A: 1 (Renesas)
3	USB	• USB Series-A receptacle (Mini-B receptacle is optional)
4	Connectors and through-holes	• H-UDI port connectors (36-pin and 14-pin) • RS-232C connector (D-sub 9-pin) • 20-pin MIL-spec connectors ・SH7267 expansion connectors: 6 (Ports A, C to F, H, and J) • 30-pin MIL-spec connectors ・SH7267 expansion connectors: 2 (Ports B and G) • 40-pin MIL-spec connector ・SH7267 expansion connector: 1 (Ports E, and F)
5	LEDs	• Power supply LED: 1 • User LEDs: 2 (connected to the SH7267 I/O pins)

Table 1.3.2 Board Specifications (2/2)

No.	Item	Description
6	Switches	• Reset switch: 1 • NMI switch: 1 • IRQ1 switch: 1 • TEST switch: 1 • System setting DIP switches: 6/package • User DIP switches: 6/package
7	Board specifications	• Dimensions: 148 mm x 105 mm • Mounting form: 6 layers, double-sided • Board thickness: 1.6 mm • Number of boards: 1

1.4 R0K572670C000BR Exterior

The following figure shows the exterior of the R0K572670C000BR.

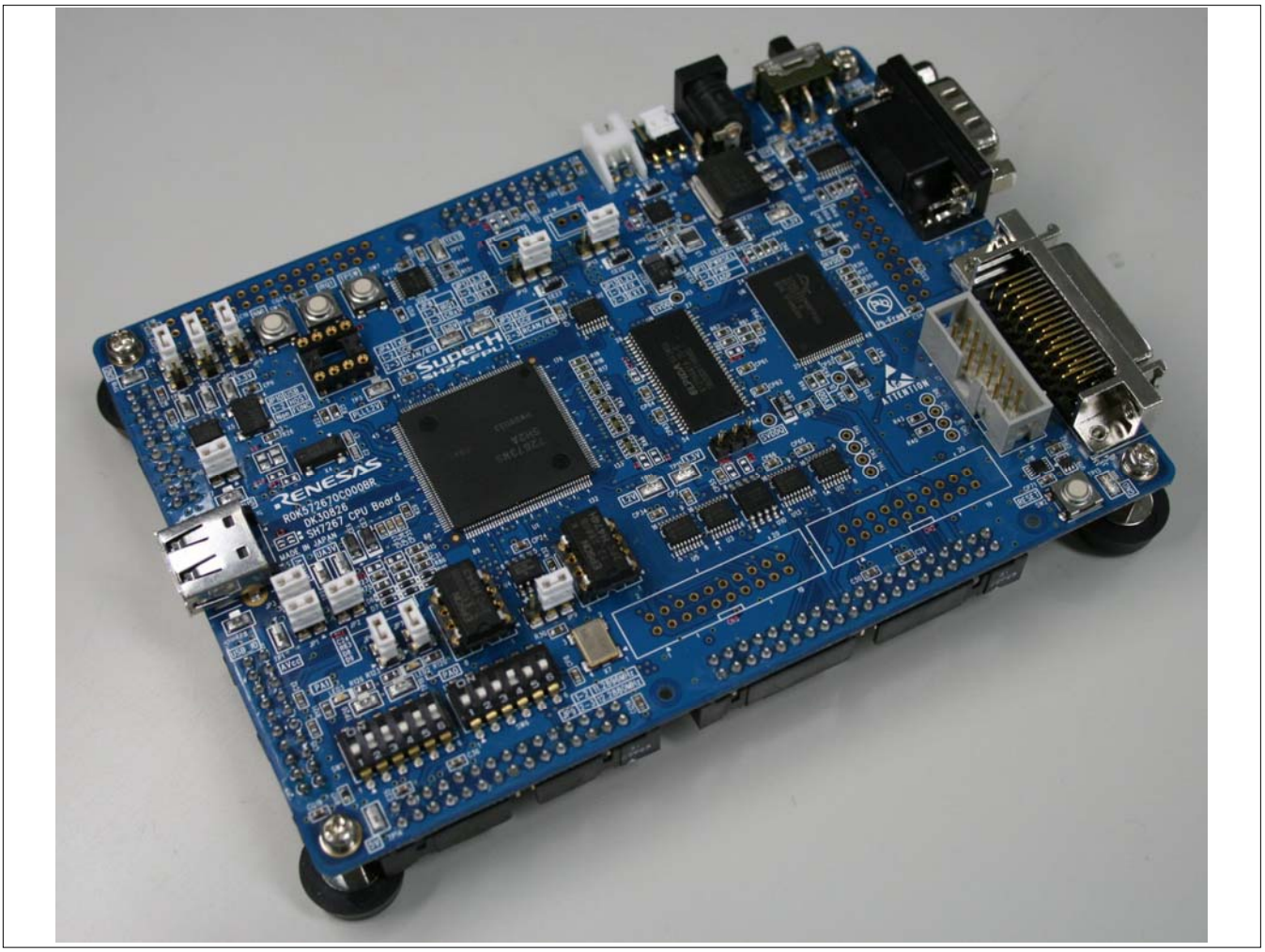


Figure 1.4.1 SH7267 CPU board Exterior

1.5 R0K572670C000BR Block Diagram

The following figure shows the system block diagram of the R0K572670C000BR.

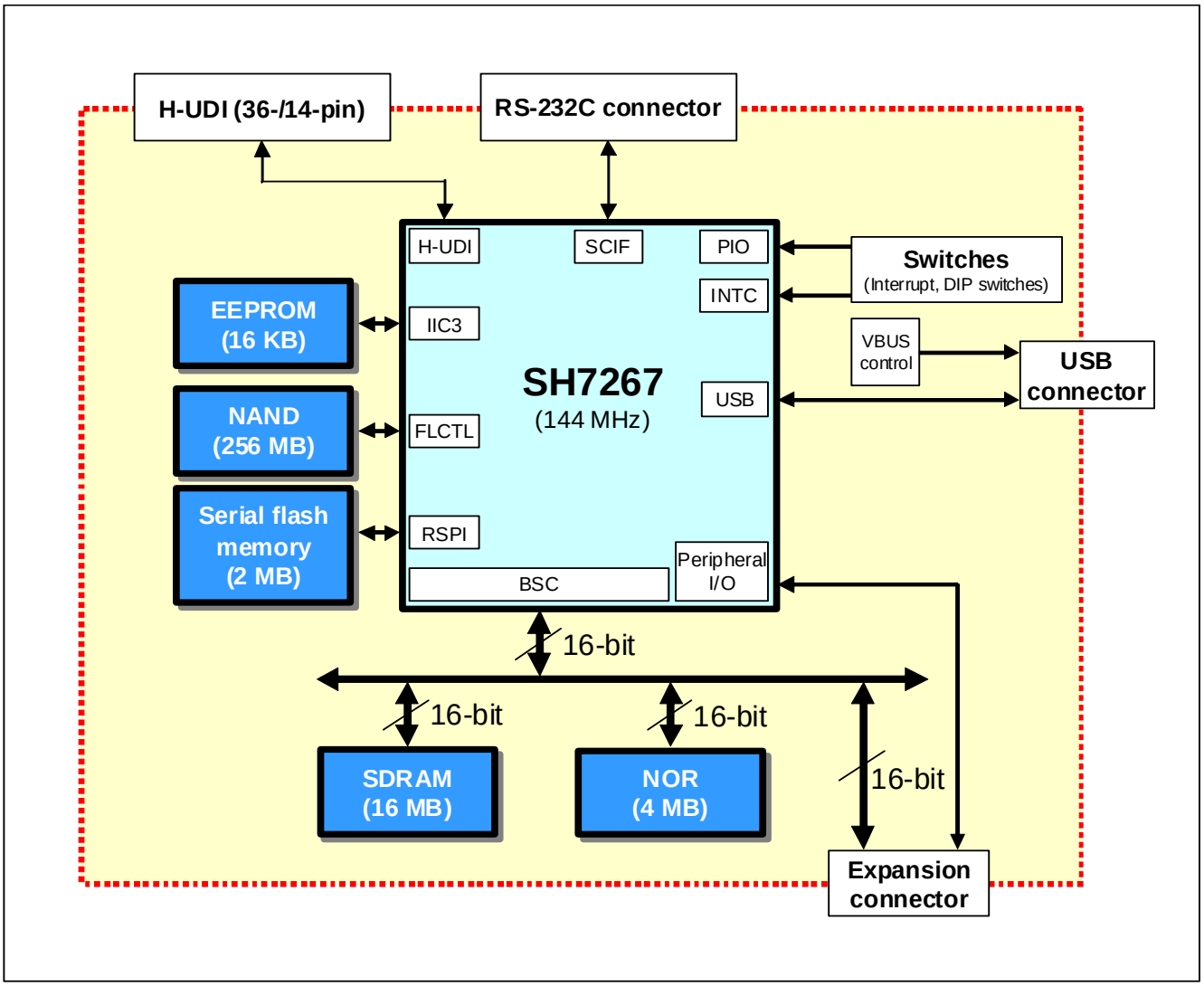


Figure 1.5.1 R0K572670C000BR System Block Diagram

1.6 R0K572670C000BR Major Components

Figure 1.6.1 and Figure 1.6.2 show the R0K572670C000BR layout and locations of the major components (PCB drawing).

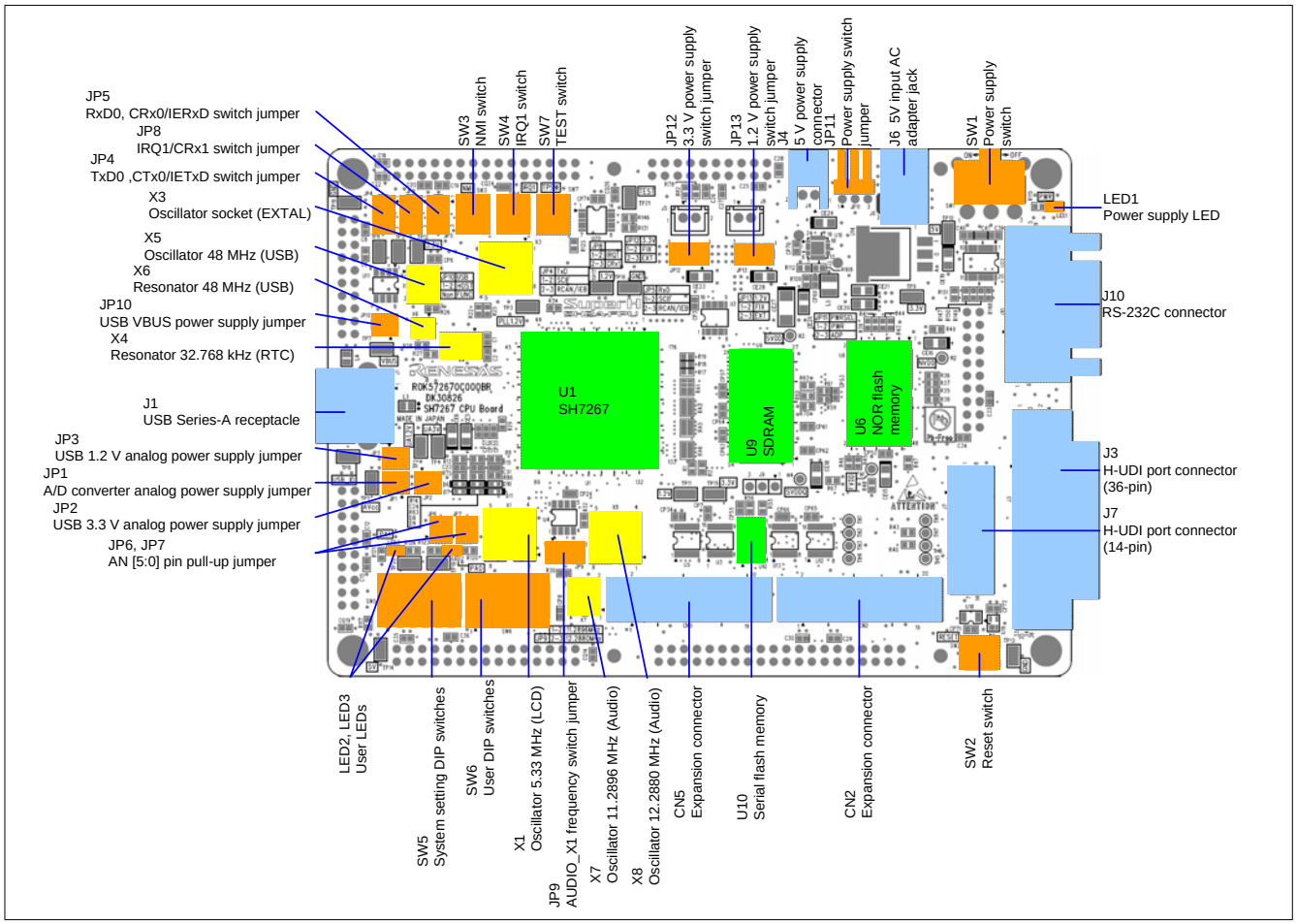


Figure 1.6.1 R0K572670C000BR Component Layout and Placement (Top View of the Component Side)

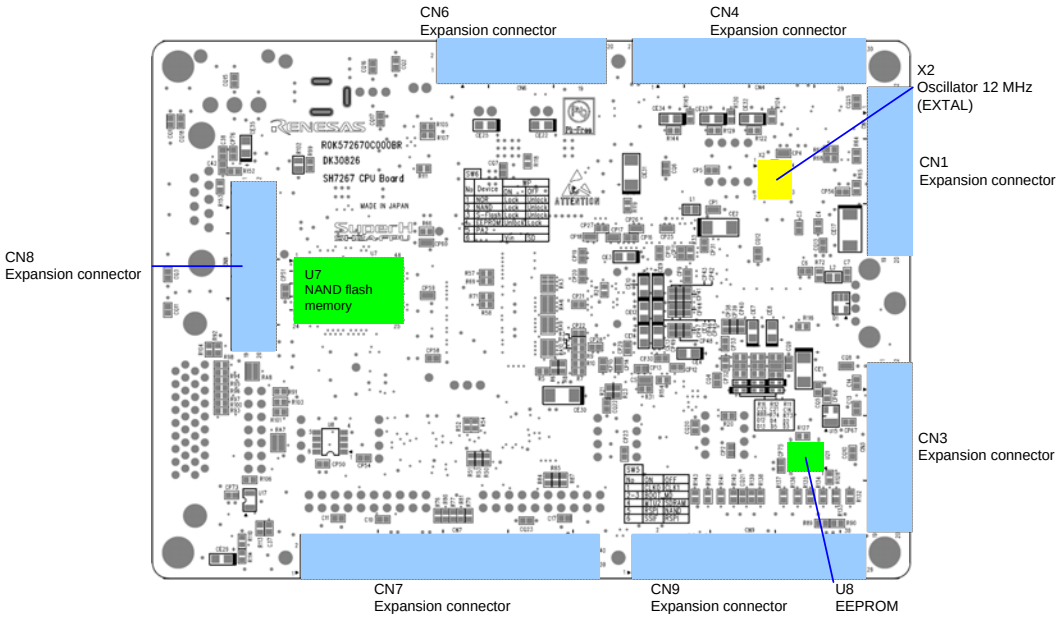


Figure 1.6.2 R0K572670C000BR Layout and Component Placement (Top View of the Solder Side)

The following tables list the major components on the R0K572670C000BR.

Table 1.6.1 Major components on the R0K572670C000BR - ICs (1/3)

No.	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	MCU	R5S72673P144FPU	Renesas	Main MCU	1
2	SDRAM	EDS1216AATA-75E	Elpida	16-bit bus, 16 MB	1
3	NOR Flash memory	S29GL032N90TFI030	Spansion	16-bit bus, 4 MB	1
4	NAND Flash memory	K9F2G08U0A-PCB0	Samsung	8-bit bus, 256 MB	1
5	Serial Flash memory	SST25VF016B-75	SST	4-wire serial, 2 MB	1
6	EEPROM	R1EX24128ASA00A	Renesas	2-wire serial 16 KB	1
7	Reset IC	RNA50C27AUS	Renesas		1
8	RS-232C driver	MAX3222ECUP	MAXIM		1
9	Adjustable regulator	LMS1587CSX-ADJ	NS	3.3 V	1
10	Adjustable regulator	R2A20101NP	Renesas	1.25 V	1
11	Voltage reference	LM4132AMF-3.3	NS	Reference power supply for ADC	1
12	Multiplexers	SN74CB3Q3257DBQR	TI	Analog switch	6

Table 1.6.2 Major components on the R0K572670C000BR - Connectors (2/3)

No.	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	36-pin H-UDI port connector	DX10M-36SE	HRS		1
2	14-pin H-UDI port connector	7614-6002	3M		1
3	RS-232C connector	XM2C-0942-132L	OMRON	D-sub 9-pin	1
4	20-pin expansion connectors	XG4C-2031	OMRON	20-pin MIL-spec connector	6
5	30-pin expansion connectors	XG4C-3031	OMRON	30-pin MIL-spec connector	2
6	40-pin expansion connector	XG4C-4031	OMRON	40-pin MIL-spec connector	1
7	DIP switches (6/package)	A6S-6104-H	OMRON	System setting and user DIP switches	2
8	USB Series-A receptacle	UBA-4R-D14T-4D	J.S.T	DIP type	1
9	USB Mini-B receptacle	54819-0572	MOLEX	Optional	0

Table1.6.3 Major components on the R0K572670C000BR -USB and peripherals (3/3)

No.	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	USB power distribution switch	MIC-2025-2YM	MICREL	VBUS power control	1
2	Zener Diode	HZN6.2Z4MFA	Renesas	Optional	0
3	Ferrite Beads	BLM21PG600SN1	Murata	Optional	0
4	Common mode choke	DLW21HN900SQ2	Rohm	Optional	0

1.7 M3A-HS64G01 Configuration

The following figure shows an example of the system configuration using the M3A-HS64G01 (optional board for audio).

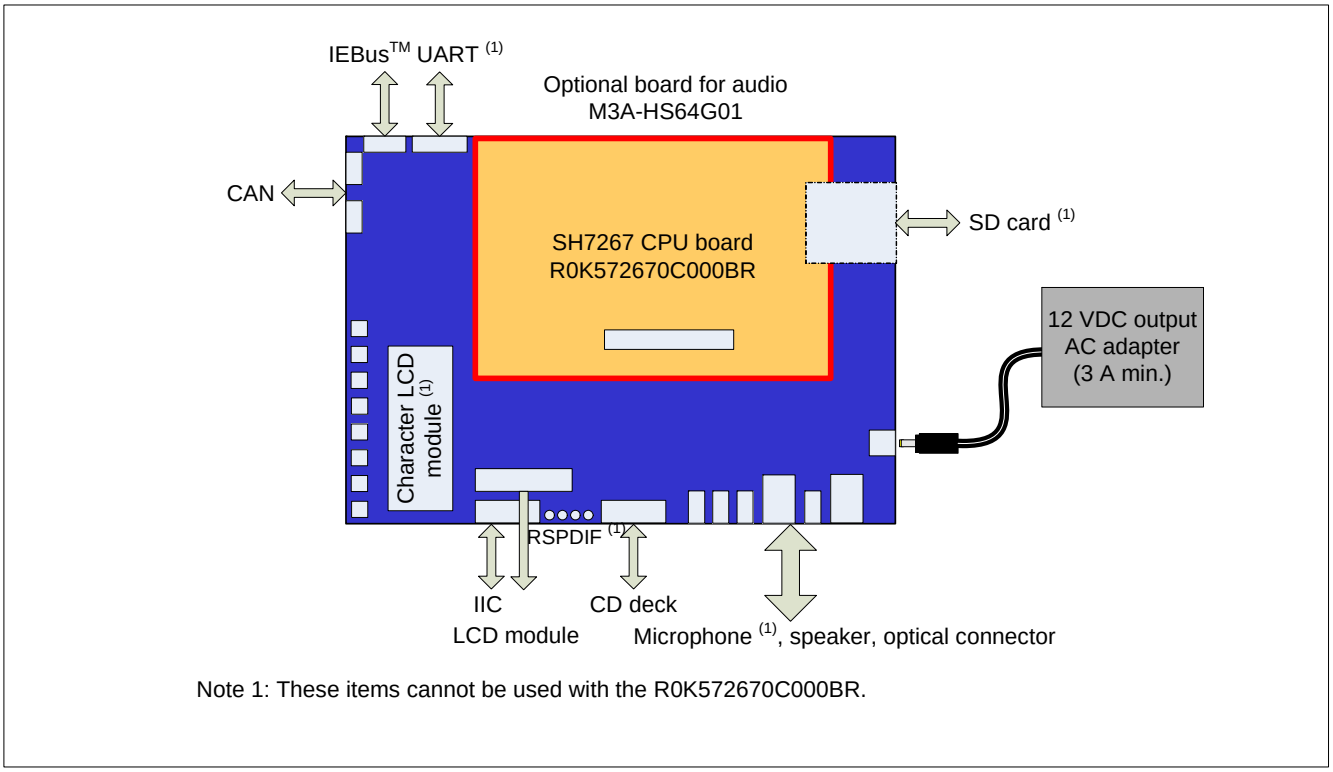


Figure 1.7.1 M3A-HS64G01 System Configuration Example

1.8 M3A-HS64G01 Board Specifications

The following table describes the board specifications of the M3A-HS64G01.

Table 1.8.1 Board Specifications

No.	Item	Description
1	LCD	Comes with following connecters to control an LCD module by the SH7267 on-chip Video Display Controller 3 (VDC3) • Flexible connectors for LCD module: 2 • MIL-spec connector for LCD module: 1 (30-pin)
2	Character LCD	Controls the character LCD module by the SH7267 on-chip general-purpose I/O ports Note: This module cannot used with the R0K572670C000BR. • 16 x 2 semi-transmissive character LCD module with LED backlight: 1
3	Audio	Comes with audio codecs for audio input (AK4353) and audio input/output (AK4524) by the SH7267 on-chip Serial Sound Interface with FIFO (SSIF) • AK4353 (Asahi Kasei EMD Corporation): 2 • 96 kHz 24-bit DAC, on-chip digital audio transmitter • Sampling frequency: 16 kHz to 96 kHz • Stereo pin jacks: 2 • Optical connectors: 2 Note: One audio codec (AK4353) can be used with the R0K572670C000BR. • AK4524 (Asahi Kasei EMD Corporation): 1 • 24-bit stereo codec with microphone AMP • Sampling frequency: 32 kHz to 48 kHz Note: This module cannot be used with the R0K572670C000BR.
4	CD deck	Inputs PCM data using the SH7267 on-chip SSIF and controls the CD deck by the Renesas Serial Peripheral Interface (RSPI) • Flexible connector for connecting a CD deck: 1
5	SD card interface	Accesses the SD card by the SH7267 on-chip SD host interface (SDHI) Note: This module cannot be used with the R0K572670C000BR. • SD card slot : 1 • Includes a card power control IC (Software control NOT allowed)
6	CAN	CAN (Controller Area Network) communication by the SH7267 on-chip CAN (RCAN-TL1) • HA13721FP (Renesas CAN driver IC), includes a voltage level shifter
7	IEBus™	IEBus™ communication by the SH7267 on-chip IEBus controller (IEB) • HA12187FP (Renesas IEBus driver IC), includes a voltage level shifter
8	UART interface	Connected to the SH7267 on-chip Serial Communication Interface with FIFO (SCIF) pin Note: This module cannot be used with the R0K572670C000BR.
9	IIC	Connected to the SH7267 on-chip IIC bus interface (IIC3) pin • MIL-spec connector for connecting an external IIC interface: 1 (20-pin)
10	Switches	Key input by the SH7267 on-chip A/D converter • Key input switches: 16 (4 switches x 4 inputs)
11	Board specifications	• Specifications: 210 mm x 148 mm • Mounting form: 4 layers, double-sided • Board thickness: 1.6 mm • Number of boards: 1

1.9 M3A-HS64G01 Exterior

The following figure shows the exterior of the M3A-HS64G01.

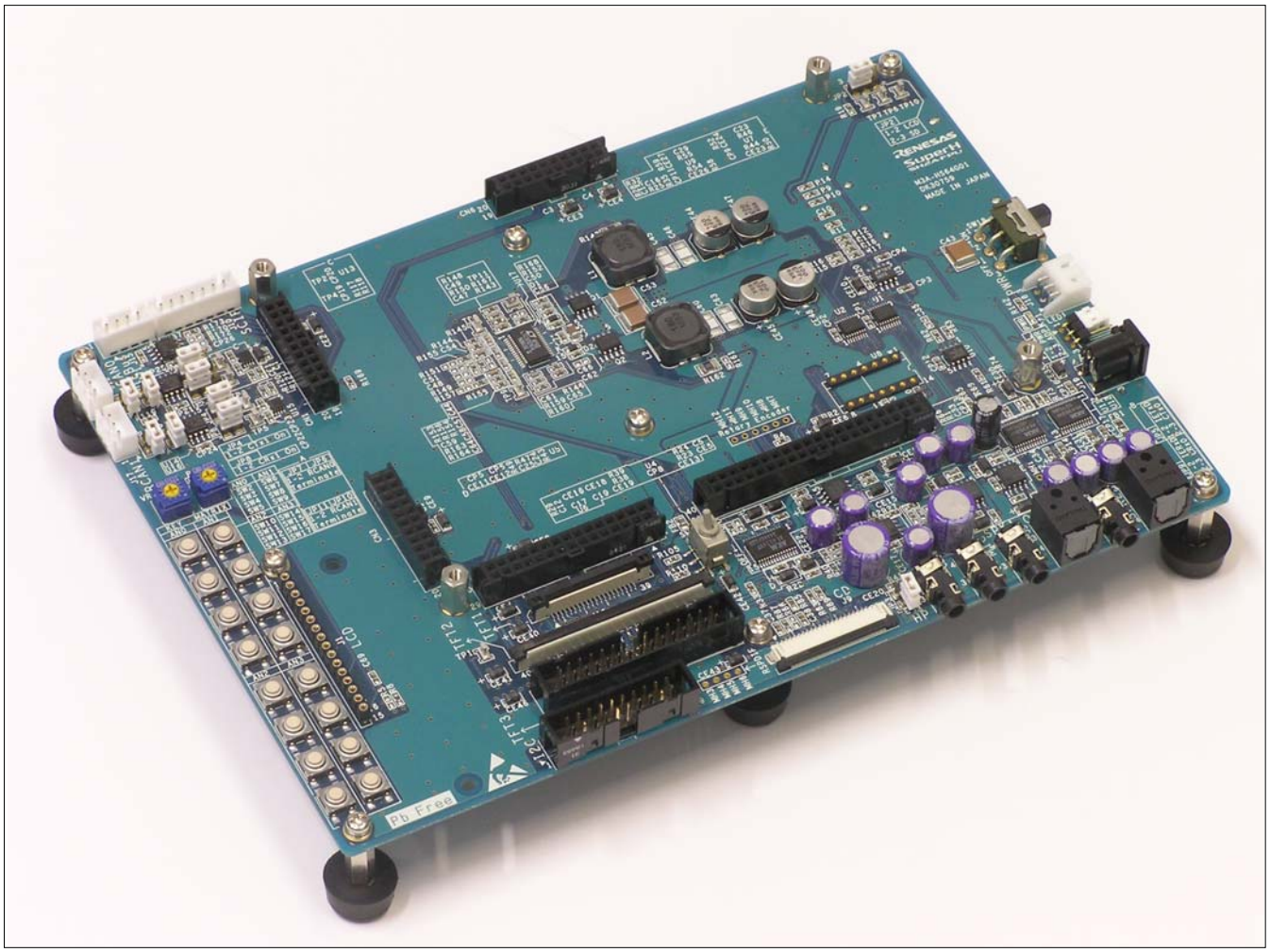


Figure 1.9.1 M3A-HS64G01 Exterior

1.10 M3A-HS64G01 Block Diagram

The following figure shows the block diagram of the M3A-HS64G01.

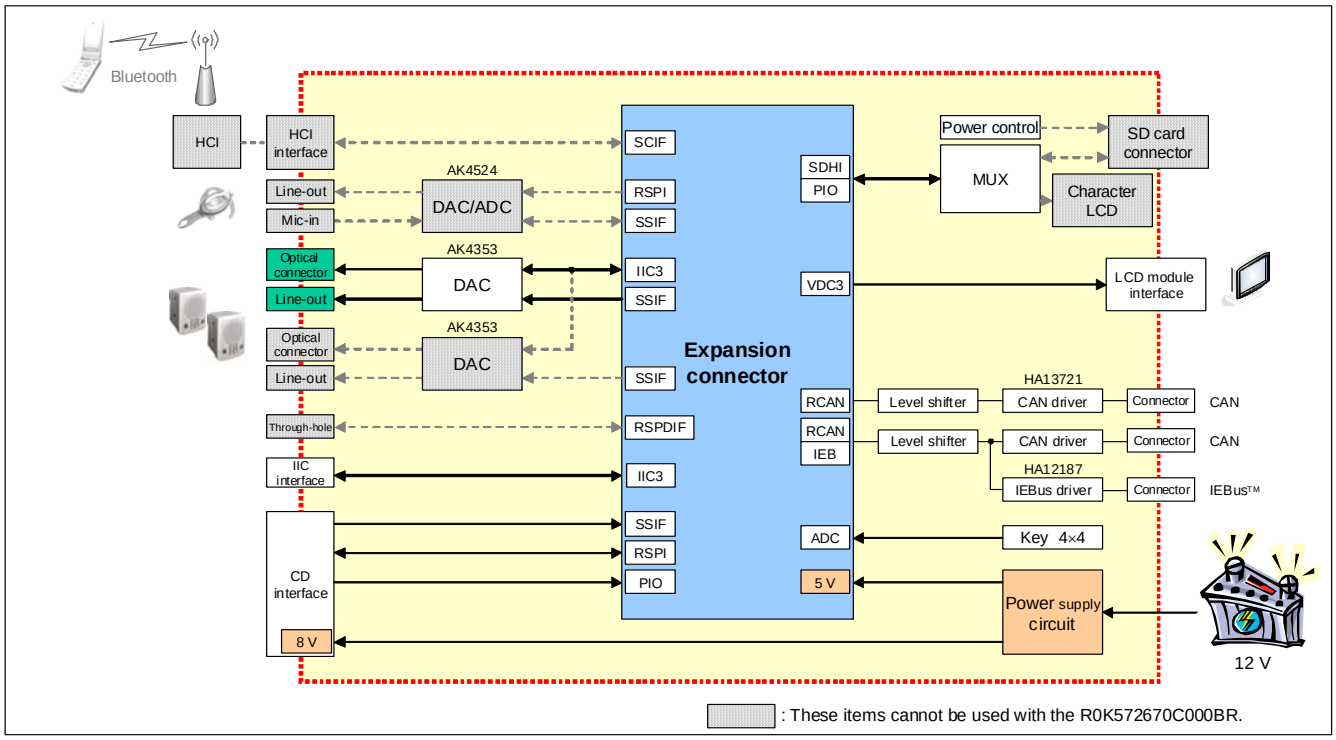


Figure 1.10.1 M3A-HS64G01 Block Diagram

1.11 M3A-HS64G01 Major Components

Figure 1.11.1 and Figure 1.11.2 show the M3A-HS64G01 layout and locations of the major components (PCB drawing).

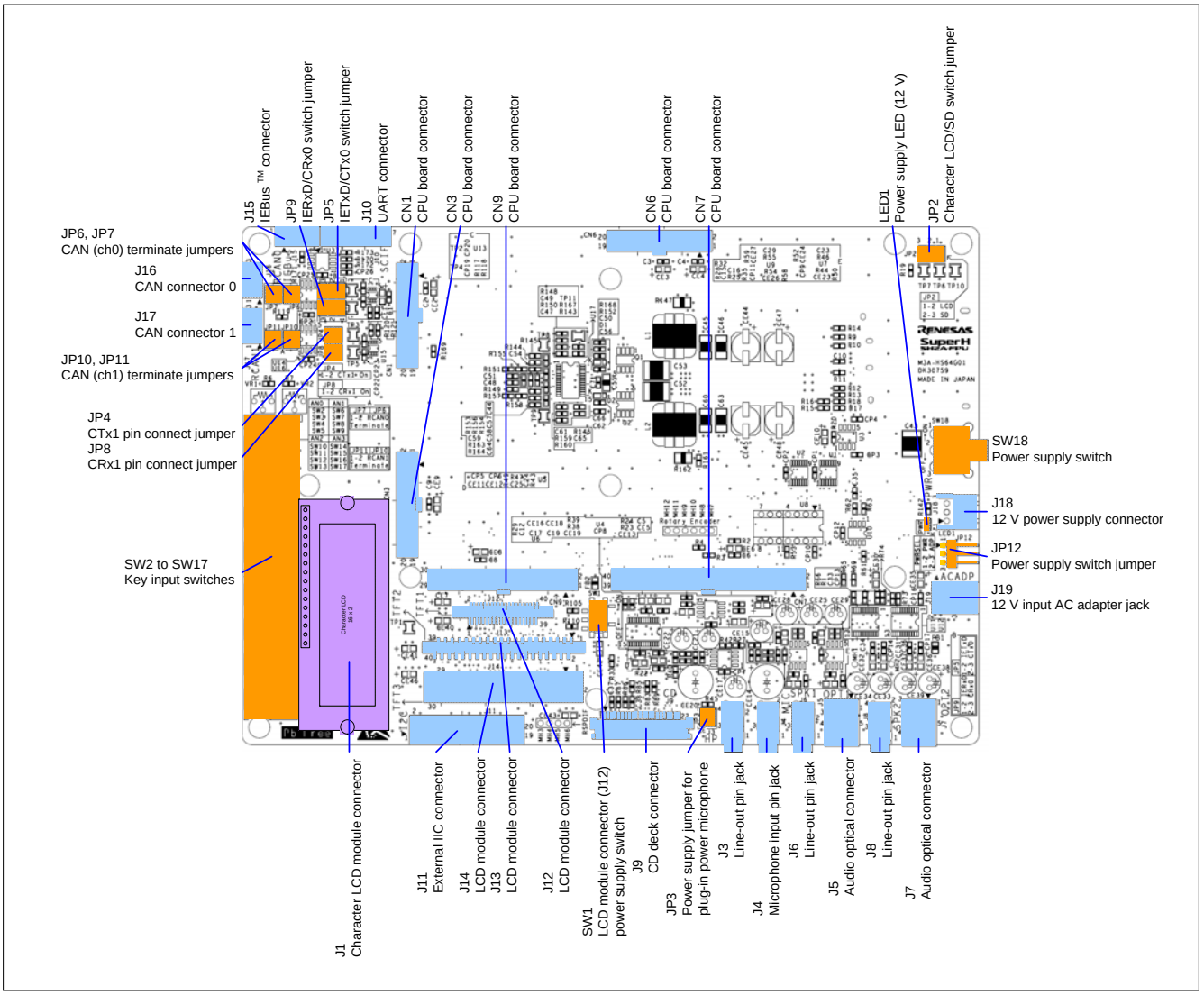


Figure 1.11.1 M3A-HS64G01 Layout and Component Placement (Top View of the Component Side)

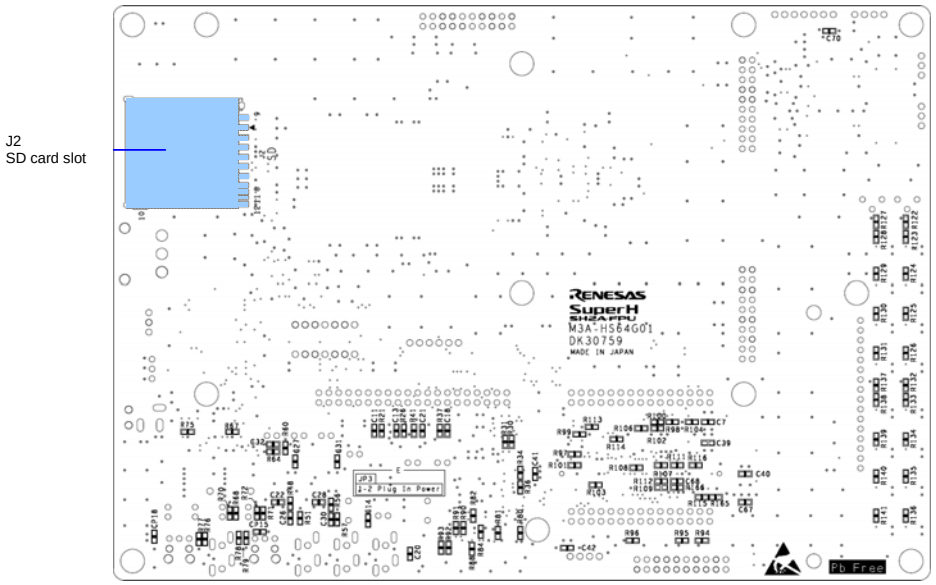


Figure 1.11.2 M3A-HS64G01 Layout and Component Placement (Top View of the Solder Side)

The following tables list the major components on the M3A-HS64G01.

Table 1.11.1 Major Components - ICs (1)

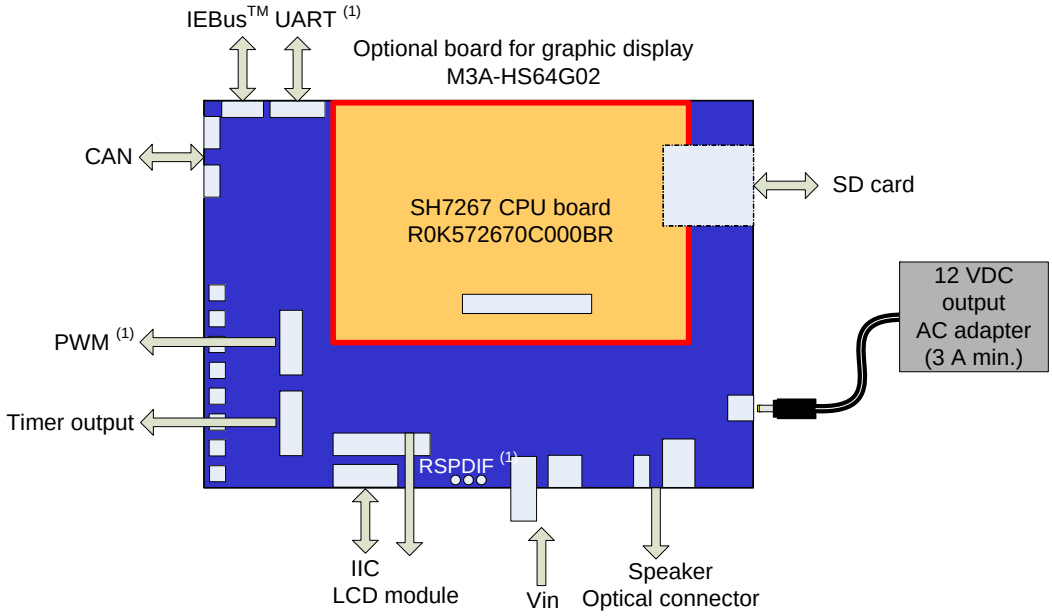
No.	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	Character LCD module	SD1602H	SUNLIKE	16 characters x 2 lines	1
2	Audio codec	AK4524VF	AKM	24-bit 96 kHz audio codec	1
3	D/A converters	AK4353VF	AKM	96 kHz 24-bit D/A converter	2
4	CAN drivers	HA13721FP	Renesas		2
5	IEBus™ driver	HA12187FP	Renesas		1
6	Adjustable regulator	LTC3727EG	LT	8 V/5 V	1
7	Multiplexers	SN74CB3Q3257DBQR	TI	Analog switch	2

Table 1.11.2 Major Components -Connectors (2)

No.	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	20-pin expansion connectors	XG4C-2031	OMRON	20-pin MIL-spec connector	3
2	30-pin expansion connector	XG4C-3031	OMRON	30-pin MIL-spec connector	1
3	40-pin expansion connector	XG4C-4031	OMRON	40-pin MIL-spec connector	1
4	SD card slot	DM1B-DSF-PEJ	HRS	Reverse type	1
5	Audio optical connectors	TOTX147PL	TOSHIBA		2
6	CD deck connector	IMSA-9617S-22	IRISO	1 mm pitch FFC	1
7	UART connector	B7B-XH-A	J.S.T	TTL level	1
8	External IIC connector	XG4C-2031	OMRON	20-pin MIL-spec connector	1
9	LCD module connector 1 (J12)	IMSA-9639S-40D	IRISO	0.5 mm pitch FFC, for TX09D55VM1CDA only	1
10	LCD module connector 2 (J13)	IMSA-9619S-40B	IRISO	1 mm pitch FFC, for TX09D14VM3CCA only	1
11	LCD module connector 3 (J14)	XG4C-3031	OMRON	30-pin MIL-spec connector General-purpose	1
12	IEBus™ connector	B4B-XH-A	J.S.T	2.5 mm pitch	1
13	CAN connectors	B3B-XH-A	J.S.T	2.5 mm pitch	2

1.12 M3A-HS64G02 Configuration

The following figure shows an example of the system configuration using the M3A-HS64G02 (optional board for graphic display).



Note 1: These items cannot be used with the R0K572670C000BR.

Figure 1.12.1 M3A-HS64G02 System Configuration Example

1.13 M3A-HS64G02 Board Specifications

The following table describes the M3A-HS64G02 board specifications.

Table 1.13.1 Board Specifications

No.	Item	Description
1	LCD	Comes with following connectors to control an LCD module by the SH7267 on-chip VDC3 • Flexible connectors for LCD module: 2 • MIL-spec connector for LCD module: 1 (30-pin)
2	Video signal input	Inputs the video signal in the SH7267 on-chip VDC3 • AK8851 (Asahi Kasei EMD Corporation): 1 ・Decodes NTSC or PAL composite video signal and S-video signal digitally ・Includes two channels of a 10-bit ADC (Operates at 27 MHz) ・Composite video pin (RCA connector) ・S-video connector
3	Audio	Comes with an audio codec for audio output by the SH7267 on-chip SSIF • AK4353 (Asahi Kasei EMD Corporation): 1 • 96 kHz 24-bit D/A converter, on-chip digital audio transmitter • Sampling frequency: 16 kHz to 96 kHz • Stereo pin jack: 1 • Optical connector: 1
4	PWM	Connected to the SH7267 on-chip Motor Control PWM timer pin Note: This module cannot be used with the R0K572670C000BR. • MIL-spec connector for PWM timer output: 1 (20-pin)
5	Timer output	Controls the LED brightness by the PWM mode in the SH7267 on-chip MTU2 • MIL-spec connector for timer output: 1 (20-pin)
6	SD card interface	Accesses the SD card by the SH7267 on-chip SDHI • SD card slot: 1 • Includes a card power control IC (Software control NOT allowed)
7	CAN	CAN communication by the SH7267 on-chip CAN (RCAN-TL1) • HA13721FP (Renesas CAN driver IC), includes a voltage level shifter
8	IEBus™	IEBus™ communication by the SH7267 on-chip IEBus controller (IEB) • HA12187FP (Renesas IEBus driver IC), includes a voltage level shifter
9	IIC	Connected to the SH7267 on-chip IIC bus interface (IIC3) pin • MIL-spec connector for connecting an external IIC interface: 1 (20-pin)
10	Switches	Key input by the SH7267 on-chip ADC • Key input switches: 16 (4 switches x 4 inputs)
11	Board specifications	• Dimensions: 210 mm x 148 mm • Mounting form: 4 layers, double-sided • Board thickness: 1.6 mm • Number of boards: 1

1.14 M3A-HS64G02 Exterior

The following figure shows the exterior of the M3A-HS64G02.

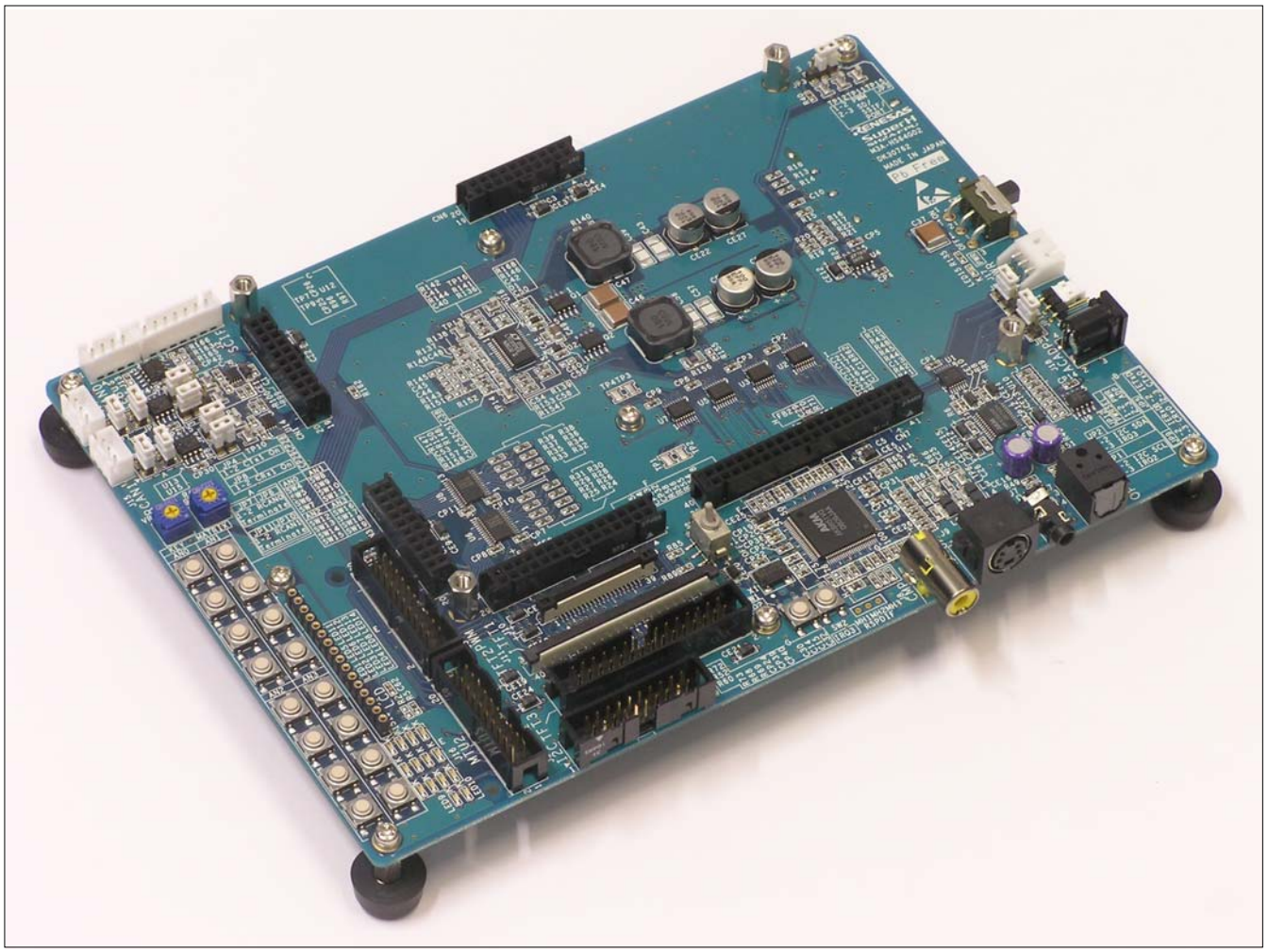


Figure 1.14.1 M3A-HS64G02 Exterior

1.15 M3A-HS64G02 Block Diagram

The following figure shows the block diagram of the M3A-HS64G02.

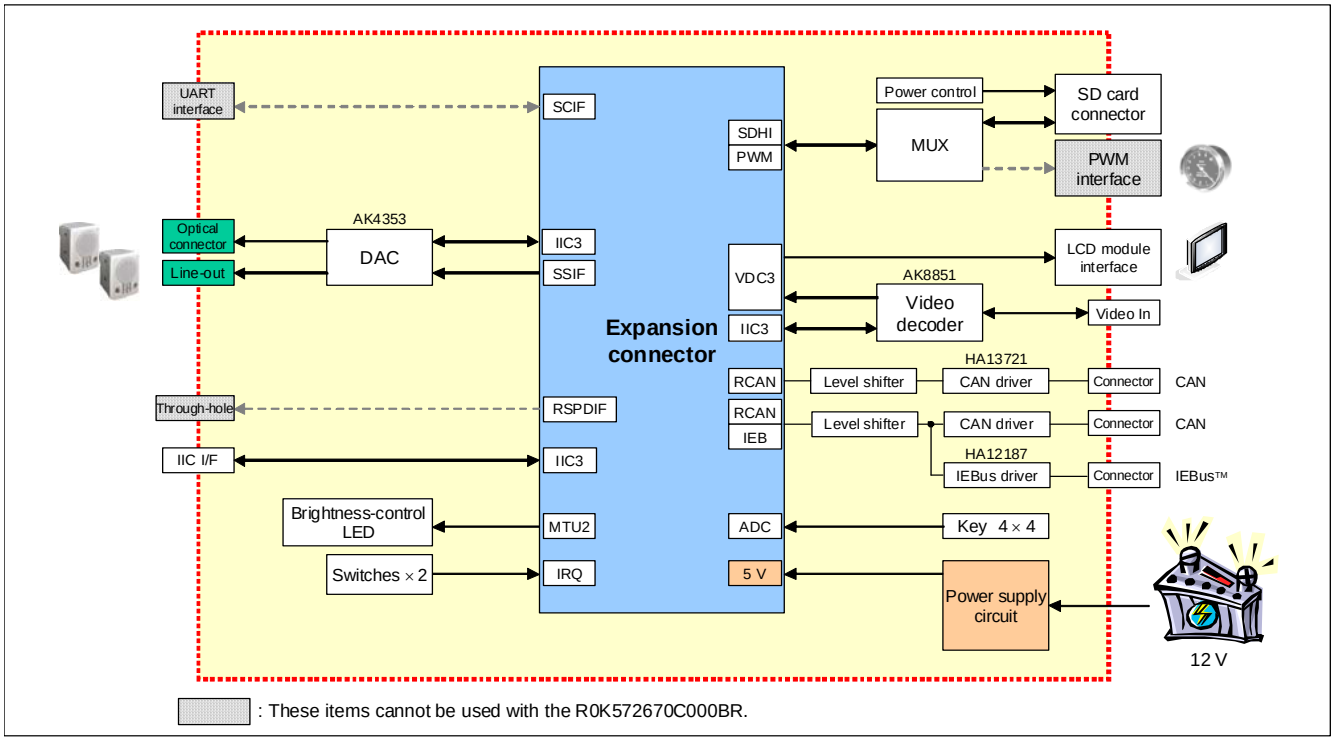


Figure 1.15.1 M3A-HS64G02 Block Diagram

1.16 M3A-HS64G02 Major Components

The following figure shows the M3A-HS64G02 layout and locations of the major components (PCB drawing).

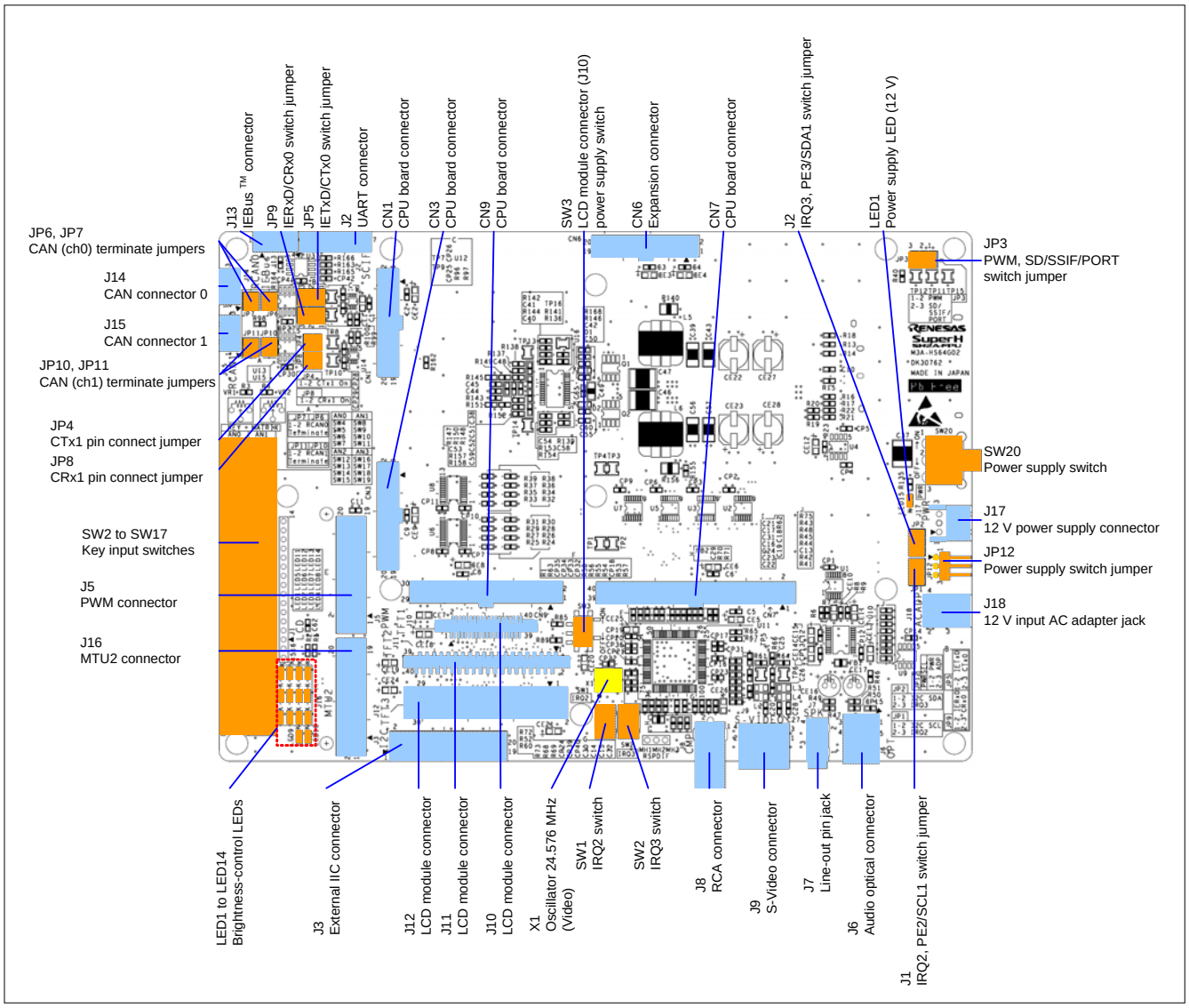


Figure 1.16.1 M3A-HS64G02 Layout and Component Placement (Top View of the Component Side)

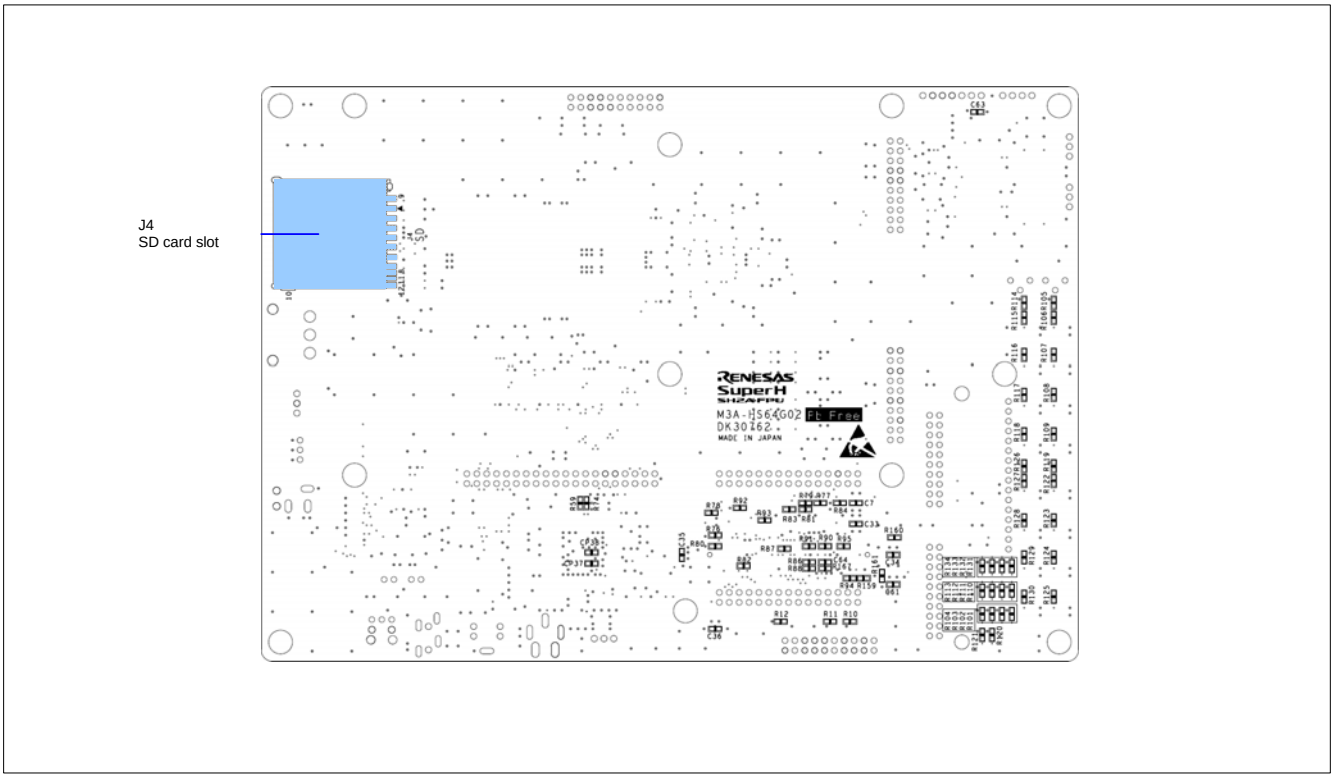


Figure 1.16.2 M3A-HS64G02 Layout and Component Placement (Top View of the Solder Side)

Table 1.16.1 and Table 1.16.2 list the major components on the M3A-HS64G02.

Table 1.16.1 Major Components - ICs (1/2)

No	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	Character LCD module	SD1602H	SUNLIKE	16 characters x 2 lines	1
2	Video decoder	AK8851VQ	AKM	Supports NTSC/PAL/SECAM	1
3	D/A converter	AK4353VF	AKM	96 kHz, 24-bit D/A converter	1
4	CAN drivers	HA13721FP	Renesas		2
5	IEBus™ driver	HA12187FP	Renesas		1
6	Adjustable regulator	LTC3727EG	LT	8 V/5 V	1
7	Multiplexers	SN74CB3Q3257DBQR	TI	Analog switch	4

Table 1.16.2 Major Components -Connectors (2/2)

No	Name	Part Number	Manufacturer Name	Remarks	Qty per board
1	20-pin expansion connectors	XG4C-2031	OMRON	20-pin MIL-spec connector	3
2	30-pin expansion connector	XG4C-3031	OMRON	30-pin MIL-spec connector	1
3	40-pin expansion connector	XG4C-4031	OMRON	40-pin MIL-spec connector	1
4	SD card slot	DM1B-DSF-PEJ	HRS	Reverse type	1
5	Audio optical connector	TOTX147PL	TOSHIBA		1
6	UART connector	B7B-XH-A	J.S.T	TTL level	1
7	External IIC connector	XG4C-2031	OMRON	20-pin MIL-spec connector	1
8	LCD module connector 1 (J10)	IMSA-9639S-40D	IRISO	0.5 mm pitch FFC, for TX09D55VM1CDA only	1
9	LCD module connector 2 (J11)	IMSA-9619S-40B	IRISO	1 mm pitch FFC, for TX09D14VM3CCA only	1
10	LCD module connector 3 (J12)	XG4C-3031	OMRON	30-pin MIL-spec connector Multi-purpose	1
11	IEBus™ connector	B4B-XH-A	J.S.T	2.5 mm pitch	1
12	CAN connectors	B3B-XH-A	J.S.T	2.5 mm pitch	2
13	PWM connector	XG4C-2031	OMRON	20-pin MIL-spec connector	1
14	MTU2 connector	XG4C-2031	OMRON	20-pin MIL-spec connector	1

1.17 Memory Maps

The following figure shows memory map examples of the SH7267 and the R0K572670C000BR.

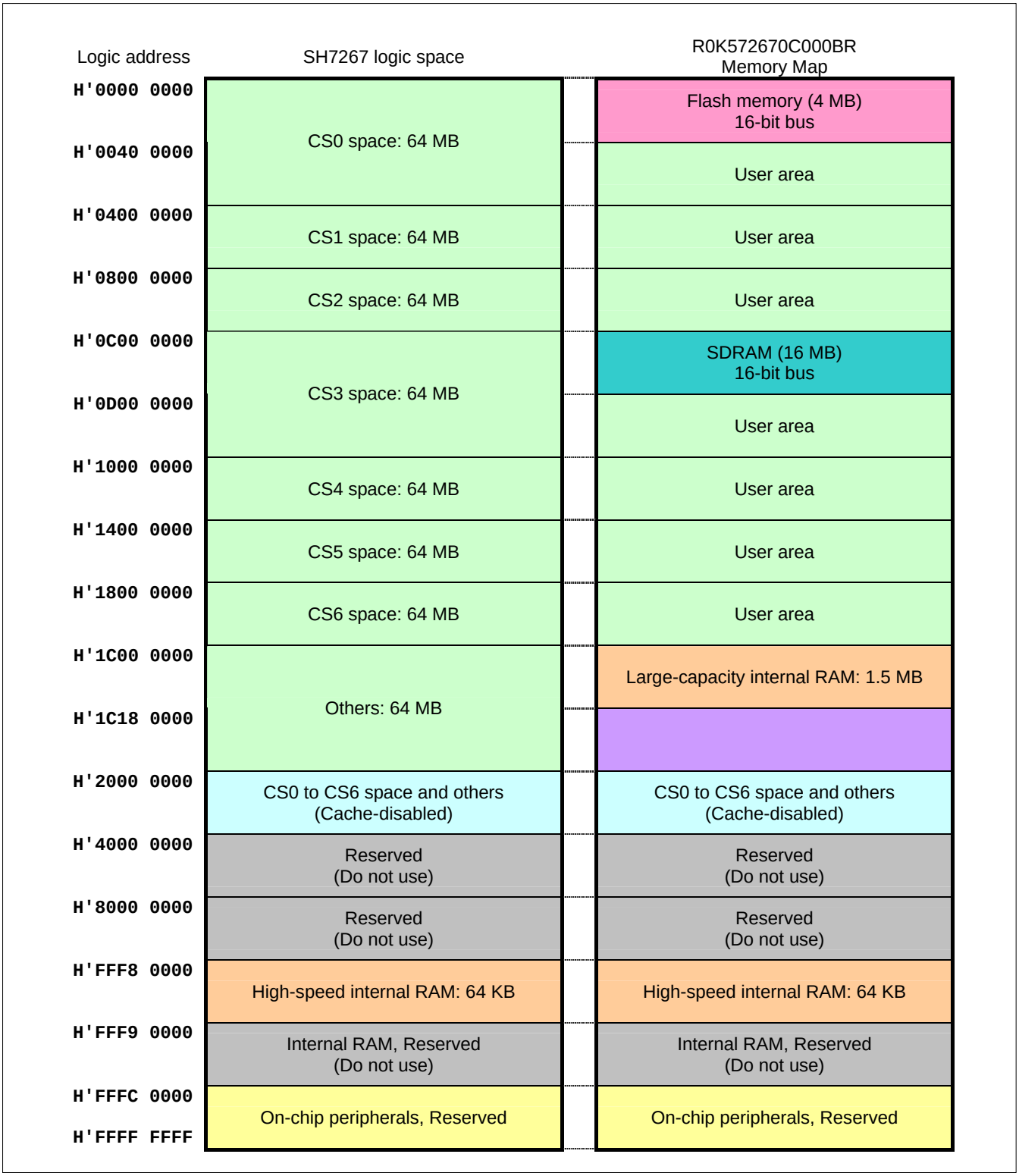


Figure 1.17.1 SH7267 and the R0K572670C000BR Memory Map Example

1.18 Absolute Maximum Ratings

Table 1.18.1 and Table 1.18.2 list the absolute maximum ratings of the R0K572670C000BR, and its optional boards.

Table 1.18.1 Absolute Maximum Ratings on the R0K572670C000BR

Symbol	Parameter	Value	Remarks
VCC	5 V system power supply voltage	-0.3 to 6.0 V	Reference voltage: VSS
3VCC	3.3 V system power supply voltage	-0.3 to 4.6 V	Reference voltage: VSS
1.2VCC	1.25 V system power supply voltage	-0.3 to 1.7 V	Reference voltage: VSS
Topr	Operating ambient temperature	-10 to 55°C	Do not expose to condensation or corrosive gas
Tstr	Storage ambient temperature	-20 to 60°C	Do not expose to condensation or corrosive gas

Note: Ambient temperature refers to the air temperature in the vicinity of the board.

Table 1.18.2 Absolute Maximum Ratings on the SH7267 Optional Boards

Symbol	Parameter	Value	Remarks
12VCC	12 V system power supply voltage	-0.3 to 15.0 V	Reference voltage: VSS
8VCC	8 V system power supply voltage	-0.3 to 10.0 V	Reference voltage: VSS
5VCC	5 V system power supply voltage	-0.3 to 6.0 V	Reference voltage: VSS
3VCC	3.3 V system power supply voltage	-0.3 to 4.6 V	Reference voltage: VSS
Topr	Operating ambient temperature	-10°C to 55°C	Do not expose to condensation or corrosive gas
Tstr	Storage ambient temperature	-20°C to 60°C	Do not expose to condensation or corrosive gas

Note: Ambient temperature refers to the air temperature in the vicinity of the board.

1.19 Operating Conditions

Table 1.19.1 and Table 1.19.2 list the operating conditions of the R0K572670C000BR, and its optional boards.

Table 1.19.1 R0K572670C000BR Operating Conditions

Symbol	Parameter	Value	Remarks
VCC	5 V system power supply voltage	4.75 to 5.25 V	Reference voltage: VSS
3VCC	3.3 V system power supply voltage	3.0 to 3.6 V	Reference voltage: VSS
1.2VCC	1.25 V system power supply voltage	1.15 to 1.35 V	Reference voltage: VSS
-	Maximum current consumption	1.5 A max.	
Topr	Operating ambient temperature	0°C to 40°C	Do not expose to condensation or corrosive gas

Table 1.19.2 SH7267 Optional Boards Operating Conditions

Symbol	Parameter	Value	Remarks
12VCC	12 V system power supply voltage	11.4 to 12.6 V	Reference voltage: VSS
8VCC	8 V system power supply voltage	7.6 to 8.4 V	Reference voltage: VSS
VCC	5 V system power supply voltage	4.75 to 5.25 V	Reference voltage: VSS
3VCC	3.3 V system power supply voltage	3.0 to 3.6 V	Reference voltage: VSS
-	Maximum current consumption	3 A max.	Includes the R0K572670C000BR
Topr	Operating ambient temperature	0°C to 40°C	Do not expose to condensation or corrosive gas

1.20 Usage Note

This section describes usage note the SH7267 CPU board and optional boards.

1.20.1 Configuring Unused Pins

Set the SH7267 unused (unconnected) multiplexed pins to output when not connecting the optional board with the SH7267 CPU board. Port H requires external resistors (R11 to R16) or must be set to an analog input.

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Chapter 2
R0K572670C000BR Functions

2.1 Overview of Functions

R0K572670C000BR includes the function modules listed in the following table.

Table 2.1.1 R0K572670C000BR Function Modules

Section	Function	Description
2.2	CPU	• SH7267
2.3	Memory	• Connects the SH7267 external bus interface and an NOR flash memory - SH7267 Bus State Controller (BSC) recommended setting - Access timing example • Connects the SH7267 external bus interface and an SDRAM - SH7267 BSC recommended setting - Access timing example • Connects the SH7267 NAND flash memory controller (FLCTL) and NAND flash memory • Connects the SH7267 Renesas Serial Peripheral Interface (RSPI) and serial flash memory • Connects the SH7267 IIC bus interface 3 (IIC3) and an EEPROM
2.4	USB Interface	• Connects the SH7267 USB 2.0 Host/function module and a USB connector
2.5	RS-232C Interface	• Connects the SH7267 Serial Communication Interface with FIFO (SCIF) and an RS-232C connector
2.6	I/O Ports	• Connect the SH7267 I/O ports, LEDs, and DIP switches
2.7	Interrupt Switches	• Connects the SH7267 NMI pin, IRQ1 pin and push-button switches
2.8	Clock Modules	• Controls the system clock • Controls the peripheral I/O clock
2.9	Reset Module	• Resets devices on the R0K572670C000BR
2.10	Power Supply Module	• Controls the R0K572670C000BR system power supply
2.11	E10A-USB Interface	• Connects the SH7267 user debug interface and an H-UDI port connector
-	Operating Specifications	• Connectors, switches, and LEDs Refer to Chapter 5 for details.

2.2 CPU

2.2.1 SH7267 Overview

The R0K572670C000BR includes the SH7267, the 32-bit RISC MCU that operates with a maximum frequency of 144 MHz.

2.2.2 SH7267 Pin Functions Used on the R0K572670C000BR

Table 2.2.1 to Table 2.2.5 list the SH7267 pin functions used on the R0K572670C000BR.

Table 2.2.1 SH7267 Pin Functions (1/5)

No.	Name	Symbol	Description	Expansion connector	Remarks
1	PVcc				
2	PG18/LCD_DE/TIOC2A/RxD3/ RTS1	–	–	CN9, pin 24	
3	Vss				
4	PB1/A1/LCD_HSYNC	A1	Address bus	CN4, pin 1	
5	Vcc				
6	PB2/A2/LCD_VSYNC	A2	Address bus	CN4, pin 2	
7	PB3/A3/LCD_DATA15	A3	Address bus	CN4, pin 3	
8	PB4/A4/TIOC0A/LCD_DATA14	A4	Address bus	CN4, pin 4	
9	PG9/LCD_DATA9/SSIRxD0/ TxD4/SIOFSYNC	–	–	CN9, pin 11	
10	PVcc				
11	PG8/LCD_DATA8/SSITxD0/ RxD4/SIOFSCK	–	–	CN9, pin 12	
12	Vss				
13	PB5/A5/TIOC0B/LCD_DATA13	A5	Address bus	CN4, pin 5	
14	PB6/A6/TIOC0C/LCD_DATA12	A6	Address bus	CN4, pin 6	
15	PB7/A7/TIOC0D/LCD_DATA11	A7	Address bus	CN4, pin 9	
16	PB8/A8/TIOC1A/LCD_DATA10	A8	Address bus	CN4, pin 10	
17	PVcc				
18	PB9/A9/TIOC1B/LCD_DATA9	A9	Address bus	CN4, pin 11	
19	Vss				
20	PB10/A10/TIOC2A/LCD_DATA8	A10	Address bus	CN4, pin 12	
21	Vcc				
22	PB11/A11/TIOC2B/LCD_DATA7	A11	Address bus	CN4, pin 13	
23	PB12/A12/TIOC3A/LCD_DATA6	A12	Address bus	CN4, pin 14	
24	PB13/A13/TIOC3B/LCD_DATA5	A13	Address bus	CN4, pin 17	
25	PB14/A14/TIOC3C/LCD_DATA4	A14	Address bus	CN4, pin 18	
26	PB15/A15/TIOC3D/LCD_DATA3	A15	Address bus	CN4, pin19	
27	PG7/LCD_DATA7/SD_CD/PINT7/ IRQ7	–	–	CN9, pin 9	
28	PG6/LCD_DATA6/SD_WP/PINT6/ IRQ6	–	–	CN9, pin 7	
29	PVcc				
30	PG5/LCD_DATA5/SD_D1/PINT5/ IRQ5	–	–	CN9, pin 8	
31	Vss				
32	PG4/LCD_DATA4/SD_D0/PINT4/ IRQ4	–	–	CN9, pin 6	

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 2.2.2 SH7267 Pin Functions (2/5)

No.	Name	Symbol	Description	Expansion connector	Remarks
33	Vcc				
34	PB16/A16/TIOC4A/LCD_DATA2	A16	Address bus	CN4, pin 20	
35	PB17/A17/TIOC4B/LCD_DATA1/ SCK1	A17	Address bus	CN4, pin 21	
36	PB18/A18/TIOC4C/LCD_DATA0/ TxD1	A18	Address bus	CN4, pin 22	
37	PB19/A19/TIOC4D/RxD1	A19	Address bus	CN4, pin 25	
38	PB20/A20/SPDIF_IN/SCK4	A20	Address bus	CN4, pin 26	
39	PB21/A21/SPDIF_OUT/TxD4	A21	Address bus	CN4, pin 27	
40	PVcc				
41	CKIO	CKIO	Connected to the SDRAM CLK pin	CN6, pin 20	
42	Vss				
43	PB22/A22/CS4#/RxD4	PB22	Switches the system setting/user interface	CN4, pin 28	Low: MD High: IO
44	NMI	NMI	Non-maskable interrupt	–	
45	PLLVcc				
46	RES#	RES#	Reset input	CN7, pin 6	
47	PLLVss				
48	PA0/MD_CLK0	PA0	Connected to LED2 as a user output port	CN1, pin 10	PB22: High
		MD_CLK0	Connected to SW5-1 as clock mode input 0		PB22: Low
49	PA1/MD_BOOT0	PA1	Connected to LED3 as a user output port	CN1, pin 9	PB22: High
		MD_BOOT0	Connected to SW5-2 as boot mode input 0		PB22: Low
50	EXTAL	EXTAL	Connects system external clock to MCU	–	12 MHz
51	XTAL	XTAL	Open	–	
52	PG3/LCD_DATA3/SD_CLK/ PINT3	–	–	CN9, pin 3	
53	PG2/LCD_DATA2/SD_CMD/ PINT2	–	–	CN9, pin 4	
54	PG1/LCD_DATA1/SD_D3/PINT1	–	–	CN9, pin 1	
55	PG0/LCD_DATA0/SD_D2/PINT0	–	–	CN9, pin 2	
56	Vss				
57	PVcc				
58	PG20/LCD_EXTCLK/SCK1	LCD_EXTCLK	Connects the LCD module external clock to MCU	CN9, pin 26	Default: 5.33 MHz
59	Vss				
60	RTC_X1	RTC_X1	Connects the real-time clock resonator to MCU	–	32.768 kHz
61	RTC_X2	RTC_X2		–	
62	PA2/MD_BOOT1	PA2	Connected to SW6-5 as a user input port	CN1, pin 8	PB22: High
		MD_BOOT1	Connected to SW5-3 as boot mode input 1	–	PB22: Low
63	USB_X1	USB_X1	Connects the USB external clock to MCU	–	48 MHz
64	USB_X2	USB_X2	Open	–	
65	ASEMD#	ASEMD#	ASE mode select	–	H-UDI
66	USBDPVcc				
67	USBDPVss				
68	DM	DM	USB differential signal D− data	–	
69	DP	DP	USB differential signal D+ data	–	
70	VBUS	VBUS	VBUS input	–	
71	USBDVcc				
72	USBDVss				
73	REFRIN	REFRIN	Reference input	–	Connects a 5.6 kΩ ± 1% resistor
74	USBAPVss				

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 2.2.3 SH7267 Pin Functions (3/5)

No.	Name	Symbol	Description	Expansion connector	Remarks
75	USBAPVcc				
76	USBAVcc				
77	USBAVss				
78	USBUVcc				
79	USBUVss				
80	PH0/AN0	–	–	CN3, pin 4	
81	PH1/AN1	–	–	CN3, pin 3	
82	PH2/AN2	–	–	CN3, pin 8	
83	PH3/AN3	–	–	CN3, pin 7	
84	AVss				
85	PH4/AN4	–	–	CN1, pin 2	
86	AVref				
87	PH5/AN5	–	–	CN1, pin 4	
88	AVcc				
89	TRST#	TRST#	Initialize-signal input pin	–	H-UDI
90	ASEBRKAK#/ASEBRK#	ASEBRKAK#	Break mode acknowledge	–	H-UDI
		ASEBRK#	Break request		
91	TDO	TDO	Test data output	–	H-UDI
92	TDI	TDI	Test data input	–	H-UDI
93	TMS	TMS	Test mode select	–	H-UDI
94	TCK	TCK	Test clock	–	H-UDI
95	AUDIO_X2	AUDIO_X2	Open	–	
96	AUDIO_X1	AUDIO_X1	Connects the audio external clock to MCU	–	Switched by JP9
97	PG24/MISO1/TIOC0D	–	–	CN6, pin 13	
98	PVcc				
99	PG23/MOSI1/TIOC0C	–	–	CN6, pin 12	
100	Vss				
101	PG22/SSL10/TIOC0B	–	–	CN9, pin 27	
102	Vcc				
103	PG21/RSPCK1/TIOC0A	–	–	CN9, pin 28	
104	PJ3/CRx1/CRx0/CRx1/IRQ1/ AUDIO_XOUT/WDTOVF#	IRQ1	IRQ1 switch	–	JP8: 1-2
		–	–	CN1, pin 17	JP8: 2-3
105	PJ2/CTx1/CTx0&CTx1/CS2#/ SCK0/LCD_M_DISP	–	–	CN1, pin 18	
106	PJ1/CRx0/IERxD/IRQ0/RxD0	RxD0	Connected to the RS-232C connector (J10)	–	JP5: 1-2
		–	–	CN1, pin 19	JP5: 2-3
107	PJ0/CTx0/IETxD/CS1#/TxD0/ A0	TxD0	Connected to the RS-232C connector (J10)	–	JP4: 1-2
		–	–	CN1, pin 20	JP4: 2-3
108	PF8/CE2B#/SSIDATA2/DV_CLK/ SD_CD	–	–	CN7, pin 27	SW6-6: ON
				CN7, pin 15	SW6-6: OFF
109	PF7/CE2A#/SSIWS2/DV_DATA7/ TCLKD/SD_WP	–	–	CN7, pin 28	SW6-6: ON
				CN7, pin 16	SW6-6: OFF
110	PVcc				
111	PF6/CS6#/CE1B#/SSISCK2/ DV_DATA6/TCLKB/SD_D1	–	–	CN7, pin 25	SW6-6: ON
				CN7, pin 13	SW6-6: OFF
112	Vss				
113	PF5/CS5#/CE1A#/SSIDATA1/ DV_DATA5/TCLKC/SD_D0/ AUDATA3	AUDATA3	Connected to the H-UDI port connector (J3)	CN7, pin 23	AUD
		–	–		SW6-6: ON
				CN7, pin 14	SW6-6: OFF
114	Vcc				

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 2.2.4 SH7267 Pin Functions (4/5)

No.	Name	Symbol	Description	Expansion connector	Remarks
115	PF4/ICIOWR#/AH#/SSIWS1/ DV_DATA4/TxD3/SD_CLK/ AUDATA2	AUDATA2	Connected to the H-UDI port connector (J3)	CN7, pin 24	AUD
		–	–		SW6-6: ON
				CN7, pin 3	SW6-6: OFF
116	PF3/ICIORD#/SSISCK1/ DV_DATA3/RxD3/SD_CMD/ AUDATA1	AUDATA1	Connected to the H-UDI port connector (J3)	CN7, pin 22	AUD
		–	–		SW6-6:ON
				CN7, pin 4	SW6-6:OFF
117	PF2/BACK#/DV_DATA2/TxD2/ DACK0/SD_D3/AUDATA0	AUDATA0	Connected to the H-UDI port connector (J3)	CN7, pin 19	AUD
		–	–		SW6-6: ON
				CN7, pin 1	SW6-6: OFF
118	PF1/BREQ#/DV_DATA1/RxD2/ DREQ0/SD_D2/AUDSYNC#	AUDSYNC#	Connected to the H-UDI port connector (J3)	CN7, pin 20	AUD
		–	–		SW6-6: ON
				CN9, pin 29	
				CN7, pin 2	SW6-6: OFF
119	PF0/WAIT#/DV_DATA0/SCK2/ TEND0/AUDCK	AUDCK	Connected to the H-UDI port connector (J3)	CN7, pin 17	AUD
		–	–		
				CN7, pin 32	
120	PVcc				
121	PG17/LCD_HSYNC/TIOC1B/ TxD1	–	–	CN9, pin 21	
122	Vss				
123	PG16/LCD_VSYNC/TIOC1A/ RxD1	–	–	CN9, pin 19	
124	PF12/BS#/MISO0/TIOC3D/ SPDIF_OUT	MISO0	Connected to the serial flash memory SO pin	CN7, pin 33	SW5-6: OFF
		–	–		
				CN7, pin 38	SW5-6: ON
125	PF11/A25/SSIDATA3/MOSI0/ TIOC3C/SPDIF_IN	MOSI0	Connected to the serial flash memory SI pin	CN7, pin 31	SW5-6: OFF
		–	–		
				CN7, pin 37	SW5-6: ON
126	PVcc				
127	PF10/A24/SSIWS3/SSL00/ TIOC3B/FCE#	SSL00	Connected to the serial flash memory CS# pin	–	SW5-5: ON SW5-6: OFF
		–	–	CN7, pin 35	SW5-5: ON SW5-6: ON
		FCE#	Connected to the NAND flash memory CE# pin	–	SW5-5: OFF
128	Vss				
129	PF9/A23/SSISCK3/RSPCK0/ TIOC3A/FRB	RSPCK0	Connected to the serial flash memory SCK pin	CN7, pin 30	SW5-5: ON SW5-6: OFF
		–	–		
				CN7, pin 36	SW5-5: ON SW5-6: ON
		FRB	Connected to the NAND flash memory R/B# pin	–	SW5-5: OFF
130	Vcc				
131	PD15/D15/NAF7/PWM2H	D15/NAF7	Data bus	CN8, pin 19	
132	PD14/D14/NAF6/PWM2G	D14/NAF6	Data bus	CN8, pin 17	
133	PE5/SDA2/DV_HSYNC	–	–	CN7, pin 12	
134	PE4/SCL2/DV_VSYNC	–	–	CN7, pin 9	
135	PE3/SDA1/IRQ3	SDA1	Connected to the EEPROM SDA pin	CN7, pin 10	JP10: 1-2
		–	–		
136	PE2/SCL1/IRQ2	SCL1	Connected to the EEPROM SCL pin	CN7, pin 7	JP9: 1-2
		–	–		
137	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ ADTRG#/LCD_EXTCLK	–	–	CN7, pin 8	
138	PE0/SCL0/AUDIO_CLK/IRQ0	–	–	CN7, pin 5	

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 2.2.5 SH7267 Pin Functions (5/5)

No.	Name	Symbol	Description	Expansion connector	Remarks
139	PD13/D13/NAF5/PWM2F	D13/NAF5	Data bus	CN8, pin 14	
140	PD12/D12/NAF4/PWM2E	D12/NAF4	Data bus	CN8, pin 12	
141	PVcc				
142	PD11/D11/NAF3/PWM2D	D11/NAF3	Data bus	CN8, pin 9	
143	Vss				
144	PD10/D10/NAF2/PWM2C	D10/NAF2	Data bus	CN8, pin 7	
145	PD9/D9/NAF1/PWM2B	D9/NAF1	Data bus	CN8, pin 4	
146	PD8/D8/NAF0/PWM2A	D8/NAF0	Data bus	CN8, pin 2	
147	PD7/D7/FWE#/PWM1H	D7/FWE#	Connected to the data bus and the NAND flash memory WE# pin	CN8, pin 18	Auto-switch
148	PD6/D6/FALE/PWM1G	D6/FALE	Connected to the data bus and the NAND flash memory ALE pin	CN8, pin 16	Auto-switch
149	PD5/D5/FCLE/PWM1F	D5/FCLE	Connected to the data bus and the NAND flash memory CLE pin	CN8, pin 13	Auto-switch
150	PG15/LCD_DATA15/TIOC0D/ TxD7	–	–	CN9, pin 20	
151	PG14/LCD_DATA14/TIOC0C/ RxD7	–	–	CN9, pin 17	
152	PVcc				
153	Vss				
154	PG13/LCD_DATA13/TIOC0B/ TxD6	–	–	CN9, pin 18	
155	PG12/LCD_DATA12/TIOC0A/ RxD6	–	–	CN9, pin 16	
156	PD4/D4/FRE#/PWM1E	D4/FRE#	Connected to the data bus and the NAND flash memory RE# pin	CN8, pin 11	Auto-switch
157	PD3/D3/PWM1D	D3	Data bus	CN8, pin 8	
158	PD2/D2/PWM1C	D2	Data bus	CN8, pin 6	
159	PD1/D1/PWM1B	D1	Data bus	CN8, pin 3	
160	PD0/D0/PWM1A	D0	Data bus	CN8, pin 1	
161	PC0/CS0#/SSIWS0	CS0#	Connected to the NOR flash memory CE# pin	CN6, pin 5	
162	PVcc				
163	PC1/RD#/SSISCK0	RD#	Connected to the NOR flash memory OE# pin	CN6, pin 6	
164	Vss				
165	PC2/RD/WR#/SSIRxD0	RD/WR#	Connected to the SDRAM WE# pin	CN6, pin 7	
166	PC3/WE0#/DQML/SSITxD0	WE0#	Connected to the NOR flash memory WE# pin	CN6, pin 8	
		DQML	Connected to the SDRAM DQML pin		
167	PC4/WE1#/DQMU/WE#	DQMU	Connected to the SDRAM DQMU pin	CN6, pin 9	
168	PC5/RAS#/TIOC4A/IRQ4	RAS#	Connected to the SDRAM RAS# pin	–	SW5-4: OFF
		–	–	CN6, pin 14	SW5-4: ON
169	PG11/LCD_DATA11/SSIWS0/ IRQ3/TxD5/SIOFTxD	–	–	CN9, pin 13	
170	PVcc				
171	PG10/LCD_DATA10/SSISCK0/ IRQ2/RxD5/SIOFRxD	–	–	CN9, pin 14	
172	Vss				
173	PC6/CAS#/TIOC4B/IRQ5	CAS#	Connected to the SDRAM CAS# pin	–	SW5-4: OFF
		–	–	CN6, pin 15	SW5-4: ON
174	PC7/CKE/TIOC4C/IRQ6	CKE	Connected to the SDRAM CKE pin	–	SW5-4: OFF
		–	–	CN6, pin 16	SW5-4: ON
175	PC8/CS3#/TIOC4D/IRQ7	CS3#	Connected to the SDRAM CS# pin	–	SW5-4: OFF
		–	–	CN6, pin 17	SW5-4: ON
176	PG19/LCD_CLK/TIOC2B/TxD3/ CTS1	–	–	CN9, pin 23	

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

2.2.3 R0K572670C000BR Module Availability

The following table shows which combination of modules can/cannot be used.

Table 2.2.6 R0K572670C000BR Module Availability

				R0K572670C000BR												
	SH7267 Peripherals	Component No.	Module Name	NOR flash memory	SDRAM	NAND flash memory	EEPROM	Serial flash memory	USB	H-UDI (14-pin)	H-UDI (36-pin)	LED	NMI switch	IRQ1 switch	DIP switches	RS-232C
R0K572670C000BR	BSC	U6	NOR flash memory		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	BSC	U9	SDRAM	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	FLCTL	U7	NAND flash memory	Y	Y		Y	(2)	Y	Y	Y	Y	Y	Y	Y	Y
	IIC3	U8	EEPROM	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y
	RSPI	U10	Serial flash memory	Y	Y	(2)	Y		Y	Y	Y	Y	Y	Y	Y	Y
	USB	J1, J2	USB	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y
	H-UDI	J7	H-UDI (14-pin)	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y
	H-UDI, AUD	J3	H-UDI (36-pin)	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y
	I/O ports	LED2, LED3	LED	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	(1)	Y
	INTC	SW3	NMI switch	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y
	INTC	SW4	IRQ1 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y
	I/O ports	SW5, SW6	DIP switches	Y	Y	Y	Y	Y	Y	Y	Y	(1)	Y	Y		Y
	SCIF	J10	RS-232C	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	

Y: Yes

Notes:
1: When using LED2, and LED3, SW5-1, SW5-2, and SW5-3 on the R0K572670C000BR cannot be used.
2: PF9,and PF10 are multiplexed pins. When setting SW5-5, and SW5-6, either serial or NAND can be used.

2.2.4 SH7267 Multiplex Pins Used on the R0K572670C000BR

Table 2.2.7 to Table 2.2.13 list SH7267 multiplex pin functions used on the R0K572670C000BR.

These multiplex pins are set as port input pins by default. Set the MD bit in the port control register to use the SH7267 peripheral functions (except I/O ports).

Table 2.2.7 SH7267 Multiplex Pin Functions (BSC)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
BSC	CS0#	PCCR0	PC0MD[1:0] = B'01	PC0/CS0#/SSIWS0 (1)
	CS3#	PCCR2	PC8MD[1:0] = B'01	PC8/CS3#/TIOC4D/IRQ7
	RD#	PCCR0	PC1MD[1:0] = B'01	PC1/RD#/SSISCK0 (1)
	WE0#/DQML	PCCR0	PC3MD[1:0] = B'01	PC3/WE0#/DQML/SSITxD0
	WE1#/DQMU/WE#	PCCR1	PC4MD0 = B'1	PC4/WE1#/DQMU/WE#
	RAS#	PCCR1	PC5MD[1:0] = B'01	PC5/RAS#/TIOC4A/IRQ4
	CAS#	PCCR1	PC6MD[1:0] = B'01	PC6/CAS#/TIOC4B/IRQ5
	CKE	PCCR1	PC7MD[1:0] = B'01	PC7/CKE/TIOC4C/IRQ6
	RD/WR#	PCCR0	PC2MD[1:0] = B'01	PC2/RD/WR#/SSIRxD0
	A21	PBCR5	PB21MD[2:0] = B'001	PB21/A21/SPDIF_OUT/TxD4
	D15	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H (1)
	D14	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G (1)
	D13	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F (1)
	D12	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E (1)
	D11	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D (1)
	D10	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C (1)
	D9	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B (1)
	D8	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A (1)
	D7	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H (1)
	D6	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G (1)
	D5	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F (1)
	D4	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E (1)
	D3	PDCR0	PD3MD[1:0] = B'01	PD3/D3/PWM1D (1)
	D2	PDCR0	PD2MD[1:0] = B'01	PD2/D2/PWM1C (1)
	D1	PDCR0	PD1MD[1:0] = B'01	PD1/D1/PWM1B (1)
	D0	PDCR0	PD0MD[1:0] = B'01	PD0/D0/PWM1A (1)

Note 1: For boot modes 1 to 3

Table 2.2.8 SH7267 Multiplex Pin Functions (INTC)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
INTC	IRQ1	PJCR1	PJ3MD[2:0] = B'011	PJ3/CRx1/CRx0&CRx1/IRQ1/AUDIO_XOUT/WDTOVF#

Table 2.2.9 SH7267 Multiplex Pin Functions (SCIF)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
SCIF	RxD0	PJCR0	PJ1MD[2:0] = B'100	PJ1/CRx0/IERxD/IRQ0/RxD0
	TxD0	PJCR0	PJ0MD[2:0] = B'100	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 2.2.10 SH7267 Multiplex Pin Functions (IIC3)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
IIC3	SDA1	PECR0	PE3MD[1:0] = B'01	PE3/SDA1/IRQ3
	SCL1	PECR0	PE2MD[1:0] = B'01	PE2/SCL1/IRQ2

Table 2.2.11 SH7267 Multiplex Pin Functions (FLCTL)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
FLCTL	NAF7	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H
	NAF6	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G
	NAF5	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F
	NAF4	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E
	NAF3	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D
	NAF2	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C
	NAF1	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B
	NAF0	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A
	FWE#	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H
	FALE	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G
	FCLE	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F
	FRE#	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E
	FCE#	PFCR2	PF10MD[2:0] = B'101	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	FRB	PFCR2	PF9MD[2:0] = B'101	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 2.2.12 SH7267 Multiplex Pin Functions (RSPI)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
RSPI	MISO0	PFCR3	PF12MD[2:0] = B'011	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
	MOSI0	PFCR2	PF11MD[2:0] = B'011	PF11/A25/SSIDATA3/MOSI0/TIOC3C/SPDIF_IN
	SSL00	PFCR2	PF10MD[2:0] = B'011	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	RSPCK0	PFCR2	PF9MD[2:0] = B'011	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 2.2.13 SH7267 Multiplex Pin Functions (PORT)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
PORT	PB22	PBCR5	PB22MD[2:0] = B'000	PB22/A22/CS4#/RxD4

2.3 Memory

The R0K572670C000BR includes the SH7267 internal RAM, an external flash memory, an external SDRAM, and an external EEPROM.

2.3.1 SH7267 Internal RAM

The SH7267 includes 64 KB high-speed internal RAM that allows high-speed access to MCU, and 1.5 MB large-capacity internal RAM of which 128 KB is used for data retention.

2.3.2 NOR Flash Memory Interface

The R0K572670C000BR comes standard with an NOR flash memory listed in the table below to store the user program.
The NOR flash memory works at 16-bit mode, and 3.3 V-only single power supply. It is write-protected or write-enabled by system setting DIP switches. The figure below shows the NOR flash memory block diagram. Table 2.3.2 lists the DIP switches setting (SW6-1).

Table 2.3.1 NOR Flash Memory Specifications

Part Number	Bus Size	Capacity	Access Time
S29GL032N90TFI030	16-bit	4 MB (16-bit x 2 Mwords x 1)	90 ns

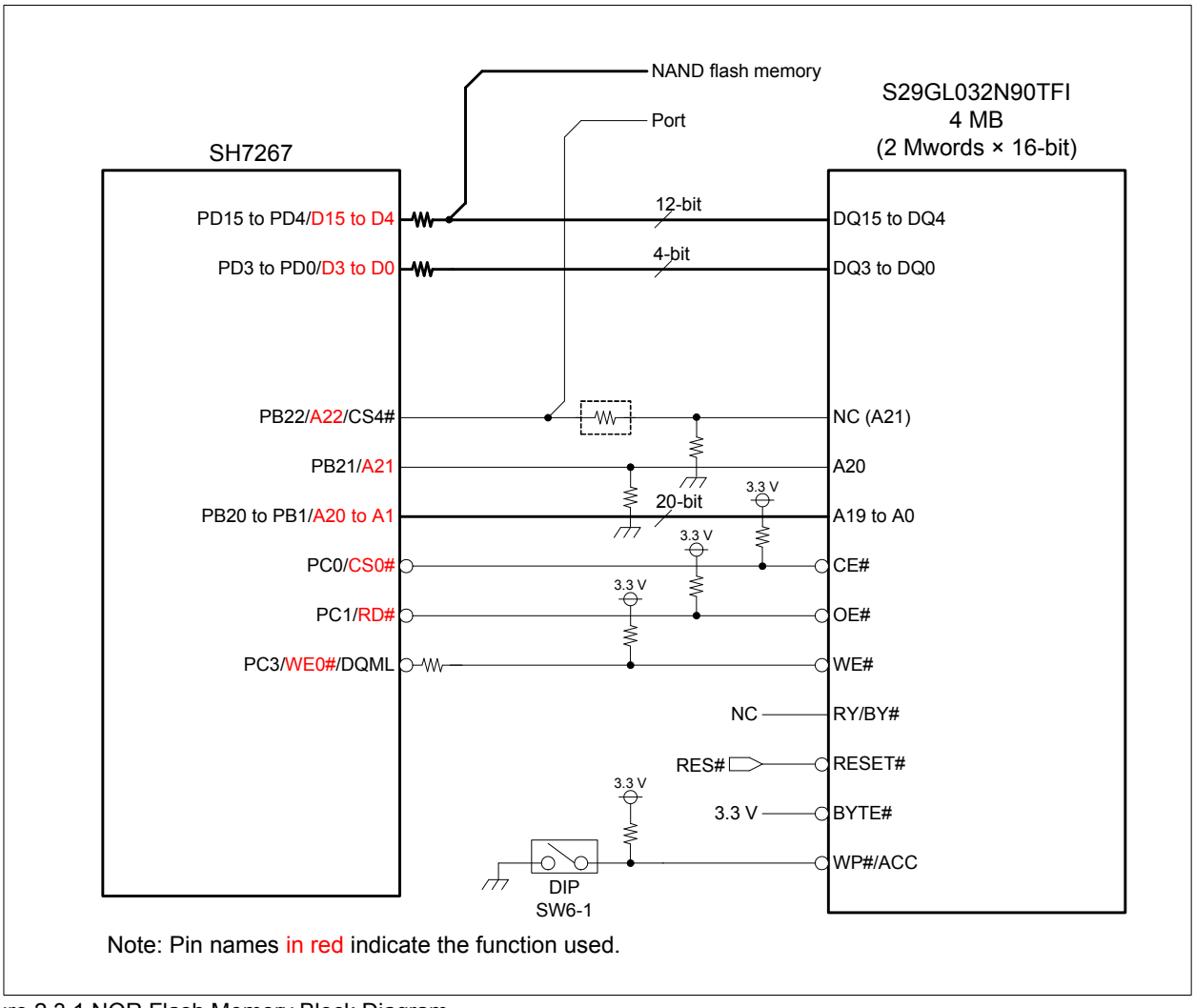

Figure 2.3.1 NOR Flash Memory Block Diagram

Table 2.3.2 DIP Switches Setting (SW6-1)

Number	Function	
	OFF (High)	ON (Low)
SW6-1	NOR flash memory is write-enabled (default)	NOR flash memory is write-protected

The figure below shows the write and read access timing example of the NOR flash memory. The table below lists the bus state controller settings (write/read) when the SH7267 bus clock works at 72 MHz.

Write and read timing

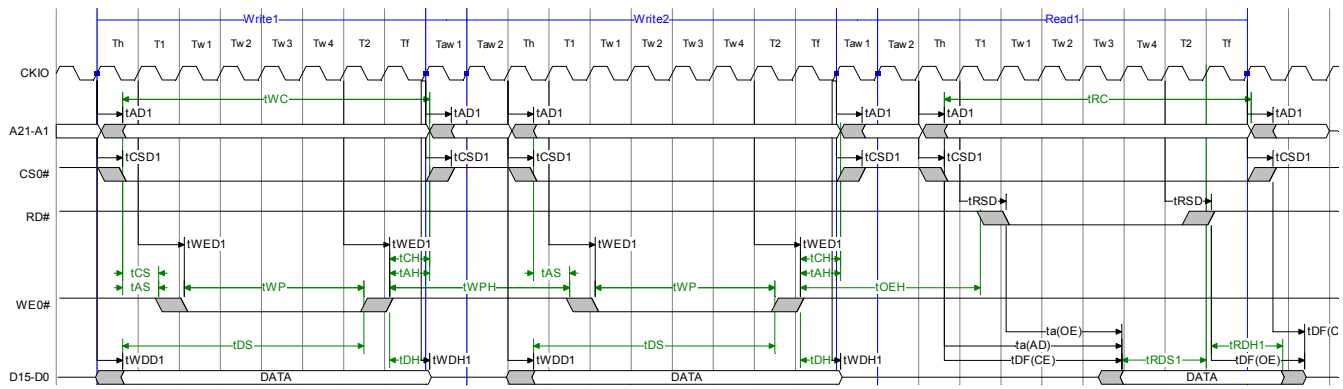

Figure 2.3.2 NOR Flash Memory write/read Access Timing Example

Table 2.3.3 Bus State Controller Setting (Write and read the NOR flash memory)

User area	Target Device	Setting
CS0	S29GL032N90TFI030	CS0 Space Bus Control Register (CS0BCR): Initial value: H'36DB 0400 (MD = Low) Recommended value: H'1240 0400 • Idle Cycles between Write-Read Cycles and Write-Write Cycles IWW [2:0] = B'001; 1 idle cycle inserted • Idle Cycles for Another Space Read-Write IWRWD [2:0] = B'001; 1 idle cycle inserted • Idle Cycles for Read-Write in the Same Space IWRWS [2:0] = B'001; 1 idle cycle inserted • Data bus width BSZ [1:0] = B'10; 16-bit CS0 Space Wait Control Register (CS0WCR): Initial value: H'0000 0500 Recommended value: H'0000 0B41 • Number of Delay Cycles from address, CS0# Assertion to RD#, WEn# Assertion: SW [1:0] = B'01; 1.5 cycles • Number of Access Wait Cycles WR [3:0] = B'0110; 6 cycles • External WAIT Mask Specification WM = B'1; Ignore external WAIT input • Number of Delay Cycles from RD#, WEn# Negation to address, CS0# Negation HW [1:0] = B'00; 0.5 cycles

2.3.3 External SDRAM Interface

The R0K572670C000BR comes standard with an SDRAM listed in the table below. The SDRAM is controlled by the SH7267 on-chip Bus State Controller (BSC). The R0K572670C000BR allows 16-bit bus access only.

The figure below shows the SDRAM block diagram, and Table 2.3.5 lists the DIP switches setting (SW5-4).

Table 2.3.4 SDRAM Specifications

Item	Description
Part number	EDS1216AATA-75E
Configuration	16 MB (Bus size: 16-bit) x 1
Capacity	16 MB
Access time	7.5 ns
CAS latency	2 (When the system clock works at 72 MHz)
Refresh	4096 cycles every 64 ms
Row address	A11 to A0
Column address	A8 to A0
Number of banks	4 (controlled by BA0, and BA1)

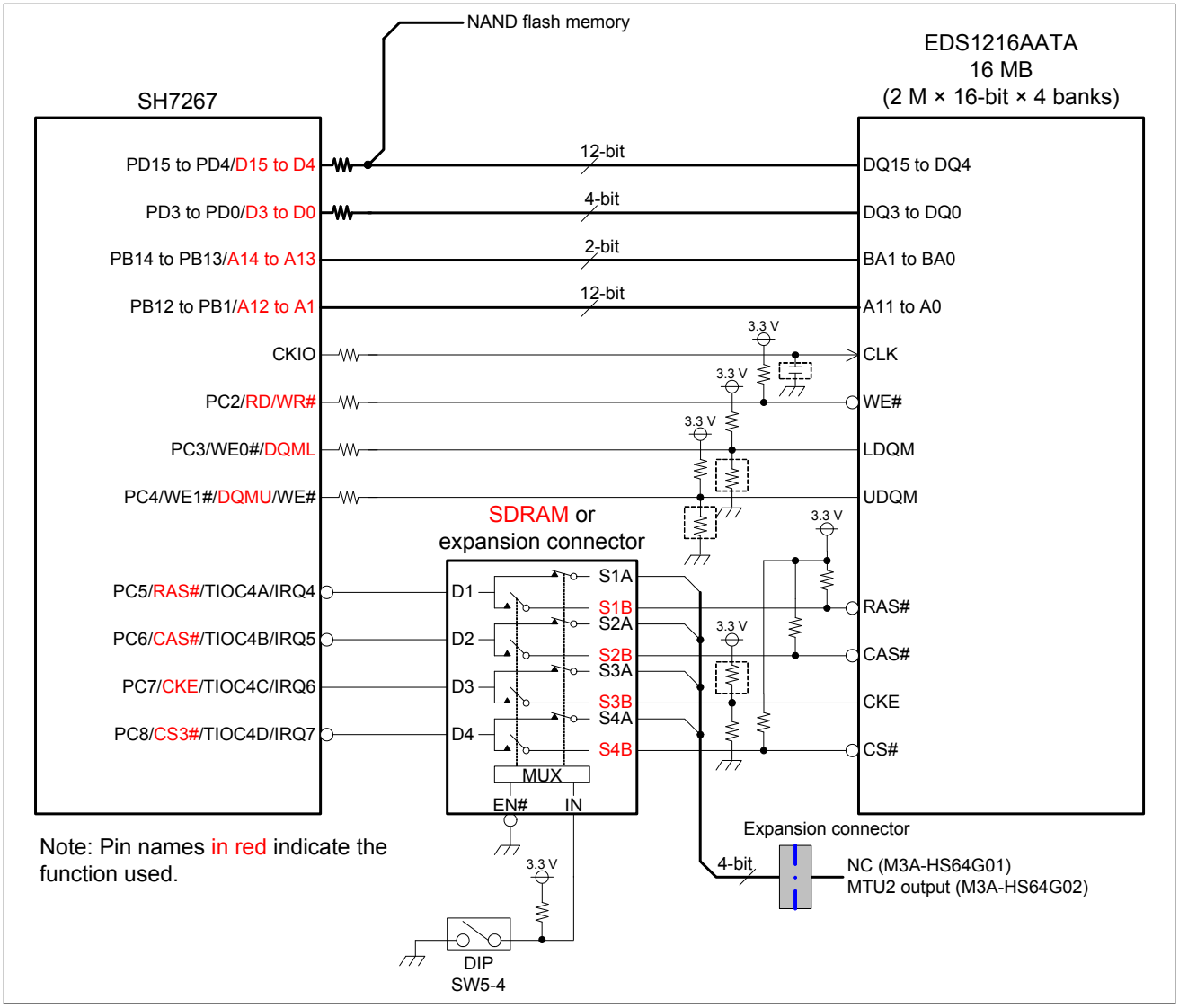

Figure 2.3.3 External SDRAM Block Diagram

Table 2.3.5 DIP Switches Setting (SW5-4)

Number	Function	
	OFF(High)	ON (Low)
SW5-4	Connected to the SDRAM (default)	Connected to the expansion connector

The following figure shows the single read and write timing example of the SDRAM. Table 2.3.6 lists the bus state controller setting when the SH7267 bus clock works at 72 MHz.

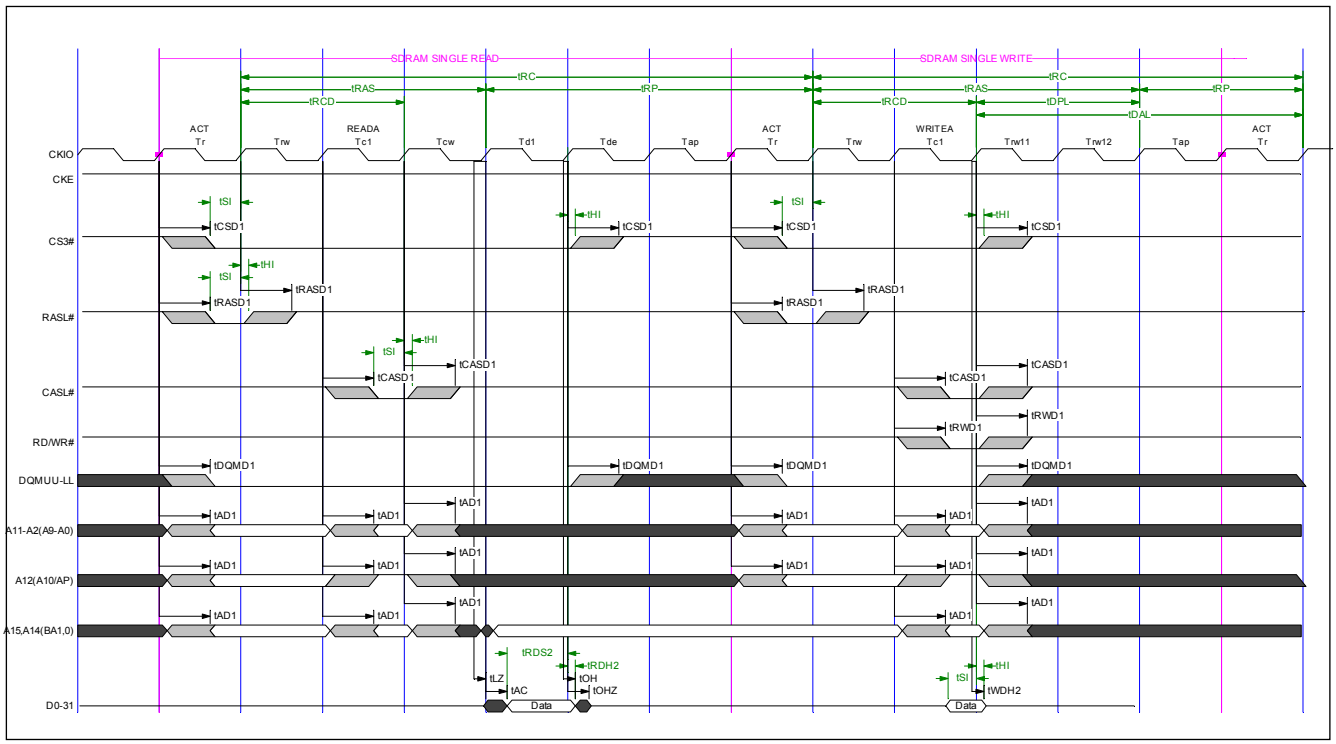

Figure 2.3.4 SDRAM Single Read/Write Timing Example

Table 2.3.6 Bus State Controller Setting (Read and Write the SDRAM)

User Area	Target Device	Setting
CS3	EDS1216AATA-75E	CS3 Space Bus Control Register (CS3BCR): Initial value: H'36DB 0400 Recommended value: H'0000 4400 • Memory TYPE [2:0] = B'100; SDRAM • Data bus width BSZ [1:0] = B'10; 16-bit CS3 Space Wait Control Register (CS3WCR): Initial value: H'0000 0500, Recommended value: H'0000 2892 • Number of Auto-Precharge Completion Wait Cycles: WTRP[1:0] = B'01; 1 cycle • Number of Wait Cycles between ACTV Command and READ (A)/WRIT(A) Command WTRCD [1:0] = B'10; 2 cycles • CAS Latency for Area 3 A3CL [1:0] = B'01; 2 cycles • Number of Auto-Precharge Startup Wait Cycles TRWL [1:0] = B'10; 2 cycles • Number of Idle Cycles from REF Command/Self-Refresh Release to ACTV/REF/MRS Command: WTRC [1:0] = B'10; 5 cycles SDRAM Control Register (SDCR): Initial value: H'0000 0000, Recommended value: H'0000 0809 • Refresh Control RFSH = B'1; SDRAM is refreshed • Refresh Control RMODE = B'0; Auto-refreshed • Bank Active Mode BACTV = B'0; Auto-precharge mode • Number of Bits of Row Address for Area 3 A3ROW [1:0] = B'01; 12 bits • Number of Bits of Column Address for Area 3 A3COL [1:0] = B'01; 9 bits Refresh Timer Control/Status Register (RTCSR): Initial value: H'0000 0000, Recommended value: H'A55A 0010 • Clock Select CKS [2:0] = B'010; BΦ/16 • Refresh Count RRC [2:0] = B'000; 1 time Refresh Time Constant Register (RTCOR): Initial value: H'0000 0000, Recommended value: H'A55A 0046 The refresh request interval when the clock select is set to BΦ/16 is as follows: 1 cycle: 222 nsec (72 MHz/16 = 4.5 MHz) Refresh request interval in this SDRAM: 15.625 µsec/time 15.625 µsec/222 nsec = 70 (0x46) cycles/refresh counts

2.3.4 NAND Flash Memory Interface

The R0K572670C000BR comes standard with an NAND flash memory listed in the table below.

NAND flash memory works at 8-bit mode, and 3.3 V-only single power supply. It is write-protected or write-enabled by system setting DIP switches.

The SH7267 NAND flash memory controller pin (FLCTL) is also used as the data bus (D15 to D4) and the channel 0 pin of the Renesas Serial Peripheral Interface (RSPI). When connecting it with NAND flash memory, set SW5-5 to OFF. The figure below shows the NAND flash memory block diagram. Table 2.3.8 lists the DIP switches setting (SW5-5, and SW6-2).

Table 2.3.7 NAND Flash Memory Specifications

Part Number	Bus Size	Capacity	Access Time
K9F2G08U0A-PCB0	8-bit	256 MB (8-bit x 256 Mwords x 1)	Random: 25 µs (max.) Page: 25 ns (min.)

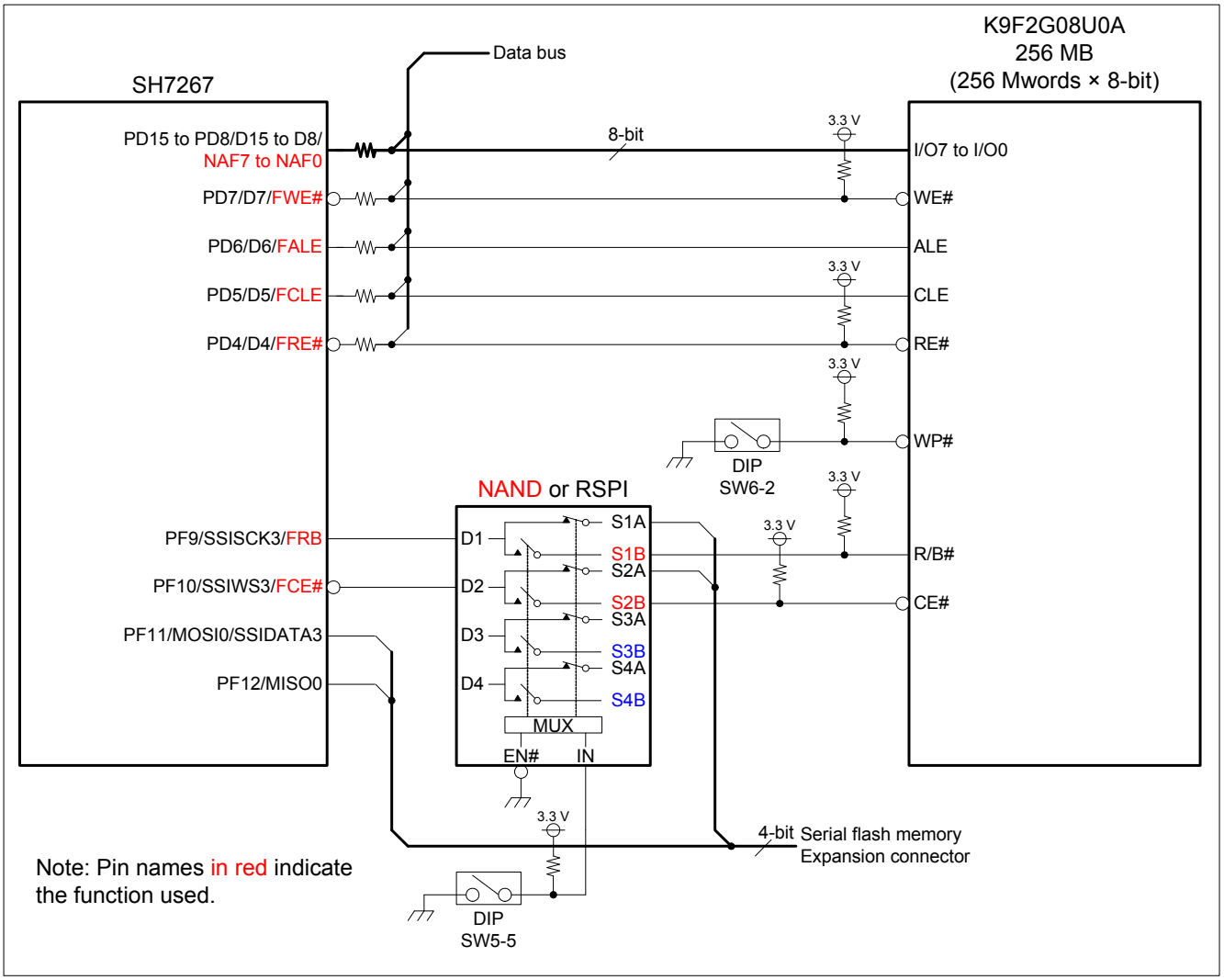

Figure 2.3.5 NAND Flash Memory Block Diagram

Table 2.3.8 DIP Switches Setting (SW5-5, and SW6-2)

Number	Function	
	OFF (High)	ON (Low)
SW5-5	Connected to the NAND flash memory	Connected to the device which is connected to RSPI/SSIF (default)
SW6-2	NAND flash memory is write-enabled (default)	NAND flash memory is write-protected

2.3.5 External Serial Flash Memory Interface

The R0K572670C000BR comes standard with a serial flash memory listed in the table below. The serial flash memory is controlled by the RSPI built in the SH7267.

The SH7267 RSPI channel 0 pin is also used as the FLCTL pin. When connecting it with serial flash memory, set SW5-5 to ON, and SW5-6 to OFF.

Serial flash memory is write-protected or write-enabled by the system setting DIP switches.

The figure below shows the serial flash memory block diagram. Table 2.3.10 lists the DIP switch setting (SW5, and SW6).

Table 2.3.9 Serial Flash Memory Specifications

Part Number	Interface	Capacity	Package
SST25VF016B-75	4-wire serial (RSPI)	2 MB	8-pin, SOP

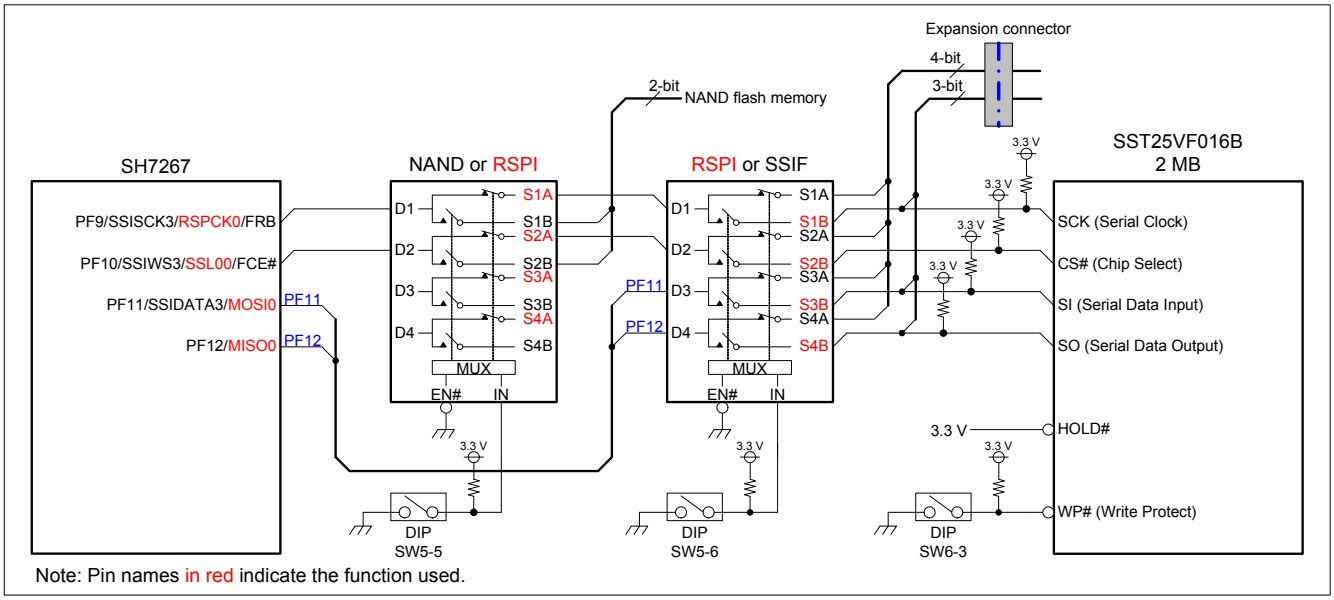

Figure 2.3.6 Serial Flash Memory Interface Block Diagram

Table 2.3.10 DIP Switches Setting (SW5, and SW6)

Number	Function	
	OFF (High)	ON (Low)
SW5-5	Connected to the NAND flash memory	Connected to the device which is connected to RSPI/SSIF (default)
SW5-6	Connected to the serial flash memory/ expansion connector (RSPI0)	Connected to the expansion connector (SSIF3) - default
SW6-3	Serial flash memory is write-enabled (default)	Serial flash memory is write-protected

2.3.6 External EEPROM Interface

The R0K572670C000BR comes standard with an EEPROM listed in the table below. The EEPROM is controlled by the IIC bus interface 3 (IIC3) built in the SH7267.

The EEPROM is write-protected or write-enabled by system setting DIP switches.

The figure below shows the EEPROM Interface Block Diagram. Table 2.3.12 lists the DIP switches setting (SW6-4).

Table 2.3.11 EEPROM Specifications

Part Number	Interface	Capacity	Package
R1EX24128ASA00A	2-wire serial (IIC)	16 KB (16 Kwords x 8-bit)	8-pin, SOP

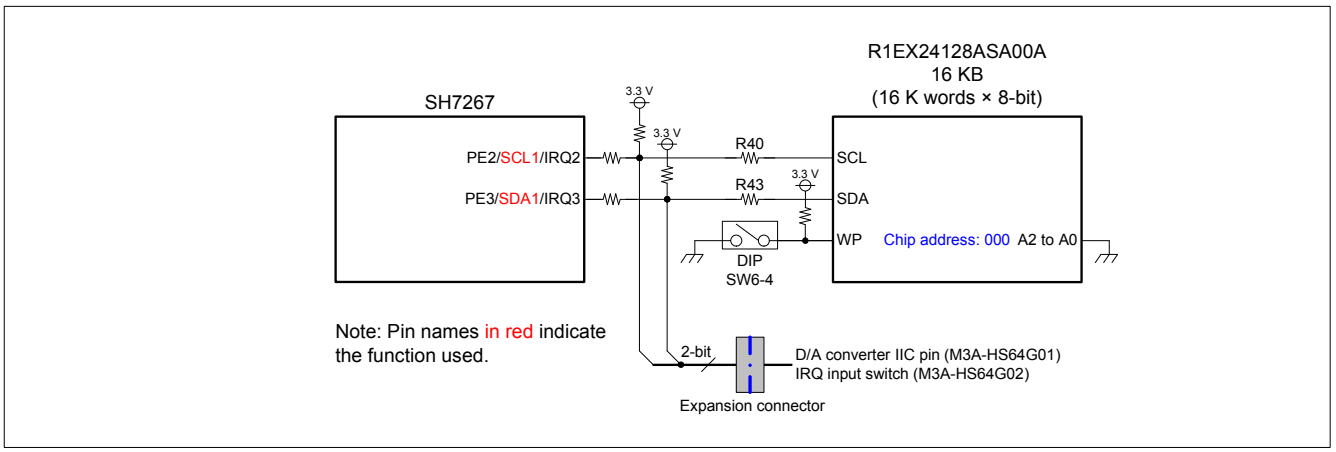

Figure 2.3.7 EEPROM Interface Block Diagram

Table 2.3.12 DIP Switches Setting (SW6-4)

Number	Function	
	OFF (High)	ON (Low)
SW6-4	EEPROM is write-protected	EEPROM is write-enabled (default)

2.4 USB Interface

The R0K572670C000BR comes standard with a USB Series-A receptacle. The wiring pattern on the R0K572670C000BR allows for connecting a Mini-B receptacle to evaluate the USB host and function modules. Remove the series-A receptacle to connect a USB mini-B receptacle. The figure below shows the USB interface block diagram. The table below lists the jumper settings (JP10).

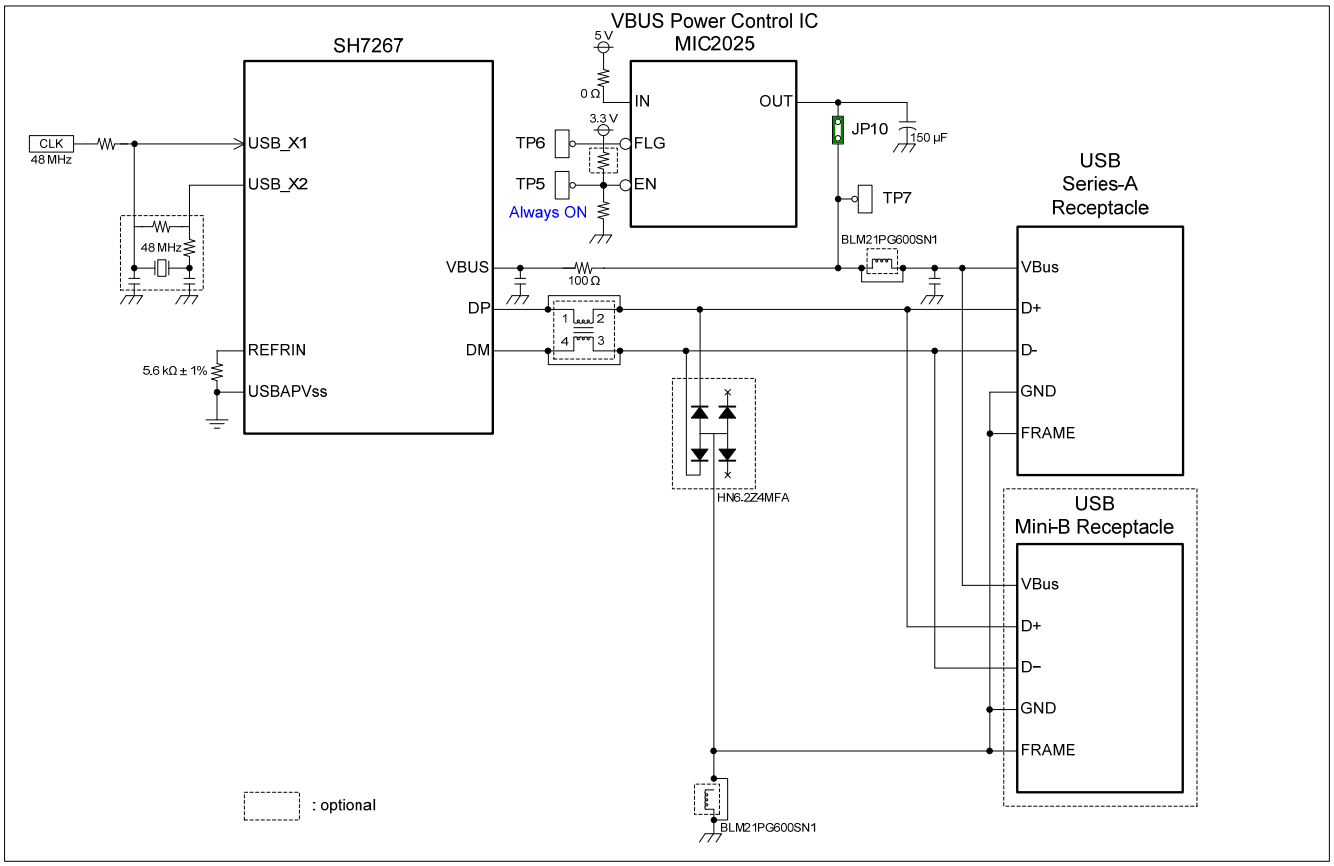

Figure 2.4.1 USB Interface Block Diagram

Table 2.4.1 Jumper Setting (JP10)

Number	1-2	None (Open)
JP10	USB host mode (Supplies the VBUS power, default)	USB function mode (Does not supply the VBUS power)

2.5 RS-232C Interface

The SH7267 includes a serial communication interface with FIFO (SCIF). D-sub 9-pin connector on the R0K572670C000BR is connected to the SH7267 SCIF channel 0 pin via an RS-232C driver IC.

The SH7267 SCIF channel 0 pin is also used as the channel 0 pin of the Controller Area Network (RCAN-TL1).

The following figure shows the RS-232C interface block diagram. The table below lists the jumpers setting (JP4, and JP5).

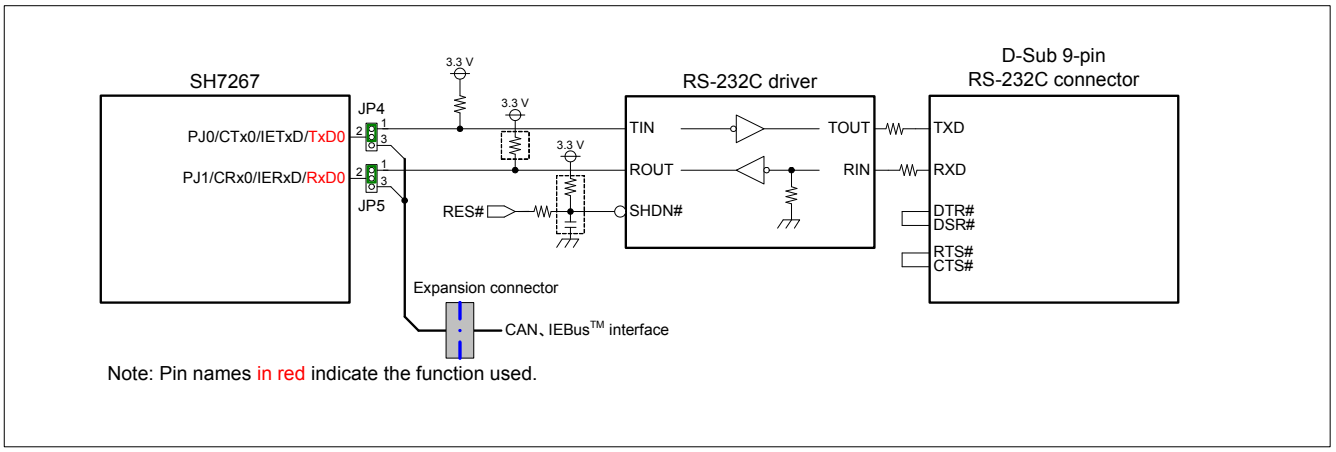

Figure 2.5.1 RS-232C Interface Block Diagram

Table 2.5.1 Jumpers Setting (JP4, and JP5)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) pin - default	Selects the CTx0 (RCAN-TL1) /IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) pin - default	Selects the CRx0 (RCAN-TL1) /IERxD (IEB) pins

2.6 I/O Ports

SH7267 I/O ports are connected to switches and LEDs on the R0K572670C000BR.

Ports PH0 to PH5 can be used as analog input pins (AN0 to AN5). Remove JP7 to use PH4 and PH5 as an analog input pin.

Port A can be used as a user interface by setting PB22 pin to output high level.

The following figure shows the I/O ports block diagram. Table 2.6.1 lists the jumpers setting (JP6, and JP7). Table 2.6.2 shows Port A function switching.

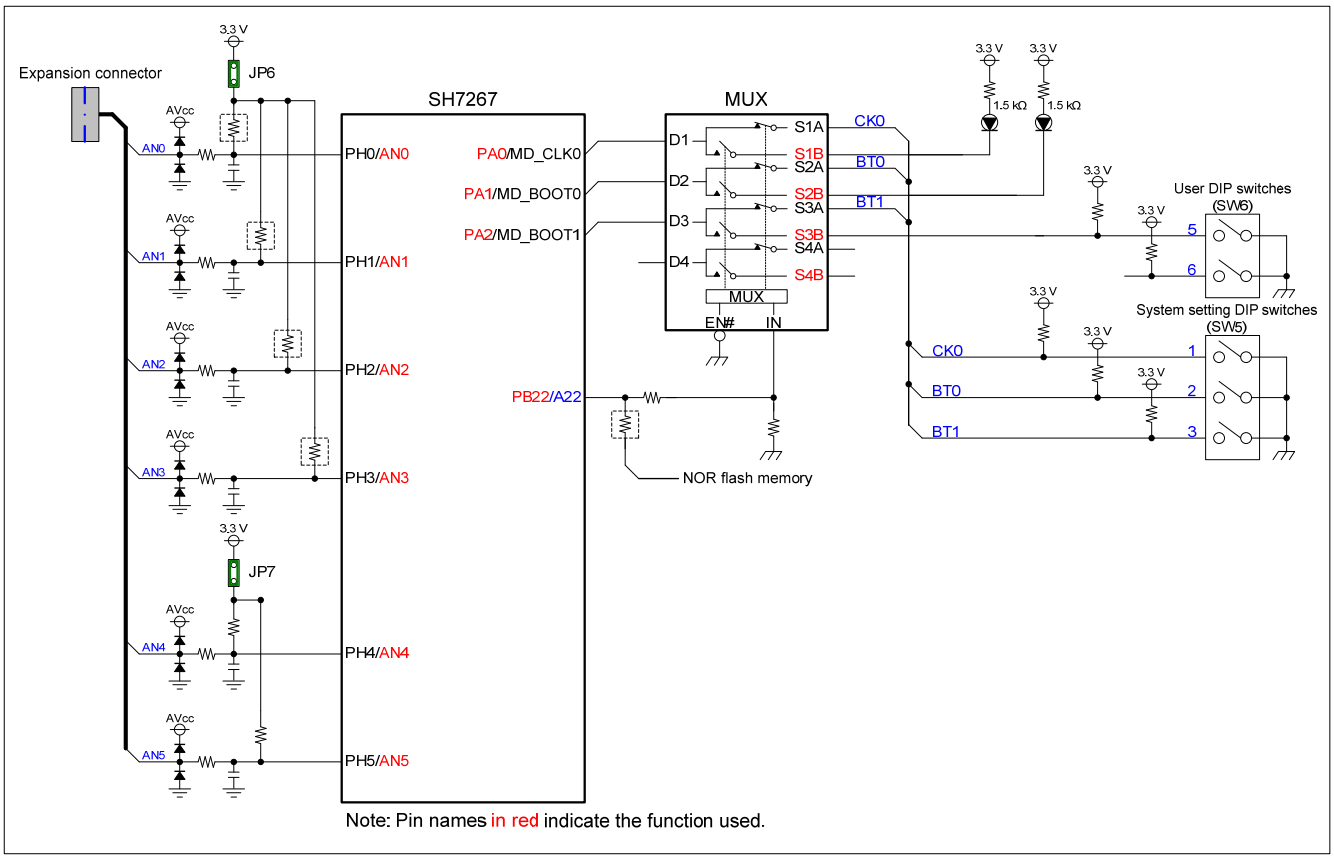

Figure 2.6.1 I/O Ports Block Diagram

Table 2.6.1 Jumpers Setting (JP6, JP7)

Number	1-2	None (Open)
JP6	Uses PH [3:0] as an input port (default) (1)	Uses PH [3:0] as an analog input pin
JP7	Uses PH [5:4] as an input port (default)	Uses PH [5:4] as an analog input pin (2)

Notes: (1) Mount R11 to R14 when using PH [3:0] as an input port.

(2) Remove R15 and R16 when using PH [5:4] as an analog input pin.

Table 2.6.2 Port A Function Switching

Number	High output	Low output
PB22	Uses Port A as a user interface	Mode sampling (At power-up)

2.7 Interrupt Switches

The R0K572670C000BR includes two push-button switches (NMI switch and IRQ1 switch) for the NMI and IRQ1 interrupt signals input from the SH7267, and a push-button switch (TEST switch) for test signals.

The TEST switch is open to allow for connecting a desired pin. Set JP8 to use IRQ1 switch.

The figure below shows the interrupt switch block diagram. The table below lists the jumper setting (JP8).

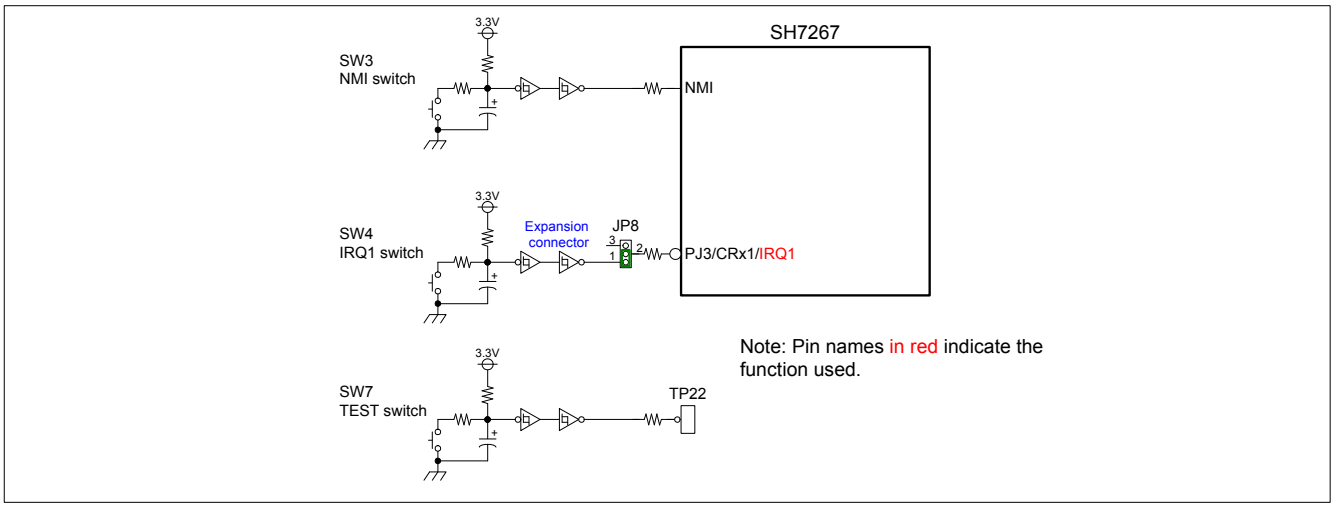

Figure 2.7.1 Interrupt Switch Block Diagram

Table 2.7.1 Jumper Setting (JP8)

Number	1-2	2-3
JP8	Uses PJ3 as the IRQ1 input pin (default)	Uses PJ3 as the CRx1 input pin

2.8 Clock Modules

Provide following clocks with the SH7267 on the R0K572670C000BR.

- SH7267 input clock: 12 MHz
- SH7267 RTC clock: 32.768 kHz
- SH7267 audio clock: 12.2880 MHz, and 11.2896 MHz (default)
- SH7267 USB clock: 48.00 MHz
- SH7267 LCD clock: 5.33 MHz (default)

➢ How to select the system clock frequency of AK4353 (D/A converter), and AK4524 (audio codec)

SH7267 audio clock provides either 12.2880 MHz or 11.2896 MHz with AK4353 and AK4524 by switching JP9.

The following figure shows the clock module block diagram. The table below lists the audio clock switching.

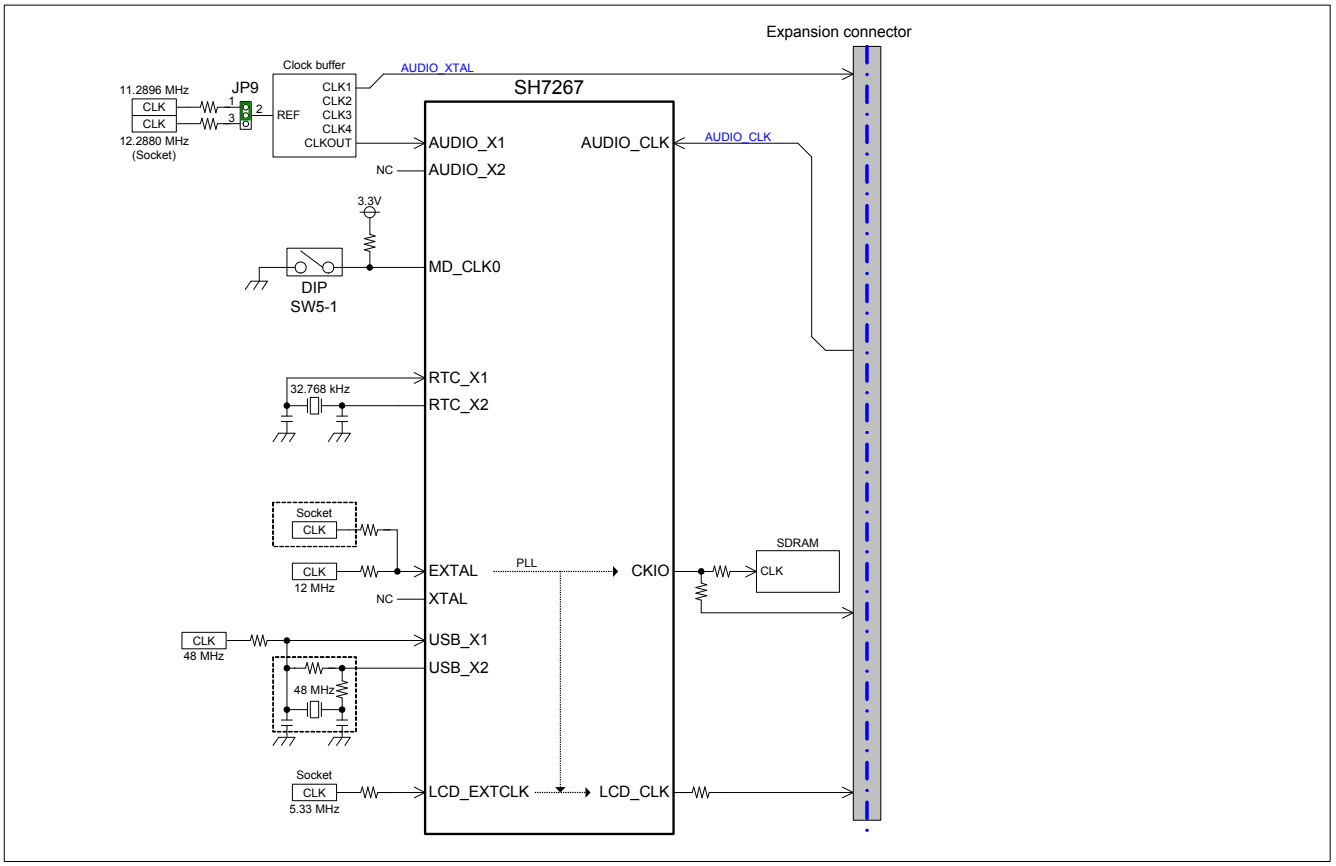

Figure 2.8.1 Clock Module Block Diagram

Table 2.8.1 Audio Clock Switching

Number	1-2	2-3
JP9	Provides 11.2896 MHz with the AUDIO_X1 pin (default)	Provides 12.2880 MHz with the AUDIO_X1 pin

2.9 Reset Module

A reset IC controls reset signals connected to the SH7267, flash memory and peripheral I/Os on the R0K572670C000BR. There are two system reset options; power-on reset, and reset by switch.

The following figure shows the reset module block diagram.

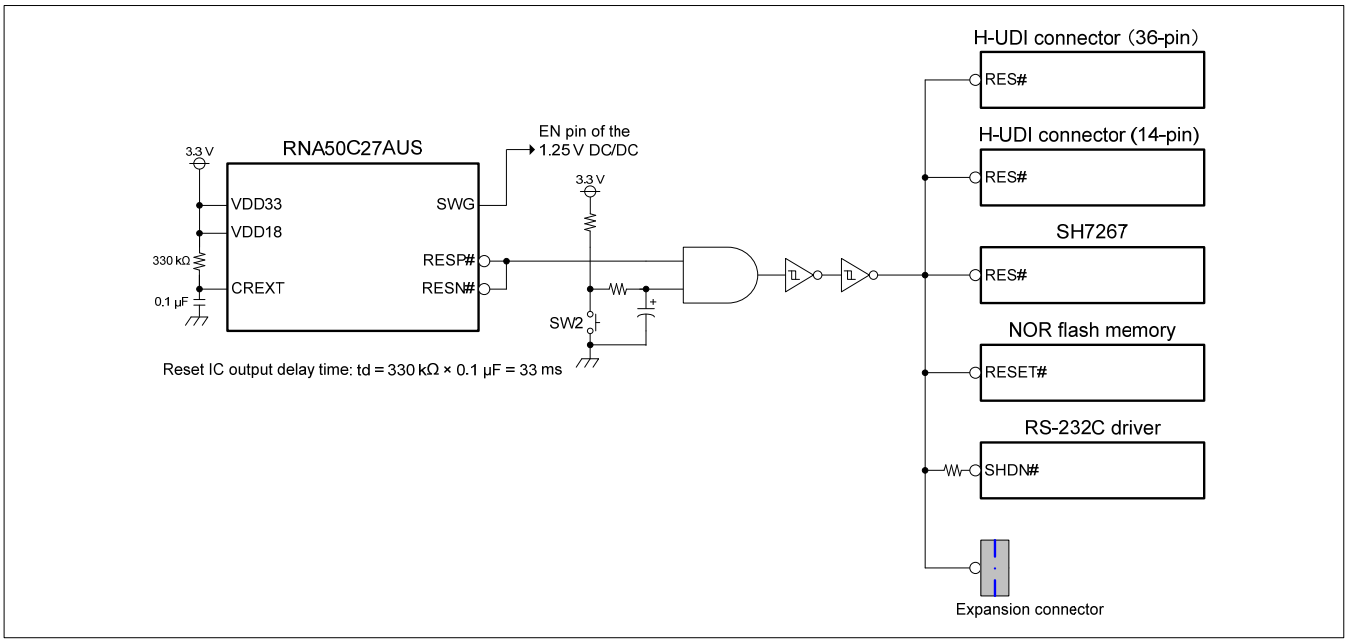

Figure 2.9.1 Reset Module Block Diagram

2.10 Power Supply Module

The R0K572670C000BR is supplied 5 V power supply, the voltage regulator on the R0K572670C000BR generates 3.3 V voltage, the reference voltage for the A/D converter (3.3 V), and 1.25 V. CPU 3.3 V and 1.25 V power can be externally-supplied.

The following figure shows the power supply module block diagram.

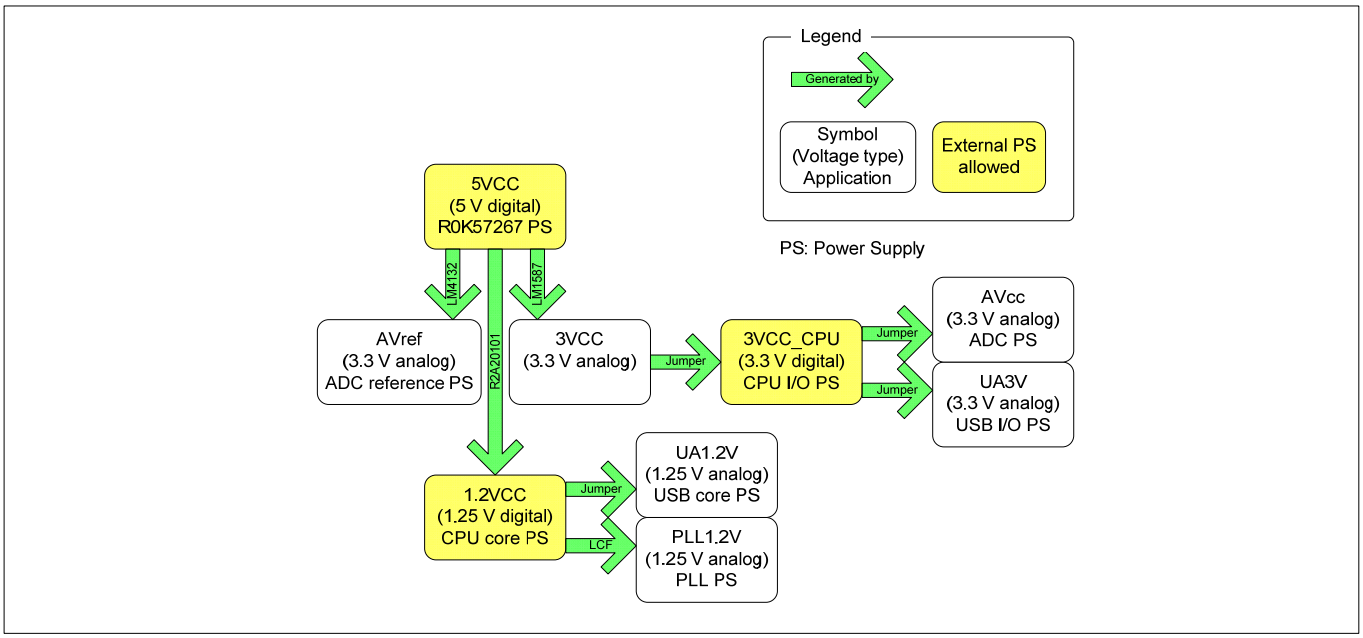

Figure 2.10.1 Power Supply Module Block Diagram

2.11 E10A-USB Interface

The R0K572670C000BR includes two H-UDI port connectors (14-pin and 36-pin) to connect to the E10A-USB emulator.

The AUD pin is also used as SSIF (Serial Sound Interface with FIFO) pin, and VDC3 (Video Display Controller 3) pin.

AUD function can be used when the R0K572670C000BR is used only. (Do not use the AUD function when connecting optional boards.) When using AUD function, set the AUDCK frequency to 40 MHz or lower.

The following figure shows the E10A-USB interface block diagram.

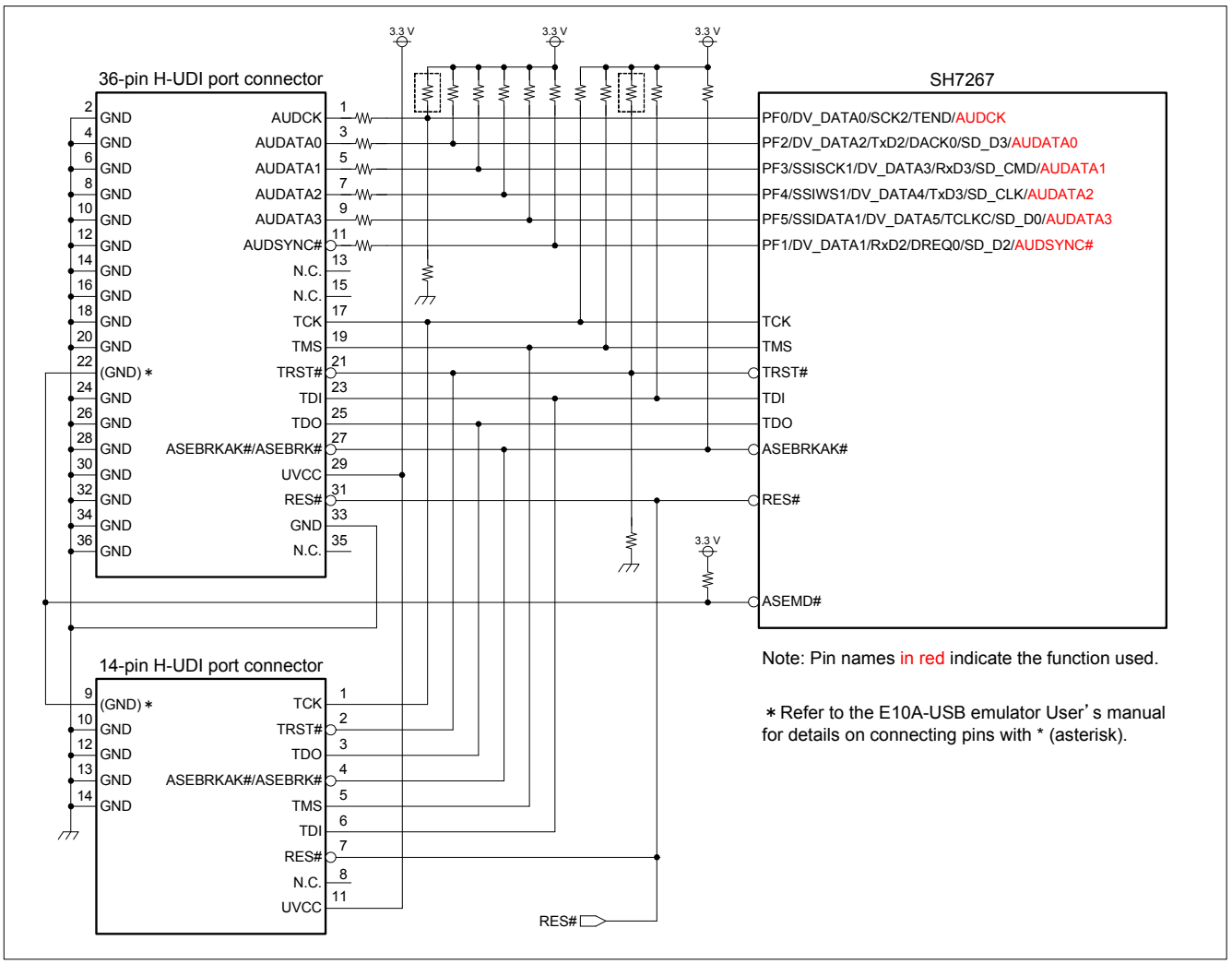

Figure 2.11.1 E10A-USB Interface Block Diagram

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Chapter 3
M3A-HS64G01 Functions

3.1 Overview of Functions

M3A-HS64G01 includes the function modules listed in the following table.

Table 3.1.1 M3A-HS64G01 Function Modules

Section	Function	Description
3.2	CPU	• SH7267
3.3	LCD Module Interface	• LCD module interface - Connects the SH7267 Video Display Controller 3 (VDC3) and LCD module connectors - Flexible connectors for LCD module are included • Character LCD module with LED backlight Note: This module cannot be used with the R0K572670C000BR.
3.4	Audio Modules	• Connects the SH7267, D/A converters, and an audio codec - 96 kHz 24-bit D/A converters: 2 Note: One D/A converter can be used with the R0K572670C000BR. - 24-bit stereo codec with microphone AMP: 1 Note: This module cannot be used with the R0K572670C000BR.
3.5	CD Deck Interface	• Connects RSPI, SSIF and a CD deck
3.6	SD Card Interface	• Connects the SH7267 SD Host Interface (SDHI) and an SD card slot Note: This module cannot be used with the R0K572670C000BR.
3.7	UART Interface	• Connects the SH7267 Serial Communication Interface with FIFO (SCIF) and a UART connector Note: This module cannot be used with the R0K572670C000BR.
3.8	CAN Interface	• Connects the SH7267 Controller Area Network (RCAN-TL1) and a CAN connector
3.9	IEBus™ Interface	• Connects the SH7267 IEBus™ controller (IEB) and IEBus™ connector
3.10	I/O Ports	• Connect the SH7267 I/O ports, LEDs, and DIP switches
3.11	Clock Modules	• Controls the system clock • Controls the peripheral I/O clock
3.12	Reset Module	• Resets devices on the M3A-HS64G01
3.13	Power Supply Module	• Controls the M3A-HS64G01 system power supply
–	Operating Specifications	• Connectors, switches, and LEDs Refer to Chapter 6 for details.

3.2 CPU

3.2.1 SH7267 Overview

The R0K572670C000BR includes the SH7267, the 32-bit RISC MCU that operates with a maximum frequency of 144 MHz.

3.2.2 SH7267 Pin Functions Used on the M3A-HS64G01

Table 3.2.1 to Table 3.2.6 list the SH7267 pin functions used on the M3A-HS64G01.

Table 3.2.1 SH7267 Pin Functions (1/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
1	PVcc				
2	PG18/LCD_DE/TIOC2A/RxD3/ RTS1	LCD_DE	Connected to the LCD module EN pin	CN9, pin 24	
3	Vss				
4	PB1/A1/LCD_HSYNC	A1	Address bus	CN4, pin 1	
5	Vcc				
6	PB2/A2/LCD_VSYNC	A2	Address bus	CN4, pin 2	
7	PB3/A3/LCD_DATA15	A3	Address bus	CN4, pin 3	
8	PB4/A4/TIOC0A/LCD_DATA14	A4	Address bus	CN4, pin 4	
9	PG9/LCD_DATA9/SSIRxD0/ TxD4/SIOFSYNC	LCD_DATA 9	Connected to the LCD module D9 pin	CN9, pin 11	G4
10	PVcc				
11	PG8/LCD_DATA8/SSITxD0/ RxD4/SIOFSCK	LCD_DATA 8	Connected to the LCD module D8 pin	CN9, pin 12	G3
12	Vss				
13	PB5/A5/TIOC0B/LCD_DATA13	A5	Address bus	CN4, pin 5	
14	PB6/A6/TIOC0C/LCD_DATA12	A6	Address bus	CN4, pin 6	
15	PB7/A7/TIOC0D/LCD_DATA11	A7	Address bus	CN4, pin 9	
16	PB8/A8/TIOC1A/LCD_DATA10	A8	Address bus	CN4, pin 10	
17	PVcc				
18	PB9/A9/TIOC1B/LCD_DATA9	A9	Address bus	CN4, pin 11	
19	Vss				
20	PB10/A10/TIOC2A/LCD_DATA8	A10	Address bus	CN4, pin 12	
21	Vcc				
22	PB11/A11/TIOC2B/LCD_DATA7	A11	Address bus	CN4, pin 13	
23	PB12/A12/TIOC3A/LCD_DATA6	A12	Address bus	CN4, pin 14	
24	PB13/A13/TIOC3B/LCD_DATA5	A13	Address bus	CN4, pin 17	
25	PB14/A14/TIOC3C/LCD_DATA4	A14	Address bus	CN4, pin 18	
26	PB15/A15/TIOC3D/LCD_DATA3	A15	Address bus	CN4, pin 19	
27	PG7/LCD_DATA7/SD_CD/ PINT7/IRQ7	LCD_DATA 7	Connected to the LCD module D7 pin	CN9, pin 9	G2
28	PG6/LCD_DATA6/SD_WP/ PINT6/IRQ6	LCD_DATA 6	Connected to the LCD module D6 pin	CN9, pin 7	G1
29	PVcc				
30	PG5/LCD_DATA5/SD_D1/ PINT5/IRQ5	LCD_DATA 5	Connected to the LCD module D5 pin	CN9, pin 8	G0
31	Vss				
32	PG4/LCD_DATA4/SD_D0/ PINT4/IRQ4	LCD_DATA 4	Connected to the LCD module D4 pin	CN9, pin 6	B5
33	Vcc				

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 3.2.2 SH7267 Pin Functions (2/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
34	PB16/A16/TIOC4A/LCD_DATA2	A16	Address bus	CN4, pin 20	
35	PB17/A17/TIOC4B/LCD_DATA1/ SCK1	A17	Address bus	CN4, pin 21	
36	PB18/A18/TIOC4C/LCD_DATA0/ TxD1	A18	Address bus	CN4, pin 22	
37	PB19/A19/TIOC4D/RxD1	A19	Address bus	CN4, pin 25	
38	PB20/A20/SPDIF_IN/SCK4	A20	Address bus	CN4, pin 26	
39	PB21/A21/SPDIF_OUT/TxD4	A21	Address bus	CN4, pin 27	
40	PVcc				
41	CKIO	CKIO	Connected to the SDRAM CLK pin	CN6, pin 20	
42	Vss				
43	PB22/A22/CS4#/RxD4	PB22	Switches the system setting/user interface	CN4, pin 28	Low: MD Hi: IO
44	NMI	NMI	Non-maskable interrupt	–	
45	PLLVcc				
46	RES#	RES#	Reset input	CN7, pin 6	
47	PLLVss				
48	PA0/MD_CLK0	PA0	Connected to LED2 as a user output port	CN1, pin 10	PB22: High
		MD_CLK0	Connected to SW5-1 as clock mode input 0		PB22: Low
49	PA1/MD_BOOT0	PA1	Connected to LED2 as a user output port	CN1, pin 9	PB22: High
		MD_BOOT0	Connected to SW5-2 as boot mode input 0		PB22: Low
50	EXTAL	EXTAL	Connects the system external clock to MCU	–	12 MHz
51	XTAL	XTAL	Open	–	
52	PG3/LCD_DATA3/SD_CLK/ PINT3	LCD_DATA3	Connected to the LCD module D3 pin	CN9, pin 3	B4
53	PG2/LCD_DATA2/SD_CMD/ PINT2	LCD_DATA2	Connected to the LCD module D2 pin	CN9, pin 4	B3
54	PG1/LCD_DATA1/SD_D3/PINT1	LCD_DATA1	Connected to the LCD module D1 pin	CN9, pin 1	B2
55	PG0/LCD_DATA0/SD_D2/PINT0	LCD_DATA0	Connected to the LCD module D0 pin	CN9, pin 2	B1, B0
56	Vss				
57	PVcc				
58	PG20/LCD_EXTCLK/SCK1	LCD_EXTCLK	Connects the LCD module external clock to MCU	CN9, pin 26	Default: 5.33 MHz
59	Vss				
60	RTC_X1	RTC_X1	Connects the real-time clock resonator to MCU	–	32.768 kHz
61	RTC_X2	RTC_X2		–	
62	PA2/MD_BOOT1	PA2	Connected to SW6-5 as a user input port	CN1, pin 8	PB22:"H"
		MD_BOOT1	Connected to SW5-3 as boot mode input 1		PB22:"L"
63	USB_X1	USB_X1	Connects the USB external clock to MCU	–	48 MHz
64	USB_X2	USB_X2	Open	–	
65	ASEMD#	ASEMD#	ASE mode select	–	H-UDI
66	USBDPVcc				
67	USBDPVss				
68	DM	DM	USB differential signal D− data	–	
69	DP	DP	USB differential signal D+ data	–	
70	VBUS	VBUS	VBUS input	–	
71	USBDVcc				
72	USBDVss				
73	REFRIN	REFRIN	Reference input	–	Connects a 5.6 kΩ ± 1% resistor
74	USBAPVss				
75	USBAPVcc				

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 3.2.3 SH7267 Pin Functions (3/6)

No.	Name	Function	Description	Expansion connector	Remarks
76	USBAVcc				
77	USBAVss				
78	USBUVcc				
79	USBUVss				
80	PH0/AN0	AN0	Connected to the push-botton switch as key input	CN3, pin 4	
81	PH1/AN1	AN1	Connected to the push-botton switch as key input	CN3, pin 3	
82	PH2/AN2	AN2	Connected to the push-botton switch as key input	CN3, pin 8	
83	PH3/AN3	AN3	Connected to the push-botton switch as key input	CN3, pin 7	
84	AVss				
85	PH4/AN4	PH4	Connected to the CD deck TRANS pin	CN1, pin 2	
86	AVref				
87	PH5/AN5	PH5	Connected to the CD deck FLAG6 pin	CN1, pin 4	
88	AVcc				
89	TRST#	TRST#	Initialization-signal input pin	–	H-UDI
90	ASEBRKAK#/ASEBRK#	ASEBRKAK#	Break mode acknowledge	–	H-UDI
		ASEBRK#	Break request		
91	TDO	TDO	Test data output	–	H-UDI
92	TDI	TDI	Test data input	–	H-UDI
93	TMS	TMS	Test mode select	–	H-UDI
94	TCK	TCK	Test clock	–	H-UDI
95	AUDIO_X2	AUDIO_X2	Open	–	
96	AUDIO_X1	AUDIO_X1	Connects the audio external clock to MCU	–	Switched by JP9
97	PG24/MISO1/TIOC0D	–	Connected to the character LCD E pin	CN6, pin 13	Not available
98	PVcc				
99	PG23/MOSI1/TIOC0C	–	Connected to the character LCD RS pin	CN6, pin 12	Not available
100	Vss				
101	PG22/SSL10/TIOC0B	–	Connected to the AK4524 (U6) CS pin	CN9, pin 27	Not available
102	Vcc				
103	PG21/RSPCK1/TIOC0A	–	Connected to the AK4524 (U6) CCLKI pin	CN9, pin 28	Not available
104	PJ3/CRx1/CRx0/CRx1/IRQ1/ AUDIO_XOUT/WDTOVF#	IRQ1	IRQ1 switch	–	JP8: 1-2
		CRx1	Connected to the CAN driver IC (U16)	CN1, pin 17	JP8: 2-3
105	PJ2/CTx1/CTx0&CTx1/ CS2#/SCK0/LCD_M_DISP	CTx1	Connected to the CAN driver IC (U16)	CN1, pin 18	
		LCD_M_DISP	LCD AC control signal		
106	PJ1/CRx0/IERxD/IRQ0/RxD0	RxD0	Connected to the RS-232C connector (J10)	–	JP5: 1-2
		CRx0	Connected to the CAN driver IC (U14)	CN1, pin 19	JP5: 2-3
		IERxD	Connected to the IEBus™ driver IC		
107	PJ0/CTx0/IETxD/CS1#/ TxD0/A0	TxD0	Connected to the RS-232C connector (J10)	–	JP4: 1-2
		CTx0	Connected to the CAN driver IC (U14)	CN1, pin 20	JP4: 2-3
		IETxD	Connected to the IEBus™ driver IC		
108	PF8/CE2B#/SSIDATA2/ DV_CLK/SD_CD	SSIDATA2	Connected to the CD deck IIS_DATA pin	CN7, pin 27	SW6-6: ON
		–	Connected to the character LCD DB7 pin	CN7, pin 15	SW6-6: OFF JP2: 1-2
		–	Connected to the SD card slot CD pin		SW6-6: OFF JP2: 2-3
109	PF7/CE2A#/SSIWS2/ DV_DATA7/TCLKD/SD_WP	SSIWS2	Connected to the CD deck IIS_LRCK pin	CN7, pin 28	SW6-6: ON
		–	Connected to the character LCD DB6 pin	CN7, pin 16	SW6-6: OFF JP2: 1-2
		–	Connected to the SD card slot WP pin		SW6-6: OFF JP2: 2-3
110	PVcc				

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 3.2.4 SH7267 Pin Functions (4/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
111	PF6/CS6#/CE1B#/SSISCK2/ DV_DATA6/TCLKB/SD_D1	SSISCK2	Connected to the CD deck IIS_BCK pin	CN7, pin 25	SW6-6: ON
		–	Connected to the character LCD DB5 pin	CN7, pin 13	SW6-6: OFF JP2: 1-2
		–	Connected to the SD card slot DAT1 pin		SW6-6: OFF JP2: 2-3
112	Vss				
113	PF5/CS5#/CE1A#/SSIDATA1/ DV_DATA5/TCLKC/SD_D0/ AUDATA3	AUDATA3	Connected to the H-UDI port connector (J3)	CN7, pin 23	AUD
		SSIDATA1	Connected to the AK4353 (U12) SDTI pin		SW6-6: ON
		–	Connected to the character LCD DB4 pin	CN7, pin 14	SW6-6: OFF JP2: 1-2
		–	Connected to the SD card slot DAT0 pin		SW6-6: OFF JP2: 2-3
114	Vcc				
115	PF4/ICIOWR#/AH#/SSIWS1/ DV_DATA4/TxD3/SD_CLK/ AUDATA2	AUDATA2	Connected to the H-UDI port connector (J3)	CN7, pin 24	AUD
		SSIWS1	Connected to the AK4353 (U12) LRCK pin		SW6-6: ON
		–	Connected to the character LCD DB3 pin	CN7, pin 3	SW6-6: OFF JP2: 1-2
		–	Connected to the SD card slot CLK pin		SW6-6: OFF JP2: 2-3
116	PF3/ICIORD#/SSISCK1/ DV_DATA3/RxD3/SD_CMD/ AUDATA1	AUDATA1	Connected to the H-UDI port connector (J3)	CN7, pin 22	AUD
		SSISCK1	Connected to the AK4353 (U12) BICKI pin		SW6-6: ON
		–	Connected to the character LCD DB2 pin	CN7, pin 4	SW6-6: OFF JP2: 1-2
		–	Connected to the SD card slot CMD pin		SW6-6: OFF JP2: 2-3
117	PF2/BACK#/DV_DATA2/TxD2/ DACK0/SD_D3/AUDATA0	AUDATA0	Connected to the H-UDI port connector (J3)	CN7, pin 19	AUD
		–	Connected to the AK4353 (U11) SDTI pin		SW6-6: ON
		–	Connected to the character LCD DB1 pin	CN7, pin 1	SW6-6: OFF JP2: 1-2
		–	Connected to the SD card slot DAT3 pin		SW6-6: OFF JP2: 2-3
118	PF1/BREQ#/DV_DATA1/RxD2/ DREQ0/SD_D2/AUDSYNC#	AUDSYNC#	Connected to the H-UDI port connector (J3)	CN7, pin 20	AUD
		–	Connected to the AK4353 (U11) LRCKI pin		SW6-6: ON
		PF1	Connected to the AK4524 and AK4353 PDN# pin	CN9, pin 29	
		–	Connected to the character LCD DB0 pin	CN7, pin 2	SW6-6: OFF JP2: 1-2
		–	Connected to the SD card slot DAT2 pin		SW6-6: OFF JP2: 2-3
119	PF0/WAIT#/DV_DATA0/SCK2/ TEND0/AUDCK	AUDCK	Connected to the H-UDI port connector (J3)	CN7, pin 17	AUD
		–	Connected to the AK4353 (U11) BICKI pin		
		PF0	Connected to the CD deck CDFS pin	CN7, pin 32	
120	PVcc				
121	PG17/LCD_HSYNC/TIOC1B/ TxD1	LCD_HSYNC	Connected to the LCD module HSYNC pin	CN9, pin 21	
122	Vss				
123	PG16/LCD_VSYNC/TIOC1A/ RxD1	LCD_VSYNC	Connected to the LCD module VSYNC pin	CN9, pin 19	
124	PF12/BS#/MISO0/TIOC3D/ SPDIF_OUT	MISO0	Connected to the serial flash memory SO pin	CN7, pin 33	SW5-6: OFF
			Connected to the CD deck CDSO pin		
		–	Connected to the AK4524 (U6) SDTO pin	CN7, pin 38	SW5-6: ON
125	PF11/A25/SSIDATA3/MOSI0/ TIOC3C/SPDIF_IN	MOSI0	Connected to the serial flash memory SI pin	CN7, pin 31	SW5-6: OFF
			Connected to the CD deck CDSI pin		
		–	Connected to the AK4524 (U6) SDTI pin	CN7, pin 37	SW5-6: ON

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 3.2.5 SH7267 Pin Functions (5/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
126	PVcc				
127	PF10/A24/SSIWS3/SSL00/ TIOC3B/FCE#	SSL00	Connected to the serial flash memory CS# pin	–	SW5-5:ON SW5-6:OFF
		–	Connected to the AK4524 (U6) LRCK pin	CN7, pin 35	SW5-5:ON SW5-6:ON
		FCE#	Connected to the NAND flash memory CE# pin	–	SW5-5:OFF
128	Vss				
129	PF9/A23/SSISCK3/RSPCK0/ TIOC3A/FRB	RSPCK0	Connected to the serial flash memory SCK pin	CN7, pin 30	SW5-5:ON SW5-6:OFF
			Connected to the CD deck CDCK pin		
		–	Connected to the AK4524 (U6) BICK pin	CN7, pin 36	SW5-5: ON SW5-6:ON
		FRB	Connected to the NAND flash memory R/B# pin	–	SW5-5:OFF
130	Vcc				
131	PD15/D15/NAF7/PWM2H	D15/NAF7	Data bus	CN8, pin 19	
132	PD14/D14/NAF6/PWM2G	D14/NAF6	Data bus	CN8, pin 17	
133	PE5/SDA2/DV_HSYNC	SDA2	Connected to the external IIC connector (J11)	CN7, pin 12	
134	PE4/SCL2/DV_VSYNC	SCL2	Connected to the external IIC connector (J11)	CN7, pin 9	
135	PE3/SDA1/IRQ3	SDA1	Connected to the EEPROM SDA pin	CN7, pin 10	JP10:1-2
			Connected to the AK4353 (U11, U12) SDA/CDTI pins		
136	PE2/SCL1/IRQ2	SCL1	Connected to the EEPROM SCL pin	CN7, pin 7	JP9:1-2
			Connected to the AK4353 (U11, U12) SCL/CCLKI pins		
137	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ ADTRG#/LCD_EXTCLK	IRQ1	Connected to the CD deck BLKCK pin	CN7, pin 8	
		TCLKA	Connected to the through-hole (MH8)		
138	PE0/SCL0/AUDIO_CLK/IRQ0	AUDIO_CLK	Connected to the external clock input socket (U8)	CN7, pin 5	
139	PD13/D13/NAF5/PWM2F	D13/NAF5	Data bus	CN8, pin 14	
140	PD12/D12/NAF4/PWM2E	D12/NAF4	Data bus	CN8, pin 12	
141	PVcc				
142	PD11/D11/NAF3/PWM2D	D11/NAF3	Data bus	CN8, pin 9	
143	Vss				
144	PD10/D10/NAF2/PWM2C	D10/NAF2	Data bus	CN8, pin 7	
145	PD9/D9/NAF1/PWM2B	D9/NAF1	Data bus	CN8, pin 4	
146	PD8/D8/NAF0/PWM2A	D8/NAF0	Data bus	CN8, pin 2	
147	PD7/D7/FWE#/PWM1H	D7/FWE#	Connected to the data bus and the NAND flash memory WE# pin	CN8, pin 18	Auto-switch
148	PD6/D6/FALE/PWM1G	D6/FALE	Connected to the data bus and the NAND flash memory ALE pin	CN8, pin 16	Auto-switch
149	PD5/D5/FCLE/PWM1F	D5/FCLE	Connected to the data bus and the NAND flash memory CLE pin	CN8, pin 13	Auto-switch
150	PG15/LCD_DATA15/TIOC0D/ TxD7	LCD_DATA15	Connected to the LCD module D15 pin	CN9, pin 20	R5
151	PG14/LCD_DATA14/TIOC0C/ RxD7	LCD_DATA14	Connected to the LCD module D14 pin	CN9, pin 17	R4
152	PVcc				
153	Vss				

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 3.2.6 SH7267 Pin Functions (6/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
154	PG13/LCD_DATA13/TIOC0B/ TxD6	LCD_DATA13	Connected to the LCD module D13 pin	CN9, pin 18	R3
155	PG12/LCD_DATA12/TIOC0A/ RxD6	LCD_DATA12	Connected the LCD module D12 pin	CN9, pin 16	R2
156	PD4/D4/FRE#/PWM1E	D4/FRE#	Connected to the data bus and the NAND flash memory RE# pin	CN8, pin 11	Auto-switch
157	PD3/D3/PWM1D	D3	Data bus	CN8, pin 8	
158	PD2/D2/PWM1C	D2	Data bus	CN8, pin 6	
159	PD1/D1/PWM1B	D1	Data bus	CN8, pin 3	
160	PD0/D0/PWM1A	D0	Data bus	CN8, pin 1	
161	PC0/CS0#/SSIWS0	CS0#	Connected to the NOR flash memory CE# pin	CN6, pin 5	
162	PVcc				
163	PC1/RD#/SSISCK0	RD#	Connected to the NOR flash memory OE# pin	CN6, pin 6	
164	Vss				
165	PC2/RD/WR#/SSIRxD0	RD/WR#	Connected to the SDRAM WE# pin	CN6, pin 7	
166	PC3/WE0#/DQML/SSITxD0	WE0#	Connected to the NOR flash memory WE# pin	CN6, pin 8	
		DQML	Connected to the SDRAM DQML pin		
167	PC4/WE1#/DQMU/WE#	DQMU	Connected to the SDRAM DQMU pin	CN6, pin 9	
168	PC5/RAS#/TIOC4A/IRQ4	RAS#	Connected to the SDRAM RAS# pin	–	SW5-4: OFF
		–	NC	CN6, pin 14	SW5-4: ON
169	PG11/LCD_DATA11/SSIWS0/ IRQ3/TxD5/SIOFTxD	LCD_DATA11	Connected to the LCD module D11 pin	CN9, pin 13	R1, R0
170	PVcc				
171	PG10/LCD_DATA10/SSISCK0/ IRQ2/RxD5/SIOFRxD	LCD_DATA10	Connected to the LCD module D10 pin	CN9, pin 14	G5
172	Vss				
173	PC6/CAS#/TIOC4B/IRQ5	CAS#	Connected to the SDRAM CAS# pin	–	SW5-4: OFF
		–	NC	CN6, pin 15	SW5-4: ON
174	PC7/CKE/TIOC4C/IRQ6	CKE	Connected to the SDRAM CKE pin	–	SW5-4: OFF
		–	NC	CN6, pin 16	SW5-4: ON
175	PC8/CS3#/TIOC4D/IRQ7	CS3#	Connected to the SDRAM CS# pin	–	SW5-4: OFF
		–	NC	CN6, pin 17	SW5-4: ON
176	PG19/LCD_CLK/TIOC2B/TxD3/ CTS1	LCD_CLK	Connected to the LCD module CLK pin	CN9, pin 23	

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

3.2.3 M3A-HS64G01 Module Availability

The following table shows which combination of modules can/cannot be used.

Table 3.2.7 M3A-HS64G01 Module Availability

				R0K572670C000BR													R0K572670C000BR+M3A-HS64G01													
	SH7267 Peripherals	Component No.	Module Name	NOR flash memory	SDRAM	NAND flash memory	EEPROM	Serial flash memory	USB	H-UDI (14-pin)	H-UDI (36-pin)	LED	NMI switch	IRQ1 switch	DIP switches	RS-232C	Character LCD	SD card	Audio codec	D/A converter 1	D/A converter 2	CD deck	UART	IIC	LCD	IEBus™	CAN0	CAN1	Key input switch
R0K572670C000BR	BSC	U6	NOR flash memory		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	–	Y	Y	–	Y	Y	Y	Y	Y	Y
	BSC	U9	SDRAM	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	–	Y	Y	–	Y	Y	Y	Y	Y	Y
	FLCTL	U7	NAND flash memory	Y	Y		Y	(2)	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	–	Y	(2)	–	Y	Y	Y	Y	Y	Y
	IIC3	U8	EEPROM	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	–	Y	Y	–	Y	Y	Y	Y	Y	Y
	RSPI	U10	Serial flash memory	Y	Y	(2)	Y		Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	–	Y	(2)	–	Y	Y	Y	Y	Y	Y
	USB	J1, J2	USB	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	–	–	–	–	Y	Y	–	Y	Y	Y	Y	Y	Y
	H-UDI	J7	H-UDI (14-pin)	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	–	–	–	–	Y	Y	–	Y	Y	Y	Y	Y	Y
	H-UDI, AUD	J3	H-UDI (36-pin)	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	–	–	–	–	×	Y	–	Y	Y	Y	Y	Y	Y
	I/O ports	LED2, LED3	LED	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	(1)	Y	–	–	–	–	Y	Y	–	Y	Y	Y	Y	Y	Y
	INTC	SW3	NMI switch	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	–	–	–	–	Y	Y	–	Y	Y	Y	Y	Y	Y
	INTC	SW4	IRQ1 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	–	–	–	–	Y	Y	–	Y	Y	Y	Y	(5)	Y
	I/O ports	SW5, SW6	DIP switches	Y	Y	Y	Y	Y	Y	Y	Y	(1)	Y	Y		Y	–	–	–	–	Y	Y	–	Y	Y	Y	Y	Y	Y
	SCIF	J10	RS-232C	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		–	–	–	–	Y	Y	–	Y	Y	(3)	(3)	Y	Y
R0K572670C000BR+M3A-HS64G01	I/O ports	J1	Character LCD	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	Y	Y	–	Y	Y	Y	Y	Y	Y
	SDHI	J2	SD card	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–	–	–	–	–
	SSIF, RSPI	U6	Audio codec	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–	–	–	–
	SSIF, IIC3	U11	D/A converter 1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–	–	–
	SSIF, IIC3	U12	D/A converter 2	Y	Y	Y	Y	Y	Y	×	Y	Y	Y	Y	Y	Y	Y	–	–	–		Y	–	Y	Y	Y	Y	Y	Y
	ROMDEC	J9	CD deck	Y	Y	(2)	Y	(2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	Y		–	Y	Y	Y	Y	Y	Y
	SCIF	J10	UART	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–
	IIC3	J11	IIC	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	Y	Y	–		Y	Y	Y	Y	Y
	VDC3	J12 to J14	LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	Y	Y	–	Y		Y	Y	(6)	Y
	IEB	J15	IEBus™	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(3)	Y	–	–	–	Y	Y	–	Y	Y		(4)	Y	Y
	RCAN	J16	CAN0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(3)	Y	–	–	–	Y	Y	–	Y	Y	(4)		Y	Y
	RCAN	J17	CAN1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(5)	Y	Y	Y	–	–	–	Y	Y	–	Y	(6)	Y	Y		Y
	I/O ports	SW2 to SW17	Key input switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	Y	Y	–	Y	Y	Y	Y	Y	

Y: Yes, —: N/A

Notes:
1: When using LED2 and LED3, SW5-1, SW5-2, and SW5-3 on the R0K572670C000BR cannot be used.
2: PF9, and PF10 are multiplex pins. When setting SW5-5, and SW5-6, on the R0K572670C000BR, only one module can be used at these intersections.
3: When changing JP4, and JP5 settings on the R0K572670C000BR, only one module can be used at these intersections.
4: When changing JP5, and JP9 settings on the M3A-HS64G01, either CAN 0 or IEBus can be used.
5: When changing JP8 setting on the R0K572670C000BR, either CAN1 or IRQ1 switch can be used.
6: PJ2 is a multiplex pin. When using the signal LCD_M_DISP, CAN1 cannot be used. When using CAN1, the signal LCD_M_DISP cannot be used.

3.2.4 SH7267 Multiplex Pins Used on the M3A-HS64G01

Table 3.2.8 to Table 3.2.19 list SH7267 multiplex pin functions used on the M3A-HS64G01.

These multiplex pins are set as port input pins by default. Set the MD bit in the port control register to use the SH7267 peripheral functions (except I/O ports).

Table 3.2.8 SH7267 Multiplex Pin Functions (BSC)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
BSC	CS0#	PCCR0	PC0MD[1:0] = B'01	PC0/CS0#/SSIWS0 (1)
	CS3#	PCCR2	PC8MD[1:0] = B'01	PC8/CS3#/TIOC4D/IRQ7
	RD#	PCCR0	PC1MD[1:0] = B'01	PC1/RD#/SSISCK0 (1)
	WE0#/DQML	PCCR0	PC3MD[1:0] = B'01	PC3/WE0#/DQML/SSITxD0
	WE1#/DQMU/WE#	PCCR1	PC4MD0 = B'1	PC4/WE1#/DQMU/WE#
	RAS#	PCCR1	PC5MD[1:0] = B'01	PC5/RAS#/TIOC4A/IRQ4
	CAS#	PCCR1	PC6MD[1:0] = B'01	PC6/CAS#/TIOC4B/IRQ5
	CKE	PCCR1	PC7MD[1:0] = B'01	PC7/CKE/TIOC4C/IRQ6
	RD/WR#	PCCR0	PC2MD[1:0] = B'01	PC2/RD/WR#/SSIRxD0
	A21	PBCR5	PB21MD[2:0] = B'001	PB21/A21/SPDIF_OUT/TxD4
	D15	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H (1)
	D14	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G (1)
	D13	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F (1)
	D12	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E (1)
	D11	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D (1)
	D10	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C (1)
	D9	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B (1)
	D8	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A (1)
	D7	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H (1)
	D6	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G (1)
	D5	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F (1)
	D4	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E (1)
	D3	PDCR0	PD3MD[1:0] = B'01	PD3/D3/PWM1D (1)
	D2	PDCR0	PD2MD[1:0] = B'01	PD2/D2/PWM1C (1)
	D1	PDCR0	PD1MD[1:0] = B'01	PD1/D1/PWM1B (1)
	D0	PDCR0	PD0MD[1:0] = B'01	PD0/D0/PWM1A (1)

Note 1: For boot modes 1 to 3

Table 3.2.9 SH7267 Multiplex Pin Functions (INTC)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
INTC	IRQ1	PJCR1	PJ3MD[2:0] = B'011	PJ3/CRx1/CRx0&CRx1/IRQ1/AUDIO_XOUT/WDTOVF#
	IRQ1	PECR0	PE1MD[2:0] = B'011	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#/LCD_EXTCLK

Table 3.2.10 SH7267 Multiplex Pin Functions (SCIF)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
SCIF	RxD0	PJCR0	PJ1MD[2:0] = B'100	PJ1/CRx0/IERxD/IRQ0/RxD0
	TxD0	PJCR0	PJ0MD[2:0] = B'100	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 3.2.11 SH7267 Multiplex Pin Functions (IIC3)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
IIC3	SDA2	PECR1	PE5MD[1:0] = B'01	PE5/SDA2/DV_HSYNC
	SCL2	PECR1	PE4MD[1:0] = B'01	PE4/SCL2/DV_VSYNC
	SDA1	PECR0	PE3MD[1:0] = B'01	PE3/SDA1/IRQ3
	SCL1	PECR0	PE2MD[1:0] = B'01	PE2/SCL1/IRQ2

Table 3.2.12 SH7267 Multiplex Pin Functions (RCAN-TL1)

Peripheral Function	Pin Nname	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
RCAN-TL1	CRx1	PJCR1	PJ3MD[2:0] = B'001	PJ3/CRx1/CRx0&CRx1/IRQ1/AUDIO_XOUT/WDTOVF#
	CTx1	PJCR0	PJ2MD[2:0] = B'001	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/LCD_M_DISP
	CRx0	PJCR0	PJ1MD[2:0] = B'001	PJ1/CRx0/IERxD/IRQ0/RxD0
	CTx0	PJCR0	PJ0MD[2:0] = B'001	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 3.2.13 SH7267 Multiplex Pin Functions (IEB)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
IEB	IERxD	PJCR0	PJ1MD[2:0] = B'010	PJ1/CRx0/IERxD/IRQ0/RxD0
	IETxD	PJCR0	PJ0MD[2:0] = B'010	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 3.2.14 SH7267 Multiplex Pin Functions (FLCTL)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
FLCTL	NAF7	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H
	NAF6	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G
	NAF5	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F
	NAF4	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E
	NAF3	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D
	NAF2	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C
	NAF1	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B
	NAF0	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A
	FWE#	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H
	FALE	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G
	FCLE	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F
	FRE#	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E
	FCE#	PFCR2	PF10MD[2:0] = B'101	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	FRB	PFCR2	PF9MD[2:0] = B'101	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 3.2.15 SH7267 Multiplex Pin Functions (SDHI)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
RSPI	MISO0	PFCR3	PF12MD[2:0] = B'011	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
	MOSI0	PFCR2	PF11MD[2:0] = B'011	PF11/A25/SSIDATA3/MOSI0/TIOC3C/SPDIF_IN
	SSL00	PFCR2	PF10MD[2:0] = B'011	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	RSPCK0	PFCR2	PF9MD[2:0] = B'011	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 3.2.16 SH7267 Multiplex Pin Functions (SSIF)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
SSIF	SSIDATA2	PFCR2	PF8MD[2:0] = B'010	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD
	SSIWS2	PFCR1	PF7MD[2:0] = B'010	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/SD_WP
	SSISCK2	PFCR1	PF6MD[2:0] = B'010	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/TCLKB/SD_D1
	SSIDATA1	PFCR1	PF5MD[2:0] = B'010	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/TCLKC/SD_D0/ AUDATA3
	SSIWS1	PFCR1	PF4MD[2:0] = B'010	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/TxD3/SD_CLK/ AUDATA2
	SSISCK1	PFCR0	PF3MD[2:0] = B'010	PF3/ICIORD#/SSISCK1/DV_DATA3/RxD3/SD_CMD/AUDATA1
	AUDIO_CLK	PECR0	PE0MD[1:0] = B'10	PE0/SCL0/AUDIO_CLK/IRQ0

Table 3.2.17 SH7267 Multiplex Pin Functions (ADC)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
ADC	AN3	PHCR0	PH3MD0 = B'1	PH3/AN3
	AN2	PHCR0	PH2MD0 = B'1	PH2/AN2
	AN1	PHCR0	PH1MD0 = B'1	PH1/AN1
	AN0	PHCR0	PH0MD0 = B'1	PH0/AN0

Table 3.2.18 SH7267 Multiplex Pin Functions (VDC3)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
VDC3	LCD_EXTCLK	PGCR5	PG20MD[2:0] = B'001	PG20/LCD_EXTCLK/SCK1
	LCD_CLK	PGCR4	PG19MD[2:0] = B'001	PG19/LCD_CLK/TIOC2B/TxD3/CTS1
	LCD_DE	PGCR4	PG18MD[2:0] = B'001	PG18/LCD_DE/TIOC2A/RxD3/RTS1
	LCD_HSYNC	PGCR4	PG17MD[2:0] = B'001	PG17/LCD_HSYNC/TIOC1B/TxD1
	LCD_VSYNC	PGCR4	PG16MD[2:0] = B'001	PG16/LCD_VSYNC/TIOC1A/RxD1
	LCD_DATA15	PGCR3	PG15MD[2:0] = B'001	PG15/LCD_DATA15/TIOC0D/TxD7
	LCD_DATA14	PGCR3	PG14MD[2:0] = B'001	PG14/LCD_DATA14/TIOC0C/RxD7
	LCD_DATA13	PGCR3	PG13MD[2:0] = B'001	PG13/LCD_DATA13/TIOC0B/TxD6
	LCD_DATA12	PGCR3	PG12MD[2:0] = B'001	PG12/LCD_DATA12/TIOC0A/RxD6
	LCD_DATA11	PGCR2	PG11MD[2:0] = B'001	PG11/LCD_DATA11/SSIWS0/IRQ3/TxD5/SIOFTxD
	LCD_DATA10	PGCR2	PG10MD[2:0] = B'001	PG10/LCD_DATA10/SSISCK0/IRQ2/RxD5/SIOFRxD
	LCD_DATA9	PGCR2	PG9MD[2:0] = B'001	PG9/LCD_DATA9/SSIRxD0/TxD4/SIOFSYNC
	LCD_DATA8	PGCR2	PG8MD[2:0] = B'001	PG8/LCD_DATA8/SSITxD0/RxD4/SIOFSCK
	LCD_DATA7	PGCR1	PG7MD[2:0] = B'001	PG7/LCD_DATA7/SD_CD/PINT7/IRQ7
	LCD_DATA6	PGCR1	PG6MD[2:0] = B'001	PG6/LCD_DATA6/SD_WP/PINT6/IRQ6
	LCD_DATA5	PGCR1	PG5MD[2:0] = B'001	PG5/LCD_DATA5/SD_D1/PINT5/IRQ5
	LCD_DATA4	PGCR1	PG4MD[2:0] = B'001	PG4/LCD_DATA4/SD_D0/PINT4/IRQ4
	LCD_DATA3	PGCR0	PG3MD[1:0] = B'01	PG3/LCD_DATA3/SD_CLK/PINT3
	LCD_DATA2	PGCR0	PG2MD[1:0] = B'01	PG2/LCD_DATA2/SD_CMD/PINT2
	LCD_DATA1	PGCR0	PG1MD[1:0] = B'01	PG1/LCD_DATA1/SD_D3/PINT1
	LCD_DATA0	PGCR0	PG0MD[1:0] = B'01	PG0/LCD_DATA0/SD_D2/PINT0
	LCD_M_DISP	PJCR0	PJ2MD[2:0] = B'101	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/LCD_M_DISP

Table 3.2.19 SH7267 Multiplex Pin Functions (PORT)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
PORT	PH5	PHCR1	PH5MD0 = B'0	PH5/AN5
	PH4	PHCR1	PH4MD0 = B'0	PH4/AN4
	PF1	PFCR0	PF1MD[2:0] = B'000	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/SD_D2/ AUDSYNC#
	PF0	PFCR0	PF0MD[2:0] = B'000	PF0/WAIT#/DV_DATA0/SCK2/TEND0/AUDCK
	PB22	PBCR5	PB22MD[2:0] = B'000	PB22/A22/CS4#/RxD4

3.3 LCD Module Interface

3.3.1 LCD Module Interface

The M3A-HS64G01 includes two flexible connectors and one MIL-spec connector for connecting LCD modules. The SH7267 on-chip VDC3 controls the LCD modules.

The following figure shows the LCD module interface block diagram.

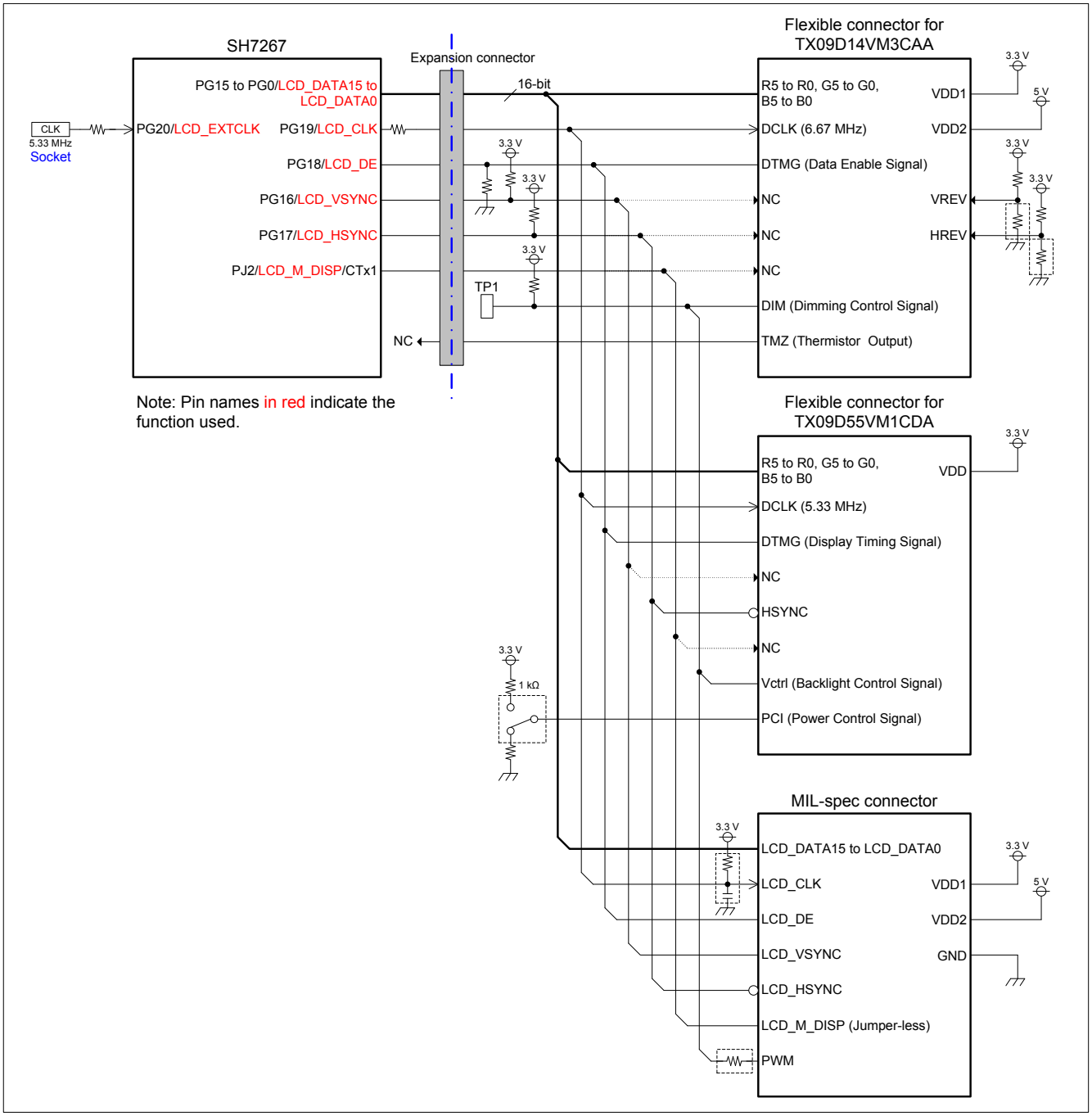


Figure 3.3.1 LCD Module Interface Block Diagram

3.3.2 Character LCD Module with LED Backlight

The M3A-HS64G01 includes a connector for 16 x 2 semi-transmissive character LCD module (SD1602H, SUNLIKE). This module cannot be used with the R0K572670C000BR.

3.4 Audio Modules

The M3A-HS64G01 includes two 96 kHz, 24-bit D/A converters with DIT (AK4353, Asahi Kasei EMD Corporation), and one 24-bit stereo codec with IPGA (AK4524). One D/A converter (AK4353, U12: D/A converter 2) can only be used with the R0K572670C000BR.

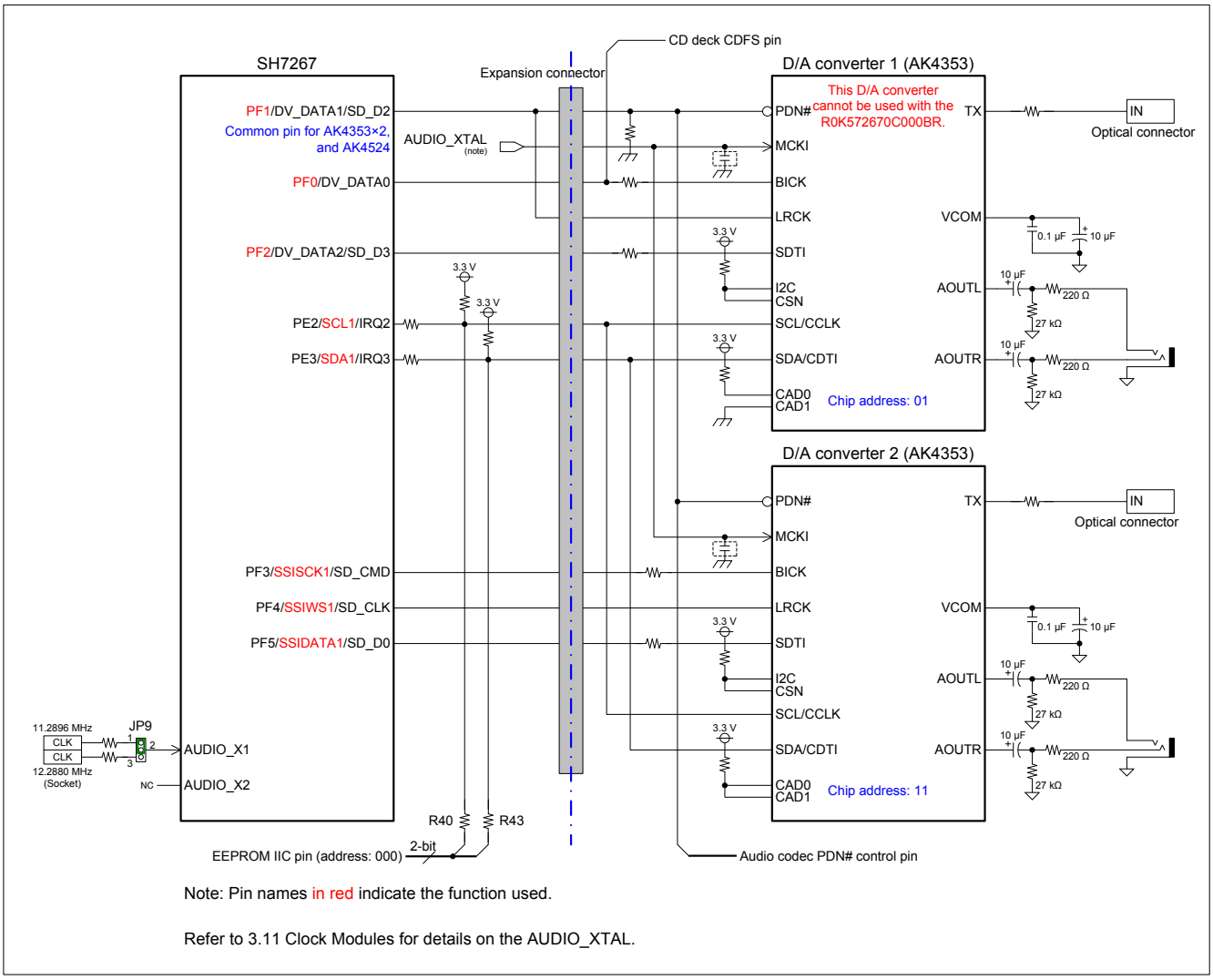
➢ AK4353, D/A Converter

SH7267 IIC3, SSIF, and I/O ports control AK4353.

- SH7267 IIC3 (Channel 1): Accesses the AK4353 registers to initialize AK4353, format data, and configure the attenuator
- SH7267 SSIF (Channel 1): Outputs the audio data
- SH7267 I/O ports (PF1): Powers down AK4353 at low, powers up AK4353 at high

Note: R0K572670C000BR allows for selecting 12.2880 MHz or 11.2896 MHz as the AK4353 system clock.

Figure 3.4.1 shows the D/A converter block diagram, and Table 3.4.1 lists the jumper setting (JP9 on the R0K572670C000BR).



Note: Pin names in red indicate the function used.

Refer to 3.11 Clock Modules for details on the AUDIO_XTAL.

Figure 3.4.1 D/A Converter Block Diagram

Table 3.4.1 Jumper Setting (JP9 on the R0K572670C000BR)

Number	1-2	2-3
JP9	Provides 11.2896 MHz with the AUDIO_X1 pin (default)	Provides 12.2880 MHz with the AUDIO_X1 pin

3.5 CD Deck Interface

The M3A-HS64G01 includes a CD deck interface connector. The SH7267 on-chip SSIF (Serial Sound Interface with FIFO) and RSPI (Renesas Peripheral Interface) control the CD deck.

The RSPI channel 0 pin is also used as the NAND flash memory controller (FLCTL) pin. When connecting it with the CD deck interface, set SW5-5 to ON, and SW5-6 to OFF.

The following figure shows the CD deck interface block diagram. Table 3.5.1 lists the DIP switches setting (SW5-5, and SW5-6 on the R0K572670C000BR).

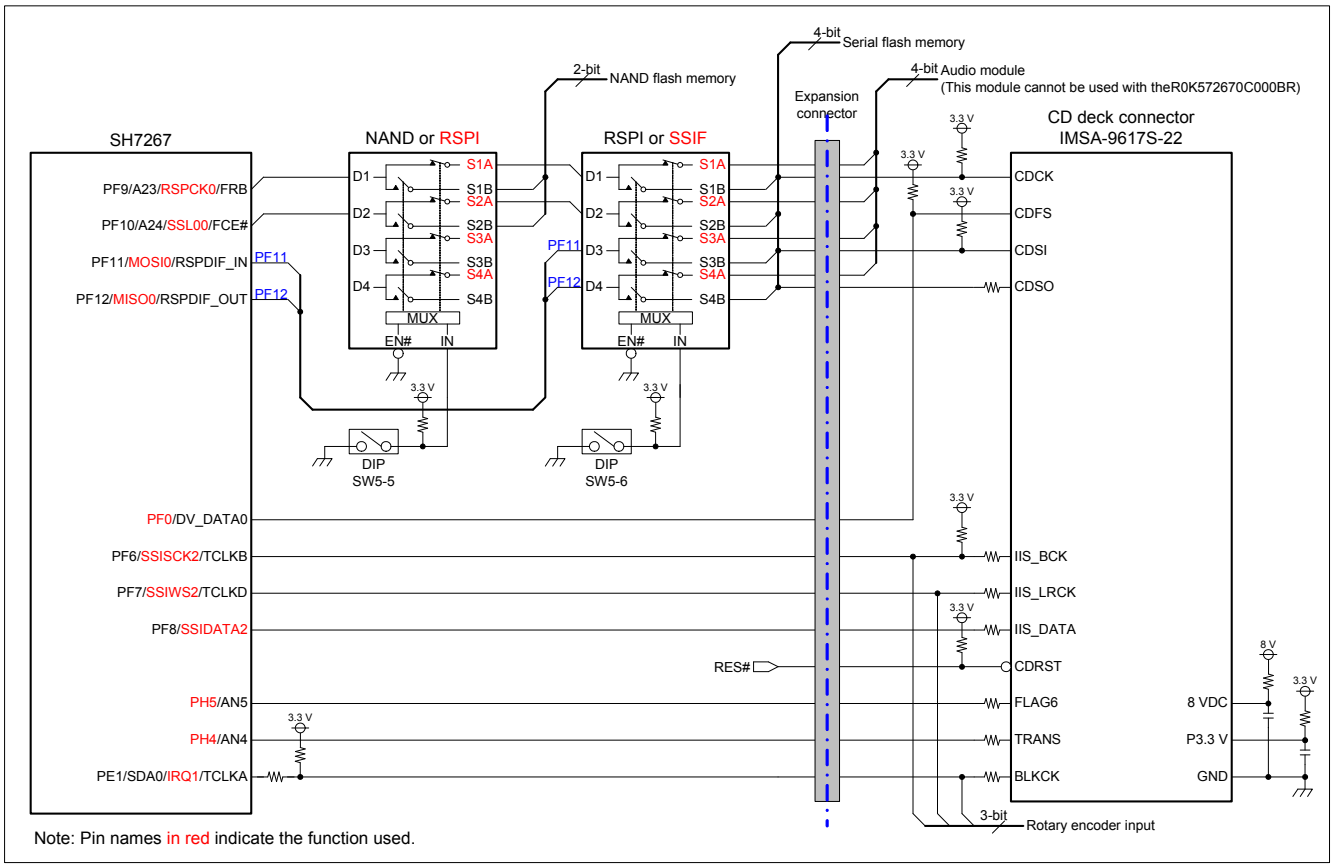


Figure 3.5.1 CD Deck Interface Block Diagram

Table 3.5.1 DIP Switches Setting (SW5 on the R0K572670C000BR)

Number	Function	
	OFF (High)	ON (Low)
SW5-5	Connected to the NAND flash memory	Connected to the device which is connected to RSPI/SSIF - default
SW5-6	Connected to the serial flash memory /CD deck (RSPI0)	Connected to the expansion connector (SSIF3) - default Note: This setting cannot be used with the R0K572670C000BR.

3.6 SD Card Interface

The M3A-HS64G01 includes an SD card slot. The SD card slot is connected to the SD Host Interface (SDHI) and the SD card slot built in the SH7267. This module cannot be used with the R0K572670C000BR.

3.7 UART Interface

The SH7267 has a Serial Communication Interface with FIFO (SCIF) and the M3A-HS64G01 includes a UART connector.

This module cannot be used with the R0K572670C000BR.

3.8 CAN Interface

The SH7267 includes RCAN-TL1 (Renesas CAN Time Trigger Level 1), the controller area network. SH7267 RCAN-TL1 channels 0 and 1 are connected to the CAN connector (3-pin, 2.5 mm pitch) on the M3A-HS64G01 via the voltage level shifter and the CAN driver IC.

The RCAN-TL1 channel 0 pin is also used as the SCIF channel 0 pin, and the IEBus™ controller (IEB) pin.

The figure below shows the CAN interface block diagram. Table 3.8.1 lists the jumpers setting (JP4, JP5, and JP8 on the R0K572670C000BR). Table 3.8.2 and Table 3.8.3 list the jumpers setting (JP4, JP5, JP8, and JP9 on the M3A-HS64G01).

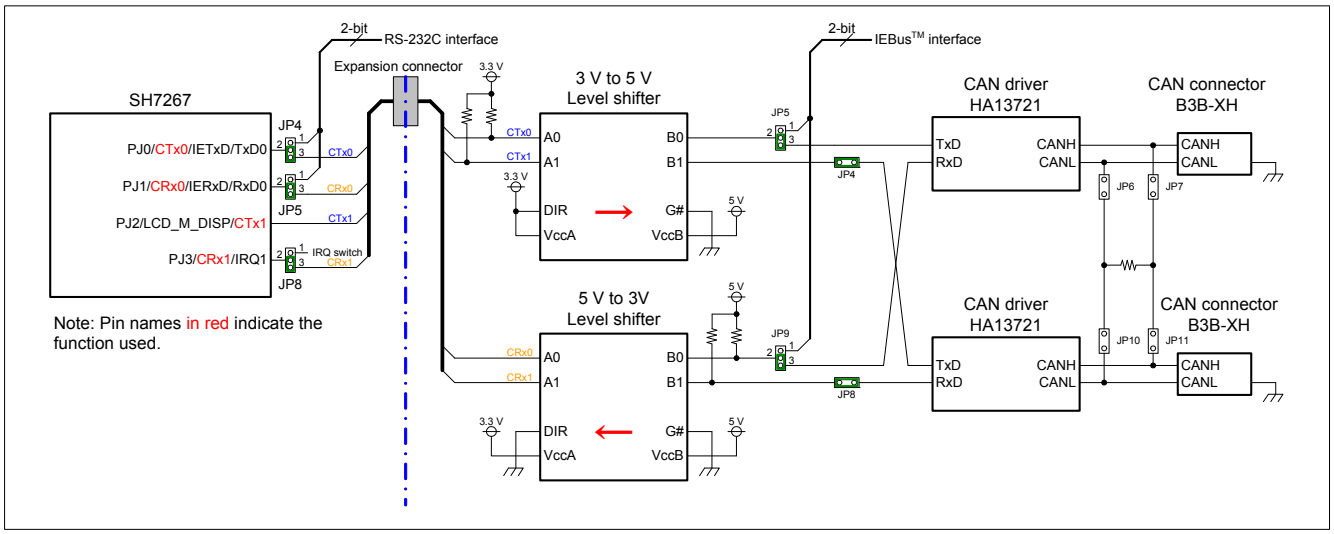


Figure 3.8.1 CAN Interface Block Diagram

Table 3.8.1 Jumpers Setting (JP4, JP5, and JP8 on the R0K572670C000BR)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) pin - default	Selects the CTx0 (RCAN-TL1) / IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) pin - default	Selects the CRx0 (RCAN-TL1) / IERxD (IEB) pins
JP8	Selects the IRQ1 switch – default	Selects the CRx1 (RCAN-TL1) pin

Table 3.8.2 Jumpers Setting (JP5, and JP9 on the M3A-HS64G01)

Number	1-2	2-3
JP5	Selects the IETxD (IEB) pin	Selects the CTx0 (RCAN-TL1) pin - default
JP9	Selects the IERxD (IEB) pin	Selects the CRx0 (RCAN-TL1) pin - default

Table 3.8.3 Jumper Setting (JP4, and JP8 on the M3A-HS64G01)

Number	1-2	None (Open)
JP4	Normal mode (Connects the CTx1 pin) - default	Debug mode (Leaves the CTx1 pin disconnected)
JP8	Normal mode (Connects the CRx1 pin) - default	Debug mode (Leaves the CRx1 pin disconnected)

3.9 IEBus™ Interface

The SH7267 includes an IEBus™ controller (IEB). The IEBus™ (Inter Equipment Bus™) is the bus for digital data transfer system on a small scale. The SH7267 IEB pin is connected to the IEBus connector (4-pin, 2.5 mm pitch) via the voltage level shifter and the IEBus™ driver IC on the M3A-HS64G01.

The IEB pin is also used as the SCIF channel 0 pin and the RCAN-TL1 channel 0 pin.

The figure below shows the IEBus™ interface block diagram. Table 3.9.1 lists the jumpers setting (JP4, and JP5 on the R0K572670C000BR). Table 3.9.2 lists the jumpers setting (JP5, and JP9 on the M3A-HS64G01).

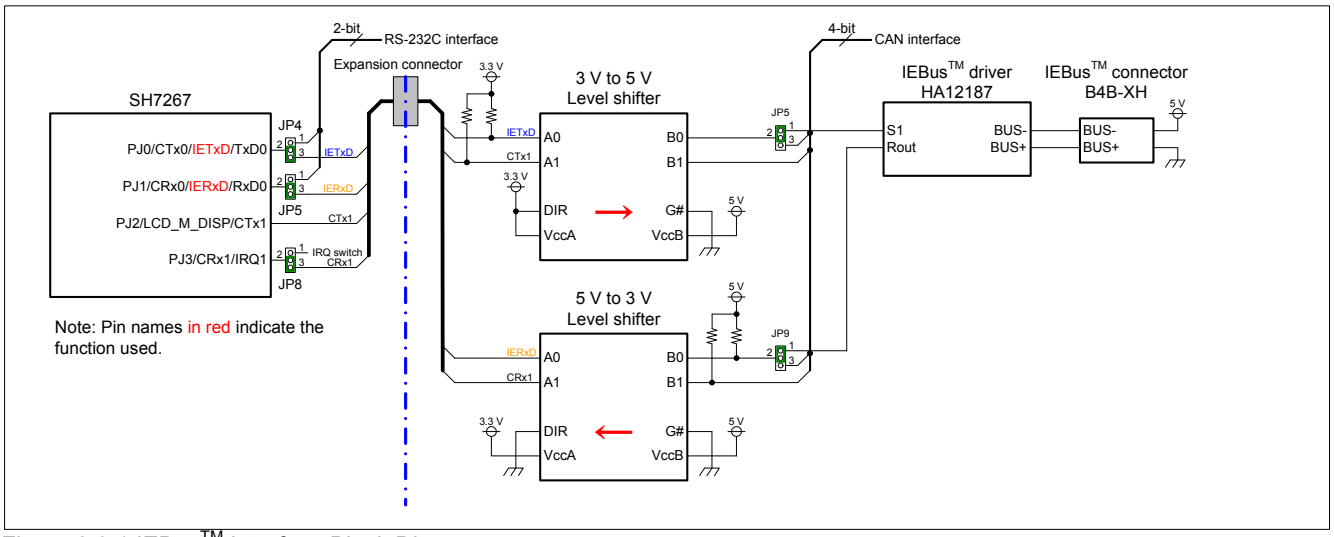


Figure 3.9.1 IEBus™ Interface Block Diagram

Table 3.9.1 Jumpers Setting (JP4, and JP5 on the R0K572670C000BR)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) - default	Selects the CTx0 (RCAN-TL1) / IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) - default	Selects the CRx0 (RCAN-TL1) / IERxD (IEB) pins

Table 3.9.2 Jumpers Setting (JP5, and JP9 on the M3A-HS64G01)

Number	1-2	2-3
JP5	Selects the IETxD (IEB) pin	Selects the CTx0 (RCAN-TL1) pin - default
JP9	Selects the IERxD (IEB) pin	Selects the CRx0 (RCAN-TL1) pin - default

3.10 I/O Ports

SH7267 I/O ports are connected to switches and LEDs on the M3A-HS64G01.

To use ports PH0 to PH3 as key input switches (4 switches x 4 inputs) via an A/D converter (ADC), set the ports as analog input pins (AN0 to AN3).

Port A can be used as a user interface by setting PB22 pin to high output.

The figure below shows the I/O ports block diagram. Table 3.10.1 lists the jumper setting (JP6 on the R0K572670C000BR). Table 3.10.2 lists the port A function switching.

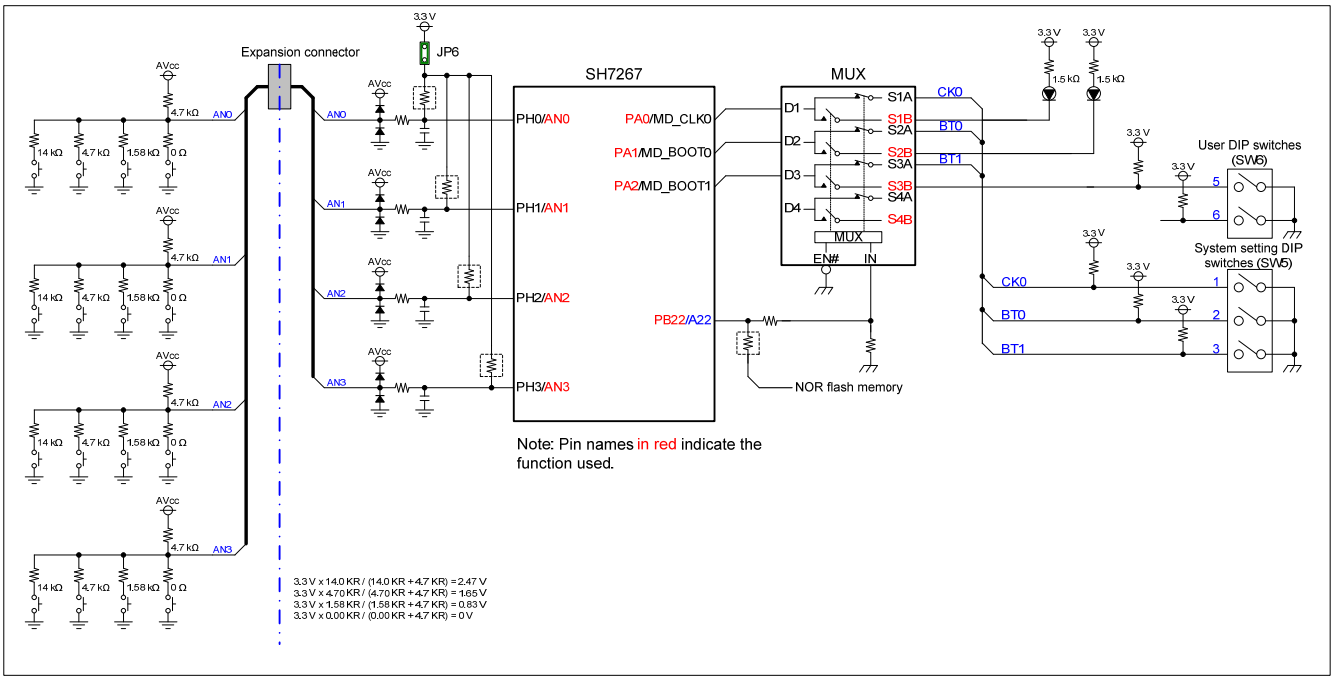


Figure 3.10.1 I/O Ports Block Diagram

Table 3.10.1 Jumper Setting (JP6 on the R0K572670C000BR)

Number	1-2	None (Open)
JP6	Uses PH[3:0] as an input port (default) (1)	Uses PH[3:0] as an analog input pin

Note 1: Mount R11 to R14 when using PH [3:0] as an input port.

Table 3.10.2 Port A Function Switching

Number	High output	Low output
PB22	Uses Port A as a user interface	Mode sampling (At power-up)

3.11 Clock Modules

Provide following clocks with the SH7267 on the R0K572670C000BR.

- SH7267 input clock: 12 MHz
- SH7267 RTC clock: 32.768 kHz
- SH7267 audio clock: 12.2880 MHz, and 11.2896 MHz (default)
- SH7267 USB clock: 48.00 MHz
- SH7267 LCD clock: 5.33 MHz

➢ How to select the system clock frequency of AK4353 (D/A converter)

SH7267 audio clock provides either 12.2880 MHz or 11.2896 MHz of the clock frequency with AK4353 by switching jumpers.

The figure below shows the clock module block diagram of the R0K572670C000BR and M3A-HS64G01.

Table 3.11.1 lists the audio clock switching (JP9 on the R0K572670C000BR).

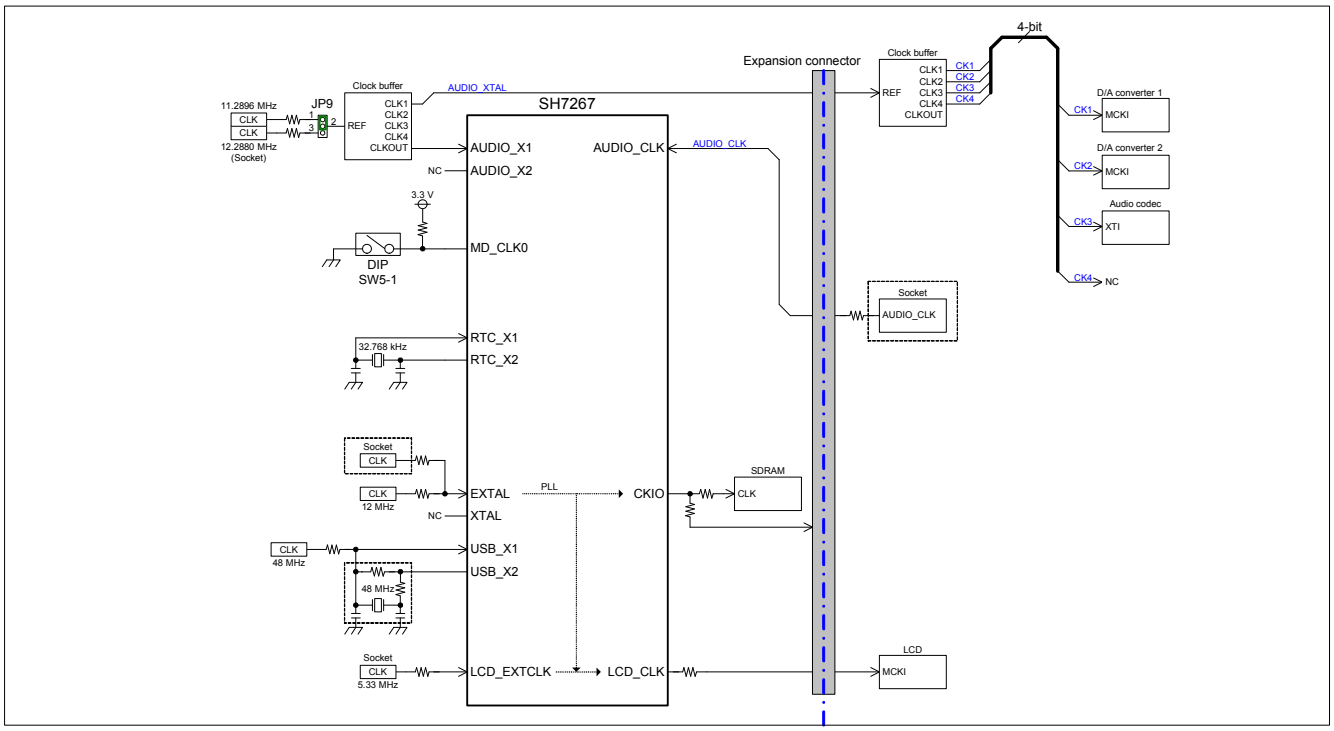


Figure 3.11.1 Clock Module Block Diagram

Table 3.11.1 Audio Clock Switching (JP9 on the R0K572670C000BR)

Number	1-2	2-3
JP9	Provides 11.2896 MHz with the AUDIO_X1 pin (default)	Provides 12.2880 MHz with the AUDIO_X1 pin

3.12 Reset Module

A reset IC controls reset signals connected to the SH7267, flash memory and peripheral I/Os on the R0K572670C000BR and M3A-HS64G01. There are two system reset options: power-on reset, and reset by switch. The following figure shows the reset module block diagram.

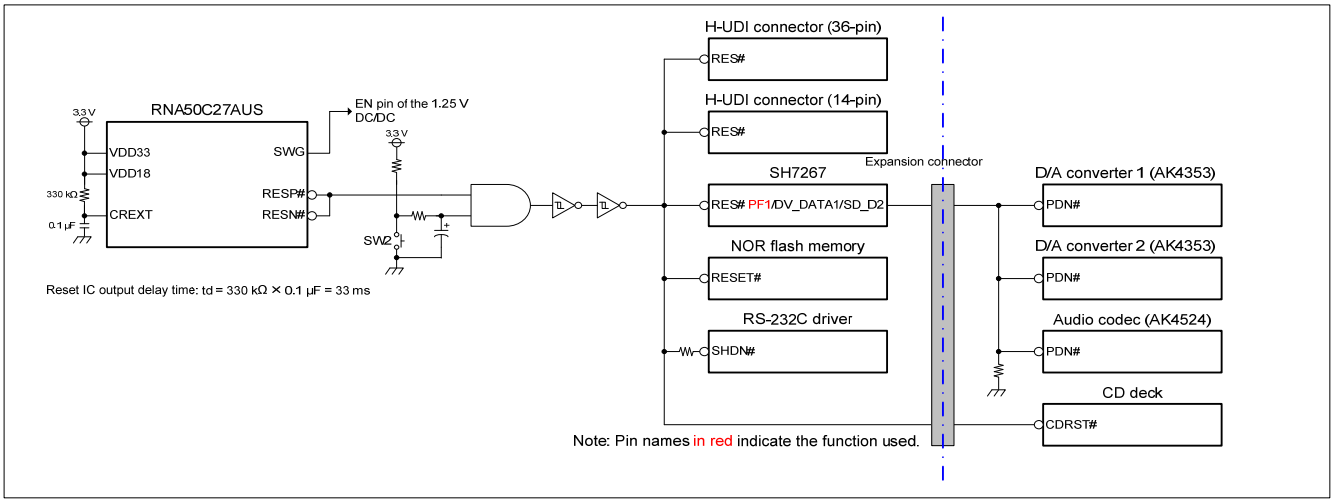


Figure 3.12.1 Reset Module Block Diagram

3.13 Power Supply Module

The M3A-HS64G01 is supplied 12 V power and the voltage regulator on the M3A-HS64G01 generates 8 V, and 5 V voltage.
5 V is supplied to the R0K572670C000BR, and the voltage regulator on the R0K572670C000BR generates digital voltage (3.3 V, 3VCC) and analog voltage (3.3 V, AVcc).
The following figure shows the power supply module block diagram.

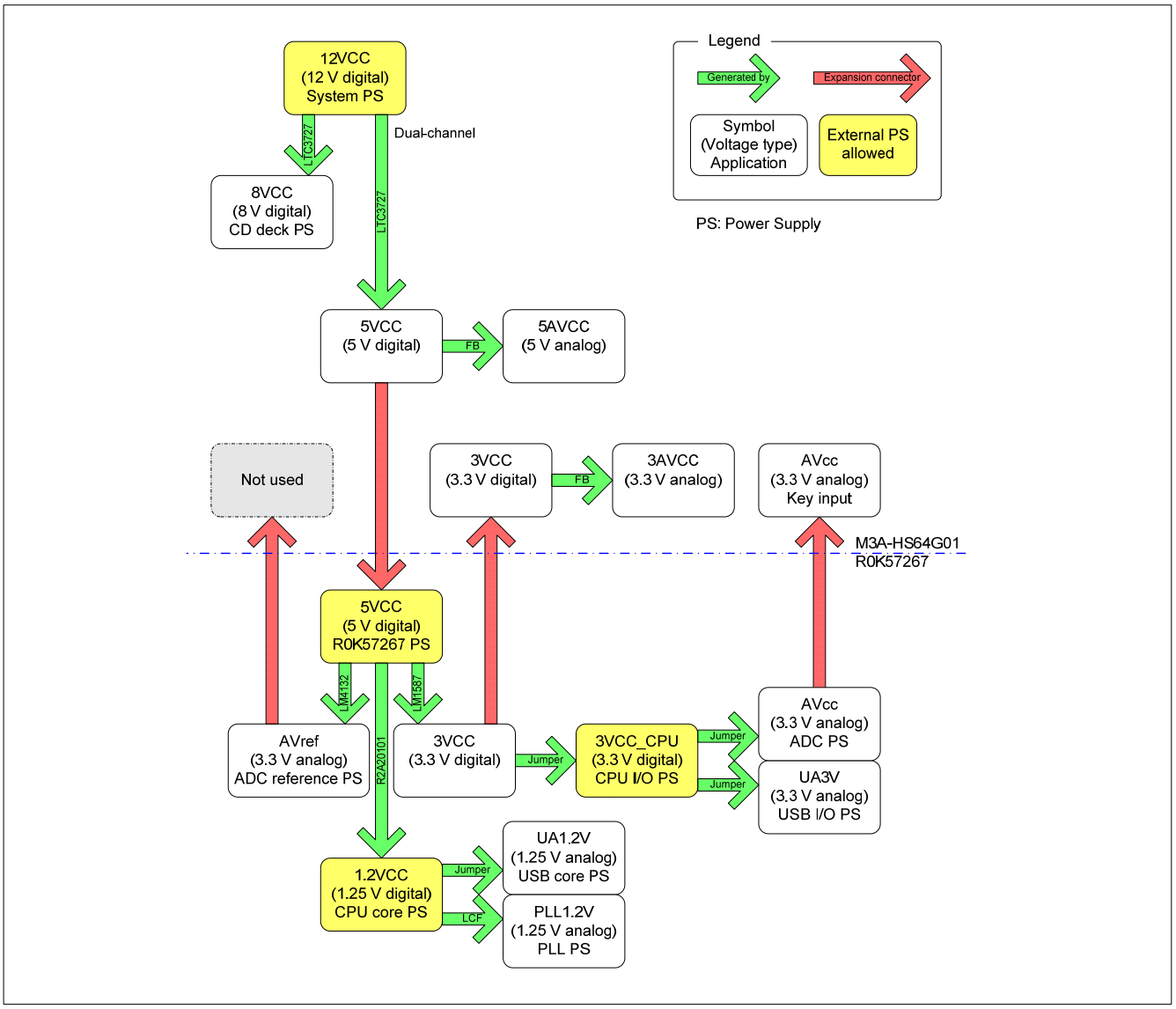


Figure 3.13.1 Power Supply Module Block Diagram

Chapter 4
M3A-HS64G02 Functions

4.1 Overview of Functions

M3A-HS64G02 includes the functional modules listed in the following table.

Table 4.1.1 M3A-HS64G02 Function Modules

Section	Function	Description
4.2	CPU	• SH7267
4.3	LCD Module Interface	• LCD module interface - Connects the SH7267 Video Display Controller 3 (VDC3) and LCD module connectors - Flexible connectors for LCD module are included • Character LCD module with LED backlight
4.4	Audio Module	• Connects the SH7267, and a D/A converter - 96 kHz 24-bit D/A converter: 1
4.5	Video Signal Input Module	• Connects the SH7267 Video Display Controller (VDC3) and a video decoder IC
4.6	SD Card Interface	• Connects the SH7267 SD Host Interface (SDHI), and an SD card slot
4.7	UART Interface	• Connects the SH7267 Serial Communication Interface with FIFO (SCIF) and a UART connector Note: This module cannot be used with the R0K572670C000BR.
4.8	CAN Interface	• Connects the SH7267 Controller Area Network (RCAN-TL1) and a CAN connector
4.9	IEBus™ Interface	• Connects the SH7267 IEBus™ controller (IEB) and IEBus™ connector
4.10	PWM Interface	• Connects the SH7267 Motor Control PWM Timer (PWM) and a 20-pin MIL-spec connector Note: This module cannot be used with the R0K572670C000BR.
4.11	MTU2 Interface	• Connects the SH7267 Multi Function Timer Pulse Unit 2 (MTU2) and a 20-pin MIL-spec connector
4.12	I/O Ports	• Connect the SH7267 I/O ports, LEDs, and DIP switches
4.13	Interrupt Switches	• Connects the SH7267 IRQ2 pin, IRQ3 pin, and push-button switches
4.14	Clock Modules	• Controls the system clock • Controls the peripheral I/O clock
4.15	Reset Module	• Resets devices on the M3A-HS64G02
4.16	Power Supply Module	• Controls the M3A-HS64G02 system power supply
-	Operating Specifications	• Connectors, switches, and LEDs Refer to Chapter 7 for details.

4.2 CPU

4.2.1 SH7267 Overview

The R0K572670C000BR includes the SH7267, the 32-bit RISC MCU that operates with a maximum frequency of 144 MHz.

4.2.2 SH7267 Pin Functions Used on the M3A-HS64G02

Table 4.2.1 to Table 4.2.6 list the SH7267 pin functions used on the M3A-HS64G02.

Table 4.2.1 SH7267 Pin Functions (1/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
1	PVcc				
2	PG18/LCD_DE/TIOC2A/ RxD3/RTS1	LCD_DE	Connected to the LCD module EN pin	CN9, pin 24	
3	Vss				
4	PB1/A1/LCD_HSYNC	A1	Address bus	CN4, pin 1	
5	Vcc				
6	PB2/A2/LCD_VSYNC	A2	Address bus	CN4, pin 2	
7	PB3/A3/LCD_DATA15	A3	Address bus	CN4, pin 3	
8	PB4/A4/TIOC0A/LCD_DATA14	A4	Address bus	CN4, pin 4	
9	PG9/LCD_DATA9/SSIRxD0/ TxD4/SIOFSYNC	LCD_DATA9	Connected to the LCD module D9 pin	CN9, pin 11	G4
10	PVcc				
11	PG8/LCD_DATA8/SSITxD0/ RxD4/SIOFSCK	LCD_DATA8	Connected to the LCD module D8 pin	CN9, pin 12	G3
12	Vss				
13	PB5/A5/TIOC0B/LCD_DATA13	A5	Address bus	CN4, pin 5	
14	PB6/A6/TIOC0C/LCD_DATA12	A6	Address bus	CN4, pin 6	
15	PB7/A7/TIOC0D/LCD_DATA11	A7	Address bus	CN4, pin 9	
16	PB8/A8/TIOC1A/LCD_DATA10	A8	Address bus	CN4, pin 10	
17	PVcc				
18	PB9/A9/TIOC1B/LCD_DATA9	A9	Address bus	CN4, pin 11	
19	Vss				
20	PB10/A10/TIOC2A/LCD_DATA8	A10	Address bus	CN4, pin 12	
21	Vcc				
22	PB11/A11/TIOC2B/LCD_DATA7	A11	Address bus	CN4, pin 13	
23	PB12/A12/TIOC3A/LCD_DATA6	A12	Address bus	CN4, pin 14	
24	PB13/A13/TIOC3B/LCD_DATA5	A13	Address bus	CN4, pin 17	
25	PB14/A14/TIOC3C/LCD_DATA4	A14	Address bus	CN4, pin 18	
26	PB15/A15/TIOC3D/LCD_DATA3	A15	Address bus	CN4, pin 19	
27	PG7/LCD_DATA7/SD_CD/ PINT7/IRQ7	LCD_DATA7	Connected to the LCD module D7 pin	CN9, pin 9	G2
28	PG6/LCD_DATA6/SD_WP/ PINT6/IRQ6	LCD_DATA6	Connected to the LCD module D6 pin	CN9, pin 7	G1
29	PVcc				
30	PG5/LCD_DATA5/SD_D1/PINT5 /IRQ5	LCD_DATA5	Connected to the LCD module D5 pin	CN9, pin 8	G0
31	Vss				
32	PG4/LCD_DATA4/SD_D0/PINT4 /IRQ4	LCD_DATA4	Connected to the LCD module D4 pin	CN9, pin 6	B5

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 4.2.2 SH7267 Pin Functions (2/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
33	Vcc				
34	PB16/A16/TIOC4A/LCD_DATA2	A16	Address bus	CN4, pin 20	
35	PB17/A17/TIOC4B/LCD_DATA1/ SCK1	A17	Address bus	CN4, pin 21	
36	PB18/A18/TIOC4C/LCD_DATA0 /TxD1	A18	Address bus	CN4, pin 22	
37	PB19/A19/TIOC4D/RxD1	A19	Address bus	CN4, pin 25	
38	PB20/A20/SPDIF_IN/SCK4	A20	Address bus	CN4, pin 26	
39	PB21/A21/SPDIF_OUT/TxD4	A21	Address bus	CN4, pin 27	
40	PVcc				
41	CKIO	CKIO	Connected to the SDRAM CLK pin	CN6, pin 20	
42	Vss				
43	PB22/A22/CS4#/RxD4	PB22	Switches the system setting/user interface	CN4, pin 28	Low: MD High: IO
44	NMI	NMI	Non-maskable interrupt	–	
45	PLLVcc				
46	RES#	RES#	Reset input	CN7, pin 6	
47	PLLVss				
48	PA0/MD_CLK0	PA0	Connected to LED2 as a user output port	CN1, pin 10	PB22: High
		MD_CLK0	Connected to SW5-1 as clock mode input 0		PB22: Low
49	PA1/MD_BOOT0	PA1	Connected to LED3 as a user output port	CN1, pin 9	PB22: High
		MD_BOOT0	Connected to SW5-2 as boot mode input 0		PB22: Low
50	EXTAL	EXTAL	Connects the system external clock to MCU	–	12 MHz
51	XTAL	XTAL	Open	–	
52	PG3/LCD_DATA3/SD_CLK/ PINT3	LCD_DATA3	Connected to the LCD module D3 pin	CN9, pin 3	B4
53	PG2/LCD_DATA2/SD_CMD/ PINT2	LCD_DATA2	Connected to the LCD module D2 pin	CN9, pin 4	B3
54	PG1/LCD_DATA1/SD_D3/PINT1	LCD_DATA1	Connected to the LCD module D1 pin	CN9, pin 1	B2
55	PG0/LCD_DATA0/SD_D2/PINT0	LCD_DATA0	Connected to the LCD module D0 pin	CN9, pin 2	B1, B0
56	Vss				
57	PVcc				
58	PG20/LCD_EXTCLK/SCK1	LCD_EXTCLK	Connects the LCD module external clock to MCU	CN9, pin 26	Default: 5.33 MHz
59	Vss				
60	RTC_X1	RTC_X1	Connects the real-time clock resonator to MCU	–	32.768 kHz
61	RTC_X2	RTC_X2		–	
62	PA2/MD_BOOT1	PA2	Connected to SW6-5 as a user input port	CN1, pin 8	PB22: High
		MD_BOOT1	Connected to SW5-3 as boot mode input 1		PB22: Low
63	USB_X1	USB_X1	Connects the USB external clock to MCU	_	48 MHz
64	USB_X2	USB_X2	Open	_	
65	ASEMD#	ASEMD#	ASE mode select	_	H-UDI
66	USBDPVcc				
67	USBDPVss				
68	DM	DM	USB differential signal D− data	_	
69	DP	DP	USB differential signal D+ data	_	
70	VBUS	VBUS	VBUS input	_	
71	USBDVcc				
72	USBDVss				
73	REFRIN	REFRIN	Reference input	–	Connects 5.6 kΩ ± 1% resistor

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 4.2.3 SH7267 Pin Functions (3/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
74	USBAPVss				
75	USBAPVcc				
76	USBAVcc				
77	USBAVss				
78	USBUVcc				
79	USBUVss				
80	PH0/AN0	AN0	Connected to the push-button switch as key input	CN3, pin 4	
81	PH1/AN1	AN1	Connected to the push-button switch as key input	CN3, pin 3	
82	PH2/AN2	AN2	Connected to the push-button switch as key input	CN3, pin 8	
83	PH3/AN3	AN3	Connected to the push-button switch as key input	CN3, pin 7	
84	AVss				
85	PH4/AN4	–	Connected to the PWM connector (J5)	CN1, pin 2	JP3: 1-2
		PH4	Connected to the test pin (TP3)		JP3: 2-3
86	AVref				
87	PH5/AN5	–	Connected to the PWM connector (J5)	CN1, pin 4	JP3: 1-2
		PH5	Connected to the test pin (TP2)		JP3: 2-3
88	AVcc				
89	TRST#	TRST#	Initialization-signal input pin	–	H-UDI
90	ASEBRKAK#/ASEBRK#	ASEBRKAK#	Break mode acknowledge	–	H-UDI
		ASEBRK#	Break request		
91	TDO	TDO	Test data output	–	H-UDI
92	TDI	TDI	Test data input	–	H-UDI
93	TMS	TMS	Test mode select	–	H-UDI
94	TCK	TCK	Test clock	–	H-UDI
95	AUDIO_X2	AUDIO_X2	Open	–	
96	AUDIO_X1	AUDIO_X1	Connects the audio external clock to MCU	–	Switched by JP9
97	PG24/MISO1/TIOC0D	PG24	Connected to the character LCD E pin	CN6, pin 13	
98	PVcc				
99	PG23/MOSI1/TIOC0C	PG23	Connected to the character LCD RS pin	CN6, pin 12	
100	Vss				
101	PG22/SSL10/TIOC0B	TIOC0B	Connected to the MTU2 connector (J16)	CN9, pin 27	
102	Vcc				
103	PG21/RSPCK1/TIOC0A	TIOC0A	Connected to the MTU2 connector (J16)	CN9, pin 28	
104	PJ3/CRx1/CRx0/CRx1/IRQ1/ AUDIO_XOUT/WDTOVF#	IRQ1	IRQ1 switch	–	JP8: 1-2
		CRx1	Connected to the CAN driver IC (U16)	CN1, pin 17	JP8: 2-3
105	PJ2/CTx1/CTx0&CTx1/CS2#/ SCK0/LCD_M_DISP	CTx1	Connected to the CAN driver IC (U16)	CN1, pin 18	
		LCD_M_DISP	LCD AC control signal		
106	PJ1/CRx0/IERxD/IRQ0/RxD0	RxD0	Connected to the RS-232C connector (J10)	–	JP5: 1-2
		CRx0	Connected to the CAN driver IC (U14)	CN1, pin 19	JP5: 2-3
		IERxD	Connected to the IEBus™ driver IC		
107	PJ0/CTx0/IETxD/CS1#/TxD0/ A0	TxD0	Connected to the RS-232C connector (J10)	–	JP4: 1-2
		CTx0	Connected to the CAN driver IC (U14)	CN1, pin 20	JP4: 2-3
		IETxD	Connected to the IEBus™ driver IC		
108	PF8/CE2B#/SSIDATA2/ DV_CLK/SD_CD	DV_CLK	Connected to the video decoder IC CLK_27MO pin	CN7, pin 27	SW6-6: ON
		PF8	Connected to the character LCD DB7 pin	CN7, pin 15	SW6-6: OFF
		–	Connected to the PWM connector (J5)		JP3: 1-2
		SD_CD	Connected to the SD card slot CD pin		SW6-6: OFF JP3: 2-3

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 4.2.4 SH7267 Pin Functions (4/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
109	PF7/CE2A#/SSIWS2/ DV_DATA7/TCLKD/SD_WP	DV_DATA7	Connected to the video decoder IC D7 pin	CN7, pin 28	SW6-6: ON
		PF7	Connected to the character LCD DB6 pin	CN7, pin 16	SW6-6: OFF JP3: 1-2
		–	Connected to the PWM connector (J5)		
		SD_WP	Connected to the SD card slot WP pin		SW6-6: OFF JP3: 2-3
110	PVcc				
111	PF6/CS6#/CE1B#/SSISCK2/ DV_DATA6/TCLKB/SD_D1	DV_DATA6	Connected to the video decoder IC D6 pin	CN7, pin 25	SW6-6: ON
		PF6	Connected to the character LCD DB5 pin	CN7, pin 13	SW6-6: OFF JP3: 1-2
		–	Connected to the PWM connector (J5)		
		SD_D1	Connected to the SD card slot DAT1 pin		SW6-6: OFF JP3: 2-3
112	Vss				
113	PF5/CS5#/CE1A#/SSIDATA1/ DV_DATA5/TCLKC/SD_D0/ AUDATA3	AUDATA3	Connected to the H-UDI port connector (J3)	CN7, pin 23	AUD
		DV_DATA5	Connected to the video decoder IC D5 pin		SW6-6: ON
		PF5	Connected to the character LCD DB4 pin	CN7, pin 14	SW6-6: OFF JP3: 1-2
		–	Connected to the PWM connector (J5)		
		SD_D0	Connected to the SD card slot DAT0 pin		SW6-6: OFF JP3: 2-3
114	Vcc				
115	PF4/ICIOWR#/AH#/SSIWS1/ DV_DATA4/TxD3/SD_CLK/ AUDATA2	AUDATA2	Connected to the H-UDI port connector (J3)	CN7, pin 24	AUD
		DV_DATA4	Connected to the video decoder IC D4 pin		SW6-6: ON
		PF4	Connected to the character LCD DB3 pin	CN7, pin 3	SW6-6: OFF JP3: 1-2
		–	Connected to the PWM connector (J5)		
		SD_CLK	Connected to the SD card slot CLK pin		SW6-6: OFF JP3: 2-3
116	PF3/ICIORD#/SSISCK1/ DV_DATA3/RxD3/SD_CMD/ AUDATA1	AUDATA1	Connected to the H-UDI port connector (J3)	CN7, pin 22	AUD
		DV_DATA3	Connected to the video decoder IC D3 pin		SW6-6: ON
		PF3	Connected to the character LCD DB2 pin	CN7, pin 4	SW6-6: OFF JP3: 1-2
		–	Connected to the PWM connector (J5)		
		SD_CMD	Connected to the SD card slot CMD pin		SW6-6: OFF JP3: 2-3
117	PF2/BACK#/DV_DATA2/TxD2/ DACK0/SD_D3/AUDATA0	AUDATA0	Connected to the H-UDI port connector (J3)	CN7, pin 19	AUD
		DV_DATA2	Connected to the video decoder IC D2 pin		SW6-6: ON
		PF2	Connected to the character LCD DB1 pin	CN7, pin 1	SW6-6: OFF JP3: 1-2
		–	Connected to the PWM connector (J5)		
		SD_D3	Connected to the SD card slot DAT3 pin		SW6-6: OFF JP3: 2-3
118	PF1/BREQ#/DV_DATA1/RxD2/ DREQ0/SD_D2/AUDSYNC#	AUDSYNC#	Connected to the H-UDI port connector (J3)	CN7, pin 20	AUD
		DV_DATA1	Connected to the video decoder IC D1 pin		SW6-6: ON
		–	Connected to the MTU2 connector (J16)	CN9, pin 29	
		PF1	Connected to the character LCD DB0 pin	CN7, pin 2	SW6-6: OFF JP3: 1-2
		–	Connected to the PWM connector (J5)		
		SD_D2	Connected to the SD card slot DAT2 pin		SW6-6: OFF JP3: 2-3
119	PF0/WAIT#/DV_DATA0/SCK2/ TEND0/AUDCK	AUDCK	Connected to the H-UDI port connector (J3)	CN7, pin 17	AUD
		DV_DATA0	Connected to the video decoder IC D0 pin		
		–	Not connected	CN7, pin 32	
120	PVcc				
121	PG17/LCD_HSYNC/TIOC1B/ TxD1	LCD_HSYNC	Connected to the LCD module HSYNC pin	CN9, pin 21	
122	Vss				
123	PG16/LCD_VSYNC/TIOC1A/ RxD1	LCD_VSYNC	Connected to the LCD module VSYNC pin	CN9, pin 19	

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 4.2.5 SH7267 Pin Functions (5/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
124	PF12/BS#/MISO0/TIOC3D/ SPDIF_OUT	MISO0	Connected to the serial flash memory SO pin	CN7, pin 33	SW5-6: OFF
		–	Connected to the MTU2 connector (J16)		
		–	Connected to the through-hole (MH2)		
		PF12	Connected to the AK4353 PDN# pin	CN7, pin 38	SW5-6: ON JP3: 2-3
		–	Connected to the PWM connector (J5)		SW5-6: ON JP3: 1-2
125	PF11/A25/SSIDATA3/MOSI0/ TIOC3C/SPDIF_IN	MOSI0	Connected to the serial flash memory SI pin	CN7, pin 31	SW5-6: OFF
		–	Connected to the MTU2 connector (J16)		
		SSIDATA3	Connected to the AK4353 SDTI pin	CN7, pin 37	SW5-6: ON JP3: 2-3
		–	Connected to the PWM connector (J5)		SW5-6: ON JP3: 1-2
126	PVcc				
127	PF10/A24/SSIWS3/SSL00/ TIOC3B/FCE#	SSL00	Connected to the serial flash memory CS# pin	–	SW5-5: ON SW5-6: OFF
		SSIWS3	Connected to the AK4353 LRCK pin	CN7, pin 35	SW5-5: ON SW5-6: ON JP3: 2-3
		–	Connected to the PWM connector (J5)		SW5-5: ON SW5-6: ON JP3: 1-2
		FCE#	Connected to the NAND flash memory CE# pin	–	SW5-5: OFF
128	Vss				
129	PF9/A23/SSISCK3/RSPCK0/ TIOC3A/FRB	RSPCK0	Connected to the serial flash memory SCK pin	CN7, pin 30	SW5-5: ON SW5-6: OFF
		SSISCK3	Connected to the AK4353 BICK pin	CN7, pin 36	SW5-5: ON SW5-6: ON JP3: 2-3
		–	Connected to the PWM connector (J5)		SW5-5: ON SW5-6: ON JP3: 1-2
		FRB	Connected to the NAND flash memory R/B# pin	–	SW5-5: OFF
130	Vcc				
131	PD15/D15/NAF7/PWM2H	D15/NAF7	Data bus	CN8, pin 19	
132	PD14/D14/NAF6/PWM2G	D14/NAF6	Data bus	CN8, pin 17	
133	PE5/SDA2/DV_HSYNC	DV_HSYNC	Connected to the video decoder IC HSYNC pin	CN7, pin 12	
134	PE4/SCL2/DV_VSYNC	DV_VSYNC	Connected to the video decoder IC VSYNC pin	CN7, pin 9	
135	PE3/SDA1/IRQ3	SDA1	Connected to the EEPROM SDA pin	CN7, pin 10	JP10: 1-2
			Connected to the AK4353 SDA/CDTI pin		JP2: 1-2
		IRQ3	IRQ3 switch		JP2: 2-3
136	PE2/SCL1/IRQ2	SCL1	Connected to the EEPROM SCL pin	CN7, pin 7	JP9: 1-2
			Connected to the AK4353 SCL/CCLKI pin		JP1: 1-2
		IRQ2	IRQ2 switch		JP1: 2-3
137	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ ADTRG#/LCD_EXTCLK	SDA0	Connected to the external IIC connector (J3)	CN7, pin 8	
			Connected to the video decoder IC SDA pin		
138	PE0/SCL0/AUDIO_CLK/IRQ0	SCL0	Connected to the external IIC connector (J3)	CN7, pin 5	
			Connected to the video decoder IC SCL pin		
139	PD13/D13/NAF5/PWM2F	D13/NAF5	Data bus	CN8, pin 14	
140	PD12/D12/NAF4/PWM2E	D12/NAF4	Data bus	CN8, pin 12	
141	PVcc				
142	PD11/D11/NAF3/PWM2D	D11/NAF3	Data bus	CN8, pin 9	
143	Vss				

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

Table 4.2.6 SH7267 Pin Functions (6/6)

No.	Name	Symbol	Description	Expansion connector	Remarks
144	PD10/D10/NAF2/PWM2C	D10/NAF2	Data bus	CN8, pin 7	
145	PD9/D9/NAF1/PWM2B	D9/NAF1	Data bus	CN8, pin 4	
146	PD8/D8/NAF0/PWM2A	D8/NAF0	Data bus	CN8, pin 2	
147	PD7/D7/FWE#/PWM1H	D7/FWE#	Connected to the data bus and the NAND flash memory WE# pin	CN8, pin 18	Auto-switch
148	PD6/D6/FALE/PWM1G	D6/FALE	Connected to the data bus and the NAND flash memory ALE pin	CN8, pin 16	Auto-switch
149	PD5/D5/FCLE/PWM1F	D5/FCLE	Connected to the data bus and the NAND flash memory CLE pin	CN8, pin 13	Auto-switch
150	PG15/LCD_DATA15/TIOC0D/ TxD7	LCD_DATA15	Connected to the LCD module D15 pin	CN9, pin 20	R5
151	PG14/LCD_DATA14/TIOC0C/ RxD7	LCD_DATA14	Connected to the LCD module D14 pin	CN9, pin 17	R4
152	PVcc				
153	Vss				
154	PG13/LCD_DATA13/TIOC0B/ TxD6	LCD_DATA13	Connected to the LCD module D13 pin	CN9, pin 18	R3
155	PG12/LCD_DATA12/TIOC0A/ RxD6	LCD_DATA12	Connected to the LCD module D12 pin	CN9, pin 16	R2
156	PD4/D4/FRE#/PWM1E	D4/FRE#	Connected to the data bus and the NAND flash memory RE# pin	CN8, pin 11	Auto-switch
157	PD3/D3/PWM1D	D3	Data bus	CN8, pin 8	
158	PD2/D2/PWM1C	D2	Data bus	CN8, pin 6	
159	PD1/D1/PWM1B	D1	Data bus	CN8, pin 3	
160	PD0/D0/PWM1A	D0	Data bus	CN8, pin 1	
161	PC0/CS0#/SSIWS0	CS0#	Connected to the NOR flash memory CE# pin	CN6, pin 5	
162	PVcc				
163	PC1/RD#/SSISCK0	RD#	Connected to the NOR flash memory OE# pin	CN6, pin 6	
164	Vss				
165	PC2/RD/WR#/SSIRxD0	RD/WR#	Connected to the SDRAM WE# pin	CN6, pin 7	
166	PC3/WE0#/DQML/SSITxD0	WE0#	Connected to the NOR flash memory WE# pin	CN6, pin 8	
		DQML	Connected to the SDRAM DQML pin		
167	PC4/WE1#/DQMU/WE#	DQMU	Connected to the SDRAM DQMU pin	CN6, pin 9	
168	PC5/RAS#/TIOC4A/IRQ4	RAS#	Connected to the SDRAM RAS# pin	–	SW5-4: OFF
		TIOC4A	Connected to the MTU2 connector (J16)	CN6, pin 14	SW5-4: ON
169	PG11/LCD_DATA11/SSIWS0/ IRQ3/TxD5/SIOFTxD	LCD_DATA11	Connected to the LCD module D11 pin	CN9, pin 13	R1, R0
170	PVcc				
171	PG10/LCD_DATA10/SSISCK0 /IRQ2/RxD5/SIOFRxD	LCD_DATA10	Connected to the LCD module D10 pin	CN9, pin 14	G5
172	Vss				
173	PC6/CAS#/TIOC4B/IRQ5	CAS#	Connected to the SDRAM CAS# pin	–	SW5-4: OFF
		TIOC4B	Connected to the MTU2 connector (J16)	CN6, pin 15	SW5-4: ON
174	PC7/CKE/TIOC4C/IRQ6	CKE	Connected to the SDRAM CKE pin	–	SW5-4: OFF
		TIOC4C	Connected to the MTU2 connector (J16)	CN6, pin 16	SW5-4: ON
175	PC8/CS3#/TIOC4D/IRQ7	CS3#	Connected to the SDRAM CS# pin	–	SW5-4: OFF
		TIOC4D	Connected to the MTU2 connector (J16)	CN6, pin 17	SW5-4: ON
176	PG19/LCD_CLK/TIOC2B/ TxD3/CTS1	LCD_CLK	Connected to the LCD module CLK pin	CN9, pin 23	

Legend: : 3.3 V power supply, : 1.25 V power supply, : GND

4.2.3 M3A-HS64G02 Module Availability

The following table shows which combination of modules can/cannot be used.

Table 4.2.7 M3A-HS64G02 Module Availability

				R0K572670C000BR												R0K572670C000BR+M3A-HS64G02														
	SH7267 Peripherals	Component No.	Module Name	NOR flash memory	SDRAM	NAND flash memory	EEPROM	Serial flash memory	USB	H-UDI (14-pin)	H-UDI (36-pin)	LED	NMI switch	IRQ1 switch	DIP switches	RS-232C	Character LCD	SD card	D/A converter	UART	IIC	LCD	IEBus™	CAN0	CAN1	Key input switch	IRQ2 switch	IRQ3 switch	PWM	Video decoder	MTU2
R0K572670C000BR	BSC	U6	NOR flash memory		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	BSC	U9	SDRAM	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	(9)
	FLCTL	U7	NAND flash memory	Y	Y		Y	(2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(2)	–	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	IIC3	U8	EEPROM	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	RSPI	U10	Serial flash memory	Y	Y	(2)	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(2)	–	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	USB	J1 and J2	USB	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	H-UDI	J7	H-UDI (14-pin)	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	H-UDI, AUD	J3	H-UDI (36-pin)	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	N	Y
	I/O ports	LED2 and LED3	LED	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	(1)	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	INTC	SW3	NMI switch	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	INTC	SW4	IRQ1 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	–	Y	Y	Y	Y	(5)	Y	Y	Y	–	Y	Y
	I/O ports	SW5 and SW6	DIP switches	Y	Y	Y	Y	Y	Y	Y	Y	(1)	Y	Y		Y	Y	Y	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	SCIF	J10	RS-232C	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	–	Y	Y	(3)	(3)	Y	Y	Y	Y	–	Y	Y
R0K572670C000BR+M3A-HS64G02	I/O ports	J1	Character LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		(6)	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	(10)	N
	SDHI	J4	SD card	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(6)		Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–	(10)	Y
	SSIF, IIC3	U10	D/A converter	Y	Y	(2)	Y	(2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		–	Y	Y	Y	Y	Y	Y	(4)	(4)	–	Y	Y
	SCIF	J2	UART	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–	–	–	–	–
	IIC3	J3	IIC	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–		Y	Y	Y	Y	Y	Y	Y	–	Y	Y
	VDC3	J10 to J12	LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y		Y	Y	(8)	Y	Y	Y	–	Y	(11)
	IEBus	J13	IEBus™	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(3)	Y	Y	Y	–	Y	Y		(7)	Y	Y	Y	Y	Y	–	Y	Y
	RCAN	J14	CAN0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(3)	Y	Y	Y	–	Y	Y	(7)		Y	Y	Y	Y	Y	–	Y	Y
	RCAN	J15	CAN1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(5)	Y	Y	Y	Y	Y	–	Y	(8)	Y	Y		Y	Y	Y	Y	–	Y	Y
	I/O ports	SW4 to SW19	Key input switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	Y	Y	Y	Y	Y		Y	Y	–	Y	Y
	INTC	SW1	IRQ2 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(4)	–	Y	Y	Y	Y	Y	Y		Y	–	Y	Y
	INTC	SW2	IRQ3 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(4)	–	Y	Y	Y	Y	Y	Y	Y		–	Y	Y
	PWM	J5	PWM	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–
	VDC3	U11	Video decoder	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	(10)	(10)	Y	–	Y	Y	Y	Y	Y	Y	Y	Y	–		Y
	MTU2	LED1 to LED14	MTU2 (12)	Y	(9)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	–	Y	(11)	Y	Y	Y	Y	Y	Y	–	Y	

Y: Yes, N: No, –: N/A

Notes:
1: When using LED2 and LED3, SW5-1, SW5-2, and SW5-3 on the R0K572670C000BR cannot be used.
2: PF9 to PF12 are multiplex pins. When setting SW5-5, and SW5-6 on the R0K572670C000BR, only one module can be used at these intersections.
3: When changing JP4 and JP5 settings on the R0K572670C000BR, only one module can be used at these intersections.
4: When changing JP1 and JP2 settings on the M3A-HS64G02, only one module can be used at these intersections.
5: When changing JP8 setting on the R0K572670C000BR, either CAN1 or IRQ1 switch can be used.
6: When changing JP3 setting on the M3A-HS64G02, either character LCD or SD card can be used.
7: When changing JP5 and JP9 settings on the M3A-HS64G02, either IEBus or CAN0 can be used.
8: PJ2 is a multiplex pin. When using the signal LCD_M_DISP, CAN1 cannot be used. When using CAN1, the signal LCD_M_DISP cannot be used.
9: PC5 to PC8 are multiplex pins. When setting SW5-4 on the R0K572670C000BR, either MTU2 or SDRAM can be used.
10: PF1 to PF8 are multiplex pins. When setting SW6-6 on the R0K572670C000BR, only one module can be used at these intersections.
11: The PG21 pin is connected to both the LCD and MTU2 modules, Therefore, any operation to either module will result in both modules performing the same operation.
12: LED1, LED2, LED7, LED8, LED11 to LED14 can be used with the R0K572670C000BR (Other LEDs cannot be used).

4.2.4 SH7267 Multiplex Pins Used on the M3A-HS64G02

Table 4.2.8 to Table 4.2.20 list SH7267 multiplex pin functions used on the M3A-HS64G02.

These multiplex pins are set as port input pins by default. Set the MD bit in the port control register to use the SH7267 peripheral functions (except I/O ports).

Table 4.2.8 SH7267 Multiplex Pin Functions (BSC)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
BSC	CS0#	PCCR0	PC0MD[1:0] = B'01	PC0/CS0#/SSIWS0 (1)
	CS3#	PCCR2	PC8MD[1:0] = B'01	PC8/CS3#/TIOC4D/IRQ7
	RD#	PCCR0	PC1MD[1:0] = B'01	PC1/RD#/SSISCK0 (1)
	WE0#/DQML	PCCR0	PC3MD[1:0] = B'01	PC3/WE0#/DQML/SSITxD0
	WE1#/DQMU/WE#	PCCR1	PC4MD0 = B'1	PC4/WE1#/DQMU/WE#
	RAS#	PCCR1	PC5MD[1:0] = B'01	PC5/RAS#/TIOC4A/IRQ4
	CAS#	PCCR1	PC6MD[1:0] = B'01	PC6/CAS#/TIOC4B/IRQ5
	CKE	PCCR1	PC7MD[1:0] = B'01	PC7/CKE/TIOC4C/IRQ6
	RD/WR#	PCCR0	PC2MD[1:0] = B'01	PC2/RD/WR#/SSIRxD0
	A21	PBCR5	PB21MD[2:0] = B'001	PB21/A21/SPDIF_OUT/TxD4
	D15	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H (1)
	D14	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G (1)
	D13	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F (1)
	D12	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E (1)
	D11	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D (1)
	D10	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C (1)
	D9	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B (1)
	D8	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A (1)
	D7	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H (1)
	D6	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G (1)
	D5	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F (1)
	D4	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E (1)
	D3	PDCR0	PD3MD[1:0] = B'01	PD3/D3/PWM1D (1)
	D2	PDCR0	PD2MD[1:0] = B'01	PD2/D2/PWM1C (1)
	D1	PDCR0	PD1MD[1:0] = B'01	PD1/D1/PWM1B (1)
	D0	PDCR0	PD0MD[1:0] = B'01	PD0/D0/PWM1A (1)

Note 1: For boot modes 1 to 3

Table 4.2.9 SH7267 Multiplex Pin Functions (INTC)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
INTC	IRQ3	PECR0	PE3MD[1:0] = B'11	PE3/SDA1/IRQ3
	IRQ2	PECR0	PE2MD[1:0] = B'11	PE2/SCL1/IRQ2
	IRQ1	PJCR1	PJ3MD[2:0] = B'011	PJ3/CRx1/CRx0&CRx1/IRQ1/AUDIO_XOUT/WDTOVF#

Table 4.2.10 SH7267 Multiplex Pin Functions (SCIF)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
SCIF	RxD0	PJCR0	PJ1MD[2:0] = B'100	PJ1/CRx0/IERxD/IRQ0/RxD0
	TxD0	PJCR0	PJ0MD[2:0] = B'100	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 4.2.11 SH7267 Multiplex Pin Functions (IIC3)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
IIC3	SDA1	PECR0	PE3MD[1:0] = B'01	PE3/SDA1/IRQ3
	SCL1	PECR0	PE2MD[1:0] = B'01	PE2/SCL1/IRQ2
	SDA0	PECR0	PE1MD[2:0] = B'001	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#/LCD_EXTCLK
	SCL0	PECR0	PE0MD[1:0] = B'01	PE0/SCL0/AUDIO_CLK/IRQ0

Table 4.2.12 SH7267 Multiplex Pin Functions (RCAN-TL1)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
RCAN-TL1	CRx1	PJCR1	PJ3MD[2:0] = B'001	PJ3/CRx1/CRx0&CRx1/IRQ1/AUDIO_XOUT/WDTOVF#
	CTx1	PJCR0	PJ2MD[2:0] = B'001	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/LCD_M_DISP
	CRx0	PJCR0	PJ1MD[2:0] = B'001	PJ1/CRx0/IERxD/IRQ0/RxD0
	CTx0	PJCR0	PJ0MD[2:0] = B'001	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 4.2.13 SH7267 Multiplex Pin Functions (IEB)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
IEB	IERxD	PJCR0	PJ1MD[2:0] = B'010	PJ1/CRx0/IERxD/IRQ0/RxD0
	IETxD	PJCR0	PJ0MD[2:0] = B'010	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 4.2.14 SH7267 Multiplex Pin Functions (FLCTL)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
FLCTL	NAF7	PDCR3	PD15MD[1:0] = B'01	PD15/D15/NAF7/PWM2H
	NAF6	PDCR3	PD14MD[1:0] = B'01	PD14/D14/NAF6/PWM2G
	NAF5	PDCR3	PD13MD[1:0] = B'01	PD13/D13/NAF5/PWM2F
	NAF4	PDCR3	PD12MD[1:0] = B'01	PD12/D12/NAF4/PWM2E
	NAF3	PDCR2	PD11MD[1:0] = B'01	PD11/D11/NAF3/PWM2D
	NAF2	PDCR2	PD10MD[1:0] = B'01	PD10/D10/NAF2/PWM2C
	NAF1	PDCR2	PD9MD[1:0] = B'01	PD9/D9/NAF1/PWM2B
	NAF0	PDCR2	PD8MD[1:0] = B'01	PD8/D8/NAF0/PWM2A
	FWE#	PDCR1	PD7MD[1:0] = B'01	PD7/D7/FWE#/PWM1H
	FALE	PDCR1	PD6MD[1:0] = B'01	PD6/D6/FALE/PWM1G
	FCLE	PDCR1	PD5MD[1:0] = B'01	PD5/D5/FCLE/PWM1F
	FRE#	PDCR1	PD4MD[1:0] = B'01	PD4/D4/FRE#/PWM1E
	FCE#	PFCR2	PF10MD[2:0] = B'101	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	FRB	PFCR2	PF9MD[2:0] = B'101	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 4.2.15 SH7267 Multiplex Pin Functions (SDHI)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
SDHI	SD_CD	PFCR2	PF8MD[2:0] = B'110	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD
	SD_WP	PFCR1	PF7MD[2:0] = B'110	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/SD_WP
	SD_D1	PFCR1	PF6MD[2:0] = B'110	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/TCLKB/SD_D1
	SD_D0	PFCR1	PF5MD[2:0] = B'110	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/TCLKC/SD_D0/AUDATA3
	SD_CLK	PFCR1	PF4MD[2:0] = B'110	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/TxD3/SD_CLK/AUDATA2
	SD_CMD	PFCR0	PF3MD[2:0] = B'110	PF3/ICIORD#/SSISCK1/DV_DATA3/RxD3/SD_CMD/AUDATA1
	SD_D3	PFCR0	PF2MD[2:0] = B'110	PF2/BACK#/DV_DATA2/TxD2/DACK0/SD_D3/AUDATA0
	SD_D2	PFCR0	PF1MD[2:0] = B'110	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/SD_D2/AUDSYNC#

Table 4.2.16 SH7267 Multiplex Pin Functions (MTU2)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
MTU2	TIOC4D	PCCR2	PC8MD[1:0] = B'10	PC8/CS3#/TIOC4D/IRQ7
	TIOC4C	PCCR1	PC7MD[1:0] = B'10	PC7/CKE/TIOC4C/IRQ6
	TIOC4B	PCCR1	PC6MD[1:0] = B'10	PC6/CAS#/TIOC4B/IRQ5
	TIOC4A	PCCR1	PC5MD[1:0] = B'10	PC5/RAS#/TIOC4A/IRQ4
	TIOC0B	PGCR5	PG22MD[1:0] = B'10	PG22/SSL10/TIOC0B
	TIOC0A	PGCR5	PG21MD[1:0] = B'10	PG21/RSPCK1/TIOC0A

Table 4.2.17 SH7267 Multiplex Pin Functions (SSIF)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
SSIF	SSIDATA3	PFCR2	PF11MD[2:0] = B'010	PF11/A25/SSIDATA3/MOSI0/TIOC3C/SPDIF_IN
	SSIWS3	PFCR2	PF10MD[2:0] = B'010	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
	SSISCK3	PFCR2	PF9MD[2:0] = B'010	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB

Table 4.2.18 SH7267 Multiplex Pin Functions (ADC)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
ADC	AN3	PHCR0	PH3MD0 = B'1	PH3/AN3
	AN2	PHCR0	PH2MD0 = B'1	PH2/AN2
	AN1	PHCR0	PH1MD0 = B'1	PH1/AN1
	AN0	PHCR0	PH0MD0 = B'1	PH0/AN0

Table 4.2.19 SH7267 Multiplex Pin Functions (VDC3)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
VDC3	DV_CLK	PFCR2	PF8MD[2:0] = B'011	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD
	DV_DATA7	PFCR1	PF7MD[2:0] = B'011	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/SD_WP
	DV_DATA6	PFCR1	PF6MD[2:0] = B'011	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/TCLKB/SD_D1
	DV_DATA5	PFCR1	PF5MD[2:0] = B'011	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/TCLKC/SD_D0/ AUDATA3
	DV_DATA4	PFCR1	PF4MD[2:0] = B'011	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/TxD3/SD_CLK/ AUDATA2
	DV_DATA3	PFCR0	PF3MD[2:0] = B'011	PF3/ICIORD#/SSISCK1/DV_DATA3/RxD3/SD_CMD/ AUDATA1
	DV_DATA2	PFCR0	PF2MD[2:0] = B'011	PF2/BACK#/DV_DATA2/TxD2/DACK0/SD_D3/AUDATA0
	DV_DATA1	PFCR0	PF1MD[2:0] = B'011	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/SD_D2/AUDSYNC#
	DV_DATA0	PFCR0	PF0MD[2:0] = B'011	PF0/WAIT#/DV_DATA0/SCK2/TEND0/AUDCK
	DV_HSYNC	PECR1	PE5MD[1:0] = B'11	PE5/SDA2/DV_HSYNC
	DV_VSYNC	PECR1	PE4MD[1:0] = B'11	PE4/SCL2/DV_VSYNC
	LCD_EXTCLK	PGCR5	PG20MD[2:0] = B'001	PG20/LCD_EXTCLK/SCK1
	LCD_CLK	PGCR4	PG19MD[2:0] = B'001	PG19/LCD_CLK/TIOC2B/TxD3/CTS1
	LCD_DE	PGCR4	PG18MD[2:0] = B'001	PG18/LCD_DE/TIOC2A/RxD3/RTS1
	LCD_HSYNC	PGCR4	PG17MD[2:0] = B'001	PG17/LCD_HSYNC/TIOC1B/TxD1
	LCD_VSYNC	PGCR4	PG16MD[2:0] = B'001	PG16/LCD_VSYNC/TIOC1A/RxD1
	LCD_DATA15	PGCR3	PG15MD[2:0] = B'001	PG15/LCD_DATA15/TIOC0D/TxD7
	LCD_DATA14	PGCR3	PG14MD[2:0] = B'001	PG14/LCD_DATA14/TIOC0C/RxD7
	LCD_DATA13	PGCR3	PG13MD[2:0] = B'001	PG13/LCD_DATA13/TIOC0B/TxD6
	LCD_DATA12	PGCR3	PG12MD[2:0] = B'001	PG12/LCD_DATA12/TIOC0A/RxD6
	LCD_DATA11	PGCR2	PG11MD[2:0] = B'001	PG11/LCD_DATA11/SSIWS0/IRQ3/TxD5/SIOFTxD
	LCD_DATA10	PGCR2	PG10MD[2:0] = B'001	PG10/LCD_DATA10/SSISCK0/IRQ2/RxD5/SIOFRxD
	LCD_DATA9	PGCR2	PG9MD[2:0] = B'001	PG9/LCD_DATA9/SSIRxD0/TxD4/SIOFSYNC
	LCD_DATA8	PGCR2	PG8MD[2:0] = B'001	PG8/LCD_DATA8/SSITxD0/RxD4/SIOFSCK
	LCD_DATA7	PGCR1	PG7MD[2:0] = B'001	PG7/LCD_DATA7/SD_CD/PINT7/IRQ7
	LCD_DATA6	PGCR1	PG6MD[2:0] = B'001	PG6/LCD_DATA6/SD_WP/PINT6/IRQ6
	LCD_DATA5	PGCR1	PG5MD[2:0] = B'001	PG5/LCD_DATA5/SD_D1/PINT5/IRQ5
	LCD_DATA4	PGCR1	PG4MD[2:0] = B'001	PG4/LCD_DATA4/SD_D0/PINT4/IRQ4
	LCD_DATA3	PGCR0	PG3MD[1:0] = B'01	PG3/LCD_DATA3/SD_CLK/PINT3
	LCD_DATA2	PGCR0	PG2MD[1:0] = B'01	PG2/LCD_DATA2/SD_CMD/PINT2
	LCD_DATA1	PGCR0	PG1MD[1:0] = B'01	PG1/LCD_DATA1/SD_D3/PINT1
	LCD_DATA0	PGCR0	PG0MD[1:0] = B'01	PG0/LCD_DATA0/SD_D2/PINT0
	LCD_M_DISP	PJCR0	PJ2MD[2:0] = B'101	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/LCD_M_DISP

Table 4.2.20 SH7267 Multiplex Pin Functions (PWM)

Peripheral Function	Pin Name	SH7267 Port Control Register		SH7267 Multiplex Pin Name
		Register Name	MD bit Setting	
PORT	PG24	PGCR6	PG24MD[1:0] = B'00	PG24/MISO1/TIOC0D
	PG23	PGCR5	PG23MD[1:0] = B'00	PG23/MOSI1/TIOC0C
	PF12	PFCR3	PF12MD[2:0] = B'000	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
	PB22	PBCR5	PB22MD[2:0] = B'000	PB22/A22/CS4#/RxD4

4.3 LCD Module Interface

4.3.1 LCD Module Interface

The M3A-HS64G02 includes two flexible connectors and one MIL-spec connector for connecting LCD modules.

The SH7267 on-chip VDC3 controls the LCD modules.

The following figure shows the LCD module interface block diagram.

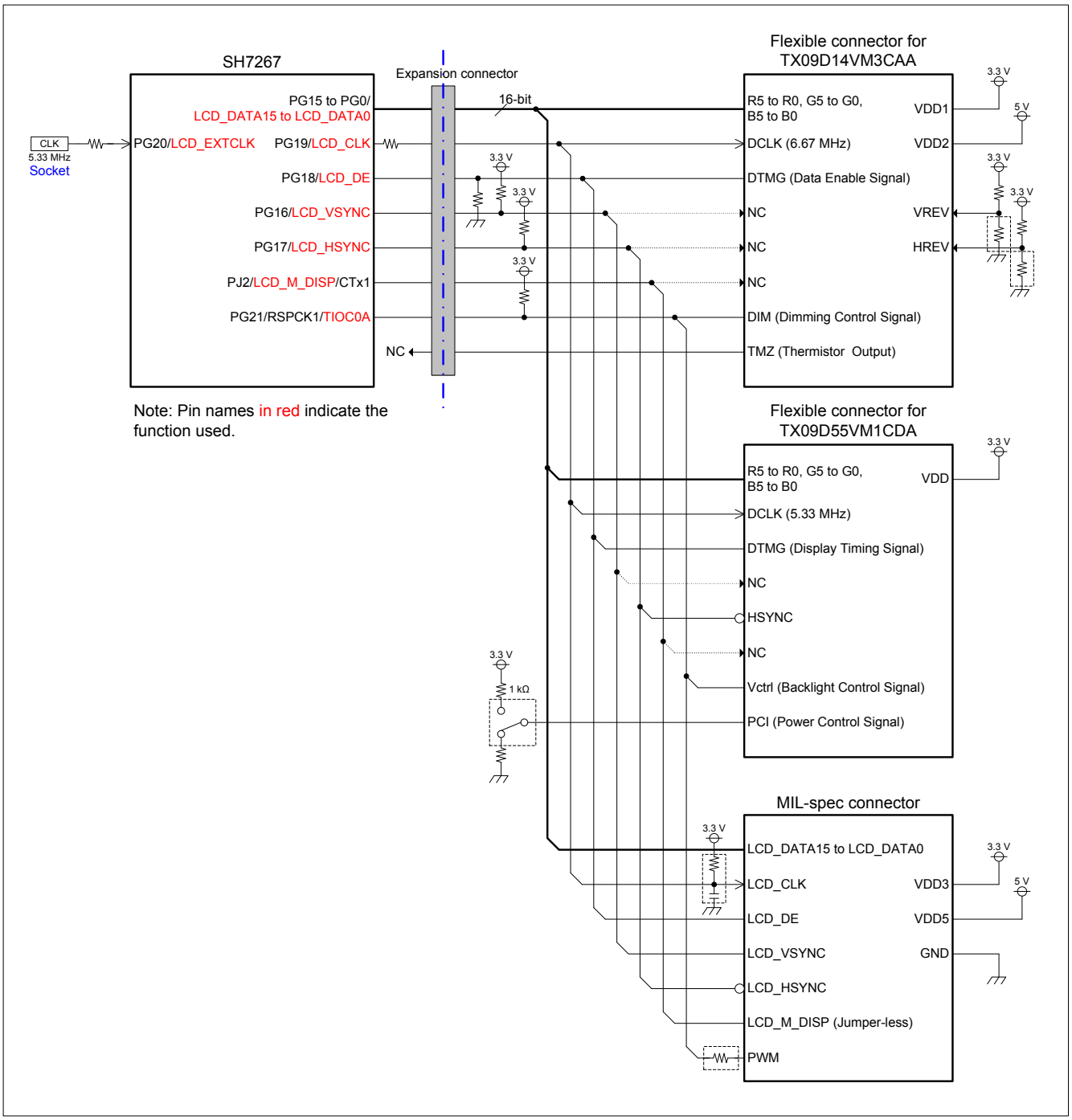


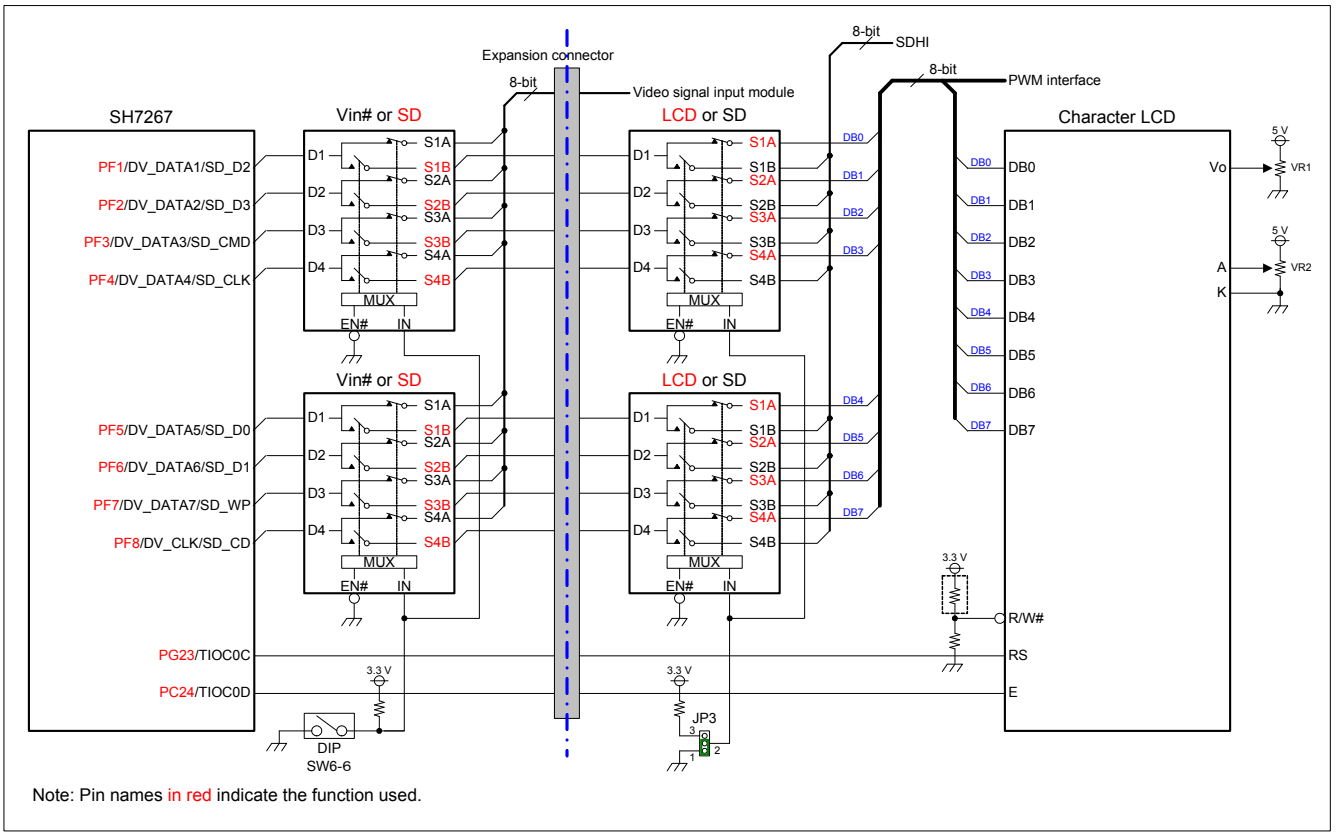
Figure 4.3.1 LCD Module Interface Block Diagram

4.3.2 Character LCD Module with LED Backlight

The M3A-HS64G02 includes a connector for 16 x 2 semi-transmissive character LCD module (SD1602H, SUNLIKE). The SH7267 general-purpose port output controls the character LCD module. The M3A-HS64G02 is intended only for writing from the SH7267 to the character LCD modules. Therefore, the character LCD module R/W signal is fixed low.

The M3A-HS64G02 also includes a variable resister (VR1) for the LCD driver voltage adjustment to control the LCD contrast and a variable resister (VR2) for LCD backlight adjustment.

SH7267 PF1 to PF8 pins are also used as the video display controller 3 (VDC3) and SDHI pins. When using the character LCD module, VDC3 and SDHI cannot be used. The figure below shows the character LCD module block diagram Table 4.3.1 the system-setting DIP switches setting (SW6-6 on the R0K572670C000BR). Table 4.3.2 lists the jumper setting (JP3 on the M3A-HS64G02).



Note: Pin names in red indicate the function used.

Figure 4.3.2 Character LCD Module Block Diagram

Table 4.3.1 DIP Switches Setting (SW6 on the R0K572670C000BR)

Number	Function	
	OFF (High)	ON (Low)
SW6-6	Connected to the SDHI/character LCD interface (default)	Connected to the VDC3

Table 4.3.2 Jumper Setting (JP3 on the M3A-HS64G02)

Number	1-2 (Low)	2-3 (High)
JP3	Connected to the character LCD interface (default)	Connected to the SDHI

4.4 Audio Module

The M3A-HS64G02 includes a 96 kHz 24-bit D/A converter with DIT (AK4353, Asahi Kasei EMD Corporation).

➢ AK4353, D/A Converter

SH7267 IIC3, SSIF, and I/O ports control AK4353.

- SH7267 IIC3 (Channel 1): Accesses the AK4353 registers to initialize AK4353, format data, and configure the attenuator
- SH7267 SSIF (Channel 3): Outputs the audio data
- SH7267 I/O ports (PF12): Powers down AK4353 at low, powers up AK4353 at high

Note: The R0K572670C000BR allows for selecting 12.2880 MHz or 11.2896 MHz as the AK4353 system clock.

The figure below shows the D/A converter block diagram. Table 4.4.1 lists the system-setting DIP switches setting (SW5 on the R0K572670C000BR). Table 4.4.2 lists the jumper setting (JP9 on the R0K572670C000BR). Table 4.4.3 lists the jumpers setting (JP1 to JP3 on the M3A-HS64G02).

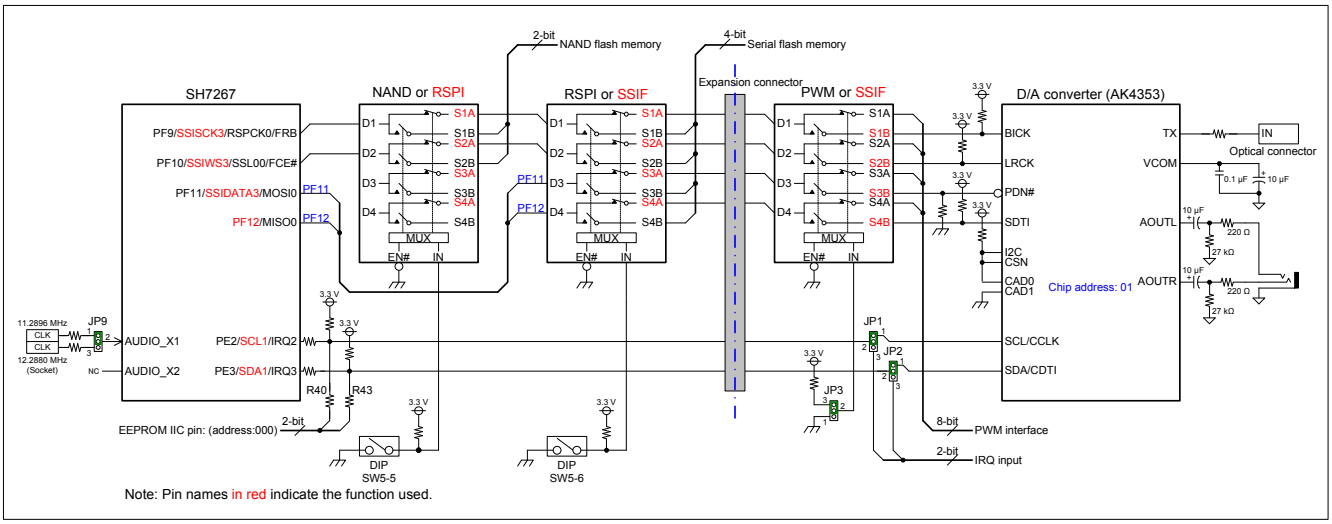


Figure 4.4.1 D/A Converter Block Diagram

Table 4.4.1 DIP Switches Setting (SW5-5, and SW5-6 on the R0K572670C000BR)

Number	Function	
	OFF (High)	ON (Low)
SW5-5	Connected to the NAND flash memory	Connected to the device which is connected to RSPI/ SSIF (default)
SW5-6	Connected to the serial flash memory	Connected to the audio module (default)

Table 4.4.2 Jumper Setting (JP9 on the R0K572670C000BR)

Number	1-2	2-3
JP9	Provides 11.2896 MHz with the AUDIO_X1 pin (default)	Provides 12.2880 MHz with the AUDIO_X1 pin

Table 4.4.3 Jumpers Setting (JP1 to JP3 on the M3A-HS64G02)

Number	1-2	2-3
JP1	IIC3 mode (Sets the PE2 as the SCL1 output pin)	IRQ mode (Sets the PE2 as the IRQ2 input pin, default)
JP2	IIC3 mode (Sets the PE3 as the SDA1 I/O pin)	IRQ mode (Sets the PE3 as the IRQ3 input pin, default)
JP3	Connected to the PWM interface (Low, default) Note: This setting cannot be used with the R0K572670C000BR.	Connected to the SSIF (High)

4.5 Video Signal Input Module

The M3A-HS64G02 includes a video decoder IC (AK8851, Asahi Kasei EMD Corporation). The M3A-HS64G02 also includes an RCA connector and an S-Video connector for NTSC and PAL video signal input as video signal input to input the digital signals to the SH7267 VDC3 module via the video decoder IC. The VDC3 pin is also used as the SDHI pins. The SH7267 on-chip IIC3 controls the video decoder.

The following figure shows the video signal input module block diagram. Table 4.5.1 lists the system-setting DIP switches setting (SW6 on the R0K572670C000BR).

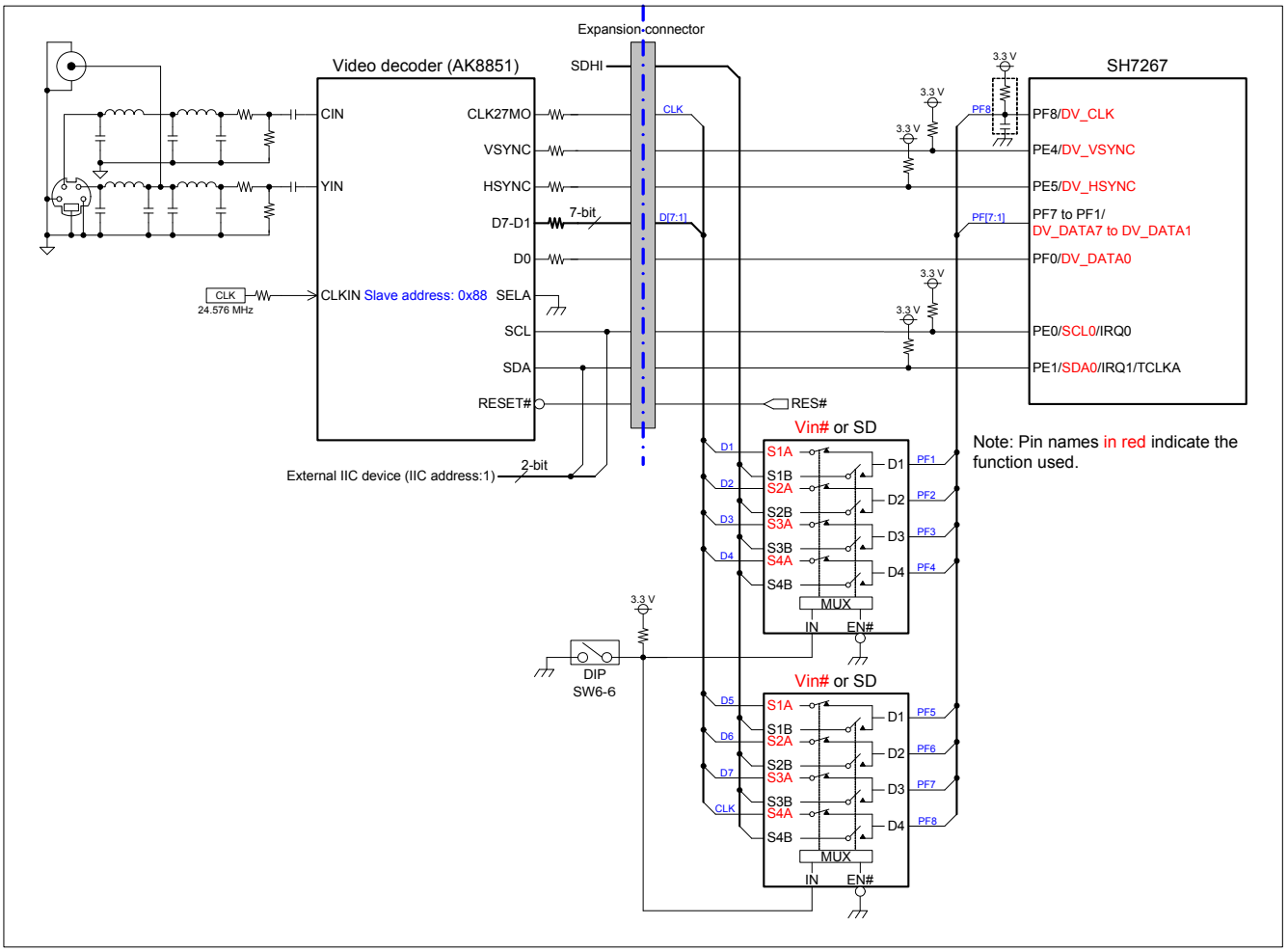


Figure 4.5.1 Video Signal Input Module Block Diagram

Table 4.5.1 DIP Switches Setting (SW6-6 on the R0K572670C000BR)

Number	Function	
	OFF (High)	ON (Low)
SW6-6	Connected to the SDHI/character LCD interface (default)	Connected to the VDC3

4.6 SD Card Interface

The M3A-HS64G02 includes an SD card slot to interface the SH7267 built-in SD Host Interface (SDHI) with the SD card slot. The SDHI pin is also used as the Video Display Controller 3 (VDC3) and the character LCD module pins. When using the SDHI, the video signal input module and the character LCD module cannot be used. The figure below shows the SD card interface block diagram. Table 4.6.1 lists the system-setting DIP switches setting (SW6-6 on the R0K572670C000BR). Table 4.6.2 lists the jumper setting (JP3 on the M3A-HS64G02).

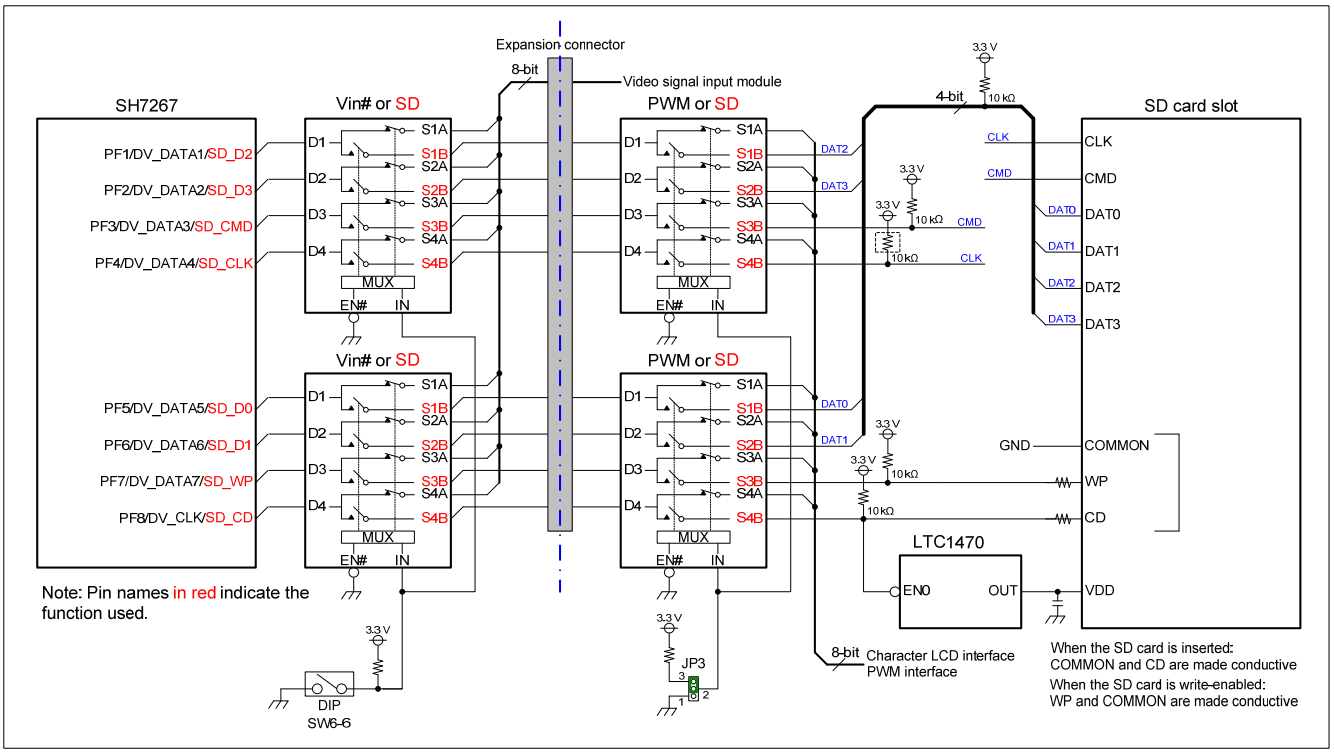


Figure 4.6.1 SD Card Interface Block Diagram

Table 4.6.1 DIP Switches Setting (SW6-6 on the R0K572670C000BR)

Number	Function	
	OFF (High)	ON (Low)
SW6-6	Connected to the SDHI/character LCD interface (default)	VDC3

Table 4.6.2 Jumper Setting (JP3 on the M3A-HS64G02)

Number	1-2 (Low)	2-3 (High)
JP3	Connected to the PWM interface (default) Note: This setting cannot be used with the R0K572670C000BR.	Connected to the SDHI

4.7 UART Interface

The SH7267 has a Serial Communication Interface with FIFO (SCIF) and the M3A-HS64G02 includes a UART connector. This module cannot be used with the R0K572670C000BR.

4.8 CAN Interface

The SH7267 includes an RCAN-TL1 (Renesas CAN Time Trigger Level 1), the Controller Area Network. RCAN-TL1 channels 0 and 1 are connected to the CAN connector (3-pin, 2.5 mm pitch) on the M3A-HS64G02 via the voltage level shifter and the CAN driver IC.

The RCAN-TL1 channel 0 pin is also used as the SCIF channel 0 pin, and the IEBus™ controller (IEB) pin.

The figure below shows the CAN interface block diagram. Table 4.8.1 lists the jumpers setting (JP4, JP5, and JP8 on the R0K572670C000BR). Table 4.8.2 and Table 4.8.3 list jumpers setting (JP4, JP5, JP8, and JP9 on the M3A-HS64G02).

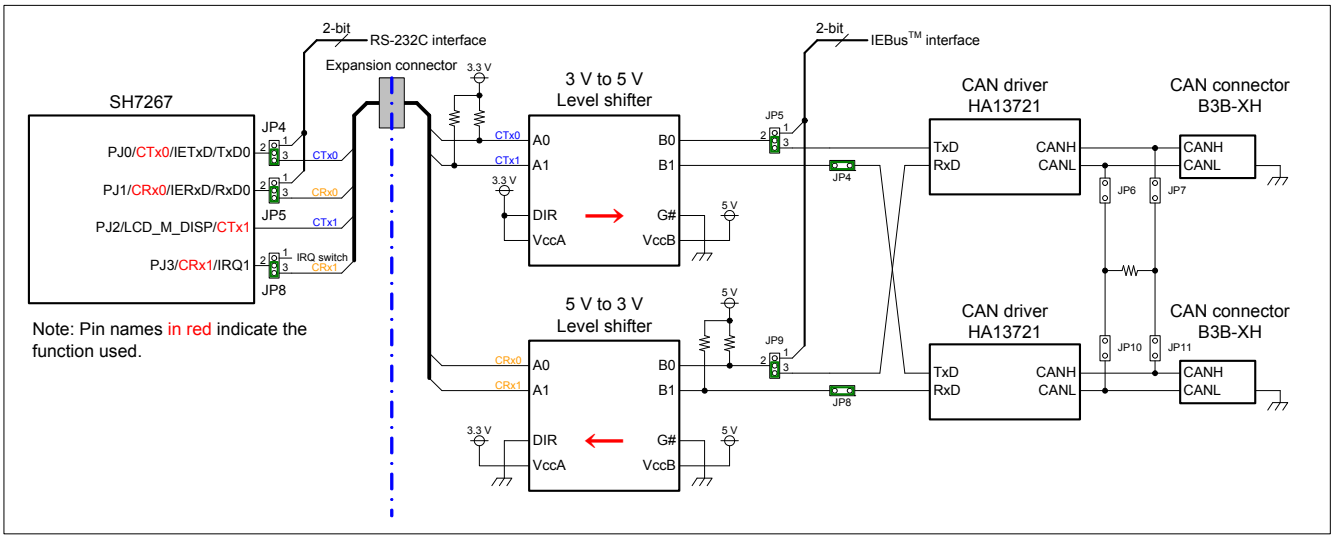


Figure 4.8.1 CAN Interface Block Diagram

Table 4.8.1 Jumpers Setting (JP4, JP5, and JP8 on the R0K572670C000BR)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) pin - default	Selects the CTx0 (RCAN-TL1) / IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) pin - default	Selects the CRx0 (RCAN-TL1) / IERxD (IEB) pins
JP8	Selects the IRQ1 switch - default	Selects the CRx1 (RCAN-TL1) pin

Table 4.8.2 Jumpers Setting (JP5, and JP9 on the M3A-HS64G02)

Number	1-2	2-3
JP5	Selects the IETxD (IEB) pin	Selects the CTx0 (RCAN-TL1) pin - default
JP9	Selects the IERxD (IEB) pin	Selects the CRx0 (RCAN-TL1) pin - default

Table 4.8.3 Jumpers Setting (JP4, and JP8 on the M3A-HS64G02)

Number	1-2	None (Open)
JP4	Normal mode (Connects the CTx1 pin) - default	Debug mode (Leaves the CTx1 pin disconnected)
JP8	Normal mode (Connects the CRx1 pin) - default	Debug mode (Leaves the CRx1 pin disconnected)

4.9 IEBus™ Interface

The SH7267 includes an IEBus™ controller (IEB). IEBus™ (Inter Equipment Bus™) is the bus for digital data transfer system on a small scale. The SH7267 IEB pin is connected to the IEBus connector (4-pin, 2.5 mm) via the voltage level shifter and the IEBus™ driver IC on the M3A-HS64G02.

The IEB pin is also used as the SCIF channel 0 pin and the RCAN-TL1 channel 0 pin.

The figure below shows the IEBus™ interface block diagram. Table 4.9.1 lists the jumpers setting (JP4, and JP5 on the R0K572670C000BR). Table 4.9.2 lists the jumpers setting (JP5, and JP9 on the M3A-HS64G02).

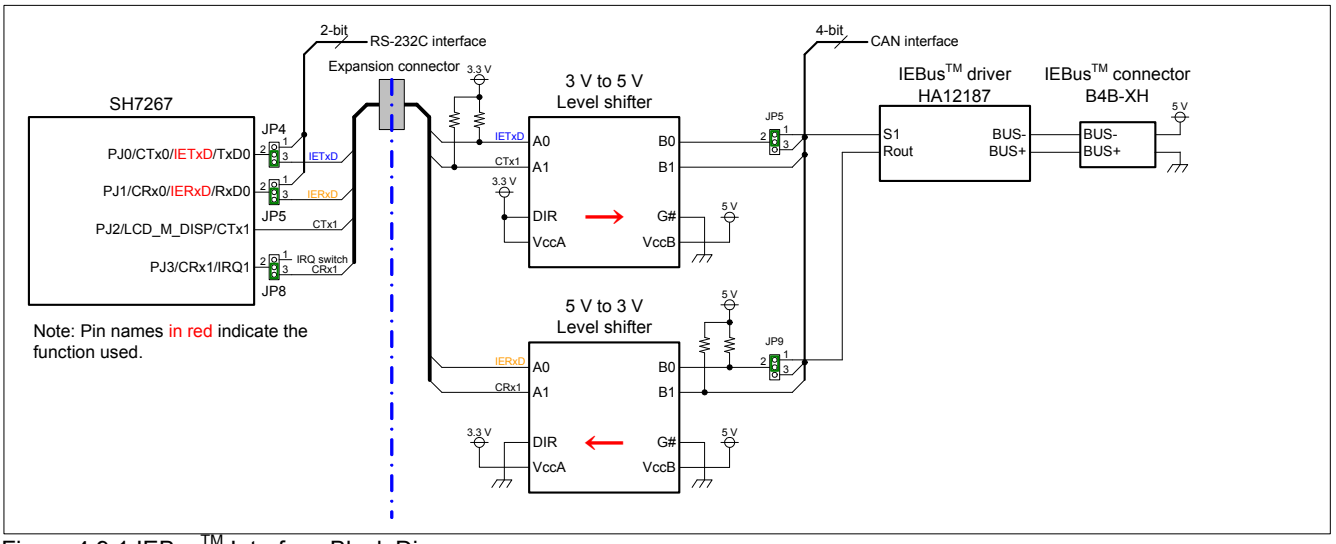


Figure 4.9.1 IEBus™ Interface Block Diagram

Table 4.9.1 Jumpers Setting (JP4, and JP5 on the R0K572670C000BR)

Number	1-2	2-3
JP4	Selects the TxD0 (SCIF) pin - default	Selects the CTx0 (RCAN-TL1) / IETxD (IEB) pins
JP5	Selects the RxD0 (SCIF) pin - default	Selects the CRx0 (RCAN-TL1) / IERxD (IEB) pins

Table 4.9.2 Jumpers Setting (JP5, and JP9 on the M3A-HS64G02)

Number	1-2	2-3
JP5	Selects the IETxD (IEB) pin	Selects the CTx0 (RCAN-TL1) pin - default
JP9	Selects the IERxD (IEB) pin	Selects the CRx0 (RCAN-TL1) pin - default

4.10 PWM Interface

The SH7267 includes two channels of on-chip Motor Control Pulse Width Modulator (PWM) timer with a maximum of eight pulse outputs per channel. This module cannot be used with the R0K572670C000BR.

4.11 MTU2 Interface

The SH7267 includes a Multi Function Timer Pulse Unit 2 (MTU2) consists of five channels of 16-bit timer counter. LEDs are connected to MTU2 pins to control LED brightness on the M3A-HS64G02. MTU2 pins are also used as SDRAM control pins and RSPI (Renesas Peripheral Interface) channel 0 pin. The figure below shows the MTU2 interface block diagram. Table 4.11.1 lists the DIP switches setting (SW5 on the R0K572670C000BR).

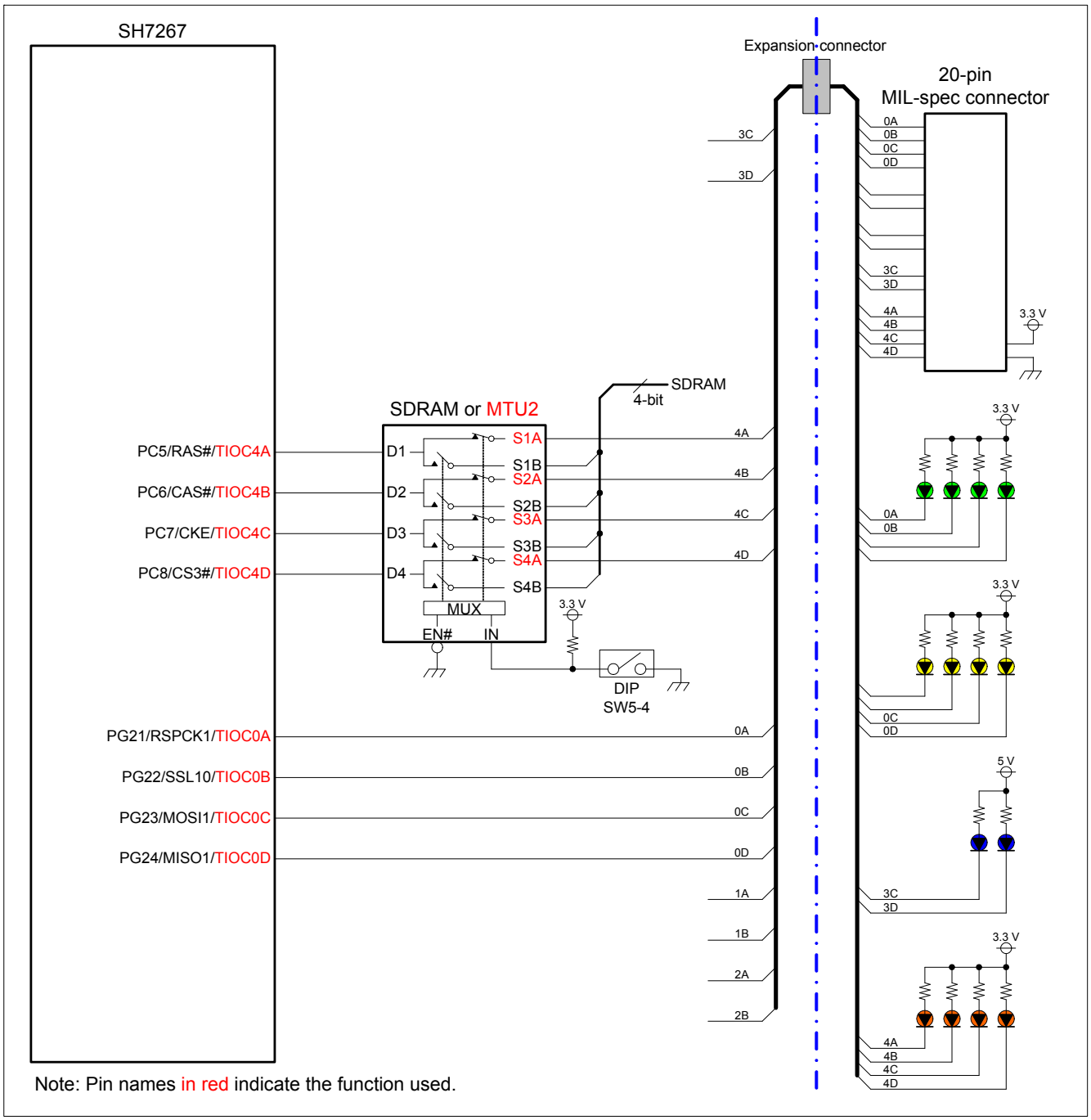


Figure 4.11.1 MTU2 Interface Block Diagram

Table 4.11.1 DIP Switches Setting (SW5 on the R0K572670C000BR)

Number	Function	
	OFF (High)	ON (Low)
SW5-4	Connected to the SDRAM (default)	Connected to the MTU2 interface

4.12 I/O Ports

SH7267 I/O ports are connected to switches and LEDs on the M3A-HS64G02.

To use ports PH0 to PH3 as key input switches (4 switches x 4 inputs) via an A/D converter (ADC), sets the ports as analog input pins (AN0 to AN3). Port A can be used as a user interface by setting PB22 pin to high output. The figure below shows the I/O ports block diagram. Table 4.12.1 lists the jumper setting (JP6 on the R0K572670C000BR). Table 4.12.2 lists the port A function switching.

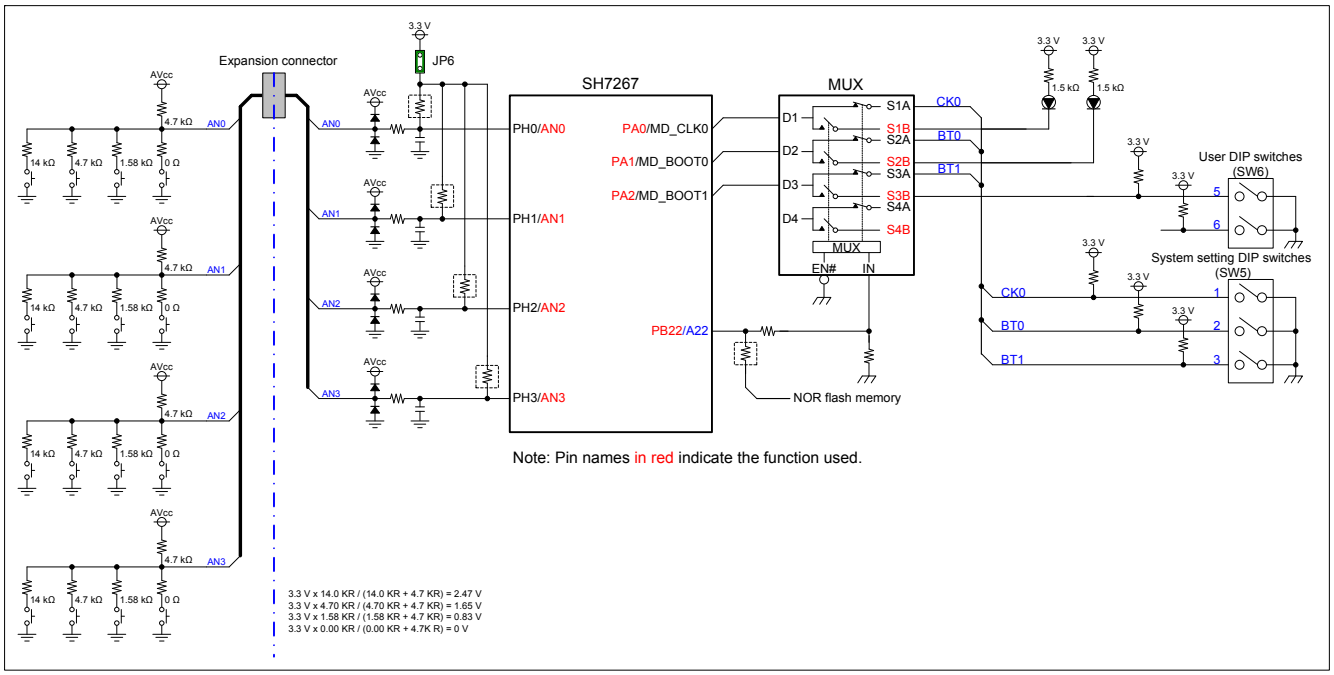


Figure 4.12.1 I/O Ports Block Diagram

Table 4.12.1 Jumper Setting (JP6 on the R0K572670C000BR)

Number	1-2	None (Open)
JP6	Uses PH [3:0] as an input port (default) (1)	Uses PH [3:0] as an analog input pin

Note 1: When using the PH [3:0] as the input port, mount R11 to R14.

Table 4.12.2 Port A Function Switching

Number	High output	Low output
PB22	Uses Port A as a user interface	Mode sampling (At power-up)

4.13 Interrupt Switches

The M3A-HS64G02 includes two push-button switches (IRQ2 switch and IRQ3 switch) for the IRQ2, and IRQ3 interrupt signals input from the SH7267.

Set jumpers JP1, and JP2 on the M3A-HS64G02 to use these switches. Also, remove resistors R40 and R43 to avoid failure on EEPROM installed on the R0K572670C000BR.

The figure below shows the interrupt switch block diagram. Table 4.13.1 lists the jumpers setting (JP1, and JP2 on the M3A-HS64G02).

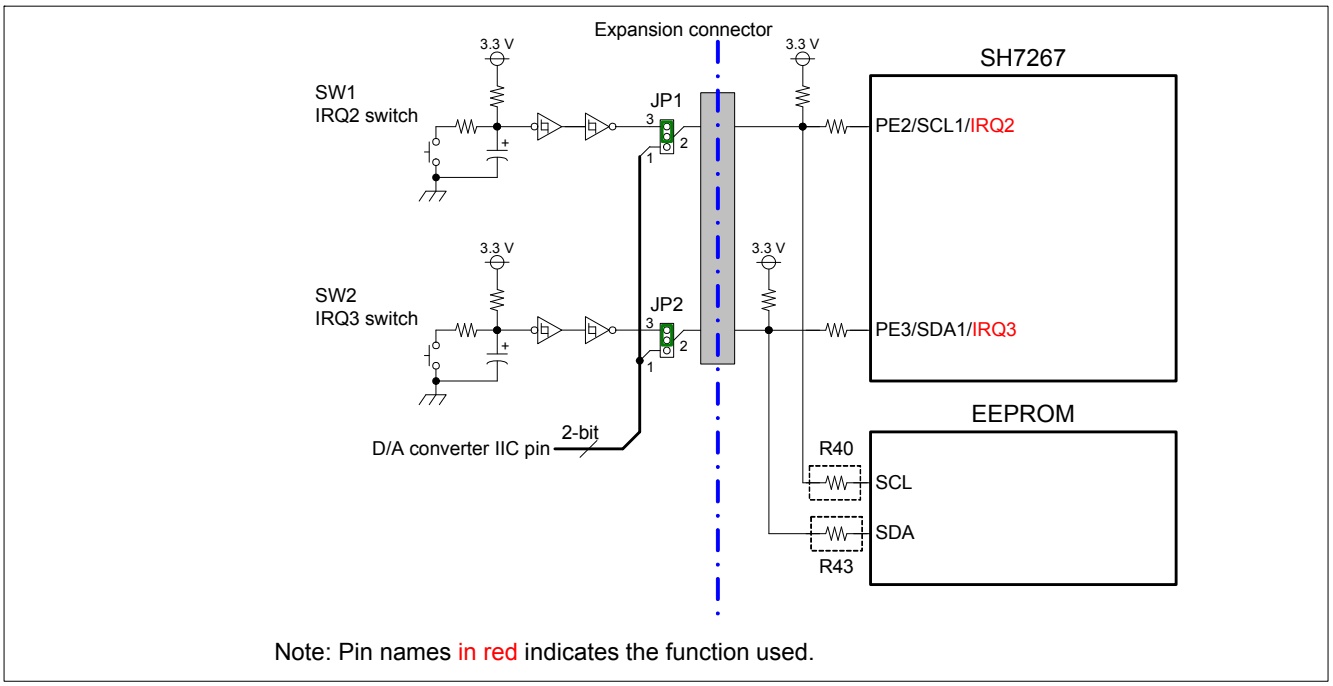


Figure 4.13.1 Interrupt Switch Block Diagram

Table 4.13.1 Jumpers Setting (JP1, and JP2 on the M3A-HS64G02)

Number	1-2	2-3
JP1	IIC3 mode (Sets the PE2 as the SCL1 output pin)	IRQ mode (Sets the PE2 as the IRQ2 input pin, default)
JP2	IIC3 mode (Sets the PE3 as the SDA1 I/O pins)	IRQ mode (Sets the PE3 as the IRQ3 input pin, default)

4.14 Clock Modules

Provide following clocks with the SH7267 on the R0K572670C000BR.

- SH7267 input clock: 12 MHz
- SH7267 RTC clock: 32.768 kHz
- SH7267 audio clock: 12.2880 MHz, and 11.2896 MHz (default)
- SH7267 USB clock: 48.00 MHz
- SH7267 LCD clock : 5.33 MHz

➢ How to select the system clock frequency of AK4353 (D/A converter)

SH7267 audio clock provides either 12.2880 MHz or 11.2896 MHz of the clock frequency with AK4353 by switching jumpers. The figure below shows the clock module block diagram of the R0K572670C000BR and M3A-HS64G02. Table 4.14.1 lists the audio clock switching (JP9 on the R0K572670C000BR).

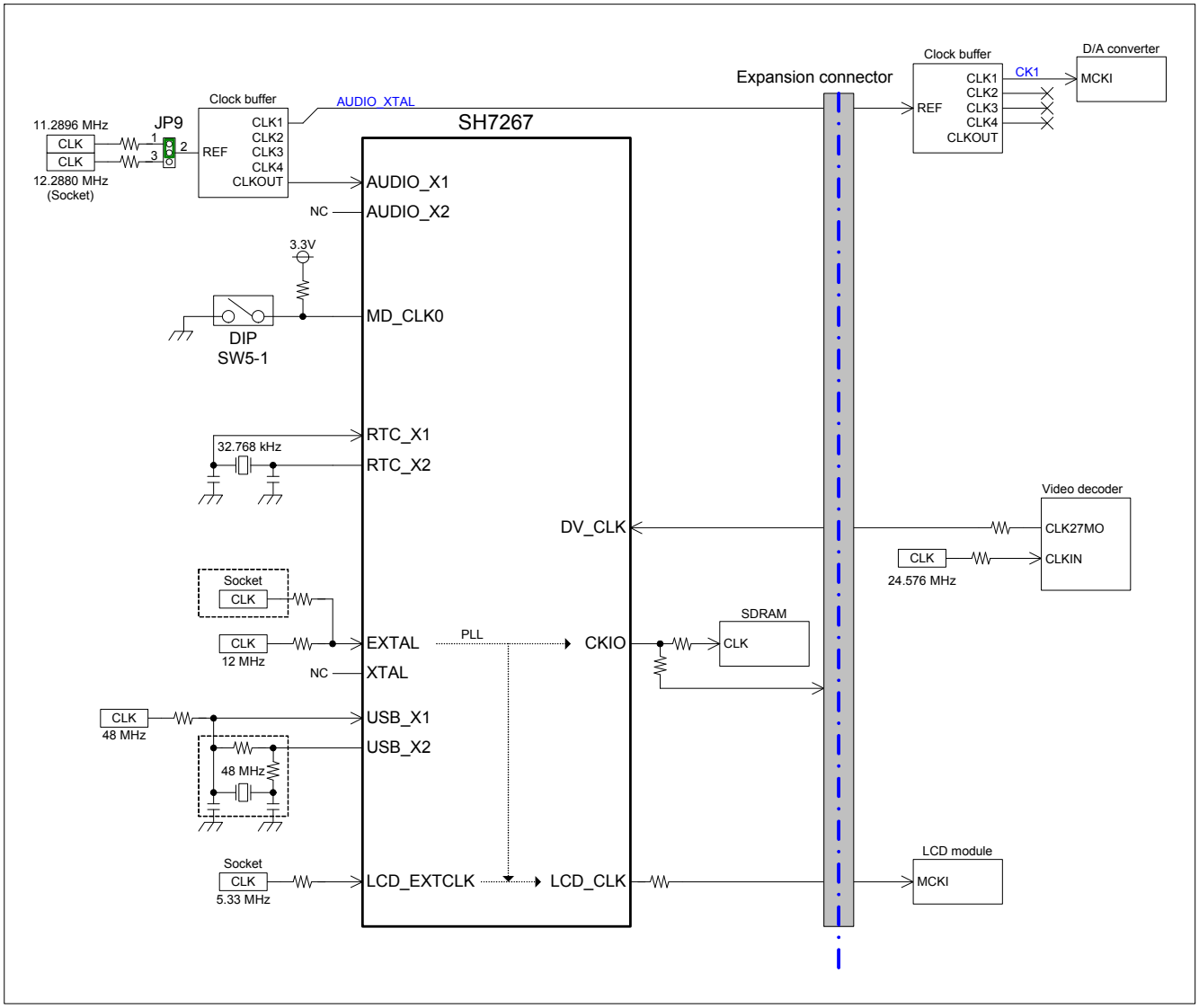


Figure 4.14.1 Clock Module Block Diagram

Table 4.14.1 Audio Clock Switching (JP9 on the R0K572670C000BR)

Number	1-2	2-3
JP9	Provides 11.2896 MHz with the AUDIO_X1 pin (default)	Provides 12.2880 MHz with the AUDIO_X1 pin

4.15 Reset Module

A reset IC controls reset signals connected to the SH7267, flash memory and peripheral I/Os on the R0K572670C000BR and M3A-HS64G02.

There are two system reset options: power-on reset, and reset by switch. The following figure shows the reset module block diagram.

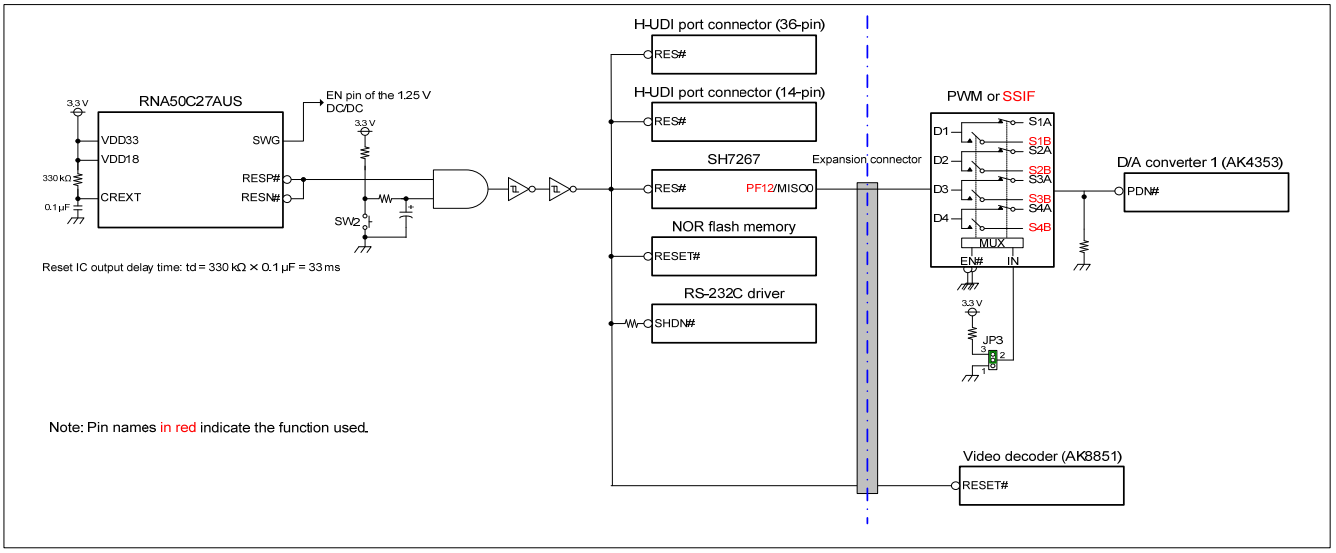


Figure 4.15.1 Reset Module Block Diagram

4.16 Power Supply Module

The M3A-HS64G02 is supplied 12 V power and the voltage regulator on the M3A-HS64G02 generates 8 V, and 5 V voltage.
5 V voltage is supplied to the R0K572670C000BR, and the voltage regulator on the R0K572670C000BR generates digital voltage (3.3 V, 3VCC) and analog voltage (3.3 V, AVcc).
The figure below shows the power supply module block diagram.

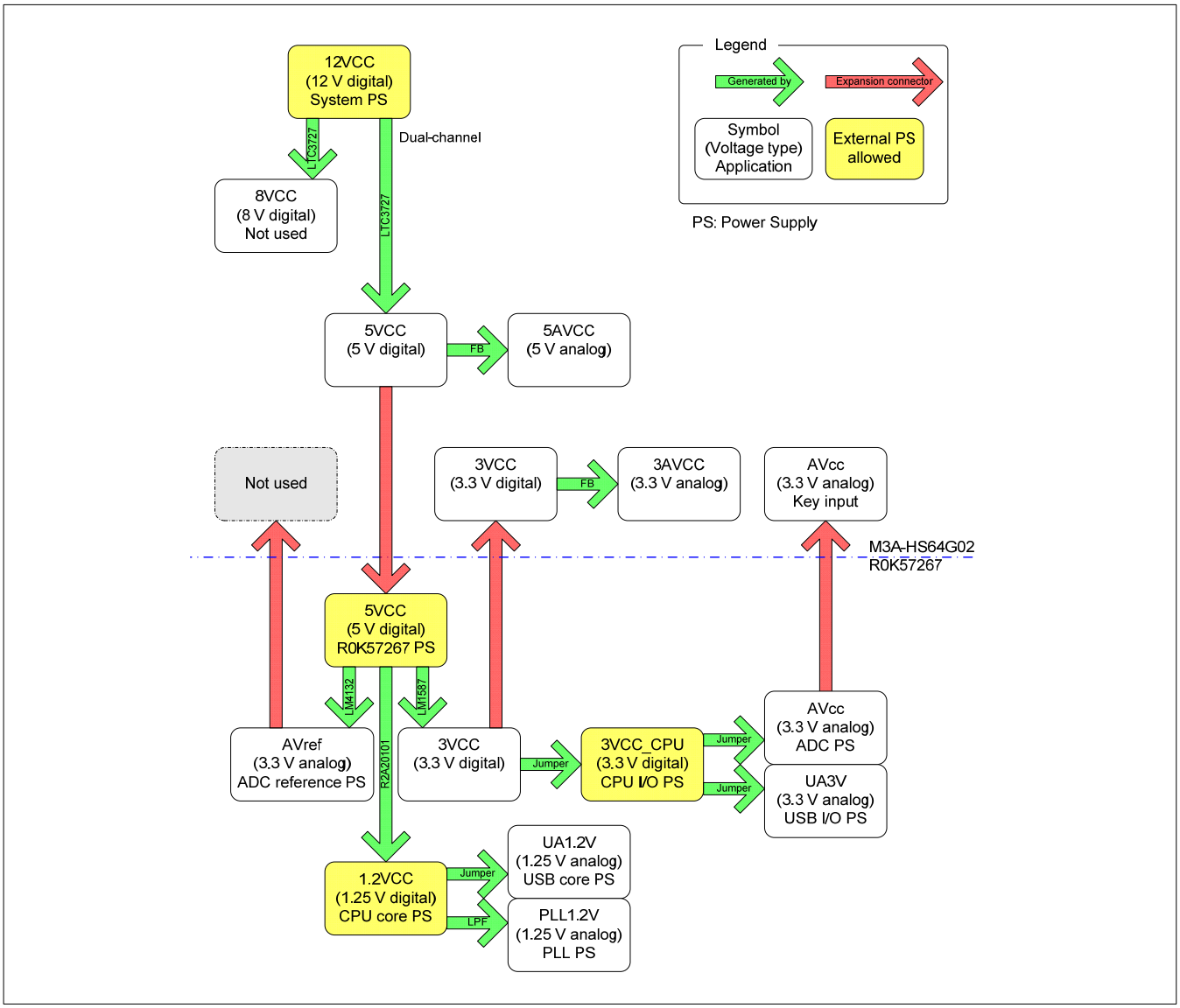


Figure 4.16.1 Power Supply Module Block Diagram

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Chapter 5
R0K572670C000BR Operating Specifications

5.1 R0K572670C000BR Connectors

Figure 5.1.1 and Figure 5.1.2 show the connector assignments for the R0K572670C000BR.

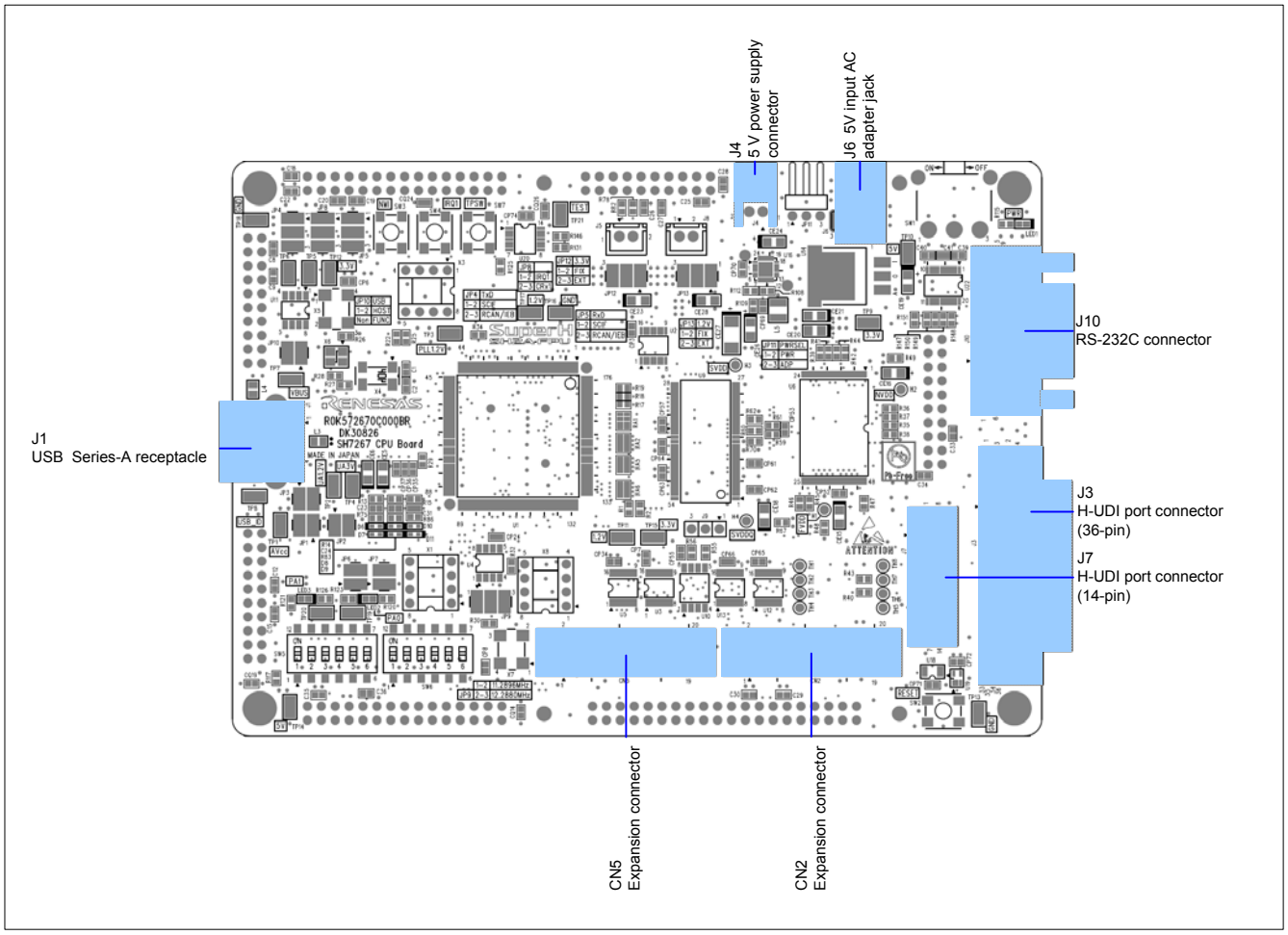


Figure 5.1.1 R0K572670C000BR Connectors (Top View of the Component Side)

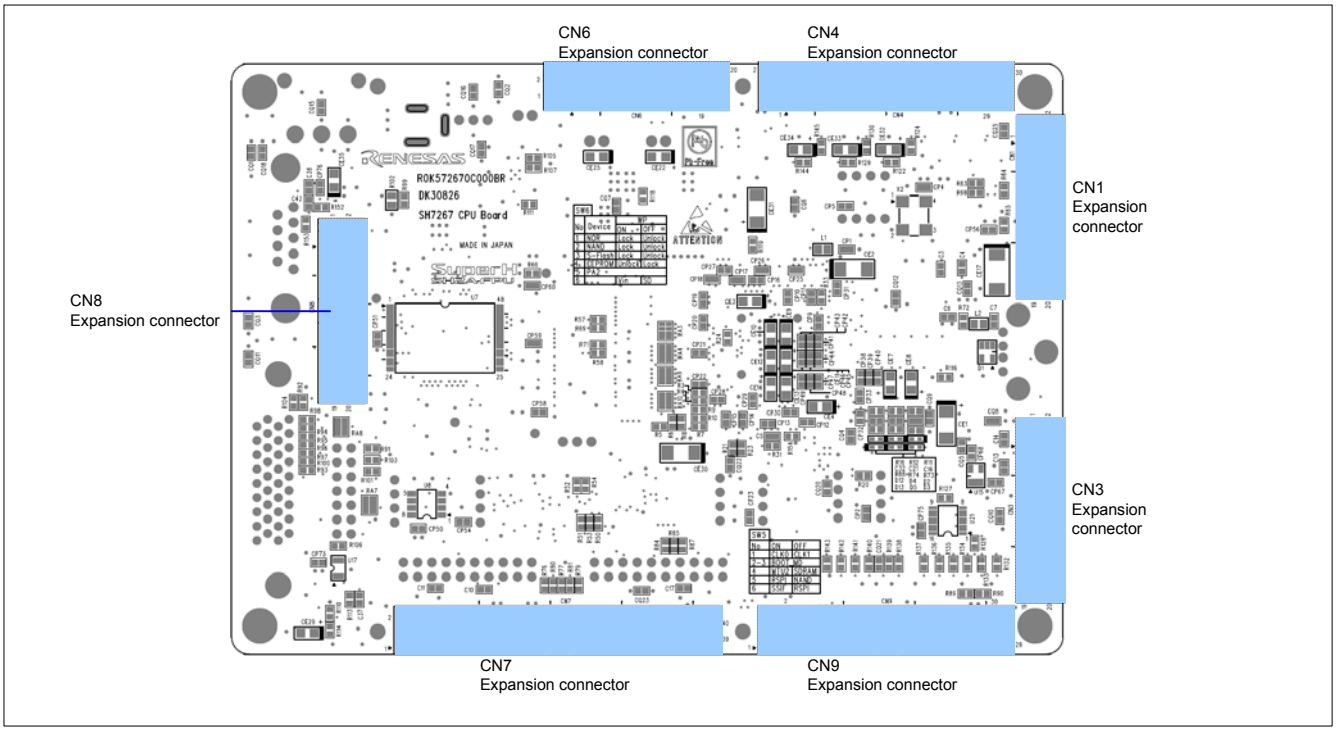


Figure 5.1.2 R0K572670C000BR Connectors (Top View of the Solder Side)

5.1.1 USB Connectors (J1 and J2)

The R0K572670C000BR includes a USB Series-A receptacle (J1).

Remove the series-A receptacle to connect a USB mini-B receptacle (J2). Refer to Table 1.6.2 in Chapter 1 for the USB mini-B receptacle allowed on the R0K572670C000BR.

The following figure shows the pin assignments for J1.

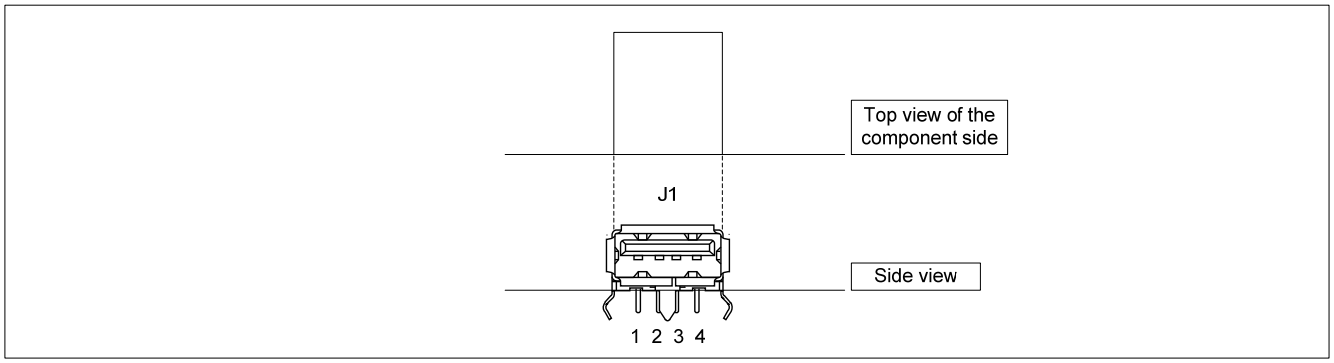


Figure 5.1.3 J1 Pin Assignments

The following figure shows the pin assignments for J2.

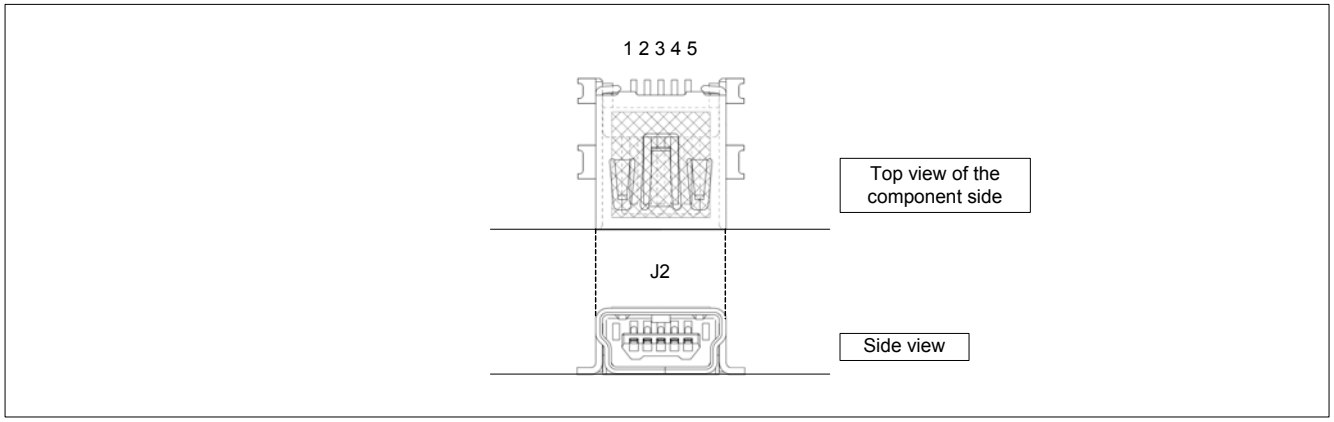


Figure 5.1.4 J2 Pin Assignments

The following table lists the pin descriptions for J1.

Table 5.1.1 J1 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	VBUS	3	DP
2	DM	4	GND

The following table lists the pin descriptions for J2.

Table 5.1.2 J2 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	VBUS	4	ID (Connected to a test pin)
2	DM	5	GND
3	DP	–	

5.1.2 H-UDI port connector (36-pin, J3)

The R0K572670C000BR includes a 36-pin H-UDI port connector (J3) to connect the board to an E10A-USB emulator.

The following figure shows the pin assignments for J3.

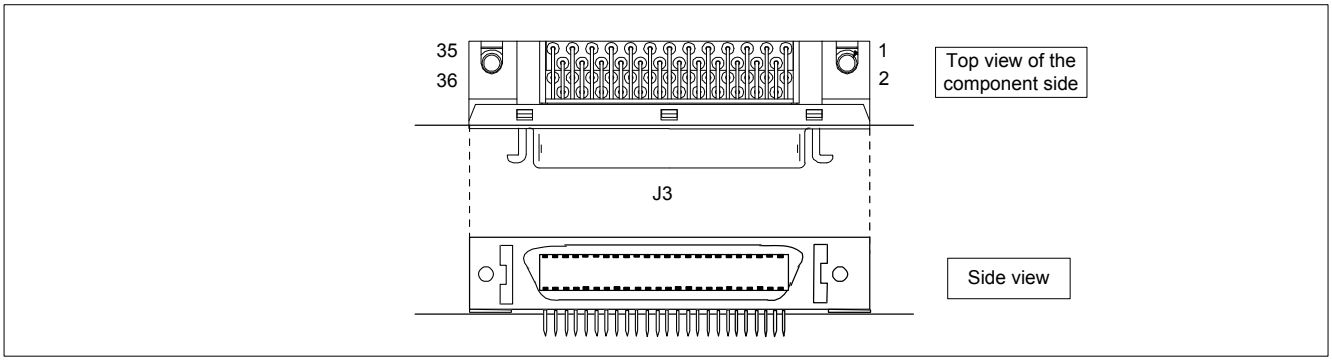


Figure 5.1.5 J3 Pin Assignments

The following table lists the pin descriptions for J3.

Table 5.1.3 J3 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	AUDCK	19	TMS
2	GND	20	GND
3	AUDATA0	21	TRST#
4	GND	22	ASEMD#
5	AUDATA1	23	TDI
6	GND	24	GND
7	AUDATA2	25	TDO
8	GND	26	GND
9	AUDATA3	27	ASEBRKAK#/ASEBRK#
10	GND	28	GND
11	AUDSYNC#	29	3.3 V
12	GND	30	GND
13	NC	31	RESET#
14	GND	32	GND
15	NC	33	GND
16	GND	34	GND
17	TCK	35	NC
18	GND	36	GND

5.1.3 5 V Power Supply Connector (J4)

The R0K572670C000BR includes a system power supply connector.

The following figure shows the pin assignments for J4.

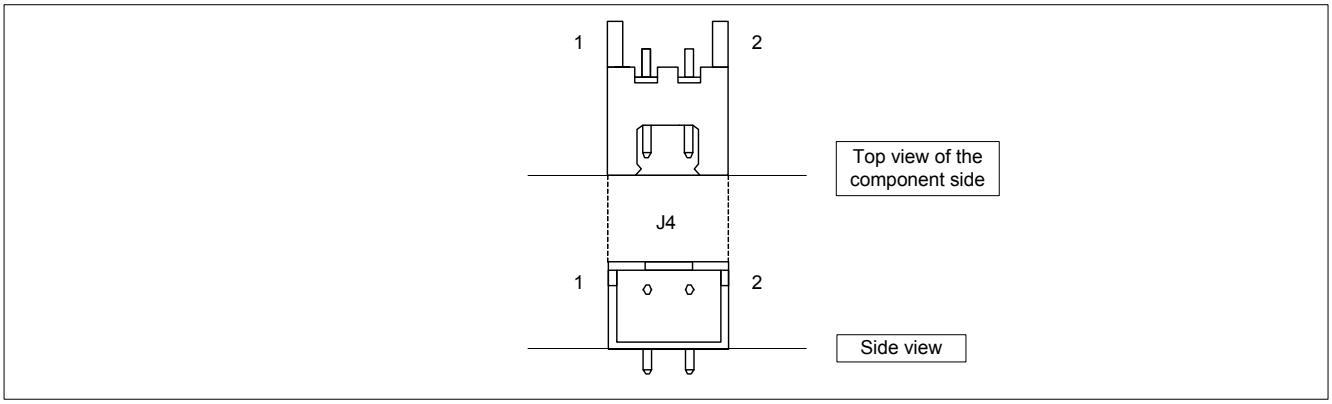


Figure 5.1.6 J4 Pin Assignments

The following table lists the pin descriptions for J4.

Table 5.1.4 J4 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	2	GND

5.1.4 5 V Input AC Adapter Jack (J6)

The R0K572670C000BR includes an AC adapter jack (J6) for 5 V DC input.

The following figure shows the pin assignments for J6.

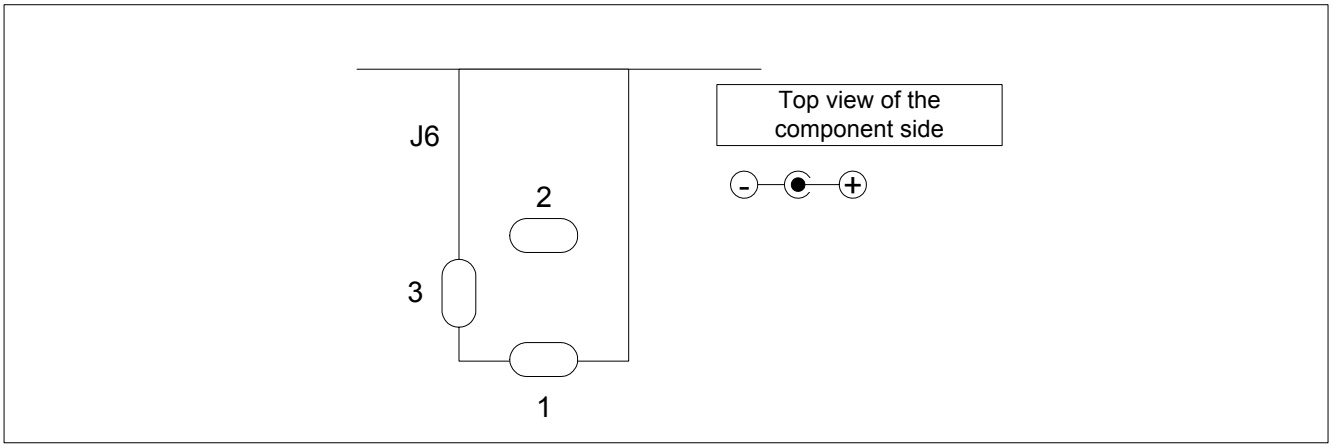


Figure 5.1.7 J6 Pin Assignments

The following table lists the pin descriptions for J6.

Table 5.1.5 J6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	3	GND
2	GND	–	

5.1.5 H-UDI port connector (14-pin, J7)

The R0K572670C000BR includes a 14-pin H-UDI port connector (J7) to connect the board to an E10A-USB emulator.

The following figure shows the pin assignments for J7.

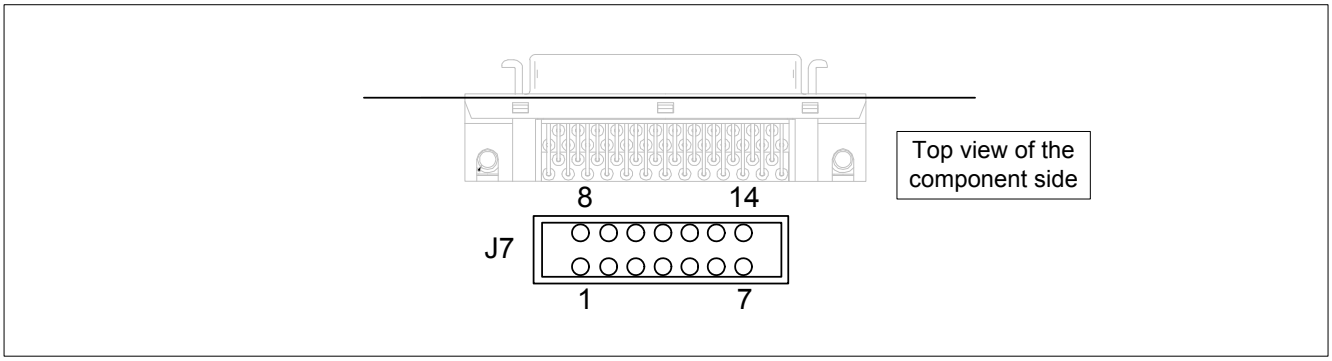


Figure 5.1.8 J7 Pin Assignments

The following table lists the pin descriptions for J7.

Table 5.1.6 J7 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	TCK	8	NC
2	TRST#	9	ASEMD#
3	TDO	10	GND
4	ASEBRKAK#/ASEBRK#	11	3.3 V
5	TMS	12	GND
6	TDI	13	GND
7	RESET#	14	GND

5.1.6 RS-232C Connector (J10)

The R0K572670C000BR includes an RS-232C connector (J10).

The following figure shows the pin assignments for J10.

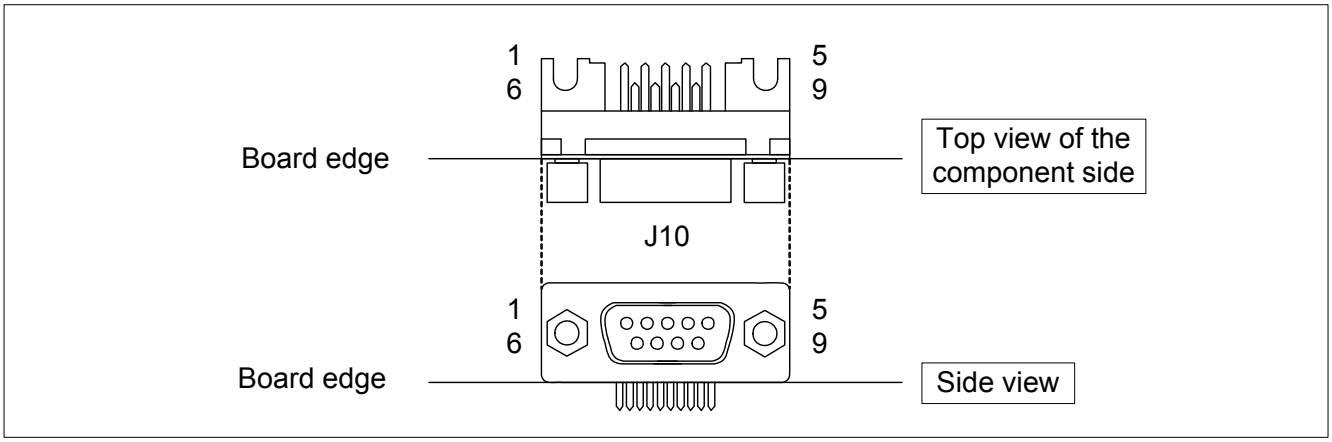


Figure 5.1.9 J10 Pin Assignments

The following table lists the pin descriptions for J10.

Table 5.1.7 J10 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC	6	DSR#
2	RXD (PJ1/CRx0/IERxD/IRQ0/RxD0)	7	RTS#
3	TXD (PJ0/CTx0/IETxD/CS1#/TxD0/A0)	8	CTS#
4	DTR#	9	NC
5	GND	–	

Pins 4 to 6 and 7 to 8 are loopback-connected.

5.1.7 Expansion Connectors (CN1 to CN9)

The R0K572670C000BR includes through-holes for mounting expansion connectors (CN1 to CN9).

Figure 5.1.10 and Figure 5.1.11show the pin assignments for expansion connectors. Table 5.1.8 to Table 5.1.16 lists the pin descriptions.

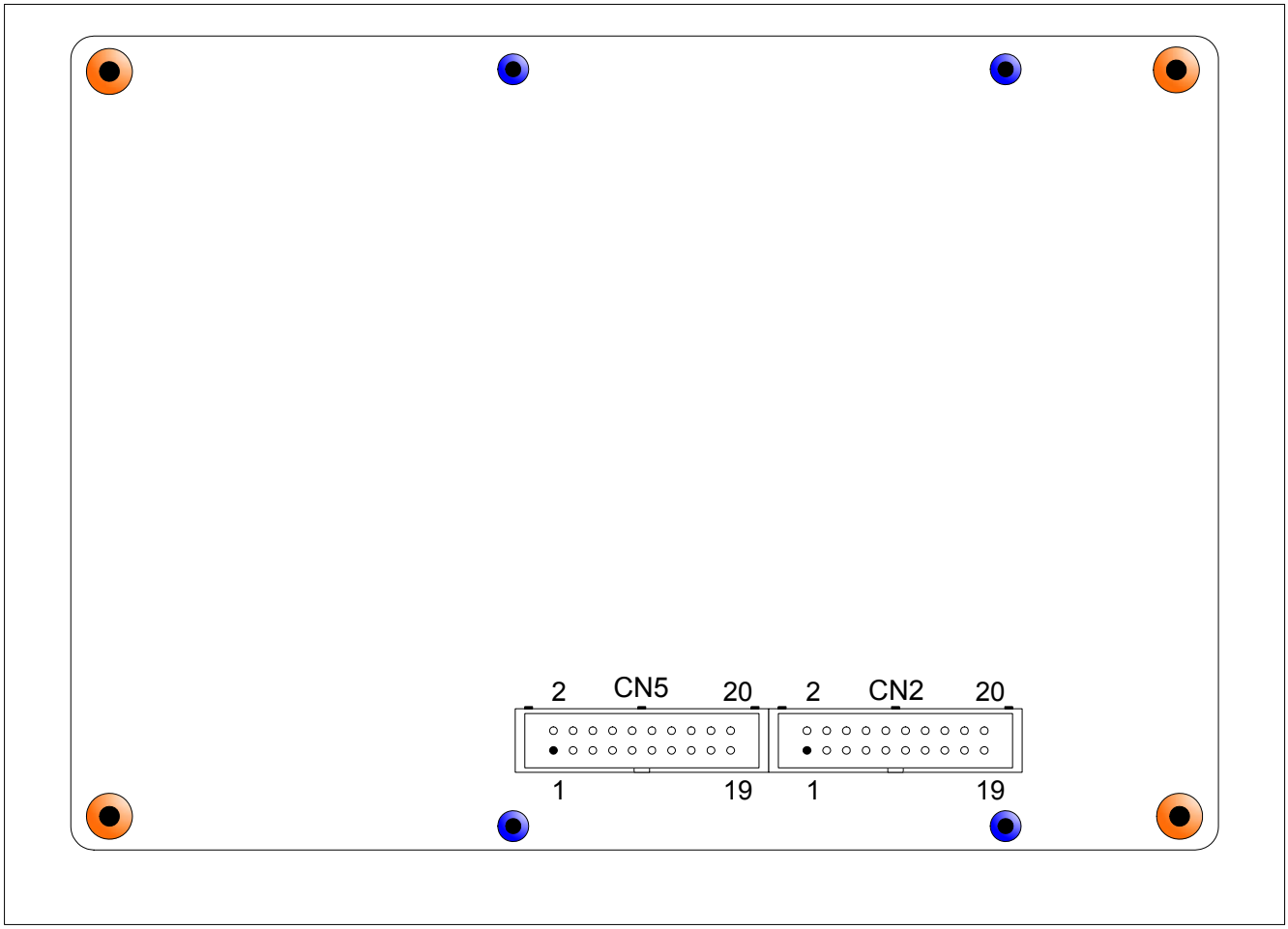


Figure 5.1.10 Expansion Connectors Pin Assignments (Top View of the Component Side)

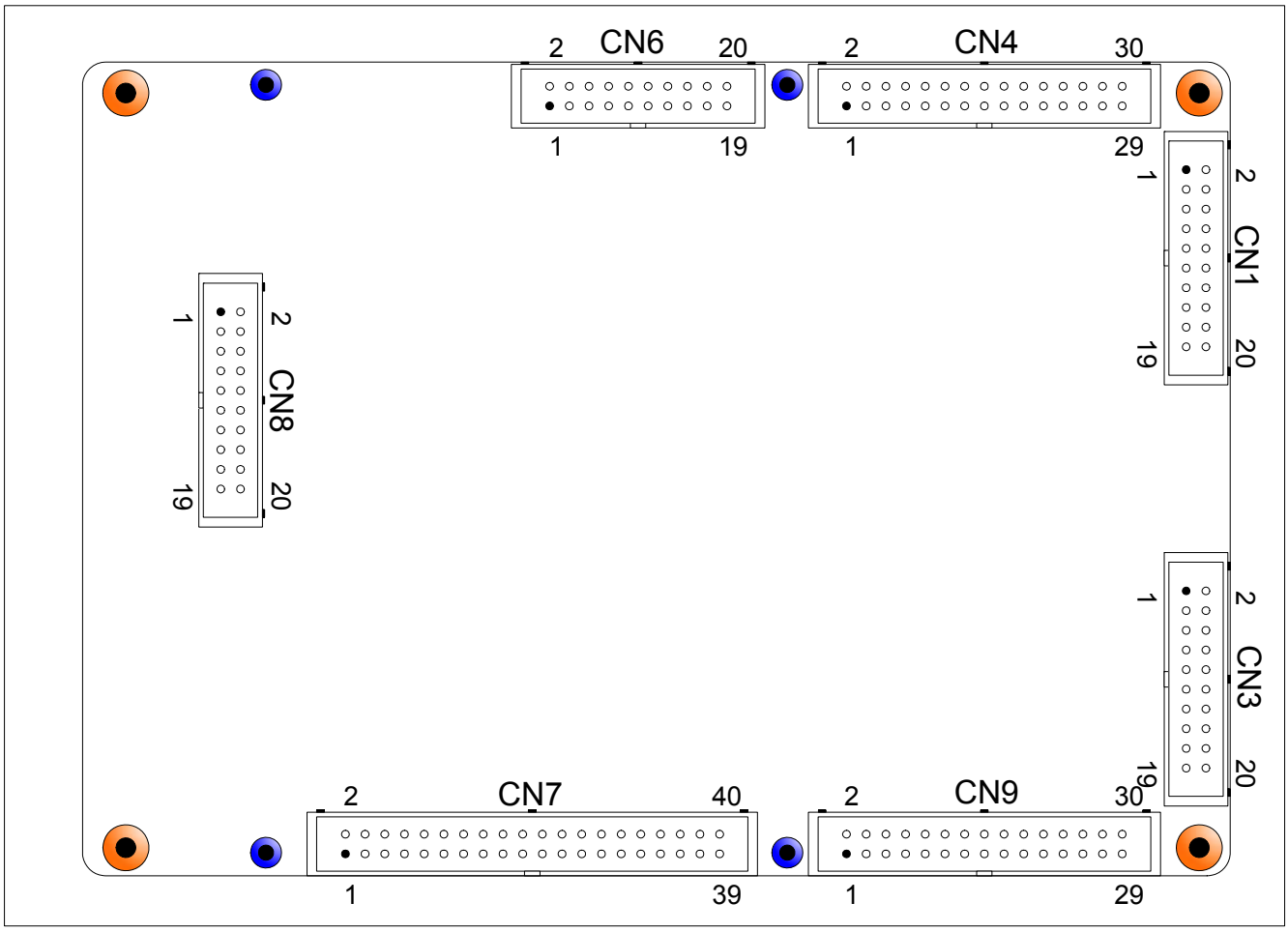


Figure 5.1.11 Expansion Connectors Pin Assignments (Top View of the Solder Side)

Table 5.1.8 CN1 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC	11	GND
2	PH4/AN4	12	NC
3	5 V	13	NC
4	PH5/AN5	14	NC
5	NC	15	NC
6	3.3 V	16	GND
7	NC	17	PJ3/CRx1/CRx0&CRx1/IRQ1/AUDIO_XOUT/ WDTOVF#
8	PA2/MD_BOOT1	18	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/ LCD_M_DISP
9	PA1/MD_BOOT0	19	PJ1/CRx0/IERxD/IRQ0/RxD0
10	PA0/MD_CLK1	20	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 5.1.9 CN2 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	11	PE2/SCL1/IRQ2
2	GND	12	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#/ LCD_EXTCLK
3	NC	13	PE0/SCL0/AUDIO_CLK/IRQ0
4	NC	14	5 V
5	NC	15	NC
6	NC	16	NC
7	3.3 V	17	NC
8	PE5/SDA2/DV_HSYNC	18	NC
9	PE4/SCL2/DV_VSYNC	19	GND
10	PE3/SDA1/IRQ3	20	GND

Table 5.1.10 CN3 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	AVref	11	NC
2	AVref	12	NC
3	PH1/AN1	13	AVcc
4	PH0/AN0	14	AVcc
5	AVref	15	NC
6	AVref	16	NC
7	PH3/AN3	17	AVss
8	PH2/AN2	18	AVss
9	AVcc	19	AVss
10	AVcc	20	AVss

Table 5.1.11 Pin Descriptions (CN4)

Pin Number	Signal Name	Pin Number	Signal Name
1	PB1/A1/LCD_HSYNC	16	GND
2	PB2/A2/LCD_VSYNC	17	PB13/A13/TIOC3B/LCD_DATA5
3	PB3/A3/LCD_DATA15	18	PB14/A14/TIOC3C/LCD_DATA4
4	PB4/A4/TIOC0A/LCD_DATA14	19	PB15/A15/TIOC3D/LCD_DATA3
5	PB5/A5/TIOC0B/LCD_DATA13	20	PB16/A16/TIOC4A/LCD_DATA2
6	PB6/A6/TIOC0C/LCD_DATA12	21	PB17/A17/TIOC4B/LCD_DATA1/SCK1
7	GND	22	PB18/A18/TIOC4C/LCD_DATA0/TxD1
8	GND	23	3.3 V
9	PB7/A7/TIOC0D/LCD_DATA11	24	3.3 V
10	PB8/A8/TIOC1A/LCD_DATA10	25	PB19/A19/TIOC4D/RxD1
11	PB9/A9/TIOC1B/LCD_DATA9	26	PB20/A20/SPDIF_IN/SCK4
12	PB10/A10/TIOC2A/LCD_DATA8	27	PB21/A21/SPDIF_OUT/TxD4
13	PB11/A11/TIOC2B/LCD_DATA7	28	PB22/A22/CS4#/RxD4
14	PB12/A12/TIOC3A/LCD_DATA6	29	5 V
15	GND	30	5 V

Table 5.1.12 CN5 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC	11	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD
2	NC	12	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP
3	NC	13	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1
4	NC	14	GND
5	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT	15	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3
6	5 V	16	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/ TxD3/SD_CLK/AUDATA2
7	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN	17	PF3/ICIORD#/SSISCK1/DV_DATA3/RxD3/ SD_CMD/AUDATA1
8	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#	18	PF2/BACK#/DV_DATA2/TxD2/DACK0/ SD_D3/AUDATA0
9	GND	19	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#
10	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB	20	PF0/WAIT#/DV_DATA0/SCK2/TEND0/ AUDCK

Table 5.1.13 CN6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	11	3.3 V
2	5 V	12	PG23/MOSI1/TIOC0C
3	5 V	13	PG24/MISO1/TIOC0D
4	5 V	14	PC5/RAS#/TIOC4A/IRQ4
5	PC0/CS0#/SSIWS0	15	PC6/CAS#/TIOC4B/IRQ5
6	PC0/CS0#/SSIWS0	16	PC7/CKE/TIOC4C/IRQ6
7	PC2/RD/WR#/SSIRxD0	17	PC8/CS3#/TIOC4D/IRQ6
8	PC2/RD/WR#/SSIRxD0	18	GND
9	PC4/WE1#/DQMU/WE#	19	GND
10	3.3 V	20	CKIO

Table 5.1.14 CN7 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PF2/BACK#/DV_DATA2/TxD2/DACK0/ SD_D3/AUDATA0	21	GND
2	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#	22	PF3/ICIORD#/SSISCK1/DV_DATA3/RxD3/ SD_CMD/AUDATA1
3	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/ TxD3/SD_CLK/AUDATA2	23	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3
4	PF3/ICIORD#/SSISCK1/DV_DATA3/RxD3/ SD_CMD/AUDATA1	24	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/ TxD3/SD_CLK/AUDATA2
5	PE0/SCL0/AUDIO_CLK/IRQ0	25	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1
6	RES#	26	GND
7	PE2/SCL1/IRQ2	27	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD
8	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ ADTRG#/LCD_EXTCLK	28	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP
9	PE4/SCL2/DV_VSYNC	29	GND
10	PE3/SDA1/IRQ3	30	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB
11	3.3 V	31	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN
12	PE5/SDA2/DV_HSYNC	32	PF0/WAIT#/DV_DATA0/SCK2/TEND0/AUDCK
13	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1	33	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
14	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3	34	GND
15	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD	35	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
16	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP	36	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB
17	PF0/WAIT#/DV_DATA0/SCK2/TEND0/ AUDCK	37	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN
18	5 V	38	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
19	PF2/BACK#/DV_DATA2/TxD2/DACK0/ SD_D3/AUDATA0	39	GND
20	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#	40	AUDIO_XTAL

Table 5.1.15 CN8 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PD0/D0/PWM1A	11	PD4/D4/FRE#/PWM1E
2	PD8/D8/NAF0/PWM2A	12	PD12/D12/NAF4/PWM2E
3	PD1/D1/PWM1B	13	PD5/D5/FCLE/PWM1F
4	PD9/D9/NAF1/PWM2B	14	PD13/D13/NAF5/PWM2F
5	GND	15	3.3 V
6	PD2/D2/PWM1C	16	PD6/D6/FALE/PWM1G
7	PD10/D10/NAF2/PWM2C	17	PD14/D14/NAF6/PWM2G
8	PD3/D3/PWM1D	18	PD7/D7/FWE#/PWM1H
9	PD11/D11/NAF3/PWM2D	19	PD15/D15/NAF7/PWM2H
10	GND	20	5 V

Table 5.1.16 CN9 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PG1/LCD_DATA1/SD_D3/PINT1	16	PG12/LCD_DATA12/TIOC0A/RxD6
2	PG0/LCD_DATA0/SD_D2/PINT0	17	PG14/LCD_DATA14/TIOC0C/RxD7
3	PG3/LCD_DATA3/SD_CLK/PINT3	18	PG13/LCD_DATA13/TIOC0B/TxD6
4	PG2/LCD_DATA2/SD_CMD/PINT2	19	PG16/LCD_VSYNC/TIOC1A/RxD1
5	GND	20	PG15/LCD_DATA15/TIOC0D/TxD7
6	PG4/LCD_DATA4/SD_D0/PINT4/IRQ4	21	PG17/LCD_HSYNC/TIOC1B/TxD1
7	PG6/LCD_DATA6/SD_WP/PINT6/IRQ6	22	5 V
8	PG5/LCD_DATA5/SD_D1/PINT5/IRQ5	23	PG19/LCD_CLK/TIOC2B/TxD3/CTS1
9	PG7/LCD_DATA7/SD_CD/PINT7/IRQ7	24	PG18/LCD_DE/TIOC2A/RxD3/RTS1
10	GND	25	3.3 V
11	PG9/LCD_DATA9/SSIRxD0/TxD4/SIOFSYNC	26	PG20/LCD_EXTCLK/SCK1
12	PG8/LCD_DATA8/SSITxD0/RxD4/SIOFSCK	27	PG22/SSL1/TIOC0B
13	PG11/LCD_DATA11/SSIWS0/IRQ3/TxD5/ SIOFTxD	28	PG21/RSPCK1/TIOC0A
14	PG10/LCD_DATA10/SSISCK0/IRQ2/ RxD5/SIOFRxD	29	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#
15	GND	30	NC (This pin must be pulled up by a 10-kΩ resistor)

5.2 R0K572670C000BR Operating Components

The following figure shows the assignments of the R0K572670C000BR operating components.

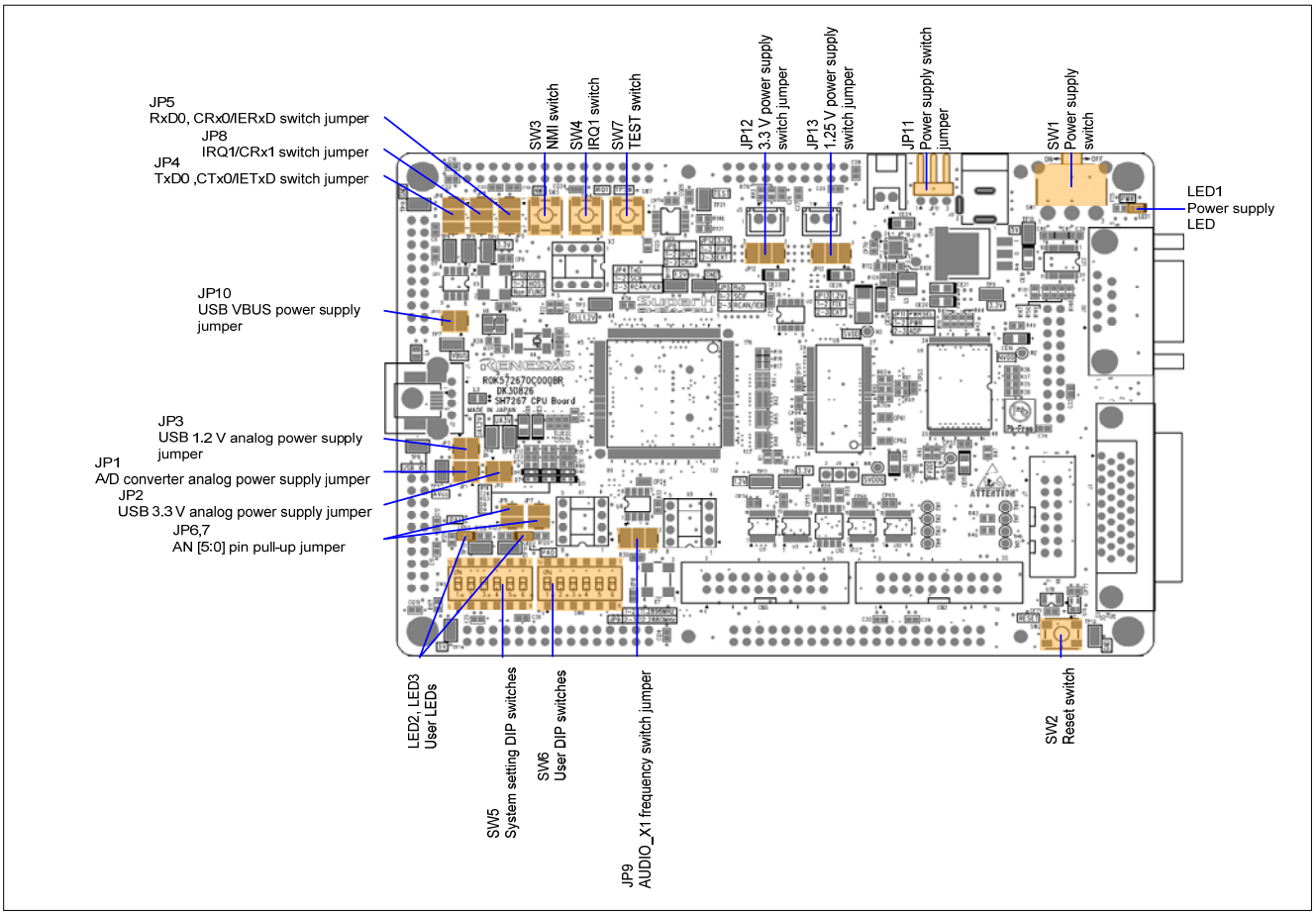


Figure 5.2.1 R0K572670C000BR Operating Component Assignments

5.2.1 Jumpers (JP1 to JP13)

The R0K572670C000BR includes 13 jumpers.

The figure below shows jumper assignments (JP1 to JP13) on the R0K572670C000BR.

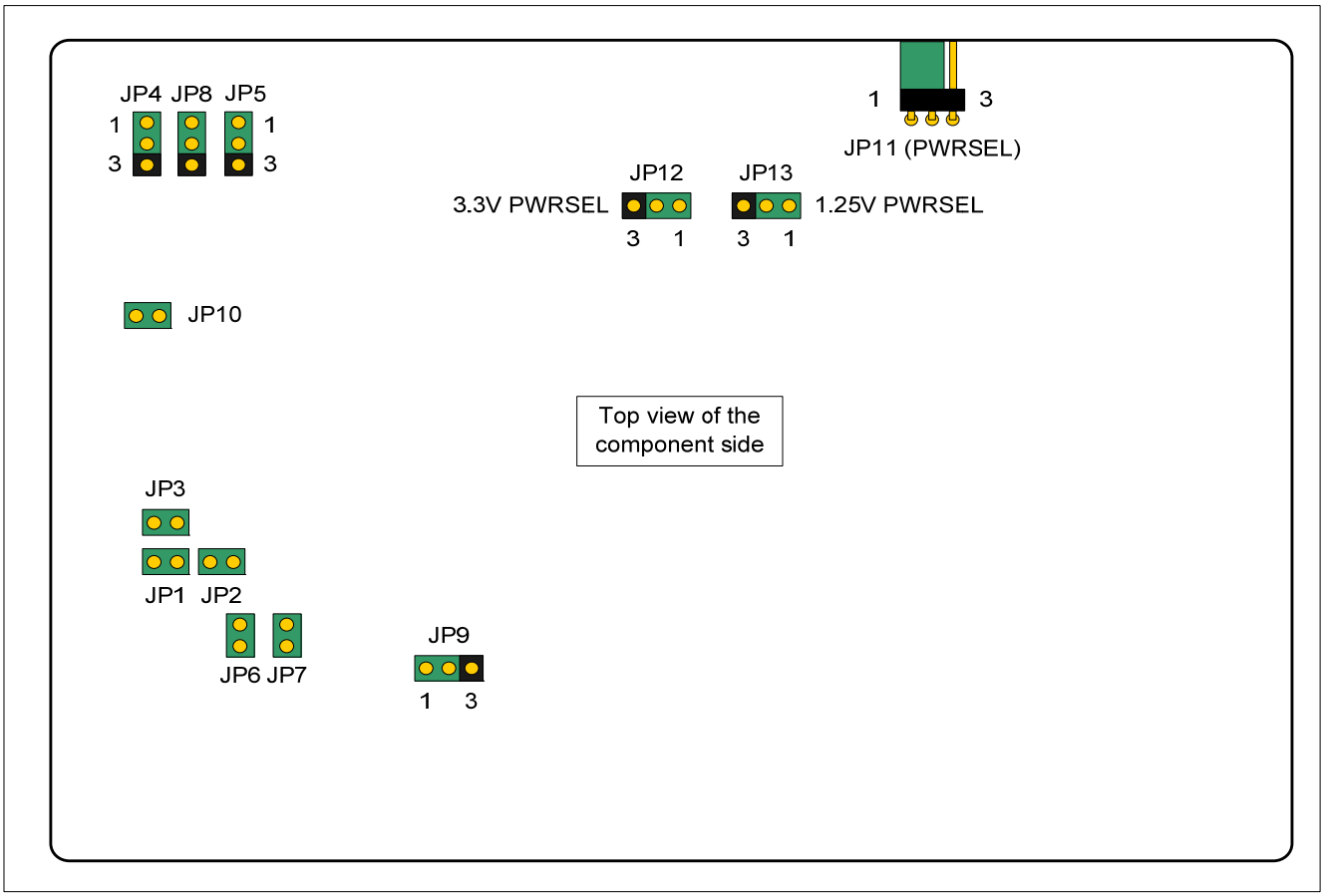


Figure 5.2.2 R0K572670C000BR Jumper Assignments (JP1 to JP15)

Table 5.2.1 to Table 5.2.6 lists jumpers settings (JP1 to JP13).

Table 5.2.1 Analog Power Supply Jumpers Setting (JP1 to JP3)

Number	Setting	Description
JP1	1 - 2	Supplies 3.3 V analog power for the A/D converter (AVcc) (1)
	Open	Does not supply 3.3 V analog power for the A/D converter (AVcc)
JP2	1 - 2	Supplies 3.3 V analog power for USB (USBAPVcc) (1)
	Open	Does not supply 3.3 V analog power for USB (USBAPVcc)
JP3	1 - 2	Supplies 1.25 V analog power for USB (USBAVcc) (1)
	Open	Does not supply 1.25 V analog power for USB (USBAVcc)

Notes:

1. Default setting

2. Do not change the jumper settings while the R0K572670C000BR is ON. Be sure to turn the power OFF before changing the settings.

Table 5.2.2 Multiplexed Pin Switch Jumpers Setting (JP4, JP5, and JP8)

Number	Setting	Description
JP4 TxD0/CTx0/IETxD	1 - 2	Connects the RS-232C driver (U22) as the TxD0 OUT pin (1)
	2 - 3	Connects the expansion connector (CN1) as the CTx0/IETxD OUT pin
JP5 RxD0/CRx0/IERxD	1 - 2	Connects the RS-232C driver (U22) as the RxD0 IN pin (1)
	2 - 3	Connects the expansion connector (CN1) as the CRx0/IERxD IN pin
JP8 IRQ1/CRx1	1 - 2	Connects IRQ1 switch (SW4) as the IRQ1 IN pin (1)
	2 - 3	Connects the expansion connector (CN1) as the CRx1 IN pin

Note 1: Default setting.

Table 5.2.3 Pin Pull-up Jumpers Setting (JP6, and JP7)

Number	Setting	Description
JP6 PH/AN [0:3]	1 - 2	Pulls up PH/AN [0:3] pin (1) (2)
	None (Open)	Does not pull up PH/AN [0:3] pin
JP7 PH/AN [4:5]	1 - 2	Pulls up PH/AN [4:5] pin (1)
	None (Open)	Does not pull up PH/AN [4:5] pin

Notes:

1: Default setting

2: Mount the resistors (R11 to R14) when using this setting.

Table 5.2.4 AUDIO_X1 Frequency Switch Jumper Setting (JP9)

Number	Setting	Description
JP9	1 - 2	Inputs the clock of 11.2896 MHz to AUDIO_X1 pin (1)
	2 - 3	Inputs the clock of 12.2880 MHz to AUDIO_X1 pin

Note 1: Default setting

Table 5.2.5 USB VBUS Power Supply Jumper Setting (JP10)

Number	Setting	Description
JP10	1 - 2	USB host mode (Supplies the power to VBUS) (1)
	None (Open)	USB function mode (Does not supply the power to VBUS)

Note 1: Default setting

Table 5.2.6 Power Supply Switch Jumper Setting (JP11 to JP13)

Number	Setting	Description
JP11 PWRSEL	1 - 2	Supplies the system power from J4 (1)
	2 - 3	Supplies the system power from J6 (AC adapter is used)
JP12 3.3V PWRSEL	1 - 2	Supplies 3.3 V power for the SH7267 from U14 (Internal power supply) (1)
	2 - 3	Supplies 3.3 V power for the SH7267 from J5 (External power supply)
JP13 1.25V PWRSEL	1 - 2	Supplies 1.25 V power for the SH7267 from U16 (Internal power supply) (1)
	2 - 3	Supplies 1.25 V power for the SH7267 from J8 (External power supply)

Notes:

1: Default setting

2. Do not change the jumper settings while the R0K572670C000BR is ON. Be sure to turn the power OFF before changing the settings.

5.2.2 Switches and LEDs

The R0K572670C000BR includes seven switches and three LEDs.

The figure below shows the assignments of switches and LEDs. Table 5.2.10 lists LEDs on the R0K572670C000BR.

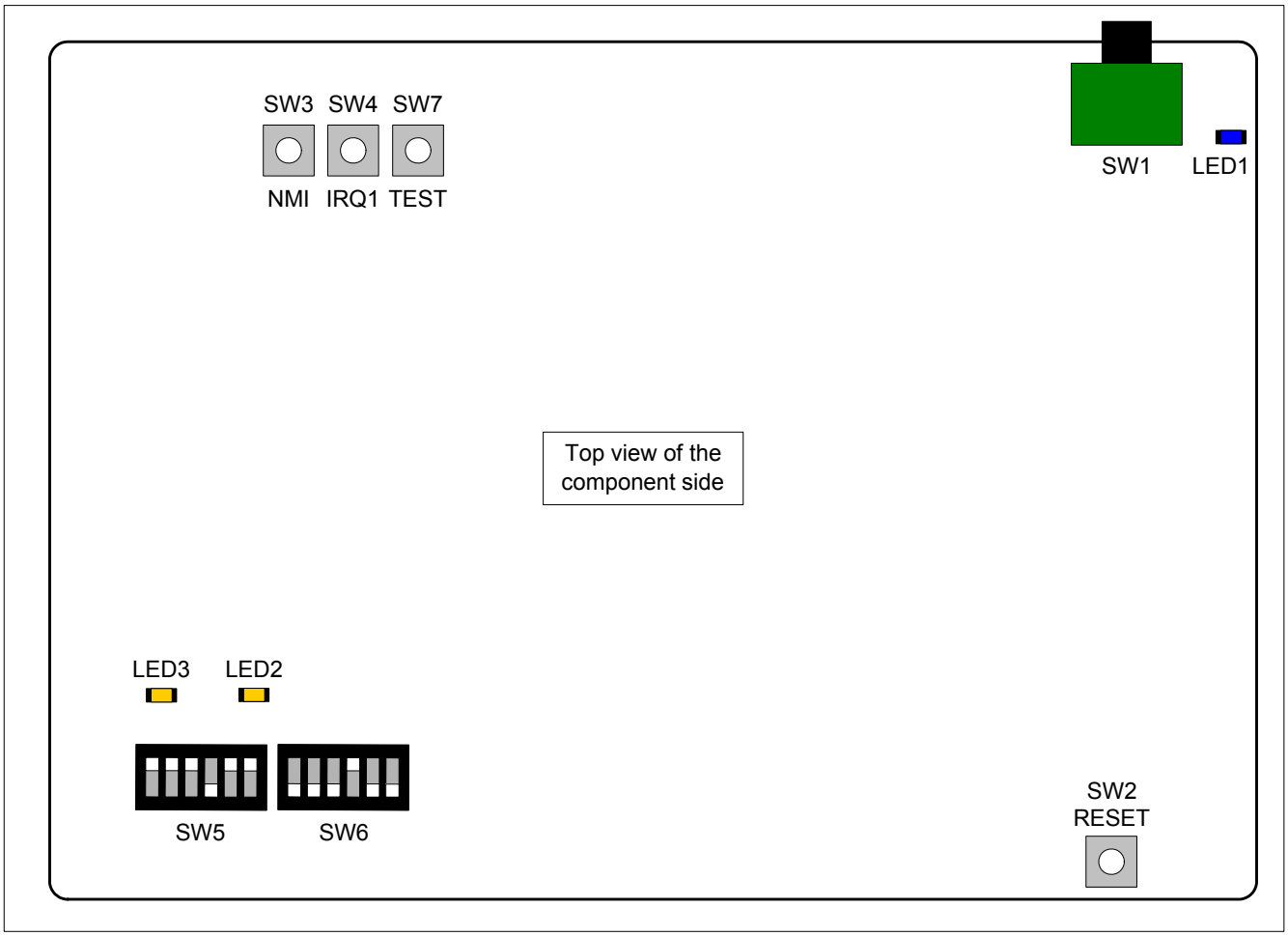


Figure 5.2.3 R0K572670C000BR Switches and LEDs Assignments

The following table lists switches mounted on the board.

Table 5.2.7 Switches

Number	Name	Remarks
SW1	Power supply switch	-
SW2	Reset switch	Refer to Section 2.9 for details.
SW3	NMI switch	Refer to Section 2.7 for details.
SW4	IRQ1 switch	Refer to Section 2.7 for details.
SW5	System setting DIP switches (6/package)	Refer to Table 5.2.8 for details.
SW6	User DIP switches (6/package)	Refer to Table 5.2.9 for details.
SW7	TEST switch	Refer to Section 2.7 for details.

Table 5.2.8 System setting DIP switches

Number	Setting		Description
SW5-1 MD_CLK0	OFF	MD_CLK0 = High	Clock operating mode 1
	ON	MD_CLK0 = Low	Clock operating mode 0 (1)
SW5-2 MD_BOOT0	OFF	MD_BOOT0 = High	Boot mode: Boot options 0: NOR flash memory (1) 1, 3: Serial flash memory 2: NAND flash memory
	ON	MD_BOOT0 = Low (1)	
SW5-3 MD_BOOT1	OFF	MD_BOOT1 = High	
	ON	MD_BOOT1 = Low (1)	
SW5-4 SD_SEL	OFF	SD_SEL = High	Connected to the SDRAM (1)
	ON	SD_SEL = Low	Connected to the expansion connector (MTU2)
SW5-5 NAND_SEL	OFF	NAND_SEL = High	Connected to the NAND flash memory
	ON	NAND_SEL = Low	Connected to the device which is connected to the RSPI/SSIF (1)
SW5-6 RSPI_SEL	OFF	RSPI_SEL = High	Connected to the serial flash memory/ expansion connector (RSPI)
	ON	RSPI_SEL = Low	Connected to the expansion connector (SSIF) (1)

Note 1: Default setting

Table 5.2.9 User DIP Switches

Number	Setting		Description
SW6-1 NOR_WP#	OFF	NOR_WP# = High	NOR flash memory is write-enabled (1)
	ON	NOR_WP# = Low	NOR flash memory is write-protected
SW6-2 NAND_WP#	OFF	NAND_WP# = High	NAND flash memory is write-enabled (1)
	ON	NAND_WP# = Low	NAND flash memory is write-protected
SW6-3 SF_WP#	OFF	SF_WP# = High	Serial flash memory is write-enabled (1)
	ON	SF_WP# = Low	Serial flash memory is write-protected
SW6-4 E2P_WP	OFF	EEPROM_WP = High	EEPROM is write-protected
	ON	EEPROM_WP = Low	EEPROM is write-enabled (1)
SW6-5 PA2	OFF	PA2 = High (1)	
	ON	PA2 = Low	
SW6-6 VIN#/SD	OFF	VIN#/SD = High (1)	Expansion connector (SDHI) (1)
	ON	VIN#/SD = Low	Expansion connector (VDC3)

Note 1: Default setting

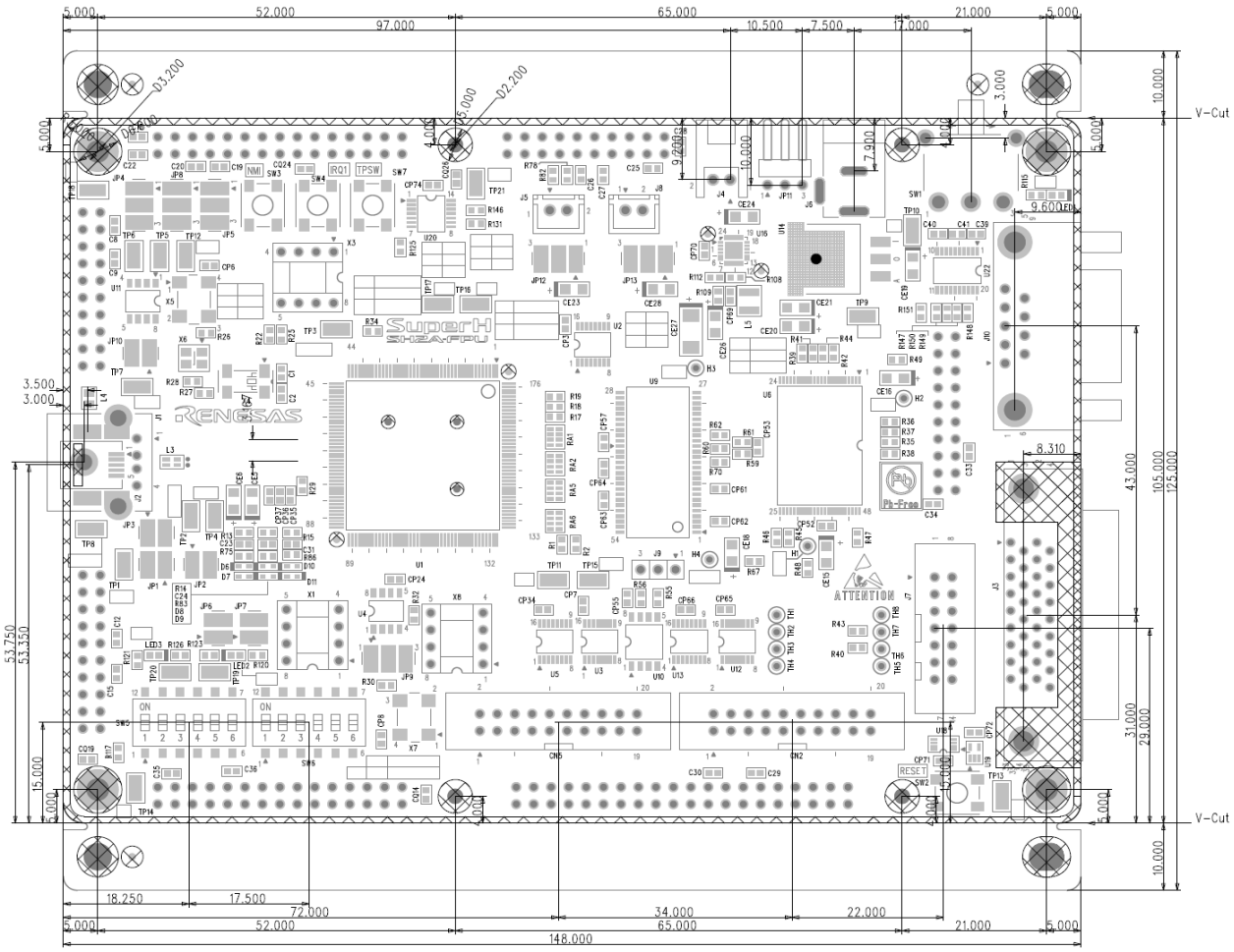
The following table lists LEDs.

Table 5.2.10 LEDs

Number	Color	Description
LED1	Blue	Power supply LED (LED1 is illuminated when 5 V power is supplied)
LED2	Yellow	User LED (LED2 is illuminated when PA0/MD_CLK0 outputs low)
LED3	Yellow	User LED (LED3 is illuminated when PA1/MD_BOOT0 outputs low)

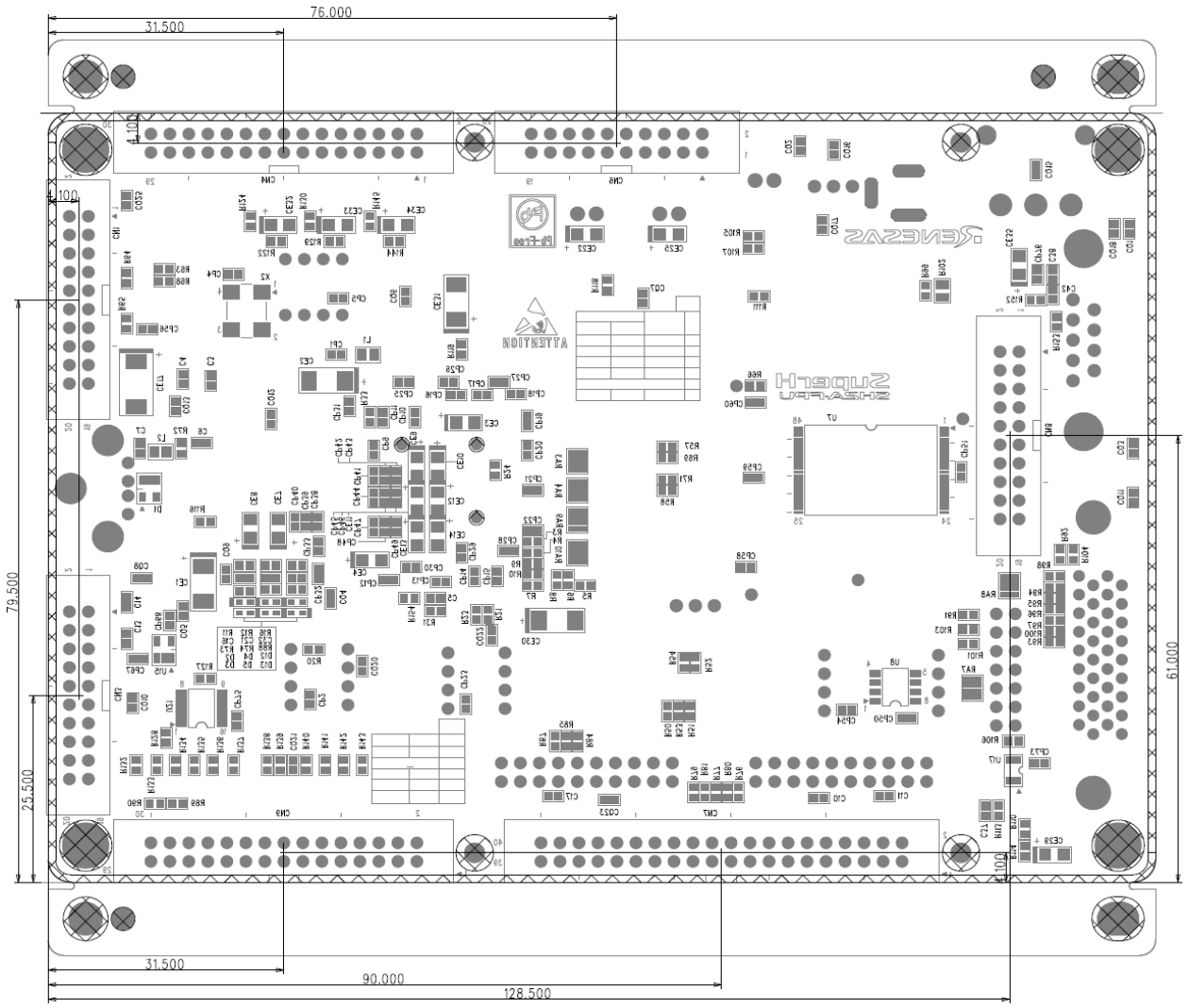
5.3 R0K572670C000BR Dimensions

Figure 5.3.1 and Figure 5.3.2 show the R0K572670C000BR dimensions.



Note: All measurements are in millimeters.

Figure 5.3.1 R0K572670C000BR Dimensions (Top View of the Component Side)



Note: All measurements are in millimeters.

Figure 5.3.2 R0K572670C000BR Dimensions (Transparent View of the Component Side)

Chapter 6
M3A-HS64G01 Operating Specifications

6.1 M3A-HS64G01 Connectors

Figure 6.1.1 and Figure 6.1.2 show the connector assignments for the M3A-HS64G01.

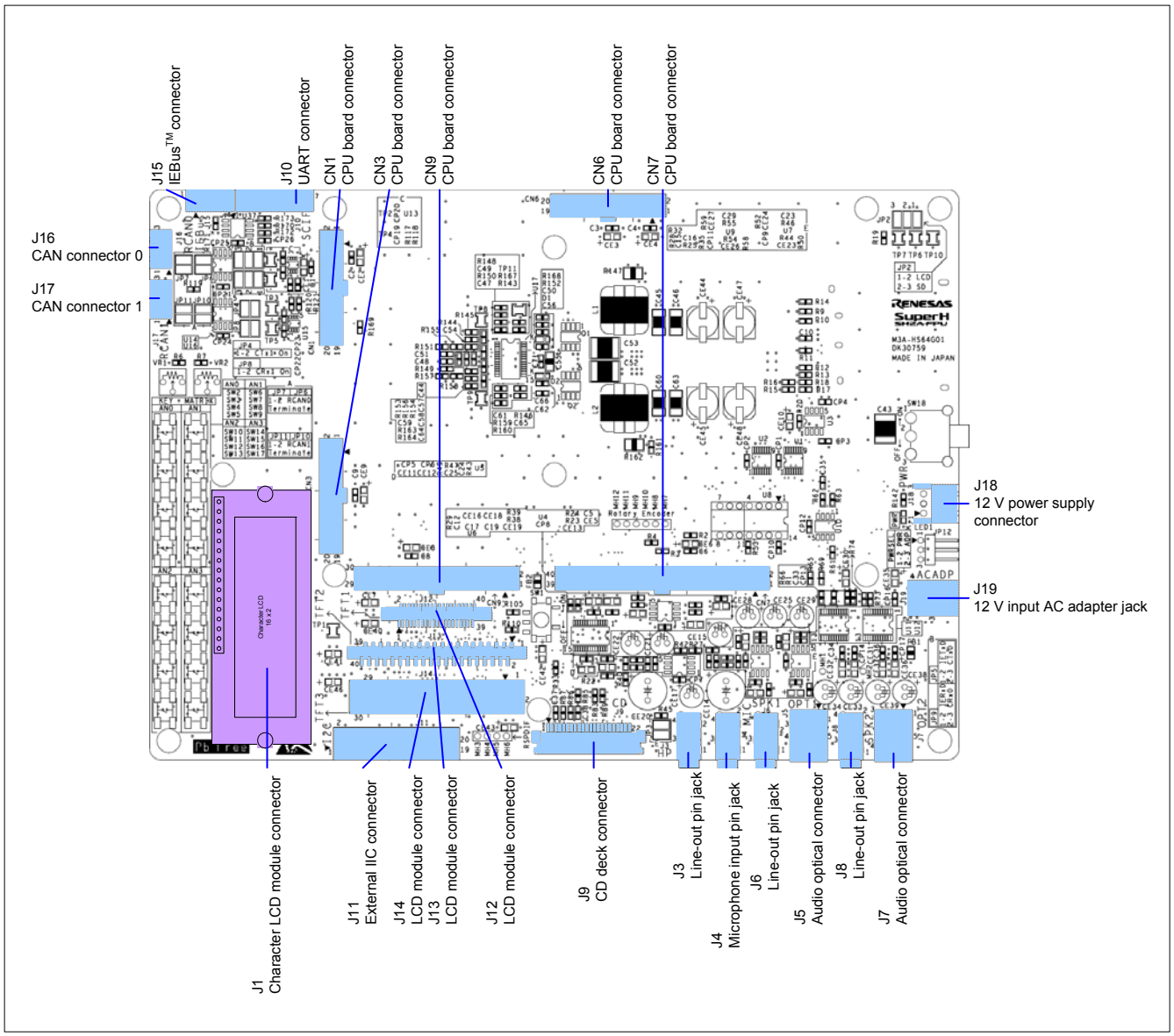


Figure 6.1.1 M3A-HS64G01 Connectors (Top View of the Component Side)

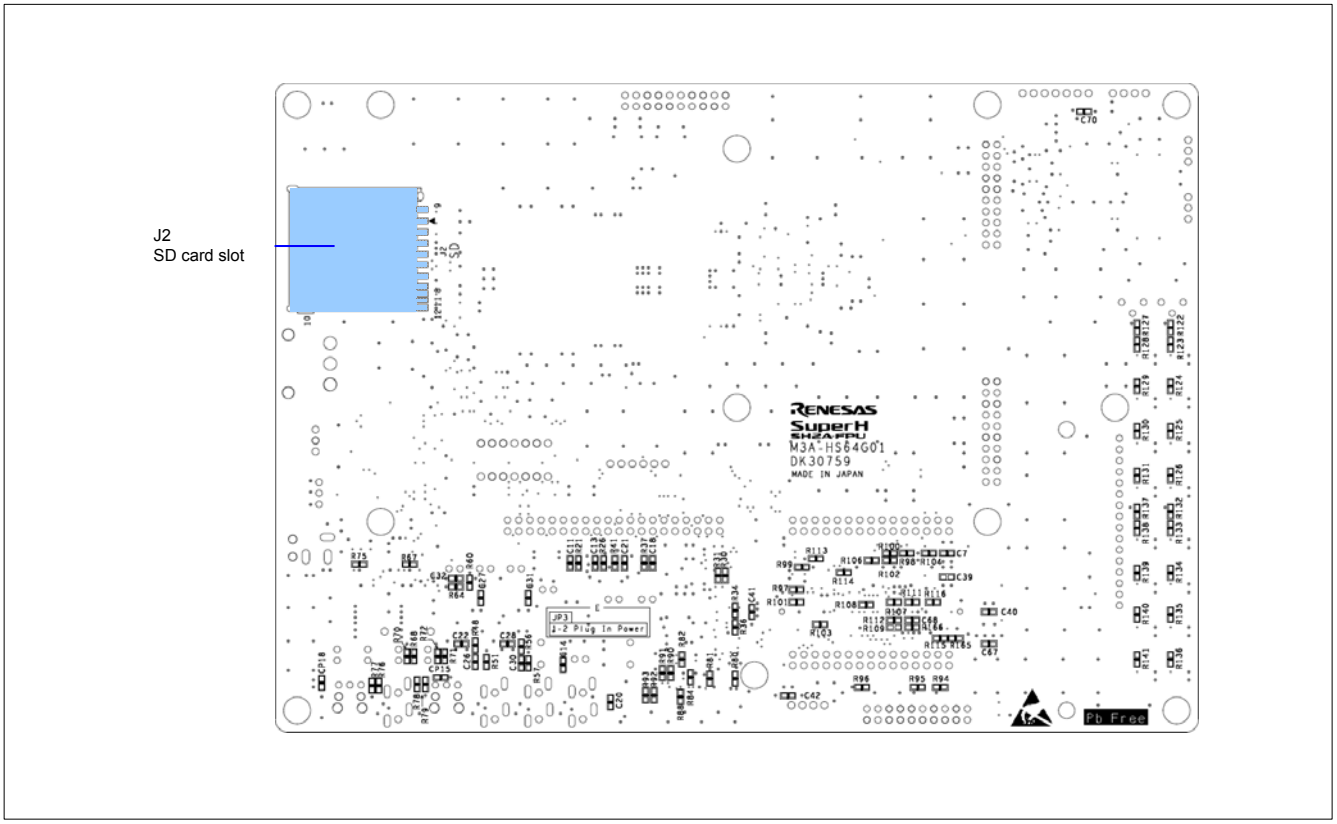


Figure 6.1.2 M3A-HS64G01 Connectors (Top View of the Solder Side)

6.1.1 CPU Board Connectors (CN1, CN3, CN6, CN7 and CN9)

The M3A-HS64G01 includes MIL-spec connectors (CN1, CN3, CN6, CN7, and CN9) for connecting the optional board to the R0K572670C000BR.

The following figure shows the pin assignments for the CPU board connectors. Table 6.1.1 to Table 6.1.5 list the pin descriptions for the CPU board connectors.

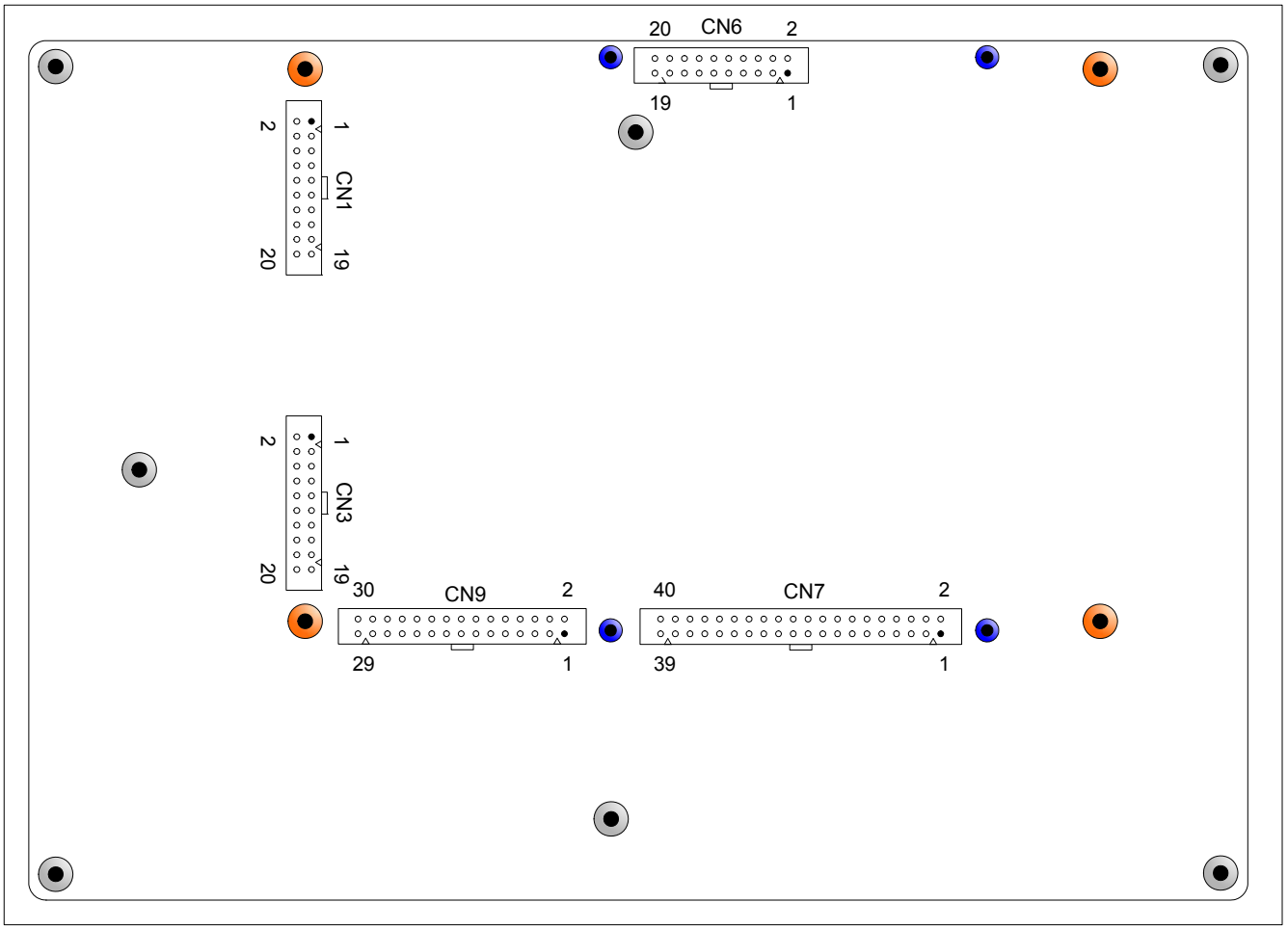


Figure 6.1.3 CPU Board Connectors Pin Assignments (Top View of the Component Side)

Table 6.1.1 CN1 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	Not connected with the R0K572670C000BR (NC)	11	GND
2	PH4/AN4	12	Not connected with the R0K572670C000BR (NC)
3	5 V	13	Not connected with the R0K572670C000BR (NC)
4	PH5/AN5	14	Not connected with the R0K572670C000BR (NC)
5	Not connected with the R0K572670C000BR (NC)	15	Not connected with the R0K572670C000BR (NC)
6	3.3 V	16	GND
7	Not connected with the R0K572670C000BR (NC)	17	PJ3/CRx1/CRx0&CRx1/IRQ1/AUDIO_XOUT/ WDTOVF#
8	PA2/MD_BOOT1 (NC)	18	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/ LCD_M_DISP
9	PA1/MD_BOOT0 (NC)	19	PJ1/CRx0/IERxD/IRQ0/RxD0
10	PA0/MD_CLK1 (NC)	20	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 6.1.2 CN3 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	AVref (NC)	11	Not connected with the R0K572670C000BR (NC)
2	AVref (NC)	12	Not connected with the R0K572670C000BR (NC)
3	PH1/AN1	13	AVcc
4	PH0/AN0	14	AVcc
5	AVref (NC)	15	Not connected with the R0K572670C000BR (NC)
6	AVref (NC)	16	Not connected with the R0K572670C000BR (NC)
7	PH3/AN3	17	AVss
8	PH2/AN2	18	AVss
9	AVcc	19	AVss
10	AVcc	20	AVss

Table 6.1.3 CN6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	11	3.3 V
2	5 V	12	PG23/MOSI1TIOC0C
3	5 V	13	PG24/MISO1/TIOC0D
4	5 V	14	PC5/RAS#/TIOC4A/IRQ4 (NC)
5	PC0/CS0#/SSIWS0 (NC)	15	PC6/CAS#/TIOC4B/IRQ5 (NC)
6	PC1/RD#/SSISCK0 (NC)	16	PC7/CKE/TIOC4C/IRQ6 (NC)
7	PC2/RD/WR#/SSIRxD0 (NC)	17	PC8/CS3#/TIOC4D/IRQ6 (NC)
8	PC3/WE0#/DQML/SSITcD0 (NC)	18	GND
9	PC4/WE1#/DQMU/WE# (NC)	19	GND
10	3.3 V	20	CKIO (NC)

Table 6.1.4 CN7 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PF2/BACK#/DV_DATA2/TxD2/DACK0/ SD_D3/AUDATA0	21	GND
2	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#	22	PF3/ICIORD#/SSISCK1/DV_DATA3/RxD3/ SD_CMD/AUDATA1
3	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/ TxD3/SD_CLK/AUDATA2	23	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3
4	PF3/ICIORD#/SSISCK1/DV_DATA3/RxD3/ SD_CMD/AUDATA1	24	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/ TxD3/SD_CLK/AUDATA2
5	PE0/SCL0/AUDIO_CLK/IRQ0	25	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1
6	RES#	26	GND
7	PE2/SCL1/IRQ2	27	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD
8	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#/ LCD_EXTCLK	28	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP
9	PE4/SCL2/DV_VSYNC	29	GND
10	PE3/SDA1/IRQ3	30	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB
11	3.3 V	31	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN
12	PE5/SDA2/DV_HSYNC	32	PF0/WAIT#/DV_DATA0/SCK2/TEND0/ AUDCK
13	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1	33	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
14	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3	34	GND
15	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD	35	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
16	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP	36	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB
17	PF0/WAIT#/DV_DATA0/SCK2/TEND0/ AUDCK	37	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN
18	5 V	38	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
19	PF2/BACK#/DV_DATA2/TxD2/DACK0/ SD_D3/AUDATA0	39	GND
20	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#	40	AUDIO_XTAL

Table 6.1.5 CN9 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PG1/LCD_DATA1/SD_D3/PINT1	16	PG12/LCD_DATA12/TIOC0A/RxD6
2	PG0/LCD_DATA0/SD_D2/PINT0	17	PG14/LCD_DATA14/TIOC0C/RxD7
3	PG3/LCD_DATA3/SD_CLK/PINT3	18	PG13/LCD_DATA13/TIOC0B/TxD6
4	PG2/LCD_DATA2/SD_CMD/PINT2	19	PG16/LCD_VSYNC/TIOC1A/RxD1
5	GND	20	PG15/LCD_DATA15/TIOC0D/TxD7
6	PG4/LCD_DATA4/SD_D0/PINT4/IRQ4	21	PG17/LCD_HSYNC/TIOC1B/TxD1
7	PG6/LCD_DATA6/SD_WP/PINT6/IRQ6	22	5 V
8	PG5/LCD_DATA5/SD_D1/PINT5/IRQ5	23	PG19/LCD_CLK/TIOC2B/TxD3/CTS1
9	PG7/LCD_DATA7/SD_CD/PINT7/IRQ7	24	PG18/LCD_DE/TIOC2A/RxD3/RTS1
10	GND	25	3.3 V
11	PG9/LCD_DATA9/SSIRxD0/TxD4/ SIOFSYNC	26	PG20/LCD_EXTCLK/SCK1（NC）
12	PG8/LCD_DATA8/SSITxD0/RxD4/SIOFSCK	27	PG22/SSL10/TIOC0B
13	PG11/LCD_DATA11/SSIWS0/IRQ3/TxD5/ SIOFTxD	28	PG21/RSPCK1/TIOC0A
14	PG10/LCD_DATA10/SSISCK0/IRQ2/RxD5/ SIOFRxD	29	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#
15	GND	30	Not connected with the R0K572670C000BR (NC)

6.1.2 Character LCD Module Connector (J1)

The M3A-HS64G01 includes a character LCD module connector (J1). This module cannot be used with the R0K572670C000BR.

The following figure shows the pin assignments for J1.

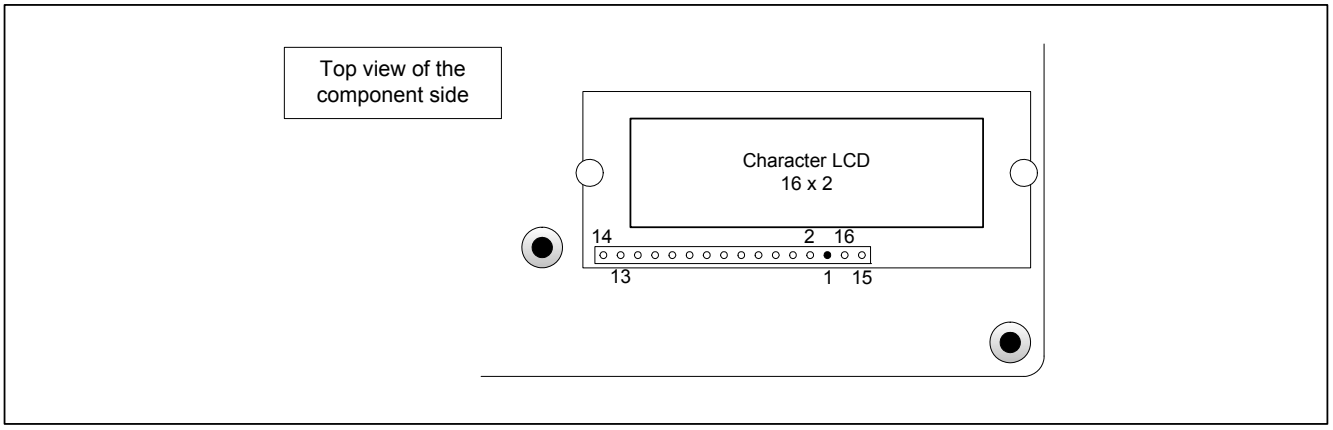


Figure 6.1.4 J1 Pin Assignments

The following table lists the pin descriptions for J1.

Table 6.1.6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	9	DB2 (PF3/ICIORD#/SSISCK1/DV_DATA3/ RxD3/SD_CMD/AUDATA1)
2	5 V	10	DB3 (PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/TxD3/ SD_CLK/AUDATA2)
3	Vo (Adjust 5 V by the voltage resistor VR1 to input)	11	DB4 (PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3)
4	RS (PG23/MOSI1/TIOC0C)	12	DB5 (PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1)
5	R/W# (GND)	13	DB6 (PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP)
6	E (PG24/MISO1/TIOC0D)	14	DB7 (PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD)
7	DB0 (PF1/BREQ#/DV_DATA1/RxD2/ DREQ0/SD_D2/AUDSYNC#)	15	A (Adjust 5 V by the variable resistor VR2 to input)
8	DB1 (PF2/BACK#/DV_DATA2/TxD2/ DACK0/SD_D3/AUDATA0)	16	K (GND)

6.1.3 SD Card Slot (J2)

The M3A-HS64G01 includes an SD card slot (J2). This module cannot be used with the R0K572670C000BR.

The following table shows the pin assignments for J2.

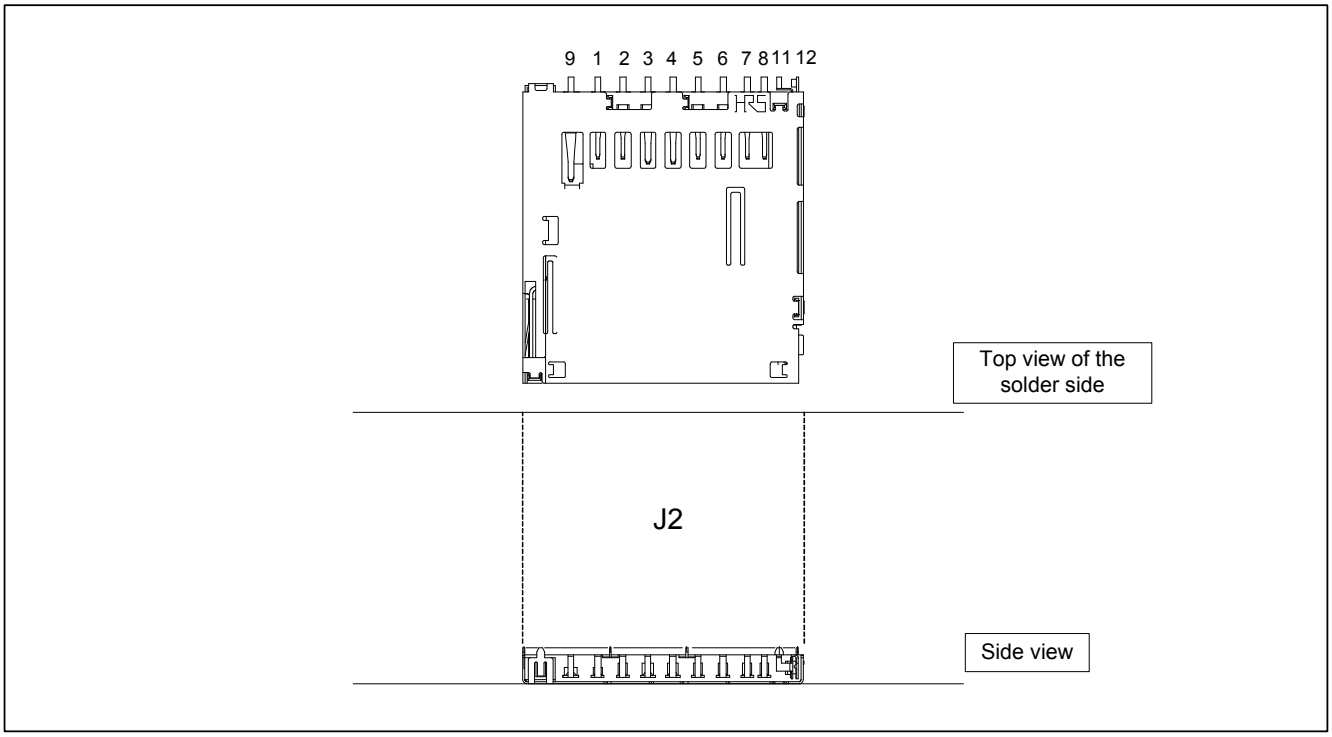


Figure 6.1.5 J2 Pin Assignments

The following table lists the pin descriptions for J2.

Table 6.1.7 J2 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	DAT3 (PK1/PWM1B/SD_D3)	7	DAT0 (PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3)
2	CMD (PF3/ICIORD#/SSISCK1/DV_DATA3/ RxD3/SD_CMD/AUDATA1)	8	DAT1 (PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1PK5/PWM1F/SD_D1)
3	GND	9	DAT2 (PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#)
4	3.3 V	10	WP (PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP)
5	CLK (PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/ TxD3/SD_CLK/AUDATA2)	11	CD (PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD)
6	GND	12	COMMON (GND)

6.1.4 Line-out Pin Jacks (J3, J6, and J8)

The M3A-HS64G01 includes line-out pin jacks (J3, J6, and J8). J8 can only be used with the R0K572670C000BR.

The following figure shows the pin assignments for J3, J6 and J8.

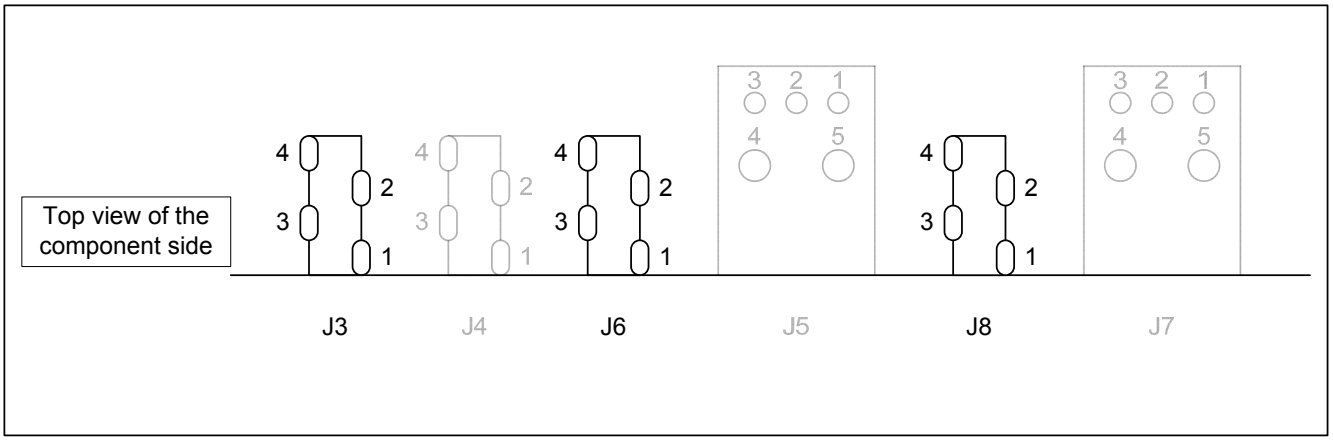


Figure 6.1.6 Line-out Pin Jacks Pin Assignments (J3, J6, and J8)

The following table lists the pin descriptions for J3, J6, and J8.

Table 6.1.8 Line-out Pin Jacks Pin Descriptions (J3, J6, and J8)

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	3	AOUTR (D/A converter analog output R pin)
2	AOUTL (D/A converter analog output L pin)	4	NC

6.1.5 Microphone Input Pin Jack (J4)

The M3A-HS64G01 includes a microphone input pin jack (J4). This module cannot be used with the R0K572670C000BR.

The following figure shows the pin assignments for J4.

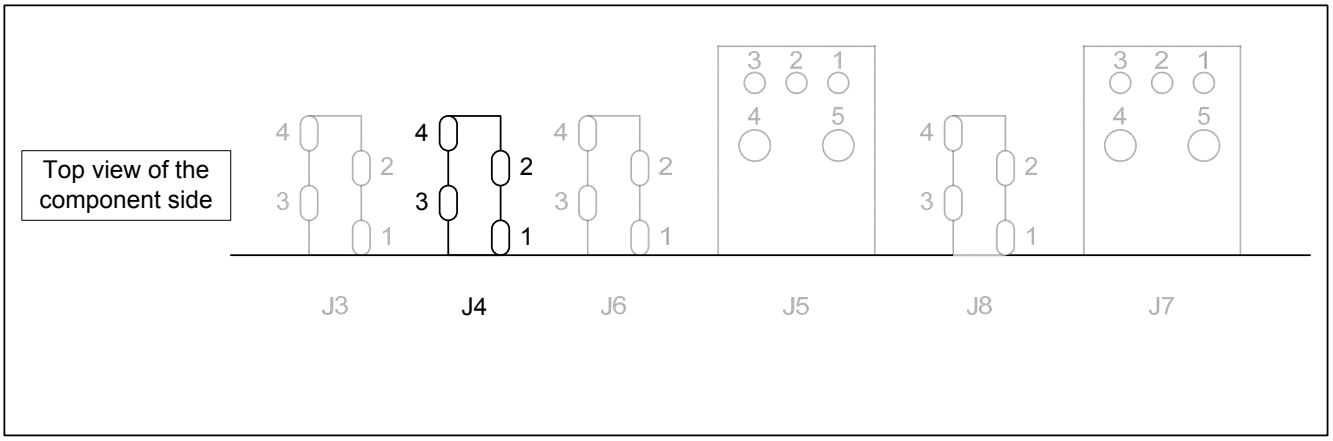


Figure 6.1.7 J4 Pin Assignments

The following table lists the pin descriptions for J4.

Table 6.1.9 J4 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	3	AINR (A/D converter analog input R pin)
2	AINL (A/D converter analog input L pin)	4	NC

6.1.6 Audio Optical Connectors (J5 and J7)

The M3A-HS64G01 includes audio optical connectors (J5 and J7). J7 can only be used with the R0K572670C000BR.

The following figure shows the pin assignments for J5 and J7.

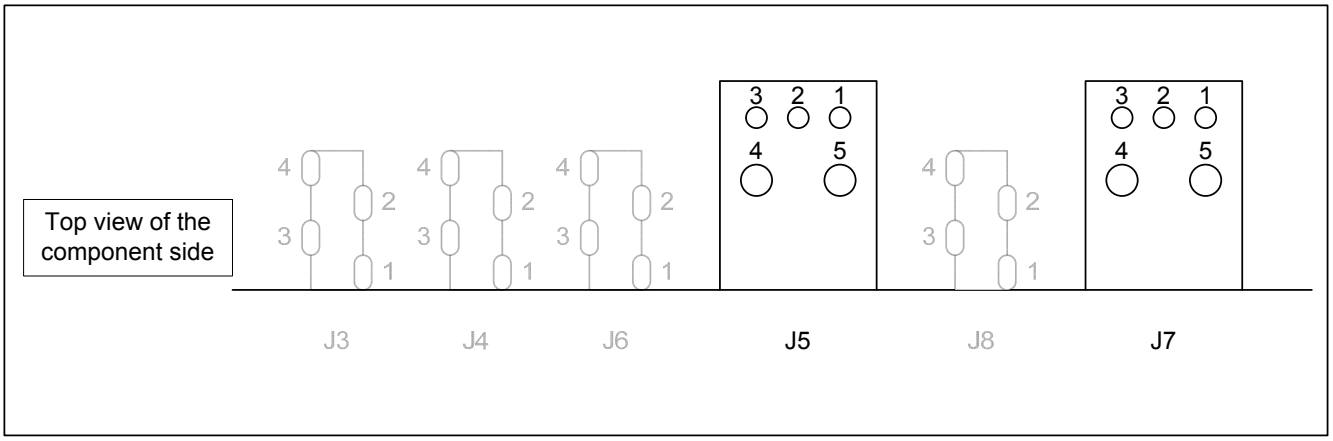


Figure 6.1.8 J5, J7 Pin Assignments

The following table lists the pin descriptions for J5 and J7.

Table 6.1.10 Pin Assignments for Optical Connectors (J5 and J7)

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	4	NC
2	3.3 V	5	NC
3	TX (D/A converter optical output pin)	–	

6.1.7 CD Deck Connector (J9)

The M3A-HS64G01 includes a flexible connector (J9) for connecting a CD deck to the board.

The following figure shows the pin assignments for J9.

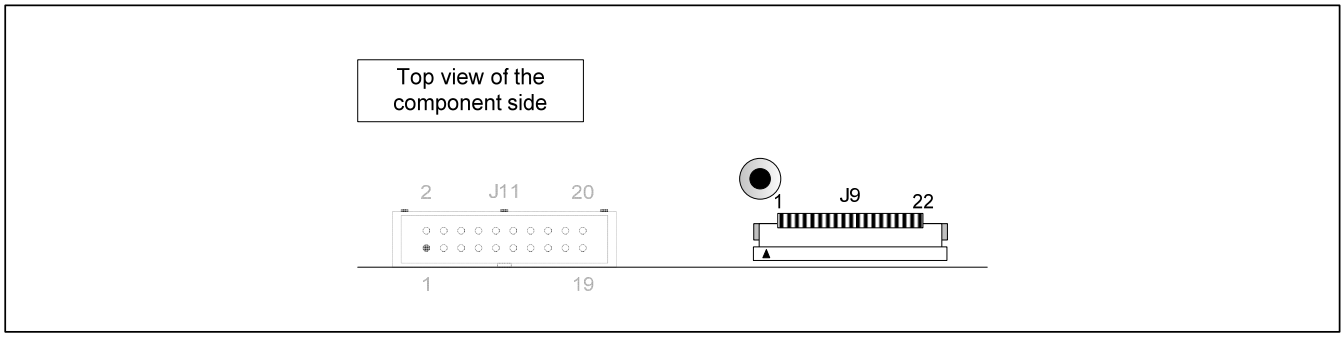


Figure 6.1.9 J9 Pin Assignments

The following table lists the pin descriptions for J9.

Table 6.1.11 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	12	CDFS (PF0/WAIT#/DV_DATA0/SCK2/TEND0/AUDCK)
2	GND	13	CDSI (PF11/A25/SSIDATA3/MOSI0/TIOC3C/SPDIF_IN)
3	8 V	14	CDCK (PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB)
4	8 V	15	CDSO (PF12/BS#/MISO0/TIOC3D/SPDIF_OUT)
5	FLAG6 (PH5/AN5)	16	NC
6	NC	17	IIS_BCK (PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/TCLKB/ SD_D1)
7	CDRST (Connects the reset IC output)	18	IIS_LRCK (PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP)
8	GND	19	IIS_DATA (PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD)
9	3.3 V	20	BLKCK (PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#/ LCD_EXTCLK)
10	3.3 V	21	TRANS (PH4/AN4)
11	GND	22	NC

6.1.8 UART Connector (J10)

The M3A-HS64G01 includes a UART connector (J10) with TTL-level flow control. This module cannot be used with the R0K572670C000BR.

The following figure shows the pin assignments for J10.

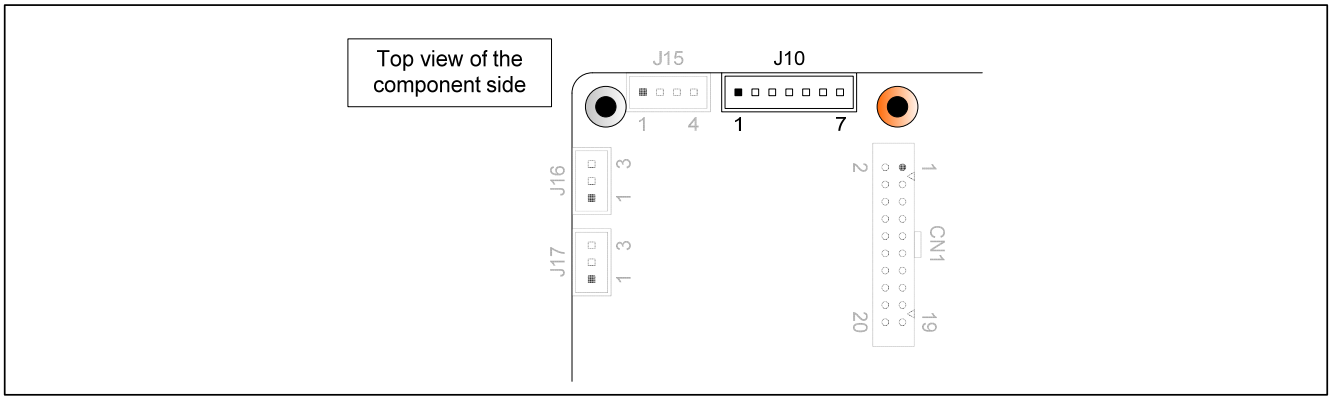


Figure 6.1.10 J10 Pin Assignments

The following table lists the pin descriptions for J10.

Table 6.1.12 J10 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	5	CTS# (Not connected with the R0K572670C000BR)
2	RXD (Not connected with the R0K572670C000BR)	6	RTS# (Not connected with the R0K572670C000BR)
3	TXD (Not connected with the R0K572670C000BR)	7	GND
4	SCK (Not connected with the R0K572670C000BR)	–	

6.1.9 External IIC Connector (J11)

The M3A-HS64G01 includes a MIL-spec connector (J11) for connecting an external IIC interface to the board.

The following figure shows the pin assignments for J11.

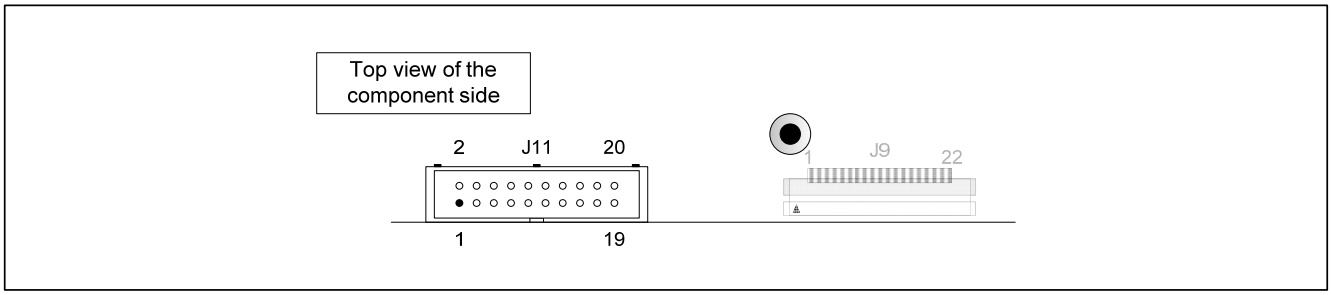


Figure 6.1.11 J11 Pin Assignments

Table 6.1.13 Pin Assignments for External IIC Connector (J11)

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	11	
2	3.3 V	12	
3		13	
4		14	
5		15	
6	GND (1)	16	
7		17	SCL (PE4/SCL2/DV_VSYNC)
8		18	SDA (PE5/SDA2/DV_HSYNC)
9		19	
10	GND (1)	20	GND (1)

Note 1: For compatibility with other CPU boards, this connector is connected with the board via a 0 Ω resistor.

6.1.10 LCD Module Connectors (J12 to J14)

The M3A-HS64G01 includes two flexible connectors (J12 and J13) and one MIL-spec connector (J14) for connecting an LCD module to the board.

The following figure shows the pin assignments for LCD module connectors.

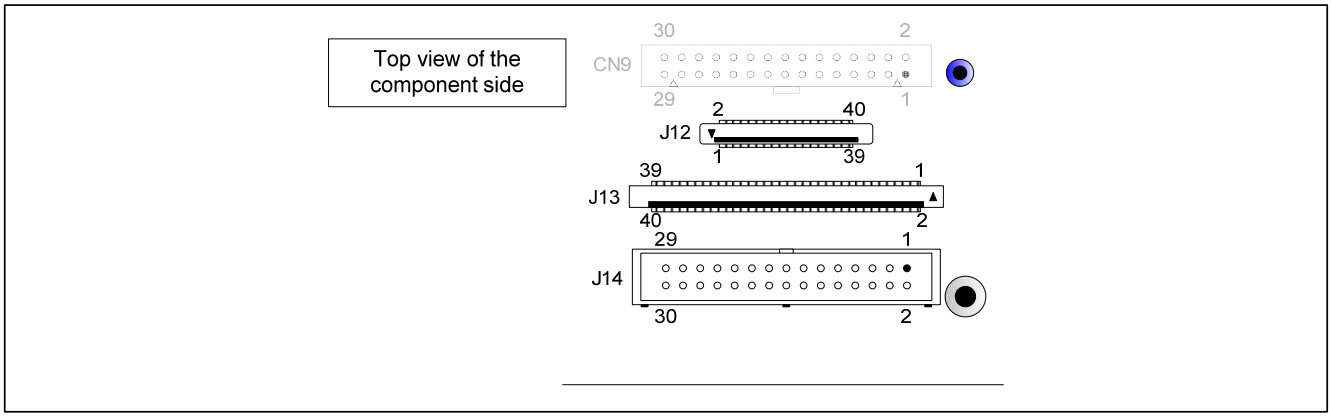


Figure 6.1.12 LCD Module Connectors Pin Assignments (J12 to J14)

The following table lists the pin descriptions for J12.

Table 6.1.14 J12 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	21	G4 (PG9/LCD_DATA9/SSIWS0/TxD4/ SIOFSYNC)
2	3.3 V	22	G3 (PG8/LCD_DATA8/SSITxD0/RxD4/SIOFSCK)
3	3.3 V	23	GND
4	DCLK (PG19/LCD_CLK/TIOC2B/TxD3/CTS1)	24	G2 (PG7/LCD_DATA7/SD_CD/PINT7/IRQ7)
5	GND	25	G1 (PG6/LCD_DATA6/SD_WP/PINT6/IRQ6)
6	HSYNC (PG17/LCD_HSYNC/TIOC1B/TxD1)	26	G0 (PG5/LCD_DATA5/SD_D1/PINT5/IRQ5)
7	GND	27	GND
8	DTMG (PG18/LCD_DE/TIOC2A/RxD3/RTS1)	28	B5 (PG4/LCD_DATA4/SD_D0/PINT4/IRQ4)
9	GND	29	B4 (PG3/LCD_DATA3/SD_CLK/PINT3)
10	NC	30	B3 (PG2/LCD_DATA2/SD_CMD/PINT2)
11	GND	31	GND
12	R5 (PG15/LCD_DATA15/TIOC0D/TxD7)	32	B2 (PG1/LCD_DATA1/SD_D3/PINT1)
13	R4 (PG14/LCD_DATA14/TIOC0C/RxD7)	33	B1 (PG0/LCD_DATA0/SD_D2/PINT0)
14	R3 (PG13/LCD_DATA13/TIOC0B/TxD6)	34	B0 (PG0/LCD_DATA0/SD_D2/PINT0)
15	GND	35	PCI (NC)
16	R2 (PG12/LCD_DATA12/TIOC0A/RxD6)	36	Vctrl (3.3 V)
17	R1(PG11/LCD_DATA11/SSIWS0/IRQ3/ TxD5/SIOFTxD)	37	NC
18	R0 (PG11/LCD_DATA11/SSIWS0/IRQ3/ TxD5/SIOFTxD)	38	NC
19	GND	39	NC
20	G5 (PG10/LCD_DATA10/SSISCK0/IRQ2/ RxD5/SIOFRxD)	40	NC

The following table lists the pin descriptions for J13.

Table 6.1.15 J13 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC	21	R3 (PG13/LCD_DATA13/TIOC0B/TxD6)
2	DTMG (PG18/LCD_DE/TIOC2A/RxD3/RTS1)	22	R2 (PG12/LCD_DATA12/TIOC0A/RxD6)
3	HREV (3.3 V)	23	R1 (PG11/LCD_DATA11/SSIWS0/IRQ3/ TxD5/SIOFTxD)
4	B5 (PG4/LCD_DATA4/SD_D0/PINT4/IRQ4)	24	R0 (PG11/LCD_DATA11/SSIWS0/IRQ3/TxD5/ SIOFTxD)
5	B4 (PG3/LCD_DATA3/SD_CLK/PINT3)	25	VREV (3.3 V)
6	B3 (PG2/LCD_DATA2/SD_CMD/PINT2)	26	NC
7	B2 (PG1/LCD_DATA1/SD_D3/PINT1)	27	NC
8	B1 (PG0/LCD_DATA0/SD_D2/PINT0)	28	GND
9	B0 (PG0/LCD_DATA0/SD_D2/PINT0)	29	DCLK (PG19/LCD_CLK/TIOC2B/TxD3/CTS1)
10	3.3 V	30	GND
11	3.3 V	31	GND
12	G5 (PG10/LCD_DATA10/SSISCK0/IRQ2/ RxD5/SIOFRxD)	32	GND
13	G4 (PG9/LCD_DATA9/SSIRxD0/TxD4/ SIOFSYNC)	33	GND
14	G3 (PG8/LCD_DATA8/SSITxD0/RxD4/ SIOFSCK)	34	GND
15	G2 (PG7/LCD_DATA7/SD_CD/PINT7/IRQ7)	35	TMZ (Not connected with the R0K572670C000BR)
16	G1 (PG6/LCD_DATA6/SD_WP/PINT6/IRQ6)	36	GND
17	G0 (PG5/LCD_DATA5/SD_D1/PINT5)	37	DIM (3.3 V)
18	GND	38	NC
19	R5 (PG15/LCD_DATA15/TIOC0D/TxD7)	39	5 V
20	R4 (PG14/LCD_DATA14/TIOC0C/RxD7)	40	5 V

The following table lists the pin descriptions for J14.

Table 6.1.16 J14 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	16	PG3/LCD_DATA3/SD_CLK/PINT3
2	3.3 V	17	PG2/LCD_DATA2/SD_CMD/PINT2
3	3.3 V	18	PG1/LCD_DATA1/SD_D3/PINT1
4	PG15/LCD_DATA15/TIOC0D/TxD7	19	PG0/LCD_DATA0/SD_D2/PINT0
5	PG14/LCD_DATA14/TIOC0C/RxD7	20	GND
6	PG13/LCD_DATA13/TIOC0B/TxD6	21	PG19/LCD_CLK/TIOC2B/TxD3/CTS1
7	PG12/LCD_DATA12/TIOC0A/RxD6	22	PG17/LCD_HSYNC/TIOC1B/TxD1
8	PG11/LCD_DATA11/SSIWS0/IRQ3/TxD5/ SIOFTxD	23	NC（LCD_VCPWC）
9	PG10/LCD_DATA10/SSISCK0/IRQ2/ RxD5/SIOFRxD	24	NC (Allowed to supply 5 V through 0-Ω resistor)
10	PG9/LCD_DATA9/SSIRxD0/TxD4/ SIOFSYNC	25	PG16/LCD_VSYNC/TIOC1A/RxD1
11	PG8/LCD_DATA8/SSISCK0/RxD4/ SIOFSCK	26	PG18/LCD_DE/TIOC2A/RxD3/RTS1
12	PG7/LCD_DATA7/SD_CD/PINT7/IRQ7	27	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/ LCD_M_DISP
13	PG6/LCD_DATA6/SD_WP/PINT6/IRQ6	28	GND
14	PG5/LCD_DATA5/SD_D1/PINT5/IRQ5	29	GND
15	PG4/LCD_DATA4/SD_D0/PINT4/IRQ4	30	GND

6.1.11 IEBus™ Connector (J15)

The M3A-HS64G01 includes an IEBus™ connector (J15).

The following figure shows the pin assignments for J15.

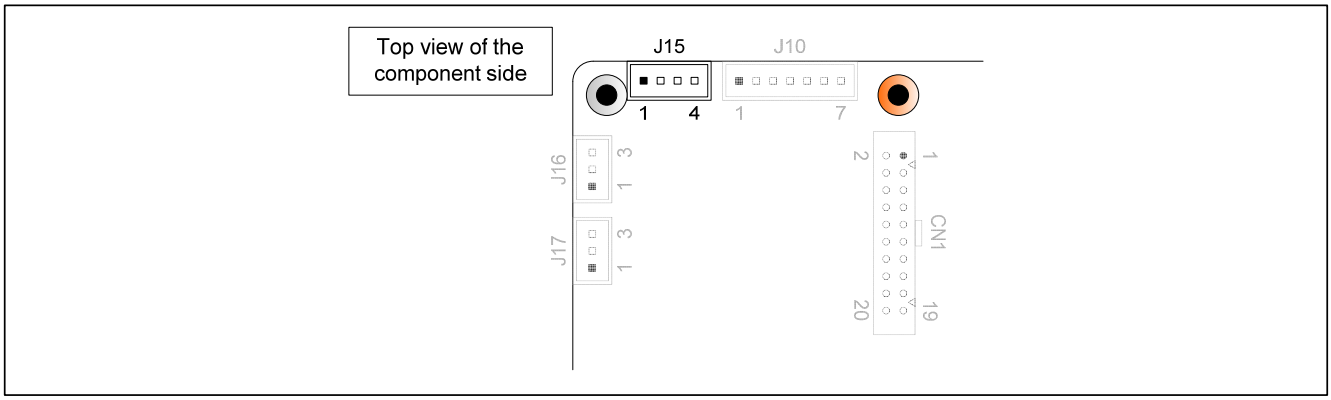


Figure 6.1.13 J15 Pin Assignments

The following table lists the pin descriptions for J15.

Table 6.1.17 J15 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	3	BUS+
2	BUS−	4	GND

6.1.12 CAN Connectors (J16 and J17)

The M3A-HS64G01 includes CAN connectors (J16 and J17).

The following figure shows the pin assignments for J16 and J17.

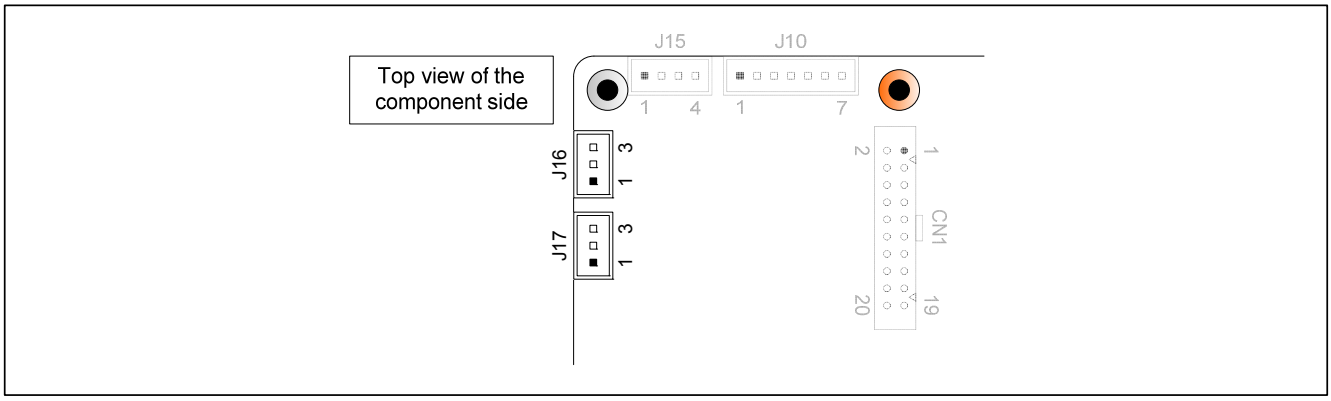


Figure 6.1.14 J16, J17 Pin Assignments

The following table lists the pin descriptions for J16 and J17.

Table 6.1.18 J16, J17 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	CANH	3	GND
2	CANL	–	

J16 and J17 are connected to channel 0 (CTx0/CRx0) and channel 1 (CTx1/CRx1), respectively.

6.1.13 12 V Power Supply Connector (J18)

The M3A-HS64G01 includes a system power supply connector (J18). The number of pins of this connector differs from the power supply connector mounted on the R0K572670C000BR to prevent improper insertion.

The following figure shows the pin assignments for J18.

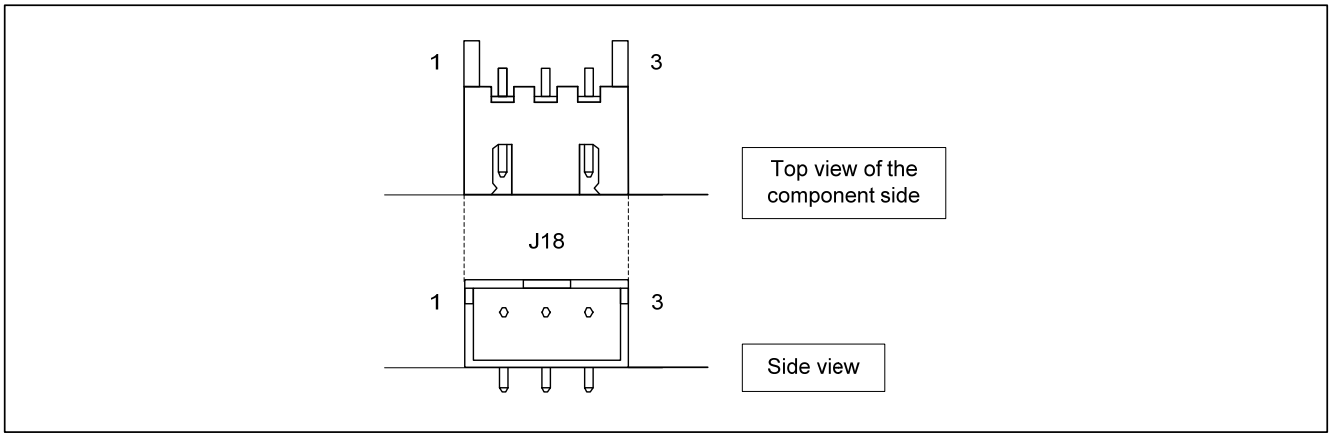


Figure 6.1.15 J18 Pin Assignments

The following table lists the pin descriptions for J18.

Table 6.1.19 J18 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	12 V	3	GND
2	NC	–	

6.1.14 12 V Input AC Adapter Jack (J19)

The M3A-HS64G01 includes an AC adapter jack (J19) for 12 V DC input.

The following figure shows the pin assignments for J19.

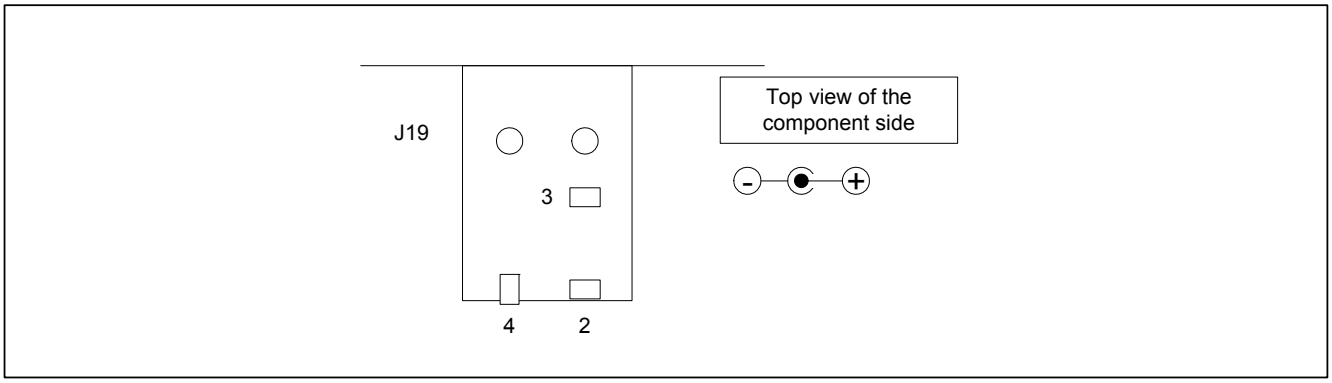


Figure 6.1.16 J19 Pin Assignments

The following table lists the pin descriptions for J19.

Table 6.1.20 J19 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC (No pins)	3	GND
2	12 V	4	GND

6.2 M3A-HS64G01 Operating Components

The following figure shows the assignments of the M3A-HS64G01 operating components.

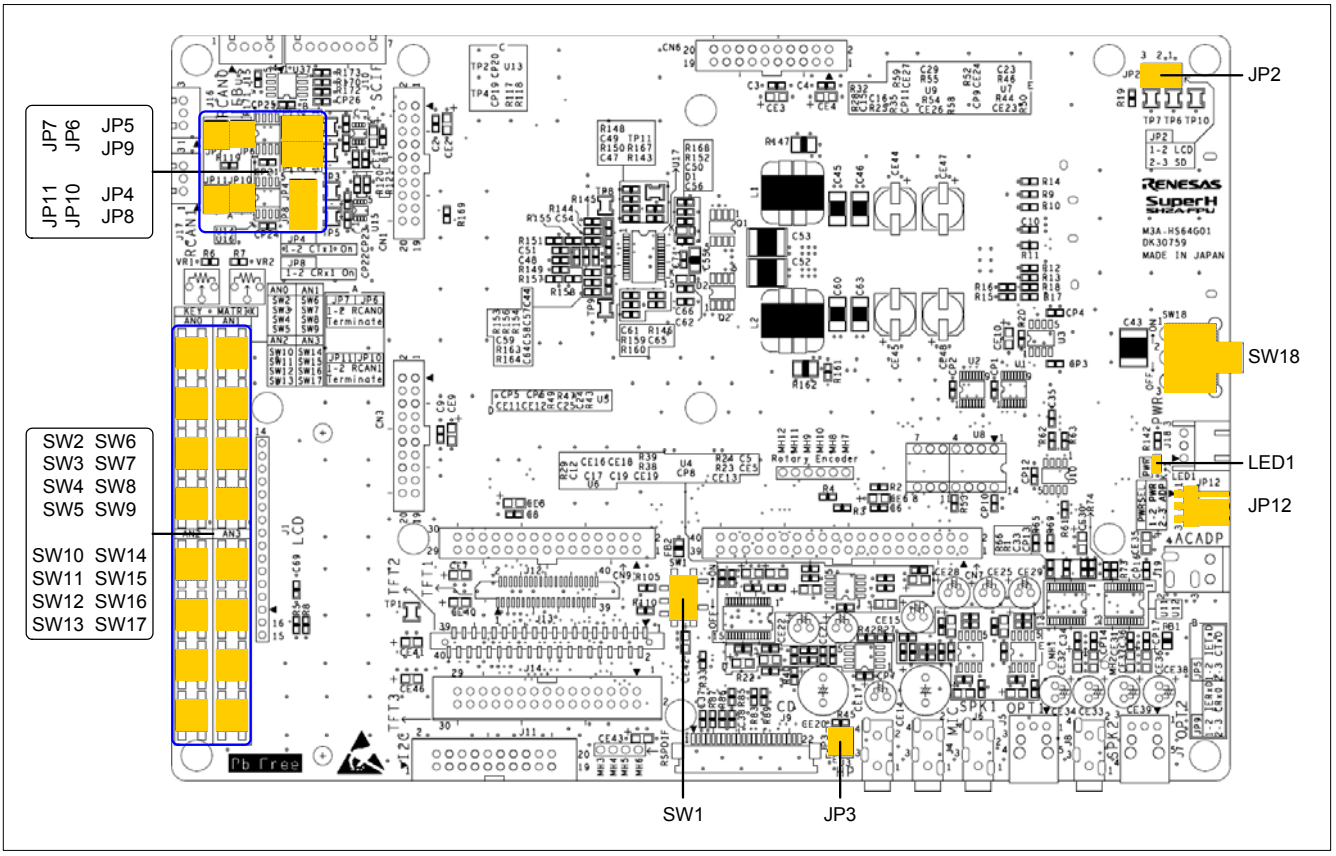


Figure 6.2.1 M3A-HS64G01 Operating Component Assignments (Top View of the Component Side)

6.2.1 Jumpers (JP2 to JP12)

The M3A-HS64G01 includes 11 jumpers.

The following figure shows jumper assignments (JP2 to JP12) on the M3A-HS64G01.

Figure 6.2.2 M3A-HS64G01 Jumper Assignments (JP2 to JP12)

The following table lists the jumpers setting for JP2, JP5, and JP9.

Table 6.2.1 Multiplexed Pin Switch Jumpers Setting (JP2, JP5, and JP9)

Number	Setting	Description
JP2	1 - 2	Connects the character LCD connector (J1) as the LCD data output pin (1)
LCD/SD	2 - 3	Connects the SD card slot (J1) as the SDHI I/O pin
JP5	1 - 2	Connects the IEBus™ driver (U37) as the IETxD output pin
IETxD/CTx0	2 - 3	Connects the CAN driver (U14) as the CTx0 output pin (1)
JP9	1 - 2	Connects the IEBus™ driver (U37) as the IERxD input pin
IERxD/CRx0	2 - 3	Connects the CAN driver (U14) as the CRx0 input pin (1)

Notes:

1. Default setting

2. Do not change the jumper settings while the M3A-HS64G01 is ON. Be sure to turn the power OFF before changing the settings.

The following table lists the jumpers setting for JP3.

Table 6.2.2 Plug-in Power Microphone Jumper Setting (JP3)

Number	Setting	Description
JP3	1 - 2	Supplies the power (Plug-in power microphone)
	Open	Does not supply the power (Typical microphone) (1)

Note 1: Default setting

The following table lists the jumpers setting for JP4, JP6, JP7, JP8, JP10, and JP11.

Table 6.2.3 CAN Evaluation Jumpers Setting (JP4, JP6, JP7, JP8, JP10, and JP11)

Number	Setting	Description
JP4 Connects CTx1	1 - 2	Connects the CTx1 pin to the CAN driver (U16) (1)
	Open	Leaves the CTx1 pin disconnected to the CAN driver (U16)
JP8 Connects CRx1	1 - 2	Connects the CRx1 pin to the CAN driver (U16) (1)
	Open	Leaves the CRx1 pin disconnected to the CAN driver (U16)
JP6 Terminates CANL (ch0)	1 - 2	Terminates the CANL (ch0) pin
	Open	Leaves the CANL (ch0) pin not terminated (1)
JP7 Terminates CANH (ch0)	1 - 2	Terminates the CANH (ch0) pin
	Open	Leaves the CANH (ch0) pin not terminated (1)
JP10 Terminates CANL (ch1)	1 - 2	Terminates the CANL (ch1) pin
	Open	Leaves the CANL (ch1) pin not terminated
JP11 Terminates CANH (ch1)	1 - 2	Terminates the CANH (ch1) pin
	Open	Leaves the CANH (ch1) pin not terminated (1)

Note 1: Default setting

The following table lists the jumpers setting for JP12.

Table 6.2.4 Power Supply Switch Jumper Setting (JP12)

Number	Setting	Description
JP12 PWRSEL	1 - 2	Supplies the system power from J18
	2 - 3	Supplies the system power from J19 (AC adapter is used) (1)

Notes:

1. Default setting
2. Do not change the jumper settings while the M3A-HS64G01 is ON. Be sure to turn the power OFF before changing the settings.

6.2.2 Switches and LED

The M3A-HS64G01 includes 18 switches and one LED.

The following figure shows assignments for switches and the LED.

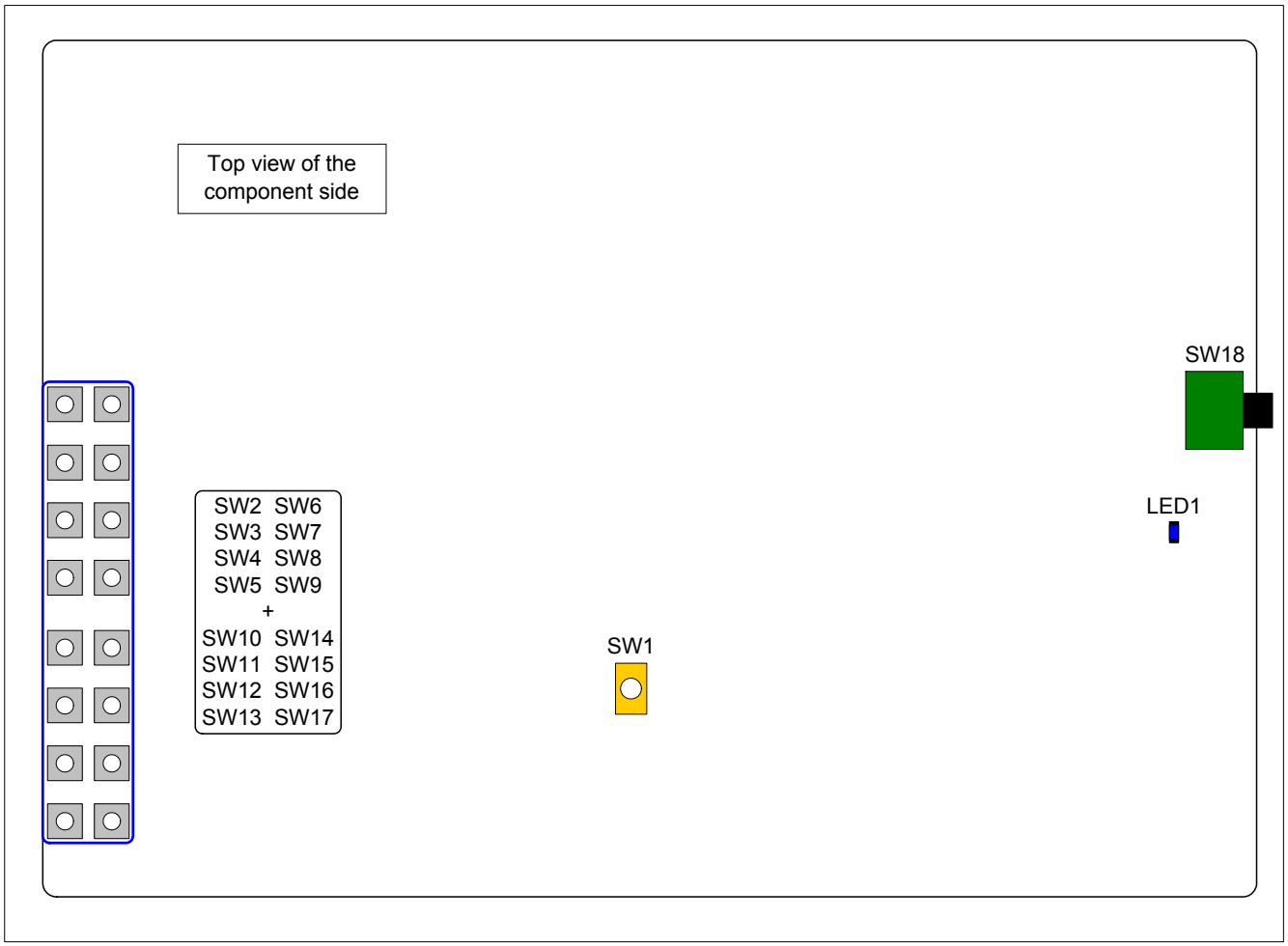


Figure 6.2.3 M3A-HS64G01 Switches and LED Assignments

The following table lists the switches mounted on the board.

Table 6.2.5 Switches

Number	Name	Remarks
SW1	LCD module connector (J12) power supply switch	Optional
SW2 to SW17	Key input switches	Refer to Section 3.10 for details
SW18	Power supply switch	-

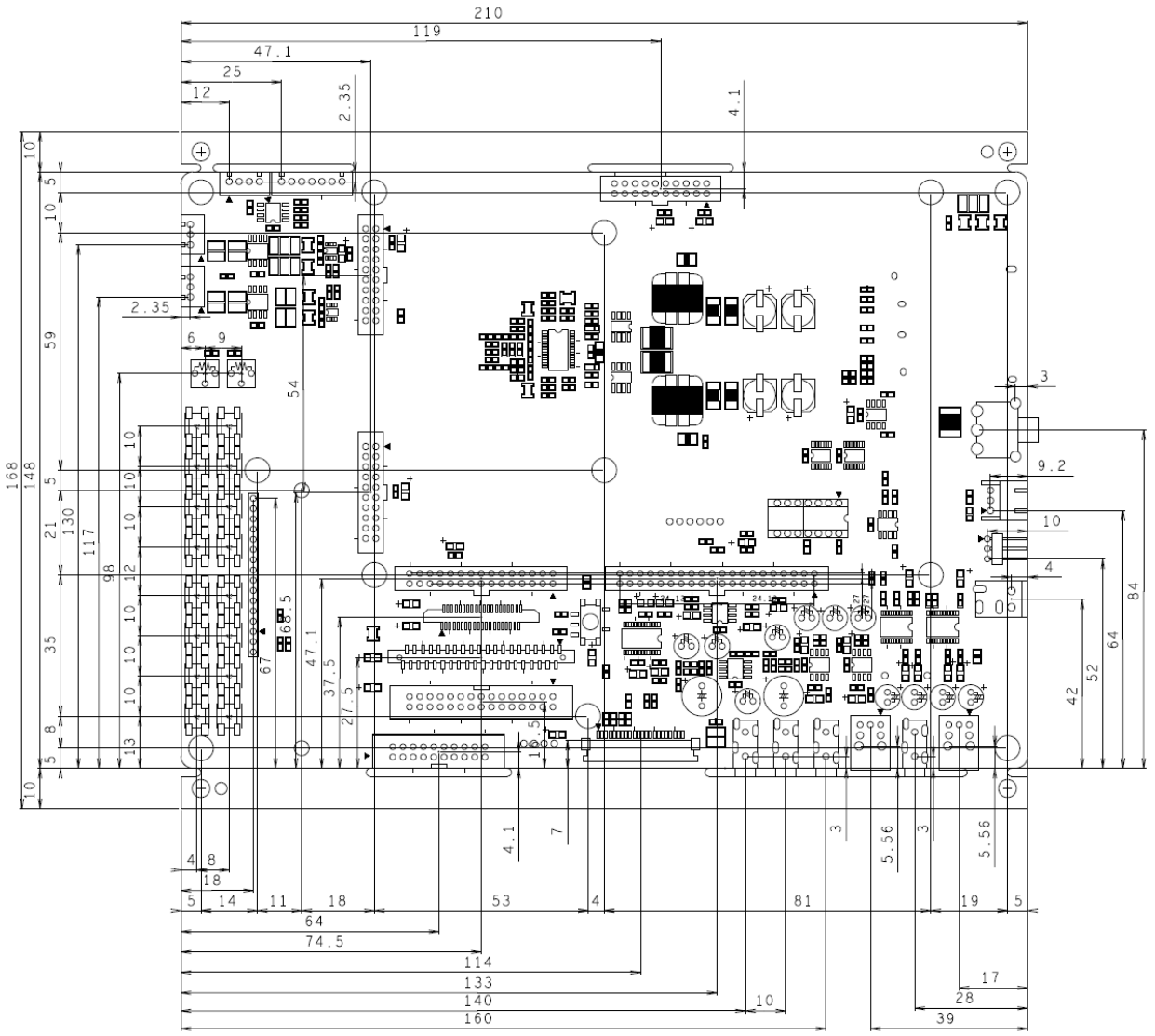
The following table lists the LED mounted on the board.

Table 6.2.6 LED

Number	Color	Description
LED1	Blue	Power supply LED (LED1 is illuminated when 12 V power is supplied)

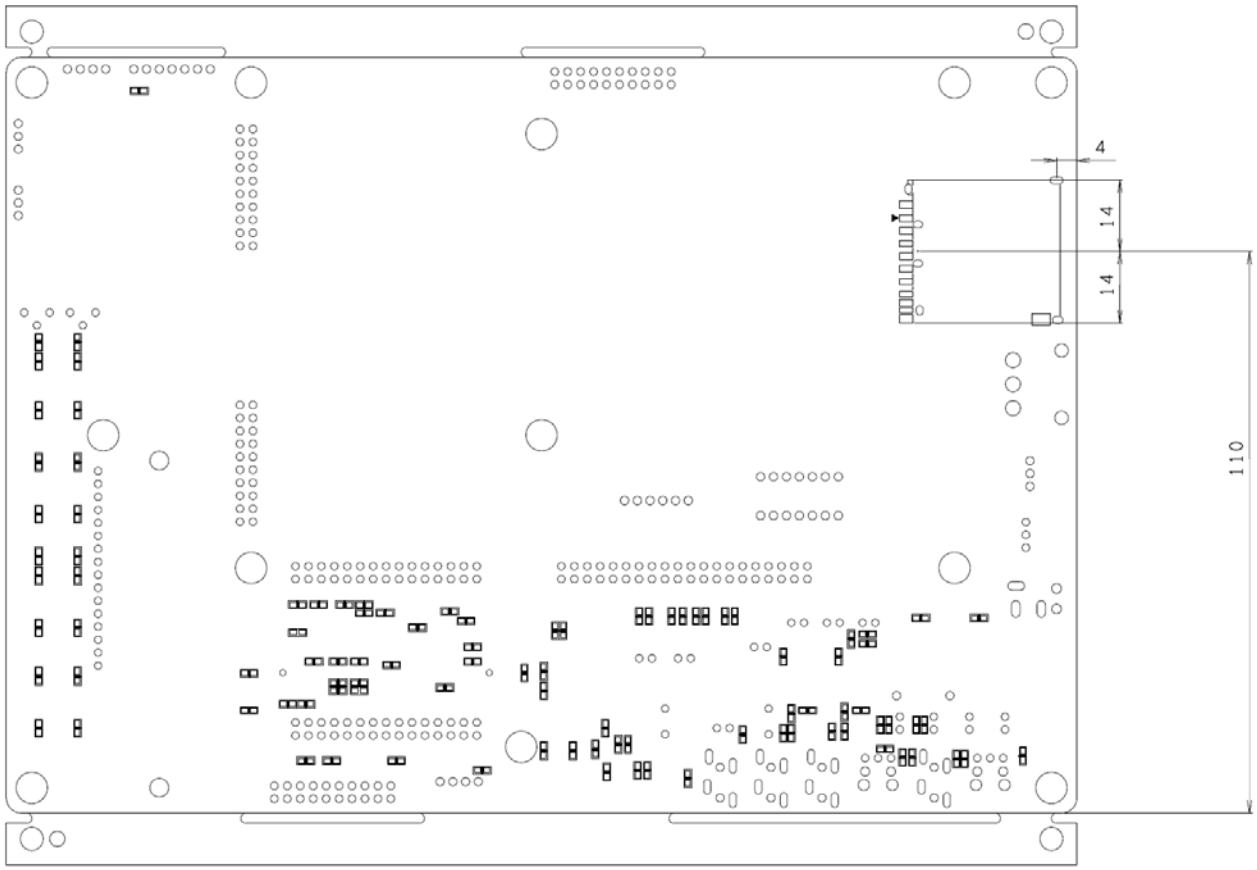
6.3 M3A-HS64G01 Dimensions

Figure 6.3.1 and Figure 6.3.2 show the M3A-HS64G01 dimensions.



Note: All measurements are in millimeters.

Figure 6.3.1 M3A-HS64G01 Dimensions (Top View of the Component Side)



Note: All measurements are in millimeters.

Figure 6.3.2 M3A-HS64G01 Dimensions (Transparent View of the Component Side)

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Chapter 7
M3A-HS64G02 Operating Specifications

7.1 M3A-HS64G02 Connectors

Figure 7.1.1 and Figure 7.1.2 show the M3A-HS64G02 connector assignments.

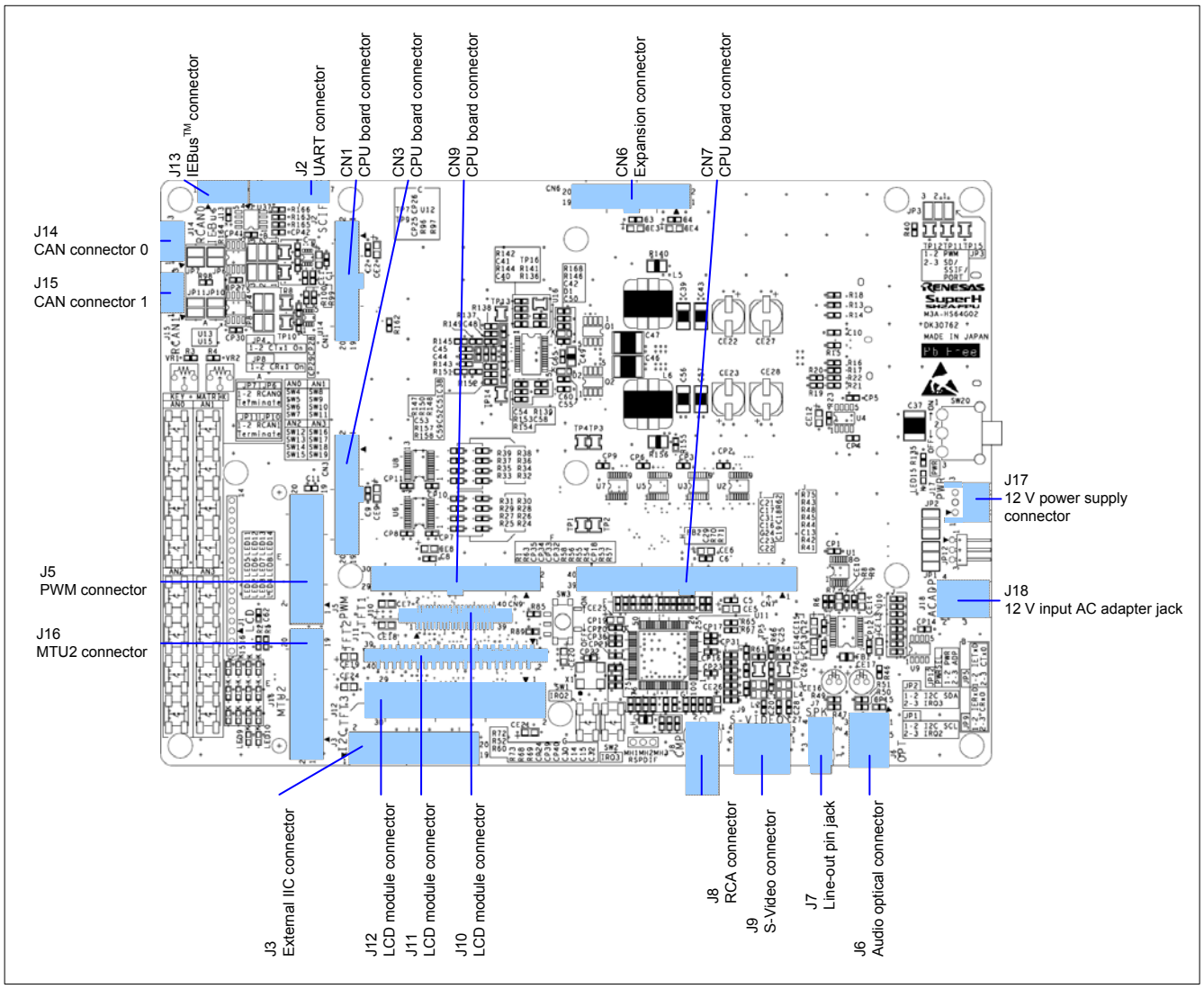


Figure 7.1.1 M3A-HS64G02 Connectors (Top View of the Component Side)

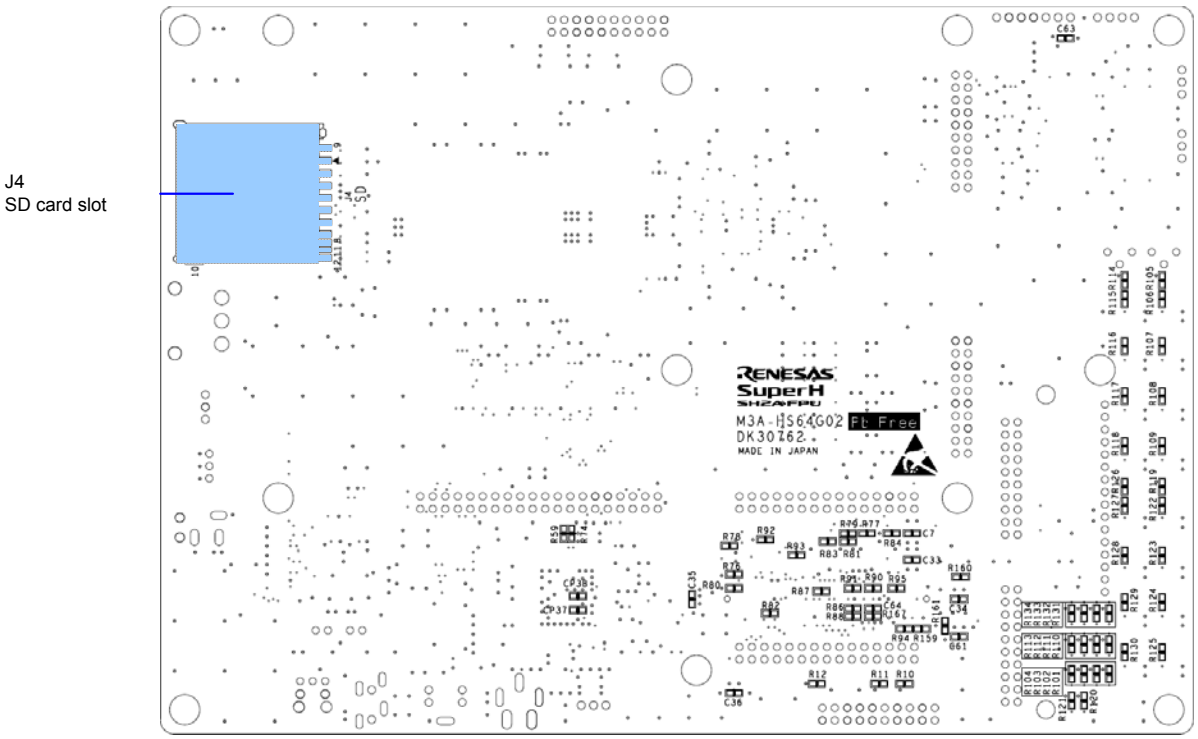


Figure 7.1.2 M3A-HS64G02 Connectors (Top View of the Solder Side)

7.1.1 CPU Board Connectors (CN1, CN3, CN6, CN7 and CN9)

The M3A-HS64G02 includes five MIL-spec connectors (CN1, CN3, CN6, CN7, and CN9) for connecting this optional board to the R0K572670C000BR. The following figure shows the pin assignments for the CPU board connectors. Table 7.1.1 to Table 7.1.5 lists the pin descriptions for the CPU board connectors.

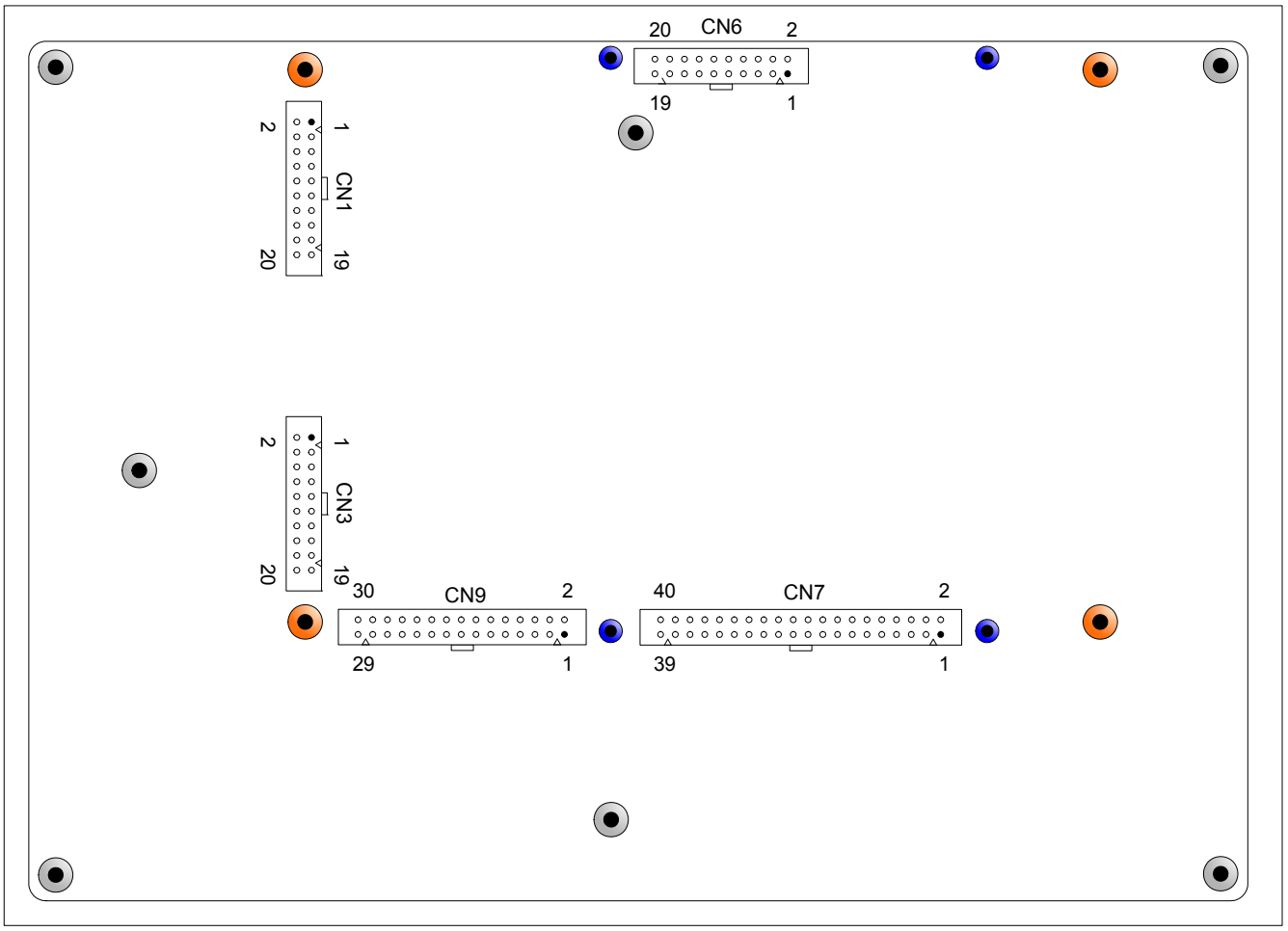


Figure 7.1.3 CPU Board Connectors Pin assignments (CN1, CN3, CN6, CN7, and CN9)

Table 7.1.1 CN1 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	Not connected with the R0K572670C000BR (NC)	11	GND
2	PH4/AN4	12	Not connected with the R0K572670C000BR (NC)
3	5 V	13	Not connected with the R0K572670C000BR (NC)
4	PH5/AN5	14	Not connected with the R0K572670C000BR (NC)
5	Not connected with the R0K572670C000BR (NC)	15	Not connected with the R0K572670C000BR (NC)
6	3.3 V	16	GND
7	Not connected with the R0K572670C000BR (NC)	17	PJ3/CRx1/CRx0&CRx1/IRQ1/AUDIO_XOUT/ WDTOVF#
8	PA2/MD_BOOT1 (NC)	18	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/ LCD_M_DISP
9	PA1/MD_BOOT0 (NC)	19	PJ1/CRx0/IERxD/IRQ0/RxD0
10	PA0/MD_CLK1 (NC)	20	PJ0/CTx0/IETxD/CS1#/TxD0/A0

Table 7.1.2 CN3 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	AVref (NC)	11	Not connected with the R0K572670C000BR (NC)
2	AVref (NC)	12	Not connected with the R0K572670C000BR (NC)
3	PH1/AN1	13	AVcc
4	PH0/AN0	14	AVcc
5	AVref (NC)	15	Not connected with the R0K572670C000BR (NC)
6	AVref (NC)	16	Not connected with the R0K572670C000BR (NC)
7	PH3/AN3	17	AVss
8	PH2/AN2	18	AVss
9	AVcc	19	AVss
10	AVcc	20	AVss

Table 7.1.3 CN6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	11	3.3 V
2	5 V	12	PG23/MOSI1/TIOC0C
3	5 V	13	PG24/MISO1/TIOC0D
4	5 V	14	PC5/RAS#/TIOC4A/IRQ4
5	PC0/CS0#/SSIWS0 (NC)	15	PC6/CAS#/TIOC4B/IRQ5
6	PC1/RD#/SSISCK0 (NC)	16	PC7/CKE/TIOC4C/IRQ6
7	PC2/RD/WR#/SSIRxD0 (NC)	17	PC8/CS3#/TIOC4D/IRQ6
8	PC3/WE0#/DQML/SSITxD0 (NC)	18	GND
9	PC4/WE1#/DQMU/WE# (NC)	19	GND
10	3.3 V	20	CKIO (NC)

Table 7.1.4 CN7 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PF2/BACK#/DV_DATA2/TxD2/DACK0/ SD_D3/AUDATA0	21	GND
2	PK0/PWM1A/SD_D2	22	PF3/ICIORD#/SSISCK1/DV_DATA3/RxD3/ SD_CMD/AUDATA1
3	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/ TxD3/SD_CLK/AUDATA2	23	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3
4	PK2/PWM1C/SD_CMD	24	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/ TxD3/SD_CLK/AUDATA2
5	PE0/SCL0/AUDIO_CLK/IRQ0	25	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1
6	RES#	26	GND
7	PE2/SCL1/IRQ2	27	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD
8	PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#/ LCD_EXTCLK	28	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP
9	PE4/SCL2/DV_VSYNC	29	GND
10	PE3/SDA1/IRQ3	30	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB (NC)
11	3.3 V	31	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN
12	PE5/SDA2/DV_HSYNC	32	PF0/WAIT#/DV_DATA0/SCK2/TEND0/AUDCK (NC)
13	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1	33	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
14	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3	34	GND
15	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD	35	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
16	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP	36	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB
17	PF0/WAIT#/DV_DATA0/SCK2/TEND0/ AUDCK	37	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN
18	5 V	38	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
19	PF2/BACK#/DV_DATA2/TxD2/DACK0/ SD_D3/AUDATA0	39	GND
20	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#	40	AUDIO_XTAL

Table 7.1.5 CN9 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PG1/LCD_DATA1/SD_D3/PINT1	16	PG12/LCD_DATA12/TIOC0A/RxD6
2	PG0/LCD_DATA0/SD_D2/PINT0	17	PG14/LCD_DATA14/TIOC0C/RxD7
3	PG3/LCD_DATA3/SD_CLK/PINT3	18	PG13/LCD_DATA13/TIOC0B/TxD6
4	PG2/LCD_DATA2/SD_CMD/PINT2	19	PG16/LCD_VSYNC/TIOC1A/RxD1
5	GND	20	PG15/LCD_DATA15/TIOC0D/TxD7
6	PG4/LCD_DATA4/SD_D0/PINT4/IRQ4	21	PG17/LCD_HSYNC/TIOC1B/TxD1
7	PG6/LCD_DATA6/SD_WP/PINT6/IRQ6	22	5 V
8	PG5/LCD_DATA5/SD_D1/PINT5/IRQ5	23	PG19/LCD_CLK/TIOC2B/TxD3/CTS1
9	PG7/LCD_DATA7/SD_CD/PINT7/IRQ7	24	PG18/LCD_DE/TIOC2A/RxD3/RTS1
10	GND	25	3.3 V
11	PG9/LCD_DATA9/SSIRxD0/TxD4/ SIOFSYNC	26	PG20/LCD_EXTCLK/SCK1 (NC)
12	PG8/LCD_DATA8/SSITxD0/RxD4/ SIOFSCK	27	PG22/SSL10/TIOC0B
13	PG11/LCD_DATA11/SSIWS0/IRQ3/ TxD5/SIOFTxD	28	PG21/RSPCK1/TIOC0A
14	PG10/LCD_DATA10/SSISCK0/IRQ2/ RxD5/SIOFRxD	29	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#
15	GND	30	Not connected with the R0K572670C000BR (NC)

7.1.2 UART Connector (J2)

The M3A-HS64G02 includes a UART connector (J2) with TTL-level flow control. This module cannot be used with the R0K572670C000BR.

The following figure shows the pin assignments for J2.

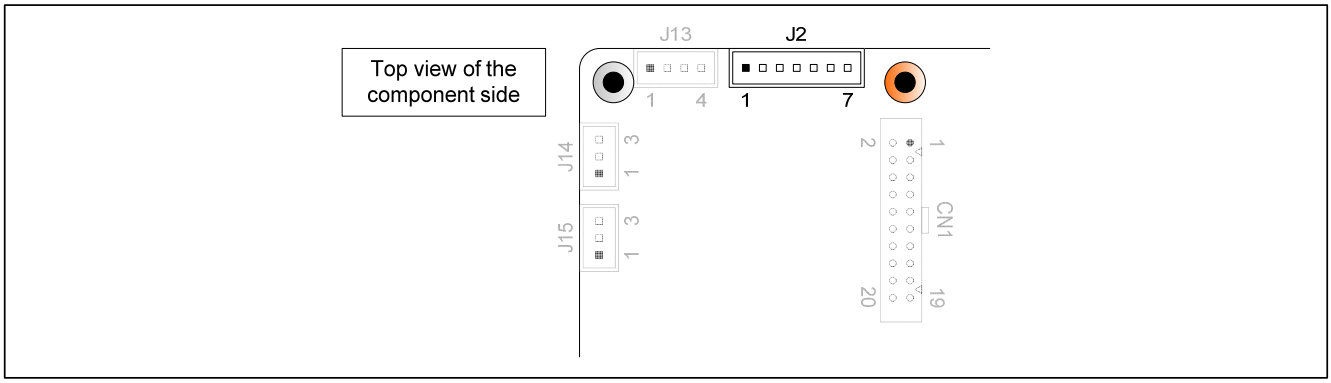


Figure 7.1.4 J2 Pin Assignments

The following table lists the pin descriptions for J2.

Table 7.1.6 J2 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	5	NC
2	RXD (Not connected with the R0K572670C000BR)	6	NC
3	TXD (Not connected with the R0K572670C000BR)	7	GND
4	NC	–	

7.1.3 External IIC Connector (J3)

The M3A-HS64G01 includes a MIL-spec connector (J3) for connecting an external IIC interface to this optional board.

The following figure shows the pin assignments for J3.

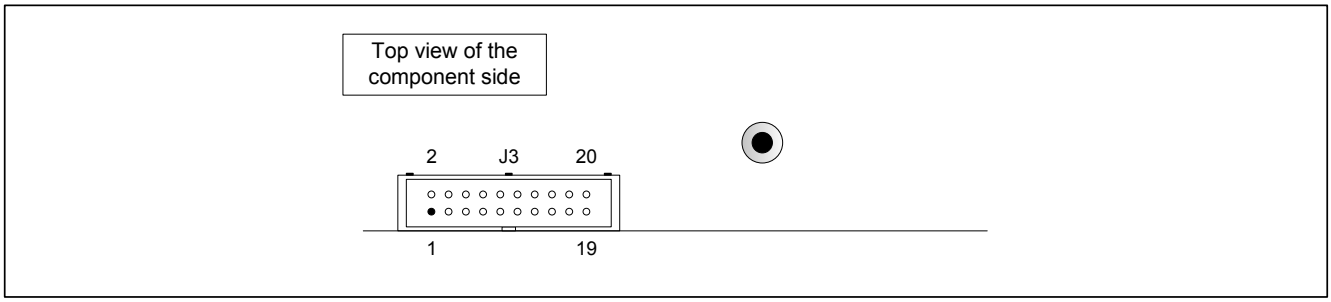


Figure 7.1.5 J3 Pin Assignments

The following table lists the pin descriptions for J3.

Table 7.1.7 J3 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	11	
2	3.3 V	12	
3		13	
4		14	
5		15	
6	GND (1)	16	
7		17	SCL (PE0/SCL0/AUDIO_CLK/IRQ0)
8		18	SDA (PE1/SDA0/IOIS16#/IRQ1/TCLKA/ADTRG#)
9		19	
10	GND (1)	20	GND (1)

Note: For compatibility with other CPU boards, this connector is connected with the board via a 0 Ω resistor.

7.1.4 SD Card Slot (J4)

The M3A-HS64G02 includes an SD card slot (J4).

The following figure shows the pin assignments for J4.

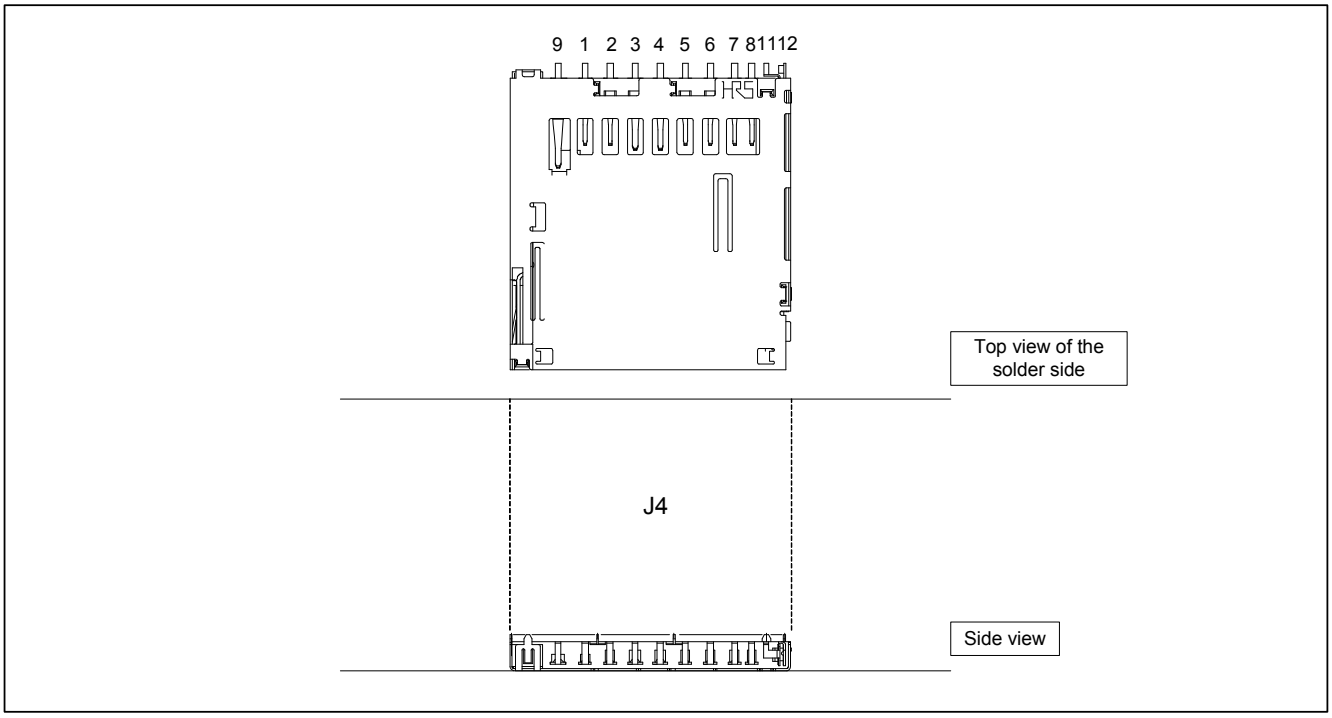


Figure 7.1.6 J4 Pin Assignments

The following table lists the pin descriptions for J4.

Table 7.1.8 J4 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	DAT3 (PF2/BACK#/DV_DATA2/TxD2/DACK0/ SD_D3/AUDATA0)	7	DAT0 (PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3)
2	CMD (PF3/ICIORD#/SSISCK1/DV_DATA3/ RxD3/SD_CMD/AUDATA1)	8	DAT1 (PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1)
3	GND	9	DAT2 (PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#)
4	3.3 V	10	WP (PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP)
5	CLK (PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/ TxD3/SD_CLK/AUDATA2)	11	CD (PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD)
6	GND	12	COMMON (GND)

7.1.5 PWM Connector (J5)

The M3A-HS64G02 includes one MIL-spec connector (J5) for PWM output. This module cannot be used with the R0K572670C000BR.

The following figure shows the pin assignments for J5.

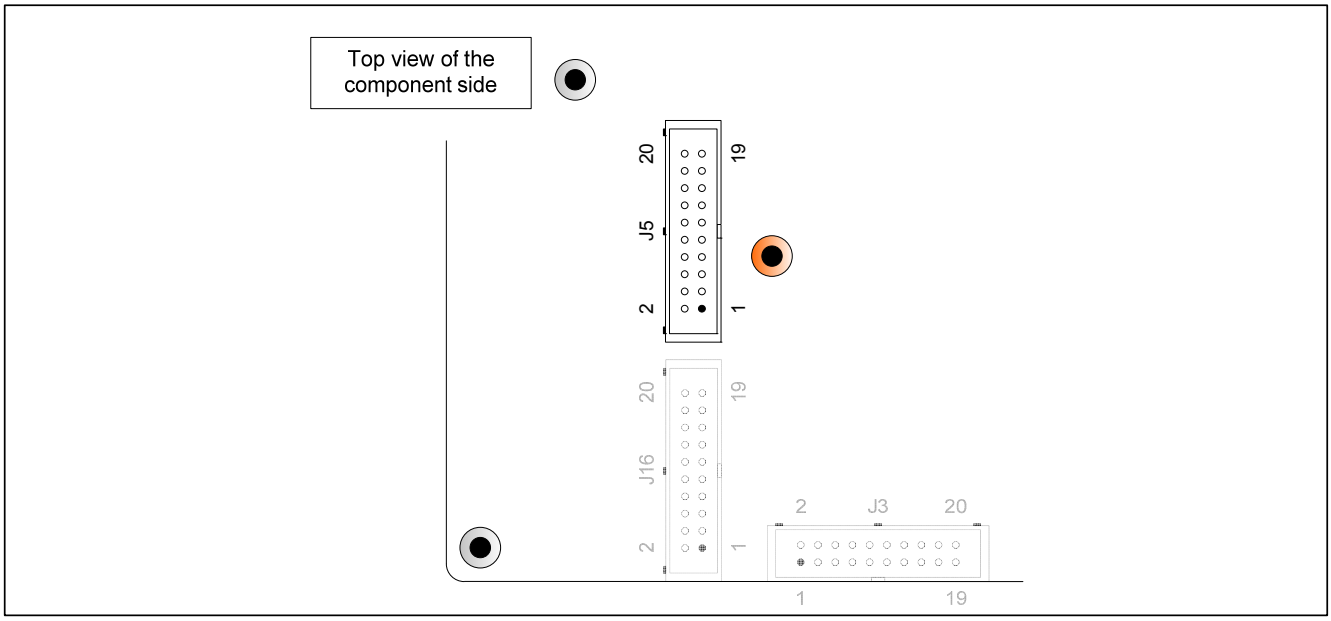


Figure 7.1.7 J5 Pin Assignments

The following table lists the pin descriptions for J5.

Table 7.1.9 J5 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#	11	PF9/A23/SSISCK3/RSPCK0/TIOC3A/FRB
2	PF2/BACK#/DV_DATA2/TxD2/DACK0/ SD_D3/AUDATA0	12	PF10/A24/SSIWS3/SSL00/TIOC3B/FCE#
3	PF3/ICIORD#/SSISCK1/DV_DATA3/RxD3/ SD_CMD/AUDATA1	13	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT
4	PF4/ICIOWR#/AH#/SSIWS1/DV_DATA4/ TxD3/SD_CLK/AUDATA2	14	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN
5	PF5/CS5#/CE1A#/SSIDATA1/DV_DATA5/ TCLKC/SD_D0/AUDATA3	15	Not connected with the R0K572670C000BR
6	PF6/CS6#/CE1B#/SSISCK2/DV_DATA6/ TCLKB/SD_D1	16	PH5/AN5
7	PF7/CE2A#/SSIWS2/DV_DATA7/TCLKD/ SD_WP	17	PH4/AN4
8	PF8/CE2B#/SSIDATA2/DV_CLK/SD_CD	18	Not connected with the R0K572670C000BR
9	GND	19	5 V
10	GND	20	5 V

7.1.6 Audio Optical Connector (J6)

The M3A-HS64G02 includes an audio optical connector (J6).

The following figure shows the pin assignments for J6.

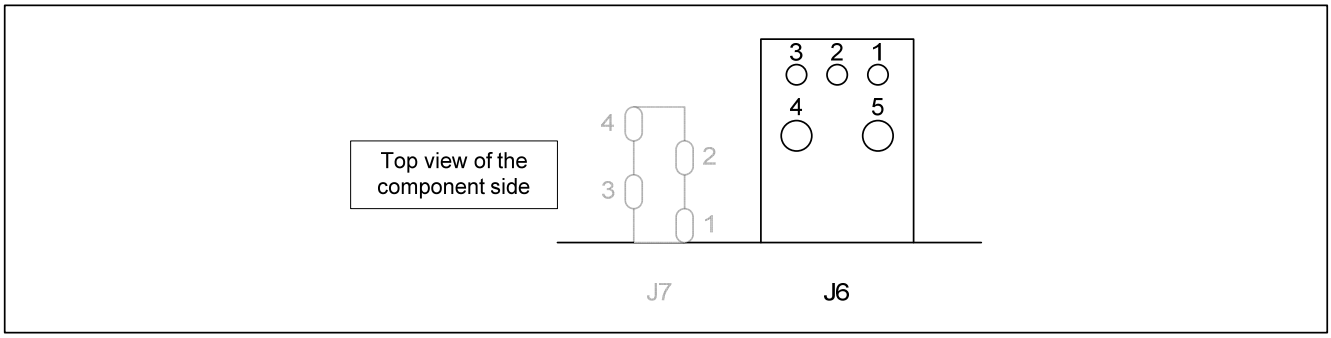


Figure 7.1.8 J6 Pin Assignments

The following table lists the pin descriptions for J6.

Table 7.1.10 J6 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	4	NC
2	3.3 V	5	NC
3	TX (D/A converter optical output pin)	–	

7.1.7 Line-out Pin Jack (J7)

The M3A-HS64G02 includes a line-out pin jack (J7).

The following figure shows the pin assignments for J7.

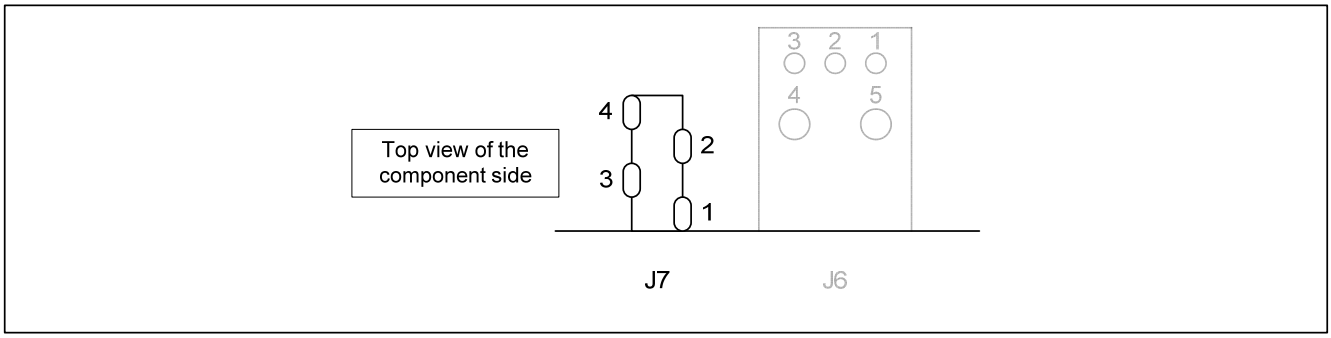


Figure 7.1.9 J7 Pin Assignments

The following table lists the pin descriptions for J7.

Table 7.1.11 J7 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	3	AOUTR (D/A converter analog output R pin)
2	AOUTL (D/A converter analog output L pin)	4	NC

7.1.8 RCA Connector (J8)

The M3A-HS64G02 includes an RCA connector (J8).

The following figure shows the pin assignments for J8.

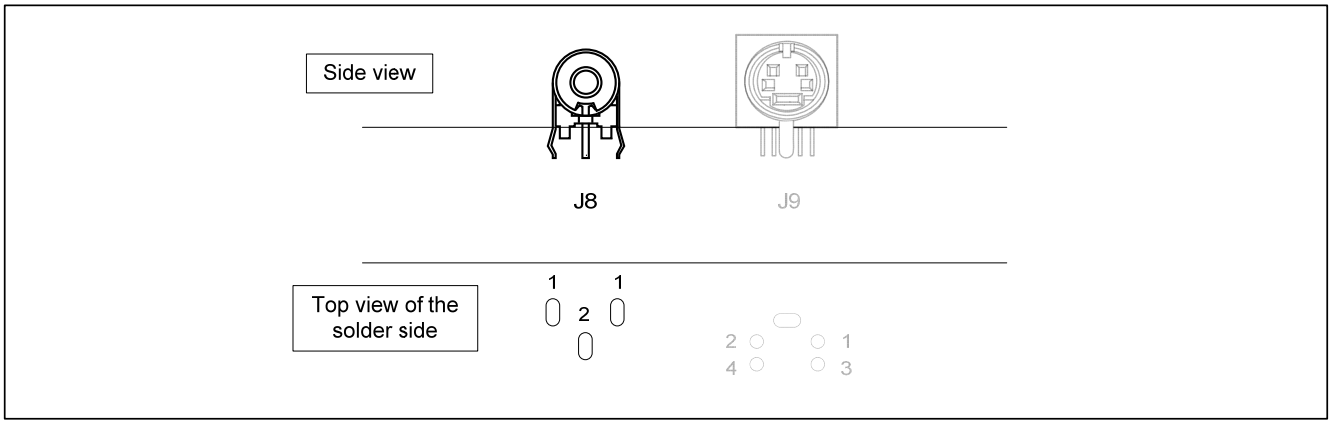


Figure 7.1.10 J8 Pin Assignments

The following table lists the pin descriptions for J8.

Table 7.1.12 J8 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	AIN2 (Video decoder analog input pin)

7.1.9 S-Video Connector (J9)

The M3A-HS64G02 includes an S-Video connector (J9).

The following figure shows the pin assignments for J9.

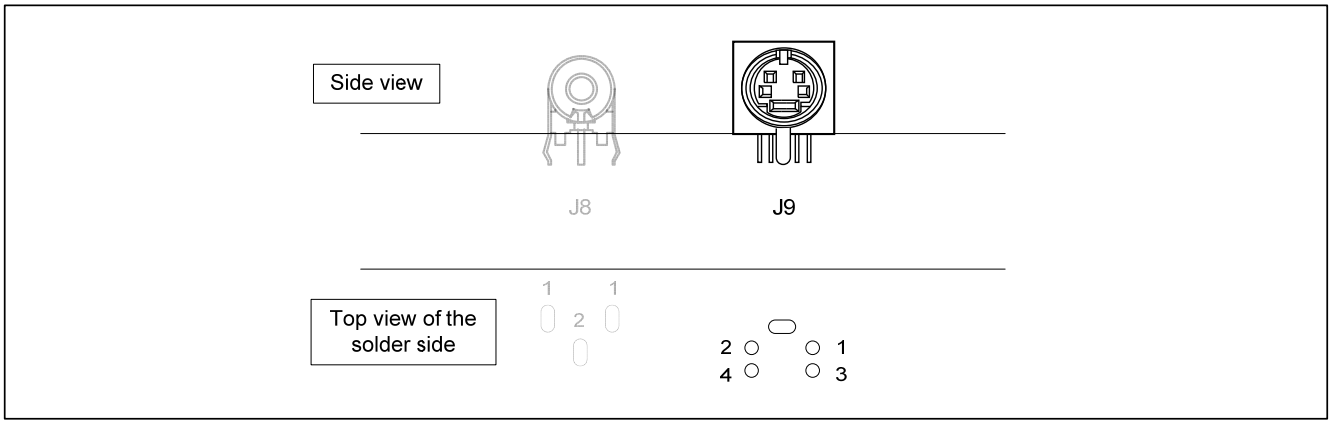


Figure 7.1.11 J9 Pin Assignments

The following table lists the pin descriptions for J9.

Table 7.1.13 J9 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	3	AIN2 (Video decoder analog input pin)
2	GND	4	AIN5 (Video decoder analog input pin)

7.1.10 LCD Module Connectors (J10 to J12)

The M3A-HS64G02 includes two flexible connectors (J10 and J11), and one MIL-spec connector (J12) for connecting an LCD module to this optional board.

The following figure shows the pin assignments for LCD module connectors.

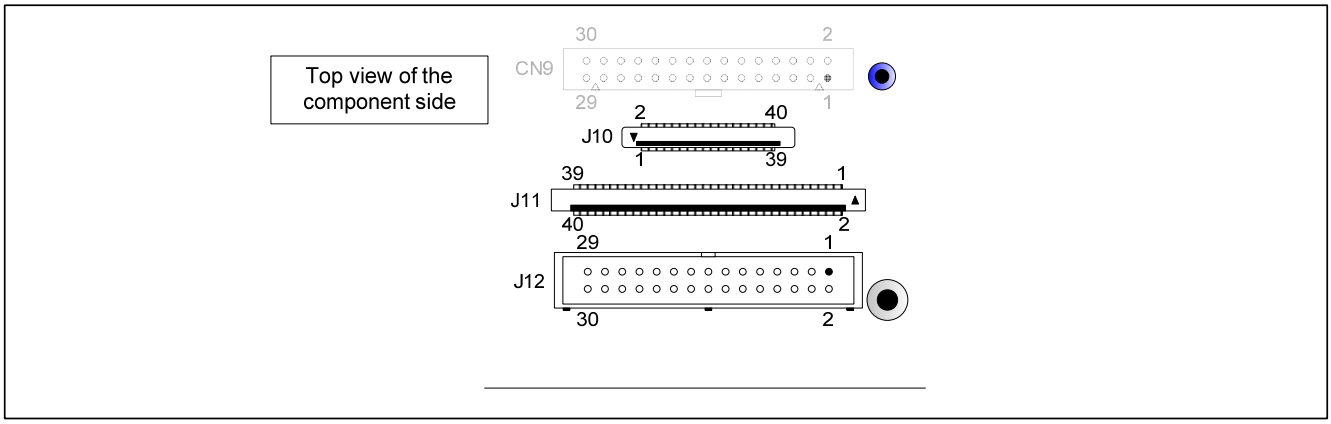


Figure 7.1.12 LCD Module Connectors Pin Assignments (J10 to J12)

The following table lists the pin descriptions for J10.

Table 7.1.14 J10 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	21	G4 (PG9/LCD_DATA9/SSIRxD0/TxD4/ SIOFSYNC)
2	3.3 V	22	G3 (PG8/LCD_DATA8/SSITxD0/RxD4/SIOFSCK)
3	3.3 V	23	GND
4	DCLK (PG19/LCD_CLK/TIOC2B/TxD3/CTS1)	24	G2 (PG7/LCD_DATA7/SD_CD/PINT7/IRQ7)
5	GND	25	G1 (PG6/LCD_DATA6/SD_WP/PINT6/IRQ6)
6	HSYNC (PG17/LCD_HSYNC/TIOC1B/TxD1)	26	G0 (PG5/LCD_DATA5/SD_D1/PINT5/IRQ5)
7	GND	27	GND
8	DTMG (PG18/LCD_DE/TIOC2A/RxD3/RTS1)	28	B5 (PG4/LCD_DATA4/SD_D0/PINT4/IRQ4)
9	GND	29	B4 (PG3/LCD_DATA3/SD_CLK/PINT3)
10	NC	30	B3 (PG2/LCD_DATA2/SD_CMD/PINT2)
11	GND	31	GND
12	R5 (PG15/LCD_DATA15/TIOC0D/TxD7)	32	B2 (PG1/LCD_DATA1/SD_D3/PINT1)
13	R4 (PG14/LCD_DATA14/TIOC0C/RxD7)	33	B1 (PG0/LCD_DATA0/SD_D2/PINT0)
14	R3 (PG13/LCD_DATA13/TIOC0B/TxD6)	34	B0 (PG0/LCD_DATA0/SD_D2/PINT0)
15	GND	35	PCI (NC)
16	R2 (PG12/LCD_DATA12/TIOC0A/RxD6)	36	Vctrl (3.3 V)
17	R1 (PG11/LCD_DATA11/SSIWS0/IRQ3/ TxD5/SIOFTxD)	37	NC
18	R0 (PG11/LCD_DATA11/SSIWS0/IRQ3/ TxD5/SIOFTxD)	38	NC
19	GND	39	NC
20	G5 (PG10/LCD_DATA10/SSISCK0/IRQ2/ RxD5/SIOFRxD)	40	NC

The following table lists the pin descriptions for J11.

Table 7.1.15 J11 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC	21	R3(PG13/LCD_DATA13/TIOC0B/TxD6)
2	DTMG (PG18/LCD_DE/TIOC2A/RxD3/RTS1)	22	R2(PG12/LCD_DATA12/TIOC0A/RxD6)
3	HREV (3.3 V)	23	R1(PG11/LCD_DATA11/SSITxD0/IRQ3/ TxD5/SIOFTxD)
4	B5 (PG4/LCD_DATA4/SD_D0/PINT4/IRQ4)	24	R0 (PG11/LCD_DATA11/SSIWS0/IRQ3/ TxD5/SIOFTxD)
5	B4 (PG3/LCD_DATA3/SD_CLK/PINT3)	25	VREV (3.3 V)
6	B3 (PG2/LCD_DATA2/SD_CMD/PINT2)	26	NC
7	B2 (PG1/LCD_DATA1/SD_D3/PINT1)	27	NC
8	B1 (PG0/LCD_DATA0/SD_D2/PINT0)	28	GND
9	B0 (PG0/LCD_DATA0/SD_D2/PINT0)	29	DCLK (PG19/LCD_CLK/TIOC2B/TxD3/CTS1)
10	3.3 V	30	GND
11	3.3 V	31	GND
12	G5 (PG10/LCD_DATA10/SSISCK0/IRQ2/ RxD5/SIOFRxD)	32	GND
13	G4 (PG9/LCD_DATA9/SSIRxD0/TxD4/ SIOFSYNC)	33	GND
14	G3 (PG8/LCD_DATA8/SSITxD0/RxD4/ SIOFSCK)	34	GND
15	G2 (PG7/LCD_DATA7/SD_CD/PINT7/IRQ7)	35	TMZ (Not connected with the R0K572670C000BR)
16	G1 (PG6/LCD_DATA6/SD_WP/PINT6/IRQ6)	36	GND
17	G0 (PG5/LCD_DATA5/SD_D1/PINT5/IRQ5)	37	DIM (3.3 V)
18	GND	38	NC
19	R5(PG15/LCD_DATA15/TIOC0D/TxD7)	39	5 V
20	R4 (PG14/LCD_DATA14/TIOC0C/RxD7)	40	5 V

The following table lists the pin descriptions for J12.

Table 7.1.16 J12 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3 V	16	PG3/LCD_DATA3/SD_CLK/PINT3
2	3.3 V	17	PG2/LCD_DATA2/SD_CMD/PINT2
3	3.3 V	18	PG1/LCD_DATA1/SD_D3/PINT1
4	PG15/LCD_DATA15/TIOC0D/TxD7	19	PG0/LCD_DATA0/SD_D2/PINT0
5	PG14/LCD_DATA14/TIOC0C/RxD7	20	GND
6	PG13/LCD_DATA13/TIOC0B/TxD6	21	PG19/LCD_CLK/TIOC2B/TxD3/CTS1
7	PG12/LCD_DATA12/TIOC0A/RxD6	22	PG17/LCD_HSYNC/TIOC1B/TxD1
8	PG11/LCD_DATA11/SSIWS0/IRQ3/TxD5/ SIOFTxD	23	NC (LCD_VCPWC)
9	PG10/LCD_DATA10/SSISCK0/IRQ2/RxD5/ SIOFRxD	24	NC (Allowed to supply 5 V through 0-Ω resistor)
10	PG9/LCD_DATA9/SSIRxD0/TxD4/SIOFSYNC	25	PG16/LCD_VSYNC/TIOC1A/RxD1
11	PG8/LCD_DATA8/SSITxD0/RxD4/SIOFSCK	26	PG18/LCD_DE/TIOC2A/RxD3/RTS1
12	PG7/LCD_DATA7/SD_CD/PINT7/IRQ7	27	PJ2/CTx1/CTx0&CTx1/CS2#/SCK0/ LCD_M_DISP
13	PG6/LCD_DATA6/SD_WP/PINT6/IRQ6	28	GND
14	PG5/LCD_DATA5/SD_D1/PINT5/IRQ5	29	GND
15	PG4/LCD_DATA4/SD_D0/PINT4/IRQ4	30	GND

7.1.11 IEBus™ Connector (J13)

The M3A-HS64G02 includes an IEBus™ connector (J13).

The following figure shows the pin assignments for J13.

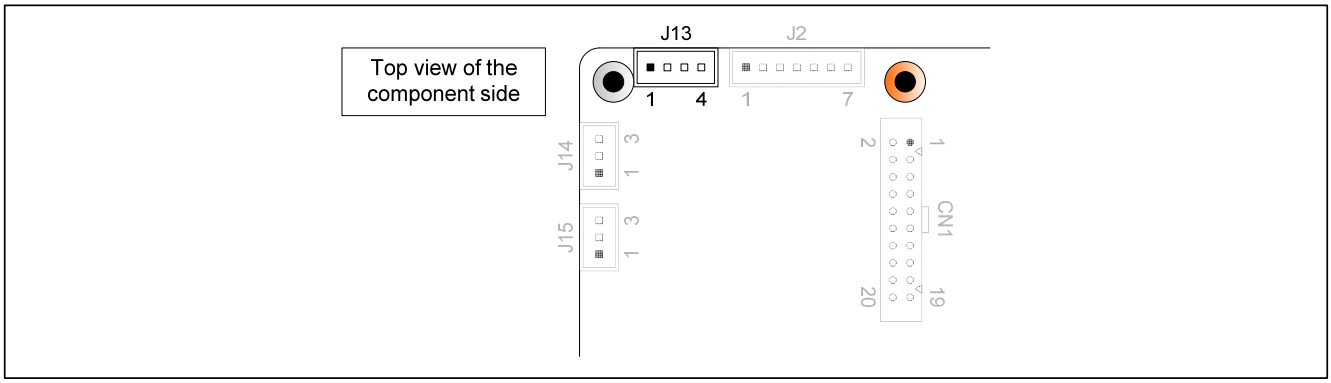


Figure 7.1.13 J13 Pin Assignments

The following table lists the pin descriptions for J13.

Table 7.1.17 J13 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	5 V	3	BUS+
2	BUS−	4	GND

7.1.12 CAN Connectors (J14 and J15)

The M3A-HS64G02 includes two CAN connectors (J14 and J15).

The following figure shows the pin assignments for J14 and J15.

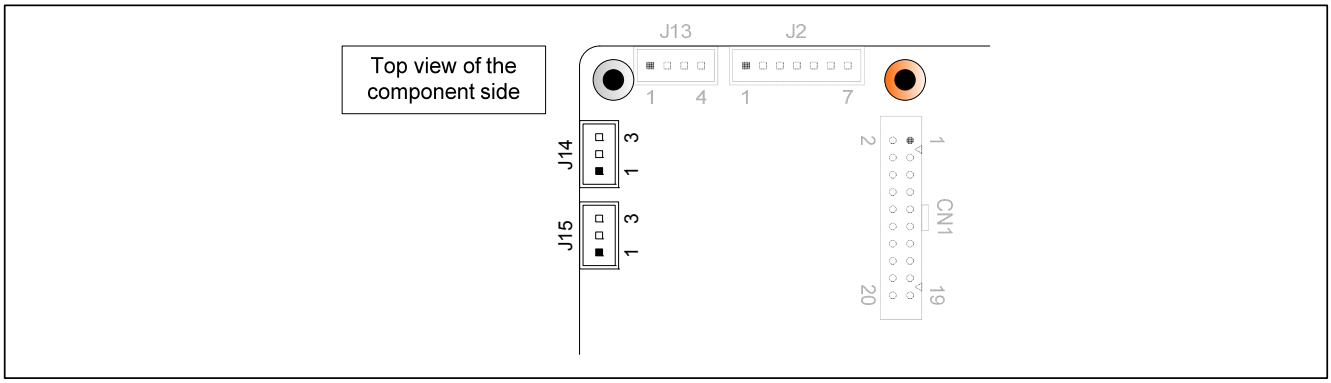


Figure 7.1.14 J14, J15 Pin Assignments

The following table lists the pin descriptions for J14 and J15.

Table 7.1.18 J14, J15 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	CANH	3	GND
2	CANL	–	

J14 and J15 are connected to channel 0 (CTx0/CRx0) and channel 1 (CTx1/CRx1), respectively.

7.1.13 MTU2 Connector (J16)

The M3A-HS64G02 includes a MIL-spec connector (J16) for MTU2 output. Available pins are limited when using this module with the R0K572670C000BR.

The following figure shows the pin assignments for J16.

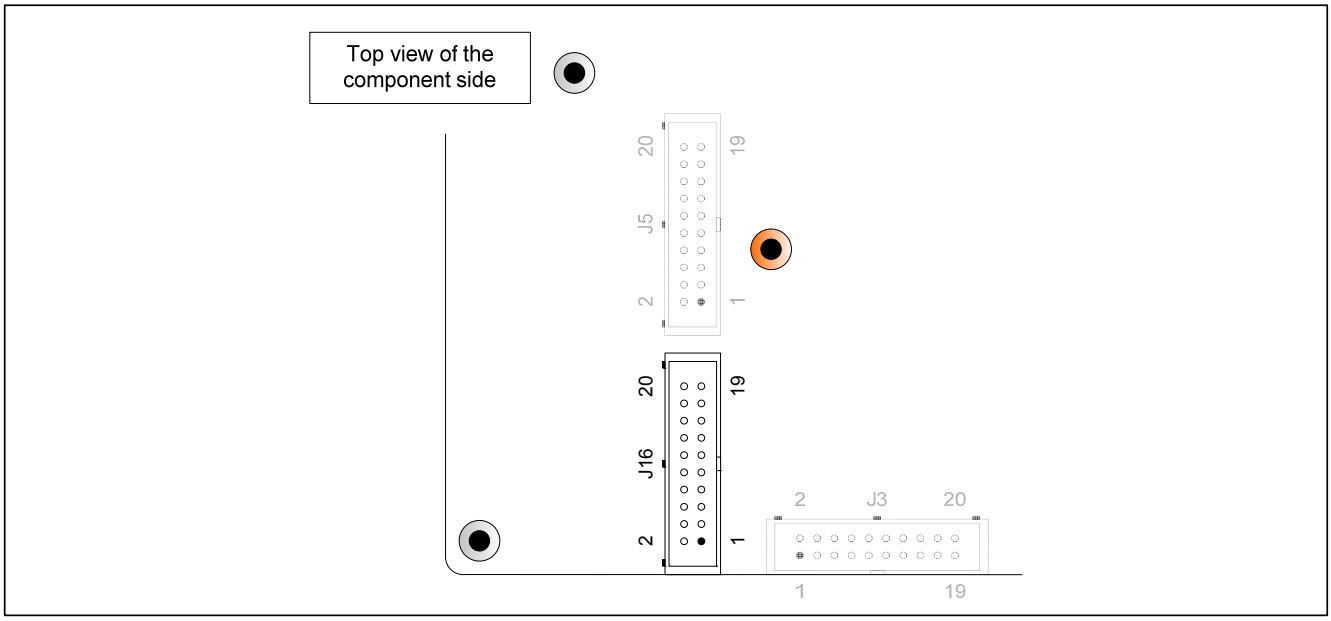


Figure 7.1.15 Pin Assignments for MTU2 Connector (J16)

The following table lists the pin descriptions for J16.

Table 7.1.19 J16 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	PF11/A25/SSIDATA3/MOSI0/TIOC3C/ SPDIF_IN (1)	11	Not connected with the R0K572670C000BR
2	PF12/BS#/MISO0/TIOC3D/SPDIF_OUT (1)	12	Not connected with the R0K572670C000BR
3	GND	13	GND
4	GND	14	GND
5	PG22/SSL1/TIOC0B	15	PC7/CKE/TIOC4C/IRQ6
6	PF1/BREQ#/DV_DATA1/RxD2/DREQ0/ SD_D2/AUDSYNC#	16	PC8/CS3#/TIOC4D/IRQ6
7	PG21/RSPCK1/TIOC0A	17	PC5/RAS#/TIOC4A/IRQ4
8	Not connected with the R0K572670C000BR	18	PC6/CAS#/TIOC4B/IRQ5
9	GND	19	PG23/MOSI1/TIOC0C
10	GND	20	PG24/MISO1/TIOC0D

Note 1: As these pins are connected to the serial flash memory (U10) on the R0K572670C000BR, do not set the function as MTU2.

7.1.14 12 V Power Supply Connector (J17)

The M3A-HS64G02 includes a system power supply connector (J17). The number of pins of this connector differs from the power supply connector mounted on the R0K572670C000BR to prevent improper insertion.

The following figure shows the pin assignments for J17.

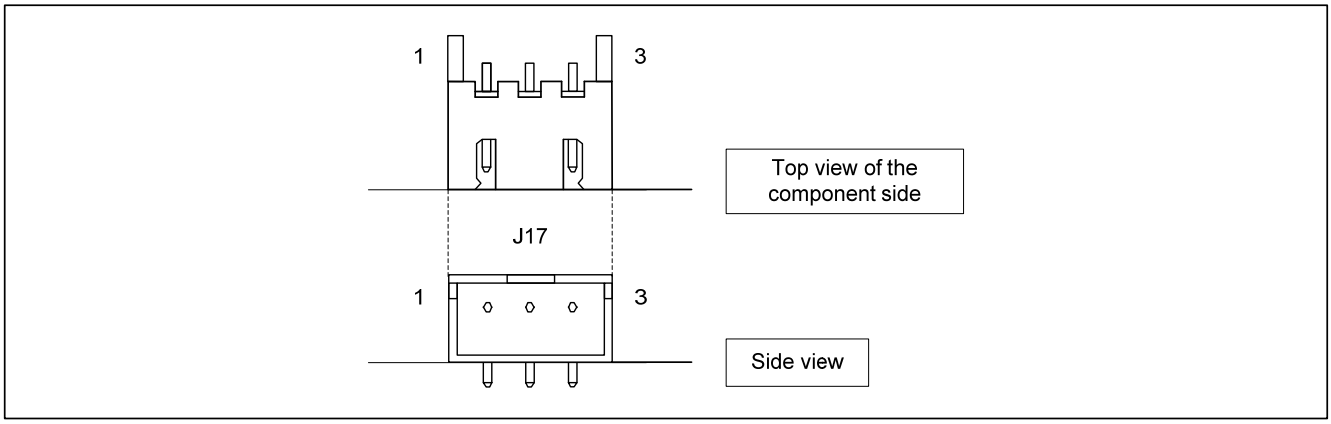


Figure 7.1.16 J17 Pin Assignments

The following table lists the pin descriptions for J17.

Table 7.1.20 J17 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	12 V	3	GND
2	NC	–	

7.1.15 12 V Input AC Adapter Jack (J18)

The M3A-HS64G02 includes an AC adapter jack (J18) for 12 V DC input.

The following figure shows the pin assignments for J18.

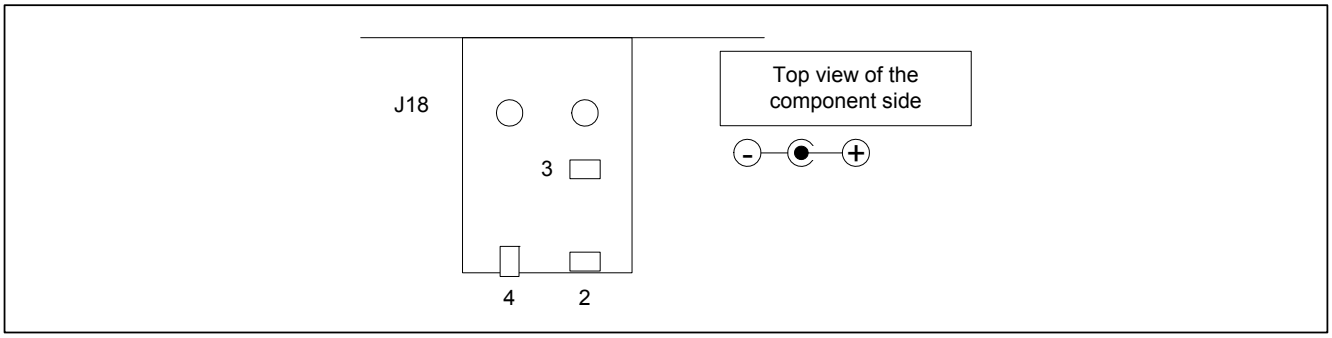


Figure 7.1.17 J18 Pin Assignments

The following table lists the pin descriptions for J18.

Table 7.1.21 J18 Pin Descriptions

Pin Number	Signal Name	Pin Number	Signal Name
1	NC (No pins)	3	GND
2	12 V	4	GND

7.2 M3A-HS64G02 Operating Components

The following figure shows the assignments of the M3A-HS64G02 operating components.

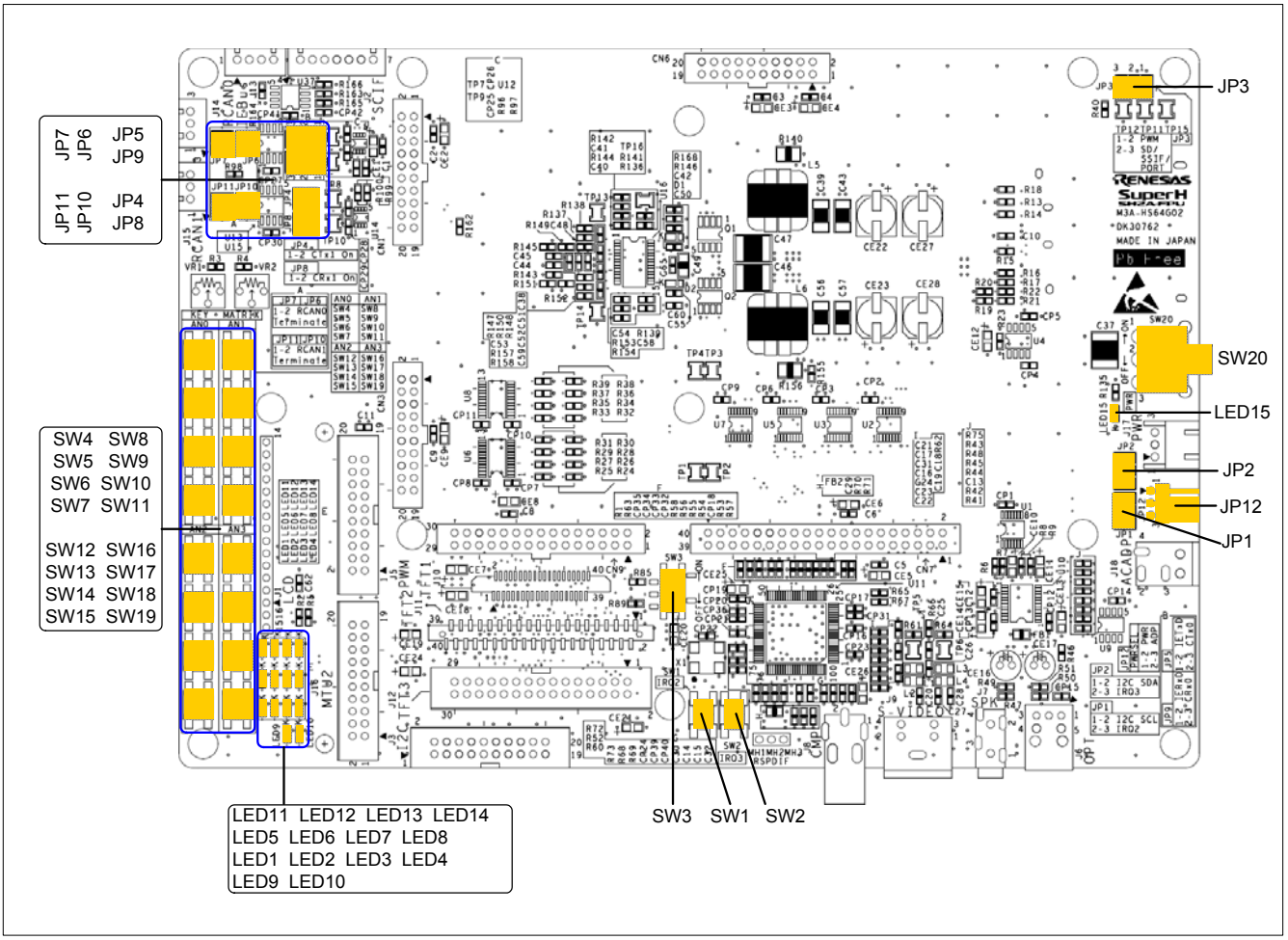


Figure 7.2.1 M3A-HS64G02 Operating Components (Top View of the Component Side)

7.2.1 Jumpers (JP1 to JP12)

The M3A-HS64G02 includes 12 jumpers. The following figure shows jumper assignments (JP1 to JP12) on the M3A-HS64G02.

Figure 7.2.2 M3A-HS64G02 Jumper Assignments (JP1 to JP12)

The following table lists the jumpers setting for JP1, JP2, JP3, JP5, and JP9.

Table 7.2.1 Multi-function Pin Switch Jumpers Setting (JP1, JP2, JP3, JP5, and JP9)

Number	Setting	Description
JP1	1 - 2	Connects the D/A converter (U10) as the SCL1 output pin
SCL1/IRQ2	2 - 3	Connects the push-button switch (SW1) as the IRQ2 input pin (1)
JP2	1 - 2	Connects the D/A converter (U10) as the SDA1 I/O pin
SDA1/IRQ3	2 - 3	Connects the push-button switch (SW2) as the IRQ3 input pin (1)
JP3	1 - 2	Connects the MIL-spec connector (J5) as the PWM data output pin (1)
PWM/ (SD/SSIF/PORT)	2 - 3	Connects the SD card slot (J4), D/A converter (U10), and test pins (TP1 to TP4) as the SDHI, SSIF, and PORT I/O pins
JP5	1 - 2	Connects the IEBus™ driver (U37) as the IETxD output pin
IETxD/CTx0	2 - 3	Connects the CAN driver (U13) as the CTx0 output pin (1)
JP9	1 - 2	Connects the IEBus™ driver (U37) as the IERxD input pin
IERxD/CRx0	2 - 3	Connects the CAN driver (U13) as the CRx0 input pin (1)

Note 1: Default setting

Table 7.2.2 CAN Evaluation Jumper Setting (JP4, JP6, JP7, JP8, JP10, and JP11)

Number	Setting	Description
JP4 Connects CTx1	1 - 2	Connects the CTx1 pin to the CAN driver (U16) (1)
	None (Open)	Leaves the CTx1 pin disconnected to the CAN driver (U16)
JP8 Connects CRx1	1 - 2	Connects the CRx1 pin to the CAN driver (U16) (1)
	None (Open)	Leaves the CRx1 pin disconnected to the CAN driver (U16)
JP6 Terminates CANL (ch0)	1 - 2	Terminates the CANL (ch0) pin
	None (Open)	Leaves the CANL (ch0) pin not terminated (1)
JP7 Terminates CANH (ch0)	1 - 2	Terminates the CANH (ch0) pin
	None (Open)	Leaves the CANH (ch0) pin not terminated (1)
JP10 Terminates CANL (ch1)	1 - 2	Terminates the CANL (ch1) pin
	None (Open)	Leaves the CANL (ch1) pin not terminated (1)
JP11 Terminates CANH (ch1)	1 - 2	Terminates the CANH (ch1) pin
	None (Open)	Leaves the CANH (ch1) pin not terminated (1)

Table 7.2.3 Power Supply Switch Jumper Setting (JP12)

Number	Setting	Description
JP12 PWRSEL	1 - 2	Supplies the system power from J17
	2 - 3	Supplies the system power from J18 (AC adapter is used) (1)

Notes:

1. Default setting
2. Do not change the jumper settings while the M3A-HS64G02 is ON. Be sure to turn the power OFF before changing the settings.

7.2.2 Switches and LEDs

The M3A-HS64G02 includes 20 switches and 15 LEDs. The following figure shows assignments of switches and LEDs.

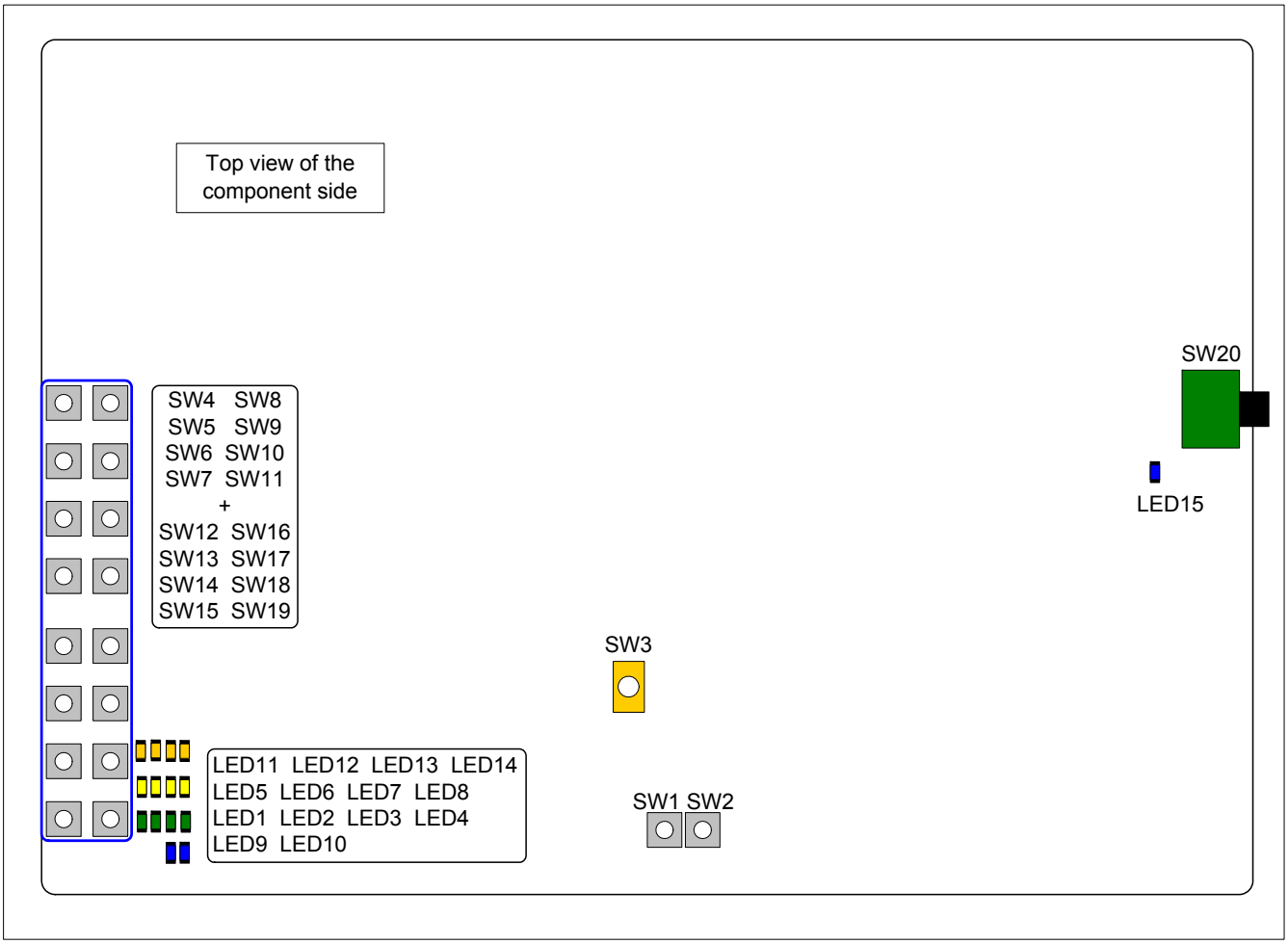


Figure 7.2.3 M3A-HS64G02 Switches and LEDs Assignments

The following table lists switches mounted on the M3A-HS64G02.

Table 7.2.4 M3A-HS64G02 Switches

Number	Name	Remarks
SW1	IRQ2 switch	Refer to Section 4.13 for details.
SW2	IRQ3 switch	Refer to Section 4.13 for details.
SW3	LCD module connector (J10) power supply switch	Optional
SW4 to SW19	Key input switches	Refer to Section 4.12 for details.
SW20	Power supply switch	–

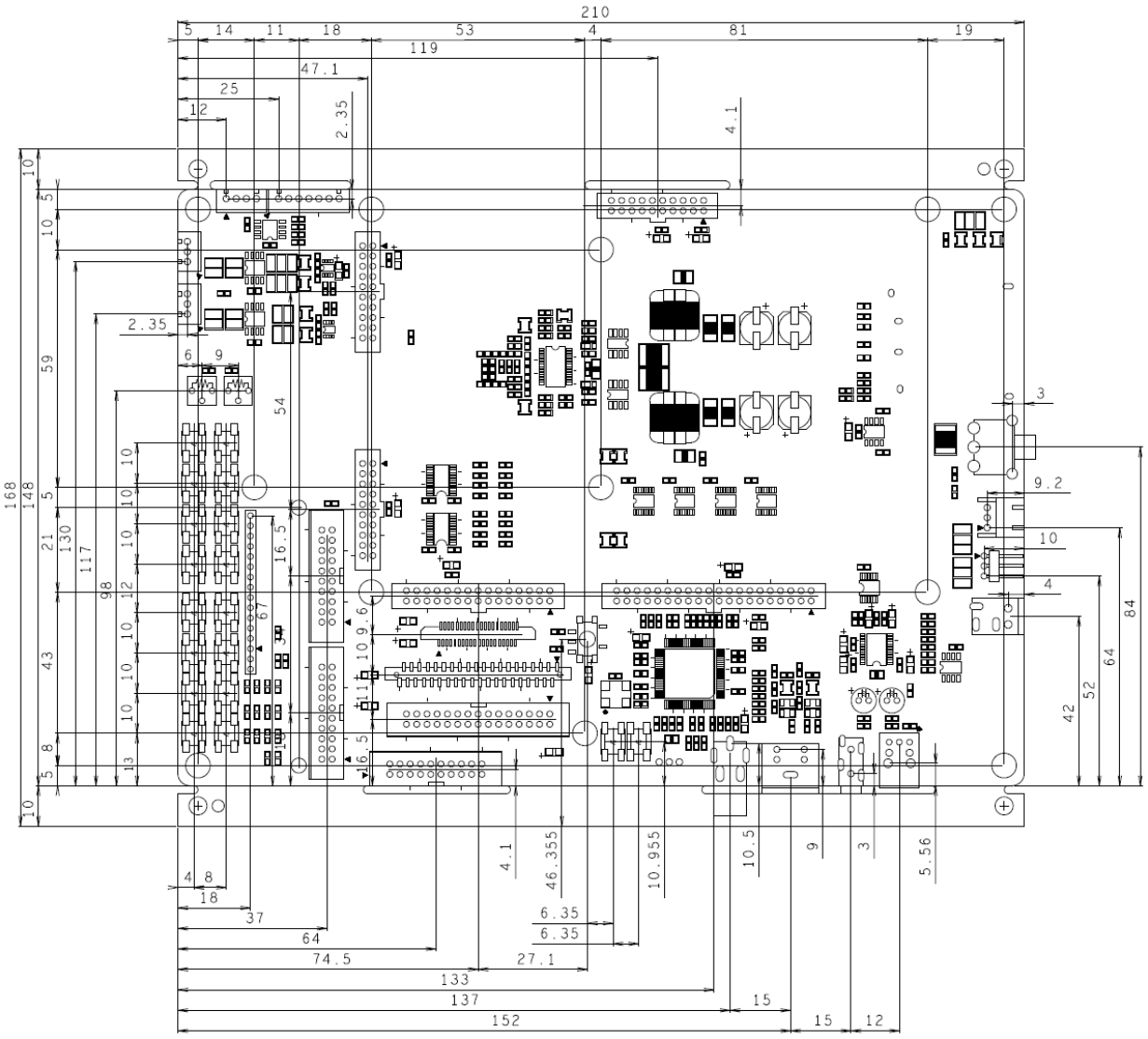
The following table lists LEDs mounted on the M3A-HS64G02.

Table 7.2.5 M3A-HS64G02 LEDs

Number	Color	Description
LED1 to LED4	Green	Brightness-control LEDs (MTU2 output pins: TIOC0A to 0D are connected)
LED5 to LED8	Yellow	Brightness-control LEDs (MTU2 output pins: TIOC1A, 1B, TIOC2A, and 2B are connected)
LED9 and LED10	Blue	Brightness-control LEDs (MTU2 output pins: TIOC3C and 3D are connected)
LED11 to LED14	Orange	Brightness-control LEDs (MTU2 output pins: TIOC4A to 4D are connected)
LED15	Blue	Power supply LED (LED15 is illuminated when 12 V power is supplied)

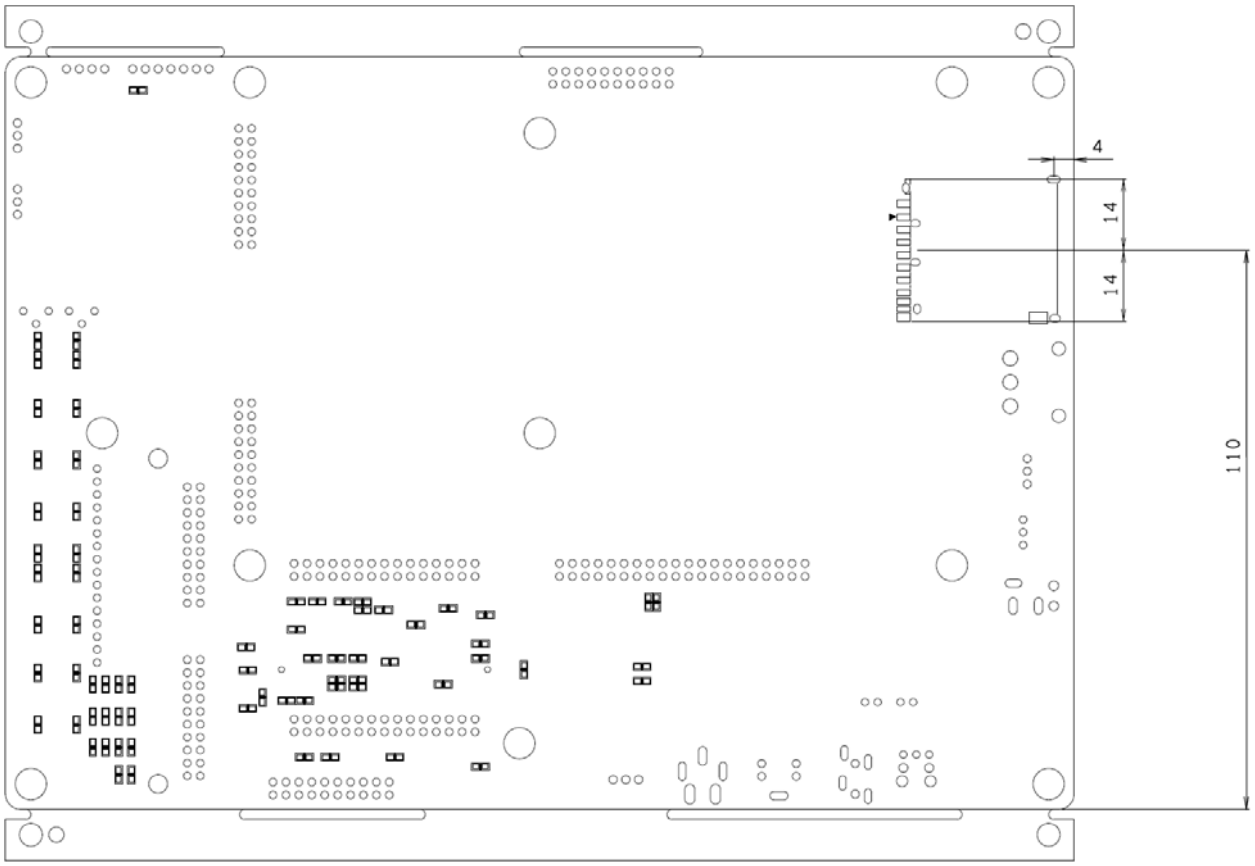
7.3 M3A-HS64G02 Dimensions

Figure 7.3.1 and Figure 7.3.2 show the M3A-HS64G02 dimensions.



Note: All measurements are in millimeters.

Figure 7.3.1 M3A-HS64G02 Dimensions (Top View of the Component Side)



Note: All measurements are in millimeters.

Figure 7.3.2 M3A-HS64G02 Dimensions (Transparent View of the Component Side)

Appendix
Schematics

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SH7267 CPU board R0K572670C000BR SCHEMATICS

TITLE	PAGE

Note:

Digital GND (GND)

Analog GND (AVss)

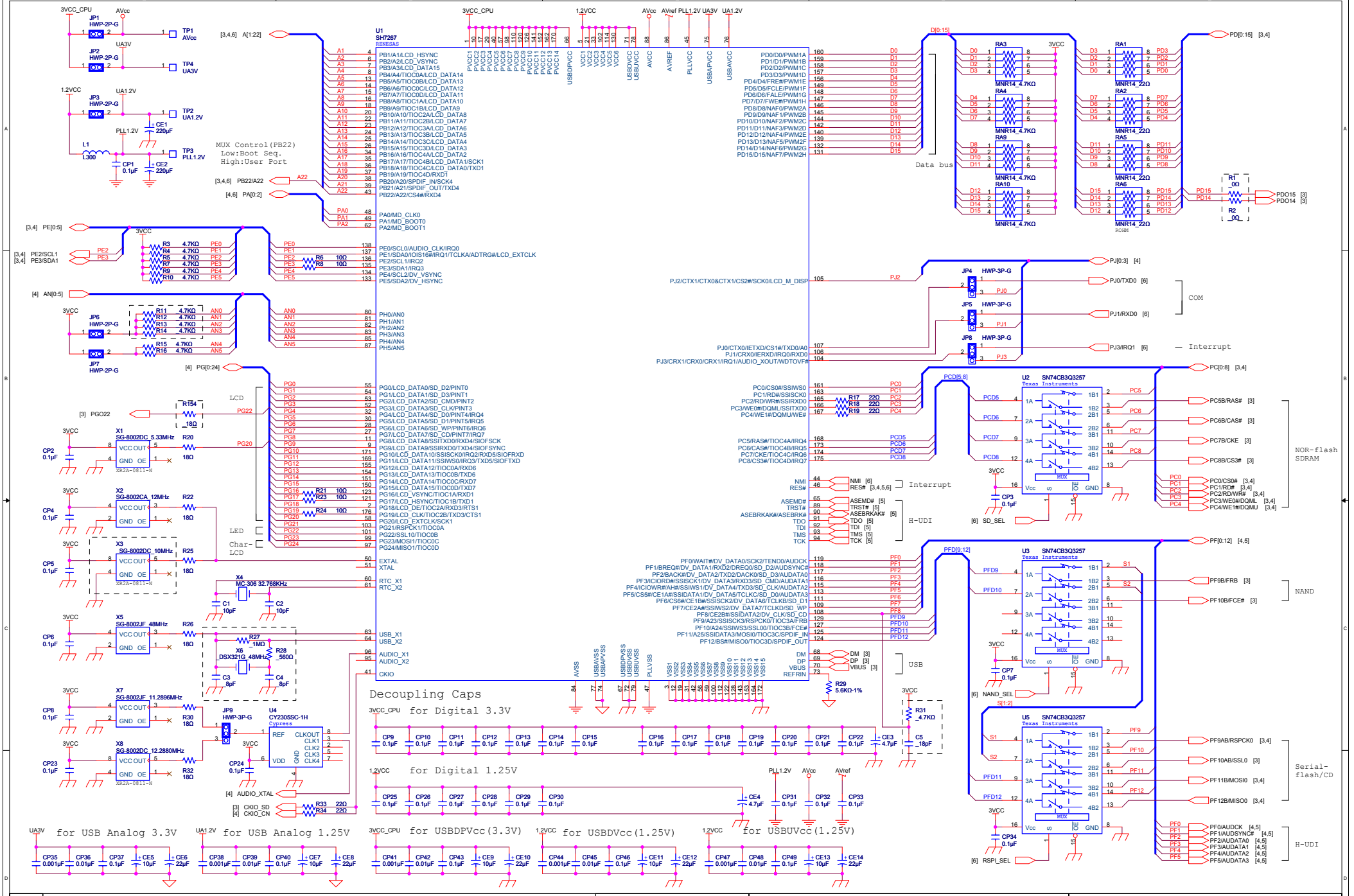
USB Analog GND (USB_AVSS)

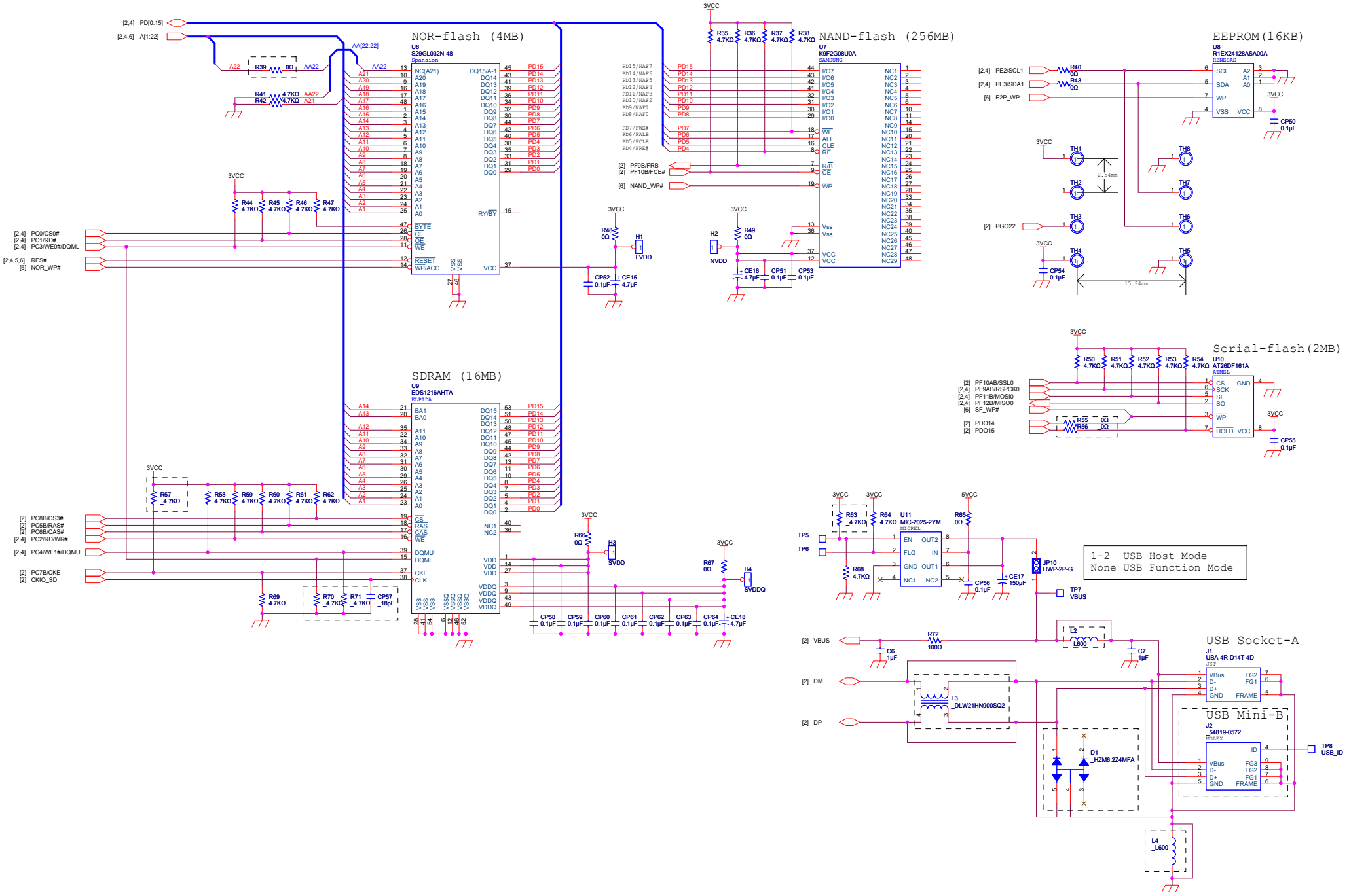
Not mounted

5VCC = Digital 5V
3VCC = Digital 3.3V
3VCC_CPU = 3.3V for CPU
1.2VCC = 1.25V
PLL1.2V = 1.25V for PLL
UA3V = Analog 3.3V for USB
UA1.2V = Analog 1.25V for USB
AVcc = Analog 3.3V
AVref = 3.3V for ADC Voltage Reference

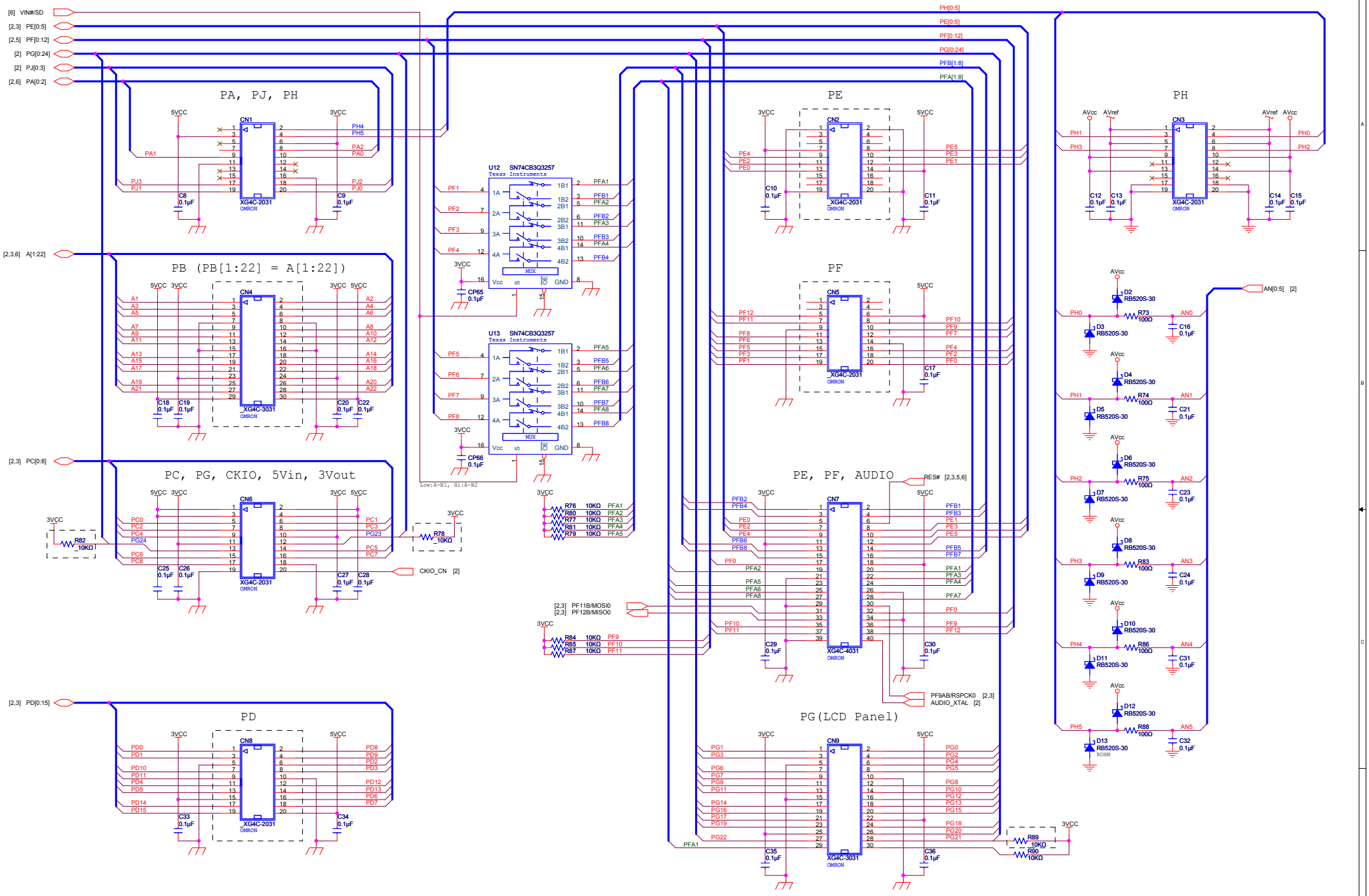
R = Fixed Resistors
RA = Resistor Array
C = Ceramic Caps
CE = Tantalum Electrolytic Caps
CP = Decoupling Caps

CHANGE						
Ver.1.00A	SCALE		Renesas Solutions Corp.			R0K572670C000BR INDEX (1 / 6)
	DATE	10-10-22	DRAWN	CHECKED	DESIGNED	APPROVED	DK30825

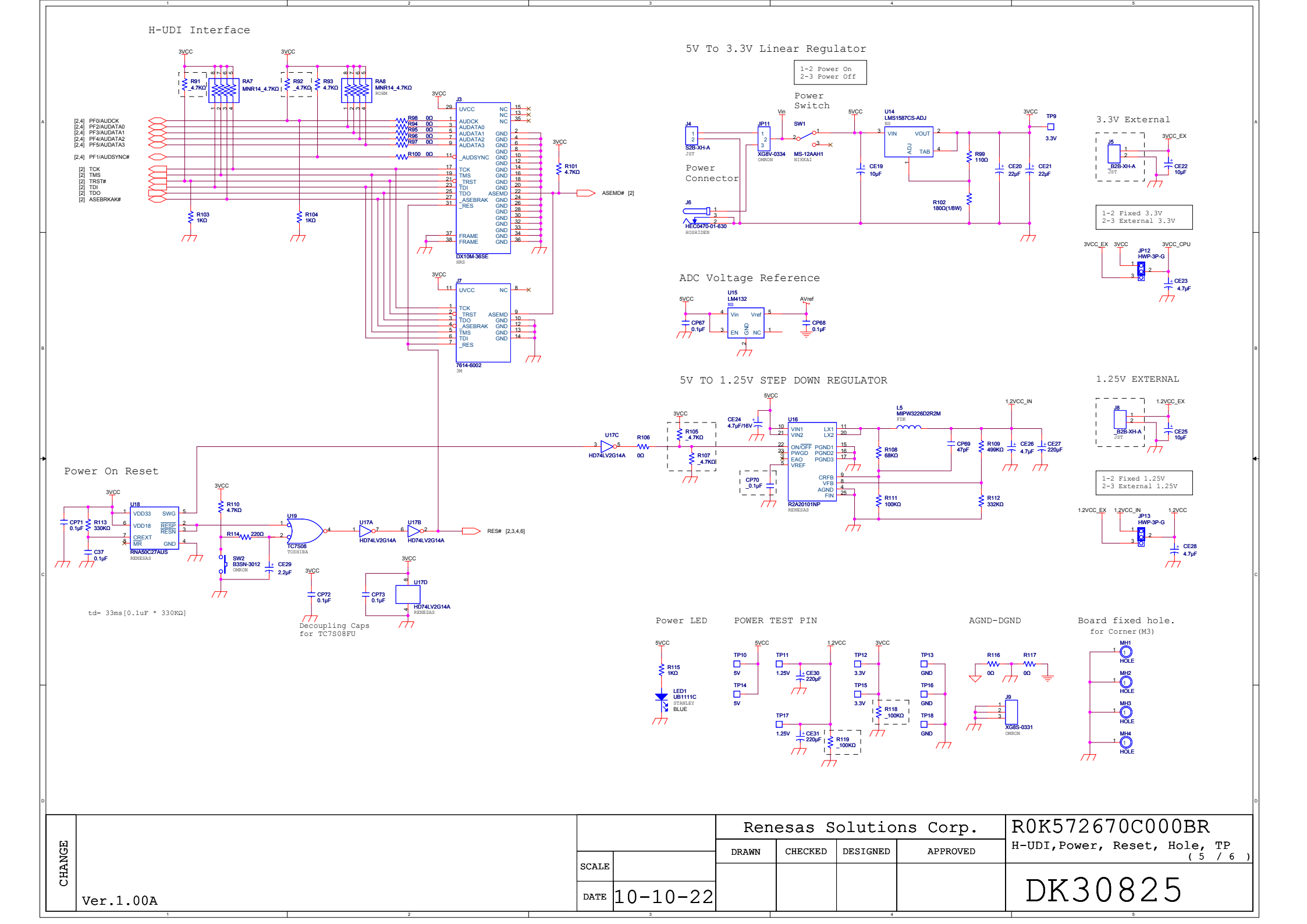

U1
SH7267
RENESAS
Decoupling Caps
for Digital 3.3V
for Digital 1.25V
for USB Analog 3.3V
for USB Analog 1.25V
for USBDPVcc(3.3V)
for USBDVcc(1.25V)
for USBUVcc(1.25V)
MUX Control(PB22)
Low:Boot Seq.
High:User Port
Data bus
COM
Interrupt
H-UDI
USB
NOR-flash
SDRAM
NAND
Serial-
flash/CD
LCD
LED
Char-
LCD
Renesas Solutions Corp.
R0K572670C000BR
CPU SH7267, Clock, MUX
(2 / 6)
DK30825
CHANGE
Ver.1.00A
SCALE
DATE
10-10-22
DRAWN
CHECKED
DESIGNED
APPROVED

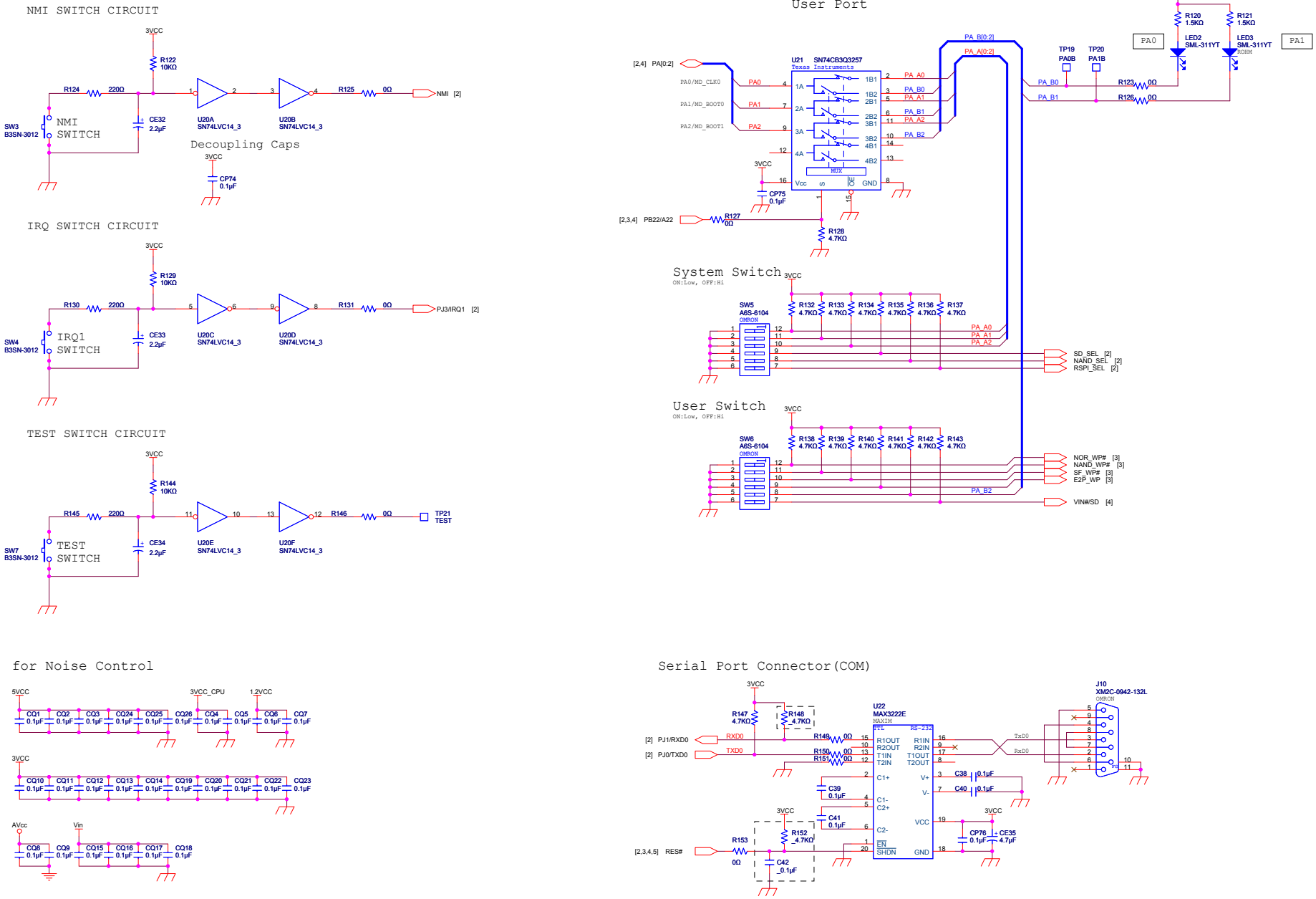


CHANGE			Renesas Solutions Corp.		R0K572670C000BR
			DRAWN / CHECKED / DESIGNED / APPROVED		Memory, USB
					(3 / 6)
Ver.1.00A		SCALE			DK30825
		DATE	10-10-22		



CHANGE			Renesas Solutions Corp.		R0K572670C000BR
			DRAWN / CHECKED / DESIGNED / APPROVED		Ext. Connector, AD Protection (4 / 6)
Ver.1.00A		SCALE			DK30825
		DATE	10-10-22		


H-UDI Interface
5V To 3.3V Linear Regulator
1-2 Power On
2-3 Power Off
Power Switch
Power Connector
3.3V External
1-2 Fixed 3.3V
2-3 External 3.3V
ADC Voltage Reference
5V TO 1.25V STEP DOWN REGULATOR
1.25V EXTERNAL
1-2 Fixed 1.25V
2-3 External 1.25V
Power On Reset
td= 33ms[0.1uF * 330KΩ]
Decoupling Caps
for TC7S08FU
Power LED
POWER TEST PIN
AGND-DGND
Board fixed hole.
for Corner(M3)
Renesas Solutions Corp.
R0K572670C000BR
H-UDI,Power, Reset, Hole, TP
(5 / 6)
DRAWN
CHECKED
DESIGNED
APPROVED
SCALE
DATE
10-10-22
CHANGE
Ver.1.00A
DK30825



CHANGE			Renesas Solutions Corp.		R0K572670C000BR
			DRAWN / CHECKED / DESIGNED / APPROVED		Switch, User Port, UART (6 / 6)
Ver.1.00A		SCALE			DK30825
		DATE	10-10-22		

SH7264/62 Optional board M3A-HS64G01 SCHEMATICS

TITLE	PAGE

Note:

Digital GND (GND)

Analog GND (AVSS)

Analog GND (AGND)

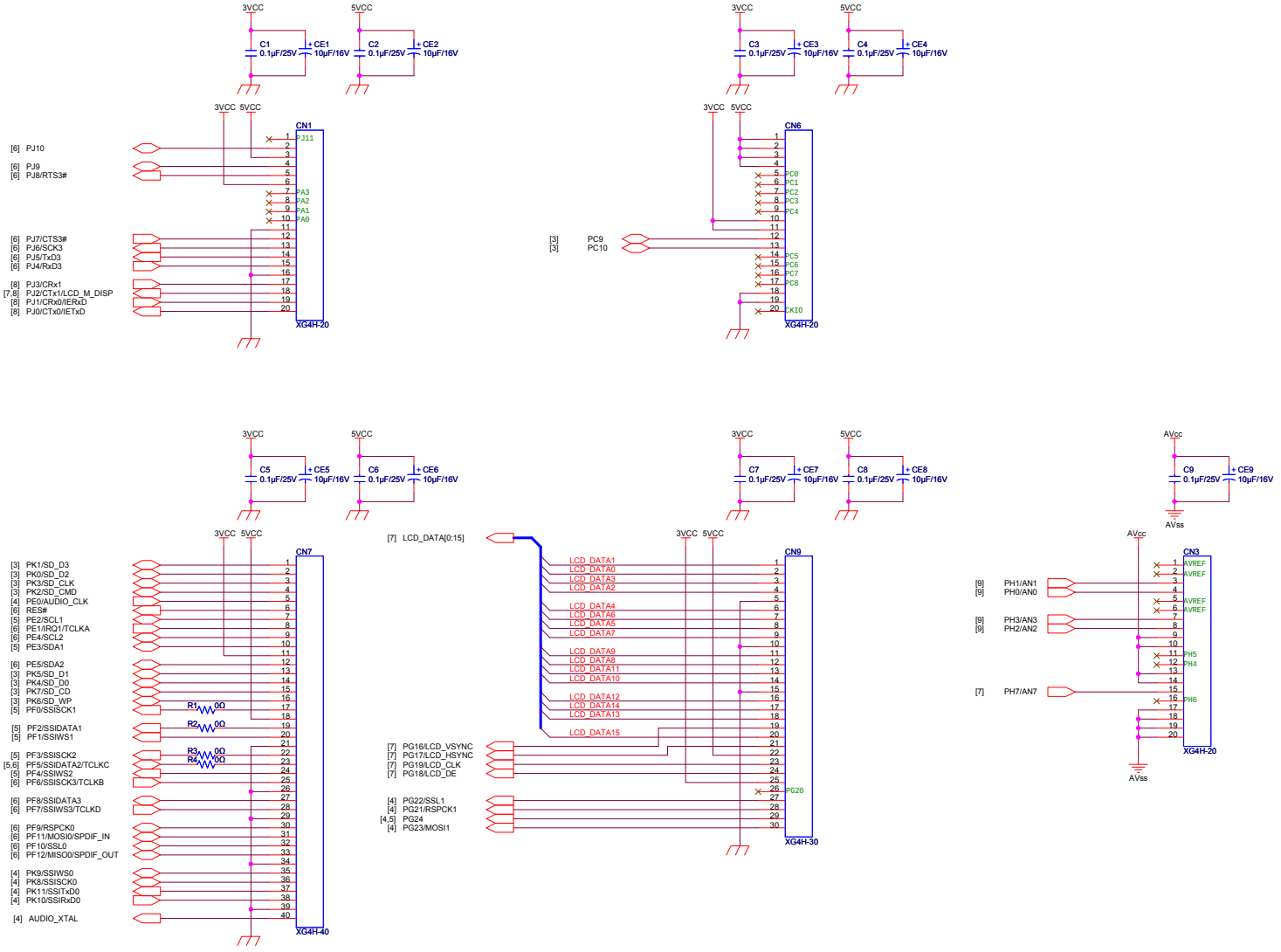
Not mounted

12VCC = Digital 12V Power in
8VCC = Digital 8V for CD
5VCC = Digital 5V
5AVCC = Analog 5V for Audio CODEC
3VCC = Digital 3.3V
3AVCC = Analog 3.3V for Audio DAC
AVcc = Analog 3.3V for Key Input
MCVCC = Digital 3.3V / 5V for SD

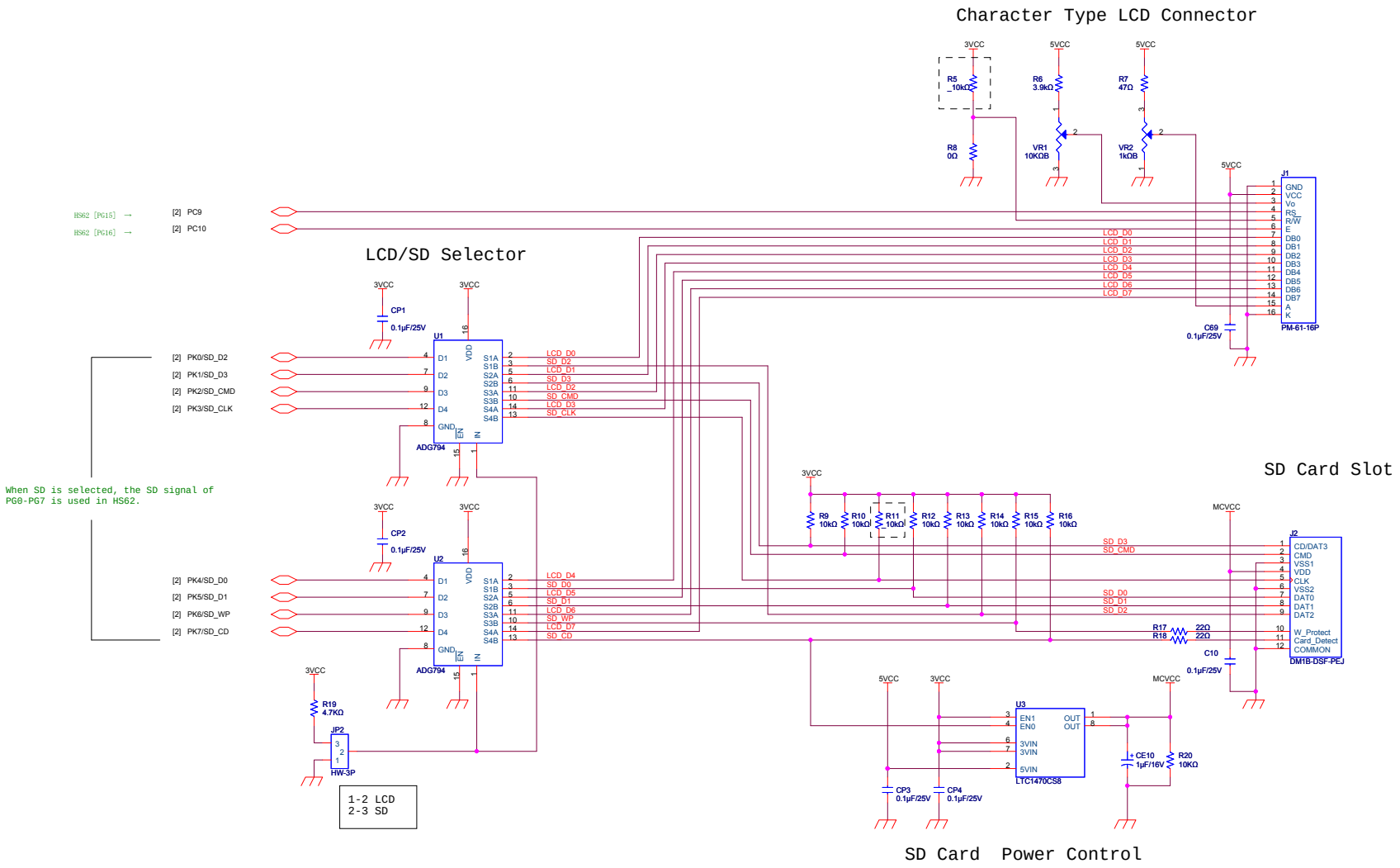
R = Fixed Resistors
C = Ceramic Caps
CP = Decoupling Caps
CE = Electrolytic Caps (Tantal / Electric)

CHANGE							
Ver. 1.00B			Renesas Solutions Corp.				M3A-HS64G01
	SCALE		DRAWN	CHECKED	DESIGNED	APPROVED	INDEX (1 / 10)
	DATE	09-03-02					DK30759

M3A-HS64/HS62 CPU Board Stack Connector

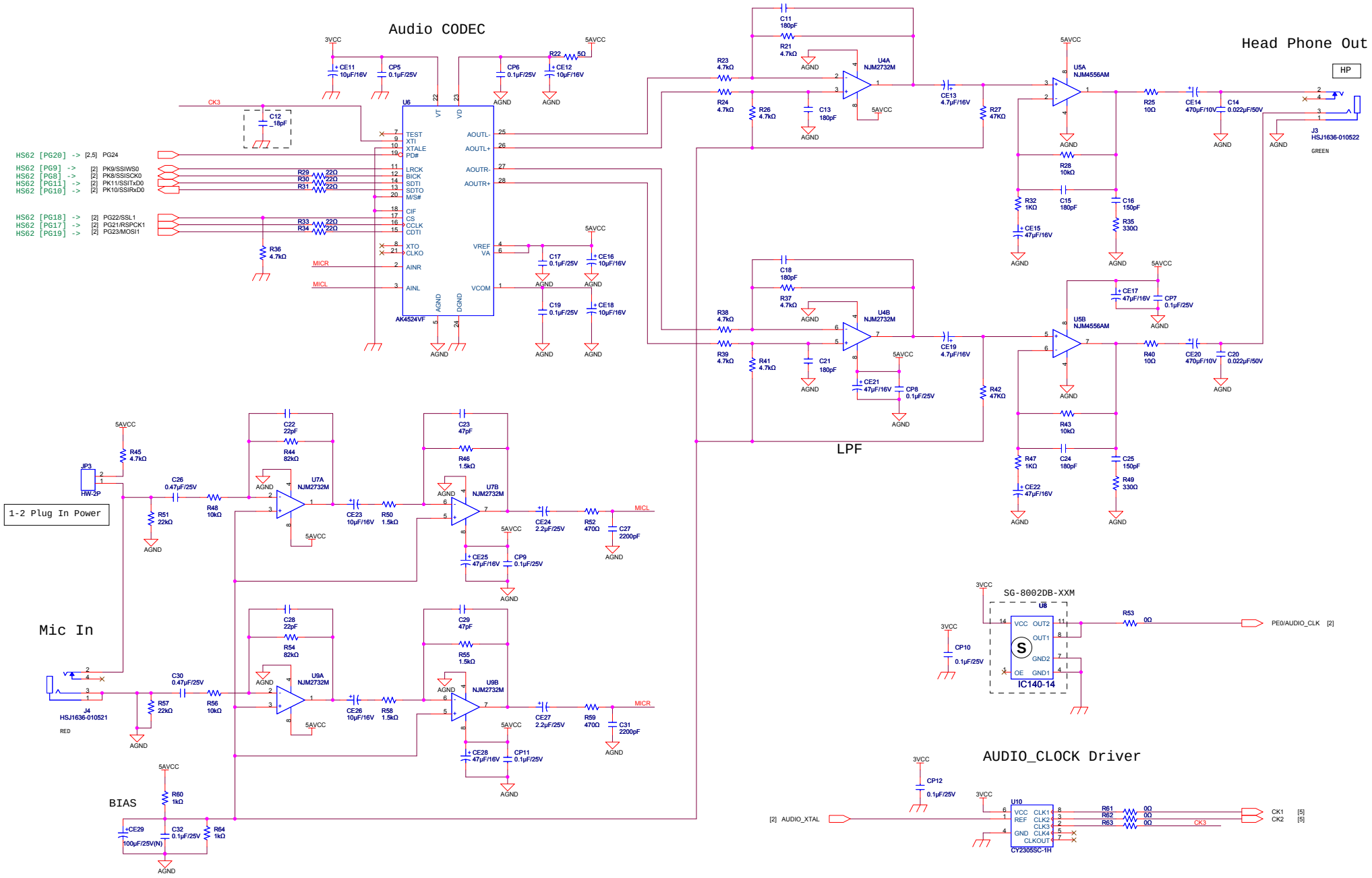


CHANGE			Renesas Solutions Corp.				M3A-HS64G01
			DRAWN	CHECKED	DESIGNED	APPROVED	CPU Board Stack Connector (2 / 10)
Ver. 1.00B		SCALE					DK30759
		DATE	09-03-02				



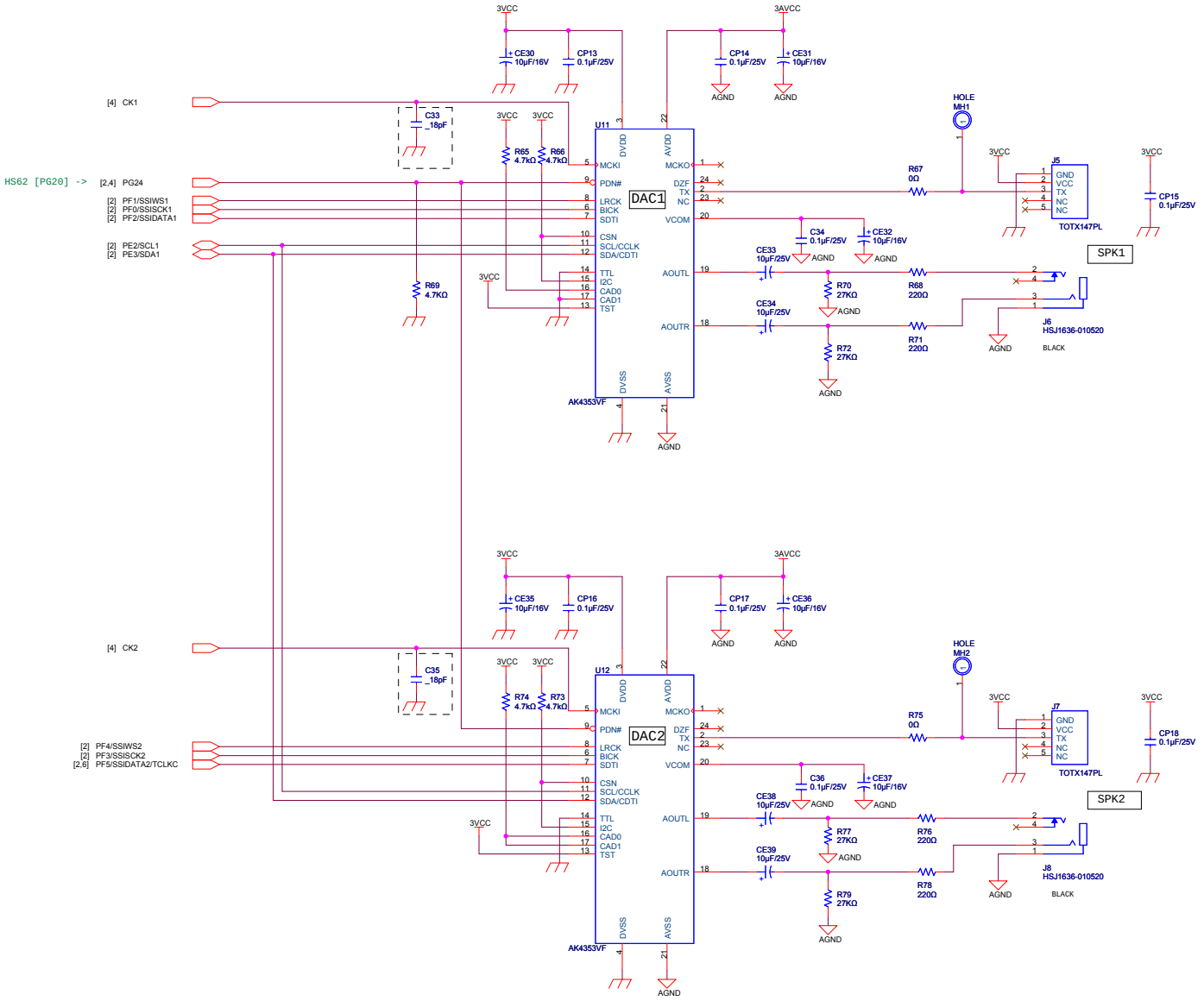
CHANGE			Renesas Solutions Corp.				M3A-HS64G01
			DRAWN	CHECKED	DESIGNED	APPROVED	Character LCD/SD Card Slot (3 / 10)
Ver. 1.00B		SCALE					DK30759
		DATE	09-03-02				

Audio Interface



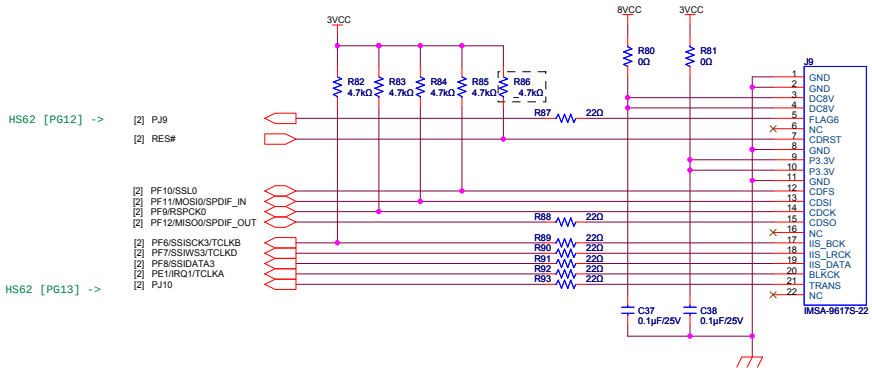
CHANGE			Renesas Solutions Corp.		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		Audio CODEC (4 / 10)
Ver. 1.00B		SCALE			DK30759
		DATE	09-03-02		

Audio DAC

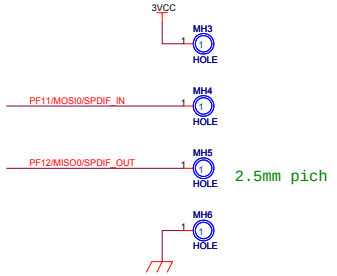


CHANGE			Renesas Solutions Corp.				M3A-HS64G01	
			DRAWN	CHECKED	DESIGNED	APPROVED	Audio D/A Converter	(5 / 10)
Ver. 1.00B	SCALE						DK30759	
	DATE	09-03-02						

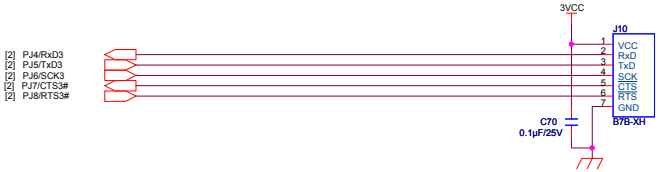
CD deck Interface



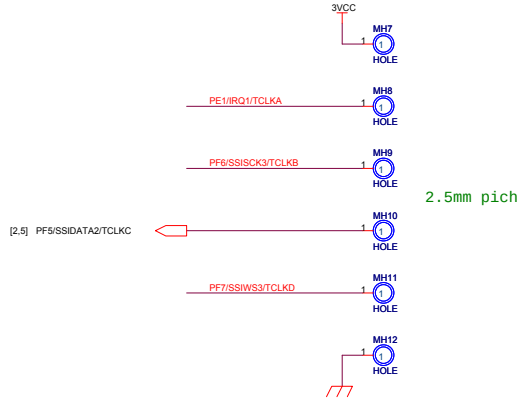
RSPDIF Through Hole.



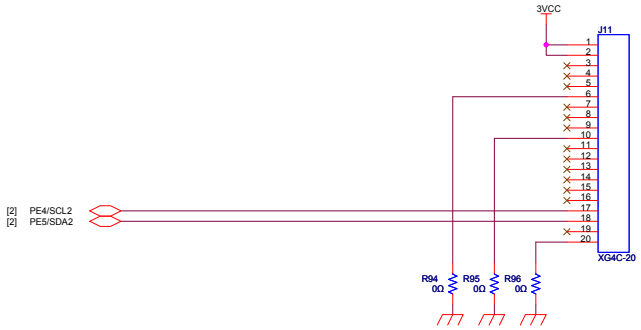
UART Interface



Rotary Encoder Through Hole.

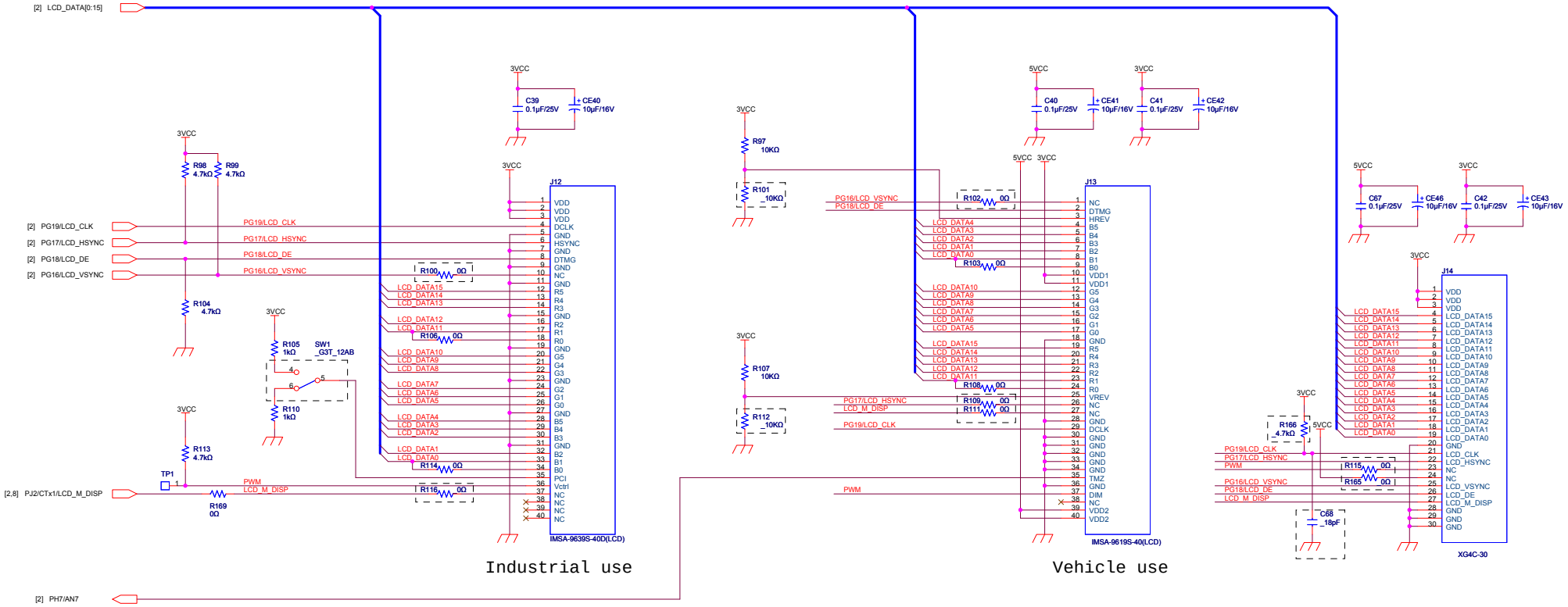


IIC Interface

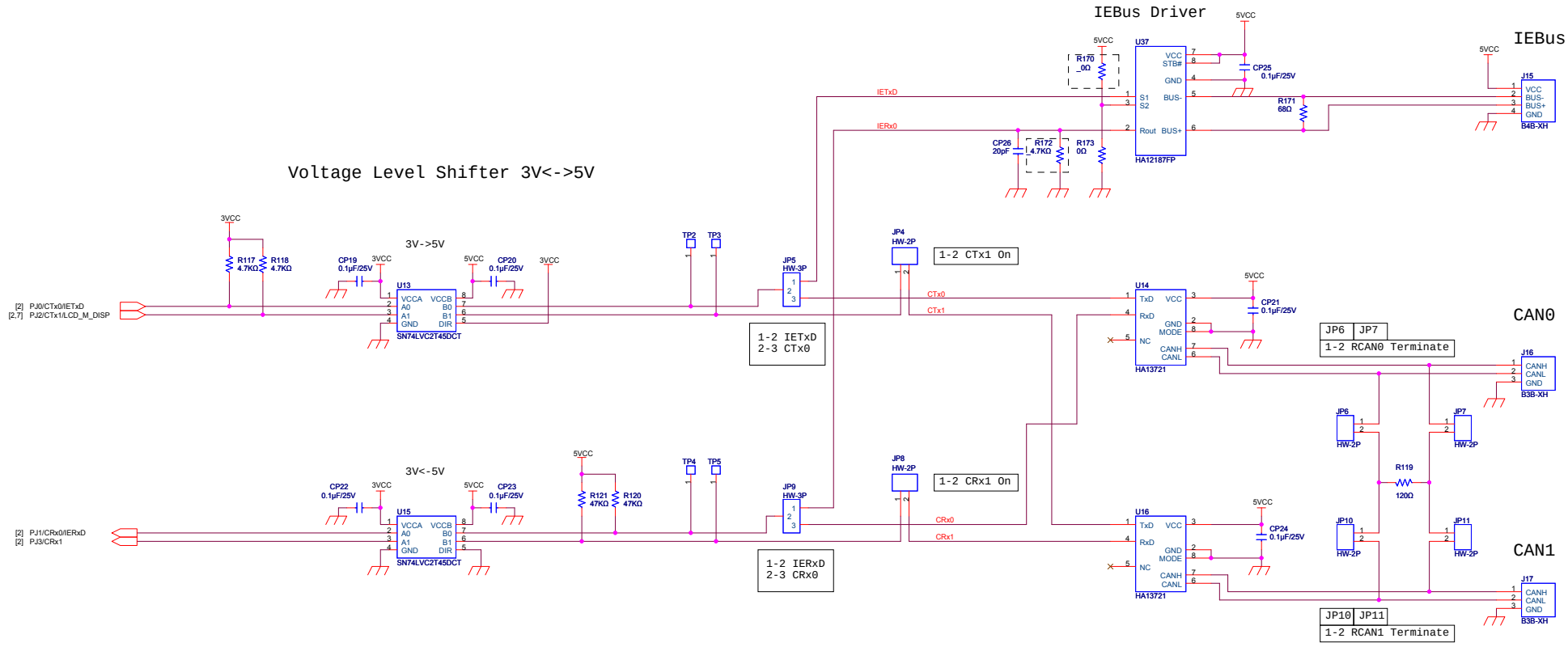


CHANGE					
Ver. 1.00B		Renesas Solutions Corp.			M3A-HS64G01
		DRAWN	CHECKED	DESIGNED	APPROVED	CD/UART/IIC/RSPDIF/Rotary Enc. (6 / 10)
	SCALE					
	DATE 09-03-02					DK30759

TFT LCD Module Interface

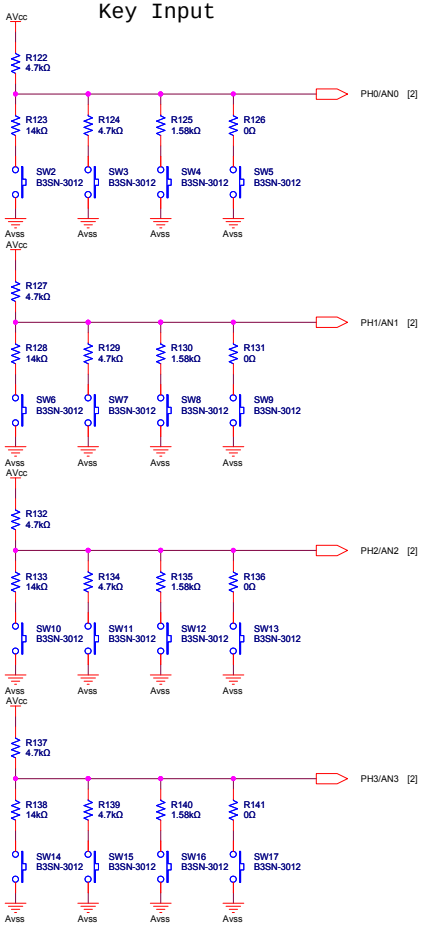


CHANGE			Renesas Solutions Corp.		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		LCD Module Connector
Ver. 1.00B		SCALE			(7 / 10)
		DATE	09-03-02		DK30759

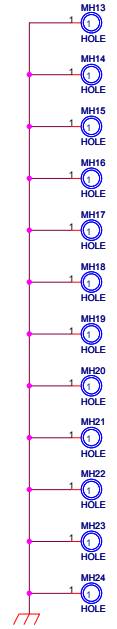


CHANGE						
Ver. 1.00B		Renesas Solutions Corp.				M3A-HS64G01
		DRAWN	CHECKED	DESIGNED	APPROVED	CAN/IEBus (8 / 10)
	SCALE					
	DATE 09-03-02					DK30759

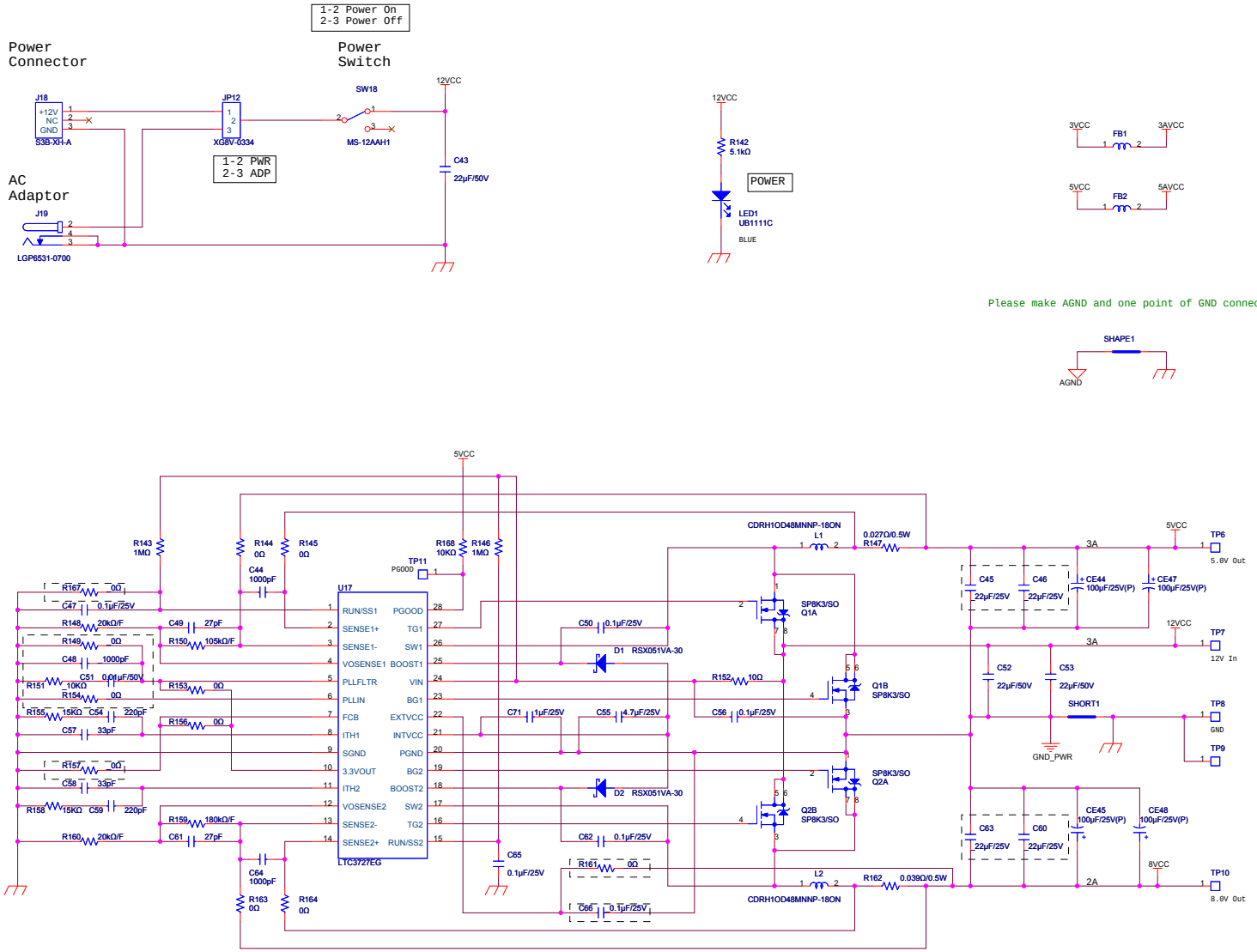
Key Input



Board fixed hole.



CHANGE						
Ver. 1.00B			Renesas Solutions Corp.			M3A-HS64G01
	SCALE		DRAWN	CHECKED	DESIGNED	APPROVED	Key Input (9 / 10)
	DATE	09-03-02					DK30759



CHANGE			Renesas Solutions Corp.		M3A-HS64G01
			DRAWN / CHECKED / DESIGNED / APPROVED		Power Generate (10 / 10)
Ver. 1.00B		SCALE			DK30759
		DATE	09-03-02		

SH7264 Optional board M3A-HS64G02 SCHEMATICS

Note:

⏚ Digital GND (GND)

⏚ Analog GND (AVSS)

⏚ Analog GND (AGND1,AGND2)

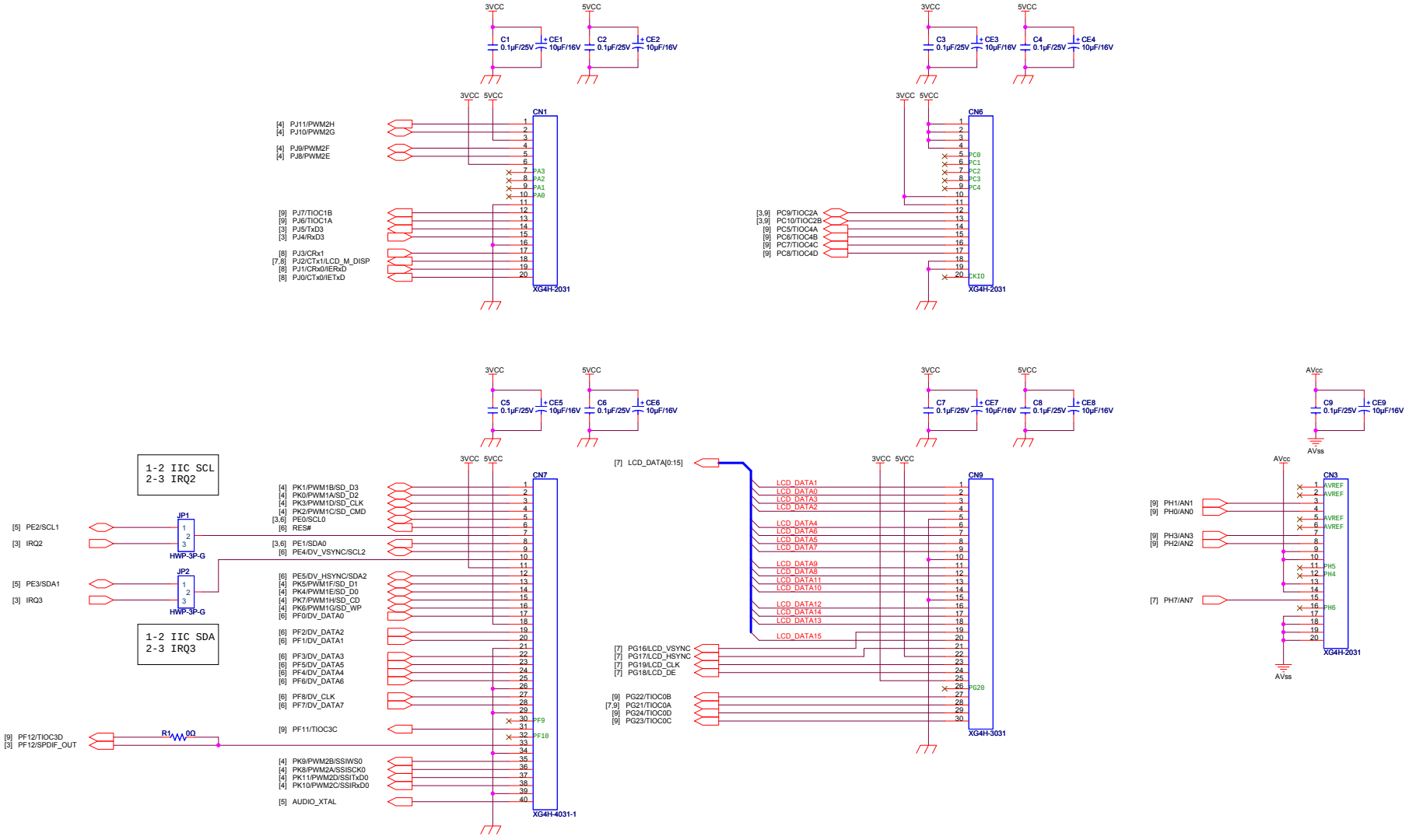
[ ] Not mounted

12VCC = Digital 12V Power in
8VCC = Digital 8V for CD
5VCC = Digital 5V
3VCC = Digital 3.3V
3AVCC1 = Analog 3.3V for Audio DAC
3AVCC2 = Analog 3.3V for Video Decoder
AVcc = Analog 3.3V for Key Input
MCVCC = Digital 3.3V / 5V for SD

R = Fixed Resistors
C = Ceramic Caps
CP = Decoupling Caps
CE = Electrolytic Caps (Tantal / Electric)

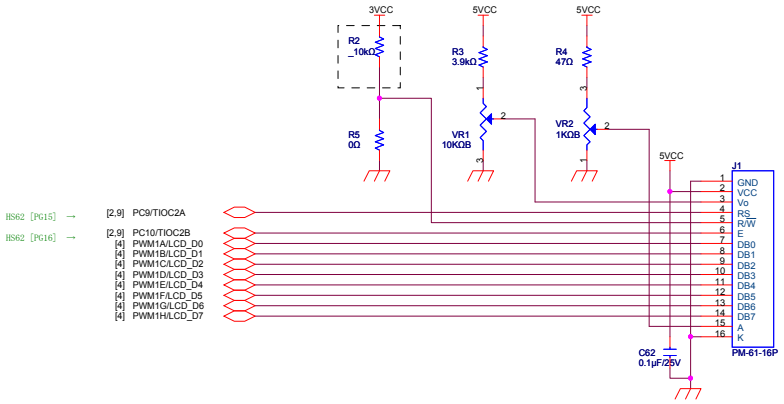
CHANGE							
Ver. 1.00B	SCALE		Renesas Solutions Corp.				M3A-HS64G02
	DATE	09-03-02	DRAWN	CHECKED	DESIGNED	APPROVED	INDEX (1 / 10)
							DK30762

SH7264 Extension Connector



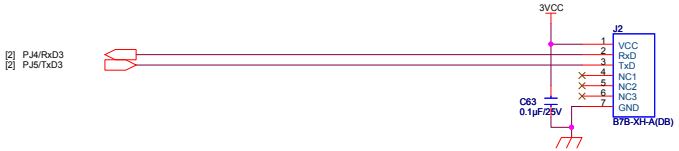
CHANGE			Renesas Solutions Corp.				M3A-HS64G02	
			DRAWN	CHECKED	DESIGNED	APPROVED	CPU Board Stack Connector	(2 / 10)
Ver. 1.00B		SCALE					DK30762	
		DATE	09-03-02					

Character Type LCD Connector

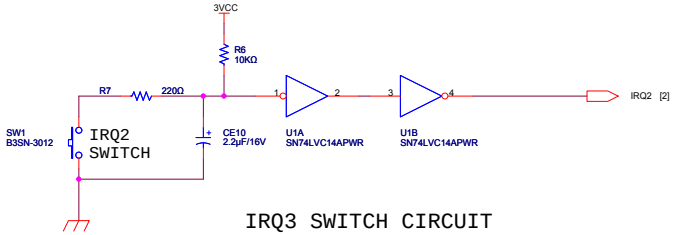


RSPDIF Through Hole.

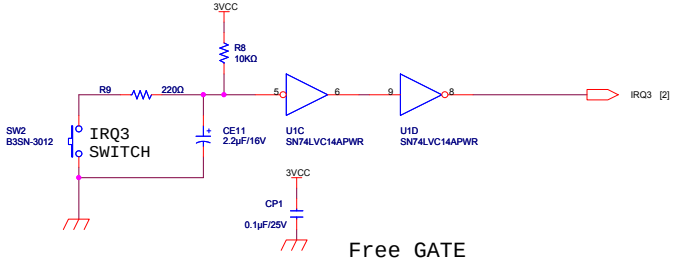
UART Interface



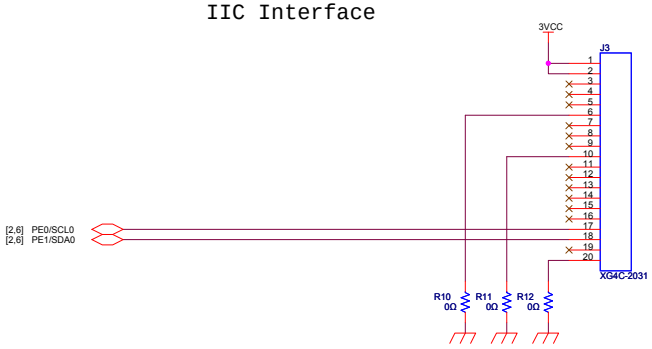
IRQ2 SWITCH CIRCUIT



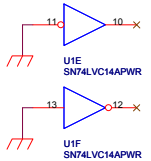
IRQ3 SWITCH CIRCUIT



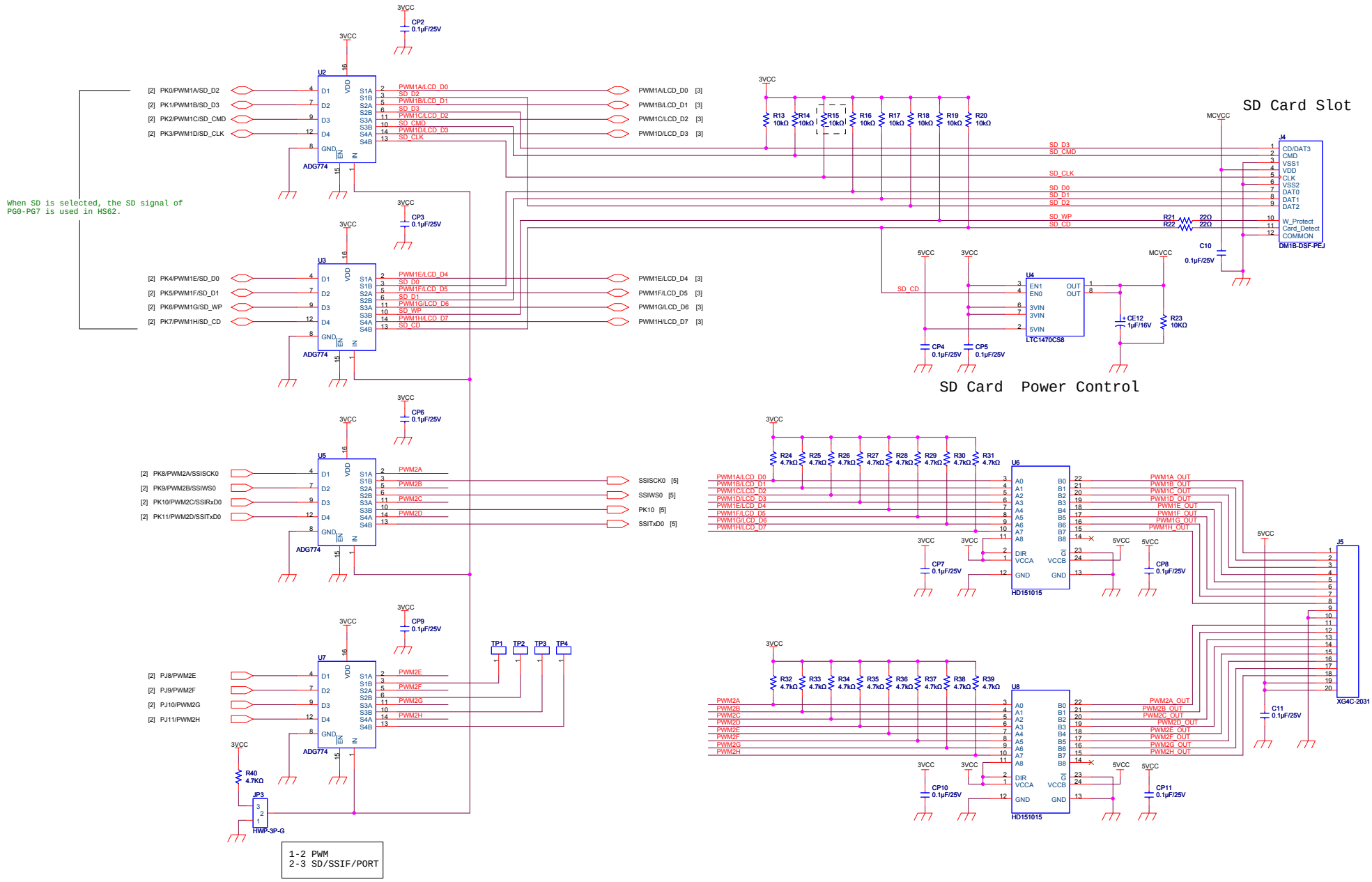
IIC Interface



Free GATE



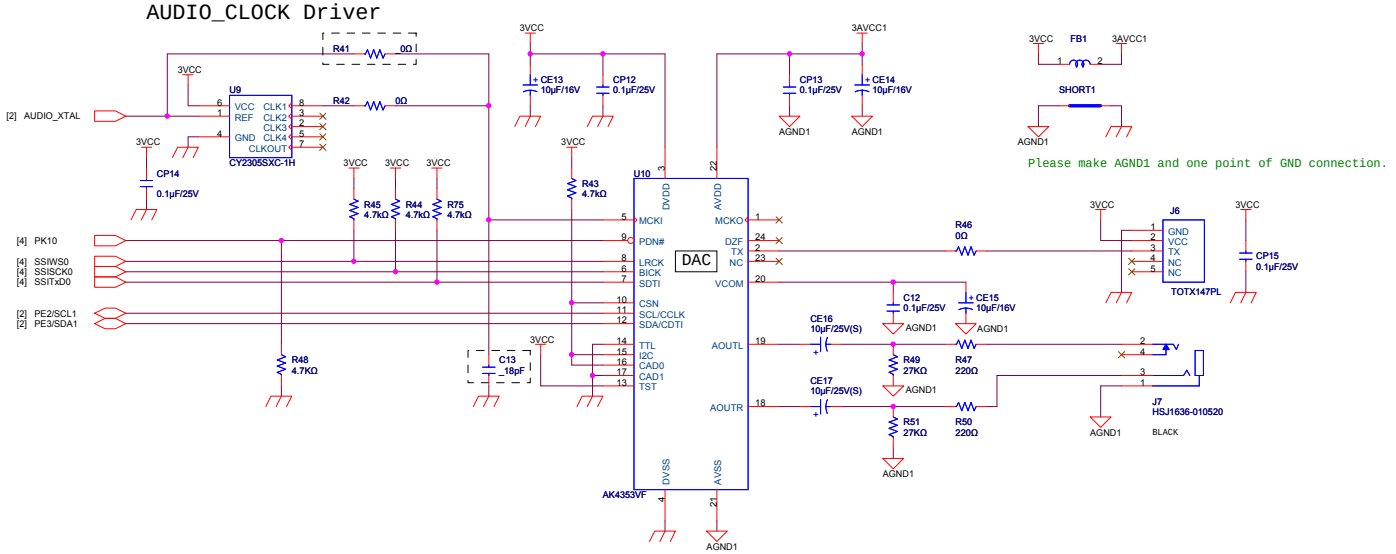
CHANGE			Renesas Solutions Corp.				M3A-HS64G02
			DRAWN	CHECKED	DESIGNED	APPROVED	Character LCD/UART/IIC/IRQ (3 / 10)
Ver. 1.00B		SCALE					DK30762
		DATE	09-03-02				



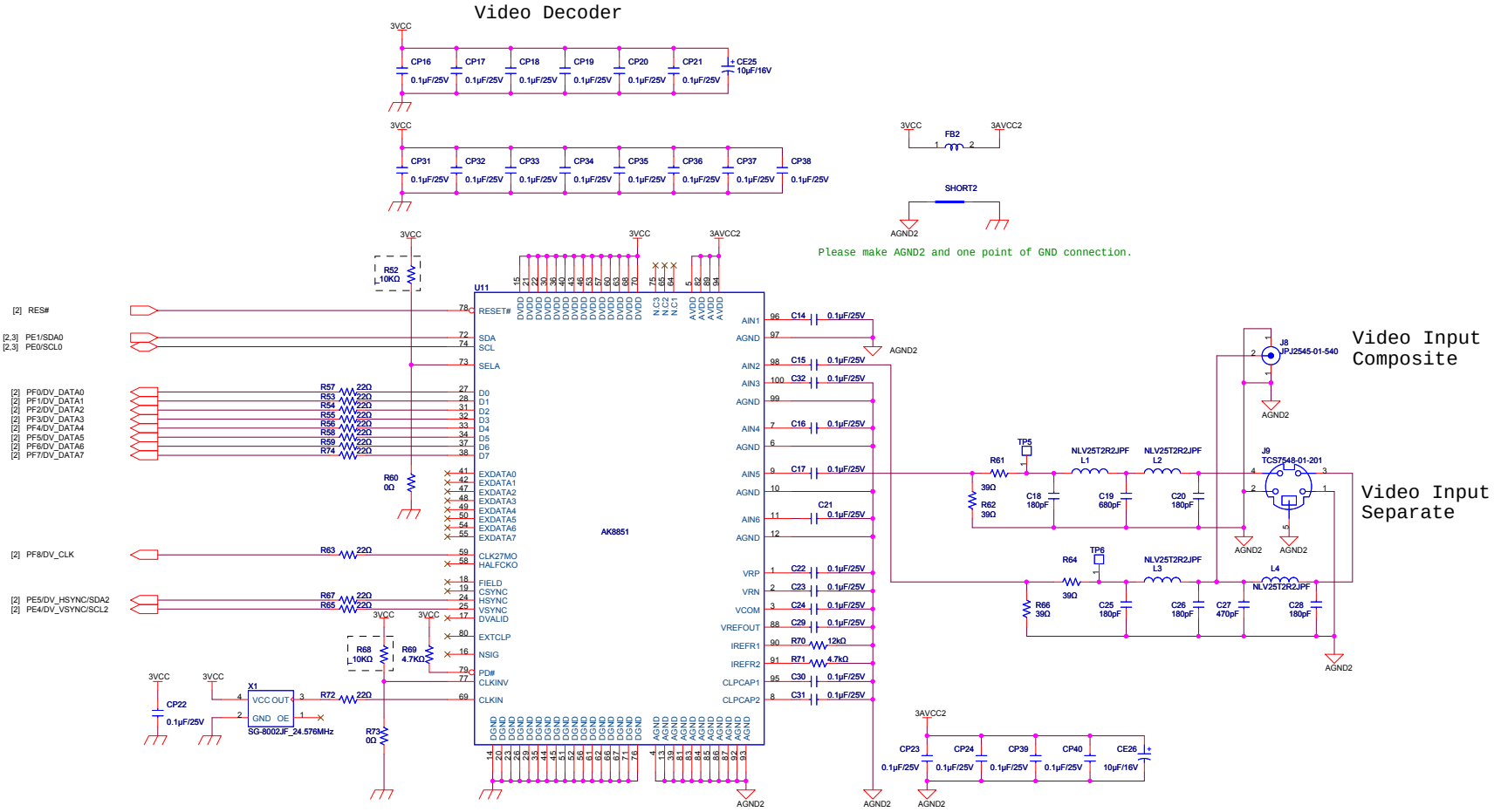
CHANGE			Renesas Solutions Corp.		M3A-HS64G02
			DRAWN / CHECKED / DESIGNED / APPROVED		SD Card Slot/PWM (4 / 10)
Ver. 1.00B		SCALE			DK30762
		DATE	09-03-02		

Audio Interface

AUDIO_CLOCK Driver

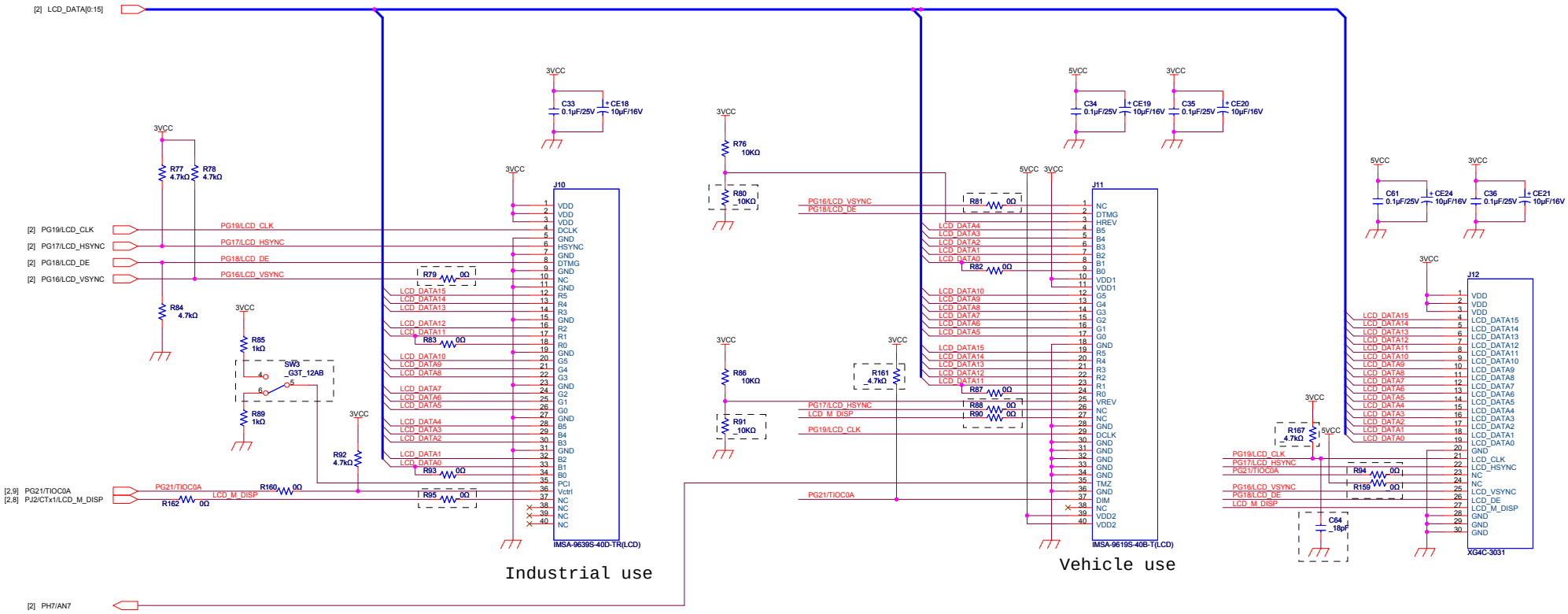


CHANGE			Renesas Solutions Corp.				M3A-HS64G02
			DRAWN	CHECKED	DESIGNED	APPROVED	Audio D/A Converter
Ver. 1.00B	SCALE						(5 / 10)
	DATE	09-03-02					DK30762



CHANGE			Renesas Solutions Corp.		M3A-HS64G02
			DRAWN / CHECKED / DESIGNED / APPROVED		Video Decoder (6 / 10)
Ver. 1.00B		SCALE			DK30762
		DATE	09-03-02		

TFT LCD Module Interface



CHANGE			Renesas Solutions Corp.		M3A-HS64G02
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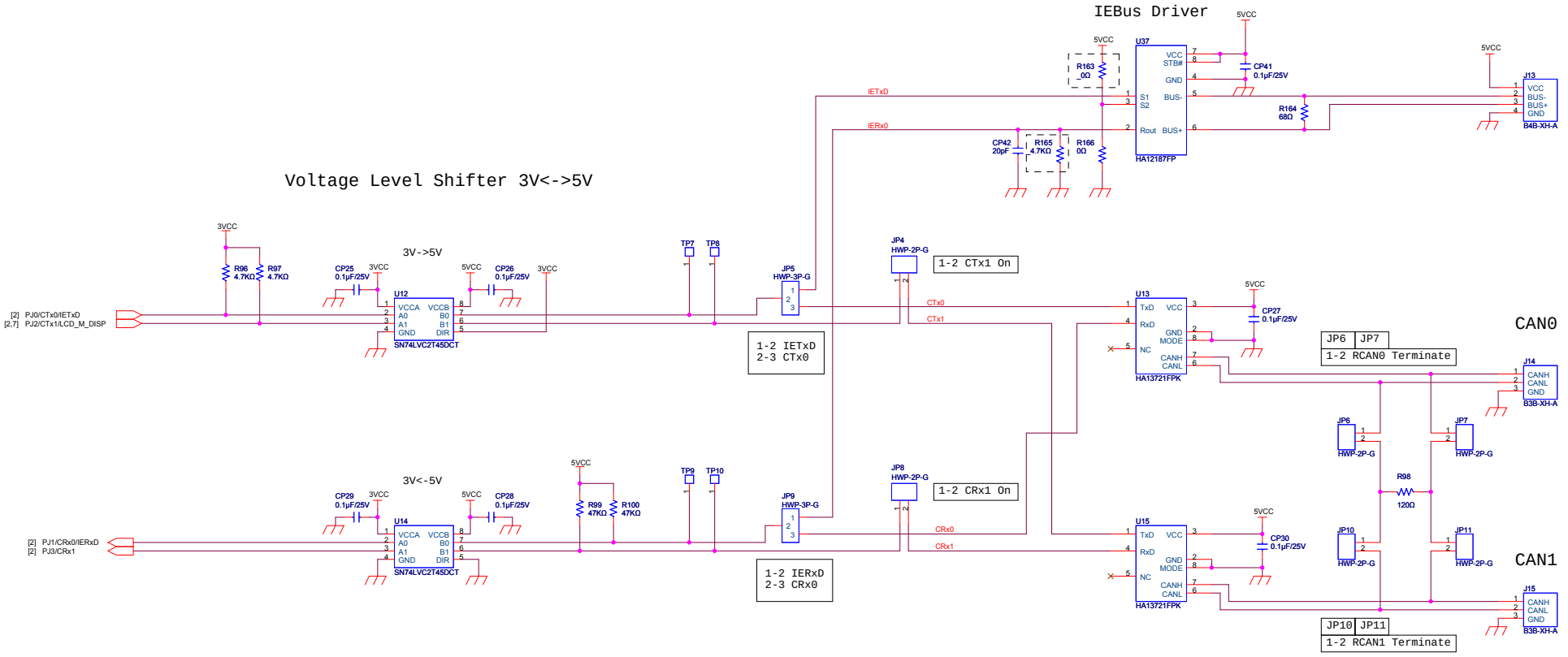
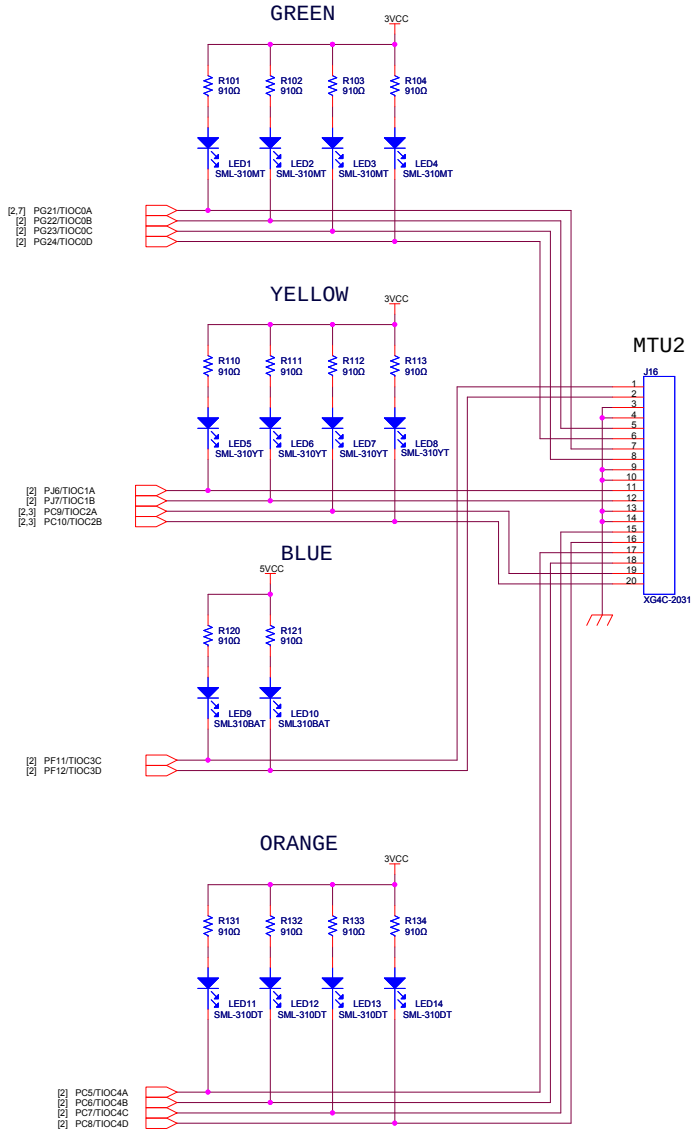
Ver. 1.00B		SCALE			DK30762
		DATE	09-03-02		

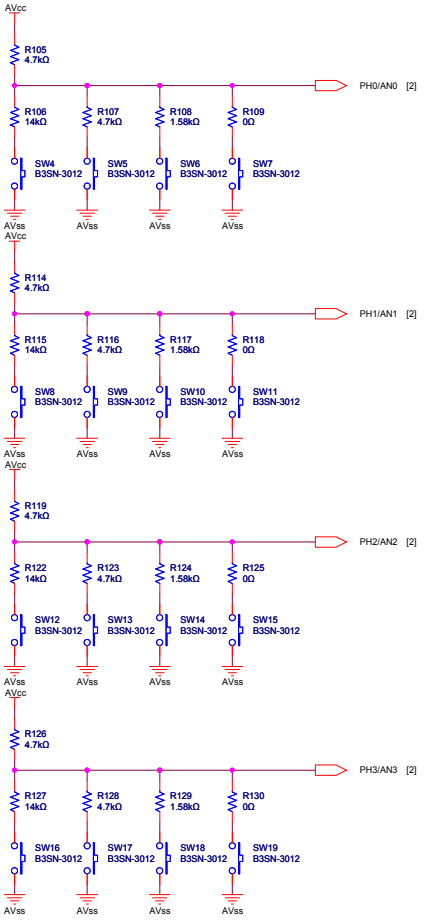


CHANGE	Ver. 1.00B	SCALE		Renesas Solutions Corp.		M3A-HS64G02
		DATE	09-03-02	DRAWN / CHECKED / DESIGNED / APPROVED		CAN/IEBus (8 / 10)
						DK30762

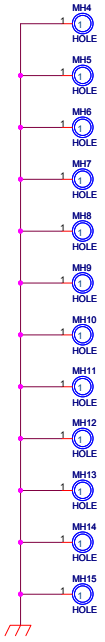
LED



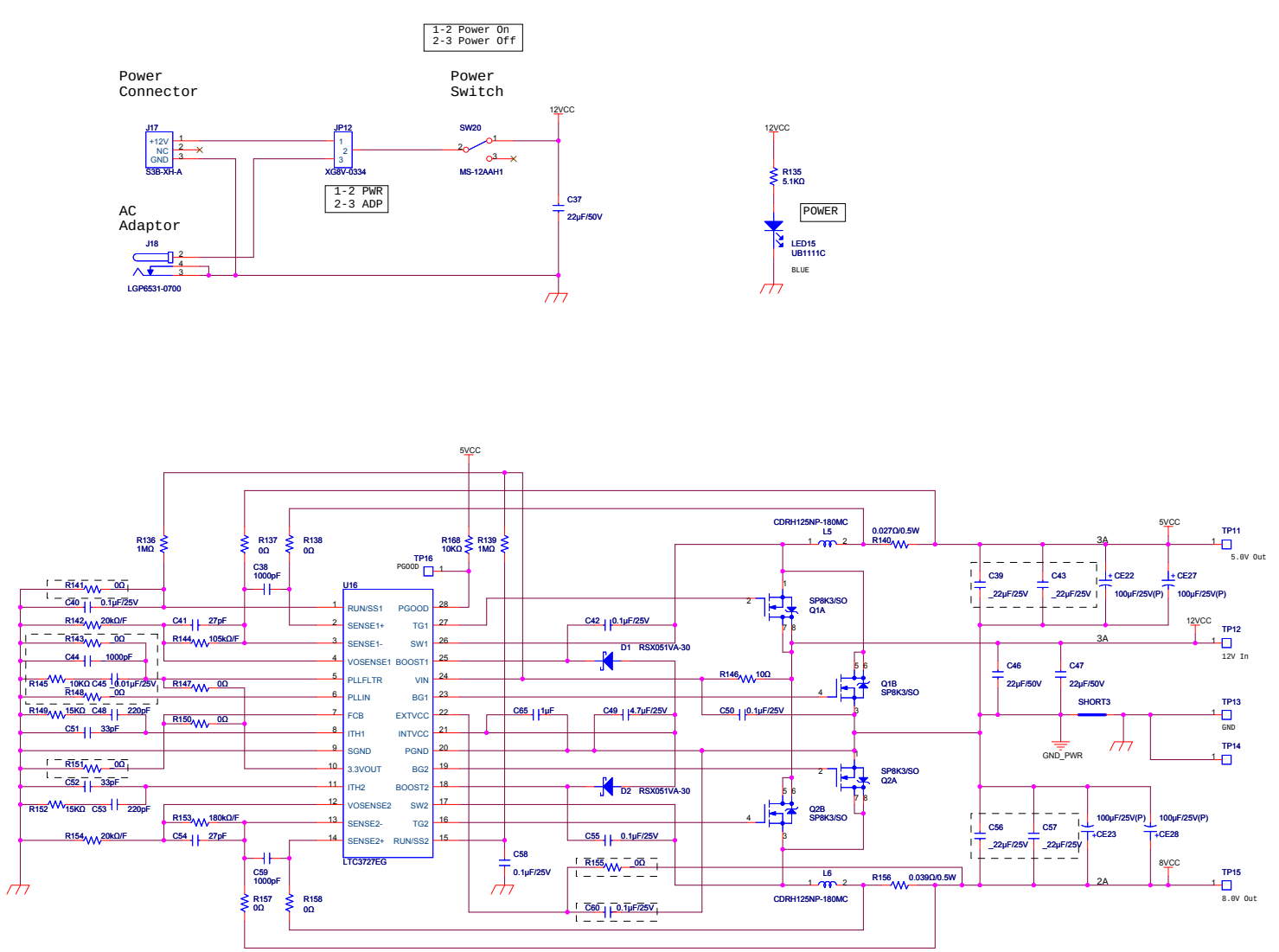
Key Input



Board fixed hole.



CHANGE					
Ver. 1.00B		Renesas Solutions Corp.			M3A-HS64G02
	SCALE	DRAWN	CHECKED	DESIGNED	APPROVED	LED/Key Input
	DATE 09-03-02					(9 / 10)
						DK30762



CHANGE			Renesas Solutions Corp.				M3A-HS64G02	
			DRAWN	CHECKED	DESIGNED	APPROVED	Power Generate	(10 / 10)
Ver. 1.00B		SCALE					DK30762	
		DATE	09-03-02					

Revision History	SH7267 CPU Board R0K572670C000BR User's Manual

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 18, 2010	-	First edition issued

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