User's Manual

32

SH7269 VDC4 Board

R0K572690B000BR

User's Manual

Renesas 32-Bit RISC Microcomputer
SuperH™ RISC engine Family / SH7260 Series

Rev. 1.20

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About This Manual

1. Purpose and Target Readers

This manual is designed to provide the user of this board with an understanding of the function and the operating specification of this evaluation board. A basic knowledge of electrical circuits, logical circuits, and microcomputers is necessary in order to use this manual.
This manual comprises the product outline, functional specification, and operational specification.

Carefully read all notes in the manual to use this evaluation board. These notes occur within the body of the text.

The Revision History summarizes primary modifications and additions to the previous versions. Refer to the text of the manual for details.

The following documents apply to the SH7269 VDC4 Board R0K572690B000BR.

Document Type	Description	Document Title	Document No.
User's Manual	Explanation of functional specification (installed devices, memory maps, electrical characteristics, etc), operational specification (connectors and switches)	SH7269 VDC4 Board R0K572690B000BR User's Manual	This publication

The following documents apply to the SH7269 group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics website.

Document Type	Description	Document Title	Document No.
Hardware manual	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to application notes for details on using peripheral functions	SH7268 Group SH7269 Group User's manual: Hardware	R01UH0048EJ
Software manual	Description of CPU instruction set	SH-2A, SH2A-FPU Software manual	REJ09B0051
Application note	Applications, sample programs	Available from the Renesas Electronics website.	
RENESAS TECHNICAL UPDATE	Product specifications, updates on documents, etc.		

2. Frequently Used Abbreviations and Acronyms

Abbreviation / acronym	English Description
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Registers
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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Table of Contents

1. Overview

1.1 Overview

The SH7269 VDC4 Board is the option board for the SH7269 CPU board. Its combination with the SH7269 CPU board enables the evaluation of function and performance assessment of the video display controller 4 (hereinafter called VDC4) embedded in the SH7269, and advanced development and its evaluation of the application software. The feature of the SH7269 VDC4 Board is described in the following section.

1.1.1 SH7269 VDC4 Board（Board type: R0K572690B000BR）

The SH7269 VDC4 Board includes four kinds of TFT-LCD panel connectors for its output evaluation. It also carries a video DAC to convert TFT-LCD panel control signal to analog RGB so to connect to a PC monitor and to evaluate its display function in the VDC4.
Additionally, it equips the connector for digital video input evaluation.

1.2 R0K572690B000BR Composition

Figure 1.2.1 shows the system composition of the SH7269 VDC4 Board with the R0K572690B000BR

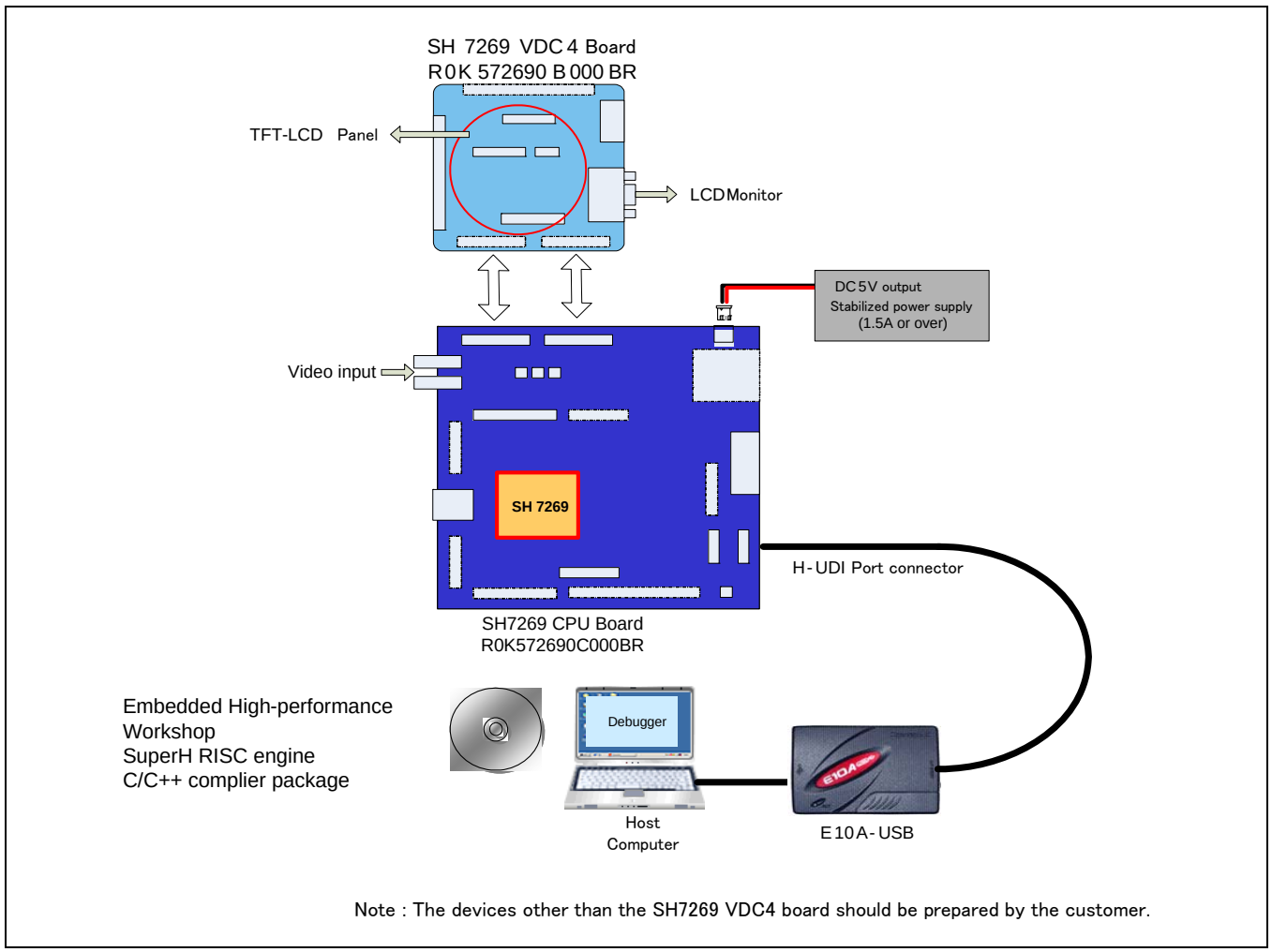

Figure 1.2.1 R0K572690B000BR System Composition

1.3 R0K572690B000BR External Specification

Table 1.3.1 describes the external specification of the R0K572690B000BR.

Table 1.3.1 List of External Specification for the R0K572690B000BR

No.	Item	Description
1	TFT-LCD panel output	includes four connectors for TFT-LCD panels ● for AA057QD01 by Mitsubishi Electric 5.7-inch QVGA TFT-LCD（RGB=6:6:6） ● for R0P7724LE0011RL by Renesas For an LDC evaluation board on SH7724 ● for TX09D55VM1CCA by Hitachi Displays 3.5-inch QVGA TFT-LCD（RGB=6:6:6） ● TFT-LCD connector for general purposes (40-pin MIL spec)
2	Analog RGB output	converts digital RGB signal for TFT-LCD to analog RGB by DAC (ADV7123) / by Analog Devices Analog RGB connector : 1 piece of D-sub15 pin connector
3	Digital RGB signal input	includes digital RGB signal input connector for SH7269 VDC4 Digital RGB input connector for general purposes : 40-pin of MIL spec
4	Switch	Video DAC setting switch : 1 piece (4 poles)
5	Dimension & Layer composition	● Dimension : 94X94mm ● Implement figuration : 4 layers / double-sided, thickness of board : 1.6mm Substrate composition : 1 piece

1.4 R0K572690B000BR Exterior Appearance

Figure1.4.1 shows the exterior appearance of the R0K572690B000BR.

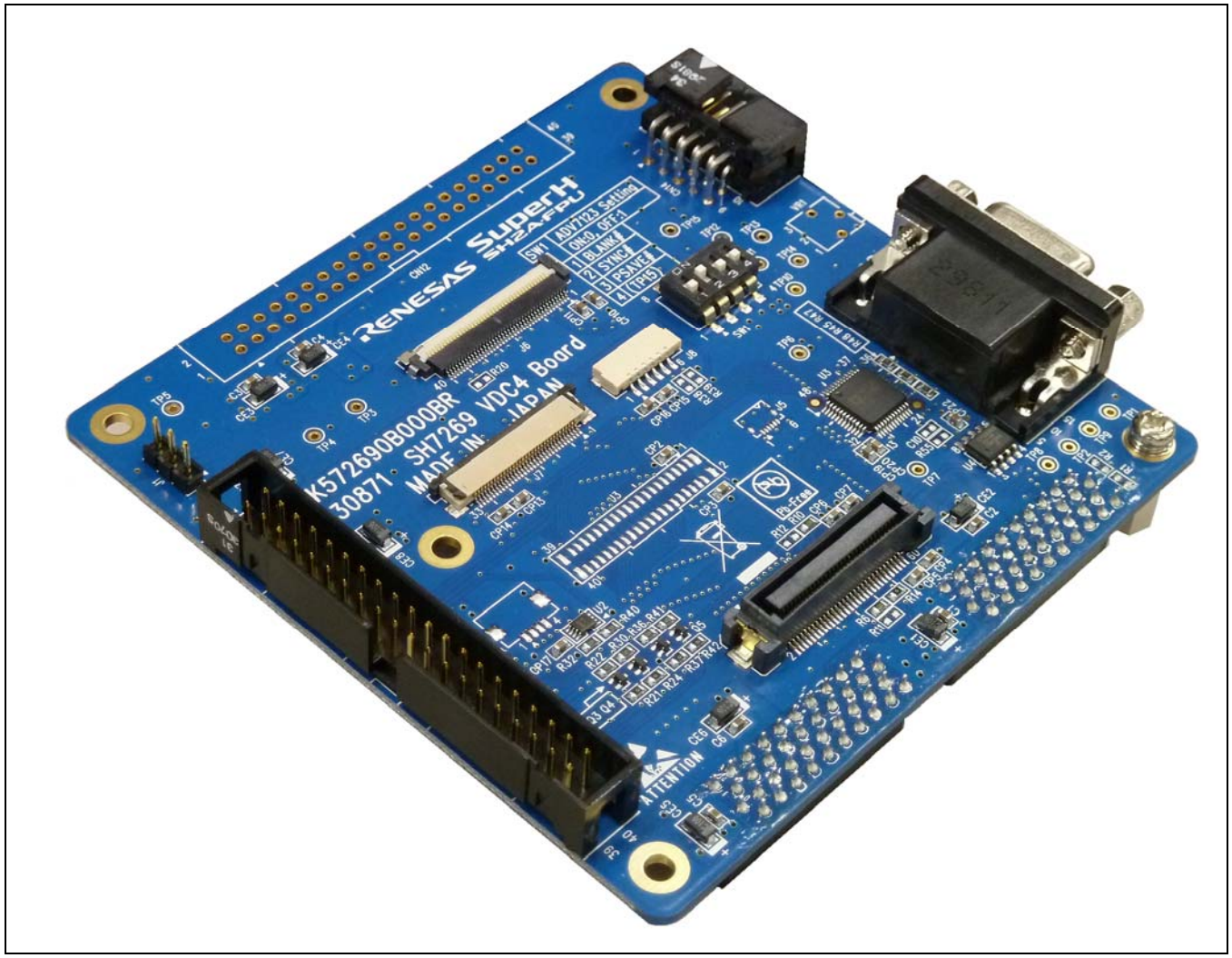

Figure1.4.1 R0K572690B000BR Exterior Appearance

1.5 Block Wiring Diagram for R0K572690B000BR

Figure1.5.1 shows the system block wiring diagram for the R0K572690B000BR.

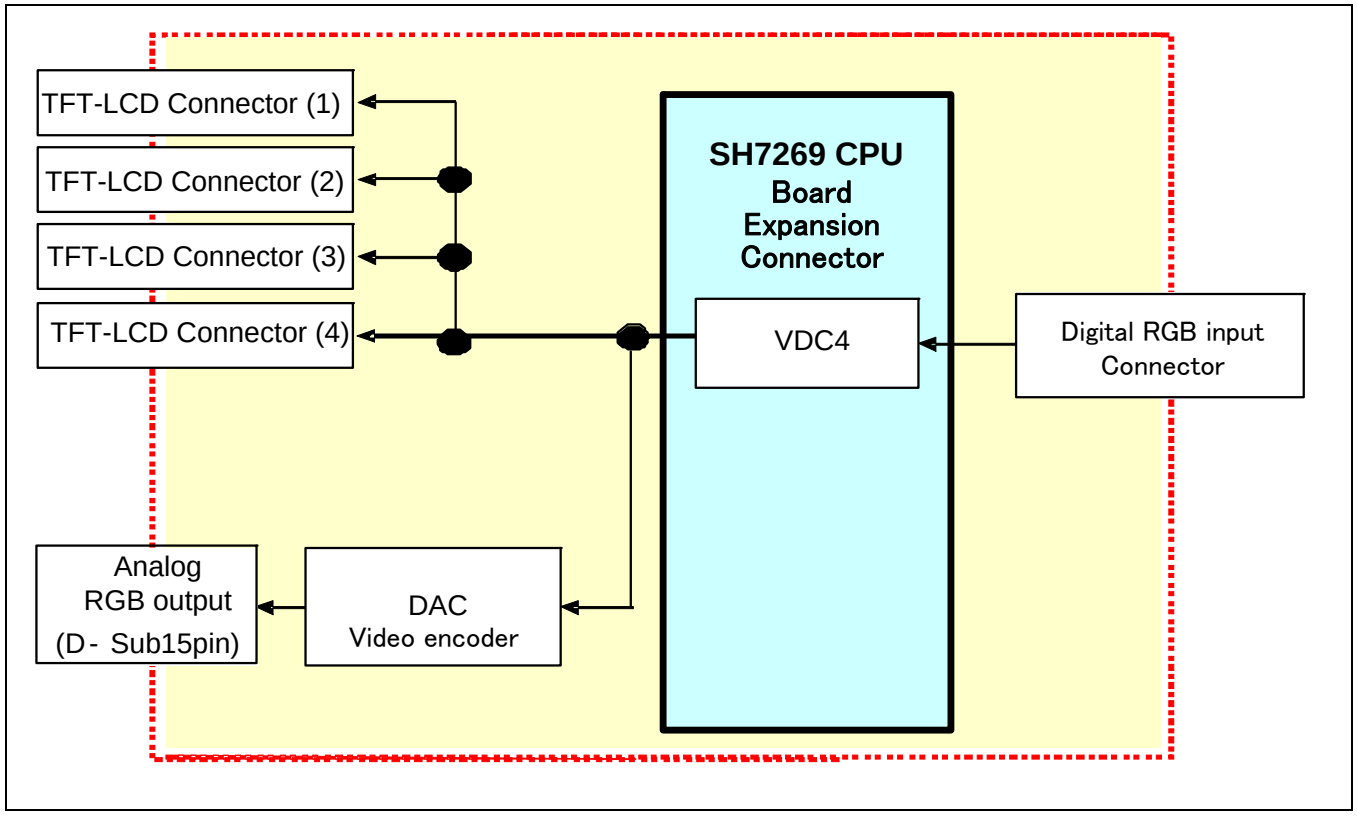

Figure1.5.1 System Block Wiring Diagram for the R0K572690B000BR

1.6 Main Parts for the R0K572690B000BR

Figure1.6.1 shows the exterior appearance of the R0K572690B000BR (PCB Diagram data).

<Top view of the component side>

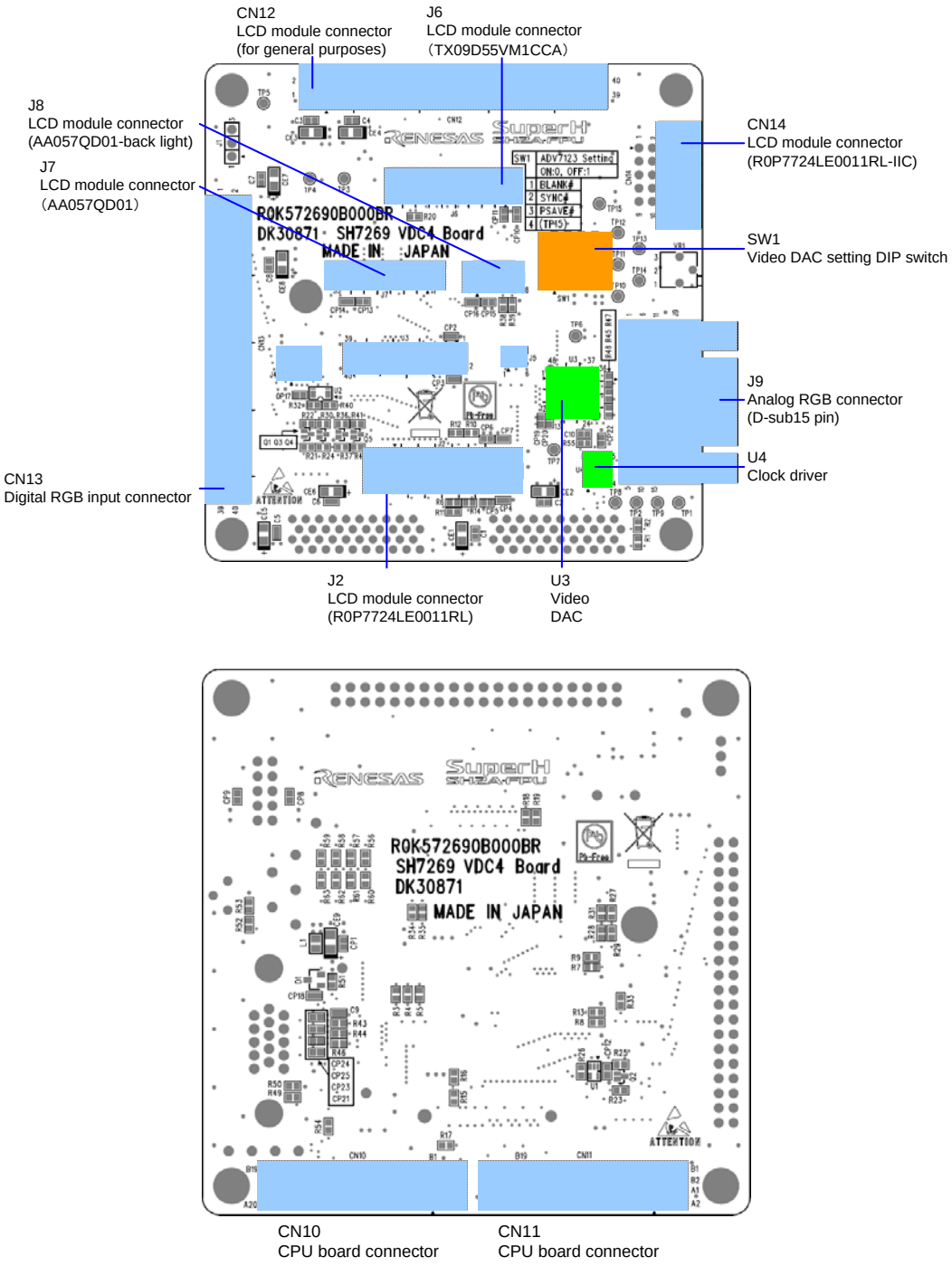

Figure1.6.1 PCB Diagram of the R0K572690B000BR

Table1.6.1 and Table1.6.2 list the main parts for the R0K572690B000BR.

Table1.6.1 Main Parts for the R0K572690B000BR (1): IC Parts

No	Item	Model No.	Maker	Description	Quantity
1	Video DAC	ADV7123KST140	Analog Devices	Triple 10-bit high speed video DAC	1
2	Clock buffer	CY2305SXC-1H	Cypress	Clock driver	1

Table1.6.2 Main Parts for the R0K572690B000BR (2): Connectors

No	Item	Model No.	Maker	Description	Quantity
1	Expansion connector	FX2C-40S-1.27DSA	HRS	for R0K572690C000BR	2
2	D-sub15 pin connector	XM4L-1542-132	OMRON	Analog RGB	1
3	TFT-LCD connector	8611-060S	KEL	for R0P7724LE0011RL	1
4	TFT-LCD connector	XG4C-1034	OMRON	for R0P7724LE0011RL-IIC	1
5	MIL spec connector	XG4C-4031	OMRON	For TFT-LCD output for general purposes / digital RBG input	2
6	TFT-LCD connector	08 6260 033 340 829+	KYOCERA ELCO	for AA057QD01	1
7	TFT-LCD connector	FI-S6P-HFE	JAE	for AA057QD01 back light	1
8	TFT-LCD connector	FA5S040HP1	JAE	for TX09D55VM1CCA	1

1.7 Absolute Maximum Rating

Table1.7.1 lists the absolute maximum rating for the R0K572690B000BR.

Table1.7.1 Absolute Maximum Rating for the R0K572690B000BR

Code	Item	Rated value	Description
VCC	5V series source voltage	−0.3V to 6.0V	VSS scale
3VCC	3.3V series source voltage	−0.3V to 4.6V	VSS scale
Topr	Operating ambient temperature	−10C to 55C	No condensation / No corrosive gas surrounding
Tstr	Preserved ambient temperature	−20C to 60C	No condensation / No corrosive gas surrounding

Note : “Operating ambient temperature” is the air temperature just next to the board.

1.8 Operating Condition

Table1.8.1 lists the operating condition for the R0K572690B000BR.

Table1.8.1 Operating Condition for the R0K572690B000BR

Code	Item	Rated value	Description
VCC	5V series source voltage	4.75V to 5.25V	VSS scale
3VCC	3.3V series source voltage	3.0V to 3.6V	VSS scale
-	Maximum consumption power on the board	1.5A or less	
Topr	Operating ambient temperature	0C to 40C	No condensation / No corrosive gas surrounding

Note : • The condition is with connection to the SH7269 CPU board (R0K572690C000BR) .
• “Operating ambient temperature” is the air temperature just next to the board.

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2. Functional Specification

2.1 Functional Outline

Table 2.1.1 lists the functional modules for the R0K572690B000BR.

Table 2.1.1 R0K572690B000BR Functional Modules

Table	Function	Description
2.2	CPU	● SH7269 pin for R0K572690B000BR
2.3	TFT-LCD	includes four connectors for TFT-LCD panels ● ffor AA057QD01 by Mitsubishi Electric 5.7 inches / QVGA TFT-LCD（RGB=6:6:6） ● for R0P7724LE0011RL by Renesas For an LDC evaluation board on SH7724 ● for TX09D55VM1CCA by Hitachi Displays 3.5 inches / QVGA TFT-LCD（RGB=6:6:6） ● TFT-LCD connector for general purposes：40-pin MIL spec
2.4	Analog RGB signal output interface	Converts digital RGB signal for TFT-LCD to analog RGB signal by video DAC (ADV7123) / by Analog Devices ● Analog RGB connector : 1 piece of D-sub15 pin connectedor
2.5	Digital RGB signal input interface	includes a digital RGB signal input connector for SH7269 VDC4 ● Digital RGB input connector for general purposes : 40-pin MIL spec
2.6	Clock module	● Controls the system clock ● Controls the peripheral I/O clock
2.7	Power supply module	● Controls the power supply for the R0K572690B000BR
―	Operational specification	● Connectors / Switches The details are in Chapter 3

2.2 CPU

2.2.1 SH7269 Features

R0K572690C000BR includes 32-bit RISC micro computer, SH7269 which runs with a maximum clock frecuency of 266.67MHz.

2.2.2 The SH7269 Pins used on the R0K572690B000BR

Table2.2.1 to Table2.2.11 list the SH7269 pins used on the R0K572690B000BR.

Table2.2.1 Pins Used (1)

Pin	Name	Symbol	Description	Expansion Connector	Remarks
1	PC1 / RD#	RD#	Connected to NOR flash memory OE# pin	#CN6, 6	
2	PVcc				
3	PC2 / RD/WR# / SCK6	RD/WR#	Connected to SDRAM WE# pin	CN6,7	
4	PC3 / WE0#/DQMLL / RxD6	WE0#	Connectedo to NOR flash memory WE# pin	CN6,8	
		DQMLL	Connected to SDRAM DQML pin		
5	PC4 / WE1#/WE#/DQMLU / TxD6	DQMLU	Connected to SDRAM DQMU pin	CN6,9	
6	PC5 / RAS# / CRx0 / CRx0/CRx1/CRx2 / IRQ0	RAS#	Connected to SDRAM RAS# pin	–	SW6-1:OFF
		–	–	CN6,14	SW6-1:ON
7	PVcc				
8	PC6 / CAS# / SCK7 / CTx0 / CTx0&CTx1&CTx2	CAS#	Connected to SDRAM CAS# pin	–	SW6-1:OFF
		–	–	CN6,15	SW6-1:ON
9	Vss				
10	PC7 / CKE / RxD7 / CRx1 / CRx0/CRx1 / IRQ1	CKE	Connected to SDRAM CKE pin	–	SW6-1:OFF
		–	–	CN6,16	SW6-1:ON
11	Vcc				
12	PC8 / CS3# / TxD7 / CTx1 / CTx0&CTx1	CS3#	Connected to SDRAM CS# pin	–	SW6-1:OFF
		–	–	CN6,17	SW6-1:ON
13	PB1 / A1 / TIOC0A	A1	Address bus	CN4,28	
14	PB2 / A2 / TIOC0B	A2	Address bus	CN4,27	
15	PB3 / A3 / TIOC0C	A3	Address bus	CN4,26	
16	PJ14 / DV_DATA14 / LCD_DATA14 / PINT6 / PWM2G / TxD6	PWM2G	PWM output	CN11,A1	TTL level
		DV_DATA14	DV input		
		–	–	CN1,4	
17	PVcc				
18	PJ15 / DV_DATA15 / LCD_DATA15 / PINT7 / PWM2H / TxD7	PWM2H	PWM output	CN11,B1	TTLlevel
		DV_DATA15	DV input		
		–	–	CN1,2	
19	Vss				
20	PB4 / A4 / TIOC0D	A4	Address bus	CN4,25	
21	Vcc				
22	PJ16 / DV_DATA16 / LCD_DATA16 / RSPCK0 / TIOC0A / SIOFSCK	PJ16	Connected to SW6-5 as a user input port 1	CN11,B13	
		DV_DATA16	DV input		
23	PJ17 / DV_DATA17 / LCD_DATA17 / SSL00 / TIOC0B / SIOFSYNC	PJ17	Connected to SW6-6 as a user input port 2	CN11,B12	
		DV_DATA17	DV input		

Legend : .... : 3.3V system power supply, ... : 1.25V system power supply, ... : GND

Table2.2.2 Pins Used (2)

Pin	Name	Symbol	Description	Expansion Connector	Remarks
24	PJ18 / DV_DATA18 / LCD_DATA18 / MOSI0 / TIOC0C / SIOFTxD	PJ18	Connecteded to LED2 as a user input port 1	CN11,B8	
		DV_DATA18	DV input		
25	PB5 / A5 / TIOC1A	A5	Address bus	CN4,22	
26	PB6 / A6 / TIOC1B	A6	Address bus	CN4,21	
27	PVcc				
28	PB7 / A7 / TIOC2A	A7	Address bus	CN4,20	
29	Vss				
30	PB8 / A8 / TIOC2B	A8	Address bus	CN4,19	
31	Vcc				
32	PB9 / A9 / TIOC3A	A9	Address bus	CN4,18	
33	PB10 / A10 / TIOC3B	A10	Address bus	CN4,17	
34	PB11 / A11 / TIOC3C	A11	Address bus	CN4,14	
35	PB12 / A12 / TIOC3D	A12	Address bus	CN4,13	
36	PJ19 / DV_DATA19 / LCD_DATA19 / MISO0 / TIOC0D/ SIOFRxD / AUDIO_XOUT	PJ19	Connecteded to LED3 as a user input port 2	CN11,A12	
		DV_DATA19	DV input		
		–	–	CN7,40	
37	PVcc				
38	PJ20 / DV_DATA20 / LCD_DATA20 / LCD_TCON3 / IRQ0 / CRx2 / CRx0/CRx1/CRx2	–	–	CN7,8	JP9:1-2
		DV_DATA20	DV input	CN11,B4	JP9:2-3
		–	–	CN1,17	
39	Vss				
40	PB13 / A13 / QIO2_1 / SPBIO2_1	A13	Address bus	CN4,12	
		QIO2_1 / SPBIO2_1	Connected to serial flash memory2 IO2 pin		
41	Vcc				
42	PJ21 / DV_DATA21 / LCD_DATA21 / LCD_TCON4 / IRQ1 / CTx2 / CTx0&CTx1&CTx2	IRQ1	IRQ1 switch	–	JP8:1-2
		DV_DATA21	DV input	CN11,A14	JP8:2-3
		–	–	CN1,18	
43	PJ22 / DV_DATA22 / LCD_DATA22 / LCD_TCON5 / IRQ2 / CRx1 / CRx0/CRx1	DV_DATA22	DV input	CN11,B14	
		LCD_TCON5	Connected LCD module DE pin	CN9,24 CN10,B17	
44	PJ23 / DV_DATA23 / LCD_DATA23 / LCD_TCON6 / IRQ3 / CTx1 / CTx0&CTx1	DV_DATA23	DV input	CN11,A15	
		LCD_TCON6	Connected to LCD module M_DISP pin	CN1,18 CN10,B18	
45	PB14 / A14 / QIO3_1 / SPBIO3_1	A14	Address bus	CN4,11	
		QIO3_1 / SPBIO3_1	Connected to serial flash memory2 IO3 pin		
46	PB15 / A15 / QIO2_0 / SPBIO2_0	A15	Address bus	CN4,10	
		QIO2_0 / SPBIO2_0	Connected to serial flash memory1 IO2 pin		
47	PVcc				
48	PB16 / A16 / QIO3_0 / SPBIO3_0	A16	Address bus	CN4,9	
		QIO3_0 / SPBIO3_0	Connected to serial flash memory1 IO3 pin		
49	Vss				
50	PB17 / A17 / QSPCLK_0 / RSPCK0 / SPBCLK	A17	Address bus	CN4,6	
		QSPCLK_0 / RSPCK0 / SPBCLK	Connected to serial flash memory1 SCK pin		
51	Vcc				

Legend : .... : 3.3V system power supply, ... : 1.25V system power supply, ... : GND

Table2.2.3 Pins Used on (3)

Pin	Name	Symbol	Description	Expansion Connector	Remarks
52	PB18 / A18 / QSSL_0 / SSL00 / SPBSSL	A18	Address bus	CN4,5	JP4 open
		QSSL_0 / SSL00 / SPBSSL	Connected to serial flash memory1 CS pin	–	JP4:1-2
53	PB19 / A19 / QMO_0/QIO0_0 / MOSI0 / SPBMO_0/SPBIO0_0	A19	Address bus	CN4,4	
		QMO_0/QIO0_0 / MOSI0 / SPBMO_0/SPBIO0_0	Connected to serial flash memory1 S pin		
54	PB20 / A20 / QMI_0/QIO1_0 / MISO0 / SPBMI_0/SPBIO1_0	A20	Address bus	CN4,3	
		QMI_0/QIO1_0 / MISO0 / SPBMI_0/SPBIO1_0	Connected to serial flash memory1 SO pin		
55	Vss				
56	PB21 / A21 / CRx2 / IERxD	A21	Address bus	CN4,2	
57	Vcc				
58	PB22 / A22 / CTx2 / IETxD / CS4#	A22	Address bus	CN4,1	
59	PC0 / CS0# / MD_BOOT2	CS0#	Connected to NOR flash memory CE# pin	CN6,5	JP5:1-2
		MD_BOOT2	Connected to SW5-4 as boot mode input 2		JP5:2-3
60	PVcc				
61	CKIO	CKIO	Connected to SDRAM CLK pin	CN6,20	
62	Vss				
63	PA0 / MD_BOOT0	MD_BOOT0	Connected to SW5-2 as boot mode input 0	CN1,10	RES#:"L"
64	Vcc				
65	PA1 / MD_BOOT1	MD_BOOT1	Connected to SW5-3 as boot mode input 1	CN1,9	RES#:"L"
66	PJ28 / SSISCK5 / TIOC1B / RTS7#	–	–	CN7,22	
67	PJ29 / SSIWS5 / TIOC2A / IERxD	–	–	CN7,24	SW6-4:ON
				CN1,19	SW6-4:OFF
68	PJ30 / SSIDATA5 / TIOC2B / IETxD	–	–	CN7,23	SW6-4:ON
				CN1,20	SW6-4:OFF
69	PJ31 / DV_CLK	DV_CLK	DV input	CN11,B16	
		–	–	CN7,27	
70	PE0 / SCL0 / TCLKA / LCD_EXTCLK	–	–	CN7,5	
71	PE1 / SDA0 / TCLKB / AUDIO_CLK / DV_CLK	–	–	CN7,8	
72	PE2 / SCL1 / TCLKC / IOIS16# / DV_VSYNC	SCL1	Connected to EEPROM SCL pin	CN7,7	
		–	–		
73	PE3 / SDA1 / TCLKD / ADTRG# / DV_HSYNC	SDA1	Connected to EEPROM SDA pin	CN7,10	
		–	–		
74	PE4 / SCL2 / RxD4 / DV_VSYNC	DV_VSYNC	DV input	CN11,A17	
		–	–	CN7,9	
75	PE5 / SDA2 / RxD5 / DV_HSYNC	DV_HSYNC	DV input	CN11,B17	
		–	–	CN7,12	
76	PE6 / SCL3 / RxD6	–	–	CN6,12	
77	PE7 / SDA3 / RxD7	–	–	CN6,13	
78	PVcc				
79	NMI	NMI	Non-maskable interrupt	–	

Legend : .... : 3.3V system power supply, ... : 1.25V system power supply, ... : GND

Table2.2.4 Pins Used (4)

Pin	Name	Symbol	Description	Expansion Connector	Remarks
80	Vss				
81	ASEMD#	ASEMD#	ASE mode select	—	H-UDI
82	Vcc				
83	PLLVcc				
84	EXTAL	EXTAL	Connects a sysem external clock	—	13.33MHz
85	XTAL	XTAL	Open	—	
86	PLLVss				
87	PLLVss				
88	RES#	RES#	Reset input	CN7,6	
89	RTC_X1	RTC_X1	Connects a crystal oscillator for real time clock	—	32.768kHz
90	RTC_X2	RTC_X2		—	
91	USBDPVcc				
92	USBDPVss				
93	DM	DM	USB differential D- data	—	
94	DP	DP	USB differential D+ data	—	
95	VBUS	VBUS	VBUS input	—	
96	USBDVcc				
97	USBDVss				
98	REFRIN	REFRIN	Reference input	—	Connects a 5.6kΩ±1% resister
99	USBAVss				
100	USBAPVcc				
101	USBAVcc				
102	USBAVss				
103	USBUVcc				
104	USBUVss				
105	USB_X1	USB_X1	Connects a USB external clock	—	48MHz
106	USB_X2	USB_X2	Open	—	
107	PVcc				
108	VIDEO_X1	VIDEO_X1	Connects a digital video decoder external clock	—	27MHz
109	VIDEO_X2	VIDEO_X2	Open	—	
110	Vss				
111	DVAVcc				
112	DVAVss				
113	VIN1	VIN1	Analog video signal input	CN10,A19	
114	VIN2	VIN2	Analog video signal input	CN10,B20	
115	VRT	VRT	TOP reference voltage	—	
116	VRB	VRB	BOTTOM reference voltage	—	
117	BIAS	BIAS	Reference voltage	—	Connects a 24kΩ±1% resister
118	PH0 / AN0 / PINT0	—	—	CN3,4	
119	PH1 / AN1 / PINT1	—	—	CN3,3	
120	PH2 / AN2 / PINT2	—	—	CN3,8	
121	PH3 / AN3 / PINT3	—	—	CN3,7	
122	PH4 / AN4 / PINT4	—	—	CN3,12 CN11,B18	
123	PH5 / AN5 / PINT5 / LCD_EXTCLK	—	—	CN3,11 CN11,A19	
124	AVss				

Legend : .... : 3.3V system power supply, ... : 1.25V system power supply, ... : GND

Table2.2.5 Pins Used (5)

Pin	Name	Symbol	Description	Expansion Connector	Remarks
125	PH6 / AN6 / PINT6	–	–	CN3,16	
				CN11,B19	
126	AVcc				
127	PH7 / AN7 / PINT7	–	–	CN3,15	
				CN11,A20	
128	AVref				
129	TRST#	TRST#	Initialization signal input pin	–	H-UDI
130	ASEBRKAK#/ASEBRK#	ASEBRKAK#	Break mode acknowledge	–	H-UDI
		ASEBRK#	Break request		
131	TDO	TDO	Test data output	–	H-UDI
132	TDI	TDI	Test data input	–	H-UDI
133	TMS	TMS	Test mode select	–	H-UDI
134	TCK	TCK	Test clock	–	H-UDI
135	Vss				
136	PG0 / D16 / LCD_DATA0 / IRQ0 / TIOC0A	LCD_DATA0	Connected to LCD module D0 pin	CN9,2 CN10,A1	B0
137	Vcc				
138	PG1 / D17 / LCD_DATA1 / IRQ1 / TIOC0B	LCD_DATA1	Connected to LCD module D1 pin	CN9,1 CN10,B1	B1
139	Vss				
140	PG2 / D18 / LCD_DATA2 / IRQ2 / TIOC0C	LCD_DATA2	Connected to LCD module D2 pin	CN9,4 CN10,A2	B2
141	PVcc				
142	AUDIO_X2	AUDIO_X2	Open	–	
143	AUDIO_X1	AUDIO_X1	Connects an audio external clock	–	11.2896MHz
144	Vss				
145	PG3 / D19 / LCD_DATA3 / IRQ3 / TIOC0D	LCD_DATA3	Connected to LCD module D3 pin	CN9,3 CN10,B2	B3
146	Vcc				
147	PG4 / D20 / LCD_DATA4 / IRQ4 / TIOC1A	LCD_DATA4	Connected to LCD module D4 pin	CN9,6 CN10,B3	B4
148	PG5 / D21 / LCD_DATA5 / IRQ5 / TIOC1B	LCD_DATA5	Connected to LCD module D5 pin	CN9,8 CN10,A4	B5
149	PG6 / D22 / LCD_DATA6 / IRQ6 / TIOC2A	LCD_DATA6	Connected to LCD module D6 pin	CN9,7 CN10,B4	B6
150	PG7 / D23 / LCD_DATA7 / IRQ7 / TIOC2B	LCD_DATA7	Connected to LCD module D7 pin	CN9,9 CN10,A5	B7
151	PJ0 / DV_DATA0 / LCD_DATA0 / SD_CD_1 / PWM1A	DV_DATA0	DV input	CN11,A6	
		PJ0	Connected to character LCD DB7 pin	CN7,15	SW6-3:OFF
		SD_CD_1	Connected to SD card slot CD pin		
		–	Connected to C/A converter1 (U11) BICKI pin	CN7,17	SW6-3:ON
152	PVcc				
153	PJ1 / DV_DATA1 / LCD_DATA1 / SD_WP_1 / PWM1B	DV_DATA1	DV input	CN11,B6	
		PJ1	Connected to LCD module DB6 pin	CN7,16	SW6-3:OFF
		SD_WP_1	Connected to SD card slot WP pin		
		–	Connected to C/A converter1 (U11) LRCKI pin	CN7,20	SW6-3:ON
154	Vss				

Legend : .... : 3.3V system power supply, ... : 1.25V system power supply, ... : GND

Table2.2.6 Pins Used (6)

Pin	Name	Symbol	Description	Expansion Connector	Remarks
155	PG8 / D24 / LCD_DATA8 / PINT0 / TIOC3A	LCD_DATA8	Connected to LCD module D6 pin	CN9,12 CN10,A6	G0
156	Vcc				
157	PJ2 / DV_DATA2 / LCD_DATA2 / SD_D1_1 / PWM1C	DV_DATA2	DV input	CN11,A10	
		PJ2	Connected to character LCD DB5 pin	CN7,13	SW6-3:OFF
		SD_D1_1	Connected to SD card slot DAT1 pin		
		–	Connected to C/A converter1（U11）SDTI pin	CN7,19	SW6-3:ON
158	PJ3 / DV_DATA3 / LCD_DATA3 / SD_D0_1 / PWM1D	DV_DATA3	DV input	CN11,B9	
		PJ3	Connected to character LCD DB4 pin	CN7,14	SW6-3:OFF
		SD_D0_1	Connected to SD card slot DAT0 pin		
		–	Connected to D/A converter2（U12）BICKI pin	CN7,22	SW6-3:ON
159	PJ4 / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / PWM1E	DV_DATA4	DV input	CN11, A9	
		–	–	CN7, 3	SW6-3:OFF
		–	–	CN7, 24	SW6-3:ON
160	PG9 / D25 / LCD_DATA9 / PINT1 / TIOC3B	LCD_DATA9	Connected to LCD module D9 pin	CN9,11 CN10, B6	G1
161	PG10 / D26 / LCD_DATA10 / PINT2 / TIOC3C	LCD_DATA10	Connected to LCD module D10 pin	CN9,14 CN10,A7	G2
162	PVcc				
163	PG11 / D27 / LCD_DATA11 / PINT3 / TIOC3D	LCD_DATA11	Connected to LCD module D11 pin	CN9,13 CN10,B7	G3
164	Vss				
165	PG12 / D28 / LCD_DATA12 / PINT4	LCD_DATA12	Connected to LCD module D12 pin	CN9,16 CN10,B8	G4
166	Vcc				
167	PG13 / D29 / LCD_DATA13 / PINT5	LCD_DATA13	Connected to LCD module D13 pin	CN9,18 CN10,A9	G5
168	PG14 / D30 / LCD_DATA14 / PINT6	LCD_DATA14	Connected to LCD module D14 pin	CN9,17 CN10,B9	G6
169	PG15 / D31 / LCD_DATA15 / PINT7	LCD_DATA15	Connected to LCD module D15 pin	CN9,20 CN10,A10	G7
170	PG16 / WE2#/ICIORD#/DQMUL / LCD_DATA16 / AUDATA0	LCD_DATA16	Connected to LCD module D16 pin	CN10,A11	R0
		AUDATA0	Connected to H-UDI port connector（J3）		AUD
171	PJ5 / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / PWM1F	DV_DATA5	DV input	CN11,A7	
		–	–	CN7,4	SW6-3:OFF
		–	–	CN7,23	SW6-3:ON
172	PVcc				
173	PJ6 / DV_DATA6 / LCD_DATA6 / SD_D3_1 / PWM1G	DV_DATA6	DV input	CN11,B7	
		–	–	CN7,1	SW6-3:OFF
		–	–	CN7,25	SW6-3:ON
174	Vss				
175	PG17 / WE3#/ICIOWR#/AH#/DQMUU / LCD_DATA17 / AUDATA1	LCD_DATA17	Connected to LCD module D17 pin	CN10,B11	R1
		AUDATA1	Connected to H-UDI port connector（J3）		AUD
176	Vcc				
177	PJ7 / DV_DATA7 / LCD_DATA7 / SD_D2_1 / PWM1H	DV_DATA7	DV input	CN11,A5	
		–	–	CN7,2	SW6-3:OFF
		–	–	CN7,28	SW6-3:ON

Legend : .... : 3.3V system power supply, ... : 1.25V system power supply, ... : GND

Table2.2.7 Pins Used (7)

Pin	Name	Symbol	Description	Expansion Connector	Remarks
178	PJ8 / DV_DATA8 / LCD_DATA8 / PINT0 / PWM2A / CTS5#	PWM2A	PWM output	CN11,A4	TTL level
		DV_DATA8	DV input		
		–	–	CN1,12	
179	PJ9 / DV_DATA9 / LCD_DATA9 / PINT1 / PWM2B / RTS5#	PWM2B	PWM output	CN11,B3	TTL level
		DV_DATA9	DV input		
		–	–	CN1,5	
180	PG18 / DV_DATA4 / LCD_DATA18 / SPDIF_IN / SCK4	LCD_DATA18	Connected to LCD module D18 pin	CN10, A12	R2
181	PG19 / DV_DATA5 / LCD_DATA19 / SPDIF_OUT / SCK5	LCD_DATA19	Connected to LCD module D19 pin	CN10,B12	R3
182	PVcc				
183	PG20 / DV_DATA6 / LCD_DATA20 / LCD_TCON3 / RxD4	LCD_DATA20	Connected to LCD module D20 pin	CN10,B13	R4
184	Vss				
185	PG21 / DV_DATA7 / LCD_DATA21 / LCD_TCON4 / TxD4 / AUDATA2	LCD_DATA21	Connected to LCD module D21 pin	CN10,A14	R5
		AUDATA2	Connected to H-UDI port connector（J3）		AUD
186	Vcc				
187	PG22 / LCD_DATA22 / LCD_TCON5 / RxD5 / AUDSYNC#	LCD_DATA22	Connected to LCD module D22 pin	CN10,B14	R6
		AUDSYNC#	Connected to H-UDI port connector（J3）		AUD
		–	–	CN1,15	
188	PG23 / LCD_DATA23 / LCD_TCON6 / TxD5 / AUDATA3	LCD_DATA23	Connected to LCD module D23 pin	CN10,A15	R7
		AUDATA3	Connected to H-UDI port connector（J3）		AUD
		–	–	CN1,14	
189	PG24 / LCD_CLK	LCD_CLK	Connected to LCD module CLK pin	CN9,23 CN10,A16	
190	PG25 / LCD_TCON0	LCD_TCON0	Connected to LCD module VSYNC pin	CN9,19 CN10,B16	
191	PG26 / LCD_TCON1	LCD_TCON1	Connected to LCD module HSYNC pin	CN9,21 CN10,A17	
192	PG27 / LCD_TCON2 / LCD_EXTCLK	LCD_EXTCLK	Connects an LCD module external clock	CN9,26	
193	PF0 / BREQ# / QSPCLK_1 / RSPCK1 / TIOC4A / DREQ0 / AUDCK	QSPCLK_1 / RSPCK1	Connected to serial flash memory 2 SCK pin	CN7,30	
		AUDCK	Connected to H-UDI port connector（J3）		AUD
		–	–		
				CN9,28	
194	PVcc				
195	PF1 / BACK# / QSSL_1 / SSL10 / TIOC4B / DACK0	QSSL_1 / SSL10	Connected to serial flash memory 2 CS# pin	CN5,20	
196	Vss				
197	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0/ SPBMO_1/SPBIO0_1	QMO_1/QIO0_1 / MOSI1/ SPBMO_1/SPBIO0_1	Connected to serial flash memory 2 S pin	CN7,31	
		–	–		
				CN9,30	

Legend : .... : 3.3V system power supply, ... : 1.25V system power supply, ... : GND

Table2.2.8 Pins Used (8)

Pin	Name	Symbol	Description	Expansion Connector	Remarks
198	PF3 / CS2# / QMI_1/QIO1_1 / MISO1 / TIOC4D / AUDIO_XOUT / SPBMI_1/SPBIO1_1	QMI_1/QIO1_1 / MISO1 / SPBMI_1/SPBIO1_1	Connected to serial flash memory 2 SO pin	CN7,33	
199	PF4 / CS5#/CE1A# / SSISCK0 / SGOUT_0	SGOUT_0		CN7,36	0Ω resister
		–	–		
200	PF5 / SSIWS0 / SGOUT_1	SGOUT_1		CN7,35	0Ω resister
		–	–		
201	PF6 / CE2A# / SSITxD0 / SGOUT_2	SGOUT_2		CN7,37	0Ω resister
		–	–		
202	PF7 / SSIRxD0 / RxD0 / SGOUT_3 / CTS1#	SGOUT_3		CN7,38	0Ω resister
		–	–		
203	PF8 / A23 / TxD0	A23	Address bus	CN5,19	
204	PF9 / BS# / DV_DATA0 / SCK0 / MMC_D4 / RTS1#	PF9		CN5,18	
205	PVcc				
206	PF10 / CS1# / SSISCK1 / DV_DATA1 / SCK1 / MMC_D5	–	–	CN7,17	
207	Vss				
208	PF11 / SSIWS1 / DV_DATA2 / RxD1 / MMC_D6	–	–	CN7,20	
209	PF12 / SSIDATA1 / DV_DATA3 / TxD1 / MMC_D7	–	–	CN7,19	
210	PF13 / A24 / SSISCK2 / SCK2	A24	Address bus	CN5,17	
211	PF14 / A25 / SSIWS2 / RxD2	RxD2	Connected to RS-232C connector（J10）	CN5,16	
212	PF15 / A0 / SSIDATA2 / WDTOVF# / TxD2 / UBCTRG#	TxD2	Connected to RS-232C connector（J10）	CN5,15	
213	PVcc				
214	PJ10 / DV_DATA10 / LCD_DATA10 / PINT2 / PWM2C / SCK5#	PWM2C	PWM output	CN11,A2	TTL level
		DV_DATA10	DV input		
		–	–	CN1,13	
215	Vss				
216	PF16 / SD_CD_0 / FCE# / IRQ4 / MMC_CD	SD_CD_0 / MMC_CD	Connected to SD/MMC card slot CD pin	CN5,13	SW6-2:ON
		FCE#	Connected to NAND flash memory CE# pin	CN5,12	SW6-2:OFF
217	PF17 / SD_WP_0 / FRB / IRQ5	SD_WP_0	Connected to SD/MMC card slot WP pin	CN5,11	SW6-2:ON
		FRB	Connected to NAND flash memory R/B# pin	CN5,10	SW6-2:OFF
218	PF18 / SD_D1_0 / SSISCK3 / IRQ6 / MMC_D1	SD_D1_0 / MMC_D1	Connected to SD/MMC card slot DAT1 pin	CN5,8	
219	PJ11 / DV_DATA11 / LCD_DATA11 / PINT3 / PWM2D / SCK6	PWM2D	PWM output	CN11,B2	TTL level
		DV_DATA11	DV input		
		–	–	CN1,1	
220	PJ12 / DV_DATA12 / LCD_DATA12 / PINT4 / PWM2E / SCK7	PWM2E	PWM output	CN11,B11	TTL level
		DV_DATA12	DV input		
221	PJ13 / DV_DATA13 / LCD_DATA13 / PINT5 / PWM2F / TxD5	PWM2F	PWM output	CN11,A11	TTL level
		DV_DATA13	DV input		
		–	–	CN7,32	
222	PVcc				

Legend : .... : 3.3V system power supply, ... : 1.25V system power supply, ... : GND

Table2.2.9 Pins Used (9)

Pin	Name	Symbol	Description	Expansion Connector	Remarks
223	PF19 / SD_D0_0 / SSIWS3 / IRQ7 / MMC_D0	SD_D0_0 / MMC_D0	Connected to SD/MMC card slot DAT0 pin	CN5,7	
224	Vss				
225	PF20 / SD_CLK_0 / SSIDATA3 / MMC_CLK	SD_CLK_0 / MMC_CLK	Connected to SD/MMC card slot CLK pin	CN5,5	
226	Vcc				
227	PF21 / SD_CMD_0 / SCK3 / MMC_CMD	SD_CMD_0 / MMC_CMD	Connected to SD/MMC card slot CMD pin	CN5,4	
228	PF22 / SD_D3_0 / RxD3 / MMC_D3	SD_D3_0 / MMC_D3	Connected to SD/MMC card slot DAT3 pin	CN5,3	
229	PF23 / SD_D2_0 / TxD3 / MMC_D2	SD_D2_0 / MMC_D2	Connected to SD/MMC card slot DAT2 pin	CN5,2	
230	PD0 / D0 / PWM1A	D0	Data bus	CN8,1	
231	PVcc				
232	PJ24 / SGOUT_0 / SSISCK4 / LCD_TCON3 / SPDIF_IN / SCK7	–	–	CN7,25	
233	Vss				
234	PD1 / D1 / PWM1B	D1	Data bus	CN8,3	
235	PD2 / D2 / PWM1C	D2	Data bus	CN8,6	
236	PD3 / D3 / PWM1D	D3	Data bus	CN8,8	
237	PJ25 / SGOUT_1 / SSIWS4 / LCD_TCON4 / SPDIF_OUT / RxD7	–	–	CN7,28	
238	PJ26 / SGOUT_2 / SSIDATA4 / LCD_TCON5 / TxD7	–	–	CN7,27	
239	PJ27 / SGOUT_3 / TIOC1A / CTS7#	–	–	CN9,29	
240	PVcc				
241	Vss				
242	PD4 / D4/FRE# / PWM1E	D4/FRE#	Data bus/ Connected to NAND flash memory RE# pin	CN8,11	Automatically switched
243	PD5 / D5/FCLE / PWM1F	D5/FCLE	Data bus/ Connected to NAND flash memory CLE pin	CN8,13	Automatically switched
244	PD6 / D6/FALE / PWM1G	D6/FALE	Data bus/ Connected to NAND flash memory ALE pin	CN8,16	Automatically switched
245	PD7 / D7/FWE# / PWM1H	D7/FWE#	Data bus/ Connected to NAND flash memory WE# pin	CN8,18	Automatically switched
246	PD8 / D8/NAF0 / PWM2A	D8/NAF0	Data bus	CN8,2	
247	PD9 / D9/NAF1 / PWM2B	D9/NAF1	Data bus	CN8,4	
248	PD10 / D10/NAF2 / PWM2C	D10/NAF2	Data bus	CN8,7	
249	PD11 / D11/NAF3 / PWM2D	D11/NAF3	Data bus	CN8,9	
250	PVcc				
251	PD12 / D12/NAF4 / PWM2E	D12/NAF4	Data bus	CN8,12	
252	Vss				
253	PD13 / D13/NAF5 / PWM2F	D13/NAF5	Data bus	CN8,14	

Legend : .... : 3.3V system power supply, ... : 1.25V system power supply, ... : GND

Table2.2.10 Pins Used (10)

Pin	Name	Symbol	Description	Expansion Connector	Remarks
254	PD14 / D14/NAF6 / PWM2G	D14/NAF6	Data bus	CN8,17	
255	PD15 / D15/NAF7 / PWM2H	D15/NAF7	Data bus	CN8,19	
256	MD_CLK0	MD_CLK0	Connected to SW5-1 as clock mode input	ー	RES#:"L"

Legend : .... : 3.3V system power supply, ... : 1.25V system power supply, ... : GND

2.2.3 R0K572690B000BR Module Combination Availability

Table2.2.11 shows the combination availability / non-availability between the modules for the R0K572690B000BR. “Y” on the table represents the combination “available”, and “N”, “not available”.

Table2.2.11 R0K572690B000BR Module Combination Availability

			R0K572690C000BR + R0K572690B000BR																
SH7269 peripheral device	Parts No.	Module	NOR flash memory	SDRAM	NAND flash memory	EEPROM	Serial flash memory 1	Serial flash memory 2	USB	SD/MMC card	H-UDI(14-pin)	H-UDI(38-pin)	LED	NMI switch	IRQ1 switch	DIP switch	RS-232C	LCD	DV	PWM
R0K572690C000BR + R0K572690B000BR																				
BSC	U6	NOR flash memory		Y	Y	Y	N	(1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
BSC	U9	SDRAM	Y		Y	Y	Y	(1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
FLCTL	U7	NAND flash memory	Y	Y		Y	Y	Y	Y	(2)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
IIC3	U8	EEPROM	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
RSPI	U10	Serial flash memory 1	N	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
RSPI	U10	Serial flash memory 2	(1)	(1)	Y	Y	Y		Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y
USB	J1,2	USB	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
SDHI/MMC	J11	SD/MMC card	Y	Y	(2)	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
H-UDI	J7	H-UDI(14-pin)	Y	Y	Y	Y	Y	Y	Y	Y		(3)	Y	Y	Y	Y	Y	Y	Y	Y
H-UDI,AUD	J3	H-UDI(38-pin)	Y	Y	Y	Y	Y	N	Y	Y	(3)		Y	Y	Y	Y	Y	N	Y	Y
IOポート	LED2,3	LED	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	(6)	Y
INTC	SW3	NMI switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	Y	Y	Y
INTC	SW4	IRQ1 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y	(5)	Y
IOポート	SW5,6	DIP switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	(7)	Y
SCIF	J10	RS-232C	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		Y	Y	Y
VDC4	CN10	LCD	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y		(4)	Y
VDC4	CN11	DV	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(6)	Y	(5)	(7)	Y	(4)		(8)
PWM	CN11	PWM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	(8)	

Notes:
(1) Quad mode is not available
(2) PF16 and PF17 are multiplexed pins. Either of them is available by setting SW6 #2.
(3) Either of them is available.
(4) Pins are commonly used between PJ22, DV_DATA22, and LCD_DATA22, also between PJ23, DV_DATA23, and LCD_DATA23.
(5) Pins are commonly used between PJ21, DV_DATA21 and IRQ1.
(6) Pins are commonly used between PJ19 and DV_DATA19, also between PJ18 and DV_DATA18.
(7) Pins are commonly used between PJ17 and DV_DATA17, also between PJ16 and DV_DATA16.

2.2.4 SH7269 Multiplexed Pins for the R0K572690B000BR

Table2.2.12 to Table2.2.25 list SH7269 multiplexed pins used for the R0K572690B000BR.
The default setting is for port input. Therefore setting the MD bit in the port control register is required to use the peripheral functions excluding I/O port.

Table2.2.12 SH7269 Multiplexed Pin Functions (BSC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
BSC	CS0#	PCCR0	PC0MD = B'1(1)	PC0 / **CS0#** / MD_BOOT2
	CS3#	PCCR2	PC8MD[2:0] = B'001	PC8 / **CS3#** / TxD7 / CTx1 / CTx0&CTx1
	RD#	PCCR0	PC1MD = B'1(1)	PC1 / **RD#**
	WE0#/DQMLL	PCCR0	PC3MD[1:0] = B'01	PC3 / **WE0#/DQMLL** / RxD6
	WE1#/WE#/DQMLU	PCCR1	PC4MD[1:0] = B'01	PC4 / **WE1#/WE#/DQMLU** / TxD6
	RAS#	PCCR1	PC5MD[2:0] = B'001	PC5 / **RAS#** / CRx0 / CRx0/CRx1/CRx2 / IRQ0
	CAS#	PCCR1	PC6MD[2:0] = B'001	PC6 / **CAS#** / SCK7 / CTx0 / CTx0&CTx1&CTx2
	CKE	PCCR1	PC7MD[2:0] = B'001	PC7 / **CKE** / RxD7 / CRx1 / CRx0/CRx1 / IRQ1
	RD/WR#	PCCR0	PC2MD[1:0] = B'01	PC2 / **RD/WR#** / SCK6
	A24	PFCR3	PF13MD[2:0] = B'001	PF13 / **A24** / SSISCK2 / SCK2
	A23	PFCR2	PF8MD[2:0] = B'001	PF8 / **A23** / TxD0
	A22	PBCR5	PB22MD[2:0] = B'001	PB22 / **A22** / CTx2 / IETxD / CS4#
	A21	PBCR5	PB21MD[1:0] = B'01	PB21 / **A21** / CRx2 / IERxD
	A20	PBCR5	PB20MD[1:0] = B'001(1)	PB20 / **A20** / QMISO0&QIO10 / MISO0/ SPBMI_0/SPBIO1_0
	A19	PBCR4	PB19MD[1:0] = B'001(1)	PB19 / **A19** / QMO_0&QIO0_0 / MOSI0 / SPBMO_0/SPBIO0_0
	A18	PBCR4	PB18MD[1:0] = B'001(1)	PB18 / **A18** / QSSL_0 / SSL00 / SPBSSL
	A17	PBCR4	PB17MD[1:0] = B'001(1)	PB17 / **A17** / QSPCLK_0 / RSPCK0 / SPBCLK
	A16	PBCR4	PB16MD[1:0] = B'001(1)	PB16 / **A16** / QIO3_0 / SPBIO3_0
	A15	PBCR3	PB15MD[1:0] = B'001(1)	PB15 / **A15** / QIO2_0 / SPBIO2_0
	A14	PBCR3	PB14MD[1:0] = B'001(1)	PB14 / **A14** / QIO3_1 / SPBIO3_1
	A13	PBCR3	PB13MD[1:0] = B'001(1)	PB13 / **A13** / QIO2_1 / SPBIO2_1
	A12	PBCR3	PB12MD[1:0] = B'01(1)	PB12 / **A12** / TIOC3D
	A11	PBCR2	PB11MD[1:0] = B'01(1)	PB11 / **A11** / TIOC3C
	A10	PBCR2	PB10MD[1:0] = B'01(1)	PB10 / **A10** / TIOC3B
	A9	PBCR2	PB9MD[1:0] = B'01(1)	PB9 / **A9** / TIOC3A
	A8	PBCR2	PB8MD[1:0] = B'01(1)	PB8 / **A8** / TIOC2B
	A7	PBCR1	PB7MD[1:0] = B'01(1)	PB7 / **A7** / TIOC2A
	A6	PBCR1	PB6MD[1:0] = B'01(1)	PB6 / **A6** / TIOC1B
	A5	PBCR1	PB5MD[1:0] = B'01(1)	PB5 / **A5** / TIOC1A
	A4	PBCR1	PB4MD[1:0] = B'01(1)	PB4 / **A4** / TIOC0D
	A3	PBCR0	PB3MD[1:0] = B'01(1)	PB3 / **A3** / TIOC0C
	A2	PBCR0	PB2MD[1:0] = B'01(1)	PB2 / **A2** / TIOC0B
	A1	PBCR0	PB1MD[1:0] = B'01(1)	PB1 / **A1** / TIOC0A
	D15	PDCR3	PD15MD[1:0] = B'01(1)	PD15 / **D15/NAF7** / PWM2H
	D14	PDCR3	PD14MD[1:0] = B'01(1)	PD14 / **D14/NAF6** / PWM2G
	D13	PDCR3	PD13MD[1:0] = B'01(1)	PD13 / **D13/NAF5** / PWM2F
	D12	PDCR3	PD12MD[1:0] = B'01(1)	PD12 / **D12/NAF4** / PWM2E
	D11	PDCR2	PD11MD[1:0] = B'01(1)	PD11 / **D11/NAF3** / PWM2D
	D10	PDCR2	PD10MD[1:0] = B'01(1)	PD10 / **D10/NAF2** / PWM2C
	D9	PDCR2	PD9MD[1:0] = B'01(1)	PD9 / **D9/NAF1** / PWM2B
	D8	PDCR2	PD8MD[1:0] = B'01(1)	PD8 / **D8/NAF0** / PWM2A
	D7	PDCR1	PD7MD[1:0] = B'01(1)	PD7 / **D7/FWE#** / PWM1H
	D6	PDCR1	PD6MD[1:0] = B'01(1)	PD6 / **D6/FALE** / PWM1G
	D5	PDCR1	PD5MD[1:0] = B'01(1)	PD5 / **D5/FCLE** / PWM1F

Notes: (1) : These values should be set in boot mode 2 to 5
The multiplexed pin names in bold style are the set function.

Table2.2.13 SH7269 Multiplexed Pin Functions (BSC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
BSC	D4	PDCR1	PD4MD[1:0] = B'01(1)	PD4 / **D4/FRE#** / PWM1E
	D3	PDCR0	PD3MD[1:0] = B'01(1)	PD3 / **D3** / PWM1D
	D2	PDCR0	PD2MD[1:0] = B'01(1)	PD2 / **D2** / PWM1C
	D1	PDCR0	PD1MD[1:0] = B'01(1)	PD1 / **D1** / PWM1B
	D0	PDCR0	PD0MD[1:0] = B'01(1)	PD0 / **D0** / PWM1A

Notes: (1) :These values should be set in boot mode 2 to 5
The multiplexed pin names in bold style are the set function.

Table2.2.14 SH7269 Multiplexed Pin Functions (INTC)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
INTC	IRQ1	PJCR5	PJ21MD[2:0] = B'100	PJ21 / DV_DATA21 / LCD_DATA21 / LCD_TCON4 / **IRQ1** / CTx2 / CTx0&CTx1&CTx2

Note: The multiplexed pin names in bold style are the set function.

Table2.2.15 SH7269 Multiplexed Pin Functions (SCIF)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
SCIF	RxD2	PFCR3	PF14MD[2:0] = B'100	PF14 / A25 / SSIWS2 / **RxD2**
	TxD2	PFCR4	PF15MD[2:0] = B'100	PF15 / A0 / SSIDATA2 / WDTOVF# / **TxD2** / UBCTRG#

Note: The multiplexed pin names in bold style are the set function.

Table2.2.16 SH7269 Multiplexed Pin Functions (IIC3)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
IIC3	SDA1	PECR0	PE3MD[2:0] = B'001	PE3 / **SDA1** / TCLKD / ADTRG# / DV_HSYNC
	SCL1	PECR0	PE2MD[2:0] = B'001	PE2 / **SCL1** / TCLKC / IOIS16# / DV_VSYNC

Note: The multiplexed pin names in bold style are the set function.

Table2.2.17 SH7269 Multiplexed Pin Functions (FLCTL)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
FLCTL	NAF7	PDCR3	PD15MD[1:0] = B'01(1)	PD15 / **D15/NAF7** / PWM2H
	NAF6	PDCR3	PD14MD[1:0] = B'01(1)	PD14 / **D14/NAF6** / PWM2G
	NAF5	PDCR3	PD13MD[1:0] = B'01(1)	PD13 / **D13/NAF5** / PWM2F
	NAF4	PDCR3	PD12MD[1:0] = B'01(1)	PD12 / **D12/NAF4** / PWM2E
	NAF3	PDCR2	PD11MD[1:0] = B'01(1)	PD11 / **D11/NAF3** / PWM2D
	NAF2	PDCR2	PD10MD[1:0] = B'01(1)	PD10 / **D10/NAF2** / PWM2C
	NAF1	PDCR2	PD9MD[1:0] = B'01(1)	PD9 / **D9/NAF1** / PWM2B
	NAF0	PDCR2	PD8MD[1:0] = B'01(1)	PD8 / **D8/NAF0** / PWM2A
	FWE#	PDCR1	PD7MD[1:0] = B'01(1)	PD7 / **D7/FWE#** / PWM1H
	FALE	PDCR1	PD6MD[1:0] = B'01(1)	PD6 / **D6/FALE** / PWM1G
	FCLE	PDCR1	PD5MD[1:0] = B'01(1)	PD5 / **D5/FCLE** / PWM1F
	FRE#	PDCR1	PD4MD[1:0] = B'01(1)	PD4 / **D4/FRE#** / PWM1E
	FCE#	PFCR5	PF16MD[2:0] = B'011	PF16 / SD_CD_0 / **FCE#** / IRQ4 / MMC_CD
	FRB	PFCR5	PF17MD[2:0] = B'011	PF17 / SD_WP_0 / **FRB** / IRQ5

Notes: (1) :These values should be set in boot mode 2 to 5
The multiplexed pin names in bold style are the set function.

Table2.2.18 SH7269 Multiplexed Pin Functions (RSPI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
RSPI	MISO0	PBCR5	PB20MD[2:0] = B'011(1)	PB20 / A20 / QMI_0/QIO1_0 / **MISO0**/ SPBMI_0/SPBIO1_0
	MOSI0	PBCR4	PB19MD[2:0] = B'011(1)	PB19 / A19 / QMO_0/QIO0_0 / **MOSI0**/ SPBMO_0/SPBIO0_0
	SSL00	PBCR4	PB18MD[2:0] = B'011(1)	PB18 / A18 / QSSL_0 / **SSL00** / SPBSSL
	RSPCK0	PBCR4	PB17MD[2:0] = B'011(1)	PB17 / A17 / QSPCLK_0 / **RSPCK0** / SPBCLK
	MISO1	PFCR0	PF3MD[2:0] = B'011	PF3 / CS2# / QMI_1/QIO1_1 / **MISO1** / TIOC4D / AUDIO_XOUT / SPBMI_1/SPBIO1_1
	MOSI1	PFCR0	PF2MD[2:0] = B'011	PF2 / WAIT# / QMO_1/QIO0_1 / **MOSI1** / TIOC4C / TEND0 / SPBMO_1/SPBIO0_1
	SSL10	PFCR0	PF1MD[2:0] = B'011	PF1 / BACK# / QSSL_1 / **SSL10** / TIOC4B / DACK0
	RSPCK1	PFCR0	PF0MD[2:0] = B'011	PF0 / BREQ# / QSPCLK_1 / **RSPCK1** / TIOC4A / DREQ0 / AUDCK

Notes: (1)Shouldn't be set in boot mode 0 and 1.
The multiplexed pin names in bold style are the set function.

Table2.2.19 SH7269 Multiplexed Pin Functions (RQSPI)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
RQSPI	QIO3_0	PBCR4	PB16MD[2:0] = B'010(1)	PB16 / A16 / **QIO3_0** / SPBIO3_0
	QIO2_0	PBCR3	PB15MD[2:0] = B'010(1)	PB15 / A15 / **QIO2_0** / SPBIO2_0
	QIO1_0	PBCR5	PB20MD[2:0] = B'010(1)	PB20 / A20 / **QMI_0/QIO1_0** / MISO0 / SPBMI_0/SPBIO1_0
	QIO0_0	PBCR4	PB19MD[2:0] = B'010(1)	PB19 / A19 / **QMO_0/QIO0_0** / MOSI0 / SPBMO_0/SPBIO0_0
	QSSL_0	PBCR4	PB18MD[2:0] = B'010(1)	PB18 / A18 / **QSSL_0** / SSL00 / SPBSSL
	QSPCLK_0	PBCR4	PB17MD[2:0] = B'010(1)	PB17 / A17 / **QSPCLK_0** / RSPCK0/ SPBCLK
	QIO3_1	PBCR4	PB14MD[2:0] = B'010(1)	PB14 / A14 / **QIO3_1** / SPBIO3_1
	QIO2_1	PBCR4	PB13MD[2:0] = B'010(1)	PB13 / A13 / **QIO2_1** / SPBIO2_1
	QIO1_1	PFCR0	PF3MD[2:0] = B'010	PF3 / CS2# / **QMI_1/QIO1_1** / MISO1 / TIOC4D / AUDIO_XOUT / SPBMI_1/SPBIO1_1
	QIO0_1	PFCR0	PF2MD[2:0] = B'010	PF2 / WAIT# / **QMO_1/QIO0_1** / MOSI1 / TIOC4C / TEND0 / SPBMO_1/SPBIO0_1
	QSSL_1	PFCR0	PF1MD[2:0] = B'010	PF1 / BACK# / **QSSL_1** / SSL10 / TIOC4B / DACK0
	QSPCLK_1	PFCR0	PF0MD[2:0] = B'010	PF0 / BREQ# / **QSPCLK_1** / RSPCK1 / TIOC4A / DREQ0 / AUDCK

Notes: (1)Shouldn't be set in boot mode 0 and 1.
The multiplexed pin names in bold style are the set function.

Table2.2.20 SH7269 Multiplexed Pin Functions (SPIBSC)

Peripheral Function	Pin Name	SH7269 Port control register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
SPIBSC	SPBCLK	PBCR4	PB17MD[2:0] = B'110 (1)	PB17 / A17 / QSPCLK_0 / RSPCK0 / **SPBCLK**
	SPBSSL QIO2_0	PBCR4	PB18MD[2:0] = B'110 (1)	PB18 / A18 / QSSL_0 / SSL00 / **SPBSSL**
	SPBMO_0/ SPBIO0_0	PBCR4	PB19MD[2:0] = B'110 (1)	PB19 / A19 / QMO_0/QIO0_0 / MOSI0 / **SPBMO_0/SPBIO0_0**
	SPBMI_0/ SPBIO1_0	PBCR5	PB20MD[2:0] = B'110 (1)	PB20 / A20 / QMI_0/QIO1_0 / MISO0 / **SPBMI_0/SPBIO1_0**
	SPBIO2_0	PBCR3	PB15MD[2:0] = B'110 (1)	PB15 / A15 / QIO2_0 / **SPBIO2_0**
	SPBIO3_0	PBCR4	PB16MD[2:0] = B'110 (1)	PB16 / A16 / QIO3_0 / **SPBIO3_0**
	SPBMO_1/ SPBIO0_1	PFCR0	PF2MD[2:0] = B'110	PF2 / WAIT# / QMO_1/QIO0_1 / MOSI1 / TIOC4C / TEND0 / **SPBMO_1/SPBIO0_1**
	SPBMI_1/ SPBIO1_1	PFCR0	PF3MD[2:0] = B'110	PF3 / CS2# / QMI_1/QIO1_1 / MISO1 / TIOC4D / AUDIO_XOUT / **SPBMI_1/SPBIO1_1**
	SPBIO2_1	PBCR3	PB13MD[2:0] = B'110 (1)	PB13 / A13 / QIO2_1 / **SPBIO2_1**
	SPBIO3_1	PBCR3	PB14MD[2:0] = B'110 (1)	PB14 / A14 / QIO3_1 / **SPBIO3_1**

Notes: (1) These values must not be set in boot modes 0 and 1.
Bold text indicates the function used.

Table 2.2.21 SH7269 Multiplexed Pin Functions (SDHI)

Peripheral Function	Pin Name	SH7269 Port control register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
SDHI	SD_CD_0	PFCR5	PF16MD[2:0] = B'001	PF16 / **SD_CD_0** / FCE# / IRQ4 / MMC_CD
	SD_WP_0	PFCR5	PF17MD[2:0] = B'001	PF17 / **SD_WP_0** / FRB / IRQ5
	SD_D1_0	PFCR5	PF18MD[2:0] = B'001	PF18 / **SD_D1_0** / SSISCK3 / IRQ6 / MMC_D1
	SD_D0_0	PFCR5	PF19MD[2:0] = B'001	PF19 / **SD_D0_0** / SSIWS3 / IRQ7 / MMC_D0
	SD_CLK_0	PFCR6	PF20MD[2:0] = B'001	PF20 / **SD_CLK_0** / SSIDATA3 / MMC_CLK
	SD_CMD_0	PFCR6	PF21MD[2:0] = B'001	PF21 / **SD_CMD_0** / SCK3 / MMC_CMD
	SD_D3_0	PFCR6	PF22MD[2:0] = B'001	PF22 / **SD_D3_0** / RxD3 / MMC_D3
	SD_D2_0	PFCR6	PF23MD[2:0] = B'001	PF23 / **SD_D2_0** / TxD3 / MMC_D2

Note: The multiplexed pin names in bold style are the set function.

Table 2.2.22 SH7269 Multiplexed Pin Functions (MMC)

Peripheral Function	Pin Name	SH7269 Port control register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
MMC	MMC_CD	PFCR5	PF16MD[2:0] = B'101	PF16 / SD_CD_0 / FCE# / IRQ4 / **MMC_CD**
	MMC_D1	PFCR5	PF18MD[2:0] = B'101	PF18 / SD_D1_0 / SSISCK3 / IRQ6 / **MMC_D1**
	MMC_D0	PFCR5	PF19MD[2:0] = B'101	PF19 / SD_D0_0 / SSIWS3 / IRQ7 / **MMC_D0**
	MMC_CLK	PFCR6	PF20MD[2:0] = B'101	PF20 / SD_CLK_0 / SSIDATA3 / **MMC_CLK**
	MMC_CMD	PFCR6	PF21MD[2:0] = B'101	PF21 / SD_CMD_0 / SCK3 / **MMC_CMD**
	MMC_D3	PFCR6	PF22MD[2:0] = B'101	PF22 / SD_D3_0 / RxD3 / **MMC_D3**
	MMC_D2	PFCR6	PF23MD[2:0] = B'101	PF23 / SD_D2_0 / TxD3 / **MMC_D2**

Note: The multiplexed pin names in bold style are the set function.

Table2.2.23 SH7269 Multiplexed Pin Functions (VDC4)

Peripheral Function	Pin Name	SH7269 Port control register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
VDC4	LCD_EXTCLK	PGCR6	PG27MD[1:0] = B'11	PG27 / LCD_TCON2 / **LCD_EXTCLK**
	LCD_CLK	PGCR6	PG24MD[1:0] = B'10	PG24 / **LCD_CLK**
	LCD_TCON6	PJCR5	PJ23MD[2:0] = B'011	PJ23 / DV_DATA23 / LCD_DATA23 / **LCD_TCON6** / IRQ3 / CTx1 / CTx0&CTx1
	LCD_TCON5	PJCR5	PJ22MD[2:0] = B'011	PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1
	LCD_TCON1	PGCR6	PG26MD[1:0] = B'10	PG26 / **LCD_TCON1**
	LCD_TCON0	PGCR6	PG25MD[1:0] = B'10	PG25 / **LCD_TCON0**
	LCD_DATA23	PGCR5	PG23MD[2:0] = B'010	PG23 / **LCD_DATA23** / LCD_TCON6 / TxD5 / AUDATA3
	LCD_DATA22	PGCR5	PG22MD[2:0] = B'010	PG22 / **LCD_DATA22** / LCD_TCON5 / RxD5 / AUDSYNC#
	LCD_DATA21	PGCR5	PG21MD[2:0] = B'010	PG21 / DV_DATA7 / **LCD_DATA21** / LCD_TCON4 / TxD4 / AUDATA2
	LCD_DATA20	PGCR5	PG20MD[2:0] = B'010	PG20 / DV_DATA6 / **LCD_DATA20** / LCD_TCON3 / RxD4
	LCD_DATA19	PGCR4	PG19MD[2:0] = B'010	PG19 / DV_DATA5 / **LCD_DATA19** / SPDIF_OUT / SCK5
	LCD_DATA18	PGCR4	PG18MD[2:0] = B'010	PG18 / DV_DATA4 / **LCD_DATA18** / SPDIF_IN / SCK4
	LCD_DATA17	PGCR4	PG17MD[1:0] = B'10	PG17 / WE3#/ICIOWR#/AH#/DQMUU / **LCD_DATA17** / AUDATA1
	LCD_DATA16	PGCR4	PG16MD[1:0] = B'10	PG16 / WE2#/ICIORD#/DQMUL / **LCD_DATA16** / AUDATA0
	LCD_DATA15	PGCR3	PG15MD[1:0] = B'10(1)	PG15 / D31 / **LCD_DATA15** / PINT7
	LCD_DATA14	PGCR3	PG14MD[1:0] = B'10(1)	PG14 / D30 / **LCD_DATA14** / PINT6
	LCD_DATA13	PGCR3	PG13MD[1:0] = B'10(1)	PG13 / D29 / **LCD_DATA13** / PINT5
	LCD_DATA12	PGCR3	PG12MD[1:0] = B'10(1)	PG12 / D28 / **LCD_DATA12** / PINT4
	LCD_DATA11	PGCR2	PG11MD[2:0] = B'010(1)	PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D
	LCD_DATA10	PGCR2	PG10MD[2:0] = B'010(1)	PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C
	LCD_DATA9	PGCR2	PG9MD[2:0] = B'010(1)	PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B
	LCD_DATA8	PGCR2	PG8MD[2:0] = B'010(1)	PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A
	LCD_DATA7	PGCR1	PG7MD[2:0] = B'010(1)	PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B
	LCD_DATA6	PGCR1	PG6MD[2:0] = B'010(1)	PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A
	LCD_DATA5	PGCR1	PG5MD[2:0] = B'010(1)	PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B
	LCD_DATA4	PGCR1	PG4MD[2:0] = B'010(1)	PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A
	LCD_DATA3	PGCR0	PG3MD[2:0] = B'010(1)	PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D
	LCD_DATA2	PGCR0	PG2MD[2:0] = B'010(1)	PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C
	LCD_DATA1	PGCR0	PG1MD[2:0] = B'010(1)	PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B
	LCD_DATA0	PGCR0	PG0MD[2:0] = B'010(1)	PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A

Note: (1)Shouldn't be set in boot mode 1.
The multiplexed pin names in bold style are the set function.

Table2.2.24 SH7269 Multiplexed Pin Functions (PWM)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
PWM	PWM2H	PJCR3	PJ15MD[2:0] = B'100	PJ15 / DV_DATA15 / LCD_DATA15 / PINT7 / **PWM2H** / TxD7
	PWM2G	PJCR3	PJ14MD[2:0] = B'100	PJ14 / DV_DATA14 / LCD_DATA14 / PINT6 / **PWM2G** / TxD6
	PWM2F	PJCR3	PJ13MD[2:0] = B'100	PJ13 / DV_DATA13 / LCD_DATA13 / PINT5 / **PWM2F** / TxD5
	PWM2E	PJCR3	PJ12MD[2:0] = B'100	PJ12 / DV_DATA12 / LCD_DATA12 / PINT4 / **PWM2E** / SCK7
	PWM2D	PJCR2	PJ11MD[2:0] = B'100	PJ11 / DV_DATA11 / LCD_DATA11 / PINT3 / **PWM2D** / SCK6
	PWM2C	PJCR2	PJ10MD[2:0] = B'100	PJ10 / DV_DATA10 / LCD_DATA10 / PINT2 / **PWM2C** / SCK5
	PWM2B	PJCR2	PJ9MD[2:0] = B'100	PJ9 / DV_DATA9 / LCD_DATA9 / PINT1/ **PWM2B** / RTS5#
	PWM2A	PJCR2	PJ8MD[2:0] = B'100	PJ8 / DV_DATA8 / LCD_DATA8 / PINT0 / **PWM2A** / CTS5#

Note: The multiplexed pin names in bold style are the set function.

Table2.2.25 SH7269 Multiplexed Pin Functions (PORT)

Peripheral Function	Pin Name	SH7269 Port Control Register		SH7269 Multiplexed Pin Name
		Name	MD Bit Setting	
PORT	PJ16	PJCR4	PJ16MD[2:0] = B'000	**PJ16** / DV_DATA16 / LCD_DATA16 / RSPCK0 / TIOC0A / SIOFSCK
	PJ17	PJCR4	PJ17MD[2:0] = B'000	**PJ17** / DV_DATA17 / LCD_DATA17 / SSL00 / TIOC0B / SIOFSYNC
	PJ18	PJCR4	PJ18MD[2:0] = B'000	**PJ18** / DV_DATA18 / LCD_DATA18 / MOSI0 / TIOC0C / SIOFTxD
	PJ19	PJCR4	PJ19MD[2:0] = B'000	**PJ19** / DV_DATA19 / LCD_DATA19 / MISO0 / TIOC0D / SIOFRxD / AUDIO_XOUT

Note: The multiplexed pin names in bold style are the set function.

2.3 TFT-LCD Panel Output Interface

R0K572690B000BR includes two flexible connectors, one 0.635mm pitch two-piece connector, and one MIL spec connector for LCD module connection. LCD module is controlled by the video display controller 4 (VDC4) embedded in the SH7269.

Figure 2.3.1 shows the LCD module interface block wiring diagram.

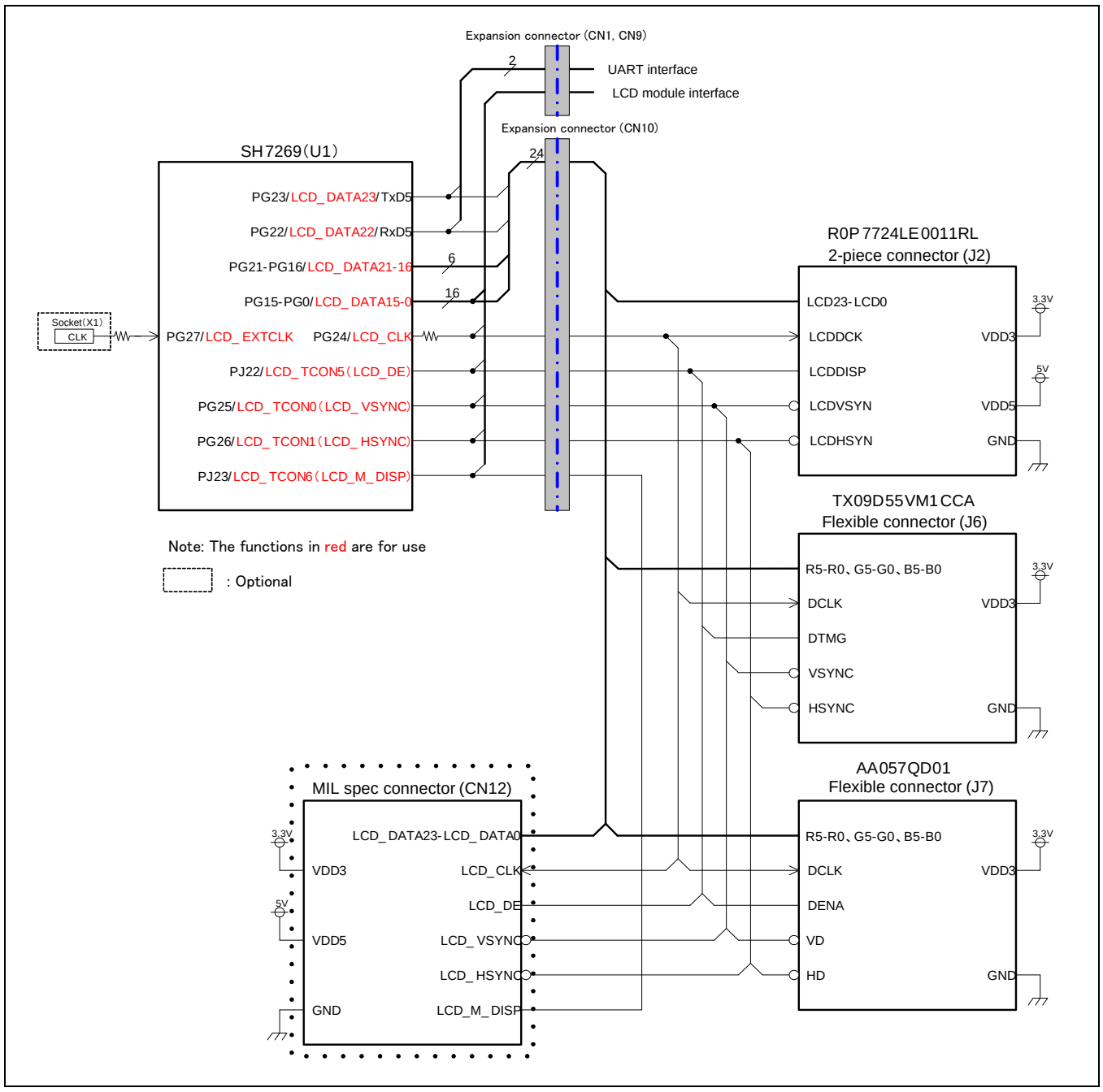

Figure 2.3.1 LCD Module Interface Block Wiring Diagram

2.4 Analog RGB Output Interface

R0K572690B000BR includes a video DAC to convert TFT-LCD panel control signal to analog RGB signal which is output from D-sub 15 pin connector.

Figure2.4.1 shows the analog RGB output interface block wiring diagram.

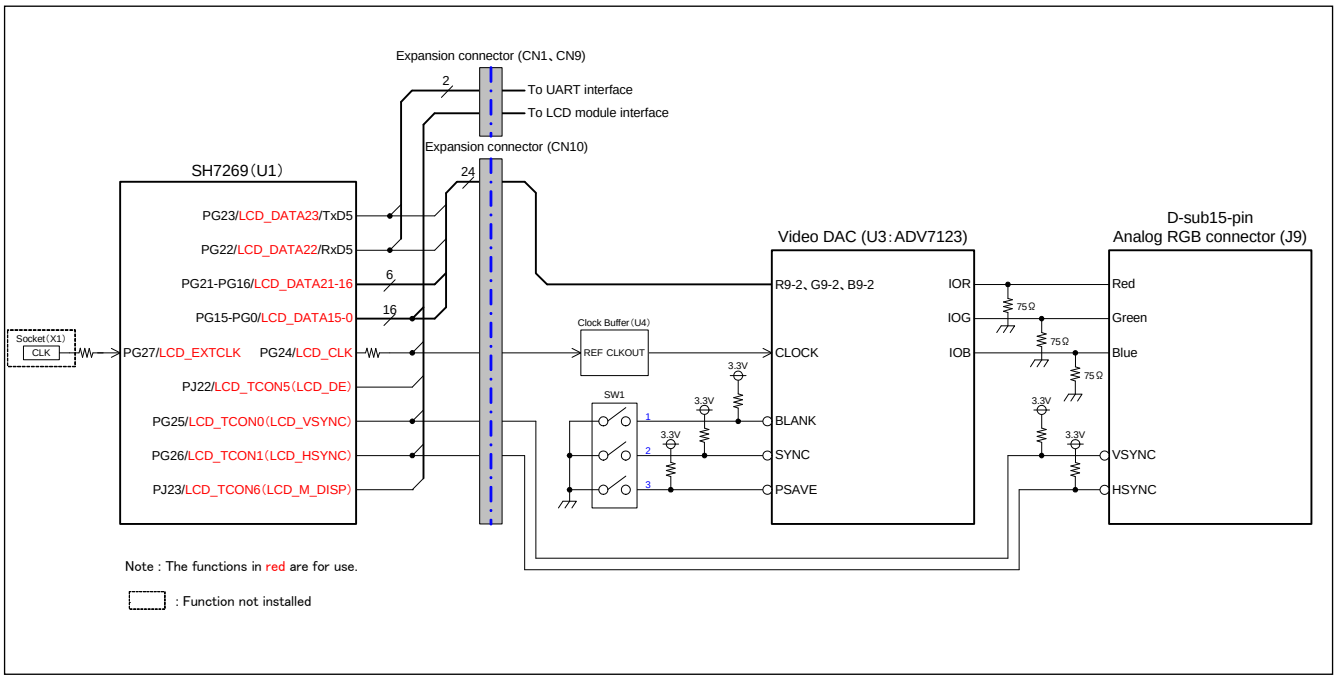

Figure2.4.1 Analog RGB Output Interface Block Wiring Diagram

2.5 Digital RGB Signal Input Interface

The R0K572690B000BR includes a digital RGB input connector for the SH7269 VDC4 to input the digital RGB signal which complies with ITU-R BT .656 and BT.601.
Figure2.5.1 shows the digital RGB signal input interface block wiring diagram.

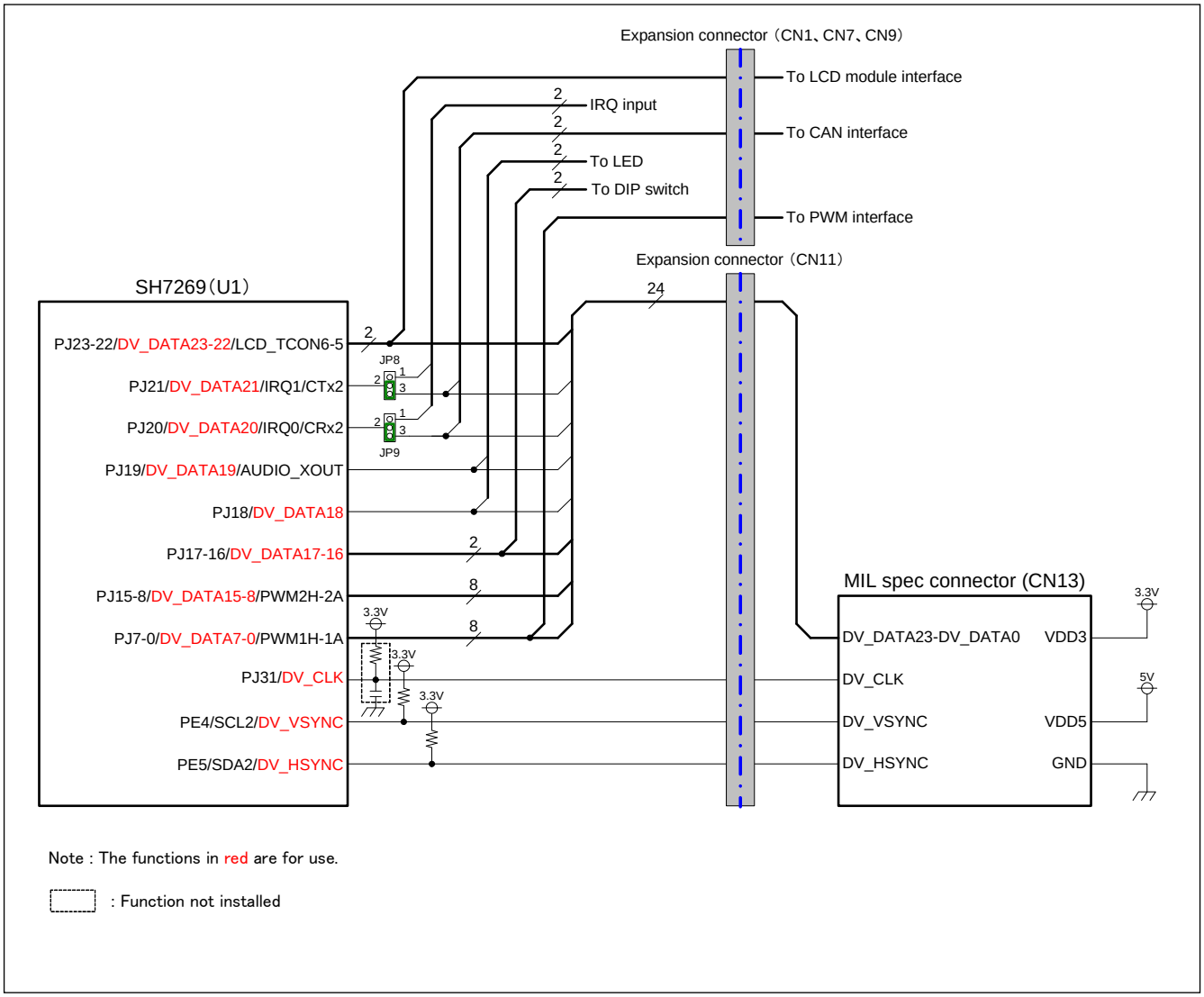

Figure2.5.1 Digital RGB Signal Input Interface Block Wiring Diagram

Table2.5.1 R0K572690C000BR Jumper Setting for JP8 and JP9

Jamer	1-2	2-3
JP8	Uses PJ21 as IRQ1 input pin (setting by default)	Uses PJ21 as CTx2 output / DV_DATA21 input pin
JP9	Uses PJ20 as IRQ0 input pin (setting by default)	Uses PJ20 as CRx2 inpout / DV_DATA20 input pin

…. : Set function

2.6 Clock Module

The following six clocks are input to the SH7269 on the R0K572690C000BR.

- SH7269 inpout clock (X4) : 13.33MHz
- SH7269 RTC clock (X5) : 32.768kHz
- SH7269 audio clock (X8) : 11.2896MHz
- SH7269 USB clock (X6) : 48.00MHz
- SH7269 LCD clock (X1) : Not installed
- SH7269 digital video decoder clock (X2) : 27.00MHz

Figure2.6.1 shows the clock module block diagram on the R0K572690C000BR and on the R0K572690B000BR.

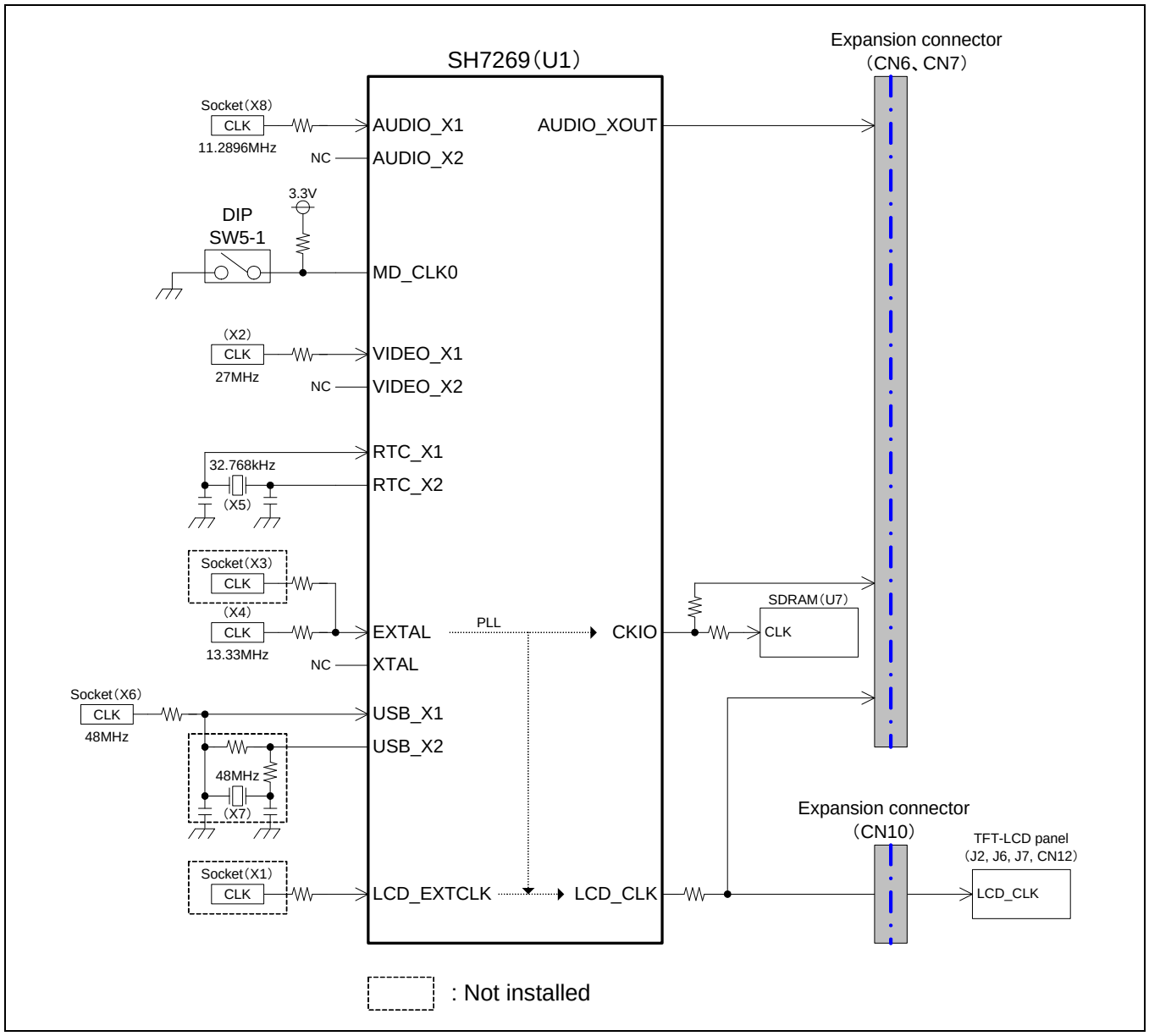

Figure2.6.1 Clock Module Block Wiring Diagram

2.7 Power Supply Module

R0K572690B000BR is operated by 5V or 3.3V power supplied from the R0K572690C000BR. The video DAC analog 3.3V power to use for analog RGB output is generated on the R0K572690B000BR.
Figure2.7.1 shows the power supply module block wiring diagram.

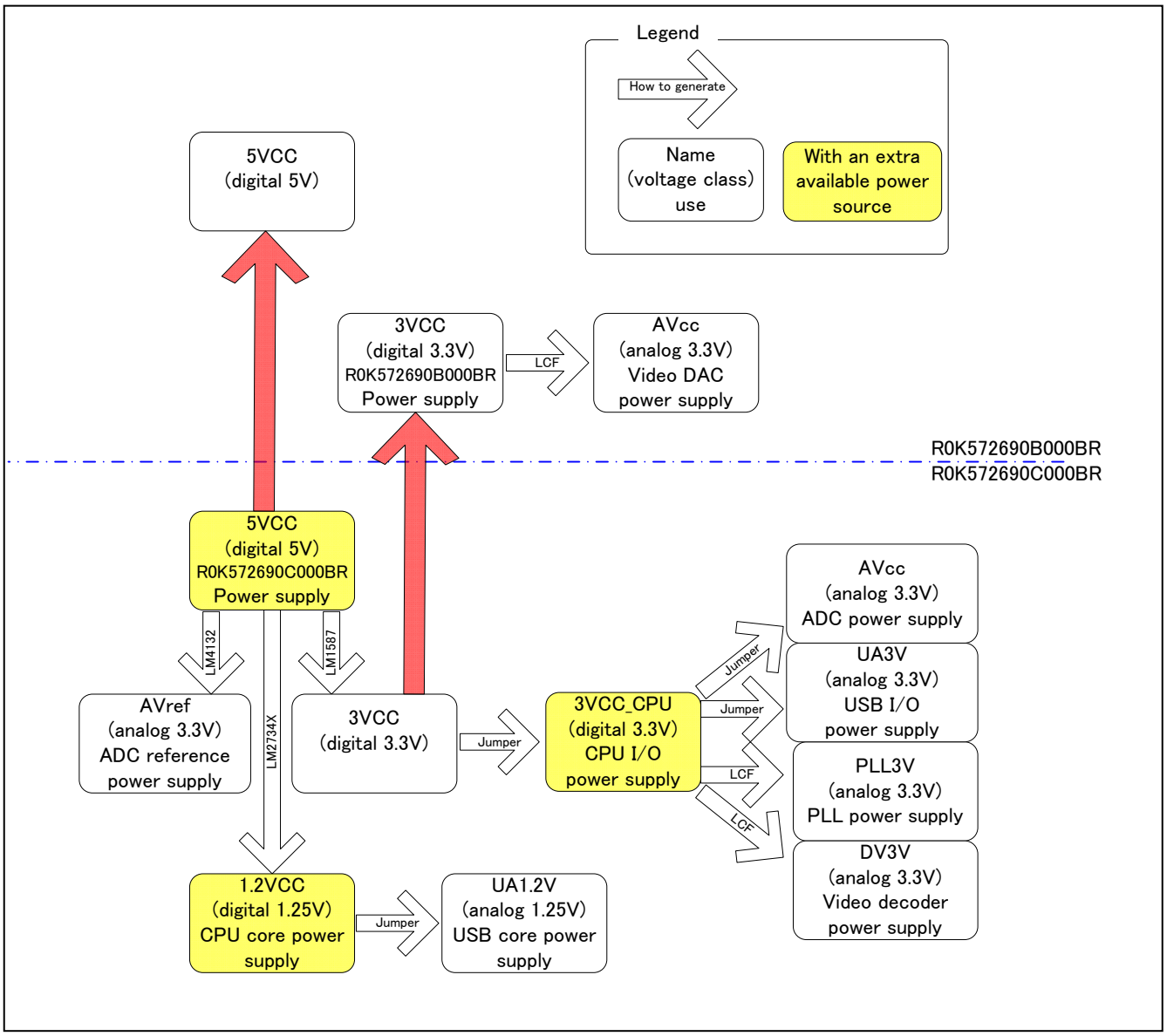

Figure2.7.1 Power Supply Module Block Wiring Diagram

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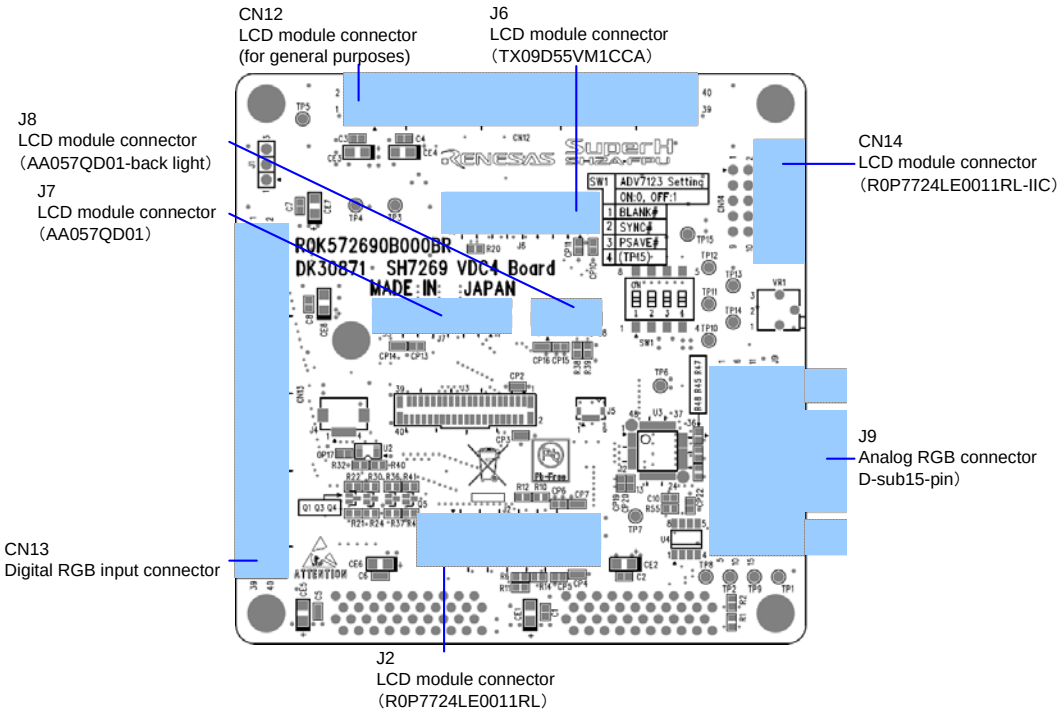
3. Operational Specification

3.1 Connector Overview

Figure 3.1.1 shows the connector assignments on the R0K572690B000BR..

<Top view of the component side>



<Top view of the solder side>

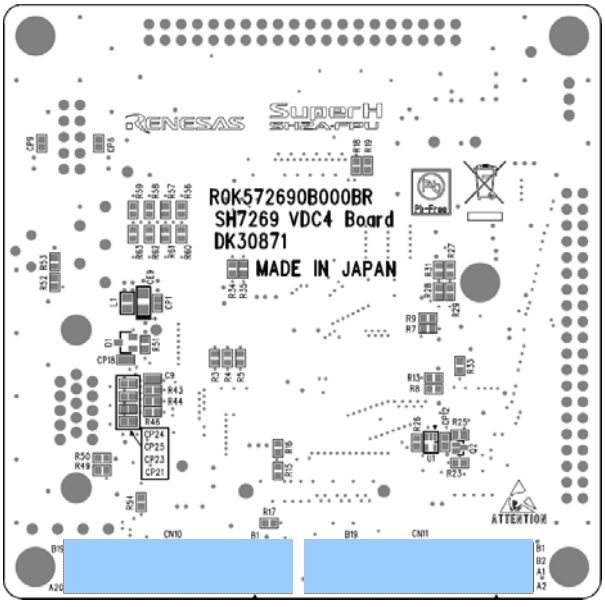


Figure 3.1.1 R0K572690B000BR Connector Assignments

3.1.1 R0K572690C000BR Connectors (CN10 and CN11)

The R0K572690B000BR includes 40-pin half pitch connectors (CN10 and CN11) to be connected to the R0K572690C000BR.
Figure3.1.2 shows the connector assignments of the R0K572690C000BR.
Table 3.1.1 and Table3.1.2 list their descriptions..

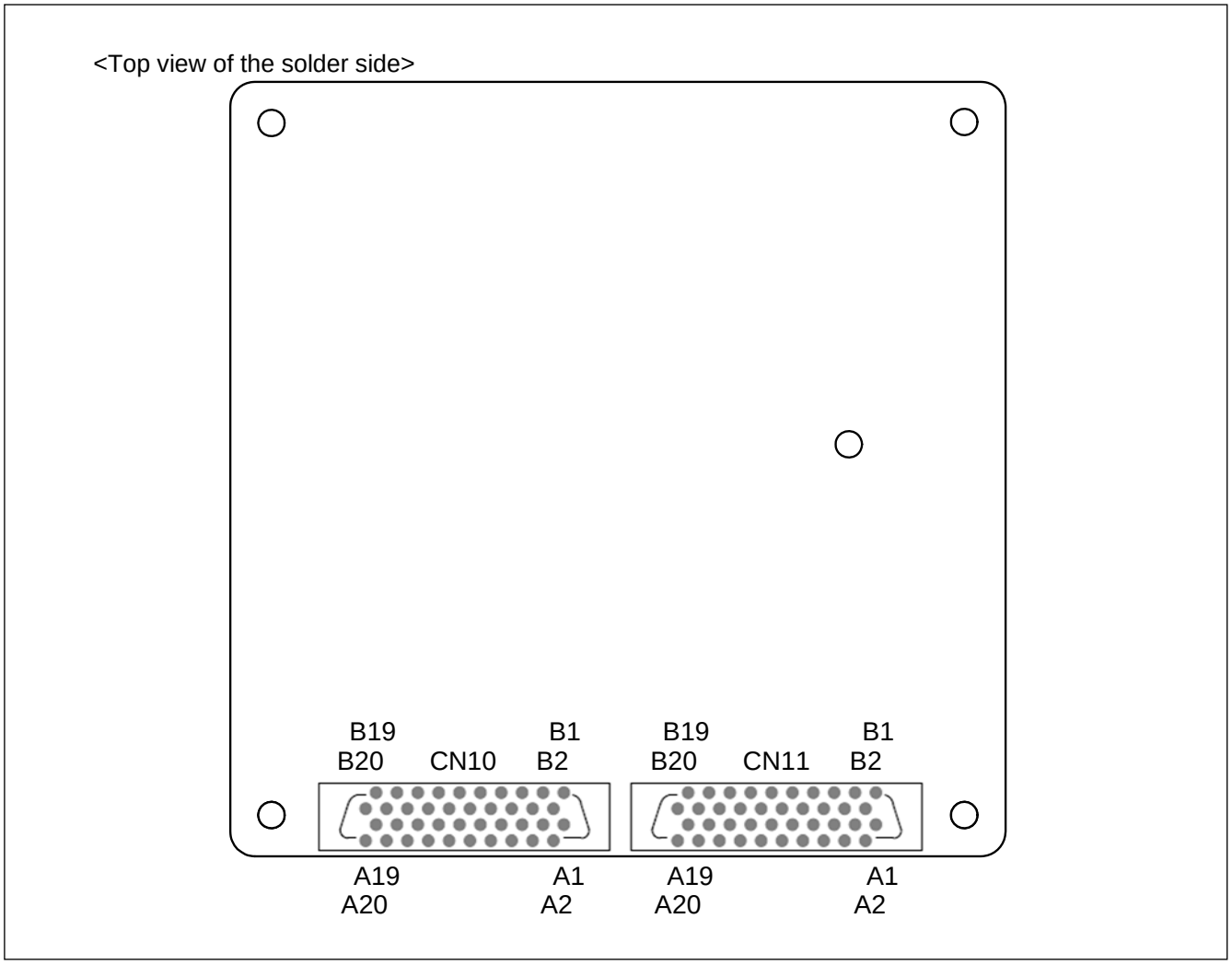


Figure3.1.2 R0K572690C000BR Connector Assignments (CN10, CN11)

Table 3.1.1 R0K572690C000BR Connector Descriptions 1 (CN10)

Pin	Signal Name	Pin	Signal Name
A1	PG0 / D16 / LCD_DATA0 / IRQ0 / TIOC0A	B1	PG1 / D17 / LCD_DATA1 / IRQ1 / TIOC0B
A2	PG2 / D18 / LCD_DATA2 / IRQ2 / TIOC0C	B2	PG3 / D19 / LCD_DATA3 / IRQ3 / TIOC0D
A3	+3.3V	B3	PG4 / D20 / LCD_DATA4 / IRQ4 / TIOC1A
A4	PG5 / D21 / LCD_DATA5 / IRQ5 / TIOC1B	B4	PG6 / D22 / LCD_DATA6 / IRQ6 / TIOC2A
A5	PG7 / D23 / LCD_DATA7 / IRQ7 / TIOC2B	B5	+5V
A6	PG8 / D24 / LCD_DATA8 / PINT0 / TIOC3A	B6	PG9 / D25 / LCD_DATA9 / PINT1 / TIOC3B
A7	PG10 / D26 / LCD_DATA10 / PINT2 / TIOC3C	B7	PG11 / D27 / LCD_DATA11 / PINT3 / TIOC3D
A8	+3.3V	B8	PG12 / D28 / LCD_DATA12 / PINT4
A9	PG13 / D29 / LCD_DATA13 / PINT5	B9	PG14 / D30 / LCD_DATA14 / PINT6
A10	PG15 / D31 / LCD_DATA15 / PINT7	B10	+5V
A11	PG16 / WE2#/ICIORD#/DQMUL / LCD_DATA16 / AUDATA0	B11	PG17 / WE3#/ICIOWR#/AH#/DQMUU / LCD_DATA17 / AUDATA1
A12	PG18 / DV_DATA4 / LCD_DATA18 / SPDIF_IN / SCK4	B12	PG19 / DV_DATA5 / LCD_DATA19 / SPDIF_OUT / SCK5
A13	GND	B13	PG20 / DV_DATA6 / LCD_DATA20 / LCD_TCON3 / RxD4
A14	PG21 / DV_DATA7 / LCD_DATA21 / LCD_TCON4 / TxD4 / AUDATA2	B14	PG22 / LCD_DATA22 / LCD_TCON5 / RxD5 / AUDSYNC#
A15	PG23 / LCD_DATA23 / LCD_TCON6 / TxD5 / AUDATA3	B15	GND
A16	PG24 / LCD_CLK	B16	PG25 / LCD_TCON0
A17	PG26 / LCD_TCON1	B17	PJ22 / DV_DATA22 / LCD_DATA22 / LCD_TCON5 / IRQ2 / CRx1 / CRx0/CRx1
A18	GND	B18	PJ23 / DV_DATA23 / LCD_DATA23 / LCD_TCON6 / IRQ3 / CTx1 / CTx0&CTx1
A19	VIN1（NC）	B19	GND
A20	GND	B20	VIN2（NC）

Legend : .... : 5V system power supply, ... : 3.3V system power supply, ... : GND

Table3.1.2 R0K572690C000BR Connector Descriptions 2 (CN11)

Pin	Signal Name	Pin	Signal Name
A1	PJ14 / DV_DATA14 / LCD_DATA14 / PINT6 / PWM2G / TxD6	B1	PJ15 / DV_DATA15 / LCD_DATA15 / PINT7 / PWM2H / TxD7
A2	PJ10 / DV_DATA10 / LCD_DATA10 / PINT2 / PWM2C / SCK5#	B2	PJ11 / DV_DATA11 / LCD_DATA11 / PINT3 / PWM2D / SCK6
A3	+3.3V	B3	PJ9 / DV_DATA9 / LCD_DATA9 / PINT1 / PWM2B / RTS5#
A4	PJ8 / DV_DATA8 / LCD_DATA8 / PINT0 / PWM2A / CTS5#	B4	PJ20 / DV_DATA20 / LCD_DATA20 / LCD_TCON3 / IRQ0 / CRx2 / CRx0/CRx1/CRx2
A5	PJ7 / DV_DATA7 / LCD_DATA7 / SD_D2_1 / PWM1H	B5	+5V
A6	PJ0 / DV_DATA0 / LCD_DATA0 / SD_CD_1 / PWM1A	B6	PJ1 / DV_DATA1 / LCD_DATA1 / SD_WP_1 / PWM1B
A7	PJ5 / DV_DATA5 / LCD_DATA5 / SD_CMD_1 / PWM1F	B7	PJ6 / DV_DATA6 / LCD_DATA6 / SD_D3_1 / PWM1G
A8	+3.3V	B8	PJ18 / DV_DATA18 / LCD_DATA18 / MOSI0 / TIOC0C / SIOFTxD
A9	PJ4 / DV_DATA4 / LCD_DATA4 / SD_CLK_1 / PWM1E	B9	PJ3 / DV_DATA3 / LCD_DATA3 / SD_D0_1 / PWM1D
A10	PJ2 / DV_DATA2 / LCD_DATA2 / SD_D1_1 / PWM1C	B10	+5V
A11	PJ13 / DV_DATA13 / LCD_DATA13 / PINT5 / PWM2F / TxD5	B11	PJ12 / DV_DATA12 / LCD_DATA12 / PINT4 / PWM2E / SCK7
A12	PJ19 / DV_DATA19 / LCD_DATA19 / MISO0 / TIOC0D/ SIOFRxD / AUDIO_XOUT	B12	PJ17 / DV_DATA17 / LCD_DATA17 / SSL00 / TIOC0B / SIOFSYNC
A13	GND	B13	PJ16 / DV_DATA16 / LCD_DATA16 / RSPCK0 / TIOC0A / SIOFSCK
A14	PJ21 / DV_DATA21 / LCD_DATA21 / LCD_TCON4 / IRQ1 / CTx2 / CTx0&CTx1&CTx2	B14	PJ22 / DV_DATA22 / LCD_DATA22 / LCD_TCON5 / IRQ2 / CRx1 / CRx0/CRx1
A15	PJ23 / DV_DATA23 / LCD_DATA23 / LCD_TCON6 / IRQ3 / CTx1 / CTx0&CTx1	B15	GND
A16	PJ31 / DV_CLK	B16	PJ31 / DV_CLK
A17	PE4 / SCL2 / RxD4 / DV_VSYNC	B17	PE5 / SDA2 / RxD5 / DV_HSYNC
A18	GND	B18	PH4 / AN4 / PINT4
A19	PH5 / AN5 / PINT5 / LCD_EXTCLK	B19	PH6 / AN6 / PINT6
A20	PH7 / AN7 / PINT7	B20	GND

Legend : …. : 5V system power supply, …. : 3.3V system power supply, …. : GND

3.1.2 LCD Module Connectors (J2, J6, J7, J8, and CN12)

The R0K572690B000BR includes three flexible connectors (J6, J7, and J8) and one 0.635mm pitch 2-piece connector (J2). The board pattern is available for one MIL spec connector (CN12).
Figure3.1.3 shows the LCD module connector pins assignment. From Table3.1.3 to Table3.1.7 list the pins and descriptions.

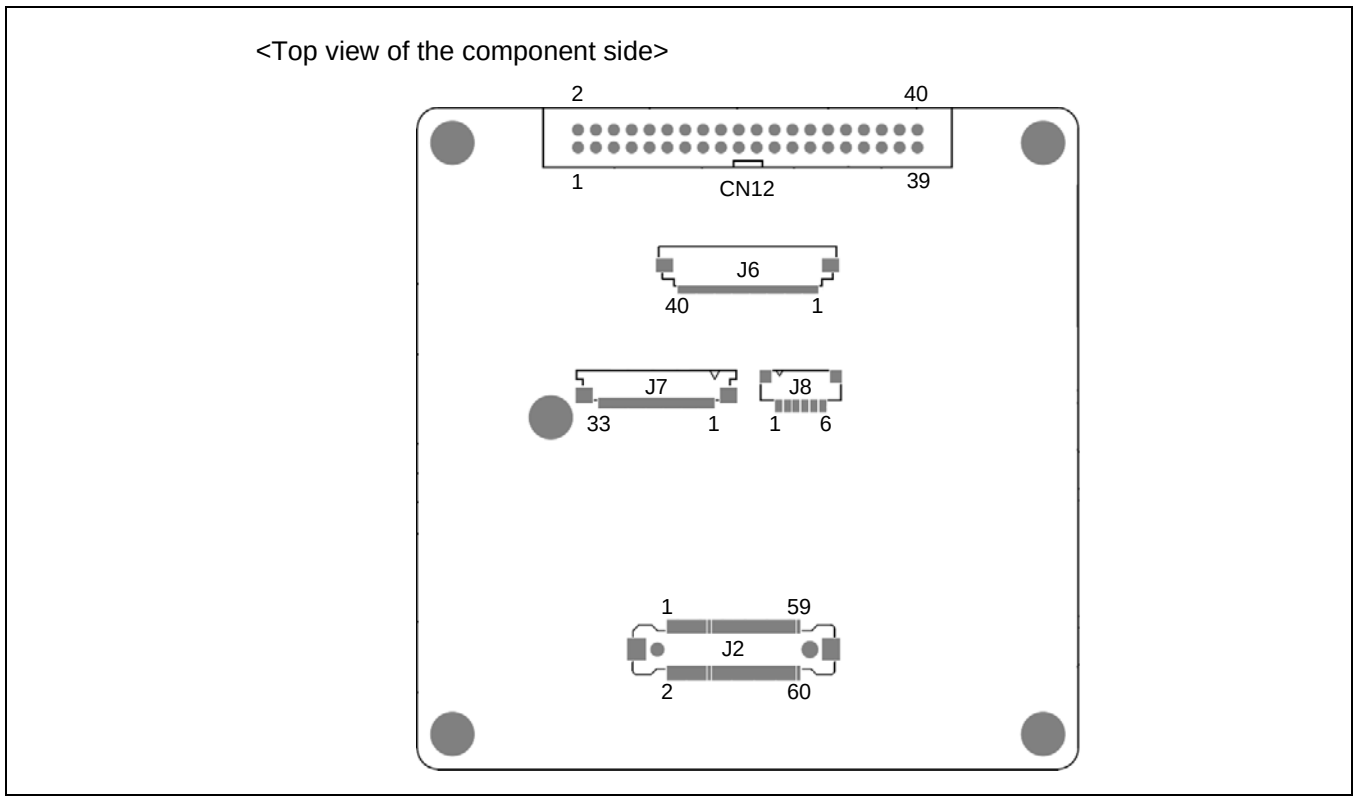


Figure3.1.3 LCD Module Connector Pins Assignment (J2, J6, J7, J8, and CN12)

Table3.1.3 0.635 mm Pitch 2-piece Connector Pin Descriptions for R0P7724LE0011RL (J2)

Pin	Signal Name	Pin	Signal Name
1	GND	2	GND
3	LCD0（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）	4	LCD1（PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B）
5	LCD2（PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C）	6	LCD3（PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D）
7	LCD4（PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A）	8	LCD5（PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B）
9	LCD6（PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A）	10	LCD7（PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B）
11	GND	12	GND
13	LCD8（PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A）	14	LCD9（PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B）
15	LCD10（PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C）	16	LCD11（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）
17	LCD12（PG12 / D28 / **LCD_DATA12** / PINT4）	18	LCD13（PG13 / D29 / **LCD_DATA13** / PINT5）
19	LCD14（PG14 / D30 / **LCD_DATA14** / PINT6）	20	LCD15（PG15 / D31 / **LCD_DATA15** / PINT7）
21	GND	22	GND
23	LCD16（PG16 / WE2#/ICIORD#/DQMUL / **LCD_DATA16** / AUDATA0）	24	LCD17（PG17 / WE3#/ICIOWR#/AH#/DQMUU / **LCD_DATA17** / AUDATA1）
25	LCD18（PG18 / DV_DATA4 / **LCD_DATA18** / SPDIF_IN / SCK4）	26	LCD19（PG19 / DV_DATA5 / **LCD_DATA19** / SPDIF_OUT / SCK5）
27	LCD20（PG20 / DV_DATA6 / **LCD_DATA20** / LCD_TCON3 / RxD4）	28	LCD21（PG21 / DV_DATA7 / **LCD_DATA21** / LCD_TCON4 / TxD4 / AUDATA2）
29	LCD22（PG22 / **LCD_DATA22** / LCD_TCON5 / RxD5 / AUDSYNC#）	30	LCD23（PG23 / **LCD_DATA23** / LCD_TCON6 / TxD5 / AUDATA3）
31	GND	32	GND
33	LCDVSYN（PG25 / **LCD_TCON0**）	34	LCDDISP/RS（PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1）
35	LCDHSYN/CS#（PG26 / **LCD_TCON1**）	36	LCDRD#（NC）
37	GND	38	GND
39	LCDDCK/WR#（PG24 / **LCD_CLK**）	40	BKPWM（+3.3V）
41	GND	42	GND
43	LCDDON（+3.3V）	44	LCDVEPWC（NC）
45	LCDCPWC（NC）	46	GND
47	GND	48	SDA0（PE5 / **SDA2** / RxD5 / DV_HSYNC）
49	SCL0（PE4 / **SCL2** / RxD4 / DV_VSYNC）	50	GND
51	GND	52	TP_IRQ#（PJ23 / DV_DATA23 / LCD_DATA23 / LCD_TCON6 / **IRQ3** / CTx1 / CTx0&CTx1）
53	+3.3V	54	+3.3V
55	+3.3V	56	GND
57	GND	58	+5V
59	+5V	60	+5V

Note: The signal names in bold style are set functions.

Table3.1.4 Flexible Connector Pin Descriptions for TX09D55VM1CCA (J6)

Pin	Signal Name	Pin	Signal Name
1	+3.3V	2	+3.3V
3	+3.3V	4	DCLK（PG24 / **LCD_CLK**）
5	GND	6	HSYNC（PG26 / **LCD_TCON1**）
7	GND	8	DTMG（PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1）
9	GND	10	NC
11	GND	12	R5（PG17 / WE3#/ICIOWR#/AH#/DQMUU / **LCD_DATA17** / AUDATA1）
13	R4（PG16 / WE2#/ICIORD#/DQMUL / **LCD_DATA16** / AUDATA0）	14	R3（PG15 / D31 / **LCD_DATA15** / PINT7）
15	GND	16	R2（PG14 / D30 / **LCD_DATA14** / PINT6）
17	R1（PG13 / D29 / **LCD_DATA13** / PINT5）	18	R0（PG12 / D28 / **LCD_DATA12** / PINT4）
19	GND	20	G5（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）
21	G4（PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C）	22	G3（PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B）
23	GND	24	G2（PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A）
25	G1（PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B）	26	G0（PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A）
27	GND	28	B5（PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B）
29	B4（PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A）	30	B3（PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D）
31	GND	32	B2（PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C）
33	B1（PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B）	34	B0（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）
35	PCI（+3.3V）	36	Vctrl（+3.3V）
37	XR（**PH4** / AN4 / PINT4）	38	YL（**PH5** / AN5 / PINT5 / LCD_EXTCLK）
39	XL（**PH6** / AN6 / PINT6）	40	YU（**PH7** / AN7 / PINT7）

Note: The signal names in bold style are set functions.

Table3.1.5 Flexible Connector Pin Descriptions for AA057QD01 (J7)

Pin	Signal Name	Pin	Signal Name
1	GND	2	DCLK（PG24 / **LCD_CLK**）
3	HD（PG26 / **LCD_TCON1**）	4	VD（PG25 / **LCD_TCON0**）
5	GND	6	R0（PG12 / D28 / **LCD_DATA12** / PINT4）
7	R1（PG13 / D29 / **LCD_DATA13** / PINT5）	8	R2（PG14 / D30 / **LCD_DATA14** / PINT6）
9	R3（PG15 / D31 / **LCD_DATA15** / PINT7）	10	R4（PG16 / WE2#/ICIORD#/DQMUL / **LCD_DATA16** / AUDATA0）
11	R5（PG17 / WE3#/ICIOWR#/AH#/DQMUU / **LCD_DATA17** / AUDATA1）	12	GND
13	G0（PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A）	14	G1（PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B）
15	G2（PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A）	16	G3（PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B）
17	G4（PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C）	18	G5（PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D）
19	GND	20	B0（PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A）
21	B1（PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B）	22	B2（PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C）
23	B3（PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D）	24	B4（PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A）
25	B5（PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B）	26	GND
27	DENA（PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1）	28	+3.3V
29	+3.3V	30	R/L（GND）
31	U/D（+3.3V）	32	NC
33	GND	-	

Note: The signal names in bold style are set functions.

Table3.1.6 Back Light Flexible Connector Pin Descriptions for AA057QD01 (J8)

Pin	Signal Name	Pin	Signal Name
1	+5V	2	+5V
3	GND	4	GND
5	BLEN（+3.3V）	6	PDIM（+3.3V）

Table3.1.7 MIL Spec Connector for General Purposes Pin Descriptions (CN12)

Pin	Signal Name	Pin	Signal Name
1	PG0 / D16 / **LCD_DATA0** / IRQ0 / TIOC0A	2	PG1 / D17 / **LCD_DATA1** / IRQ1 / TIOC0B
3	PG2 / D18 / **LCD_DATA2** / IRQ2 / TIOC0C	4	PG3 / D19 / **LCD_DATA3** / IRQ3 / TIOC0D
5	+3.3V	6	PG4 / D20 / **LCD_DATA4** / IRQ4 / TIOC1A
7	PG5 / D21 / **LCD_DATA5** / IRQ5 / TIOC1B	8	PG6 / D22 / **LCD_DATA6** / IRQ6 / TIOC2A
9	PG7 / D23 / **LCD_DATA7** / IRQ7 / TIOC2B	10	+5V
11	PG8 / D24 / **LCD_DATA8** / PINT0 / TIOC3A	12	PG9 / D25 / **LCD_DATA9** / PINT1 / TIOC3B
13	PG10 / D26 / **LCD_DATA10** / PINT2 / TIOC3C	14	PG11 / D27 / **LCD_DATA11** / PINT3 / TIOC3D
15	+3.3V	16	PG12 / D28 / **LCD_DATA12** / PINT4
17	PG13 / D29 / **LCD_DATA13** / PINT5	18	PG14 / D30 / **LCD_DATA14** / PINT6
19	PG15 / D31 / **LCD_DATA15** / PINT7	20	+5V
21	PG16 / WE2#/ICIORD#/DQMUL / **LCD_DATA16** / AUDATA0	22	PG17 / WE3#/ICIOWR#/AH#/DQMUU / **LCD_DATA17** / AUDATA1
23	PG18 / DV_DATA4 / **LCD_DATA18** / SPDIF_IN / SCK4	24	PG19 / DV_DATA5 / **LCD_DATA19** / SPDIF_OUT / SCK5
25	GND	26	PG20 / DV_DATA6 / **LCD_DATA20** / LCD_TCON3 / RxD4
27	PG21 / DV_DATA7 / **LCD_DATA21** / LCD_TCON4 / TxD4 / AUDATA2	28	PG22 / **LCD_DATA22** / LCD_TCON5 / RxD5 / AUDSYNC#
29	PG23 / **LCD_DATA23** / LCD_TCON6 / TxD5 / AUDATA3	30	GND
31	PG24 / **LCD_CLK**	32	PG25 / **LCD_TCON0**
33	PG26 / **LCD_TCON1**	34	PJ22 / DV_DATA22 / LCD_DATA22 / **LCD_TCON5** / IRQ2 / CRx1 / CRx0/CRx1
35	GND	36	PJ23 / DV_DATA23 / LCD_DATA23 / **LCD_TCON6** / IRQ3 / CTx1 / CTx0&CTx1
37	NC	38	NC
39	NC	40	GND

Note: The signal names in bold style are set functions.

3.1.3 Digital RGB Input Connector (CN13)

The R0K572690B000BR includes a digital RGB input connector (CN14) for the SH7269 VDC4.
Figure3.1.4 shows the digital RGB input connector pins assignment. Table3.1.8 lists the pins and descriptions.

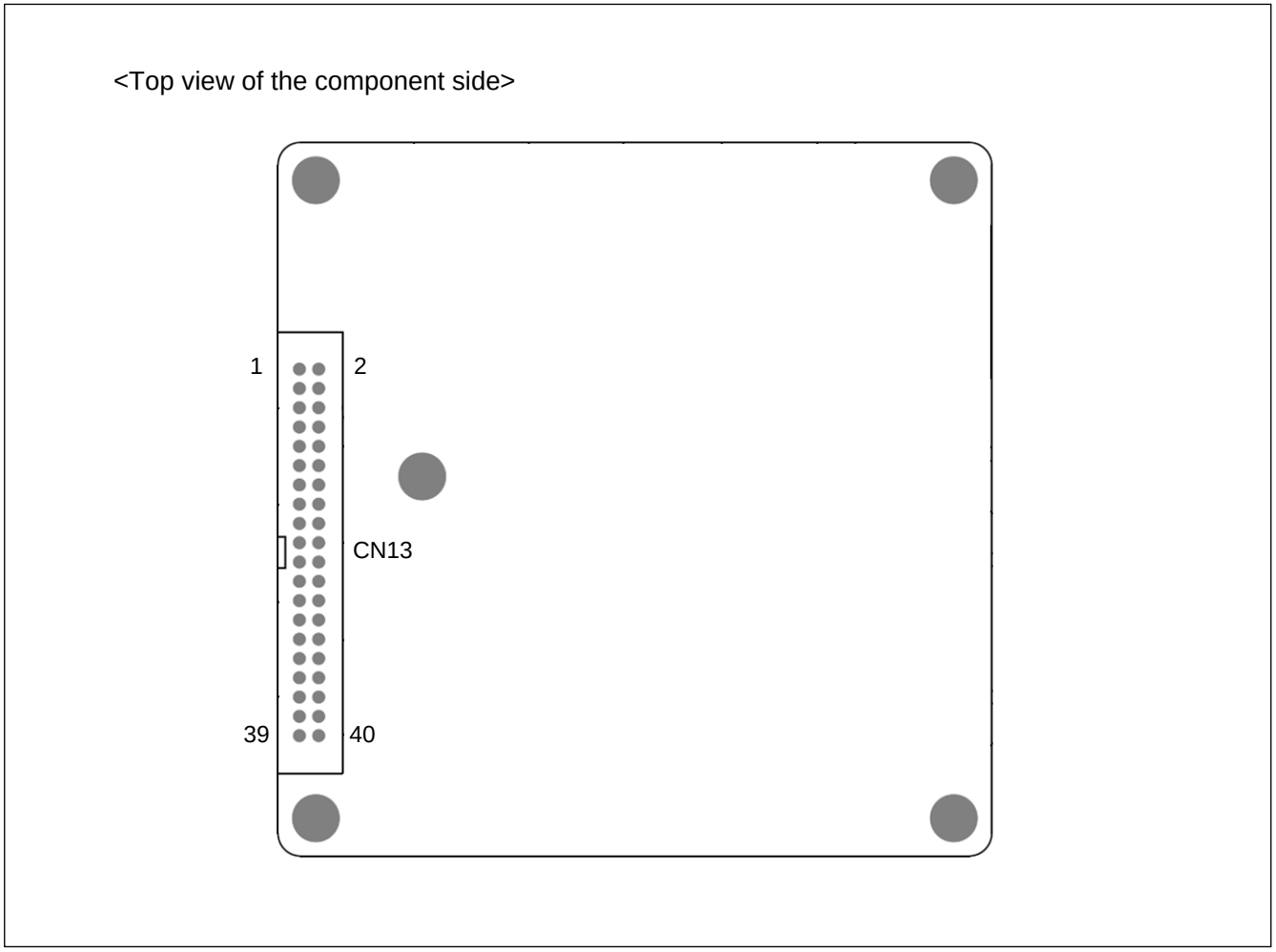


Figure3.1.4 Digital RGB Input Connector Pins Assignment (CN13)

Table3.1.8 Digital RGB Input Connector Pin Descriptions (CN13)

Pin	Signal Name	Pin	Signal Name
1	PJ14 / **DV_DATA14** / LCD_DATA14 / PINT6 / PWM2G / TxD6	2	PJ15 / **DV_DATA15** / LCD_DATA15 / PINT7 / PWM2H / TxD7
3	PJ10 / **DV_DATA10** / LCD_DATA10 / PINT2 / PWM2C / SCK5#	4	PJ11 / **DV_DATA11** / LCD_DATA11 / PINT3 / PWM2D / SCK6
5	+3.3V	6	PJ9 / **DV_DATA9** / LCD_DATA9 / PINT1 / PWM2B / RTS5#
7	PJ8 / **DV_DATA8** / LCD_DATA8 / PINT0 / PWM2A / CTS5#	8	PJ20 / **DV_DATA20** / LCD_DATA20 / LCD_TCON3 / IRQ0 / CRx2 / CRx0/CRx1/CRx2
9	PJ7 / **DV_DATA7** / LCD_DATA7 / SD_D2_1 / PWM1H	10	+5V
11	PJ0 / **DV_DATA0** / LCD_DATA0 / SD_CD_1 / PWM1A	12	PJ1 / **DV_DATA1** / LCD_DATA1 / SD_WP_1 / PWM1B
13	PJ5 / **DV_DATA5** / LCD_DATA5 / SD_CMD_1 / PWM1F	14	PJ6 / **DV_DATA6** / LCD_DATA6 / SD_D3_1 / PWM1G
15	+3.3V	16	PJ18 / **DV_DATA18** / LCD_DATA18 / MOSI0 / TIOC0C / SIOFTxD
17	PJ4 / **DV_DATA4** / LCD_DATA4 / SD_CLK_1 / PWM1E	18	PJ3 / **DV_DATA3** / LCD_DATA3 / SD_D0_1 / PWM1D
19	PJ2 / **DV_DATA2** / LCD_DATA2 / SD_D1_1 / PWM1C	20	+5V
21	PJ13 / **DV_DATA13** / LCD_DATA13 / PINT5 / PWM2F / TxD5	22	PJ12 / **DV_DATA12** / LCD_DATA12 / PINT4 / PWM2E / SCK7
23	PJ19 / **DV_DATA19** / LCD_DATA19 / MISO0 / TIOC0D/ SIOFRxD / AUDIO_XOUT	24	PJ17 / **DV_DATA17** / LCD_DATA17 / SSL00 / TIOC0B / SIOFSYNC
25	GND	26	PJ16 / **DV_DATA16** / LCD_DATA16 / RSPCK0 / TIOC0A / SIOFSCK
27	PJ21 / **DV_DATA21** / LCD_DATA21 / LCD_TCON4 / IRQ1 / CTx2 / CTx0&CTx1&CTx2	28	PJ22 / **DV_DATA22** / LCD_DATA22 / LCD_TCON5 / IRQ2 / CRx1 / CRx0/CRx1
29	PJ23 / **DV_DATA23** / LCD_DATA23 / LCD_TCON6 / IRQ3 / CTx1 / CTx0&CTx1	30	GND
31	NC	32	PJ31 / **DV_CLK**
33	PE4 / SCL2 / RxD4 / **DV_VSYNC**	34	PE5 / SDA2 / RxD5 / **DV_HSYNC**
35	GND	36	**PH4** / AN4 / PINT4
37	**PH5** / AN5 / PINT5 / LCD_EXTCLK	38	**PH6** / AN6 / PINT6
39	**PH7** / AN7 / PINT7	40	GND

Note: The signal names in bold style are set functions.

3.1.4 Analog RGB Output Connector (J9)

Through the video DAC on the R0K572690B000BR, TFT-LCD output digital RGB signal is converted to the analog RGB signal to output to the connector (J9) assigned to D-sub15 pin.
Figure3.1.5 shows analog RGB output connector pins assignment. Table3.1.9 lists the pins and descriptions.

<Top view of the component side>

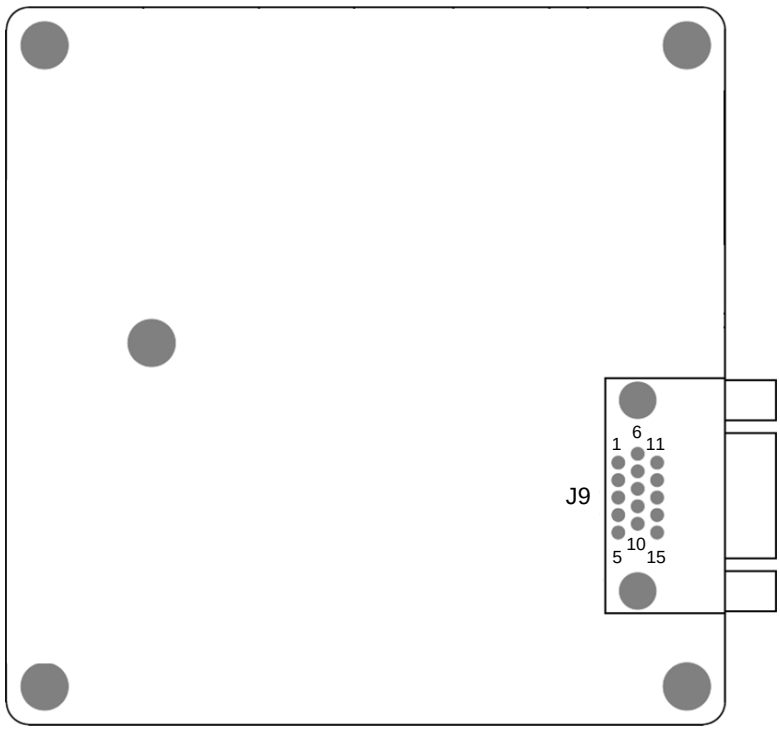


Figure3.1.5 Analog RGB Output Connector Pins Assignment (J9)

Table3.1.9 Analog RGB Output Connector Pin Descriptions (J9)

Pin	Signal Name	Pin	Signal Name
1	Video signal (red)	2	Video signal (green)
3	Video signal (blue)	4	NC
5	GND	6	GND
7	GND	8	GND
9	NC	10	GND
11	NC	12	NC
13	HSYNC（PG26 / **LCD_TCON1**）	14	VSYNC（PG25 / **LCD_TCON0**）
15	NC	-	

Note: The signal names in bold style are set functions.

3.2 R0K572690B000BR Operational Components Diagram

Figure3.2.1 shows the operational components diagram on the R0K572690B000BR.

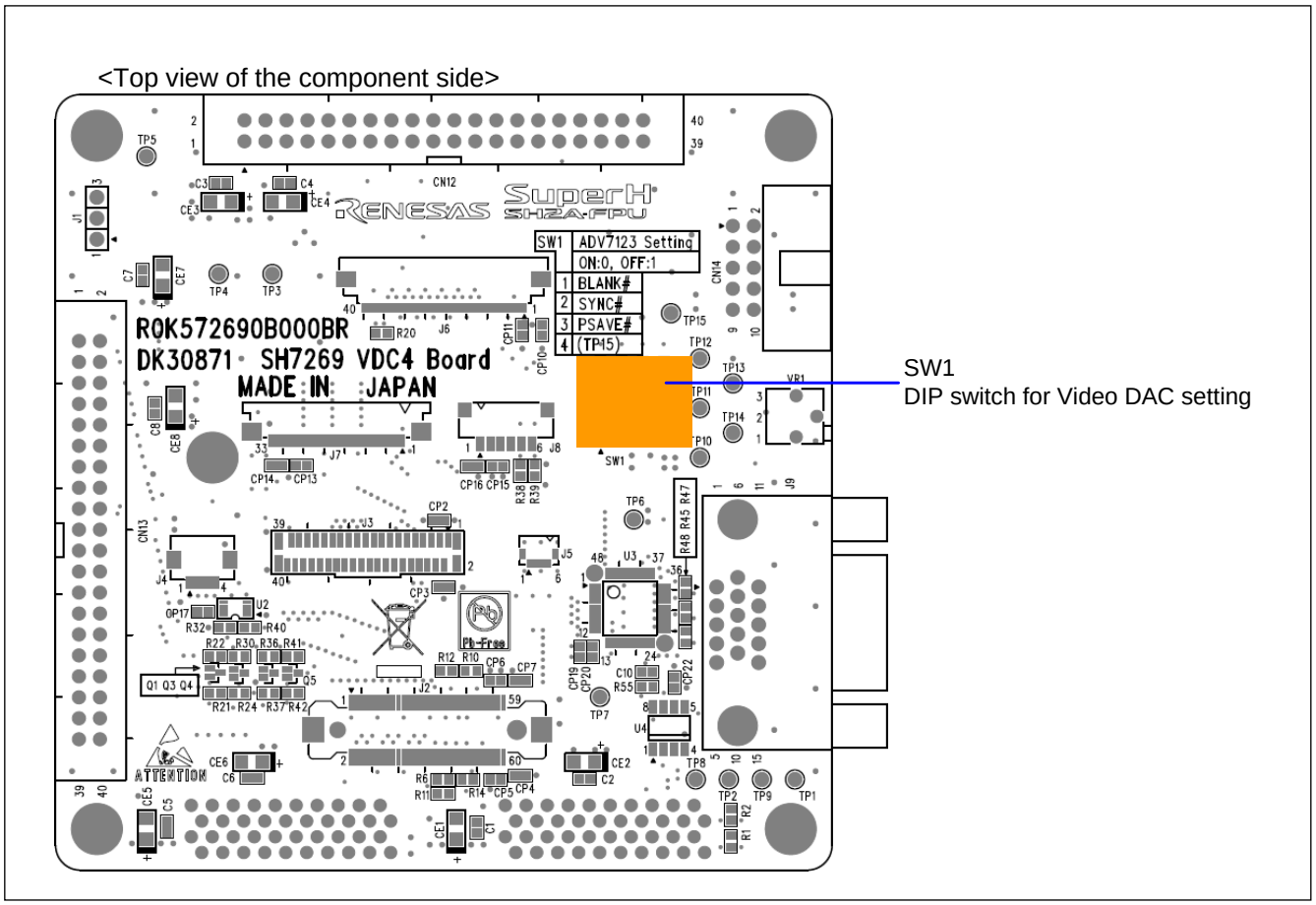


Figure3.2.1 R0K572690B000BR Operational Components Diagram

3.2.1 Switch and LEDs

R0K572690B000BR includes one switch.

Figure3.2.2 shows the switch assignment. Table3.2.2 lists the functions of the switches.

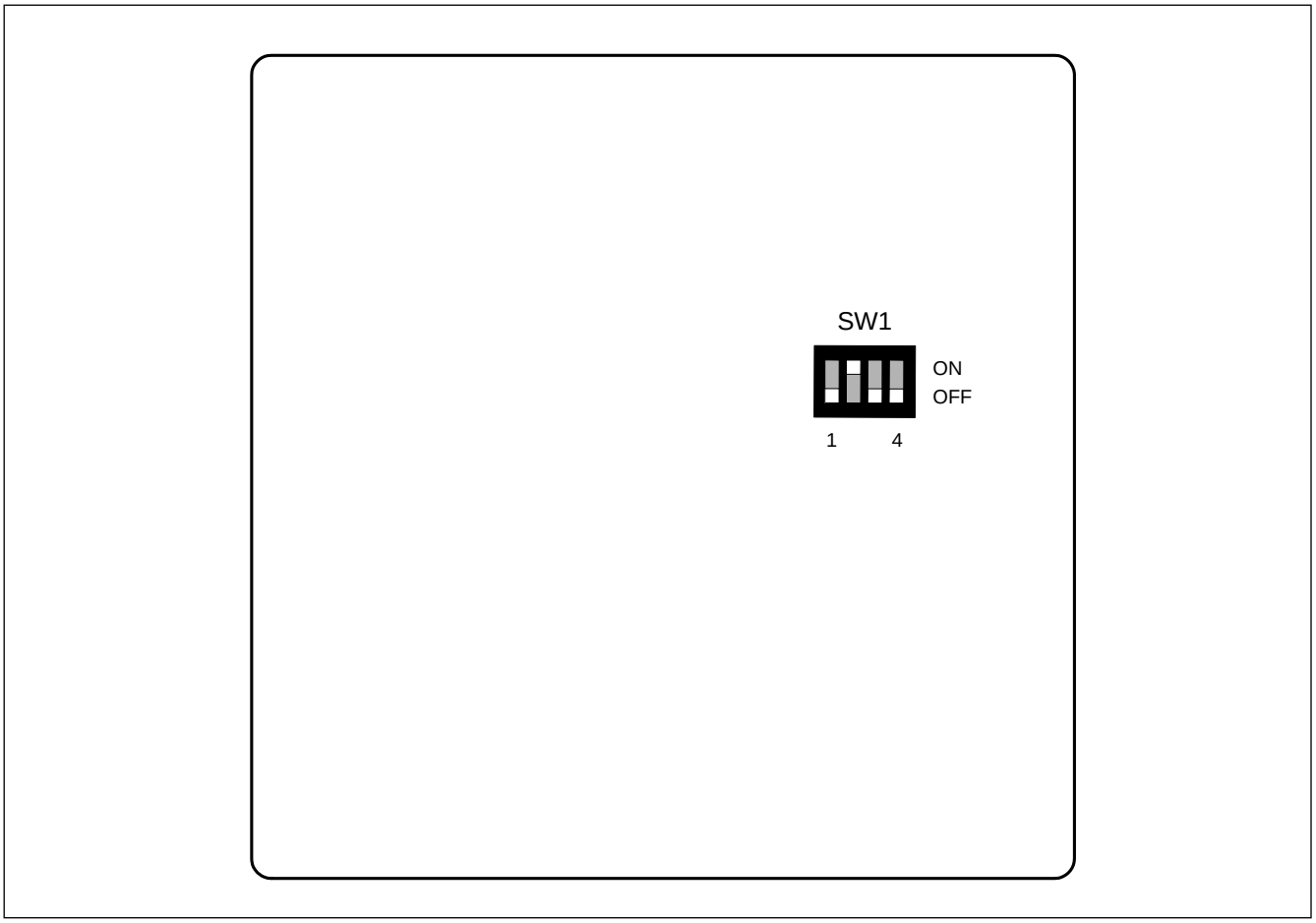


Figure3.2.2 R0K572690B000BR Switch Assignment

Table3.2.1 R0K572690B000BR Switch Description

Number	Description	Remarks
SW1	Video DAC setting switch (4 poles)	For the details, refer to Table3.2.2

Table3.2.2 DIP Switch for Video DAC Setting

Number	Setting		Function
SW1-1 BLANK pin setting	OFF	BLANK = “H”	Regular analog output
	ON	BLANK = “L”	Fixes analog outputs to the blanking level (IOR、IOB、IOG)
SW1-2 SYNC pin setting	OFF	SYNC = “H”	Not disconnect 40IRE power supply
	ON	SYNC = “L”	Disconnect 40IRE power supply
SW1-3 PSAVE pin setting	OFF	PSAVE = “H”	Regular operation mode
	ON	PSAVE = “L”	Power down mode
SW1-4 TP15 setting	OFF	TP15 = “H”	
	ON	TP15 = “L”	

3.3 R0K572690B000BR Dimensions

Figure3.3.1 shows the dimension of the R0K572690B000BR on the top view of the component side. Figure3.3.2 shows the dimension of its perspective view on the component side.

<Top view of the component side> Unit : mm

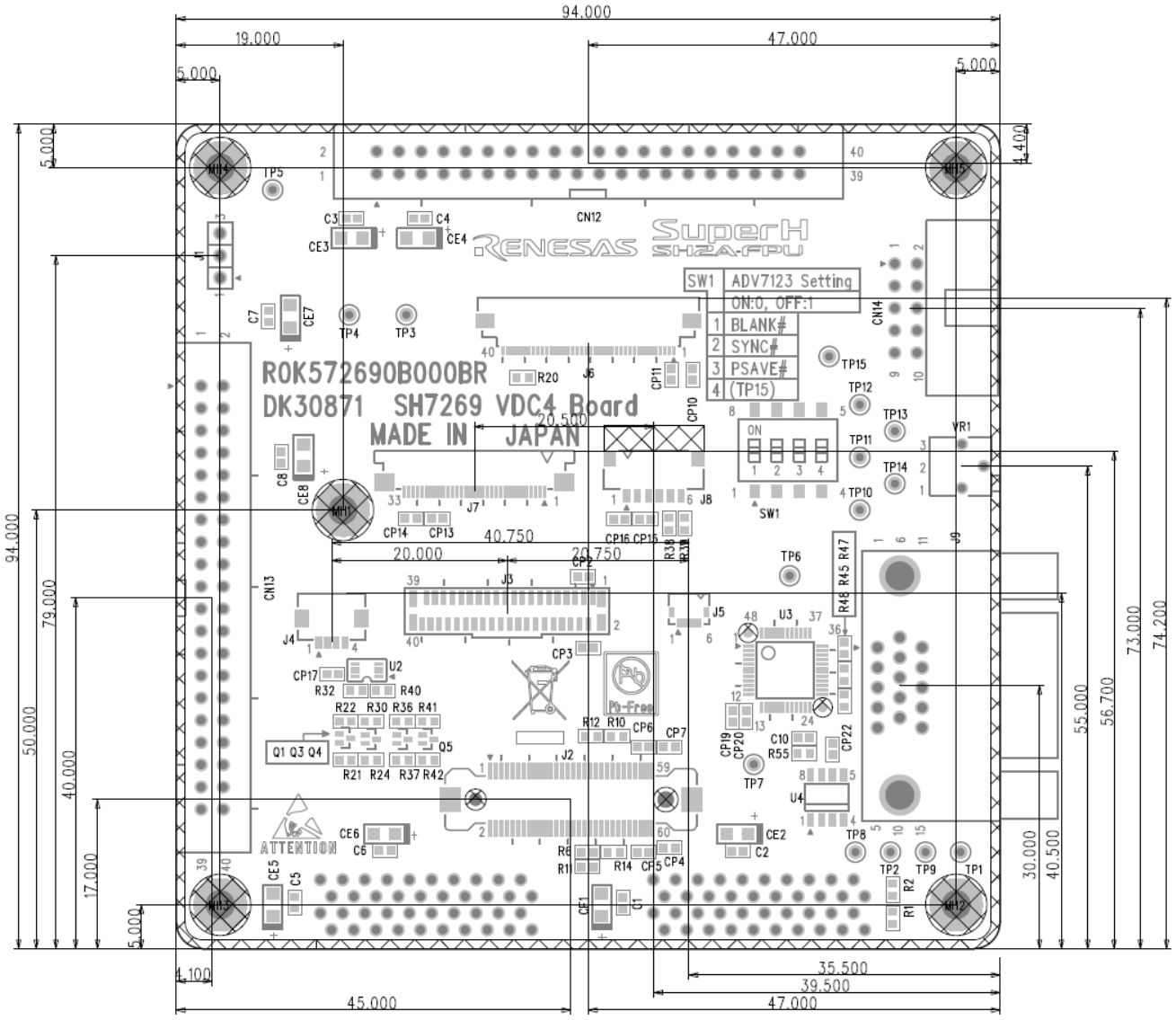


Figure3.3.1 R0K572690B000BR Dimension

<Perspective view of the component side> Unit : mm

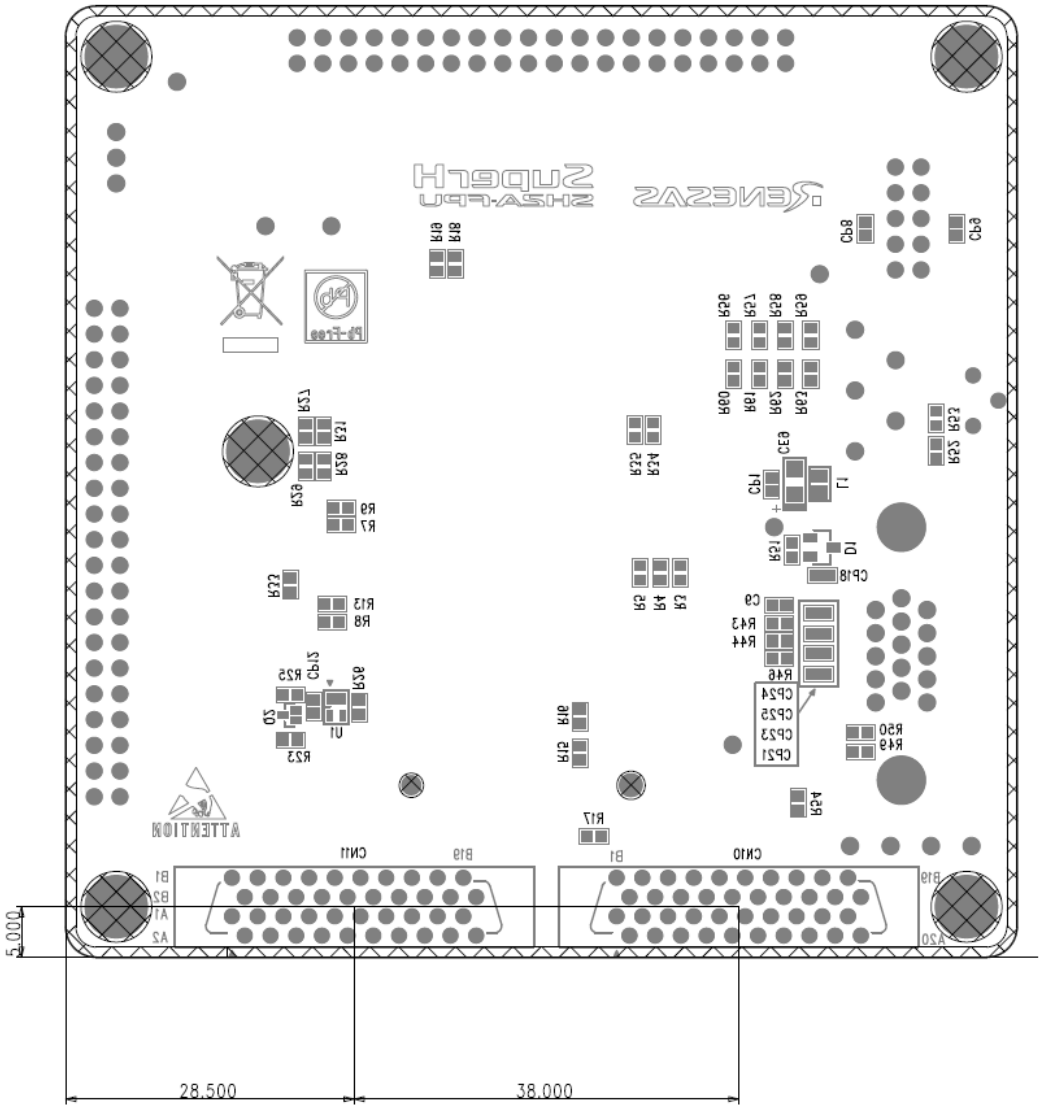


Figure3.3.2 R0K572690B000BR Dimension

Appendix Connection Diagram

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SH7269 CPU board R0K572690C000BR SCHEMATICS

Note:

Digital GND (GND)

Analog GND (AVss)

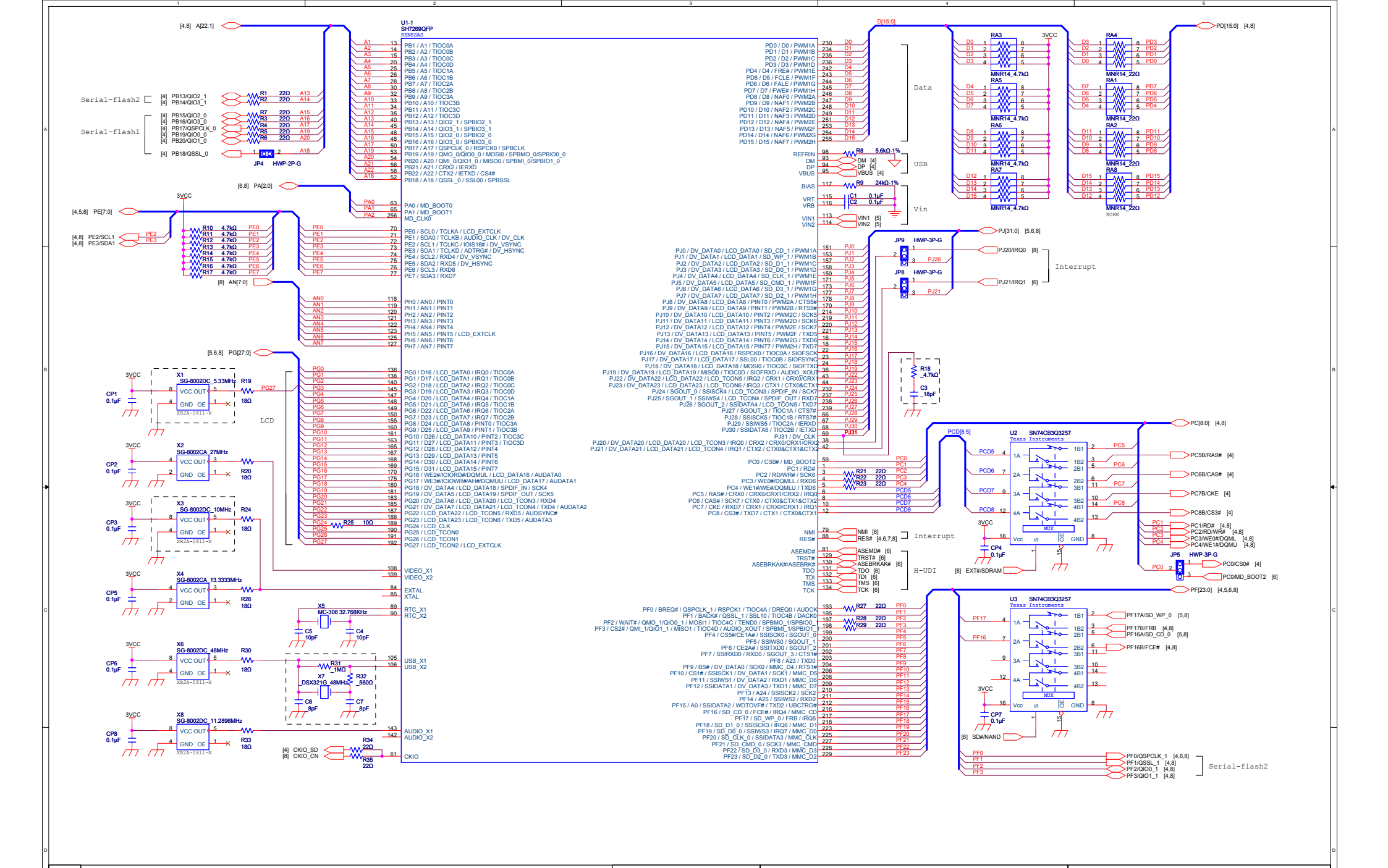
USB Analog GND (USB_AVSS)

Not mounted

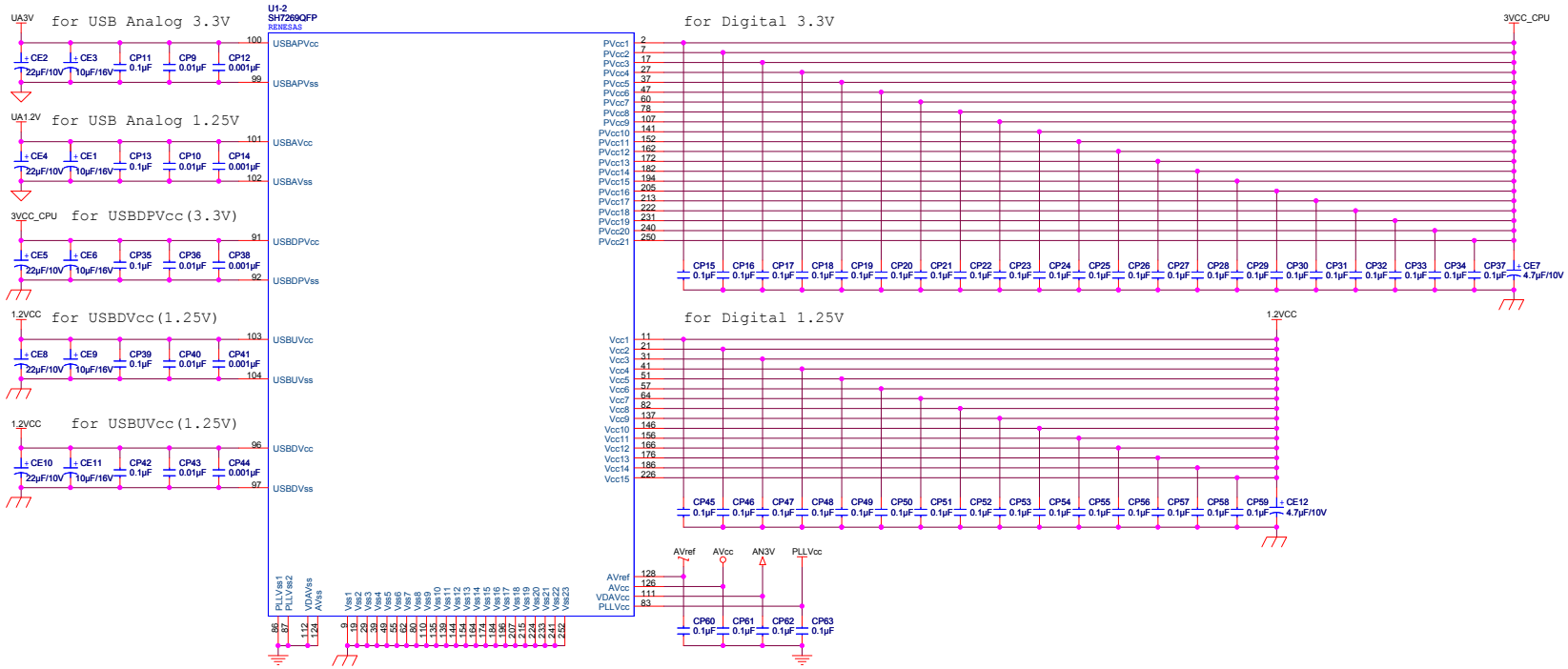
5VCC = Digital 5V
3VCC = Digital 3.3V
3VCC_CPU = 3.3V for CPU I/O
1.2VCC = 1.25V for CPU Core
PLLVcc = Analog 3.3V for PLL
UA3V = Analog 3.3V for USB
UA1.2V = Analog 1.25V for USB
AVcc = Analog 3.3V
AVref = 3.3V for ADC Voltage Reference
AN3V = Analog 3.3V for Video

R = Fixed Resistors
RA = Resistor Array
C = Ceramic Caps
CE = Tantalum Electrolytic Caps
CP = Decoupling Caps

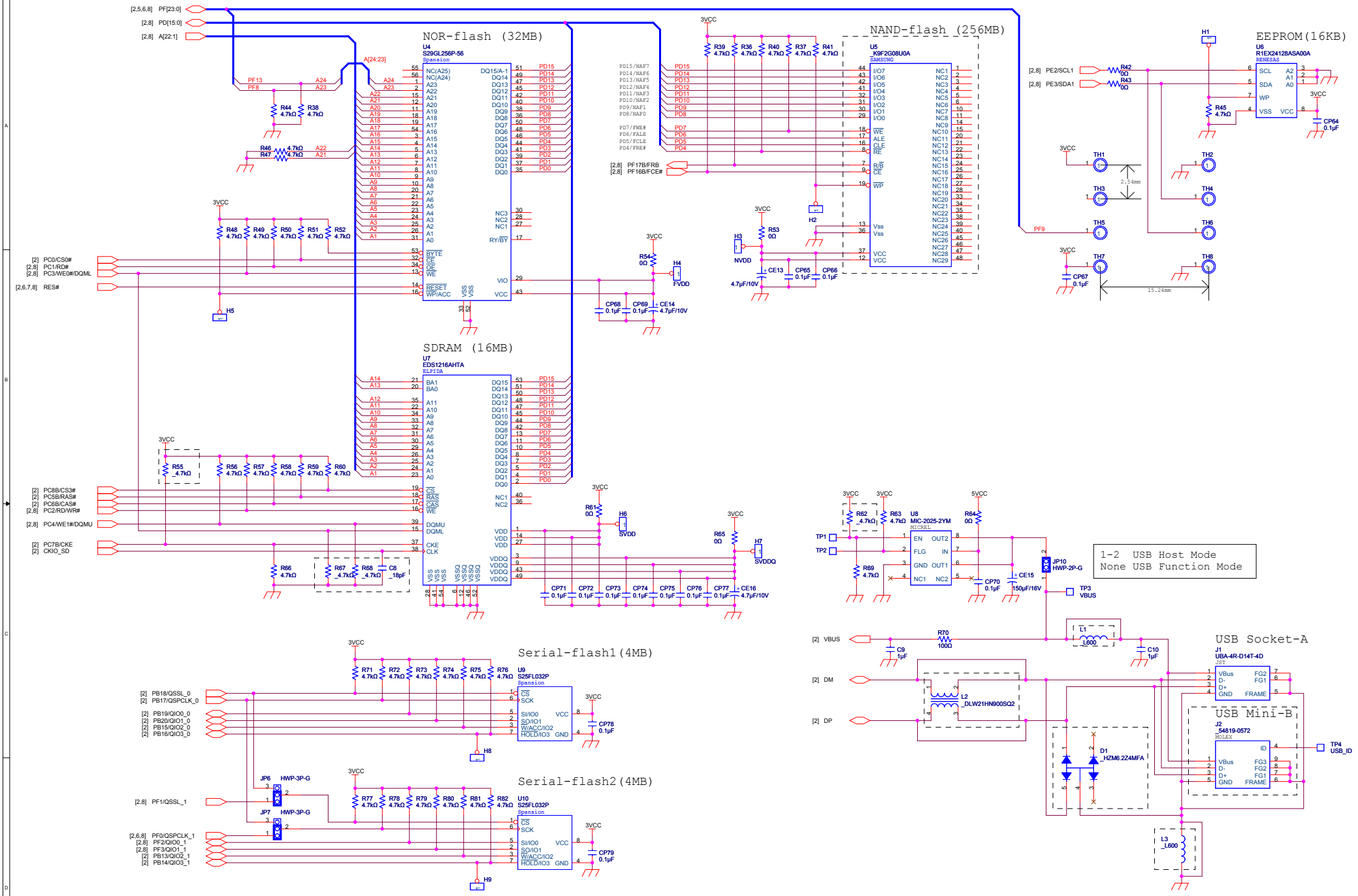
CHANGE		SCALE		Renesas Solutions Corp.				R0K572690C000BR INDEX (1 / 8)
				DRAWN	CHECKED	DESIGNED	APPROVED	
		DATE	11-08-29					D-R0K572690C000BR_C-A



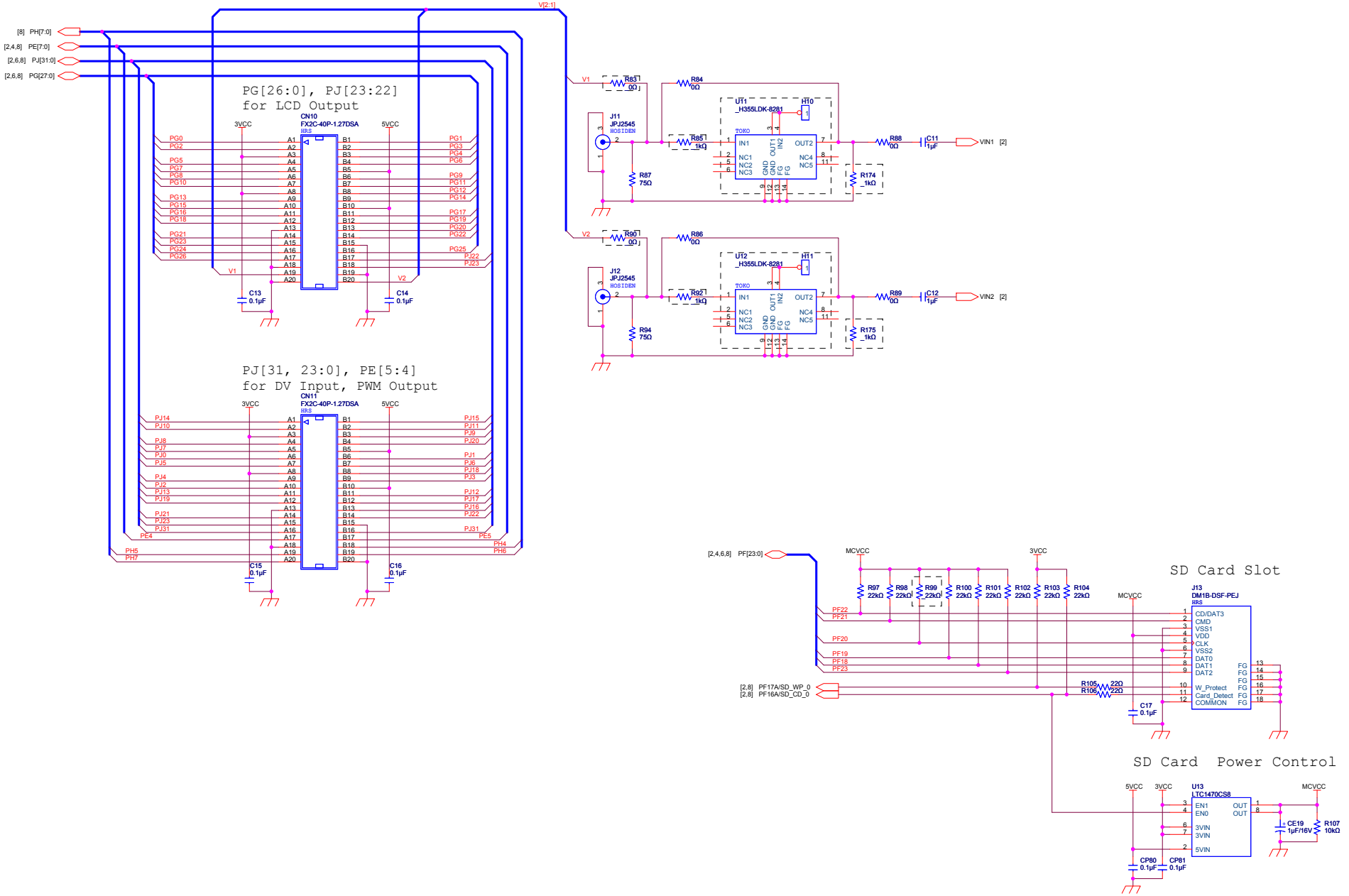
CHANGE			Renesas Solutions Corp.		R0K572690C000BR
			DRAWN / CHECKED / DESIGNED / APPROVED		CPU(SH7269), Clock (2 / 8)
		SCALE			
		DATE	11-08-29		D-R0K572690C000BR_C-A



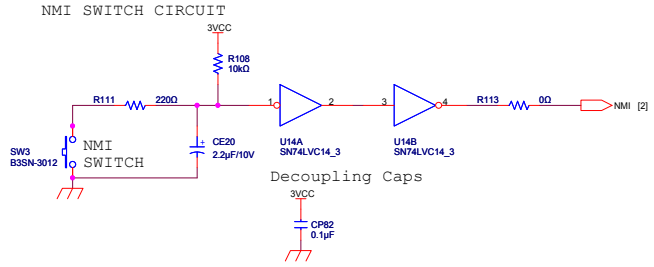
CHANGE						
			Renesas Solutions Corp.			R0K572690C000BR
			DRAWN	CHECKED	DESIGNED	APPROVED
		SCALE				CPU(SH7269)-power (3 / 8)
		DATE	11-08-29			D-R0K572690C000BR_C-A

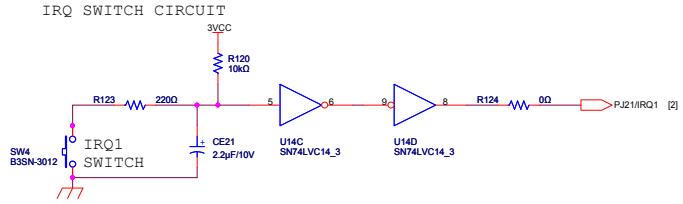


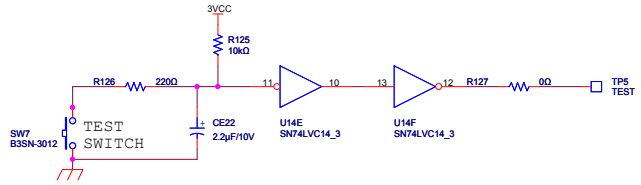
CHANGE			Renesas Solutions Corp.		R0K572690C000BR
			DRAWN / CHECKED / DESIGNED / APPROVED		Memory, USB (4 / 8)
		SCALE			D-R0K572690C000BR_C-A
		DATE	11-08-29		

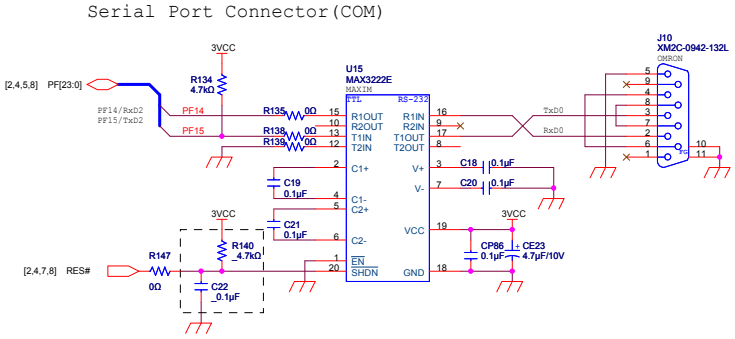


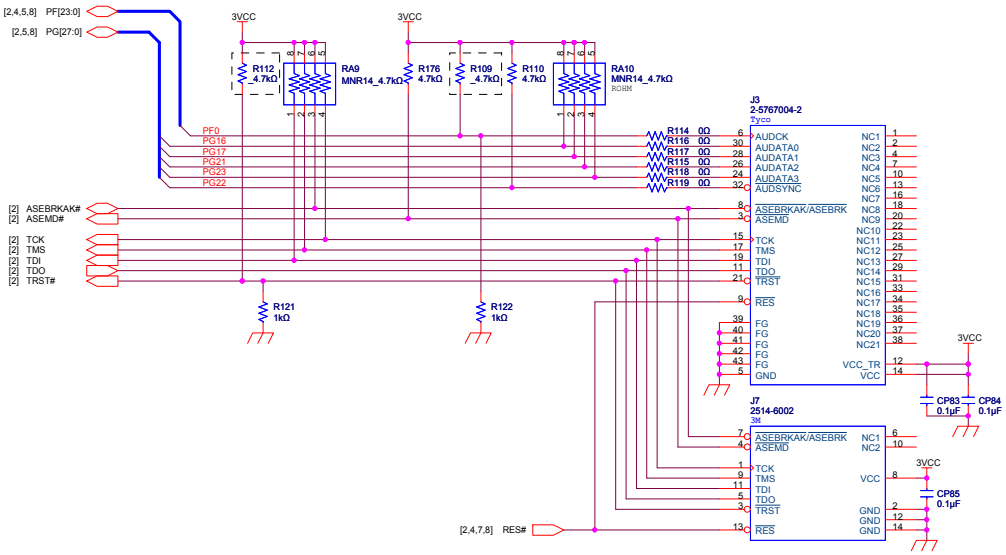
CHANGE			Renesas Solutions Corp.		R0K572690C000BR
			DRAWN	CHECKED / DESIGNED / APPROVED	VDC4, Vin, SD
		SCALE			(5 / 8)
		DATE	11-08-29		D-R0K572690C000BR_C-A

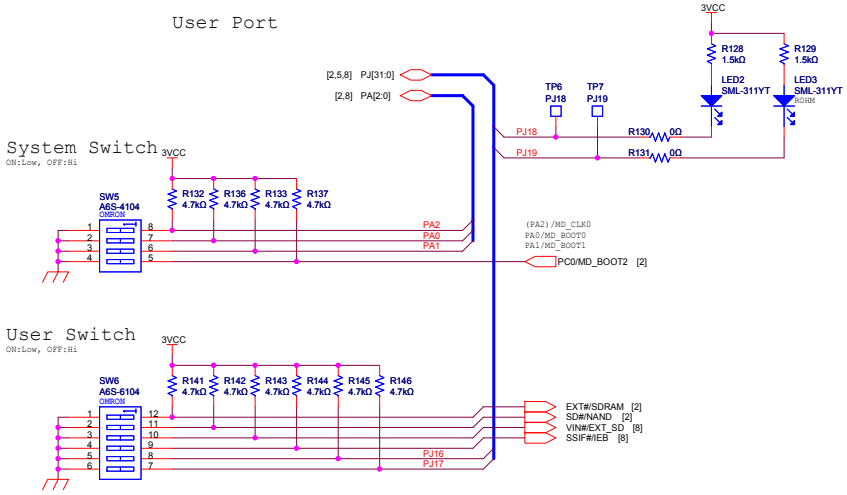




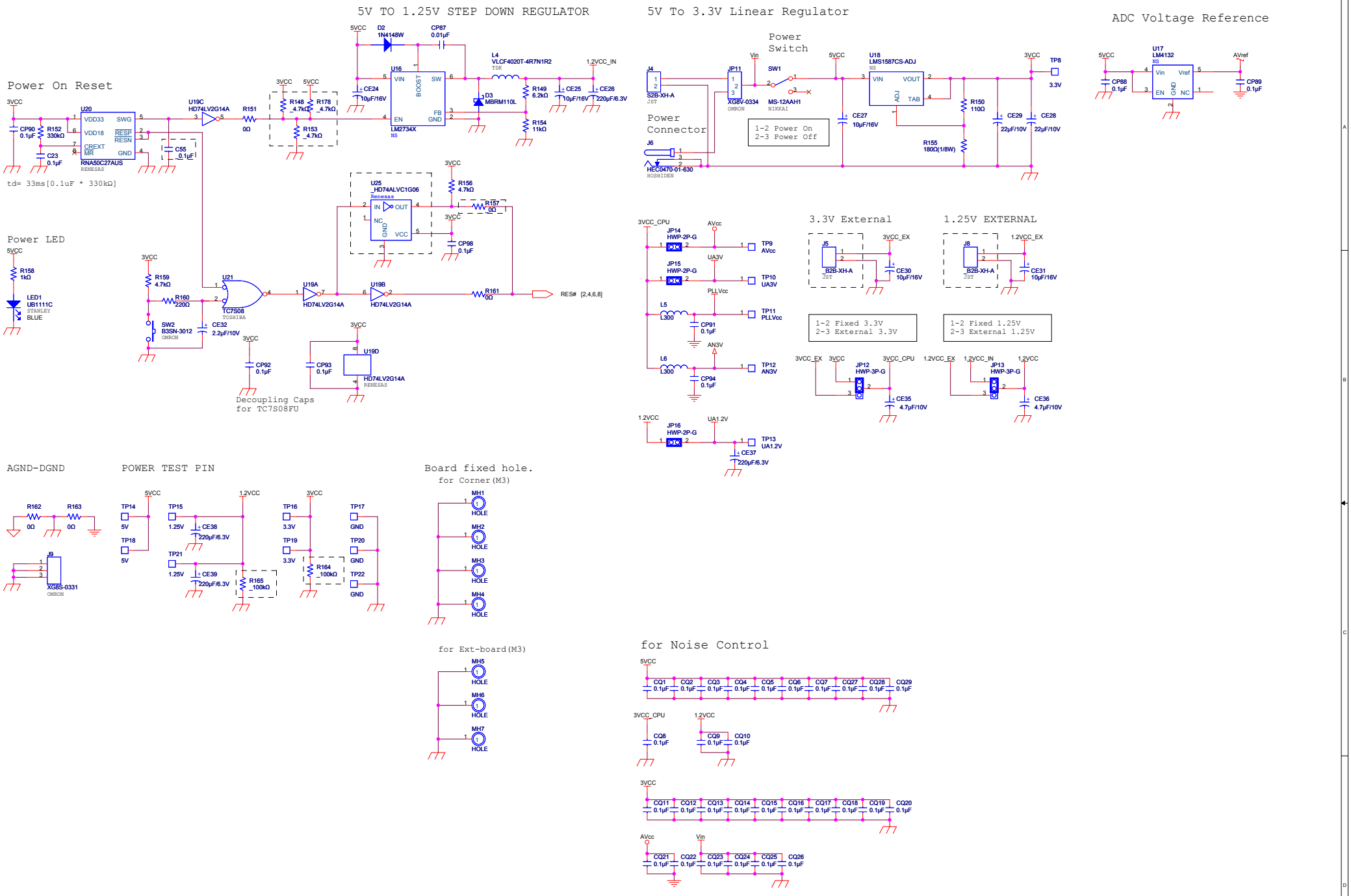




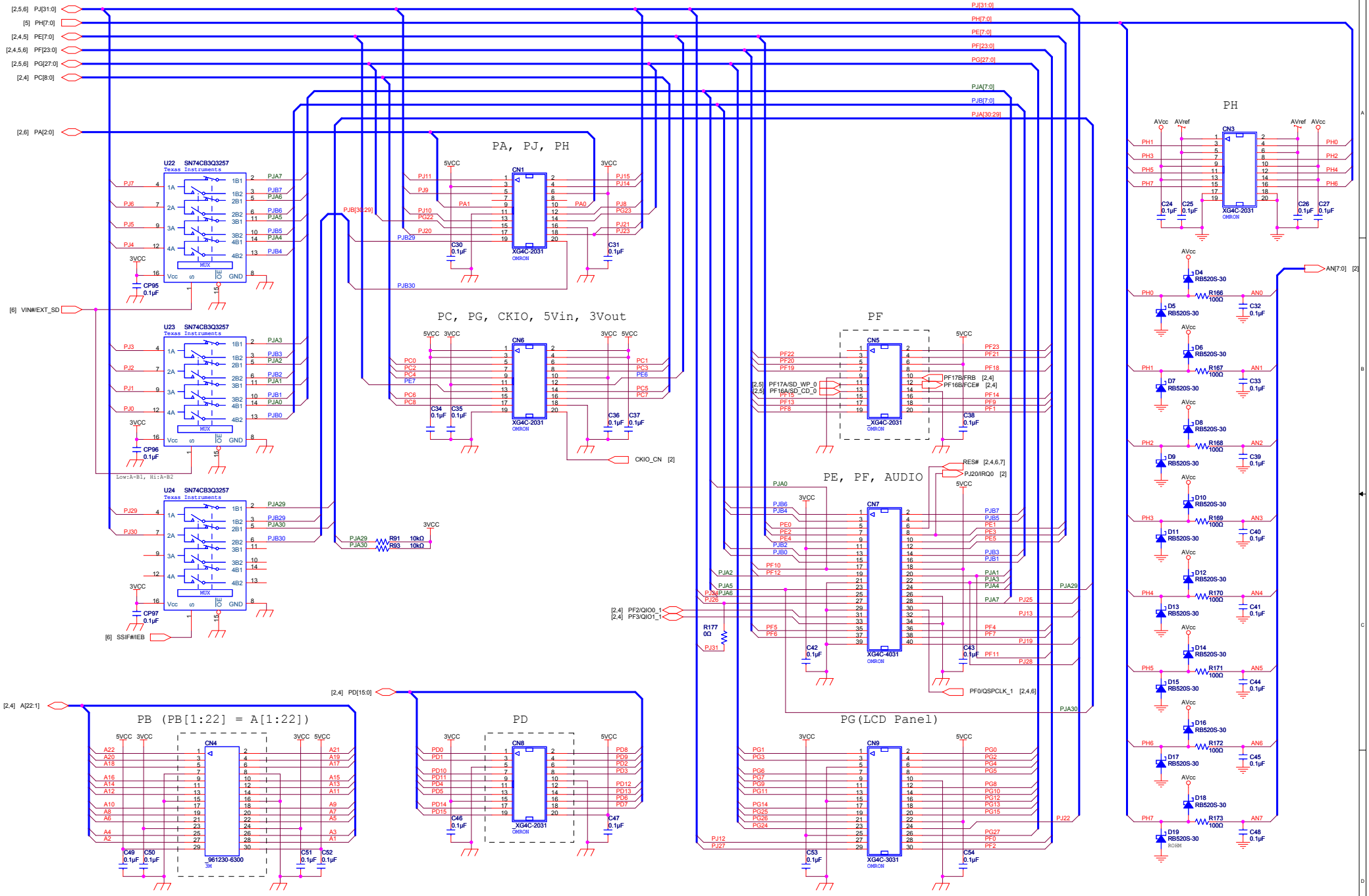




CHANGE			Renesas Solutions Corp.			R0K572690C000BR
			DRAWN	CHECKED	DESIGNED	APPROVED
		SCALE				Switch, RS-232C, H-UDI, UserI/F (6 / 8)
		DATE	11-08-29			D-R0K572690C000BR_C-A



CHANGE			Renesas Solutions Corp.		R0K572690C000BR
			DRAWN / CHECKED / DESIGNED / APPROVED		Reset, Power (7 / 8)
	SCALE				
	DATE	11-08-29			D-R0K572690C000BR_C-A



CHANGE		SCALE		Renesas Solutions Corp.				R0K572690C000BR
		DATE	11-08-29	DRAWN	CHECKED	DESIGNED	APPROVED	Ext. Connector, AD Protection (8 / 8)
								D-R0K572690C000BR_C-A

SH7269 VDC4 board R0K572690B000BR SCHEMATICS

Note:

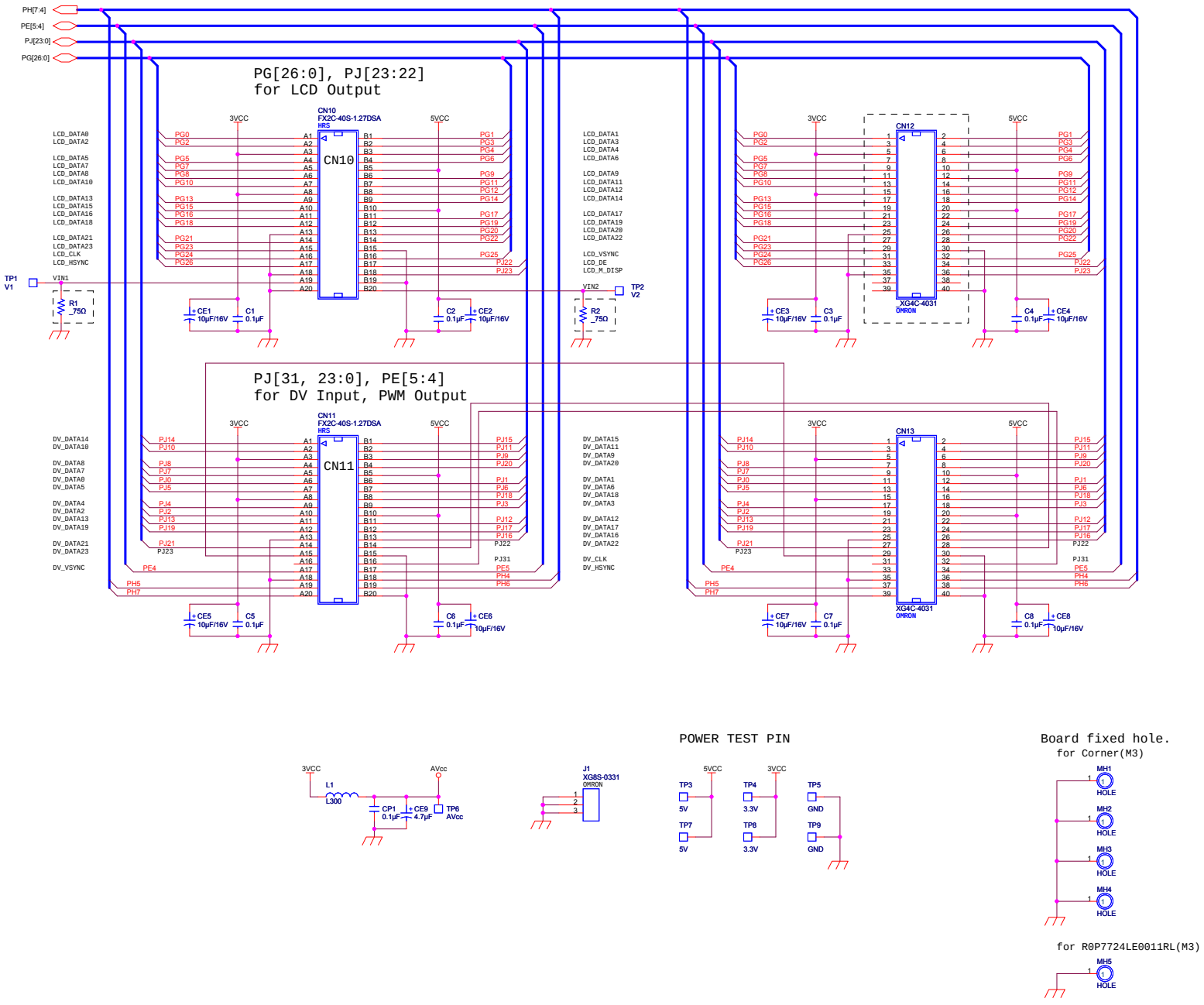
Digital GND (GND)

Not mounted

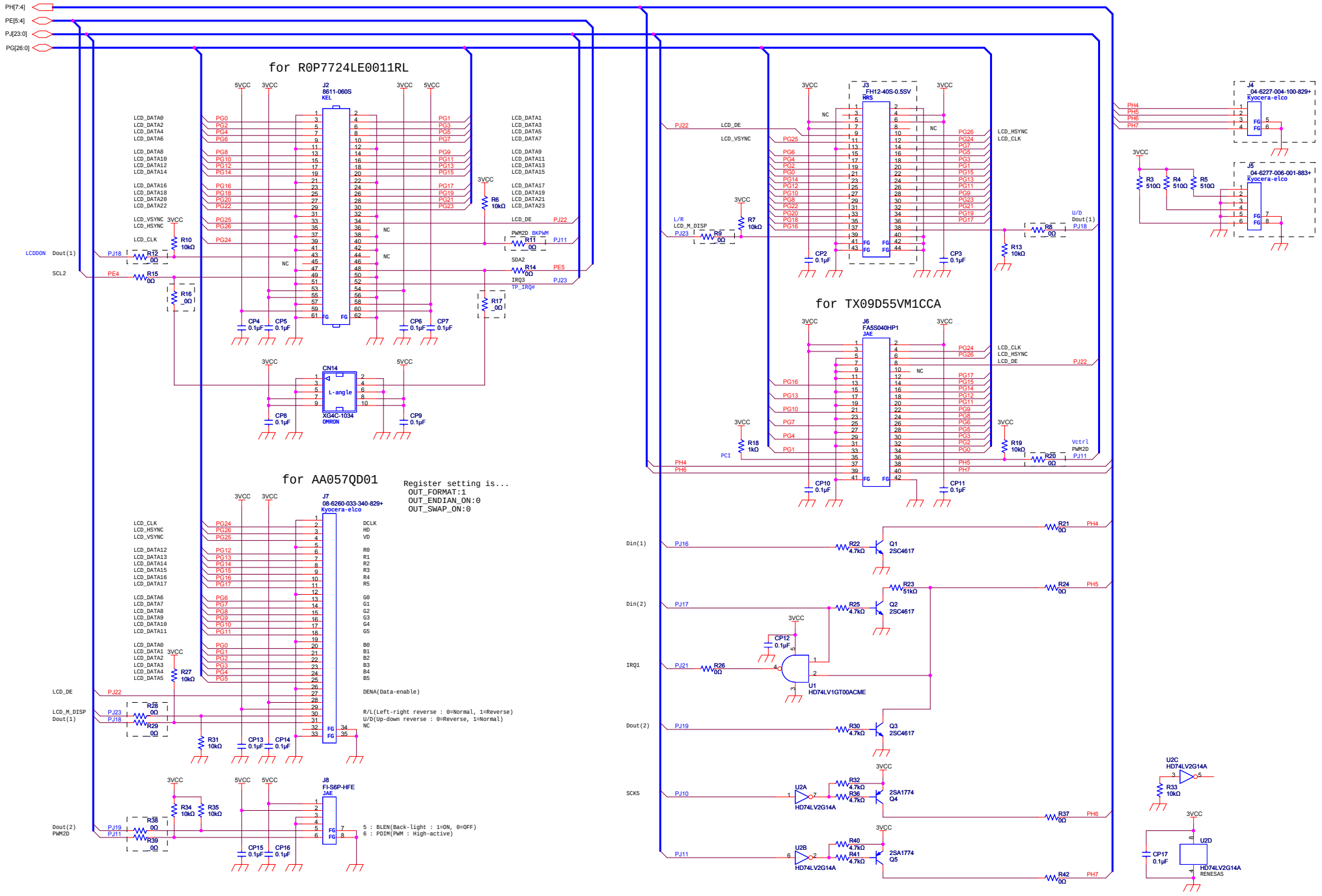
5VCC = Digital 5V
3VCC = Digital 3.3V
AVcc = Analog 3.3V

R = Fixed Resistors
C = Ceramic Caps
CE = Tantalum Electrolytic Caps
CP = Decoupling Caps

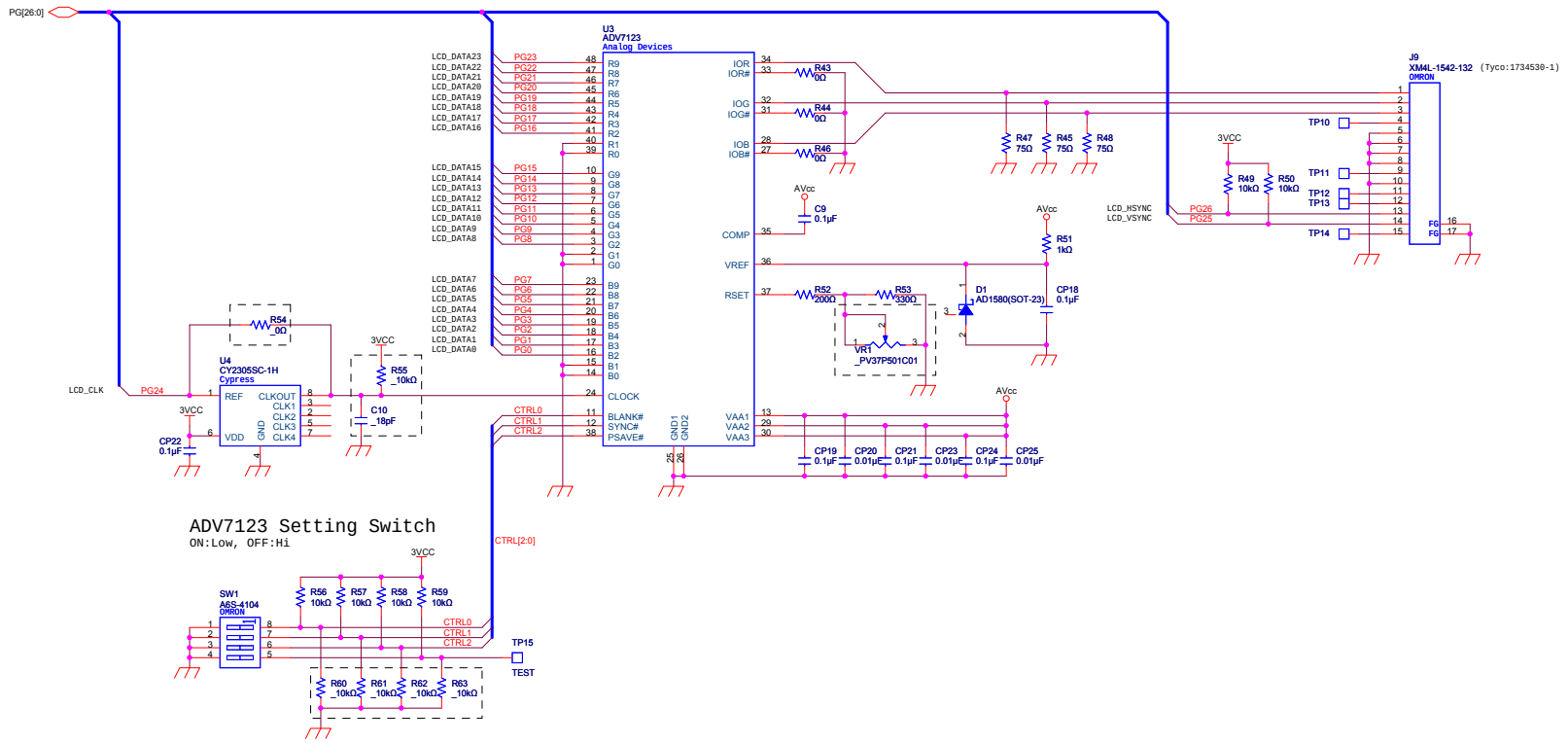
CHANGE		SCALE		Renesas Solutions Corp.				R0K572690B000BR INDEX (1 / 4)
		DATE	12-06-29	DRAWN	CHECKED	DESIGNED	APPROVED	D-R0K572690B000BR_C-C



CHANGE		SCALE		Renesas Solutions Corp.				R0K572690B000BR
		DATE	12-06-29	DRAWN	CHECKED	DESIGNED	APPROVED	Ext. Connector (2 / 4)
								D-R0K572690B000BR_C-C



CHANGE		SCALE		Renesas Solutions Corp.				R0K572690B000BR
		DATE	12-06-29	DRAWN	CHECKED	DESIGNED	APPROVED	LCD Module I/F (3 / 4)
								D-R0K572690B000BR_C-C



CHANGE			Renesas Solutions Corp.		R0K572690B000BR
			DRAWN / CHECKED / DESIGNED / APPROVED		Video Encoder (4 / 4)
		SCALE			D-R0K572690B000BR_C-C
		DATE	12-06-29		

Revision History	SH7269 VDC4 Board R0K572690B000BR User's Manual

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 8, 2011	—	First edition issued
1.10	Mar. 8, 2012	—	J3 to J5: changed to "not installed" due to specification revision. Corrected errors in description.
1.20	Sep. 28, 2012	— P1-3 P3-8 Appendix	Backlight power supply for LCD panel AA057QD01 by Mitsubishi Electric: changed from 3.3V to 5V. ・Figure 1.4.1: replaced the image. ・Table 3.1.6: changed the signal names of pin no. 1 and 2 from 3.3V to 5V. ・Changed the connection diagram of R0K572690B000BR.

SH7269 VDC4 Board R0K572690B000BR User's Manual

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Colophon 1.3

SH7269 VDC4 Board
R0K572690B000BR
User's Manual

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