SLG47011V Evaluation Board

This document describes the SLG47011V Evaluation Board functionality and provides a quick start guide.

1. Contents

Figures

2. Terms and Definitions

GPIO	General Purpose Input/Output
IC	Integrated Circuit
LDO	Low dropout linear regulator
VREF	Voltage reference
TP	Test point

3. References

[1] SLG47011, Datasheet, Renesas Electronics.

4. Introduction

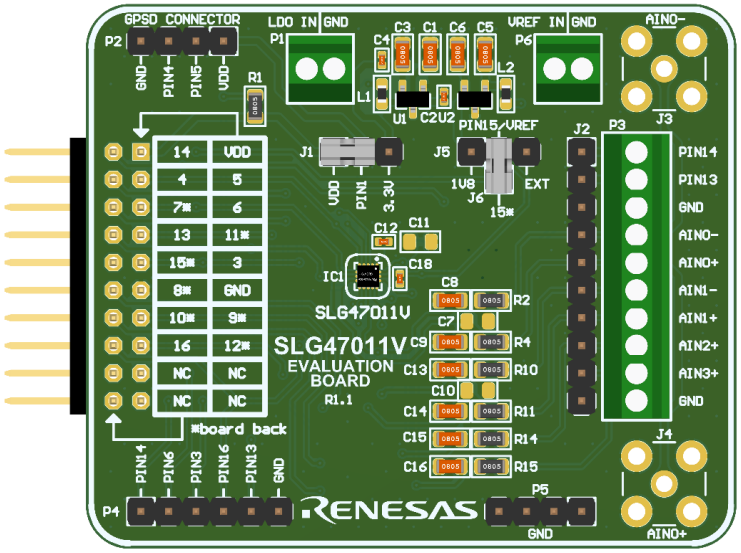


Figure 1. SLG47011V Evaluation Board (Top View)

The goal of the Evaluation board is to show the superior performance of SLG47011V as a small, low-power component used in analog-to-digital conversion and mixed-signal functions.

The evaluation board is a compact, easy-to-use hardware tool that provides SLG47011V IC hardware support for design emulation, programming and real-time testing. The evaluation board is controlled by Go Configure Hub software with emulation and IC programming.

5. Board Overview

Except SLG47011V IC Evaluation board has:

- connector for emulating/programming the SLG47011V chip with the Advanced Development Board (ADB), Light Development Board (LDB) SV1 and GREENPAK Serial Debugger (GPSD) P2.
- analog inputs terminal block P3 duplicated with J2 pin header.
- analog filters for the analog inputs.
- ability to mount SMA connectors (J3 and J4) for precision measurements.
- connector for other (digital) GPIOs.
- onboard 3.3V LDO (selectable by jumper).
- onboard 1.8V voltage reference (selectable by jumper)
- ground connector.

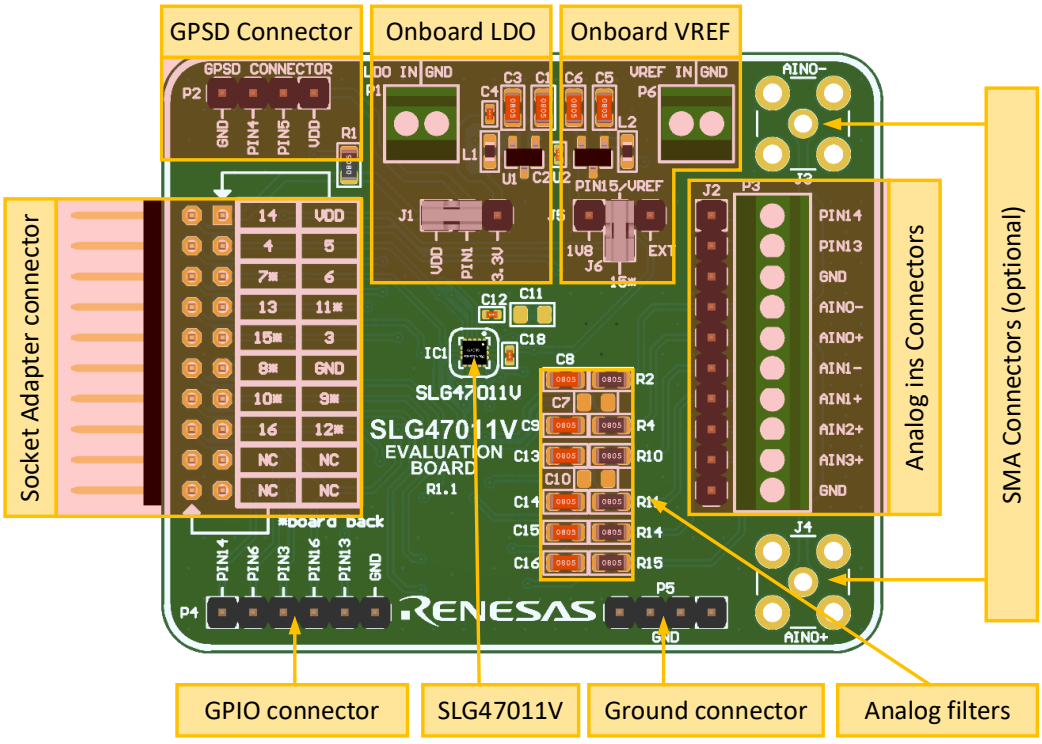


Figure 2. External Connectors and User Control

5.1 Design Emulation, Programming and Real-Time Testing

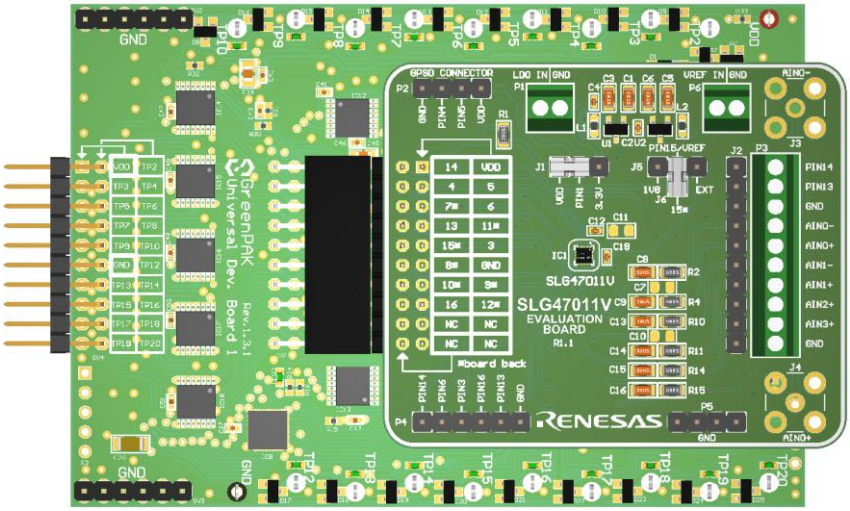


Figure 3. Using ADB for Evaluation.

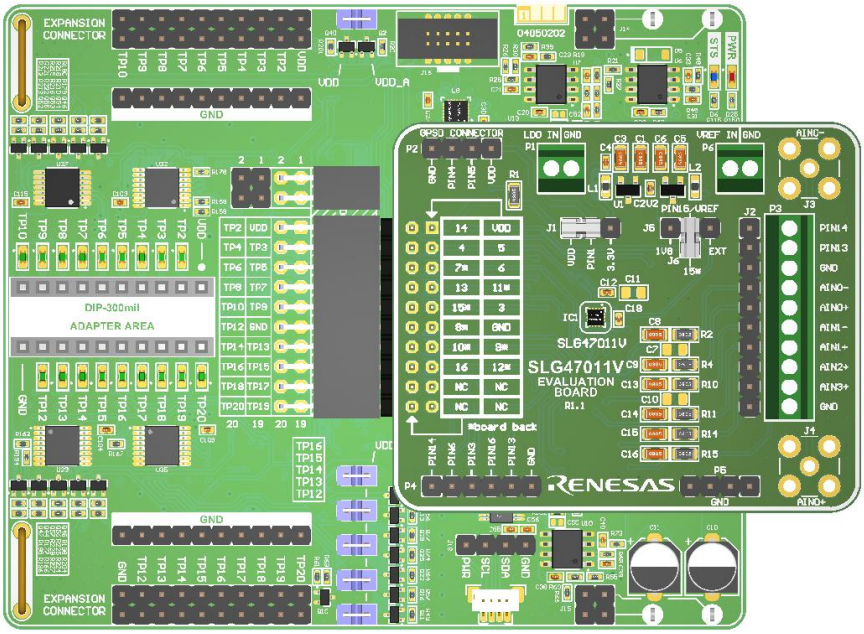


Figure 4. Using LDB for Evaluation.

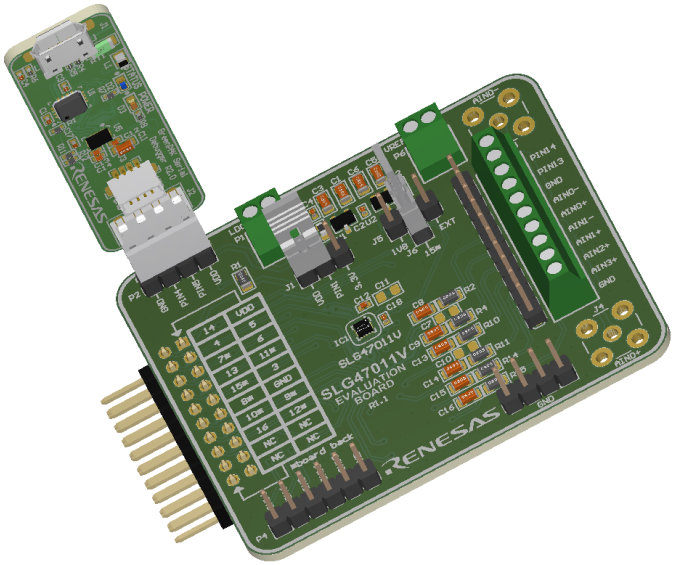


Figure 5. Using GPSD for Evaluation.

Attention! During SLG47011V IC programming 7.5V will be present on VPP (SV1-TP2, SLG47011V IC - PIN14).

5.2 Analog Inputs

P3 and J2 have same pinouts.

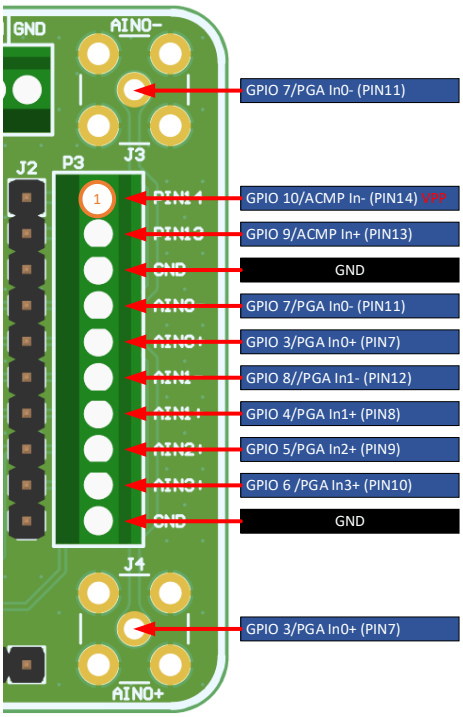


Figure 6. Analog Inputs Connectors

Board can use up to four single-ended analog inputs (AIN0..3) or two differential (AIN0(1)+/-) and two single ended analog inputs (AIN2(3)).

To use full differential filters on analog inputs AIN0 and AIN1 in the differential mode it is needed to mount C7 and C10 capacitors (1nF 0805) respectively.

For precise measurements AIN1+/- could be mounted J3 and J4 SMA connectors (Adam Tech RF2-04A-T-00-50-G for instance).

For more information, please refer to **Table 1** and **Figure 7**.

Table 1 P3/J2 pinout description

P3/J2 Contact number	P3/J2 Contact name	Assignation	Pin Functions
1	PIN14	GPIO10[1]	GPIO, ACMP In-, EXT OSC0, PGA Out-, VPP
2	PIN13	GPIO9[1]	GPIO, ACMP In+, PGA Out+
3	GND	--	--
4	PIN11	GPIO7[2,4]	GPIO, PGA In0-, CS out, ACMP In+, SLA 2
5	PIN7	GPIO3[2,3,4]	GPIO, PGA In0+, EXT OSC1
6	PIN12	GPIO8[2,4]	GPIO, PGA In1-, DAC out, SLA 3
7	PIN8	GPIO4[2,3,4]	GPIO, PGA In1+
8	PIN9	GPIO5[2,3]	GPIO, PGA In2+
9	PIN10	GPIO6[2,3]	GPIO, PGA In3+, SLA 1
10	GND	--	--

Note 1 – direct connect.
Note 2 – Connected through RC filter.
Note 3 – Used in single-ended mode.
Note 4 – Used in differential mode.

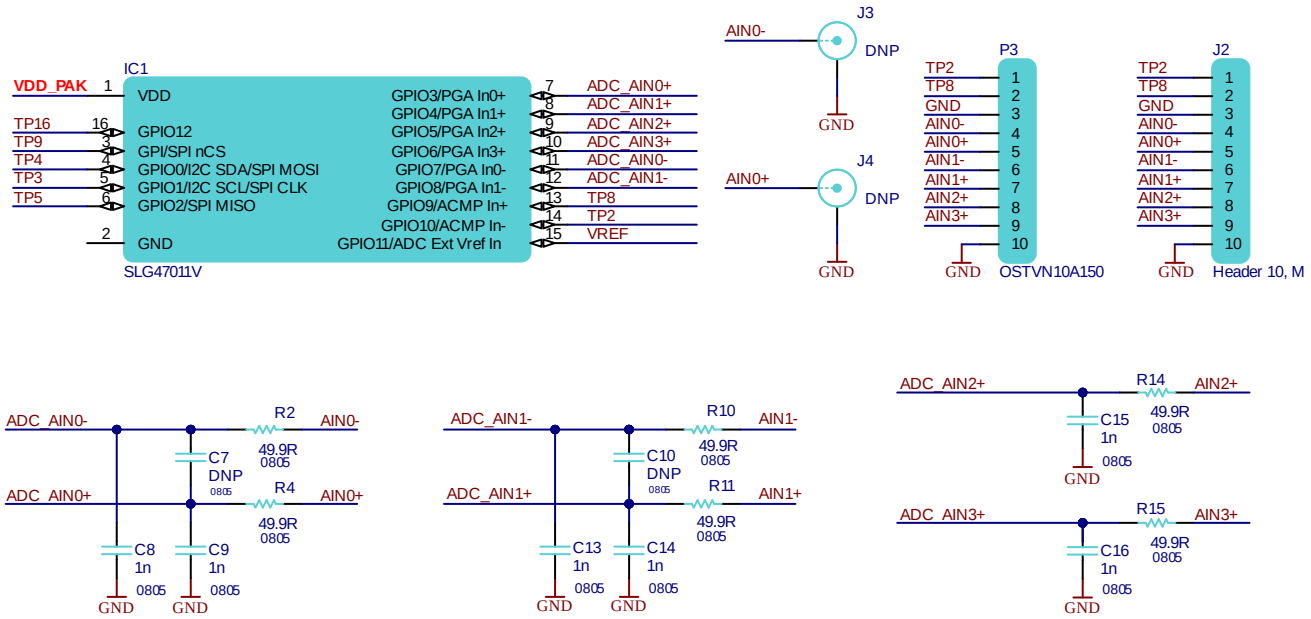


Figure 7. Analog Inputs Schematic

In the default state PGA inputs on board, listed in **Table 1**, are disconnected from socket adapter connector SV1. If it is needed to use them connected to TPs of SV1, should be mounted respective resistors jumpers on the board bottom (see **Figure 8**).

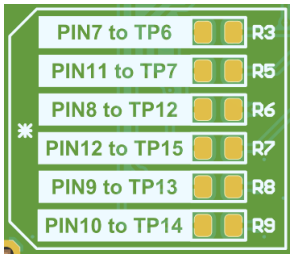


Figure 8. Jumper's Assignment to TPs of Socket Adapter Connector SV1

5.3 Onboard LDO

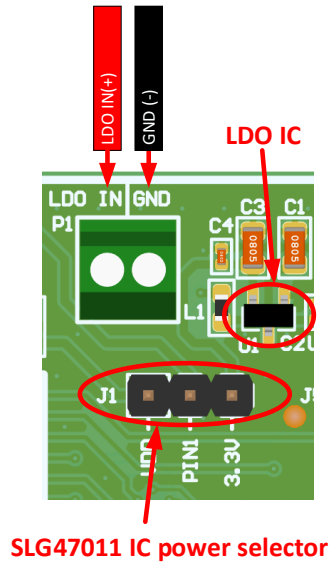


Figure 9. SLG47011V IC Power Selector View

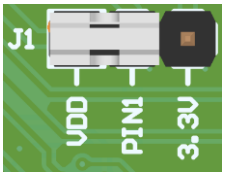
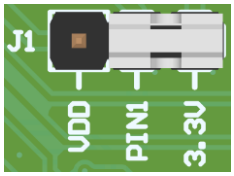
	
Powered from V_{DD} (TP1 of socket adapter connector SV1). In the case of using onboard VREF, V_{DD} should meet the input operating voltage range (**Table 3**). Default jumper's position.	Powered from LDO

Figure 10. SLG47011V IC Power Selector Usage

Table 2 Onboard LDO DC characteristics

Parameters	Min.	Typ.	Max	Units
Input Operating Voltage	3.7	--	6.0	V
Maximum Output Current -	200	--	--	mA
VOUT Temperature Coefficient	--	50	--	ppm/°C

5.4 Onboard VREF

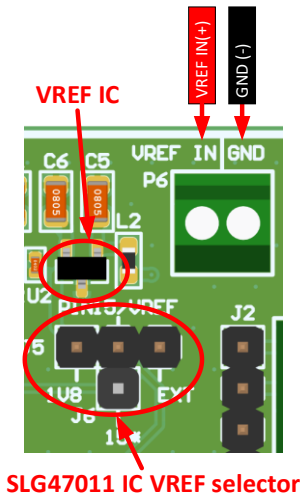


Figure 11. VREF Selector View

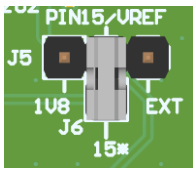
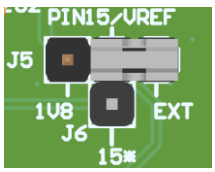
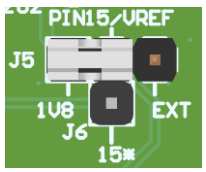
		
Connected to TP10 of socket adapter connector SV1. Default jumper's position.	External VREF from P6 terminal block	Onboard 1.8V VREF
In case of usage PIN15 as GPIO, please keep in mind C17, C18 capacitors on VREF net (see Chapter 7)	Input voltage range: 1,62 – 2V	See **Table 3**

Figure 12. VREF Selector Usage

Table 3 Onboard VREF DC Characteristics

Parameters	Min.	Typ.	Max	Units
Input Operating Voltage	2	--	5.5	V
Output Current Range	--	--	5	mA
VOUT Temperature Coefficient	--	50	--	ppm/°C

5.5 Zero Current Leakage Configuration

In case of measurements, current consumption SLG47011V IC it is recommended to cut out jumper trace JP1 on the board back to avoid leakages through onboard VREF (see **Figure 13**).

Current consumption measurements could be performed by connecting the amperemeter:

- to pin PIN1 and pin V_{DD} of J1 in case of powering from SV1.
- to pin PIN1 and pin 3.3V of J1 in case of powering from onboard LDO.

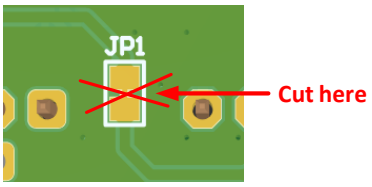


Figure 13. Cut Out Jumper Trace Usage.

5.6 GPIO Connector

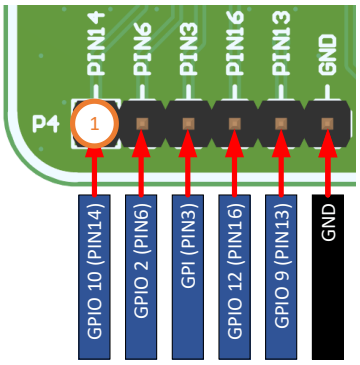


Figure 14. GPIO Connector Pinout

Table 4. P4 Pinout Description

Pin Number	SLG47011V IC pin (GPIO)	SV1
1	PIN14 (GPIO10) VPP	TP2
2	PIN6 (GPIO2)	TP5
3	PIN3 (GPI)	TP9
4	PIN16 (GPIO12)	TP16
5	PIN13 (GPIO9)	TP8
6	GND	TP11

5.7 GPSD Connector

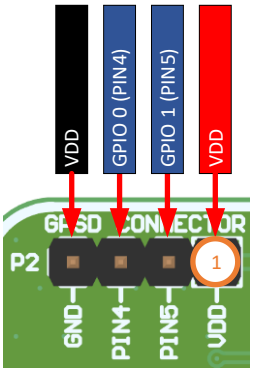


Figure 15. GPSD Connector Pinout

Table 5. GPSD (P2) Pinout Description

Pin Number	SLG47011V IC pin (GPIO)	SV1
1	PIN1 V_{DD}	TP1
2	PIN5 (GPIO1)	TP3 (SCL[1])
3	PIN4 (GPIO0)	TP4 (SDA[1])
4	GND	TP11

Note 1 – If I^2C master SCL, SDA lines do not have pull-ups it is possible to mount resistors R12 and R13 (pull up to V_{DD}) on board back.

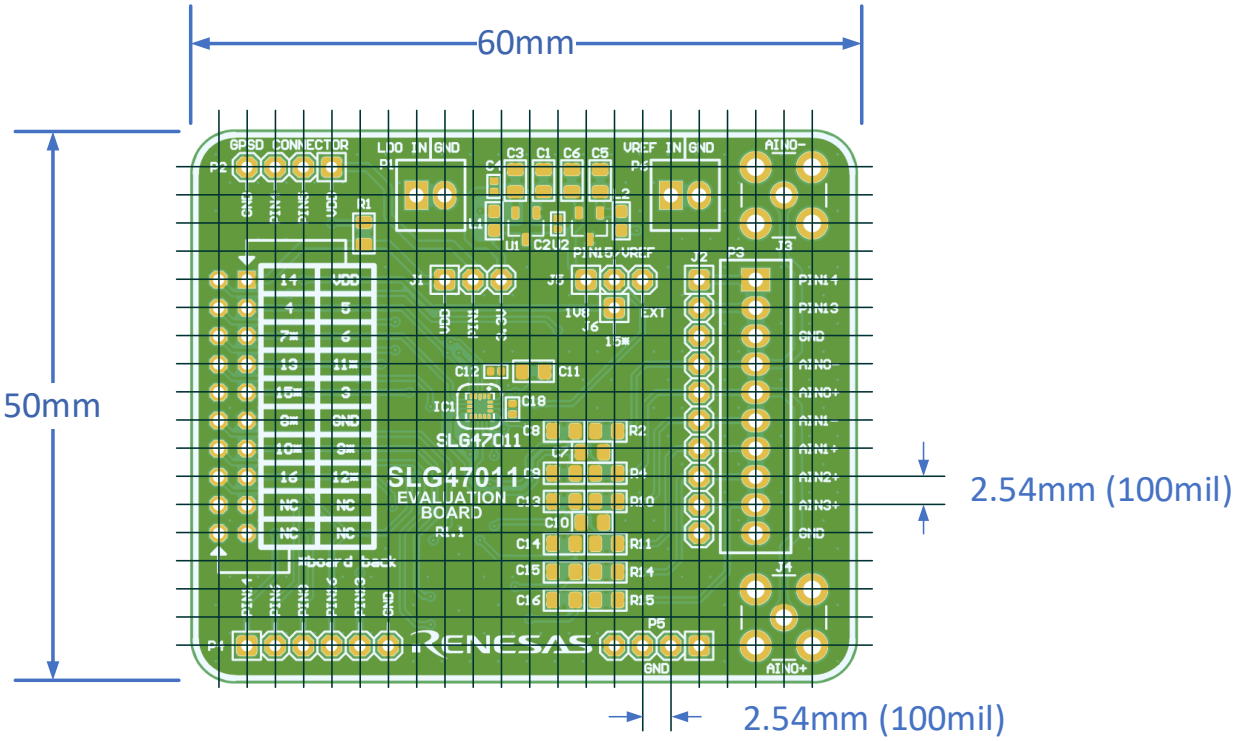
5.8 Ground Connector

Figure 16. GND Connector View

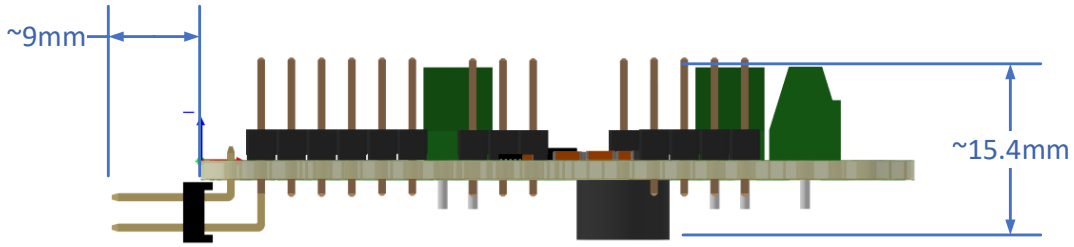
P5 (all pins are GND) is a common usage connector, for instance, simplifying measurements by oscilloscope probes.

6. Board Dimensions

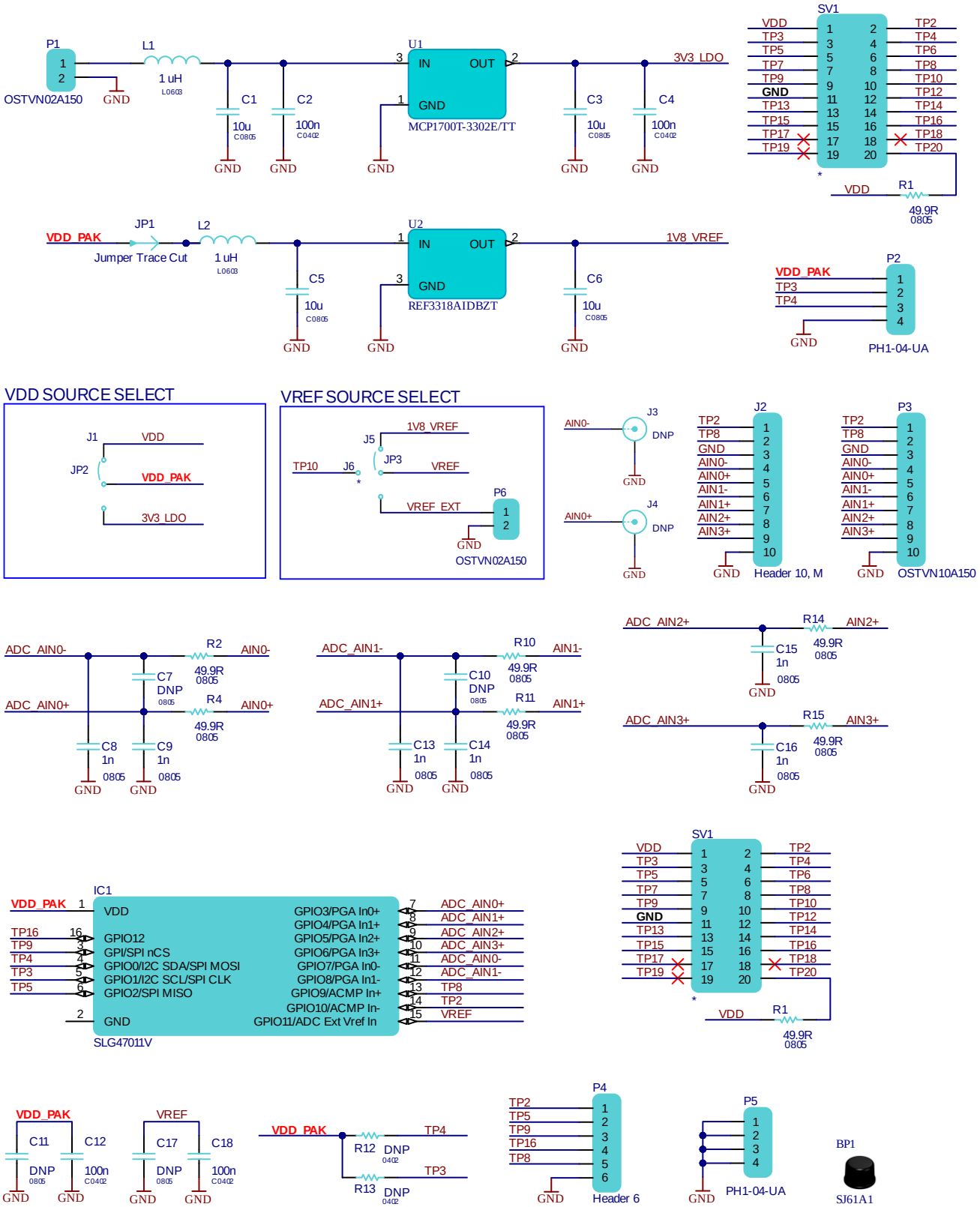
Board Top Dimensions



Board Assembly Side Dimensions



7. Schematic Diagrams



8. Bill of Materials

#	Designator	Manufacturer Part Number 1	Manufacturer 1	Quantity
1	BP1	70006431426	3M	1
2	C1, C3, C5, C6	C0805C106M8RACTU	KEMET	4
3	C2, C4, C12, C18	C0402C104K4RACTU	KEMET	4
4	C7, C10, C11, C17			4
5	C8, C9, C13, C14, C15, C16	08055C102KAT2A	Kyocera AVX	6
6	IC1	SLG47011V	Renesas	1
7	J1, J5	PH1-03-UA	Adam Equipment	2
8	J2	68001-410HLF	Amphenol ICC / FCI	1
9	J3, J4			2
10	J6	PH1-01-UA	Adam Equipment	1
11	JP2, JP3	NPC02SXON-RC	Sullins	2
12	L1, L2	CS160808-1R0K	Bourns	2
13	P1, P6	OSTVN02A150	On-Shore Technology	2
14	P2, P5	PH1-04-UA	Adam Equipment	2
15	P3	OSTVN10A150	On-Shore Technology	1
16	P4	PR20206VBNN	METZ CONNECT	1
17	R1, R2, R4, R10, R11, R14, R15	CRCW080549R9FKEA	Vishay	7
18	R3, R5, R6, R7, R8, R9, R12, R13			8
19	SV1	68021-220HLF	Amphenol ICC / FCI	1
20	U1	MCP1700T-3302E/TT	Microchip	1
21	U2	REF3318AIDBZT	Texas Instruments	1

9. Ordering Information

Part Number	Description
SLG47011V-EVB	SLG47011V Evaluation Board

10. Revision History

Revision	Date	Description
1.01	Oct 24, 2023	Added Ordering Information
1.00	Sep 22, 2023	Initial release.