SLG47011V HART Modem Demo Board

Introduction

The SLG47011V HART Modem is a demonstration board that showcases the implementation of the industrial HART protocol on a mixed-signal IC from Renesas. This manual is intended for end users of the SLG47011V HART Modem Demo Board. It describes the functionality, main interfaces, and features of the demo board, and provides a clear, step-by-step guide for getting started.

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Terms and Definitions

CD	Counter Data
DUT	Device Under Test
FD	Field Device
FSK	Frequency Shift Keying
GPIO	General Purpose Input/Output
HART	Highway Addressable Remote Transducer
HD	Host Device
IC	Integrated Circuit
MF	Multi-Functional
OCD	Output Carrier Detect
PC	Personal Computer
PCB	Printed Circuit Board
RTS	Request-to-Send
TP	Test Point

References

[1] SLG7RN47762_DS_r011_12112024.docx, Datasheet, Renesas Electronics.
[2] SLG7RN47762_GP_r002U_12092024.aap, GreenPAK Design File, Renesas Electronics

1. Basic Description

1.1 Board Overview

The SLG47011V HART Modem is a demonstration board that shows the implementation of the industrial HART protocol on a mixed signal IC from Renesas. An overall board view with all main functional blocks highlighted is shown in Figure 1.

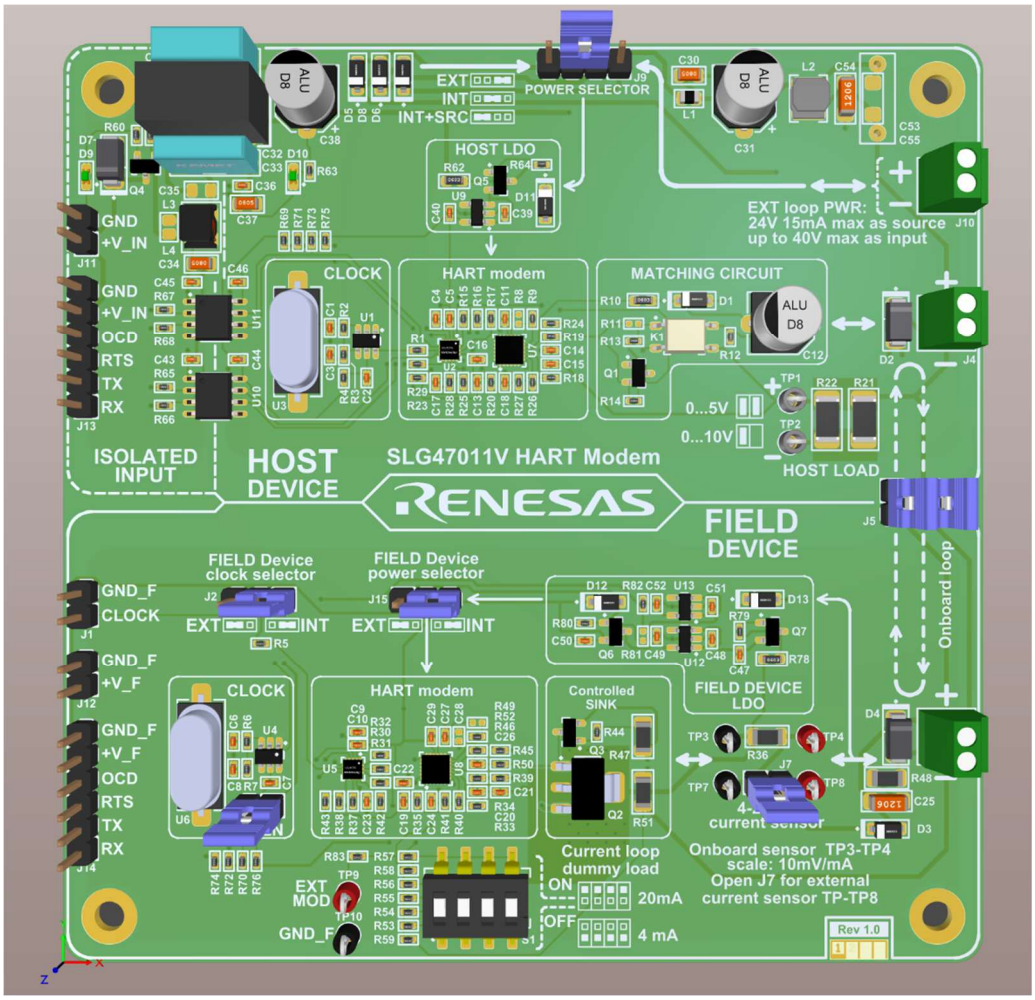


Figure 1. SLG47011V HART Modem Board Top View

The industry-standard 4-20 mA current loop is used as the physical layer for HART modulation. The demo board contains both essential components, a Host Device and a Field Device**,** which simulate the operation of a master (controller) and a remote (sensor) device, respectively.
For both parts, SLG47011V ICs are used as the modulator/demodulator front-end between the user interface (UART) and the HART interface (FSK modulation).

Board main features:

- Flexible power supply scheme – the user can test both the Host and Remote Sensor parts using onboard power supply sources or by attaching an external supply.
- Current loop load – selectable 4 mA to 20 mA current load (configurable via DIP switch).
- Onboard or external current loop path selection – the user can easily test the design with any type of external data line.

1.2 HART Protocol

The demo board provides the capability to test and evaluate the HART protocol, compatible with HART standards. The Renesas SLG47011V IC acts as a transceiver between user data (UART) and the HART interface. In addition to direct modulation and demodulation modules, the internal design also includes the management of RTS (transmit start, input) and OCD (carrier detect, output) signals. Modulated data is transmitted via a 4-20 mA current loop, through either onboard or external lines.

2. Detailed Board Description

2.1 Functional Block Diagram

The HART Modem Demo Board is designed as a single PCB and divided into two independent logic blocks. Figure 2 shows a simplified block diagram of the demo board. Since the 4-20 mA current loop interface is used as the physical layer for data transfer, the highlighted blocks in the block diagram are designed to emulate the operation of a Host Device and a Field Device (remote sensor).

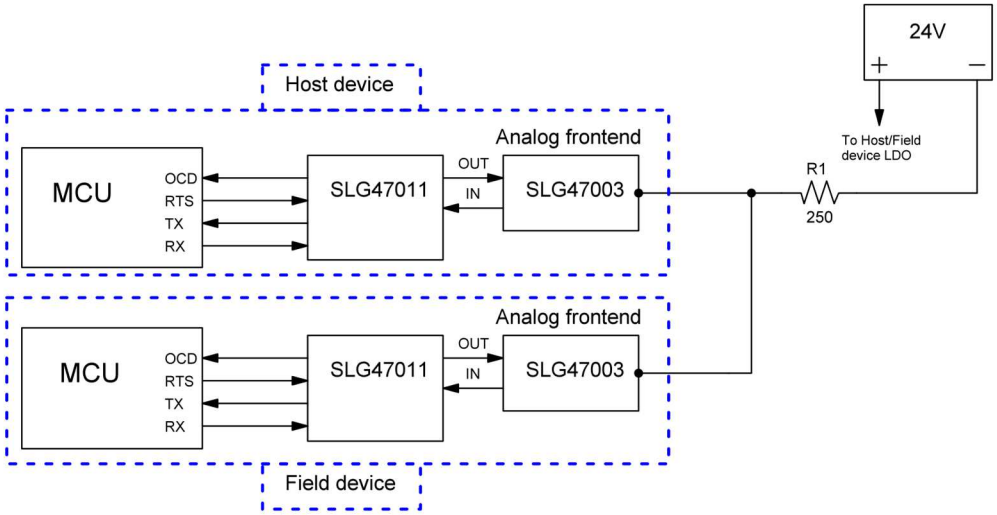


Figure 2. SLG47011V HART Modem Functional Block Diagram

Each part has a different electrical schematic, but both provide the end user with the same digital interface for communication. The power supply schemes also differ between the parts.

2.2 Power Supply

2.2.1. Host Device

In addition to data communication, the Host Device part of the Demo Board is also designed to serve as a power input when the onboard source for the 4-20 mA current loop is selected.

By adjusting the position of the “Power Selector” jumper, the user can choose one of the following options:

1) **EXT** – External power supply is used as the power source for the 4-20 mA current loop and the Host-side transceiver circuit. The acceptable range is 14 V to 34 V.
2) **INT** – The onboard DC/DC converter is used to power the Host-side transceiver circuit. The supply voltage for the 4-20 mA current loop is a nominal 24 V.
3) **INT + SRC** – This duplicates the previous option, providing a nominal 24 V with a maximum current of 10 mA.

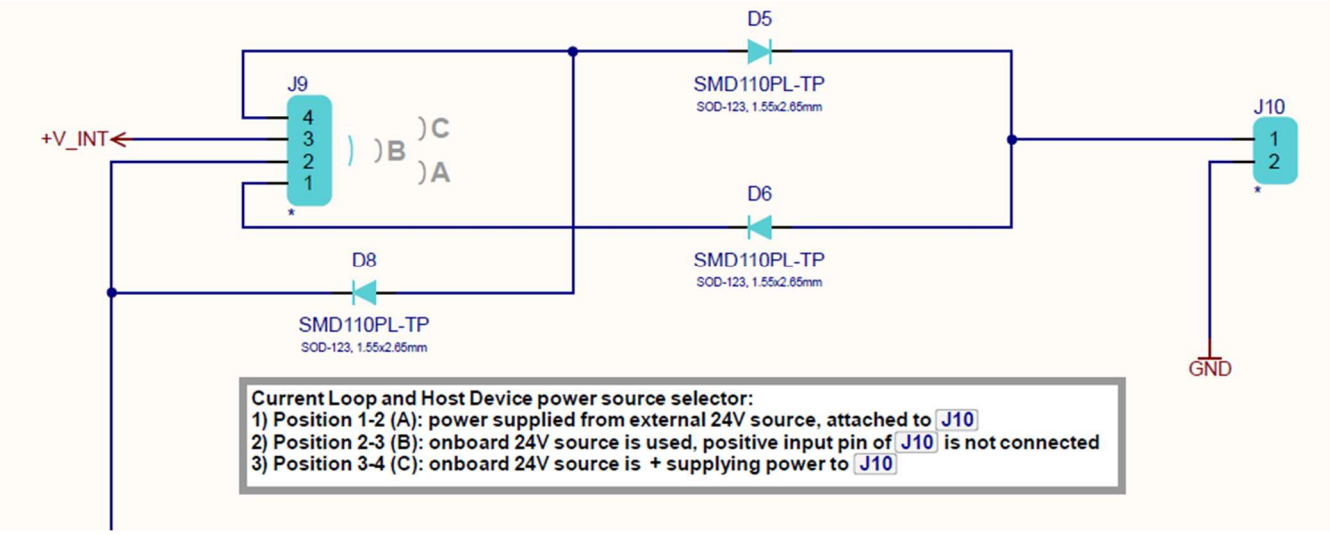


Figure 3. Host Power Selector

Notes:

- For power supply options (1) and (3), reverse polarity protection is provided.
- When using option (3), the user should ensure that the externally connected current DOES NOT exceed the maximum allowable limit.

2.2.2. Host Device Isolation

An important feature implemented in the demo board is galvanic isolation for the Host (controller) interface. Isolation is provided by U10-11 (UART interface) and A1 (Power input).

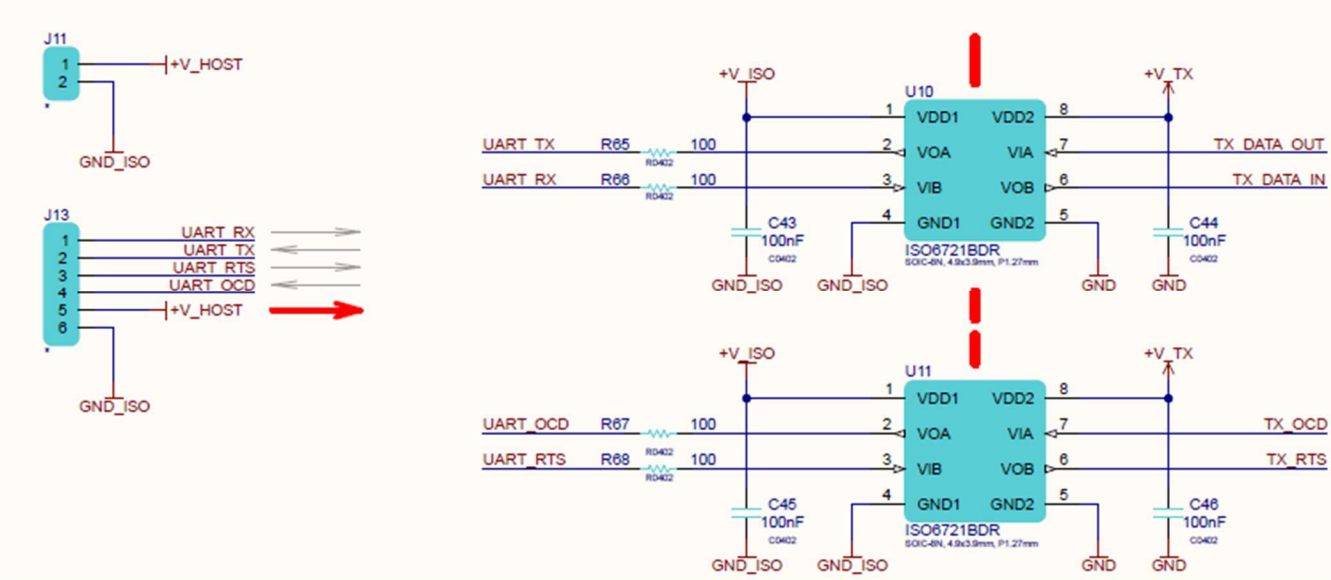


Figure 4. UART Isolation

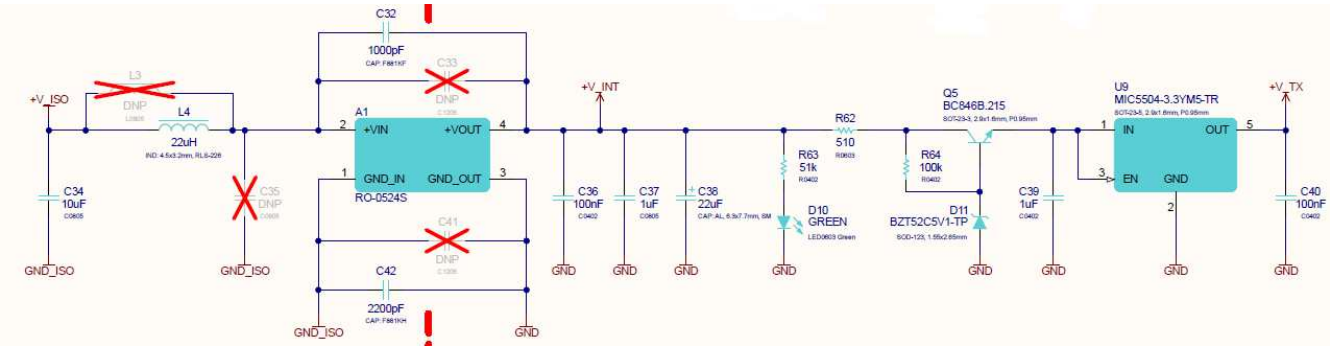


Figure 5. Power Isolation

Input part GND and loop GND are galvanically isolated.

2.2.3. Field Device

The Remote Sensor is designed to be used with one of two possible power sources: loop-powered device or externally powered. Selection between power sources is made using the “Field Device power selector” headers (see Figure 6).

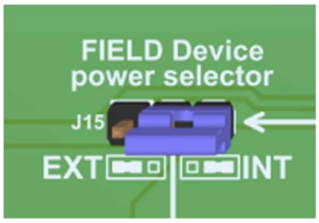


Figure 6. Field Device Power Selector

1. When the jumper is in the “INT” position, all circuits related to the Field Device are powered by the 4-20 mA current loop through the onboard LDO. This setup represents the industry-standard solution when the remote sensor does not require an additional power source, and the connection is made using only two wires. Additionally, the internal 3.3 V power supply is available on VDD_F and GND_F pins, and the user can use it to power a custom circuit (custom Remote Sensor).
2. When the jumper is in the “EXT” position, power to the Field Device circuits is supplied from the VDD_F and GND_F pins. The user must provide a power supply equal to 3.3 V.

Because the current consumption of the low-power device may be significantly affected by the clock value, and to provide additional flexibility in testing, the demo board allows the user to select between two clock sources for the target SLG47011V IC: an onboard crystal resonator with a crystal driver, or a connector for external clock connection.

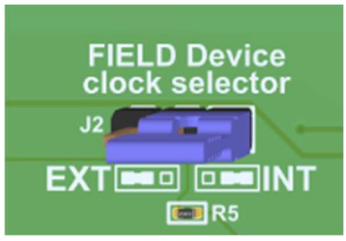


Figure 7. Clock Selector

2.3 UART to HART Interface

A standard UART interface is used for data communication. The main electrical parameters and AC timings are listed in Table 1.

Table 1. UART Interface Specification, AC Characteristics

	Min	Typical	Max
Baud Rate	-1%	1200 b/s	+1%
RTS to Carrier Start	--	--	5-bits
RTS to Carrier Stop	--	--	5-bits
Carrier Frequency Deviation	-1%	1200 Hz	+1%
	-1%	2200 Hz	+1%

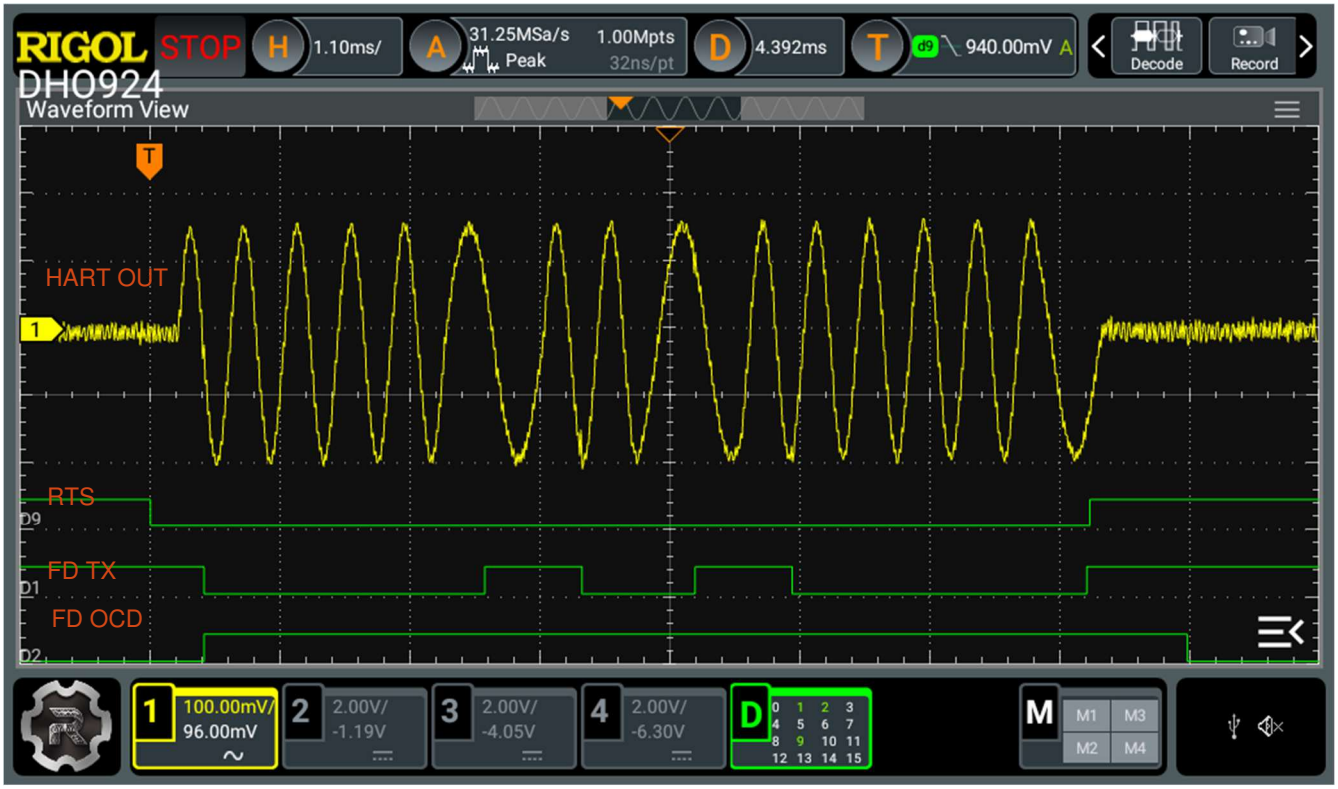


Figure 8. UART to HART Interface with Flow Control Signals

In addition to RX and TX, RTS and OCD signals are also used as part of the flow control functionality.

RTS is a digital input (active low), marking the start and end points during data transmission.

OCD is a digital output (active low), which is set to the active state when the HART carrier (1.2 kHz / 2.2 kHz) is detected.

Both RTS and OCD signals are essential for the proper operation of the SLG47011V transceiver. The user should ensure proper control of these signals when creating custom software.

Note: The internal design structure of the SLG47011V contains only the modules required for proper modulation of digital input and demodulation into digital output signals, along with the corresponding management for RTS/OCD signals. To meet full HART specifications or if the Demo Board is used in combination with a ready HART-compatible device, the user should consider protocol-level details, such as the proper structure for individual bytes (start/stop bits, parity) and the overall packet (HART telegram) structure.

2.4 4-20 mA Current Loop Implementation

As the physical layer for HART, the 4-20 mA current loop is used – an industry-standard analog interface commonly found in automation and process control applications. The user can use the demo board with either an internal or external current loop path. Switching between these options is achieved by attaching or detaching the “Onboard loop” jumpers.

If the jumpers are fitted, the current loop lines remain exposed to the screw terminals, and the onboard current path becomes active. The Host Device and Field Device functional parts are directly connected, allowing the user to evaluate the demo board with the shortest current path.

The user can use this mode of operation to write and test software, as the board functions as a simple UART-to-HART, HART-to-UART bridge.

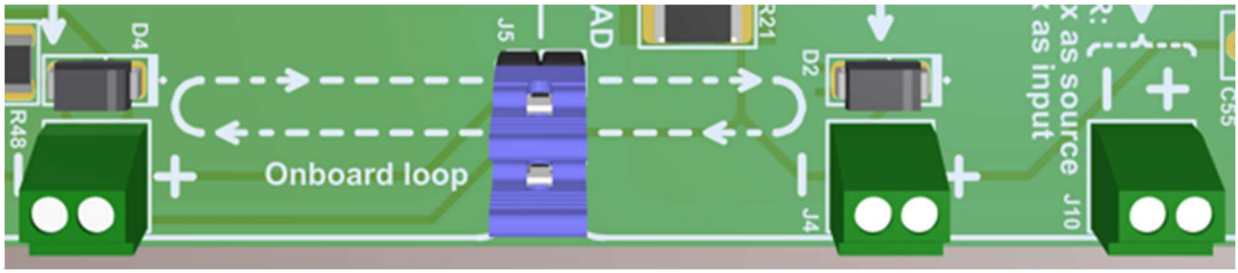
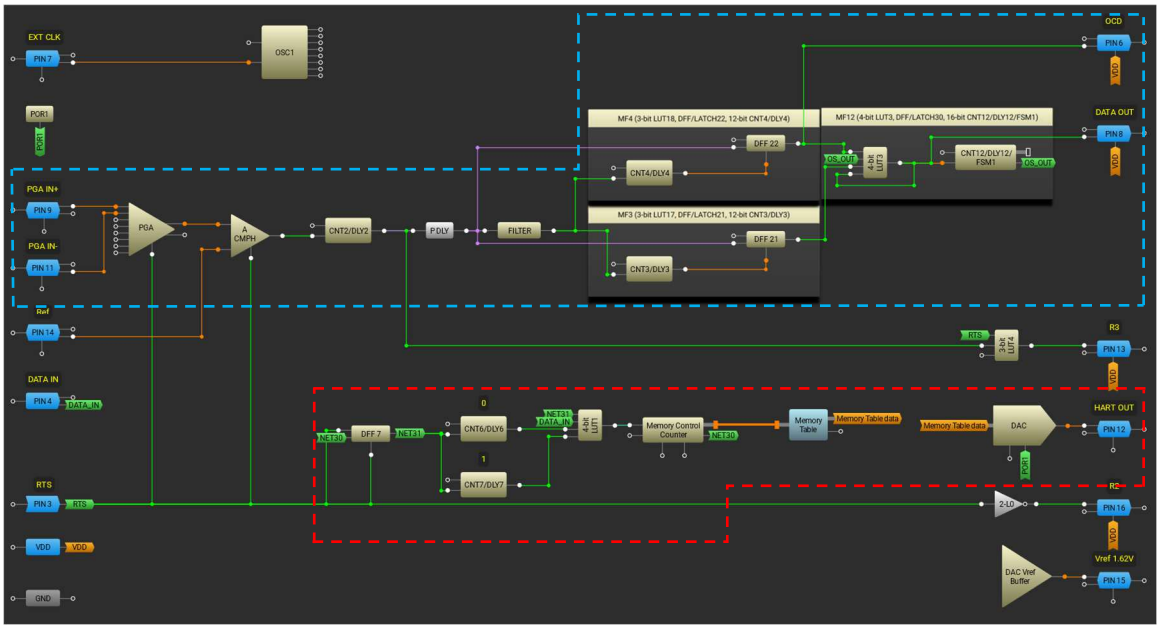


Figure 9. UART Interface with Flow Control Signals

With the “Onboard loop” jumpers removed, the current loop path is exposed only to the screw terminal blocks, disabling the internal connection and separating the two logical blocks on the demo board from each other. In this mode of operation, the user can attach an external 2-wire cable to the terminal blocks to simulate data transmission over a real cable interface. Another advantage of separating the parts of the demo board is the ability to use it as two independent devices in combination with HART-compatible third-party devices.

2.5 Design Review



(red line – signal modulation part; blue line signal demodulation part)

Figure 10. Hart Modem Design

The design can be divided into two main parts:

1. Signal Wave Modulation (red line)

Based on the DATA IN input, a clock is selected for the Memory Control Counter (when the RTS pin is 0) using DLY6 or DLY7, which modulates the sine wave frequency. For example, when DATA IN = 1, DLY7 is selected as the clock for the Memory Control Counter. Its counter data (CD) is calculated based on the following parameters:

$$CD = \frac{EXT_{CLK}}{\left(\frac{1200}{2200}\right) Words\ count} - 1$$

At UART high level = 1200 Hz HART, word count = 100, EXT_CLK = 4 MHz:

$$CD = \frac{4\ 10^6}{1200\ \ 100} - 1 = \sim 32$$

2. Signal Wave Demodulation (blue line)

The comparator is used to detect sine wave half-cycles. The duration of these half-cycles determines the sine wave frequency using MF3 and MF4 blocks. When the input sine wave frequency equals either 1200 Hz or 2200 Hz, one of the blocks (MF3 for 2200 Hz or MF4 for 1200 Hz) will trigger MF12. MF12 acts as a one-shot timer that generates pulses of constant duration for each bit according to the project baud rate of 1200.

3. Quick Start Guide

3.1 Setting up Work Setup

First, connect the power supply to the HOST part of the board (the power supply voltage should be 5 V).

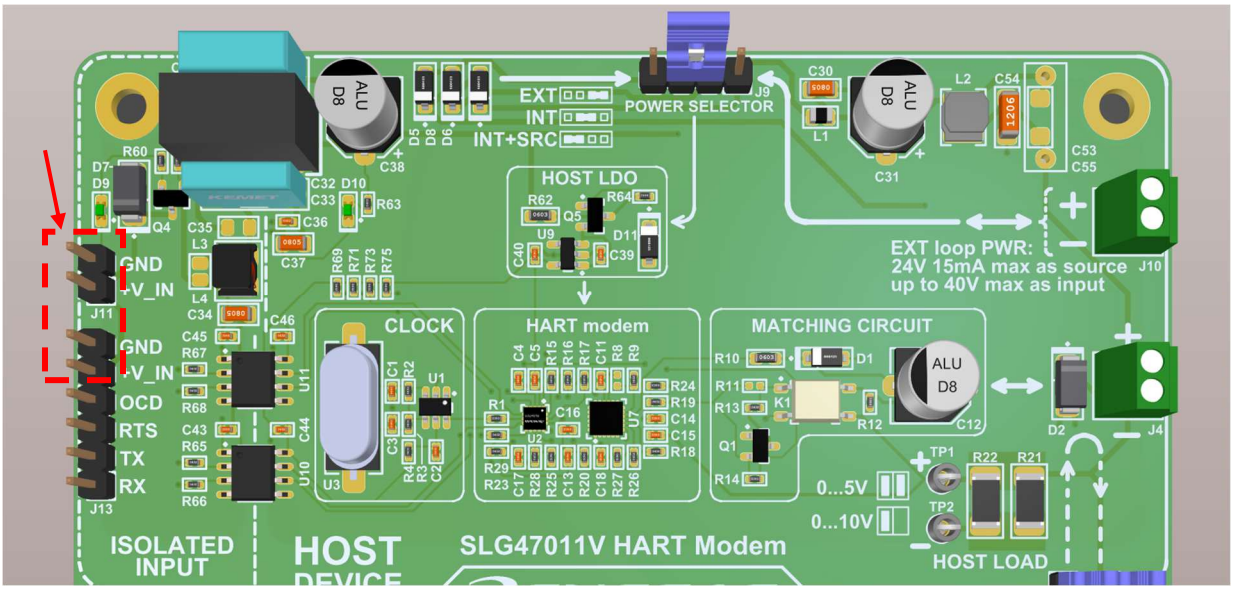


Figure 11 Board Power Supply Connection

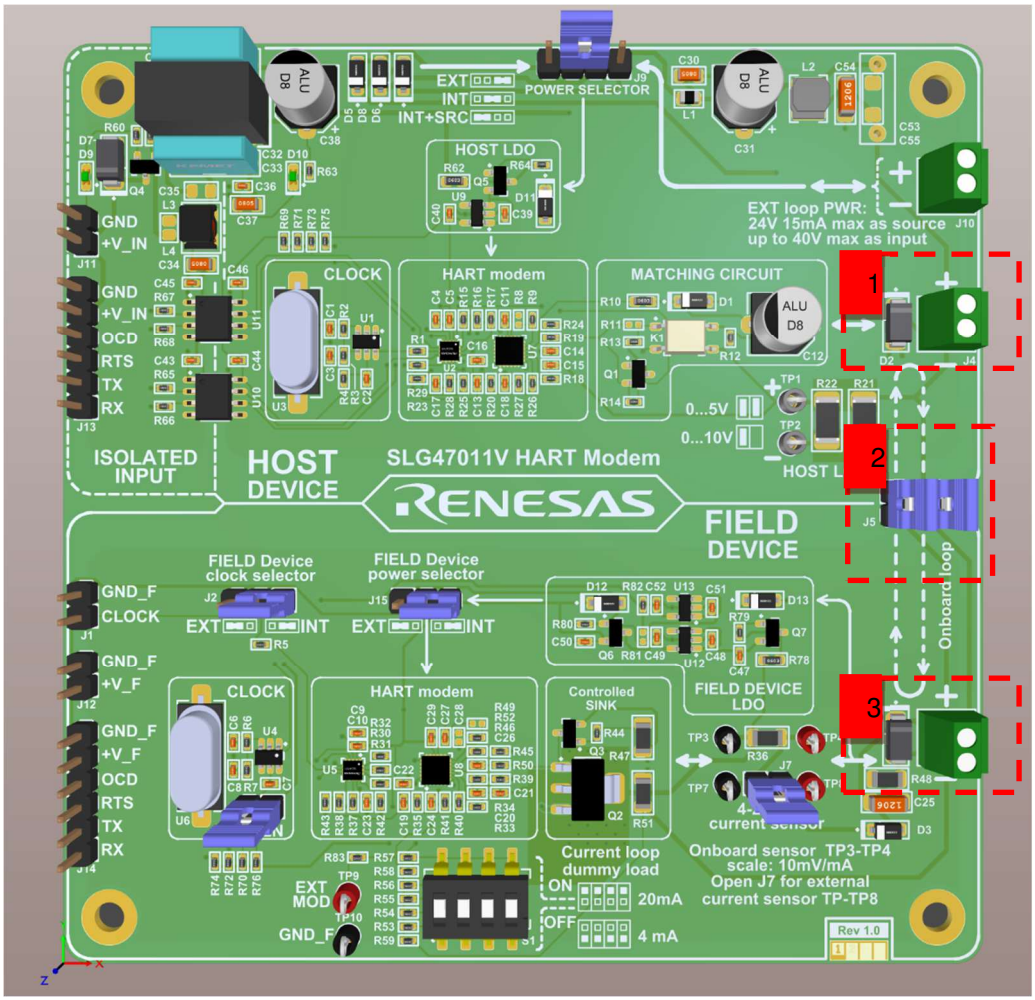
When the power supply is connected correctly, the onboard LED will light up. To start communication, connect RTS, TX, and RX on both the host and field devices. To transmit data from the host to the field device, pull down the RTS pin on the host device and pull it up on the field device (and vice versa for transferring data from the field device to the host). To view and control signal modulation, connect probes to TP1/TP2.

Note: This configuration is for the internal current loop.

For external loop usage:

- Disconnect the jumpers.
- Connect the external loop to the J4 terminals for the host device and external field device.
- Connect to J5 for the field device and external host device.

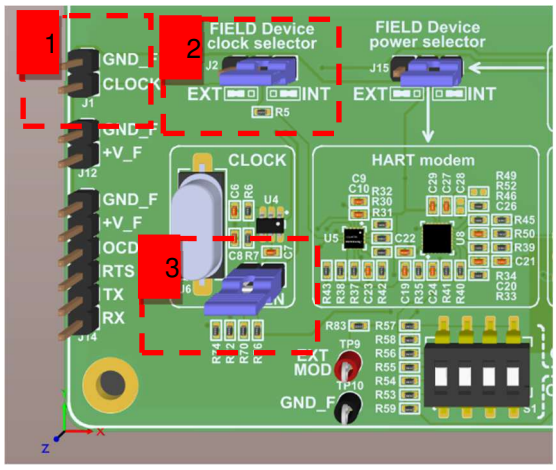
- Optionally, connect terminals J4 and J5 together to test the modem with an external line.



1 – external wire to Host Device; 2 – internal loop; 3 – external wire to Field Device

Figure 12. Current Loop

The board allows the selection of an external clock for the field device, with the default frequency set to 4 MHz. The clock frequency cannot be lower than 480 kHz. If using a clock frequency other than 4 MHz, the counter data must be changed in CNT6 and CNT7 in the design file. To select the external clock, change the jumper position to “EXT” and remove the “EN” jumper.



1– PINs for connecting external clock; 2 – clock selector; 3 – internal CLK enable

Figure 13. Field Device CLK Choose

For flexibility, the board offers selectable power supplies for the current loop and field device.

Note: If external power is chosen for the current loop, a 5 V power supply for the logic on the host part must still be connected.

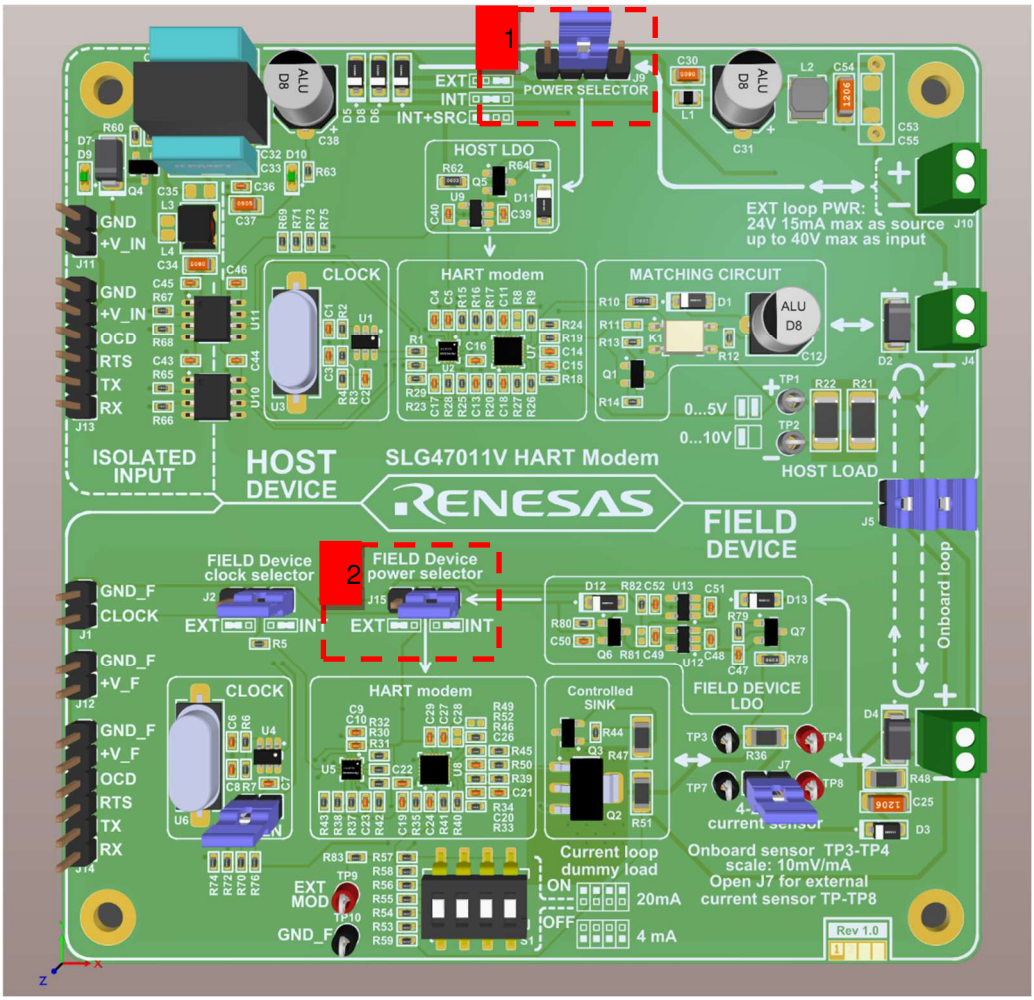
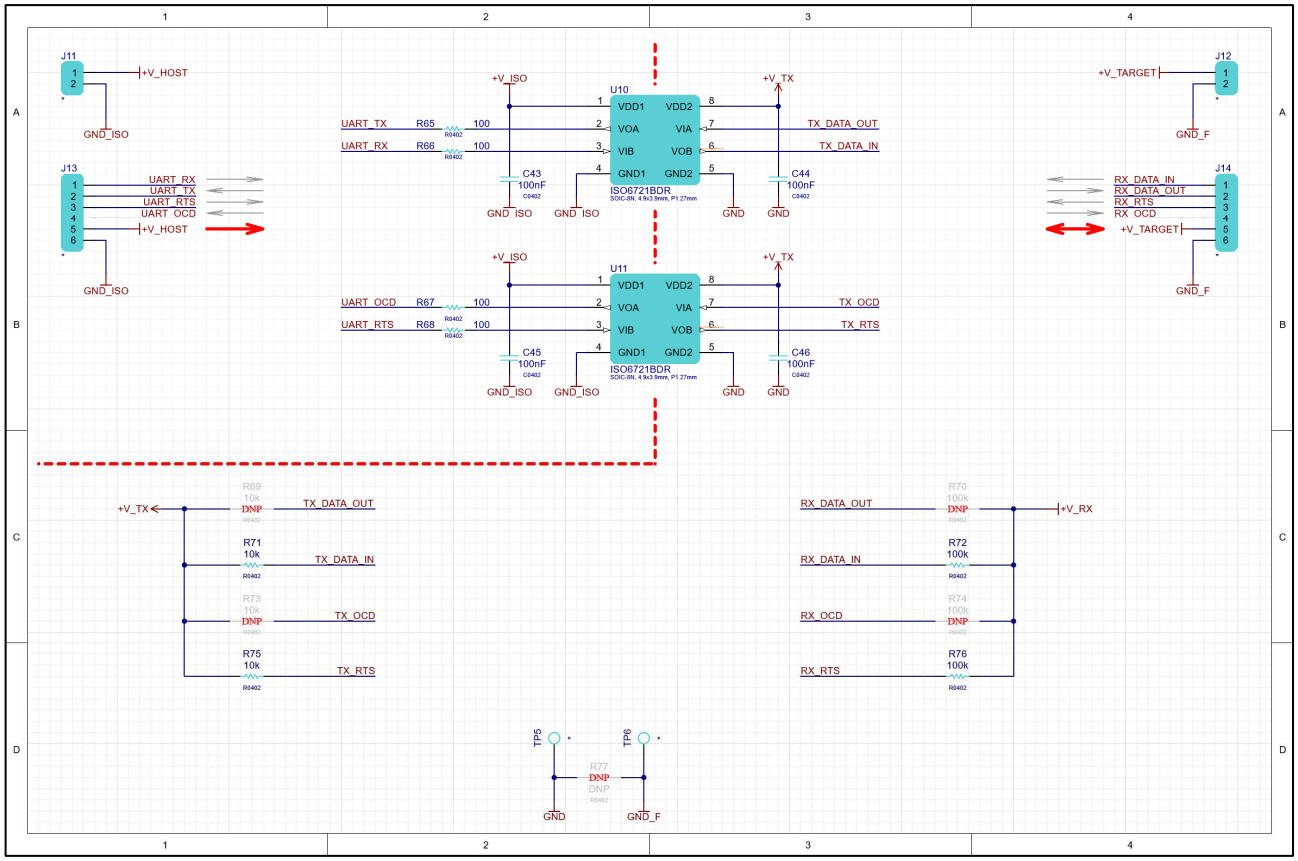
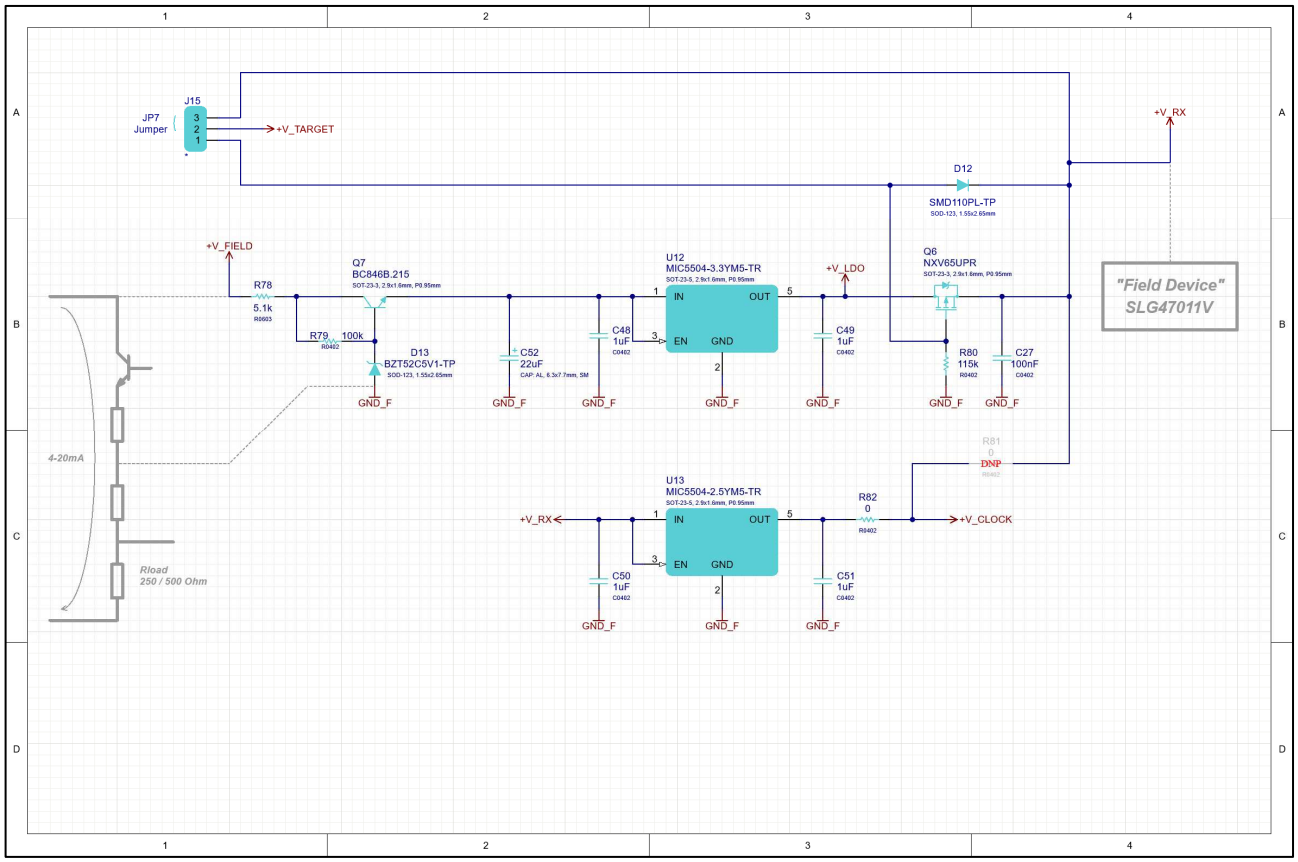
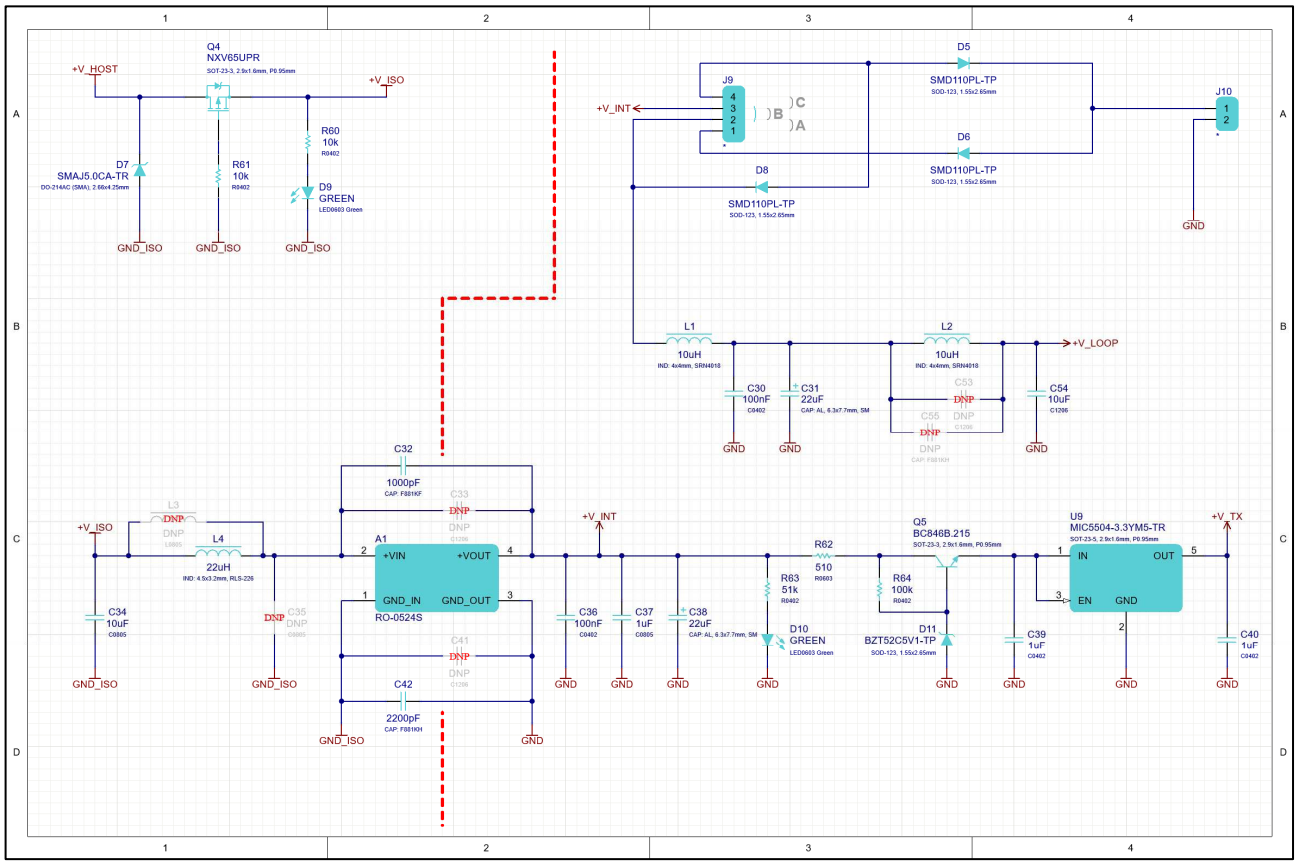


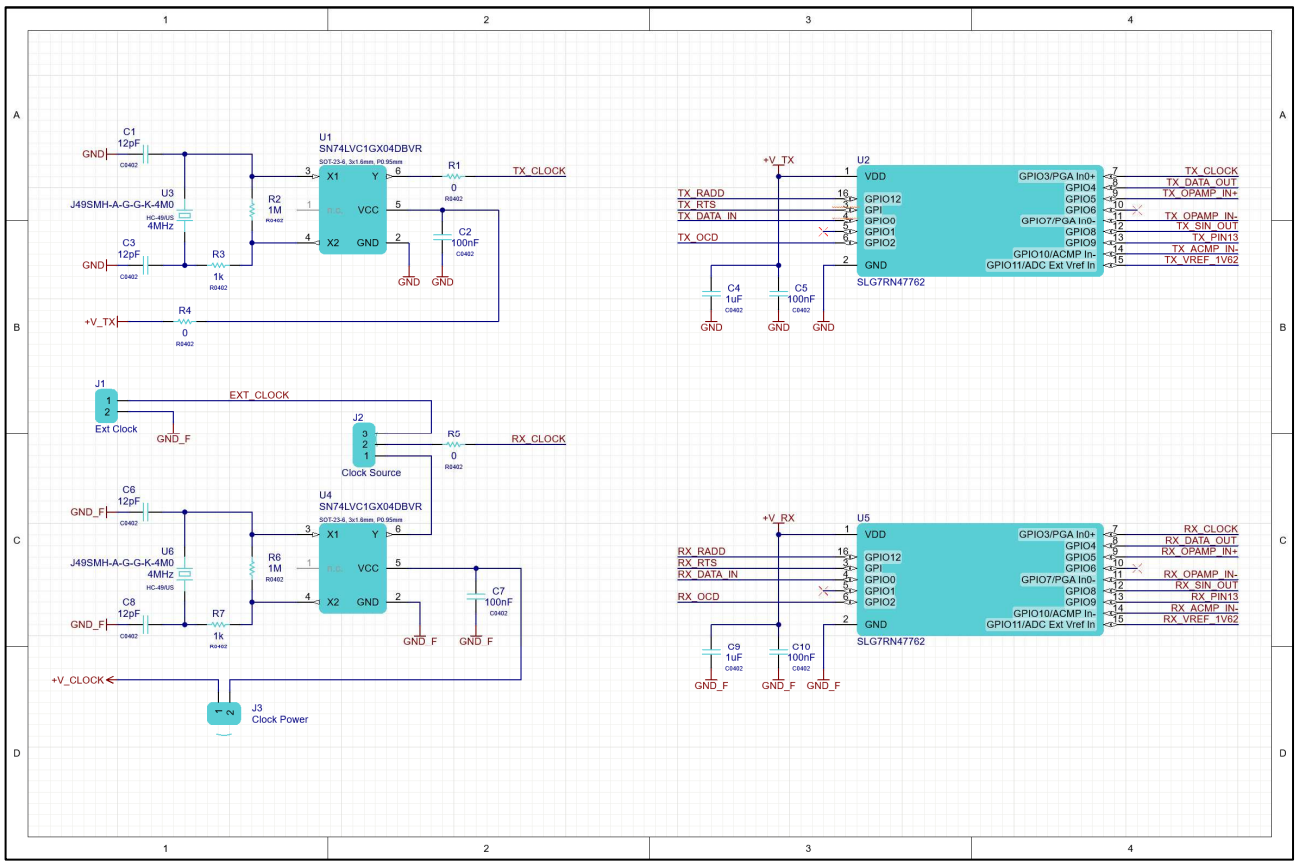
Figure 14. Power Selector for Current Loop (1) and Field Device (2)

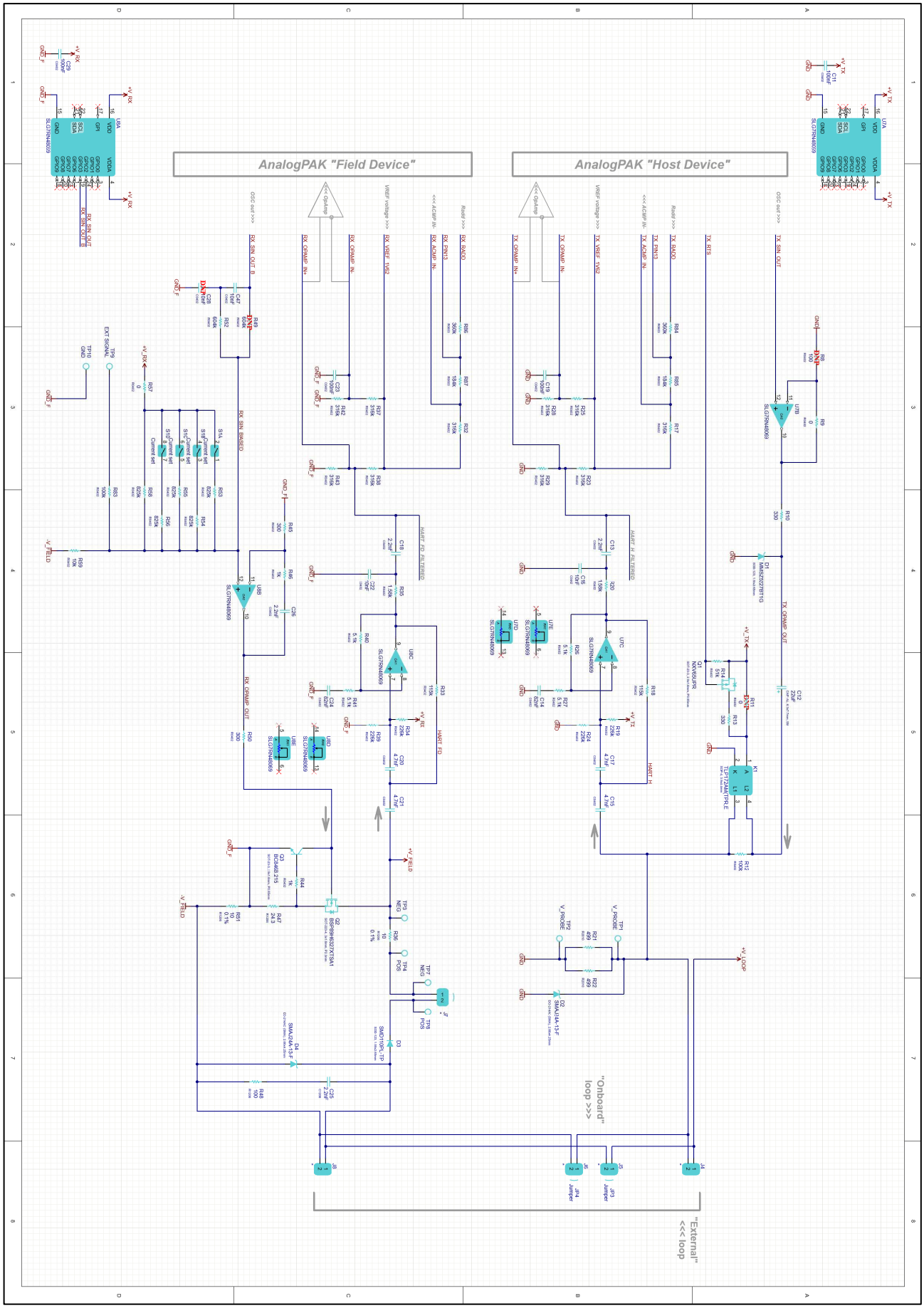
4. Board Schematics











5. Bill of Materials

#	Designator	Name	Manufacturer Part Number 1	Manufacturer 1	Q-ty
1	A1	RO-0524S	RO-0524S	Recom	1
2	BP1, BP2, BP3, BP4, BP5	SJ61A6	7010334512	3M	5
3	C1, C3, C6, C8	12pF 5% 50V C0G/NP0 0402	KGM05ACG1H120JH	Kyocera AVX	4
4	C2, C5, C7, C10, C11, C19, C23, C27, C29, C30, C36, C43, C44, C45, C46	100nF 10% 50V X7R 0402	GRM155R71H104KE14J	Murata	15
5	C4, C9, C39, C40, C48, C49, C50, C51	1µF 20% 6.3V X5R 0402	CL05A105MQ5NNNC	Samsung	8
6	C12, C31, C38, C52	22µF 50V Aluminium 6.3x7.7mm	UWT1H220MCL6GS	Nichicon	4
7	C13, C18, C26	2.2nF 10% 50V X7R 0402	GRM155R71H222KA01D	Murata	3
8	C14, C24	82nF 10% 16V X7R 0402	GCM155R71C823KA55D	Murata	2
9	C15, C17, C20, C21	4.7nF 10% 25V X7R 0402	GRM155R71H472KA01D	Murata	4
10	C16, C22, C47	10nF 10% 50V X7R 0402	GCM155R71H103KA55D	Murata	3
11	C25	2.2nF 10% 50V X7R 1206	CC1206KRX7R9BB222	Yageo	1
12	C32	1000pF 20% 1kV Polypropylen, Metallized 10mm*3mm	F881KF102M300A	KEMET	1
13	C34	10µF 10% 25V X5R 0805	CL21A106KOQNNNG	Samsung	1
14	C37	1µF 10% 50V X7R 0805	CL21B105KBFNNNE	Samsung	1
15	C42	2200pF 20% 1kV Polypropylen, Metallized 10mm*4mm	F881KH222M300L	KEMET	1
16	C54	10 µF 10% 50V X7R 1206	CL31B106KBHNNNE#	Samsung	1
17	D1	MMSZ5227BT1G	MMSZ5227BT1G	ON Semiconductor	1
18	D2, D4	SMAJ24A-13-F	SMAJ24A-13-F	Diodes	2
19	D3, D5, D6, D8, D12	SMD110PL-TP	SMD110PL-TP	MCC	5
20	D7	SMAJ5.0CA-TR	SMAJ5.0CA-TR	STMicroelectronics	1
21	D9, D10	Led H	B1911NG--20D000214U1930	Inolux	2
22	D11, D13	BZT52C5V1-TP	BZT52C5V1-TP	MCC	2
23	JP1, JP2, JP3, JP4, JP5, JP6, JP7	Jumper	09200-71-BDGB00	METZ CONNECT	7
24	K1	TLP172AM(TPR,E	TLP172AM(TPR,E	Toshiba	1
25	L1, L2	10µH 1.3A	SRN4018-100M	Bourns	2
26	L4	22µH 630mA	RLS-226	Recom	1
27	Q1, Q4, Q6	NXV65UPR	NXV65UPR	Nexperia	3
28	Q2	BSP89H6327XTSA1	BSP89H6327XTSA1	Infineon	1
29	Q3, Q5, Q7	BC846B.215	BC846B,215	Nexperia USA	3
30	R1, R4, R5, R9, R57, R82	0 5% 0402	RC0402JR-070RL	Yageo	6
31	R2, R6	1M 5% 0402	RC0402FR-071ML	Yageo	2
32	R3, R7, R44, R46	1k 1% 0402	RC0402FR-071KL	Yageo	4
33	R10, R13	330 1% 0603	RC0603FR-07330RL	Yageo	2
34	R12, R64, R72, R76, R79, R83	100k 1% 0402	RC0402FR-07100KL	Yageo	6
35	R14, R63	51k 1% 0402	RC0402FR-0751KL	Yageo	2
36	R17, R23, R25, R28, R29, R32, R37, R38, R42, R43	316k 0.1% 0402	CPF0402B316KE1	TE Connectivity	10
37	R18, R33, R80	115k 1% 0402	RC0402FR-07115KL	Yageo	3
38	R19, R24, R34, R39	226k 1% 0402	RC0402FR-07226KL	Yageo	4

#	Designator	Name	Manufacturer Part Number 1	Manufacturer 1	Q-ty
39	R20, R35	1.58k 1% 0402	RC0402FR-071K58L	Yageo	2
40	R21, R22	499 1% 2010	RC2010FK-07499RL	Yageo	2
41	R26, R27, R40, R41	5.1k 1% 0402	RC0402FR-075K1L	Yageo	4
42	R36, R51	10 0.1% 1206	RNCS1206BKE10R0	Stackpole Electronics	2
43	R45, R50	300 1% 0402	RC0402JR-07300RL	Yageo	2
44	R47	24.3 1% 1206	RC1206FR-0724R3L	Yageo	1
45	R48	100 1% 1206	RC1206FR-07100RL	Yageo	1
46	R52	604k 1% 0402	RC0402FR-07604KL	Yageo	1
47	R53, R54, R55, R56, R58	825k 1% 0402	RC0402FR-07825KL	Yageo	5
48	R59, R60, R61, R71, R75	10k 1% 0402	RC0402FR-0710KL	Yageo	5
49	R62	510 5% 0603	RC0603JR-07100RL	Yageo	1
50	R65, R66, R67, R68	100 1% 0402	RC0402FR-07100RL	Yageo	4
51	R78	5.1k 1% 0603	RC0603FR-075K1L	Yageo	1
52	R84, R86	360k 0.1% 0603	RT0603BRD07360KL	Yageo	2
53	R85, R87	184k 0.1% 0603	RT0603BRD07184KL	Yageo	2
54	S1	219-4MSTR	219-4MSTR	CTS	1
55	U1, U4	SN74LVC1GX04DBVR	SN74LVC1GX04DBVR	Texas Instruments	2
56	U2, U5	SLG7RN47762		Renesas Electronics America Inc	2
57	U3, U6	J49SMH-A-G-G-K-4M0	J49SMH-A-G-G-K-4M0	Jauch	2
58	U7, U8	SLG7RN48069	SLG7RN48069	Renesas Electronics America Inc	2
59	U9, U12	MIC5504-3.3YM5-TR	MIC5504-3.3YM5-TR	Microchip	2
60	U10, U11	ISO6721BDR	ISO6721BDR	Texas Instruments	2
61	U13	MIC5504-2.5YM5-TR	MIC5504-2.5YM5-TR	Microchip	1

6. Revision History

Revision	Date	Description
1.00	Jan 23, 2025	Initial release.