SLG51001C-EVB

SLG51001C Power GreenPAK Evaluation Board R1.1

SLG51001C Evaluation Board (EVB) provides programming, emulation, and testing functions for the SLG51001C. Working in pair with the Go Configure™ Software Hub it can be used as:

- standalone board
- with the GreenPAK Serial Debugger
- with the Power GreenPAK Development Motherboard

Features

- LDO input and output connectors with Kelvin sense
- RF connectors for each LDO input and output channel
- GPIO connector
- GreenPAK Serial Debugger connector for quick debugging
- Power GreenPAK Development Motherboard connector for advanced prototyping

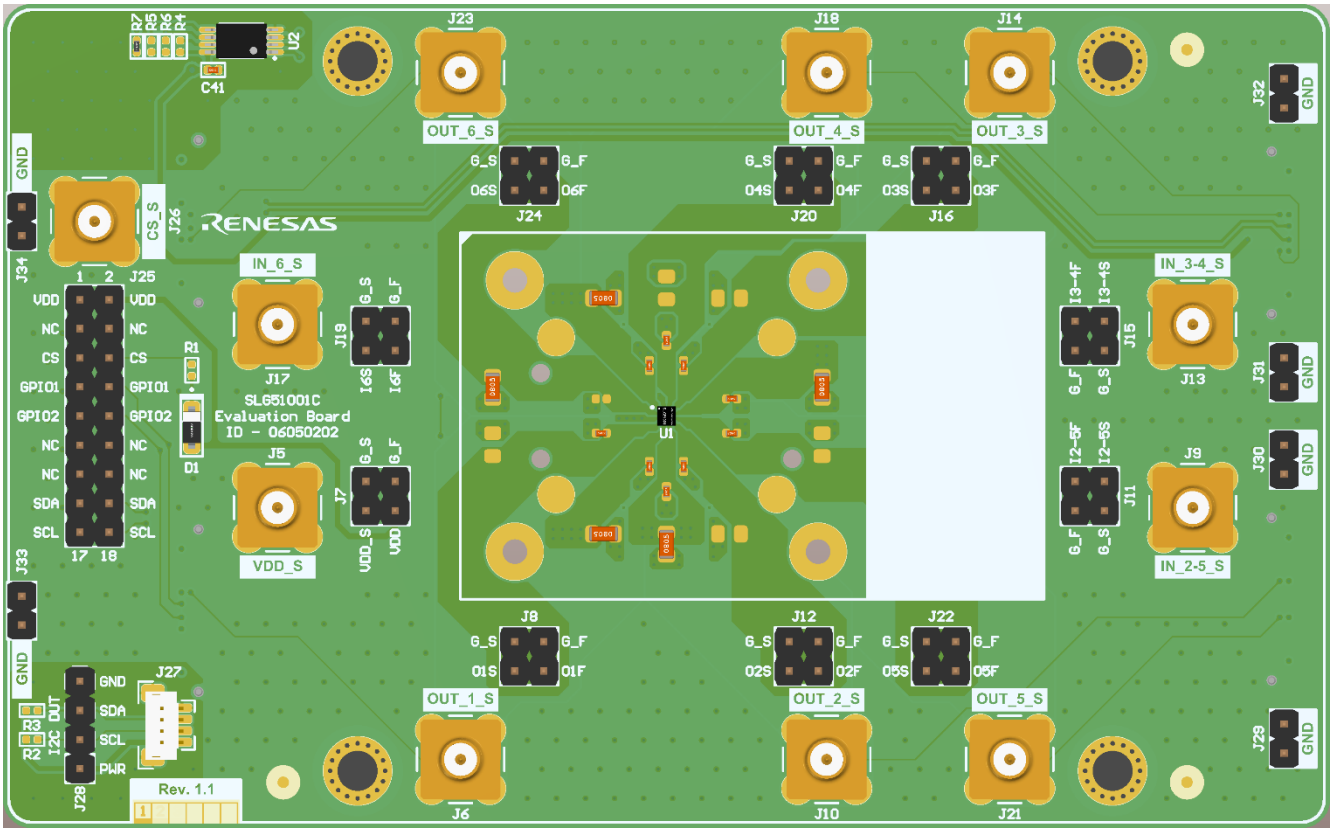

Figure 1. SLG51001C Evaluation Board

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1. Functional Description

SLG51001C Evaluation Board provides connection between an IC and the following two devices for programming, emulation, and testing functions:

- Power GreenPAK Development Motherboard (PGP_DM)
- GreenPAK Serial Debugger (GSD).

This Evaluation Board can be used to apply the Power GreenPAK IC to the custom design with a minimum of additional tools. The Evaluation Board has the following connectors, shown in Figure 2 and Figure 3:

- Input Force (power) pins for LDO channels of the SLG51001C
- Output Force (power) pins for LDO channels of the SLG51001C
- Input Sense (Kelvin) pins for input voltage measurements
- Output Sense (Kelvin) pins for output voltage measurements
- Connector for GPIO signals
- Connector for the GreenPAK Serial Debugger
- Several ground pins distributed across the board.

Figure 2 shows the main points to connect supply voltage to LDOs, LDOs output load, GPIO signals, and GSD connector. Figure 3 shows the points for more accurate measurements using SMB connectors.

Input Force pins are designed to provide input voltage to the LDO.

Output Force pins are designed for connection to the load, external circuit, and others.

Pin headers have power lines marked with the "F" suffix. For example, for positive power lines there are "VDD" – force line for the V_{DD} pin, "I3-4F" – force line for the input channel 3 and channel 4, "O3F" – force line for the output channel 3, while for negative power lines there is "G_F" – force line for ground.

The Evaluation Board can be connected to the main Development Motherboard or directly by the pin headers. The first option is standard for users and the second option allows to shorten the path from the source/sink connected to the pin headers to the device under test (DUT) IC. This connection can be used for more accurate parameters testing of the DUT IC, such as Power Supply Rejection Ratio (PSRR), transient response, and others.

Input/Output Sense pins are designed for precise voltage measurements and to eliminate voltage drop caused by the load current across the PCB polygons, between the connector pins and the IC pads. Also, they can be used as a voltage sense for more accurate voltage control near the SLG51001C. They are marked on the board with the "S" suffix. For example: "VDD_S", 'I3-4S', "O3S" – for positive sense lines and "G_S" – for negative sense lines. It is important to connect only the measuring equipment to these pins that consumes low current, otherwise, by connecting high load current, these signal lines may burn out.

GPIO signals connector is designed for interacting with external circuits, make external pull-up pin function, inject signals, and others.

GreenPAK Serial Debugger connector is designed to connect the GSD board that allows to emulate the IC through the Go Configure™ Software Hub for further custom design evaluation. This is a “light” version of the tool to interact with the IC. The more advanced tool is the Power GreenPAK Development Motherboard. Connectors for the PGP_DM are located on the bottom side of the Evaluation Board and not shown in Figure 1.

Ground pins are located across the PCB and designed for convenient signal connections to the board.

Board limitations are determined by the SLG51001C. Recommended input voltage range for LDO channels and GPIO inputs are described in Table 1.

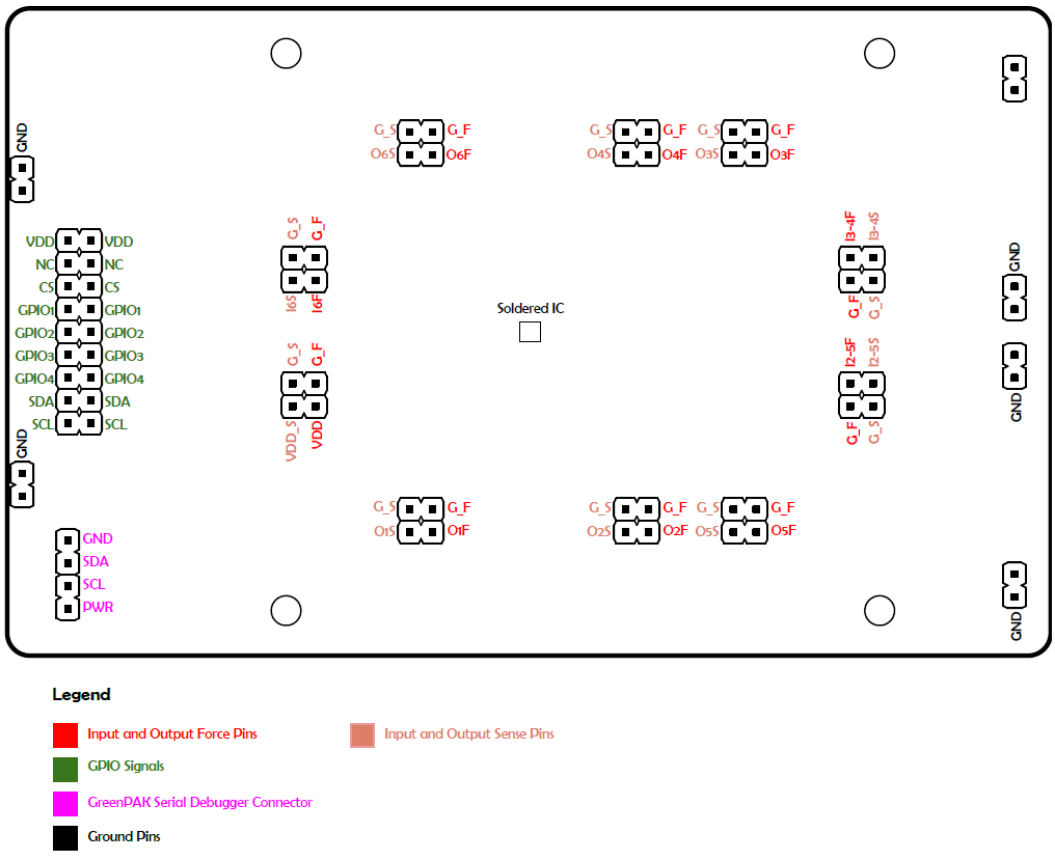

Figure 2. Pin Location of LDO Input/Output with Kelvin Functions Pins, GPIO Pins, GSD Connector on Evaluation Board

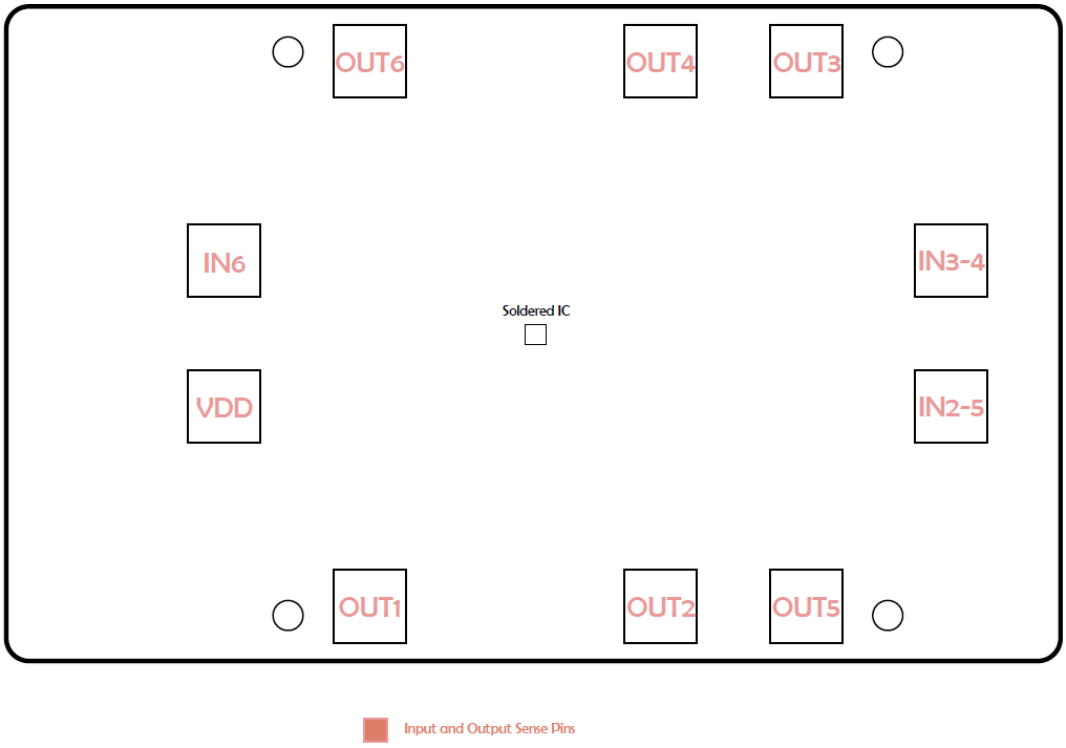

Figure 3. Pin Location of SMB Measurement Connectors on Evaluation Board

Table 1. Recommended Operating Conditions

Parameter		Min	Max	Unit
Power Supply Voltage on V_{DD} Pin		2.8	5.0	V
Power Supply Voltage on V_{IN2-5}, V_{IN3-4} Pins		1.7	5.0	V
Power Supply Voltage on V_{IN6} Pin	LDO Mode	0.8	1.5	V
	Load Switch Mode	0.5	1.25	V
Voltage on GPIO1 to GPIO3 and GPI4 Pins		0	1.8	V
Voltage on CS Pin		0	V_{DD}	V
Operating Ambient Temperature Range		-40	+85	°C

Figure 4 demonstrates connections between connectors and LDO channels of the IC. Sense lines (also, connectors) are designed only for the measuring equipment and cannot be used for power distribution. Otherwise, Kelvin functions may burn out on the PCB and the Evaluation Board will be damaged and inoperable.

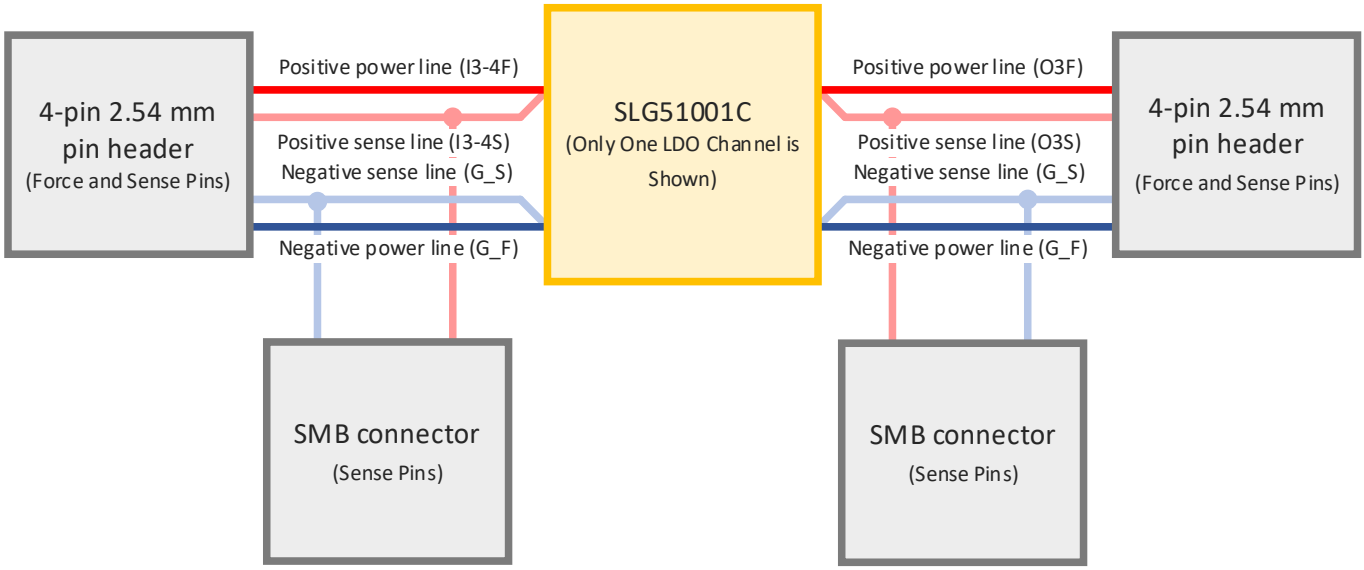

Figure 4. Input/Output Force LDO Pins with Kelvin Functions

2. Working with the SLG51001C Evaluation Board

2.1 Using GreenPAK Serial Debugger with Evaluation Board

To start using the Evaluation Board for chip emulation, the GreenPAK Serial Debugger and at least a single-channel power supply are required. For IC emulation, V_{DD} needs to be powered on and the chip select (CS) should be set High.

Please note that for the single-channel power supply this can be done using a wire on the GPIO connector – between position V_{DD} – CS.

Power up the IC and insert the GSD board as shown in Figure 5. A typical connection circuit for chip emulation is shown in Figure 6.

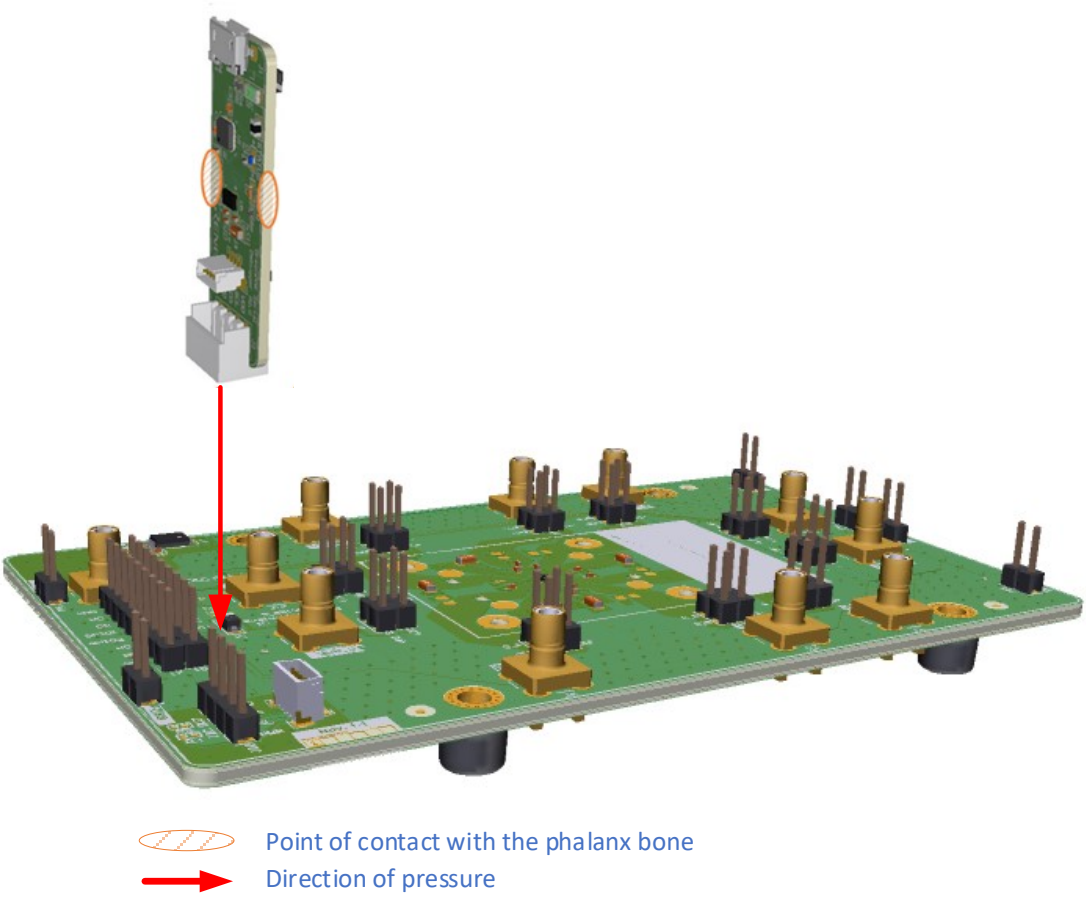

Figure 5. Connecting GSD Board to Evaluation Board

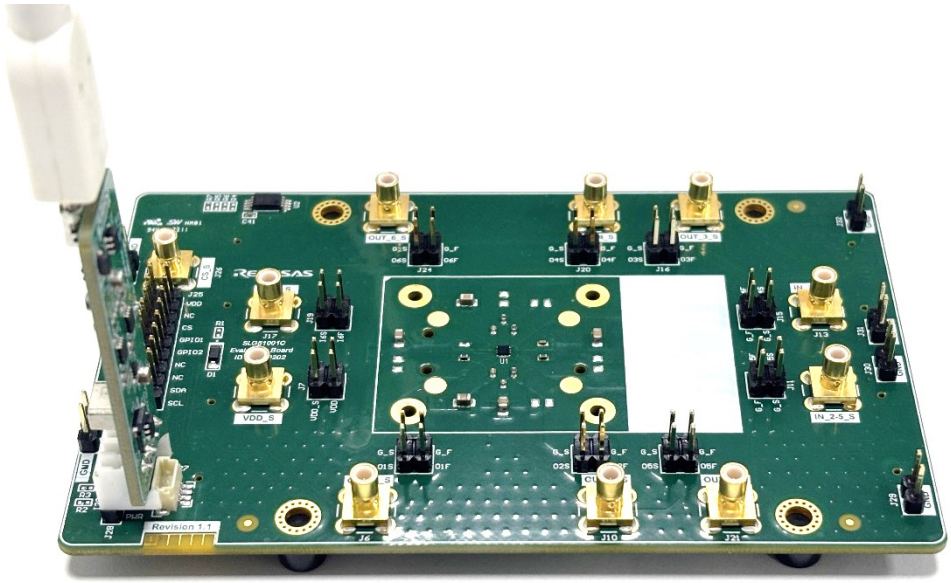

Figure 6. Evaluation Board with GreenPAK Serial Debugger

I²C levels must be within the allowed range, shown in Table 2, that corresponds to one of the configured settings in Go Configure™ Software Hub, as shown in Figure 7.

Table 2. Brief I²C Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage	--	0.4 * V_{DDLV}[1]	--	0.7 * V_{DDLV}[1]	V
V_{IL}	LOW level input voltage	--	0.3 * V_{DDLV}[1]	--	0.6 * V_{DDLV}[1]	V
[1] V_{DDLV} defines the voltage level for I²C pins (GPIO3_SDA, GPI4_SCL) in Go Configure™ Software Hub and can be selected as 1.2 V or 1.8 V.						

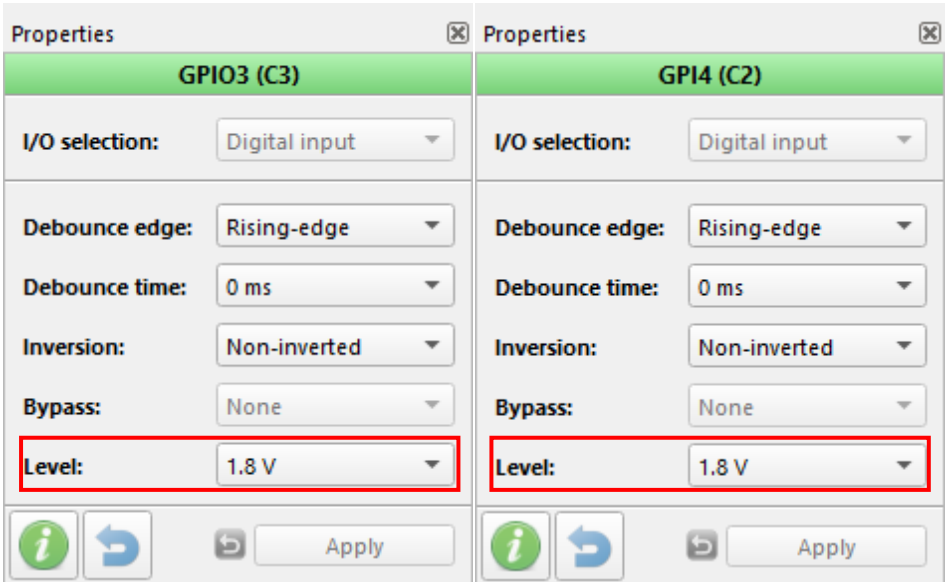

Figure 7. V_{DDLV} Level Settings for I²C in Go Configure™ Software Hub

Figure 8 shows debugging control setup for working with GSD.

Please note that the programming feature for OTP devices is not available using GSD tool.

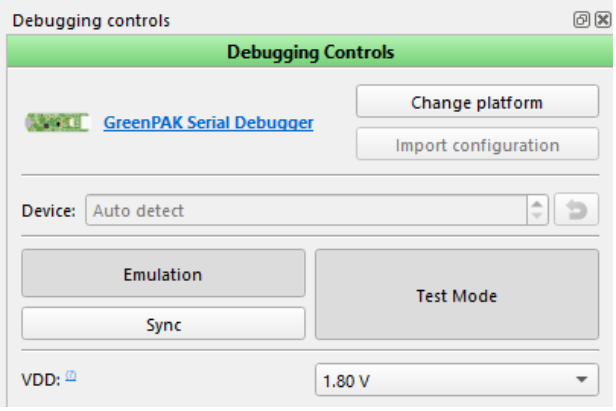

Figure 8. GSD Debugging Setup

2.2 Precise Measurements using Evaluation Board

As mentioned above, precise measurements, such as PSRR, transient response, and others, can be performed on this board without any additional modifications to the PCB.

Figure 1(top side) and Figure 9 (bottom side) show default placement of the board components.

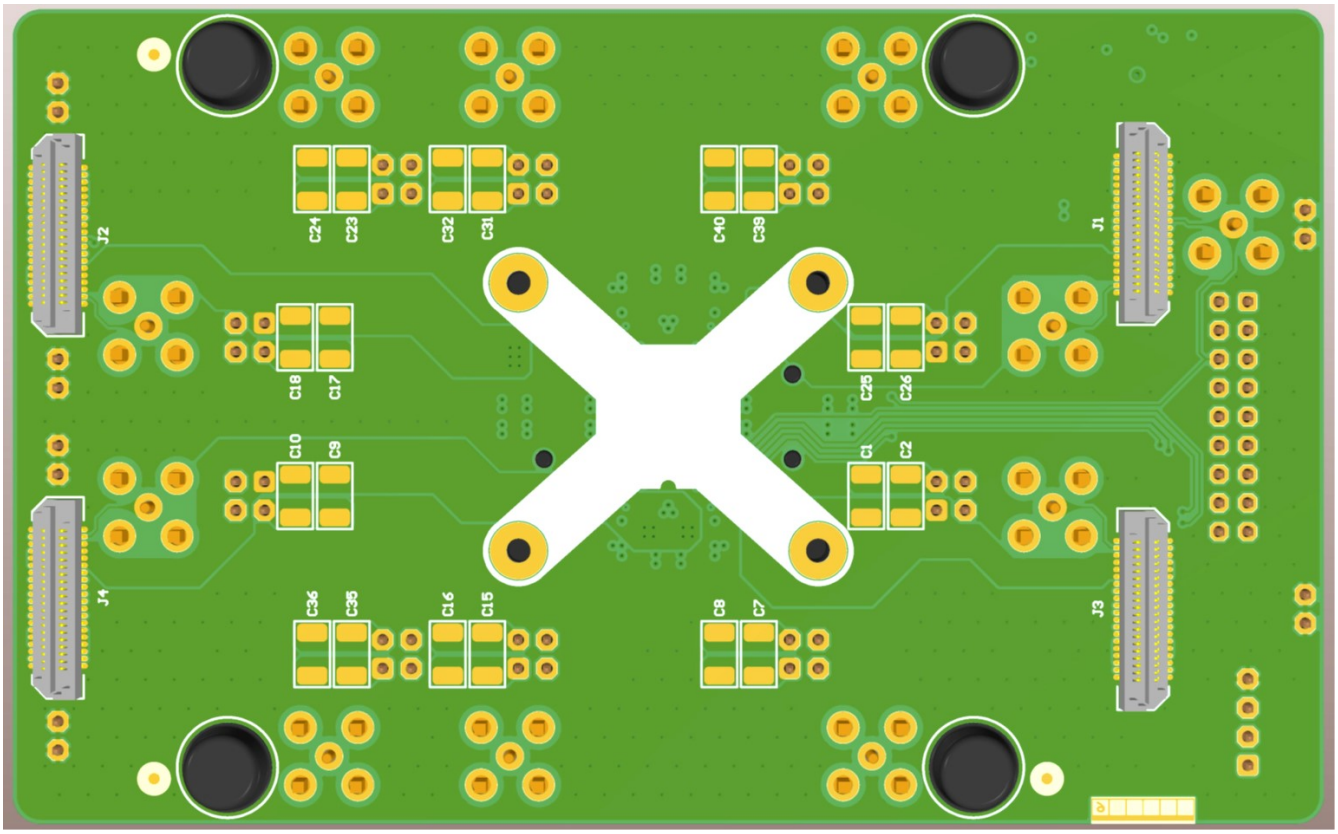

Figure 9. Bottom Side of the Evaluation Board

2.3 Using Power GreenPAK Development Motherboard with Evaluation Board

As was previously stated, the Evaluation Board can be used in pair with the Power GreenPAK Development Motherboard, as shown in Figure 10. There are two revisions of such board – R1.0 and R1.1. Further description will be referred to R1.0.

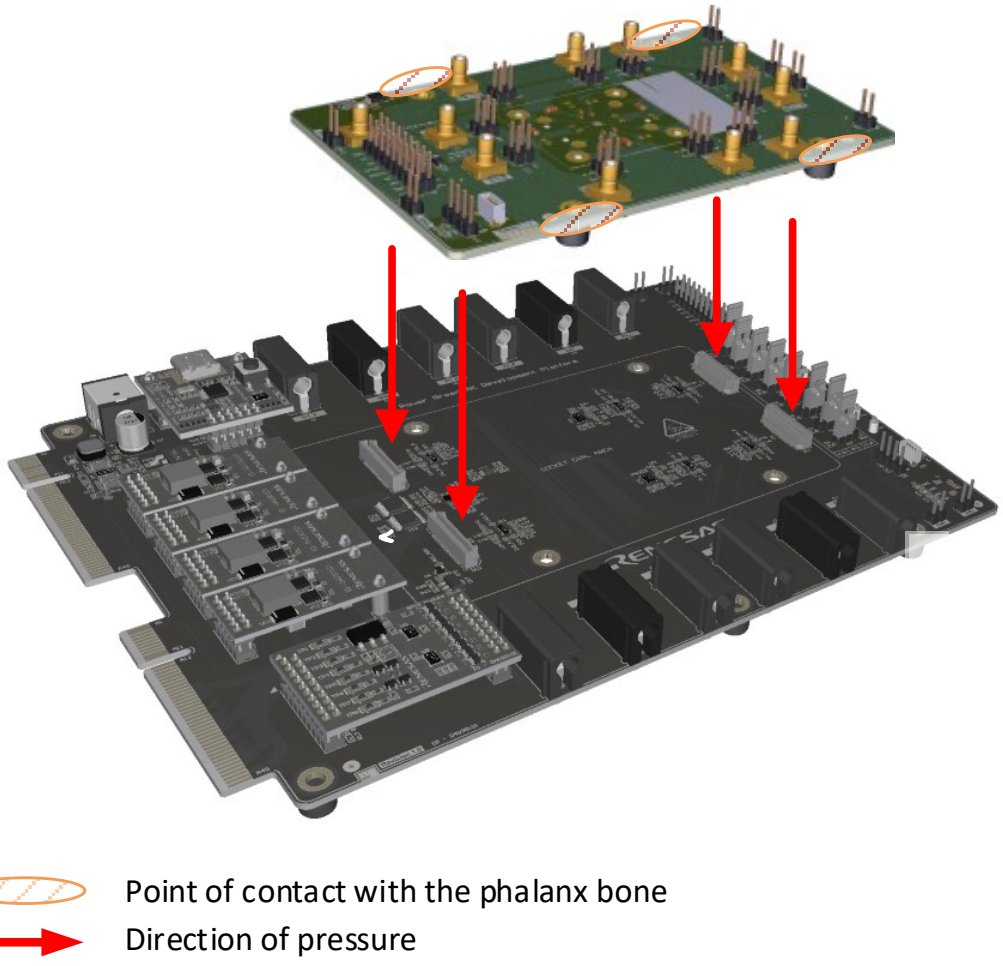

Figure 10. Inserting Evaluation Board on PGP_DM

To start using the PGP_DM, the user must have all items listed below:

- AC/DC power adapter
- USB cable
- Evaluation Board.

When all items above are available, follow the next steps:

1. Connect the AC/DC power adapter to the Motherboard (the sequence of connecting the AC and DC cables does not matter).
2. Connect the USB connector to the PC and the Motherboard (the sequence of connecting the PC and the Motherboard does not matter).
3. Open the software Go Configure™ Software Hub on the PC and start building the project. The software can be downloaded here.

When all connections are correct, “POWER” and “STATUS” LEDs on the USB Serial Module should be ON (static), D2 LED on the Motherboard and TP5, TP6, TP8 (in PGP_DM_R1.1 renamed to CS) LEDs on the GPIO Module should also be ON. The location of these LEDs is shown in Figure 11.

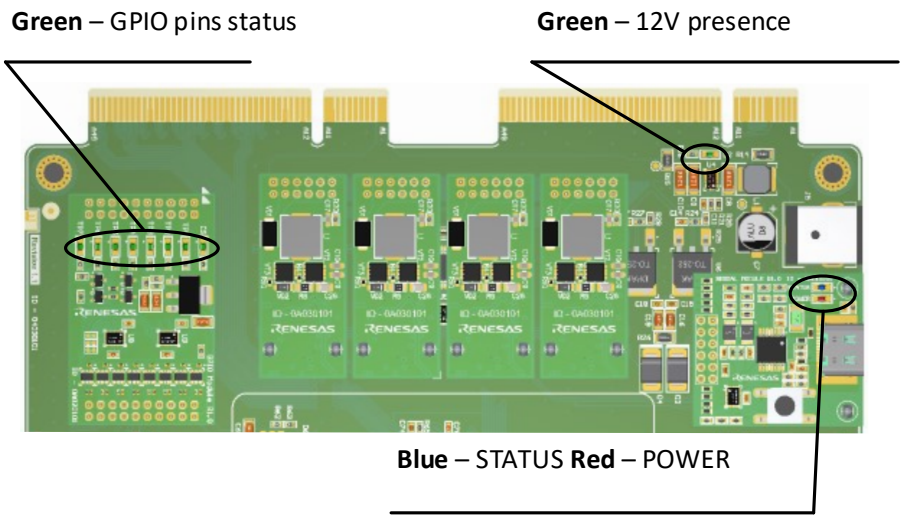

Figure 11. LEDs Location on PGP_DM

To emulate and program the IC, the Evaluation Board should be inserted in the PGP_DM. To do so, find the evaluation board area on the PGP_DM, as shown in Figure 12, and connect the Evaluation Board to the PGP_DM through the J18-J21, DC1-DC4 connectors, highlighted in red.

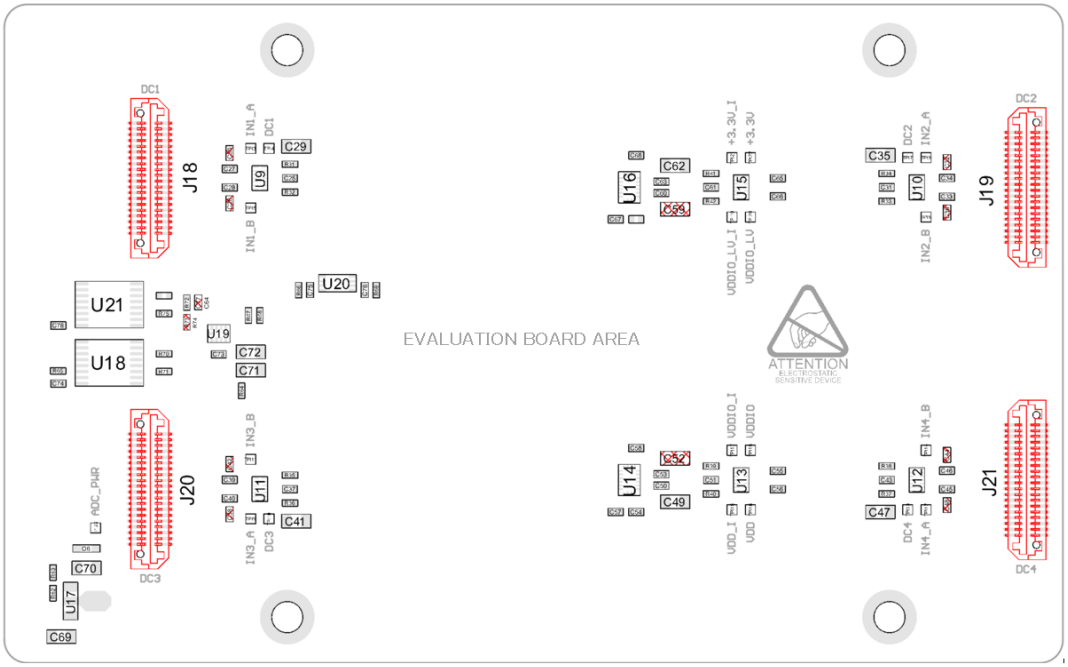

Figure 12. Evaluation Board Area on the PGP_DM

Figure 13 shows debugging control setup for working with the PGP_DM. Programming option for OTP devices is available only when using the PGP_DM.

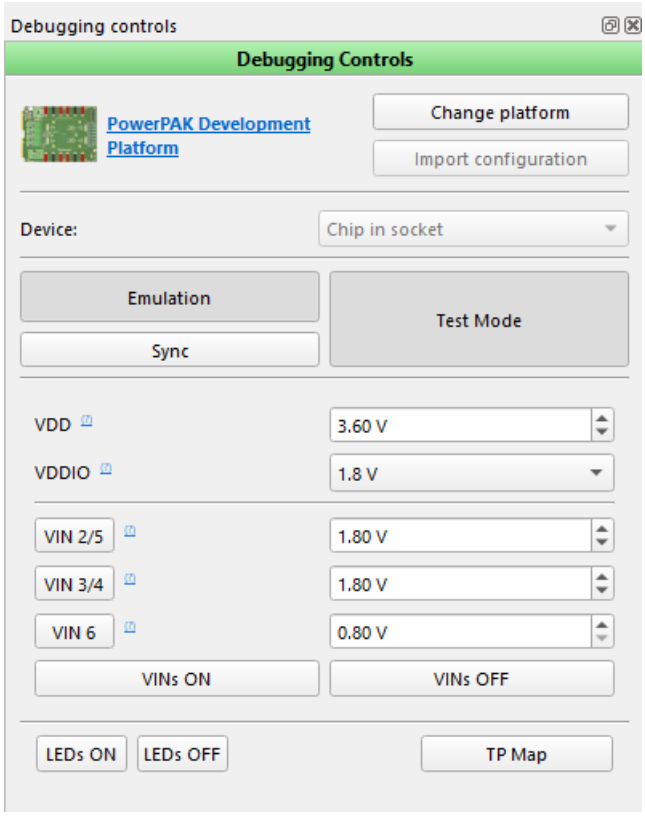

Figure 13. PGP_DM Debugging Setup

LED state indication feature is available for all TPs, GPIO pull-up, pull-down. TPs are connected to the GPIO IC pins of the installed Evaluation Board. Correspondence of TPs to the GPIO ports can be checked in the design by clicking the TP Map button shown in Figure 13.

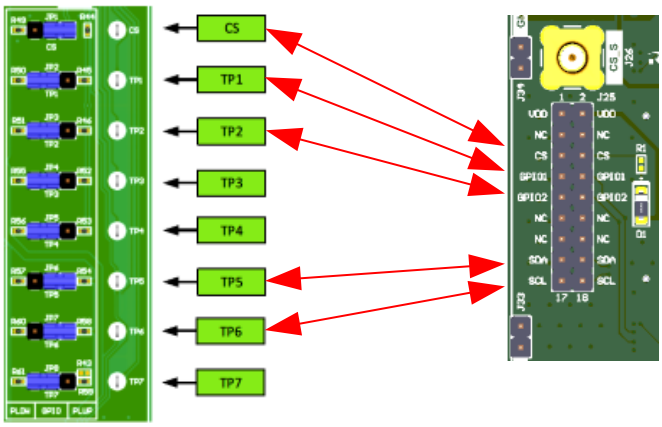

Figure 14. PGP_DM and SLG51001C-EVB GPIO Connector Pinout Correspondence

3. Ordering Information

Part Number	Description
SLG51001C-EVB	SLG51001C Power GreenPAK Evaluation Board R1.1

4. Revision History

Revision	Date	Description
1.01	Oct 17, 2024	Change details: • Replaced Figures 1, 5, 6 to show the latest EVB revision from 1.0 to 1.1 and name from SLG51001C Socket Eval to SLG51001C Evaluation Board. • Replaced Figure 12 to show the latest Evaluation Board Area name on the PGP_DM • Changed the mentions of board revision from 1.0 to 1.1 in the whole document. • Updated Figure 15 because of the changed C5 capacitance value in revision 1.1 to 4.7 uF. • Updated A.2 BOM section. • Added Figure 18
1.00	Aug 12, 2024	Initial release

A. Evaluation Board Documentation

A.1 Schematic

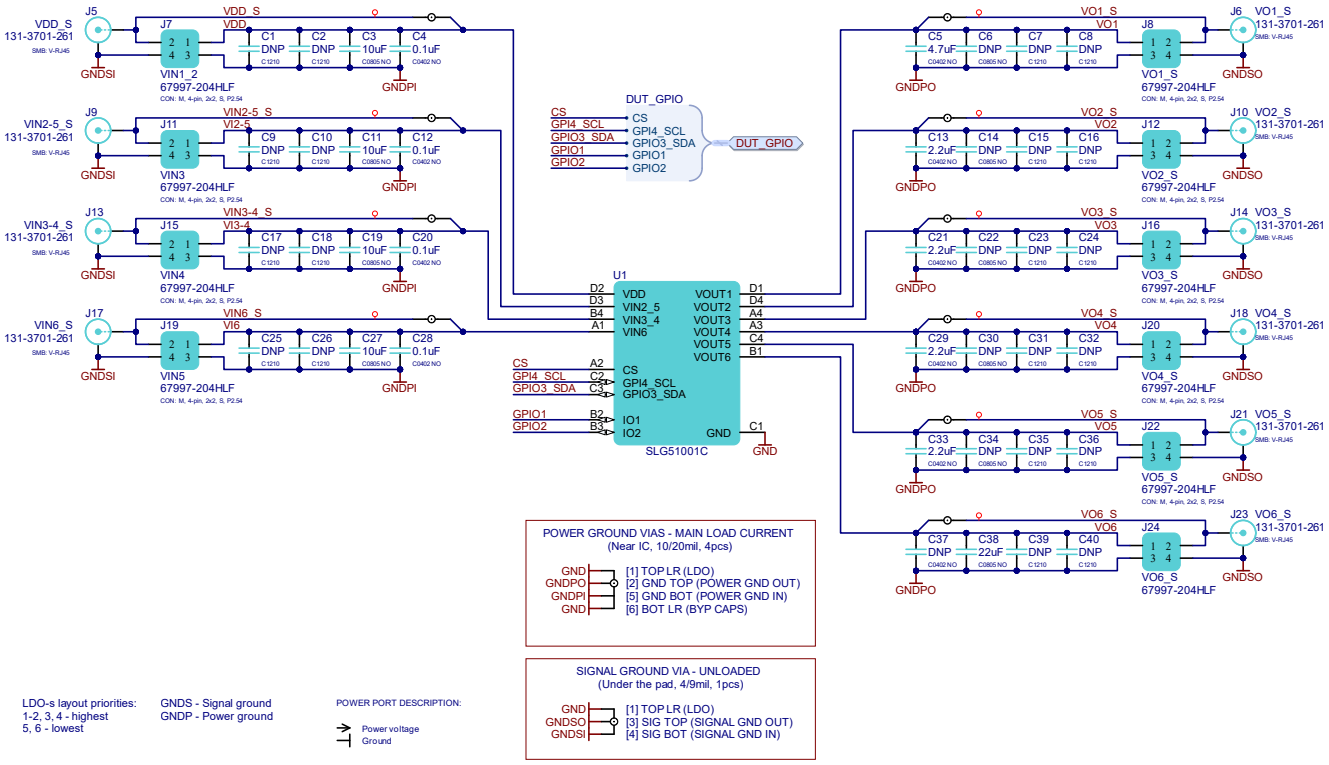

Figure 15. SLG51001C - Power Section Schematic

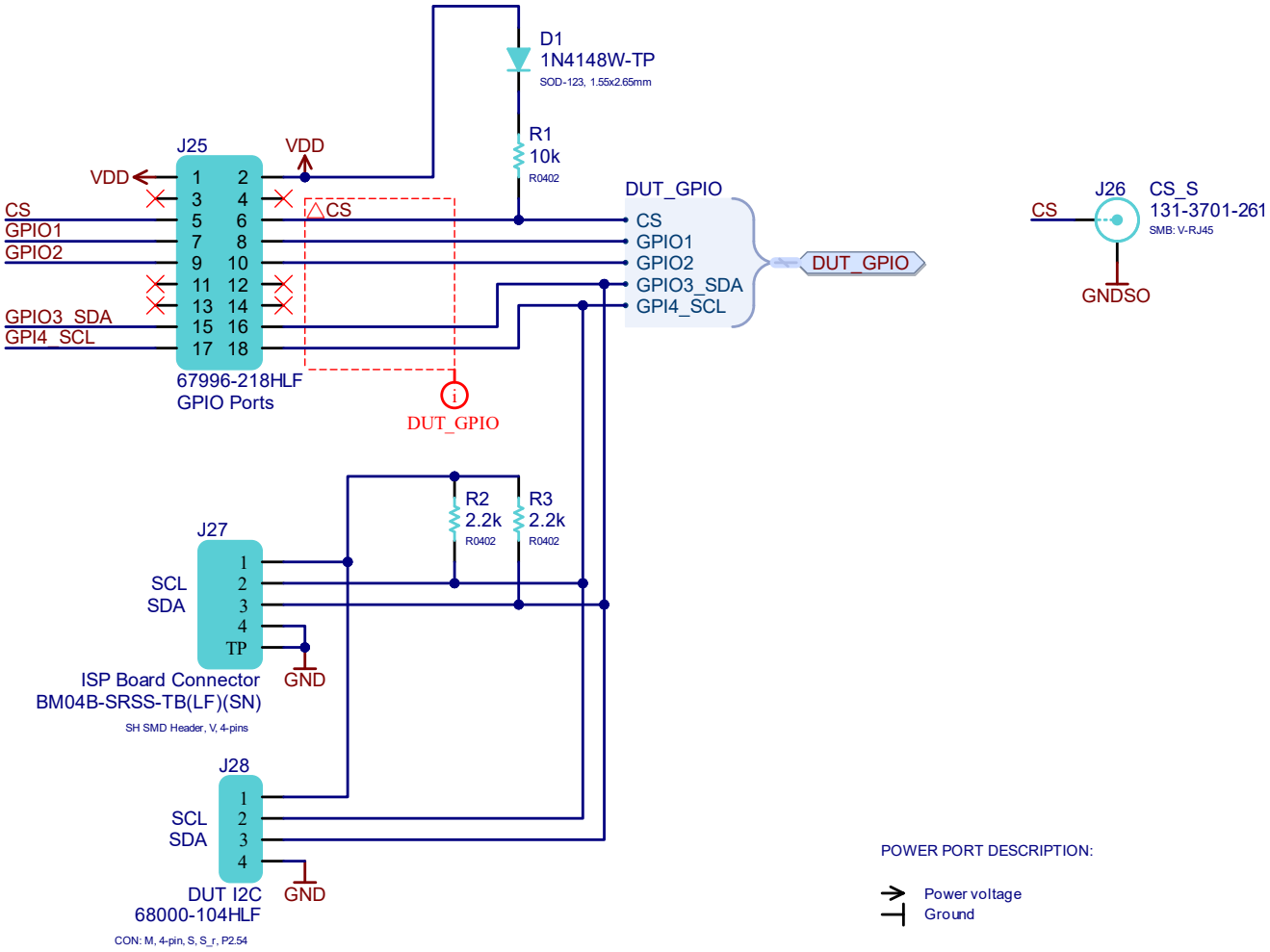

Figure 16. SLG51001C - GPIO Section Schematic

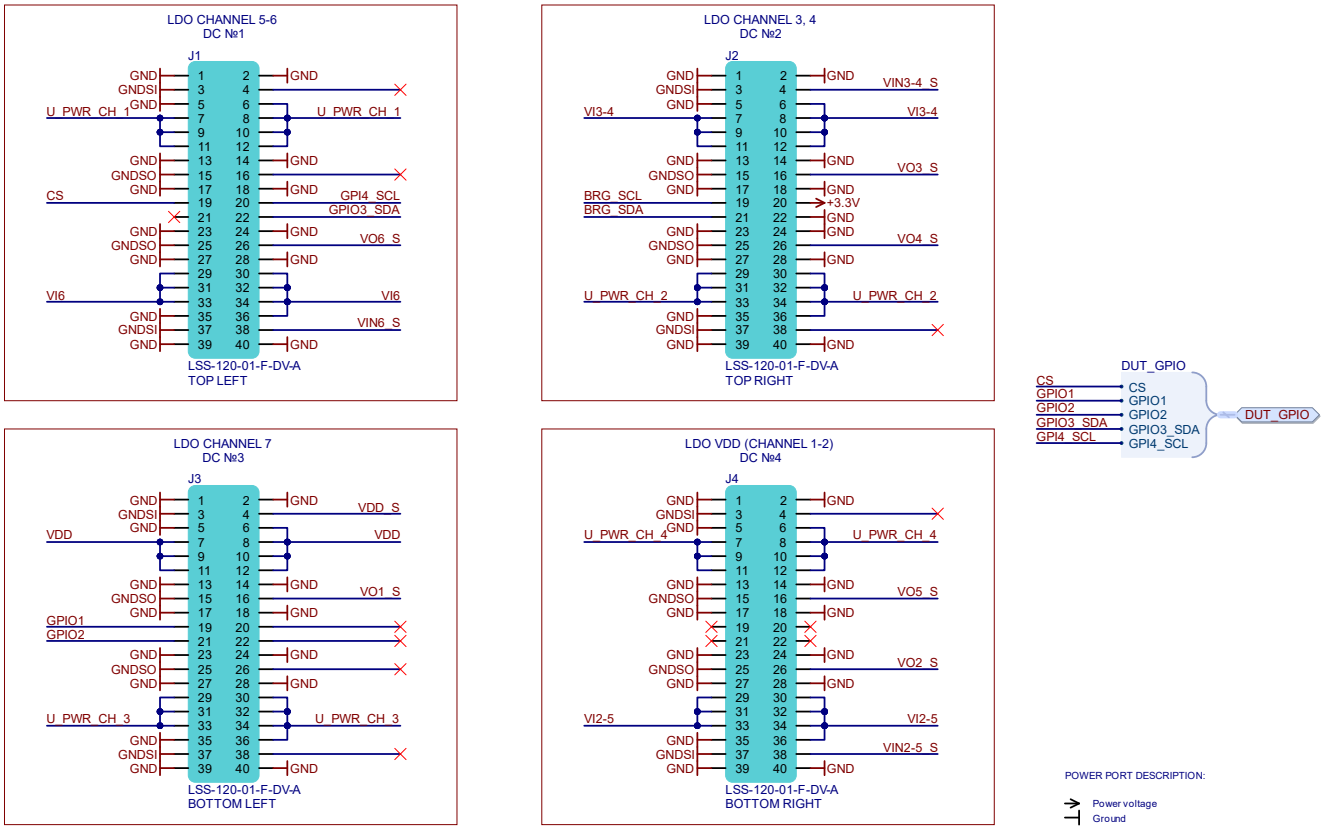

Figure 17. Connectors on the Bottom Layer for Connecting EVB to PGP_DM

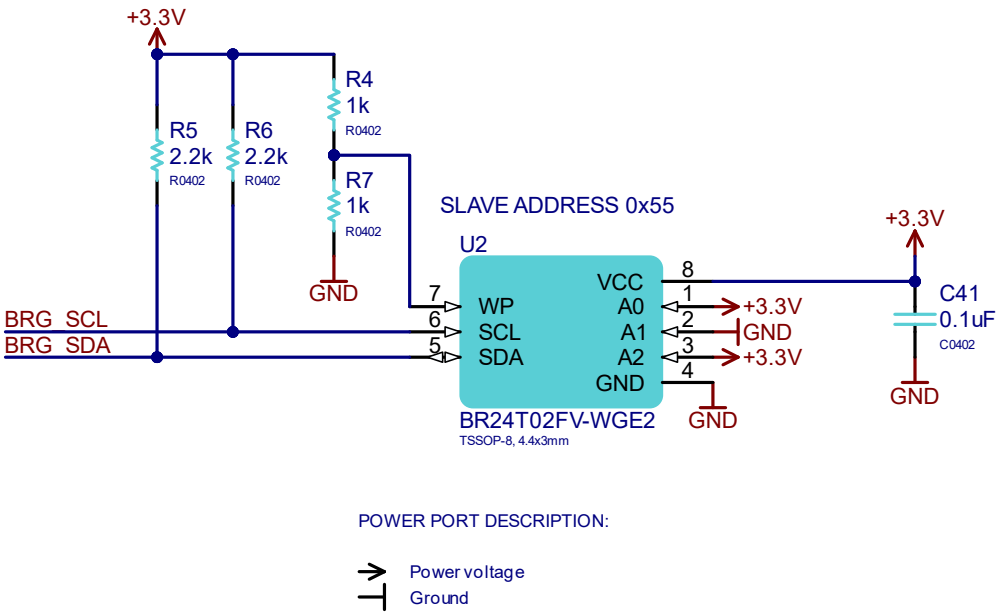

Figure 18. Board ID

A.2 BOM

#	Items	Package	Quantity per Development Board	Symbol
1	SJ61A6	Bumper: perforated hole D3.5 mm	4	BP1, BP2, BP3, BP4
2	10uF 16V X5R 0805	C0805 NO	4	C3, C11, C19, C27
3	0.1uF 16V X7R 0402	C0402 NO	5	C4, C12, C20, C28, C41
4	4.7uF 10V X5R 0402	C0402 NO	1	C5
5	2.2uF 35V X5R 0402	C0402 NO, C0402	4	C13, C21, C29, C33
6	22uF 16V X5R 0805	C0805 NO	1	C38
7	1N4148W-TP	SOD-123, 1.55x2.65mm	1	D1
8	LSS-120-01-F-DV-A	LSS-120-01-F-DV-A	4	J1, J2, J3, J4
9	131-3701-261	SMB: V-RJ45	11	J5, J6, J9, J10, J13, J14, J17, J18, J21, J23, J26
10	67997-204HLF	CON: M, 4-pin, 2x2, S, P2.54	10	J7, J8, J11, J12, J15, J16, J19, J20, J22, J24
11	67996-218HLF	CON: M, 18-pin, 9x2, P2.54	1	J25
12	BM04B-SRSS-TB(LF)(SN)	SH SMD Header, V, 4-pins	1	J27
13	68000-104HLF	CON: M, 4-pin, S, S_r, P2.54	1	J28
14	68000-102HLF	CON: M, 2-pin, S, S_r, P2.54	6	J29, J30, J31, J32, J33, J34
15	1k 0402	R0402	1	R7
16	SLG51001C	16-pin WLCSP: 1.675 mm x 1.675 mm x 0.465 mm, 0.4 mm pitch	1	U1
17	BR24T02FV-WGE2	TSSOP-8, 4.4 mm x 3 mm	1	U2

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