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RENESAS

Preliminary User's Manual

SolutionGear™-CPU-NU85ET

Evaluation Board

Document No. U16105EJ1V0UM00 (1st edition)
Date Published December 2002 N CP(K)

Printed in Japan

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
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PREFACE

Readers This manual is intended for user engineers who evaluate the “NU85E” or “NU85ET” CPU cores.

Purpose This manual is intended to give users an understanding of the hardware functions of SolutionGear-CPU-NU85ET.

Organization This manual consists of the following chapters.

- Overview
- Board Configuration
- Setting of Each Board
- Hardware Reference
- Pin Connection of μPD703193

How to Read This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	×××Z (Z suffixed to pin or signal name.)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary … ×××× or ××××B
	Decimal … ××××
	Hexadecimal … ××××H

Prefix of power of 2 (address space and memory capacity):

K (kilo) … $2^{10} = 1,024$

M (mega) … $2^{20} = 1,024^2$

G (giga) … $2^{30} = 1,024^3$

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- NU85E Hardware User's Manual (A14874E)
- NU85ET Hardware User's Manual (A15015E)
- V850E1 Architecture User's Manual (U14559E)
- Memory Controller NU85E, NU85ET User's Manual (A15019E)
- Instruction Cache, Data Cache NB85E, NB85ET User's Manual (A14247E)
- Instruction Cache, Data Cache NU85E, NU85ET User's Manual (A15241E)

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LIST OF TABLES (2/2)

CHAPTER 1 INTRODUCTION

SolutionGear-CPU-NU85ET is an evaluation board for the NEC Electronics RISC processor NB85ET (V850E core). This tool consists of the following two boards.

- AP-CPU-NU85ET: CPU board
- AP-GUBS-NU85ET: GBUS board

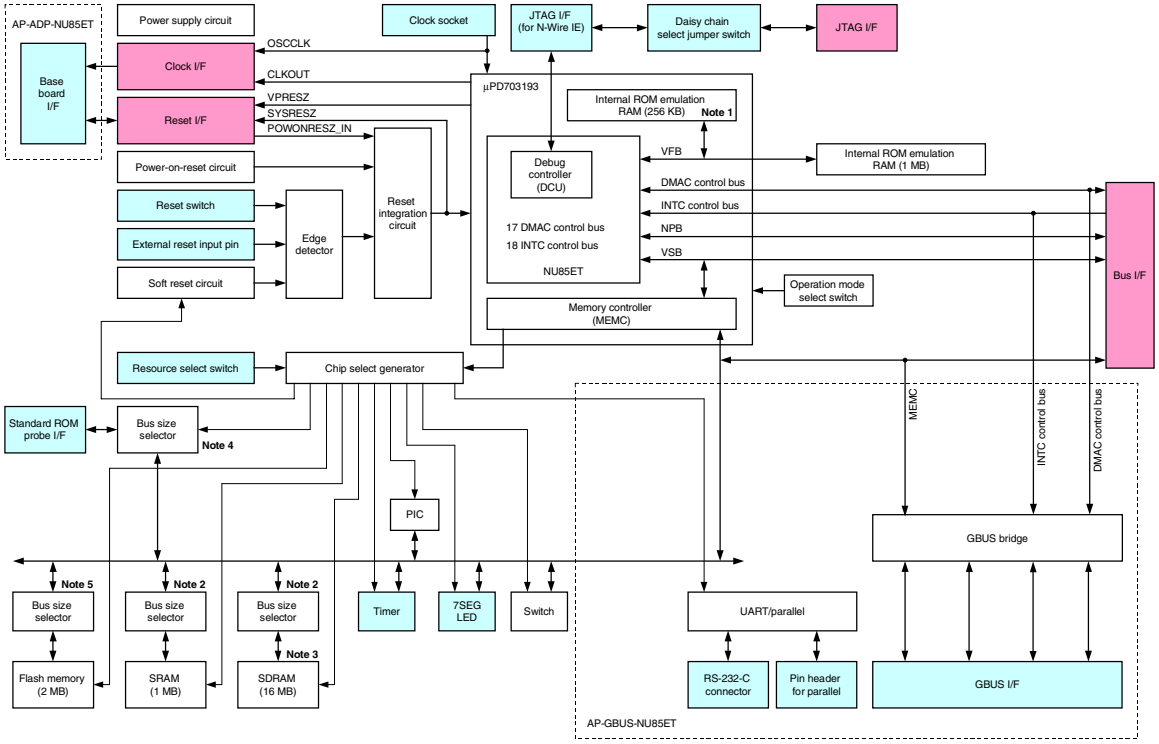
This evaluation board consists of the NU85E that operates at up to 85 MHz, memories, serial interfaces, and bus connectors for expansion. As memories, a high-speed SRAM and a large-capacity SDRAM are incorporated as standard. The SDRAM is controlled by the on-chip memory controller of the NB85E.

The functions of this evaluation board enable performance evaluation and demonstration of processors, and development of a simulator execution engine and the initial stage of an application program.

On this board, either of MULTI™ (Green Hills Software™, Inc.) or PARTNER (Midas) can be used as the source-level debugger for development. The monitor to be incorporated in ROM differs depending on the debugger used. The monitor specified by the user can be incorporated if the user purchases the debugger at the same time as this product. If the user did not purchase the debugger at the same time, purchase the monitor separately.

Figure 1-1 shows the block diagram of the CPU board.

Figure 1-1. Block Diagram of SolutionGear-CPU-NU85ET



Notes 1. In the interleave mode, the internal ROM emulation RAM (256 KB) can be used, but only half the capacity, i.e., 128 KB, can be used in the non-interleave mode. Select the interleave mode or non-interleave mode by using the RSZ register. Set SW3 to SW8 to "OFF" regardless of whether the interleave mode or non-interleave mode is selected.

2. If the bus mode selected by switches (SW2 to SW4) does not match the bus mode selected by the BSC and SCR4 registers, the operation is not performed correctly.

3. Only 8 MB can be used in the 16-bit bus mode (16 MB can be used in the 32-bit bus mode).

4. To use the ROM emulator, use one ROM probe in the 16-bit bus mode. Use two ROM probes in the 32-bit bus mode.

5. To write data to the flash memory, select the 16-bit bus mode by using the BSC register (to read the flash memory, the BSC register does not have to be set because the 16- or 32-bit bus mode is automatically identified). When the ROM probe is connected, the flash memory cannot be used because the probe is mapped to the same addresses as the flash memory.

Remarks 1. [blue]: Indicates the user interface or connector interface.

2. [red]: Indicates the signals of the user interface or connector interface connected to the CPU connectors (CN1 to CN5).

1.1 Features

- Equipped with evaluation chip (μPD703193) incorporating NU85ET
  - NU85ET and memory controller (MEMC: NT85E500, NT85E502) on-chip
  - Maximum operating frequency: 85 MHz (for the operating frequency of the NU85ET, refer to **NU85ET Hardware User's Manual (A15015E)**)
  - Internal ROM (ROM directly connected to NU85ET (connected to VFB)): 1 MB
  - Internal RAM (RAM directly connected to NU85ET (connected to VDB)): 60 KB
  - Instruction cache (NB85E213): 8 KB
  - Data cache (NB85E263): 8 KB

- Interfaces
  - GBUS interface
  - N-Wire in-circuit emulator interface (connector for debugging)
  - High-speed N-Wire in-circuit emulator interface (connector for high-speed debugging)
  - ROM emulator interface
- SRAM: 1 MB (connected to MEMC (NT85E500))
- Flash memory: 2 MB (connected to MEMC (NT85E500))
- SDRAM: 16 MB (connected to MEMC (NT85E502))
- Timer: μPD71054 $\times$ 1 (3 channels)
- RS-232-C interface $\times$ 2
- Parallel interface $\times$ 1

1.2 Basic Specifications

1.2.1 AP-CPU-NU85ET (CPU board)

Table 1-1. Specifications of AP-CPU-NU85ET (CPU Board)

Item		Description
CPU		μPD703193 (with NU85ET)
Operation clock	CPU clock	85 MHz
	Bus clock	85 MHz
Supply voltage	When CPU board is used alone	+5 V (3A)
	When CPU board and base board are connected	+5 V (3A) (+5 V is supplied from ATX power supply)
Memory	Flash memory	2 MB ((1 Mword × 16 bits) × 1)
	Internal ROM emulation RAM[Note]	1 MB ((128 Kwords × 32 bits) × 2)
	SRAM	1 MB ((256 Kwords × 16 bits) × 2)
	SDRAM	16 MB ((1 Mword × 16 bits × 4 banks) × 2)
I/O	Timer	μPD71054 (resolution: 723 ns at 1.38 MHz) (from NEC Electronics)
	I/O port	7SEG-LED × 4: Display/switch input
Interface	CPU board connector	Bus and control signals (CN1 to CN5)
	N-Wire interface	Connector for debugging (NWIRE2)
	High-speed N-Wire interface	Connector for high-speed debugging (NWIRE1)
	ROM emulator interface	Supports standard ROM probe (ROM_EMU1, ROM_EMU2)

Note An emulation memory that can be fetched in the same access time as the internal ROM is mapped and the program stored in the internal ROM can be executed without having to modify the addresses.

1.2.2 AP-GBUS-NU85ET (GBUS board)

Table 1-2. Specifications of AP-GBUS-NU85ET (GBUS Board)

Item		Description	
I/O	RS-232-C interface × 2	D-SUB 9-pin connector (RS232C1, RS232C2)	TL16PIR552 (from Texas Instruments)
	Parallel interface × 1	26-pin pin header (JH1)	
Interface	Connector for GBUS	GBUS bus and control signals (JBUS1)	
	Connector for CPU board	Bus and control signals (CN1 to CN5)	

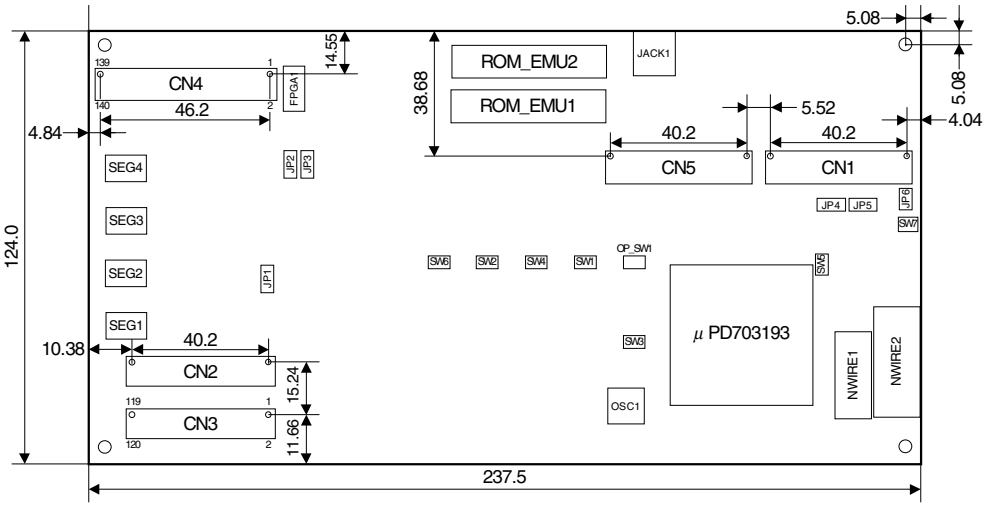
CHAPTER 2 BOARD CONFIGURATION

This chapter describes the parts of the boards.

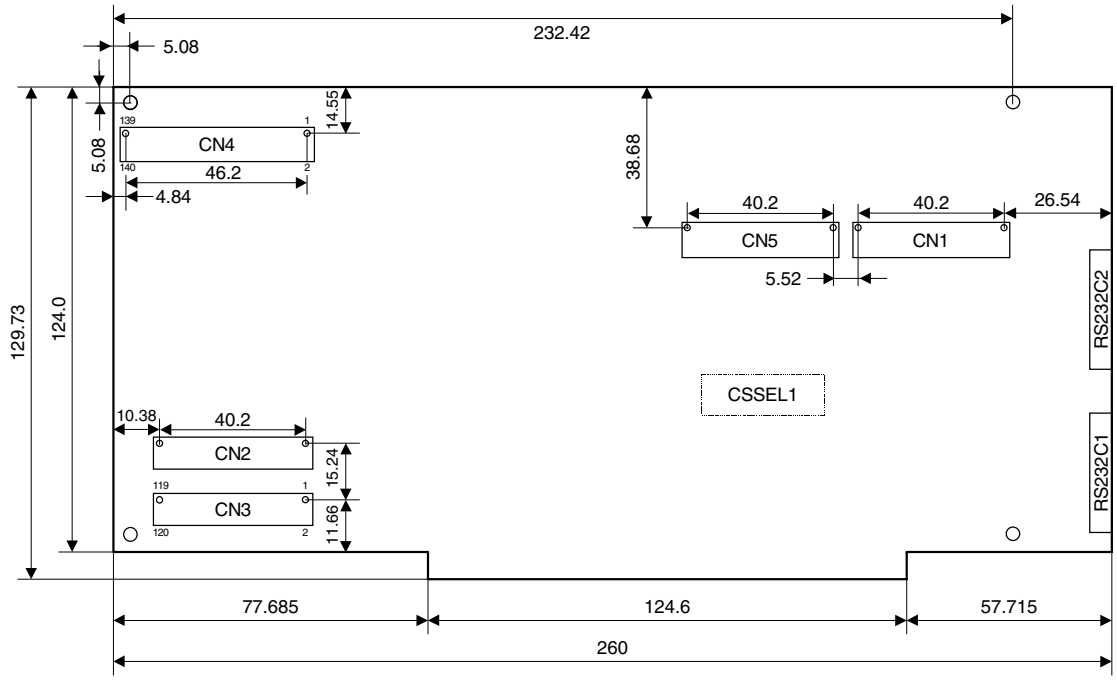
Figure 2-1 shows the component layout of the CPU board.

Figure 2-1. Component Layout (SolutionGear-CPU-NU85ET)

(1) AP-CPU-NU85ET (CPU board) (Top view)



(2) AP-GBUS-NU85ET (GBUS board) (Top view)



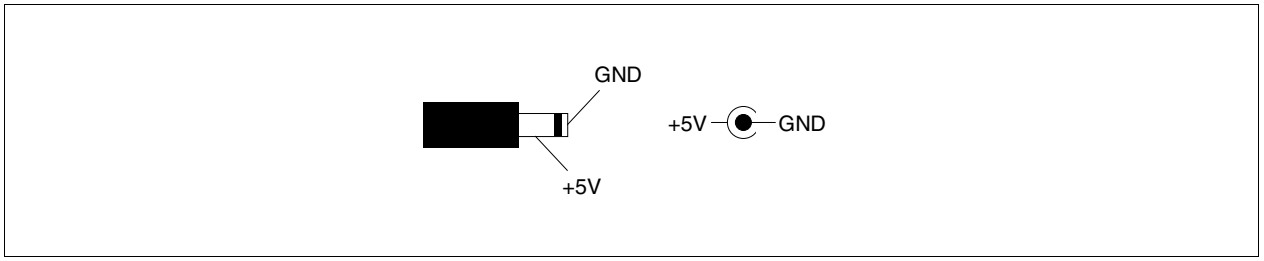
(Unit: mm)

2.1 Power Supply Connector (JACK1)

Supply the following power to JACK1:

- Voltage: +5 V
- Current: 3 A (max.)
- Adapter: Type A (ϕ5.5)
- Polarity: Refer to **Figure 2-2**.

Figure 2-2. Power Supply Connector (JACK1)



Caution When connecting SolutionGear-CPU-NU85ET to the motherboard, do not connect the power supply to JACK1 of the CPU board.

2.2 Switches

2.2.1 Switch 1 (SW1)

SW1 is a general-purpose input port. The setting status of SW1 can be read from the input port (refer to **5.5.1 SW1 (SW1 read port)**). Note, however, that when using a monitor ROM, the settings of SW1 have almost all been assigned. For the settings of the monitor ROM, refer to the manual of the monitor ROM. Note also that the monitor ROM operates only in 64M mode.

Table 2-1. Setting of SW1

No.	Signal Name	Factory-Set Condition	Function
1	BOUDRATE0	OFF	For future expansion (reserved)
2	BOUDRATE1	OFF	For future expansion (reserved)
3	TIMER0	OFF	For future expansion (reserved)
4	TIMER1	OFF	For future expansion (reserved)
5	Reserved	OFF	For future expansion (reserved)
6	Reserved	OFF	For future expansion (reserved)
7	Reserved	OFF	For future expansion (reserved)
8	7SEG	OFF	For future expansion (reserved)

Remark ON: 0, OFF: 1

2.2.2 Switch 2 (SW2)

SW2 is used to select the operation of the board.

The settings of this switch can be read from the input port (refer to **5.5.2 SW2 (SW2 read port)**).

Table 2-2. Setting of SW2 (1/2)

No.	Signal Name	Factory-Set Condition	Function
1	GBUSFLASHZ	OFF	Sets CS0 space. ON: Space to which GCS1 signal of GBUS is assigned is mapped OFF: Flash memory on the CPU board is mapped
2	Reserved	OFF	For future expansion (reserved)
3	Reserved	OFF	For future expansion (reserved)
4	BSIZE16Z	OFF	Sets the bus width on the SRAM and SDRAM hardware (the BSC and SCR4 registers must be set in accordance with this setting). ON: 16 bits OFF: 32 bits
5	NMI/INT0	OFF	For future expansion (reserved)
6	CACHE	OFF	Initializes the cache when monitor ROM is used. ON: All resources on board are initialized by CACHE OFF: All spaces are initialized by CACHE

Remark ON: 0, OFF: 1

Table 2-2. Setting of SW2 (2/2)

No.	Signal Name	Factory-Set Condition	Function
7	CACHEMODE0	OFF	Specifies the mode when SW2 to SW6 are ON (CACHE ON) while monitor ROM is used. ON: Writeback mode OFF: Write through mode
8	CACHEMODE1	OFF	Specifies the write allocation when SW2 to SW7 are ON (writeback mode) when ROM is used. ON: Write allocation enabled OFF: Write allocation disabled

Remark ON: 0, OFF: 1

2.2.3 Switch 3 (SW3)

SW3 is used to select the operation of the board.

Table 2-3. Setting of SW3

No.	Signal Name	Factory-Set Condition	Function
1	CKSEL0	OFF	Clock mode of CPU (See **Table 2-4**.)
2	CKSEL1	OFF	Clock mode of CPU (See **Table 2-4**.)
3	PWAIT0	ON	Fixed
4	PWAIT1	ON	Fixed
5	PWAIT2	ON	Fixed
6	BCLK0	OFF	Wait setting mode in accordance with operation clock of CPU
7	BCLK1	OFF	Wait setting mode in accordance with operation clock of CPU
8	ROMAA2	OFF	Sets interleave (cannot be read by I/O). However, the interleave mode is the setting when SW6-6 is “OFF” (internal ROM emulation: 1 MB). When SW6-6 is “ON” (internal ROM emulation: 256 KB), set SW3-8 to “OFF” (refer to **Notes 1** and **2** of **Figure 1-1 Block Diagram of SoluationGear-CPU-NU85ET**). ON: Normal mode (non-interleave mode) OFF: Interleave mode

Remark ON: 0, OFF: 1

Table 2-4 shows the setting of the CPU clock mode.

Table 2-4. Setting of CPU Clock Mode

CKSEL1	CKSEL0	Clock Mode	Input Clock	Internal System Clock
ON	ON	PLL mode (×1)	Oscillator (mounted in socket)	Frequency of oscillator × 1
ON	OFF	PLL mode (×2)	Oscillator (mounted in socket)	Frequency of oscillator × 2
OFF	ON	PLL mode (×4)	Oscillator (mounted in socket)	Frequency of oscillator × 4
OFF	OFF	External clock mode	Oscillator (mounted in socket)	Frequency of oscillator × 1

Remarks 1. ON: 0, OFF: 1

2. To use PLL, make setting so that the frequency of the internal system clock is 50 MHz or more.

2.2.4 Switch 4 (SW4)

SW4 is used to select the on-board memory.

Table 2-5. Setting of SW4

No.	Signal Name	Factory-Set Condition	Function
1	KILLIOZ	OFF	Selects whether on-board I/O is used (OFF if used).
2	KILLROMZ	OFF	Selects whether on-board flash memory is used (OFF if used).
3	KILLSRAMZ	OFF	Selects whether on-board SRAM is used (OFF if used).
4	KILLSDRAMZ	OFF	Selects whether on-board SDRAM is used (OFF if used)
5	Reserved	OFF	For future expansion (reserved)
6	Reserved	OFF	For future expansion (reserved)
7	Reserved	OFF	For future expansion (reserved)
8	Reserved	OFF	For future expansion (reserved)

Remark ON: 0, OFF: 1

2.2.5 Switch 5 (SW5)

SW5 is used to select the on-board interrupts.

Table 2-6. Setting of SW5

No.	Signal Name	Factory-Set Condition	Function
1	INT10	ON	ON: GINT01 → Input to INT10 OFF: INT10
2	INT11	ON	ON: GINT02 → Input to INT11 OFF: INT11
3	INT12	ON	ON: GINT03 → Input to INT12 OFF: INT12
4	INT13	ON	ON: TIC_OUT1[Note] → Input to INT13 OFF: INT13
5	INT0	OFF	ON: PIC0 output → Input to INT0 OFF: INT0
6	NMI0	ON	ON: ROM emulator interrupt → Input to NMI0 OFF: NMI0
7	NMI1	ON	ON: GINT00 → Input to NMI1 OFF: NMI1
8	NMI2	ON	ON: PIC0 output → Input to NMI2 OFF: NMI2

Note OUT1 pin of timer (μPD71054)

Remark ON: 0, OFF: 1

2.2.6 Switch 6 (SW6)

SW6 is used to set the operation mode of the μPD703193 and the VSB data bus size.

This switch is "1" when OFF and "0" when ON (refer to **B.1 Operation Modes** for details of the MODE5 to MODE0 pins). The factory-set conditions for shipment are as follows.

- Single-chip mode 0
- VSB data bus size: 32 bits

Table 2-7. Setting of SW6

No.	Signal Name	Factory-Set Condition	Function
1	MODE0	ON	Operation mode of CPU (for the setting, see **Table 2-8**.)
2	MODE1	ON	
3	MODE2	OFF	
4	MODE3	ON	
5	MODE4	OFF	Enables operation of memory controller (MEMC). ON: Disables operation of internal memory controller. OFF: Enables operation of internal memory controller.
6	MODE5	OFF	Selects internal ROM size and use of external VSB[Note]. ON: Internal ROM emulation (256 KB). External VSB can be used. OFF: Internal ROM emulation (1 MB). External VSB cannot be used.
7	IFIMAEN	OFF	Selects misalign operation. ON: Disables misalign operation. OFF: Enables misalign operation.
8	Reserved	OFF	For future expansion (reserved)

Note Be sure to set MODE5 to ON to use in the ROMless mode.

Remark ON: 0, OFF: 1

Table 2-8. Setting of CPU Operation Mode

MODE3	MODE2	MODE1	MODE0	CPU Operation Mode	VSB Data Bus Width
ON	ON	ON	ON	Single-chip mode 0 (64 MB mode) (ROM area is located from 0000000H)	16 bits
ON	ON	ON	OFF	Single-chip mode 1 (64 MB mode) (ROM area is located from 0100000H)	16 bits
ON	ON	OFF	ON	ROMless mode (64 MB mode)	16 bits
ON	OFF	ON	ON	Single-chip mode 0 (64 MB mode) (ROM area is located from 0000000H)	32 bits
ON	OFF	ON	OFF	Single-chip mode 1 (64 MB mode) (ROM area is located from 0100000H)	32 bits
ON	OFF	OFF	ON	ROMless mode (64 MB mode)	32 bits
OFF	ON	OFF	ON	ROMless mode (256 MB mode)	16 bits
OFF	OFF	OFF	ON	ROMless mode (256 MB mode)	32 bits
Other than above				Setting prohibited	

Remark ON: 0, OFF: 1

2.2.7 Reset switch (SW7)

SW7 is used to reset the entire board. When this switch is pressed, all the circuits, including the μPD703193, are reset.

Caution When the N-Wire in-circuit emulator is used, resetting the μPD703193 may be masked by the debugger during a brake. In this case, the system will be completely reset, so execute the reset command on the debugger after pressing the reset switch.

2.2.8 Option switch 1 (OP_SW1)

The setting of OP_SW1 can be read from the I/O space (for details, refer to **5.5 I/O**). When the switch is OFF, logic "1" is read; when it is ON, logic "0" is read.

Table 2-9. Setting of OP_SW1

No.	Signal Name	Factory-Set Condition	Function
1	OPTION0	OFF	For user
2	OPTION1	OFF	For user
3	OPTION2	OFF	For user
4	OPTION3	OFF	For user
5	OPTION4	OFF	For user
6	OPTION5	OFF	For user
7	OPTION6	OFF	For user
8	OPTION7	OFF	For user

Remark ON: Logic "0", OFF: Logic "1"

2.3 Jumpers 1 to 5 (JP1 to JP5) and CSSEL

The following table shows the functions (switching) of JP1 to JP5.

Table 2-10. Setting of JP1 to JP5 and CSSEL

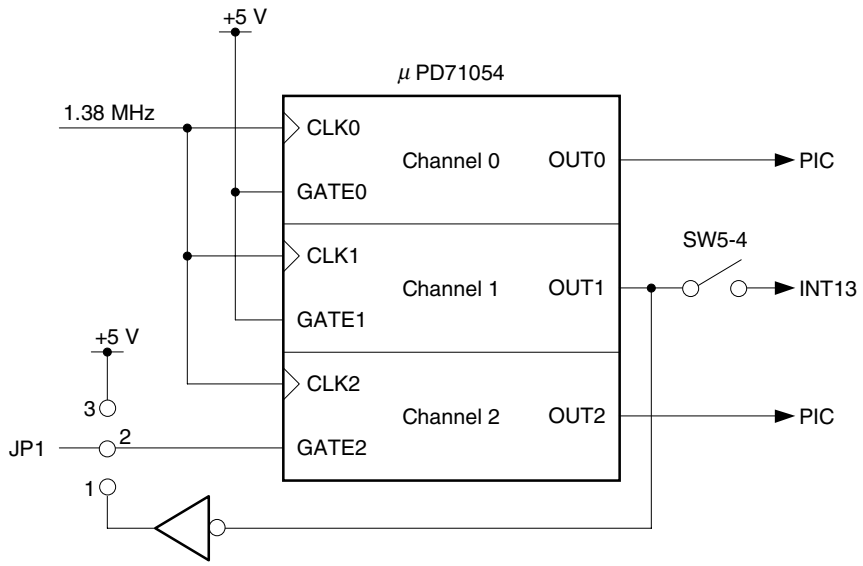
Jumper	Factory-Set Condition	When 1 and 2 Are Shorted	When 2 and 3 Are Shorted
JP1	2-3	TM2 (cascade operation mode)	TM2 (single operation mode)
JP2	2-3	–	During normal use (default)
JP3	2-3	DIP switch test mode	During normal use (default)
JP4	1-2	Connector for debugging (fixed)	Setting prohibited
JP5	1-2	Connector for high-speed debugging (fixed)	Setting prohibited
CSSEL[Note]	1-2	GBUS space setting (fixed)	Setting prohibited

Note CSSEL is at GBUS port (AP-GBUS-NU85ET).

2.3.1 JP1 (TIC operation mode selection) (Factory setting: 2-3 shorted)

JP1 is used to select whether channel 2 of TIC is used alone or connected to channel 1 in cascade.

Figure 2-3. Connection of Each Channel of TIC



Remark Example of use
Channel 0: Mode 2 (rate generator)
Channel 1: Mode 2 (rate generator)
Channel 2: Mode 0 (down counter)

2.3.2 JP2 (Factory setting: 2-3 shorted)

JP2 is a jumper reserved for future expansion. Use this jumper under the factory-set conditions for shipment (default).

2.3.3 JP3 (DIP switch test mode) (Factory setting: 2-3 shorted)

JP3 is a jumper used to execute DIP switch test mode.

If the DIP switch test mode is executed, the setting of each switch can be indicated by 7SEG_LED (SEG1) and CS_LED (D2 to D9) every 3 seconds to check the contact of the switch.

Caution When changing JP3 (DIP switch test mode), be sure to turn off the power. In the DIP switch test mode, the entire board is reset.

Table 2-11. Indication by Each LED in DIP Switch Test Mode

Indication of 7SEG_LED (SEG1)	Indication of CS_LED							
	CS7 (D9)	CS6 (D8)	CS5 (D7)	CS4 (D6)	CS3 (D5)	CS2 (D4)	CS1 (D3)	CS0 (D2)
–	Lit	Lit	Lit	Lit	Lit	Lit	Lit	Lit
1	SW1-8	SW1-7	SW1-6	SW1-5	SW1-4	SW1-3	SW1-2	SW1-1
2	SW2-8	SW2-7	SW2-6	SW2-5	SW2-4	SW2-3	SW2-2	SW2-1
3	Lit	SW3-7	SW3-6	SW3-5	SW3-4	SW3-3	SW3-2	SW3-1
4	SW4-8	SW4-7	SW4-6	SW4-5	SW4-4	SW4-3	SW4-2	SW4-1
6	SW6-8	SW6-7	SW6-6	SW6-5	SW6-4	SW6-3	SW6-2	SW6-1
0	OP_SW1-8	OP_SW1-7	OP_SW1-6	OP_SW1-5	OP_SW1-4	OP_SW1-3	OP_SW1-2	OP_SW1-1
–	Lit	Lit	Lit	Lit	Lit	Lit	Lit	Lit

Caution SW3-8 and SW5 cannot be checked in the DIP switch test mode.

Remark The indicator lights when each switch is ON, and remains dark when the switch is OFF.

2.3.4 JP4 (Factory setting: 1-2 shorted)

JP4 is a jumper for using the N-Wire in-circuit emulator.

Use this with the factory setting unchanged (default status).

2.3.5 JP5 (Factory setting: 1-2 shorted)

JP5 is a jumper for using the high-speed N-Wire in-circuit emulator.

Use this with the factory setting unchanged (default status).

2.3.6 CSSEL (Factory setting: 1-2 shorted)

CSSEL is a jumper for GBUS space expansion.

Use this with the factory setting unchanged (default status).

2.4 LEDs

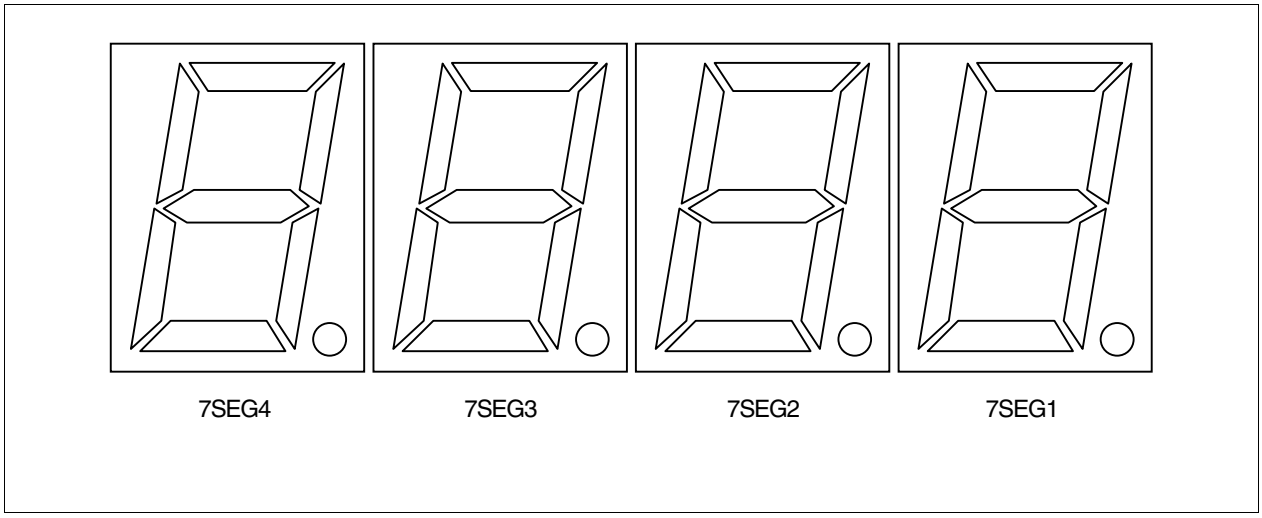
2.4.1 POWER LED (D1)

The POWER LED (D1) lights when power is being supplied.

2.4.2 7SEG-LED

This LED consists of four LEDs, 7SEG1 to 7SEG4. Each LED can be used freely by the user program.

Figure 2-4. 7SEG-LED



2.4.3 CS_LED (D2 to D9)

CS_LED lights when the CS space of the memory controller (NT85E500) is being accessed (RDZ, WRZ3 to WRZ0). However, it does not light when the SDRAM space, NPB, or VSB is being accessed.

Table 2-12. Contents of CS_LED

CS_LED		Description
CS0_LED	D2	When CS0 space is being accessed
CS1_LED	D3	When CS1 space is being accessed
CS2_LED	D4	When CS2 space is being accessed
CS3_LED	D5	When CS3 space is being accessed
CS4_LED	D6	When CS4 space is being accessed
CS5_LED	D7	When CS5 space is being accessed
CS6_LED	D8	When CS6 space is being accessed
CS7_LED	D9	When CS7 space is being accessed

2.4.4 GOOD_LED (D11)

GOOD_LED indicates that data has been correctly loaded to the FPGA that controls the CPU board. It lights when loading data to FPGA has been completed.

2.5 Clock Socket (OSC1)

Mount an oscillator (OSC) to supply the clock to the μPD703193 in the OSC1 socket.

Use a DIP 8-pin type OSC with an output of 3.3 V (half type).

An oscillator (OSC) of 85 MHz is mounted on the CPU board of this product.

2.6 ROM Emulator Connection Pins (TP3 to TP5)

The ROM emulator connection pins (TP3 and TP4) are used to connect a ROM emulator and input the following control signals. However, these pins may not be used depending on the type of the ROM emulator.

Table 2-13. Setting of ROM Emulator Connection Pins

Pin Name	Signal Name	I/O	Function
TP4	ROM_RESET	Input	Inputs a reset request signal from the ROM emulator. The μPD703193 is reset when a low level is input to this pin. A 1 kΩ pull-up resistor is connected to +5 V.
TP3[Note]	ROM_NMI	Input	Inputs an NMI request signal from the ROM emulator. The NMI request is issued to the μPD703193 when a low level is input to this pin (see **4.2 Interrupt List**). A 1 kΩ pull-up resistor is connected to +5 V.
TP5	GND	–	Connect this pin to the GND pin of the ROM emulator.

Note To use TP3, set SW5-6 (NMI0) to ON.

2.7 ROM Emulator Connectors (ROM_EMU1 and ROM_EMU2)

These connectors are used to connect a 16-bit ROM probe.
ROM_EMU1 is the lower 16 bits, and ROM_EMU2 is the higher 16 bits.

(1) To emulate ROM with 16-bit bus

Connect the ROM probe to ROM_EMU1.

(2) To emulate ROM with 32-bit bus

Connect the lower side of the ROM probe to ROM_EMU1, and the higher side to ROM_EMU2.

Figure 2-5 shows the pin configuration of the ROM emulator connectors (ROM_EMU1 and ROM_EMU2).

Figure 2-5. ROM Emulator Connectors (ROM_EMU1 and ROM_EMU2)

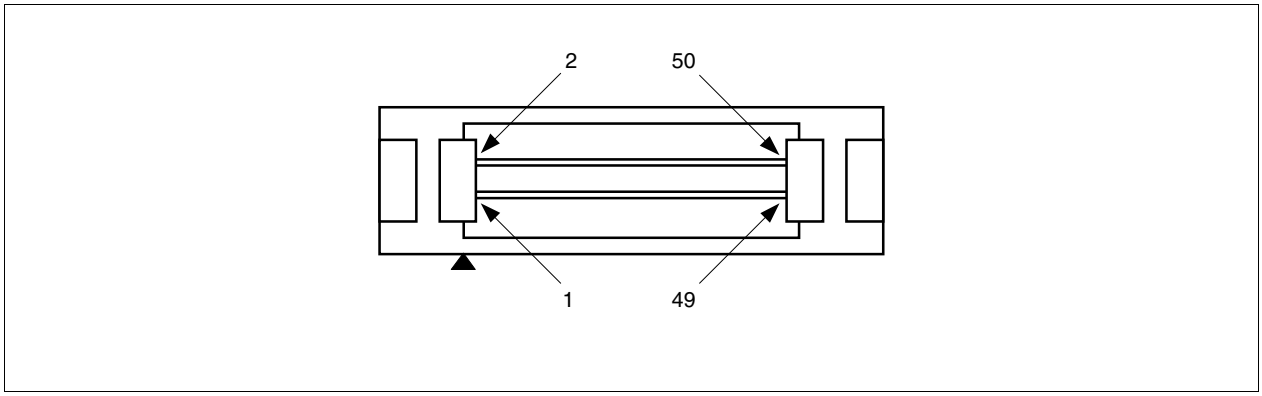


Table 2-14 shows the signals of the pins of the ROM emulator connector ROM_EMU1, and Table 2-15 shows those of ROM_EMU2.

Table 2-14. Signals of Pins of ROM Emulator Connector (ROM_EMU1)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	A2 (A1)
3	A3 (A2)	4	A4 (A3)
5	A5 (A4)	6	A6 (A5)
7	A7 (A6)	8	A8 (A7)
9	A9 (A8)	10	A10 (A9)
11	A11 (A10)	12	A12 (A11)
13	A13 (A12)	14	A14 (A13)
15	A15 (A14)	16	A16 (A15)
17	A17 (A16)	18	A18 (A17)
19	A19 (A18)	20	A20 (A19)
21	A21 (A20)	22	GND
23	GND	24	GND
25	Pulled up to 3.3 V via 10 kΩ resistor	26	INHZ
27	Pulled up to 3.3 V via 10 kΩ resistor	28	GND
29	CEZ	30	GND
31	OEZ	32	PSENSE (3.3 V connection)
33	D0	34	D1
35	D2	36	D3
37	D4	38	D5
39	D6	40	D7
41	D8	42	D9
43	D10	44	D11
45	D12	46	D13
47	D14	48	D15
49	GND	50	GND

Remark The signal names in the parentheses of pin numbers 2 to 21 are for when ROM_EMU1 only is connected using one ROM probe.

Table 2-15. Signals of Pins of ROM Emulator Connector (ROM_EMU2)

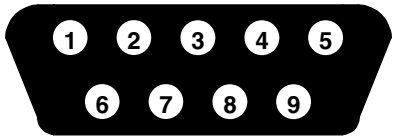
Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	A2
3	A3	4	A4
5	A5	6	A6
7	A7	8	A8
9	A9	10	A10
11	A11	12	A12
13	A13	14	A14
15	A15	16	A16
17	A17	18	A18
19	A19	20	A20
21	A21	22	GND
23	GND	24	GND
25	Pulled up to 3.3 V via 10 kΩ resistor	26	INHZ
27	Pulled up to 3.3 V via 10 kΩ resistor	28	GND
29	CEZ	30	GND
31	OEZ	32	PSENSE (3.3 V connection)
33	D16	34	D17
35	D18	36	D19
37	D20	38	D21
39	D22	40	D23
41	D24	42	D25
43	D26	44	D27
45	D28	46	D29
47	D30	48	D31
49	GND	50	GND

2.8 Serial Connectors (RS232C_1 and RS232C_2)

The RS-232-C connectors are connectors for the RS-232-C interface that is controlled by the on-board RS-232-C connector (TL16PIR552).

These connectors are the common D-SUB 9-pin connectors (male) used in PC/AT-compatible machines. The pin numbers and signal names are shown in the figure below.

Figure 2-6. RS-232-C Connectors (RS232C_1 and RS232C_2)



Pin No.	Signal Name	I/O	Pin No. of Host When Host Is Connected[Note]	
			D-SUB 9-pin	D-SUB 25-pin
1	DCD	Input	–	–
2	RxD (RD)	Input	3	2
3	TxD (SD)	Output	2	3
4	DTR (DR)	Output	1, 6	6, 8
5	GND	–	5	7
6	DSR (ER)	Input	4	20
7	RTS (RS)	Output	8	5
8	CTS (CS)	Input	7	4
9	RI	Input	–	–

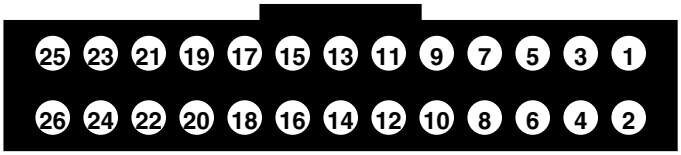
Note This table shows the pin numbers and signal names when a D-SUB 9-pin connector or a D-SUB 25-pin connector is used on the host side (when a general cross cable is used).

2.9 Parallel Connector (JH1)

The parallel connector is a connector for the parallel interface that is controlled by the on-board parallel controller (TL16PIR552).

This connector is a 26-pin header type with a 2.54 mm pitch. Its pin numbers and signal names are shown in the figure below.

Figure 2-7. Parallel Connector (JH1)



Pin No.	Signal Name	Pin No.	Signal Name
1	STB	2	AUTO_FD
3	D0	4	ERROR
5	D1	6	INIT
7	D2	8	SELECT_IN
9	D3	10	GND
11	D4	12	GND
13	D5	14	GND
15	D6	16	GND
17	D7	18	GND
19	ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SELECT	26	NC

2.10 Connectors for Debugging (NWIRE1 and NWIRE2)

The connectors for debugging (NWIRE1 and NWIRE2) are used to connect a debugging tool that uses the debugging functions of the NU85ET.

Table 2-16 shows the pins and signal names of the connector for debugging (NWIRE1), and Table 2-17 shows those of the connector for high-speed debugging (NWIRE2).

Table 2-16. Pins and Signals of Connector for Debugging (NWIRE1)

Pin No.	Signal Name	Pin No.	Signal Name
A1	TRCCLK	B1	GND
A2	TRCDATA0	B2	GND
A3	TRCDATA1	B3	GND
A4	TRCDATA2	B4	GND
A5	TRCDATA3	B5	GND
A6	TRCEND	B6	GND
A7	DDI	B7	GND
A8	DCK	B8	GND
A9	DMS	B9	GND
A10	DDO	B10	GND
A11	DRSTZ	B11	EVTTRG
A12	DBINT	B12	NC
A13	NC	B13	+3.3 V

Table 2-17. Pins and Signals of Connector for High-Speed Debugging (NWIRE2)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	20	TRCCE
2	GND	21	TRCDATA0
3	DCK	22	TRCDATA8
4	+3.3 V	23	TRCDATA1
5	DMS	24	TRCDATA9
6	DRSTZ	25	TRCDATA2
7	DDI	26	TRCDATA10
8	PORT0_OUT (DBINT)	27	TRCDATA3
9	DDO	28	TRCDATA11
10	PORT1_OUT	29	TRCDATA4
11	NC	30	TRCDATA12
12	PORT2_OUT	31	TRCDATA5
13	NC	32	TRCDATA13
14	PORT0_IN (EVTTRG)	33	TRCDATA6
15	NC	34	TRCDATA14
16	PORT1_IN	35	TRCDATA7
17	TRCCLK	36	TRCDATA15
18	PORT2_IN	37	GND
19	TRCEND	38	GND

2.11 CPU Connectors 1 to 5 (CN1 to CN5)

Tables 2-18 to 2-22 show details of the CPU connectors. The meanings of the symbols used in these tables are as follows.

- CPU connector: Number of CPU connector (CN1 to CN5)
- I/O: I/O direction when viewed from the CPU board (I: Input, O: Output)

Table 2-18. CPU Connector 1 (CN1) (1/4)

CPU Connector	Signal Name	I/O	Remark
CN1-001	GND	–	–
CN1-002	GND	–	–
CN1-003	GND	–	–
CN1-004	GND	–	–
CN1-005	DMARQ0	Input	47 kΩ pull-down
CN1-006	DMARQ1	Input	47 kΩ pull-down
CN1-007	DMARQ2	Input	47 kΩ pull-down
CN1-008	DMARQ3	Input	47 kΩ pull-down
CN1-009	DMTCO0	Output	–
CN1-010	DMTCO1	Output	–
CN1-011	DMTCO2	Output	–
CN1-012	DMTCO3	Output	–
CN1-013	GND	–	–
CN1-014	GND	–	–
CN1-015	DMACTV0	Output	–
CN1-016	DMACTV1	Output	–
CN1-017	DMACTV2	Output	–
CN1-018	DMACTV3	Output	–
CN1-019	IDMASTP	Input	47 kΩ pull-down
CN1-020	VPD15	I/O	47 kΩ pull-down
CN1-021	VPD14	I/O	47 kΩ pull-down
CN1-022	VPD13	I/O	47 kΩ pull-down
CN1-023	GND	–	–
CN1-024	GND	–	–
CN1-025	VPD12	I/O	47 kΩ pull-down
CN1-026	VPD11	I/O	47 kΩ pull-down
CN1-027	VPD10	I/O	47 kΩ pull-down
CN1-028	VPD09	I/O	47 kΩ pull-down
CN1-029	VPD08	I/O	47 kΩ pull-down
CN1-030	VPD07	I/O	47 kΩ pull-down
CN1-031	VPD06	I/O	47 kΩ pull-down

Table 2-18. CPU Connector 1 (CN1) (2/4)

CPU Connector	Signal Name	I/O	Remark
CN1-032	VPD05	I/O	47 kΩ pull-down
CN1-033	GND	–	–
CN1-034	GND	–	–
CN1-035	VPD04	I/O	47 kΩ pull-down
CN1-036	VPD03	I/O	47 kΩ pull-down
CN1-037	VPD02	I/O	47 kΩ pull-down
CN1-038	VPD01	I/O	47 kΩ pull-down
CN1-039	VPD00	I/O	47 kΩ pull-down
CN1-040	VPA13	Output	–
CN1-041	VPA12	Output	–
CN1-042	VPA11	Output	–
CN1-043	GND	–	–
CN1-044	GND	–	–
CN1-045	VPA10	Output	–
CN1-046	VPA09	Output	–
CN1-047	VPA08	Output	–
CN1-048	VPA07	Output	–
CN1-049	VPA06	Output	–
CN1-050	VPA05	Output	–
CN1-051	VPA04	Output	–
CN1-052	VPA03	Output	–
CN1-053	GND	–	–
CN1-054	GND	–	–
CN1-055	VPA02	Output	–
CN1-056	VPA01	Output	–
CN1-057	VPA00	Output	–
CN1-058	VPWRITE	Output	–
CN1-059	VPUBENZ	Output	–
CN1-060	VPSTB	Output	–
CN1-061	VPRETR	Input	47 kΩ pull-down
CN1-062	VPLOCK	Output	–
CN1-063	VPDACT	Input	10 kΩ pull-up
CN1-064	GBUSFLASH	Output	Reserved (leave open)
CN1-065	GND	–	–
CN1-066	GND	–	–
CN1-067	GINTO0	Input	Reserved (leave open)
CN1-068	GINTO1	Input	Reserved (leave open)
CN1-069	GINTO2	Input	Reserved (leave open)

Table 2-18. CPU Connector 1 (CN1) (3/4)

CPU Connector	Signal Name	I/O	Remark
CN1-070	GINTO3	Input	Reserved (leave open)
CN1-071	GINTI0	Output	Reserved (leave open)
CN1-072	GINTI1	Output	Reserved (leave open)
CN1-073	MCONNECT	Input	Reserved (leave open)
CN1-074	GCONNECT	Input	Reserved (leave open)
CN1-075	VPRESZ	Output	–
CN1-076	SYSRESZ	Output	Power-on reset (low level is valid)
CN1-077	SYSRES	Output	Power-on reset (high level is valid)
CN1-078	POWONREZ_IN	Input	Power-on reset (low level is valid) 10 kΩ pull-up (leave open when not used)
CN1-079	GND	–	–
CN1-080	GND	–	–
CN1-081	DCK	Output	Debugger output
CN1-082	DDI	Output	Debugger output
CN1-083	RMODE	Output	Debugger output
CN1-084	DDO	Input	Debugger input (leave open when not used)
CN1-085	DRSTZ	Output	Debugger output
CN1-086	DMS	Output	Debugger output
CN1-087	EVTTRG	Output	μPD703193 output
CN1-088	DBINT	Output	Debugger output
CN1-089	5 V	–	Supplying voltage from an external source is prohibited when the adapter is used.
CN1-090	5 V	–	
CN1-091	5 V	–	
CN1-092	5 V	–	
CN1-093	5 V	–	
CN1-094	5 V	–	
CN1-095	5 V	–	
CN1-096	5 V	–	
CN1-097	5 V	–	
CN1-098	5 V	–	
CN1-099	5 V	–	
CN1-100	5 V	–	
CN1-101	5 V	–	
CN1-102	5 V	–	
CN1-103	5 V	–	
CN1-104	5 V	–	
CN1-105	5 V	–	
CN1-106	5 V	–	

Table 2-18. CPU Connector 1 (CN1) (4/4)

CPU Connector	Signal Name	I/O	Remark
CN1-107	5 V	–	Supplying voltage from an external source is prohibited when the adapter is used.
CN1-108	5 V	–	
CN1-109	5 V	–	
CN1-110	5 V	–	
CN1-111	5 V	–	
CN1-112	5 V	–	
CN1-113	5 V	–	
CN1-114	5 V	–	
CN1-115	5 V	–	
CN1-116	5 V	–	
CN1-117	5 V	–	
CN1-118	5 V	–	
CN1-119	5 V	–	
CN1-120	5 V	–	

Table 2-19. CPU Connector 2 (CN2) (1/4)

CPU Connector	Signal Name	I/O	Remark
CN2-001	GND	–	–
CN2-002	GND	–	–
CN2-003	GND	–	–
CN2-004	GND	–	–
CN2-005	VBDI00	Input	47 kΩ pull-down
CN2-006	VBDI01	Input	47 kΩ pull-down
CN2-007	VBDI02	Input	47 kΩ pull-down
CN2-008	VBDI03	Input	47 kΩ pull-down
CN2-009	VBDI04	Input	47 kΩ pull-down
CN2-010	VBDI05	Input	47 kΩ pull-down
CN2-011	VBDI06	Input	47 kΩ pull-down
CN2-012	VBDI07	Input	47 kΩ pull-down
CN2-013	GND	–	–
CN2-014	GND	–	–
CN2-015	VBDI08	Input	47 kΩ pull-down
CN2-016	VBDI09	Input	47 kΩ pull-down
CN2-017	VBDI10	Input	47 kΩ pull-down
CN2-018	VBDI11	Input	47 kΩ pull-down
CN2-019	VBDI12	Input	47 kΩ pull-down
CN2-020	VBDI13	Input	47 kΩ pull-down
CN2-021	VBDI14	Input	47 kΩ pull-down
CN2-022	VBDI15	Input	47 kΩ pull-down
CN2-023	GND	–	–
CN2-024	GND	–	–
CN2-025	VBDI16	Input	47 kΩ pull-down
CN2-026	VBDI17	Input	47 kΩ pull-down
CN2-027	VBDI18	Input	47 kΩ pull-down
CN2-028	VBDI19	Input	47 kΩ pull-down
CN2-029	VBDI20	Input	47 kΩ pull-down
CN2-030	VBDI21	Input	47 kΩ pull-down
CN2-031	VBDI22	Input	47 kΩ pull-down
CN2-032	VBDI23	Input	47 kΩ pull-down
CN2-033	GND	–	–
CN2-034	GND	–	–
CN2-035	VBDI24	Input	47 kΩ pull-down
CN2-036	VBDI25	Input	47 kΩ pull-down
CN2-037	VBDI26	Input	47 kΩ pull-down
CN2-038	VBDI27	Input	47 kΩ pull-down

Table 2-19. CPU Connector 2 (CN2) (2/4)

CPU Connector	Signal Name	I/O	Remark
CN2-039	VBDI28	Input	47 kΩ pull-down
CN2-040	VBDI29	Input	47 kΩ pull-down
CN2-041	VBDI30	Input	47 kΩ pull-down
CN2-042	VBDI31	Input	47 kΩ pull-down
CN2-043	GND	–	–
CN2-044	GND	–	–
CN2-045	VMBENZ0	Output	100 kΩ pull-down when VSB is not used
CN2-046	VMBENZ1	Output	100 kΩ pull-down when VSB is not used
CN2-047	VMBENZ2	Output	100 kΩ pull-down when VSB is not used
CN2-048	VMBENZ3	Output	100 kΩ pull-down when VSB is not used
CN2-049	VMSTZ	Output	100 kΩ pull-down when VSB is not used
CN2-050	VMTTYP0	Output	100 kΩ pull-down when VSB is not used
CN2-051	VMTTYP1	Output	100 kΩ pull-down when VSB is not used
CN2-052	VMA00	Output	100 kΩ pull-down when VSB is not used
CN2-053	GND	–	–
CN2-054	GND	–	–
CN2-055	VMA01	Output	100 kΩ pull-down when VSB is not used
CN2-056	VMA02	Output	100 kΩ pull-down when VSB is not used
CN2-057	VMA03	Output	100 kΩ pull-down when VSB is not used
CN2-058	VMA04	Output	100 kΩ pull-down when VSB is not used
CN2-059	VMA05	Output	100 kΩ pull-down when VSB is not used
CN2-060	VMA06	Output	100 kΩ pull-down when VSB is not used
CN2-061	VMA07	Output	100 kΩ pull-down when VSB is not used
CN2-062	VMA08	Output	100 kΩ pull-down when VSB is not used
CN2-063	GND	–	–
CN2-064	GND	–	–
CN2-065	VMA09	Output	100 kΩ pull-down when VSB is not used
CN2-066	VMA10	Output	100 kΩ pull-down when VSB is not used
CN2-067	VMA11	Output	100 kΩ pull-down when VSB is not used
CN2-068	VMA12	Output	100 kΩ pull-down when VSB is not used
CN2-069	VMA13	Output	100 kΩ pull-down when VSB is not used
CN2-070	VMA14	Output	100 kΩ pull-down when VSB is not used
CN2-071	VMA15	Output	100 kΩ pull-down when VSB is not used
CN2-072	VMA16	Output	100 kΩ pull-down when VSB is not used
CN2-073	GND	–	–
CN2-074	GND	–	–
CN2-075	VMA17	Output	100 kΩ pull-down when VSB is not used
CN2-076	VMA18	Output	100 kΩ pull-down when VSB is not used

Table 2-19. CPU Connector 2 (CN2) (3/4)

CPU Connector	Signal Name	I/O	Remark
CN2-077	VMA19	Output	100 kΩ pull-down when VSB is not used
CN2-078	VMA20	Output	100 kΩ pull-down when VSB is not used
CN2-079	VMA21	Output	100 kΩ pull-down when VSB is not used
CN2-080	VMA22	Output	100 kΩ pull-down when VSB is not used
CN2-081	VMA23	Output	100 kΩ pull-down when VSB is not used
CN2-082	VMA24	Output	100 kΩ pull-down when VSB is not used
CN2-083	GND	–	–
CN2-084	GND	–	–
CN2-085	VMA25	Output	100 kΩ pull-down when VSB is not used
CN2-086	VMA26	Output	100 kΩ pull-down when VSB is not used
CN2-087	VMA27	Output	100 kΩ pull-down when VSB is not used
CN2-088	VBDO00	Output	100 kΩ pull-down when VSB is not used
CN2-089	VBDO01	Output	100 kΩ pull-down when VSB is not used
CN2-090	VBDO02	Output	100 kΩ pull-down when VSB is not used
CN2-091	VBDO03	Output	100 kΩ pull-down when VSB is not used
CN2-092	VBDO04	Output	100 kΩ pull-down when VSB is not used
CN2-093	GND	–	–
CN2-094	GND	–	–
Output	VBDO05	Output	100 kΩ pull-down when VSB is not used
CN2-096	VBDO06	Output	100 kΩ pull-down when VSB is not used
CN2-097	VBDO07	Output	100 kΩ pull-down when VSB is not used
CN2-098	VBDO08	Output	100 kΩ pull-down when VSB is not used
CN2-099	VBDO09	Output	100 kΩ pull-down when VSB is not used
CN2-100	VBDO10	Output	100 kΩ pull-down when VSB is not used
CN2-101	VBDO11	Output	100 kΩ pull-down when VSB is not used
CN2-102	VBDO12	Output	100 kΩ pull-down when VSB is not used
CN2-103	GND	–	–
CN2-104	GND	–	–
CN2-105	VBDO13	Output	100 kΩ pull-down when VSB is not used
CN2-106	VBDO14	Output	100 kΩ pull-down when VSB is not used
CN2-107	VBDO15	Output	100 kΩ pull-down when VSB is not used
CN2-108	VBDO16	Output	100 kΩ pull-down when VSB is not used
CN2-109	VBDO17	Output	100 kΩ pull-down when VSB is not used
CN2-110	VBDO18	Output	100 kΩ pull-down when VSB is not used
CN2-111	VBDO19	Output	100 kΩ pull-down when VSB is not used
CN2-112	VBDO20	Output	100 kΩ pull-down when VSB is not used
CN2-113	GND	–	–
CN2-114	GND	–	–

Table 2-19. CPU Connector 2 (CN2) (4/4)

CPU Connector	Signal Name	I/O	Remark
CN2-115	CS_USBZ	Output	Reserved (leave open)
CN2-116	CS_LANZ	Output	Reserved (leave open)
CN2-117	GND	–	–
CN2-118	GND	–	–
CN2-119	GND	–	–
CN2-120	GND	–	–

Table 2-20. CPU Connector 3 (CN3) (1/4)

CPU Connector	Signal Name	I/O	Remark
CN3-001	GND	–	–
CN3-002	GND	–	–
CN3-003	GND	–	–
CN3-004	GND	–	–
CN3-005	VBDO21	Output	100 kΩ pull-down when VSB is not used
CN3-006	VBDO22	Output	100 kΩ pull-down when VSB is not used
CN3-007	VBDO23	Output	100 kΩ pull-down when VSB is not used
CN3-008	VBDO24	Output	100 kΩ pull-down when VSB is not used
CN3-009	VBDO25	Output	100 kΩ pull-down when VSB is not used
CN3-010	VBDO26	Output	100 kΩ pull-down when VSB is not used
CN3-011	VBDO27	Output	100 kΩ pull-down when VSB is not used
CN3-012	VBDO28	Output	100 kΩ pull-down when VSB is not used
CN3-013	GND	–	–
CN3-014	GND	–	–
CN3-015	VBDO29	Output	100 kΩ pull-down when VSB is not used
CN3-016	VBDO30	Output	100 kΩ pull-down when VSB is not used
CN3-017	VBDO31	Output	100 kΩ pull-down when VSB is not used
CN3-018	VSAHLD	Output	Reserved (leave open)
CN3-019	VSLAST	Output	Reserved (leave open)
CN3-020	VSLOCK	Input	Reserved (leave open)
CN3-021	VSWAIT	Output	Reserved (leave open)
CN3-022	VBDV	Output	100 kΩ pull-down when VSB is not used
CN3-023	GND	–	–
CN3-024	GND	–	–
CN3-025	VBDC	Output	100 kΩ pull-down when VSB is not used
CN3-026	VSWRITE	Input	Reserved (leave open)
CN3-027	VSBENZ1	Input	Reserved (leave open)
CN3-028	VSSTZ	Input	Reserved (leave open)
Input	VSA00	Input	Reserved (leave open)
CN3-030	VSA01	Input	Reserved (leave open)
CN3-031	VSA02	Input	Reserved (leave open)
CN3-032	VSA03	Input	Reserved (leave open)
CN3-033	GND	–	–
CN3-034	GND	–	–
CN3-035	VSA04	Input	Reserved (leave open)
CN3-036	VSA05	Input	Reserved (leave open)
CN3-037	VSA06	Input	Reserved (leave open)
CN3-038	VSA07	Input	Reserved (leave open)

Table 2-20. CPU Connector 3 (CN3) (2/4)

CPU Connector	Signal Name	I/O	Remark
CN3-039	VSA08	Input	Reserved (leave open)
CN3-040	VSA09	Input	Reserved (leave open)
CN3-041	VSA10	Input	Reserved (leave open)
CN3-042	VSA11	Input	Reserved (leave open)
CN3-043	GND	–	–
CN3-044	GND	–	–
CN3-045	VSA12	Input	Reserved (leave open)
CN3-046	VSA13	Input	Reserved (leave open)
CN3-047	VDSELPZ	Output	100 kΩ pull-down when VSB is not used
CN3-048	VMAHLD	Input	47 kΩ pull-down
CN3-049	VMLAST	Input	47 kΩ pull-down
CN3-050	VMWAIT	Input	47 kΩ pull-down
CN3-051	VMBSTR	Output	100 kΩ pull-down when VSB is not used
CN3-052	VMSEQ0	Output	100 kΩ pull-down when VSB is not used
CN3-053	GND	–	–
CN3-054	GND	–	–
CN3-055	VMSEQ1	Output	100 kΩ pull-down when VSB is not used
CN3-056	VMSEQ2	Output	100 kΩ pull-down when VSB is not used
CN3-057	VMCTYP0	Output	100 kΩ pull-down when VSB is not used
CN3-058	VMCTYP1	Output	100 kΩ pull-down when VSB is not used
CN3-059	VMCTYP2	Output	100 kΩ pull-down when VSB is not used
CN3-060	VMLOCK	Output	100 kΩ pull-down when VSB is not used
CN3-061	VMWRITE	Output	100 kΩ pull-down when VSB is not used
CN3-062	VMSIZE0	Output	100 kΩ pull-down when VSB is not used
CN3-063	GND	–	–
CN3-064	GND	–	–
CN3-065	VMSIZE1	Output	100 kΩ pull-down when VSB is not used
CN3-066	VSSELPZ	Input	Reserved (leave open)
CN3-067	VDCSZ0	Output	–
CN3-068	VDCSZ1	Output	–
CN3-069	VDCSZ2	Output	–
CN3-070	VDCSZ3	Output	–
CN3-071	VDCSZ4	Output	–
CN3-072	VDCSZ5	Output	–
CN3-073	GND	–	–
CN3-074	GND	–	–
CN3-075	VDCSZ6	Output	–
CN3-076	VDCSZ7	Output	–

Table 2-20. CPU Connector 3 (CN3) (3/4)

CPU Connector	Signal Name	I/O	Remark
CN3-077	VAACK	Output	–
CN3-078	VAPREQ	Output	–
CN3-079	VAREQ	Input	47 kΩ pull-down
CN3-080	GACONNECT	Input	Reserved (leave open)
CN3-081	BCONNECT	Input	Reserved (leave open)
CN3-082	INTLAN	Input	Reserved (leave open)
CN3-083	GND	–	–
CN3-084	GND	–	–
CN3-085	INTUSB	Input	Reserved (leave open)
CN3-086	CONNECT2_1	Input	Reserved (leave open)
CN3-087	CONNECT2_2	Input	Reserved (leave open)
CN3-088	CONNECT2_3	Input	Reserved (leave open)
CN3-089	CONNECT2_4	Input	Reserved (leave open)
CN3-090	CONNECT2_5	Input	Reserved (leave open)
CN3-091	CONNECT2_6	Input	Reserved (leave open)
CN3-092	CONNECT2_7	Input	Reserved (leave open)
CN3-093	GND	–	–
CN3-094	GND	–	–
CN3-095	NC	–	Reserved (leave open)
CN3-096	NC	–	Reserved (leave open)
CN3-097	NC	–	Reserved (leave open)
CN3-098	NC	–	Reserved (leave open)
CN3-099	NC	–	Reserved (leave open)
CN3-100	NC	–	Reserved (leave open)
CN3-101	NC	–	Reserved (leave open)
CN3-102	NC	–	Reserved (leave open)
CN3-103	GND	–	–
CN3-104	GND	–	–
CN3-105	PORT0	I/O	Reserved (leave open)
CN3-106	PORT1	I/O	Reserved (leave open)
CN3-107	PORT2	I/O	Reserved (leave open)
CN3-108	PORT3	I/O	Reserved (leave open)
CN3-109	NC	–	Reserved (leave open)
CN3-110	NC	–	Reserved (leave open)
CN3-111	NC	–	Reserved (leave open)
CN3-112	NC	–	Reserved (leave open)
CN3-113	NC	–	Reserved (leave open)
CN3-114	NC	–	Reserved (leave open)

Table 2-20. CPU Connector 3 (CN3) (4/4)

CPU Connector	Signal Name	I/O	Remark
CN3-115	NC	–	Reserved (leave open)
CN3-116	NC	–	Reserved (leave open)
CN3-117	GND	–	–
CN3-118	GND	–	–
CN3-119	GND	–	–
CN3-120	GND	–	–

Table 2-21. CPU Connector 4 (CN4) (1/4)

CPU Connector	Signal Name	I/O	Remark
CN4-001	GND	–	–
CN4-002	GND	–	–
CN4-003	GND	–	–
CN4-004	GND	–	–
CN4-005	OSCCLK	Output	In-phase with μPD703193 input clock (CLKIN)
CN4-006	CLKOUT	Output	Output of μPD703193
CN4-007	GND	–	–
CN4-008	GND	–	–
CN4-009	3 V	Output	Reserved (leave open)
CN4-010	2.5 V	Output	Reserved (leave open)
CN4-011	3 V	Output	Reserved (leave open)
CN4-012	2.5 V	Output	Reserved (leave open)
CN4-013	3 V	Output	Reserved (leave open)
CN4-014	NMI2	Input	47 kΩ pull-down
CN4-015	NMI1	Input	47 kΩ pull-down
CN4-016	NMI0	Input	47 kΩ pull-down
CN4-017	GND	–	–
CN4-018	GND	–	–
CN4-019	INT63	Input	47 kΩ pull-down
CN4-020	INT62	Input	47 kΩ pull-down
CN4-021	INT61	Input	47 kΩ pull-down
CN4-022	INT60	Input	47 kΩ pull-down
CN4-023	INT59	Input	47 kΩ pull-down
CN4-024	INT58	Input	47 kΩ pull-down
CN4-025	INT57	Input	47 kΩ pull-down
CN4-026	INT56	Input	47 kΩ pull-down
CN4-027	INT55	Input	47 kΩ pull-down
CN4-028	INT54	Input	47 kΩ pull-down
CN4-029	INT53	Input	47 kΩ pull-down
CN4-030	INT52	Input	47 kΩ pull-down
CN4-031	INT51	Input	47 kΩ pull-down
CN4-032	INT50	Input	47 kΩ pull-down
CN4-033	INT49	Input	47 kΩ pull-down
CN4-034	INT48	Input	47 kΩ pull-down
CN4-035	INT47	Input	47 kΩ pull-down
CN4-036	INT46	Input	47 kΩ pull-down
CN4-037	INT45	Input	47 kΩ pull-down
CN4-038	INT44	Input	47 kΩ pull-down

Table 2-21. CPU Connector 4 (CN4) (2/4)

CPU Connector	Signal Name	I/O	Remark
CN4-039	INT43	Input	47 kΩ pull-down
CN4-040	INT42	Input	47 kΩ pull-down
CN4-041	INT41	Input	47 kΩ pull-down
CN4-042	INT40	Input	47 kΩ pull-down
CN4-043	INT39	Input	47 kΩ pull-down
CN4-044	INT38	Input	47 kΩ pull-down
CN4-045	INT37	Input	47 kΩ pull-down
CN4-046	INT36	Input	47 kΩ pull-down
CN4-047	INT35	Input	47 kΩ pull-down
CN4-048	INT34	Input	47 kΩ pull-down
CN4-049	INT33	Input	47 kΩ pull-down
CN4-050	INT32	Input	47 kΩ pull-down
CN4-051	GND	–	–
CN4-052	GND	–	–
CN4-053	INT31	Input	47 kΩ pull-down
CN4-054	INT30	Input	47 kΩ pull-down
CN4-055	INT29	Input	47 kΩ pull-down
CN4-056	INT28	Input	47 kΩ pull-down
CN4-057	INT27	Input	47 kΩ pull-down
CN4-058	INT26	Input	47 kΩ pull-down
CN4-059	INT25	Input	47 kΩ pull-down
CN4-060	INT24	Input	47 kΩ pull-down
CN4-061	INT23	Input	47 kΩ pull-down
CN4-062	INT22	Input	47 kΩ pull-down
CN4-063	INT21	Input	47 kΩ pull-down
CN4-064	INT20	Input	47 kΩ pull-down
CN4-065	INT19	Input	47 kΩ pull-down
CN4-066	INT18	Input	47 kΩ pull-down
CN4-067	INT17	Input	47 kΩ pull-down
CN4-068	INT16	Input	47 kΩ pull-down
CN4-069	INT15	Input	47 kΩ pull-down
CN4-070	INT14	Input	47 kΩ pull-down
CN4-071	INT13	Input	47 kΩ pull-down
CN4-072	INT12	Input	47 kΩ pull-down
CN4-073	INT11	Input	47 kΩ pull-down
CN4-074	INT10	Input	47 kΩ pull-down
CN4-075	INT09	Input	47 kΩ pull-down
CN4-076	INT08	Input	47 kΩ pull-down

Table 2-21. CPU Connector 4 (CN4) (3/4)

CPU Connector	Signal Name	I/O	Remark
CN4-077	INT07	Input	47 kΩ pull-down
CN4-078	INT06	Input	47 kΩ pull-down
CN4-079	INT05	Input	47 kΩ pull-down
CN4-080	INT04	Input	47 kΩ pull-down
CN4-081	INT03	Input	47 kΩ pull-down
CN4-082	INT02	Input	47 kΩ pull-down
CN4-083	INT01	Input	47 kΩ pull-down
CN4-084	INT00	Input	47 kΩ pull-down
CN4-085	GND	–	–
CN4-086	GND	–	–
CN4-087	CGREL	Output	–
CN4-088	STPRQ	Output	–
CN4-089	STPAK	Output	–
CN4-090	HWSTOPRQ	Output	–
CN4-091	SWSTOPRQ	Output	–
CN4-092	EXHLT	Output	–
CN4-093	PEWAITZ	Input	Reserved (leave open)
CN4-094	WAITB_PIO	Input	Reserved (leave open)
CN4-095	GND	–	–
CN4-096	GND	–	–
CN4-097	LA4	Output	Reserved (leave open)
CN4-098	LA5	Output	Reserved (leave open)
CN4-099	LA6	Output	Reserved (leave open)
CN4-100	LA7	Output	Reserved (leave open)
CN4-101	LA8	Output	Reserved (leave open)
CN4-102	PERDZ	Output	Reserved (leave open)
CN4-103	PEWRZ	Output	Reserved (leave open)
CN4-104	NC	–	Reserved (leave open)
CN4-105	GND	–	–
CN4-106	GND	–	–
CN4-107	LD0	I/O	Reserved (leave open)
CN4-108	LD1	I/O	Reserved (leave open)
CN4-109	LD2	I/O	Reserved (leave open)
CN4-110	LD3	I/O	Reserved (leave open)
CN4-111	LD4	I/O	Reserved (leave open)
CN4-112	LD5	I/O	Reserved (leave open)
CN4-113	LD6	I/O	Reserved (leave open)
CN4-114	LD7	I/O	Reserved (leave open)

Table 2-21. CPU Connector 4 (CN4) (4/4)

CPU Connector	Signal Name	I/O	Remark
CN4-115	GND	–	–
CN4-116	GND	–	–
CN4-117	CS_UART0Z	Output	Reserved (leave open)
CN4-118	CS_UART1Z	Output	Reserved (leave open)
CN4-119	CS_PPZ	Output	Reserved (leave open)
CN4-120	CS_ECPZ	Output	Reserved (leave open)
CN4-121	INT_UART0	Input	Reserved (leave open)
CN4-122	INT_UART1	Input	Reserved (leave open)
CN4-123	INT_PIO	Input	Reserved (leave open)
CN4-124	GND	–	–
CN4-125	CS_GATAZ	Output	Reserved (leave open)
CN4-126	TBASECLK	Output	Reserved (leave open)
CN4-127	GND	–	–
CN4-128	GND	–	–
CN4-129	STOPZ	Input	10 kΩ pull-up
CN4-130	HLDAKZ	Output	–
CN4-131	HLDRQZ	Input	10 kΩ pull-up
CN4-132	S256_16	Output	Reserved (leave open)
CN4-133	DC0	Output	–
CN4-134	DC1	Output	–
CN4-135	DC2	Output	–
CN4-136	DC3	Output	–
CN4-137	GND	–	–
CN4-138	GND	–	–
CN4-139	GND	–	–
CN4-140	GND	–	–

Table 2-22. CPU Connector 5 (CN5) (1/4)

CPU Connector	Signal Name	I/O	Remark
CN5-001	GND	–	–
CN5-002	GND	–	–
CN5-003	GND	–	–
CN5-004	GND	–	–
CN5-005	A00	Output	–
CN5-006	A01	Output	–
CN5-007	A02	Output	–
CN5-008	A03	Output	–
CN5-009	A04	Output	–
CN5-010	A05	Output	–
CN5-011	A06	Output	–
CN5-012	A07	Output	–
CN5-013	GND	–	–
CN5-014	GND	–	–
CN5-015	A08	Output	–
CN5-016	A09	Output	–
CN5-017	A10	Output	–
CN5-018	A11	Output	–
CN5-019	A12	Output	–
CN5-020	A13	Output	–
CN5-021	A14	Output	–
CN5-022	A15	Output	–
CN5-023	GND	–	–
CN5-024	GND	–	–
CN5-025	A16	Output	–
CN5-026	A17	Output	–
CN5-027	A18	Output	–
CN5-028	A19	Output	–
CN5-029	A20	Output	–
CN5-030	A21	Output	–
CN5-031	A22	Output	–
CN5-032	A23	Output	–
CN5-033	GND	–	–
CN5-034	GND	–	–
CN5-035	A24	Output	–
CN5-036	A25	Output	–
CN5-037	D00	I/O	47 kΩ pull-down
CN5-038	D01	I/O	47 kΩ pull-down

Table 2-22. CPU Connector 5 (CN5) (2/4)

CPU Connector	Signal Name	I/O	Remark
CN5-039	D02	I/O	47 kΩ pull-down
CN5-040	D03	I/O	47 kΩ pull-down
CN5-041	D04	I/O	47 kΩ pull-down
CN5-042	D05	I/O	47 kΩ pull-down
CN5-043	GND	–	–
CN5-044	GND	–	–
CN5-045	D06	I/O	47 kΩ pull-down
CN5-046	D07	I/O	47 kΩ pull-down
CN5-047	D08	I/O	47 kΩ pull-down
CN5-048	D09	I/O	47 kΩ pull-down
CN5-049	D10	I/O	47 kΩ pull-down
CN5-050	D11	I/O	47 kΩ pull-down
CN5-051	D12	I/O	47 kΩ pull-down
CN5-052	D13	I/O	47 kΩ pull-down
CN5-053	GND	–	–
CN5-054	GND	–	–
CN5-055	D14	I/O	47 kΩ pull-down
CN5-056	D15	I/O	47 kΩ pull-down
CN5-057	D16	I/O	47 kΩ pull-down
CN5-058	D17	I/O	47 kΩ pull-down
CN5-059	D18	I/O	47 kΩ pull-down
CN5-060	D19	I/O	47 kΩ pull-down
CN5-061	D20	I/O	47 kΩ pull-down
CN5-062	D21	I/O	47 kΩ pull-down
CN5-063	GND	–	–
CN5-064	GND	–	–
CN5-065	D22	I/O	47 kΩ pull-down
CN5-066	D23	I/O	47 kΩ pull-down
CN5-067	D24	I/O	47 kΩ pull-down
CN5-068	D25	I/O	47 kΩ pull-down
CN5-069	D26	I/O	47 kΩ pull-down
CN5-070	D27	I/O	47 kΩ pull-down
CN5-071	D28	I/O	47 kΩ pull-down
CN5-072	D29	I/O	47 kΩ pull-down
CN5-073	GND	–	–
CN5-074	GND	–	–
CN5-075	D30	I/O	47 kΩ pull-down
CN5-076	D31	I/O	47 kΩ pull-down

Table 2-22. CPU Connector 5 (CN5) (3/4)

CPU Connector	Signal Name	I/O	Remark
CN5-077	CSZ0	Output	47 kΩ pull-up
CN5-078	CSZ1	Output	47 kΩ pull-up
CN5-079	CSZ2	Output	47 kΩ pull-up
CN5-080	CSZ3	Output	47 kΩ pull-up
CN5-081	CSZ4	Output	47 kΩ pull-up
CN5-082	CSZ5	Output	47 kΩ pull-up
CN5-083	CSZ6	Output	47 kΩ pull-up
CN5-084	CSZ7	Output	47 kΩ pull-up
CN5-085	GND	–	–
CN5-086	GND	–	–
CN5-087	WAITZ	Input	10 kΩ pull-up
CN5-088	RDZ	Output	10 kΩ pull-up
CN5-089	WRZ0	Output	–
CN5-090	WRZ1	Output	–
CN5-091	WRZ2	Output	–
CN5-092	WRZ3	Output	–
CN5-093	IORDZ	Output	–
CN5-094	IOWRZ	Output	–
CN5-095	NC	–	Reserved (leave open)
CN5-096	BCYSTZ	Output	–
CN5-097	GND	–	–
CN5-098	GND	–	–
CN5-099	BENZ0	Output	–
CN5-100	BENZ1	Output	–
CN5-101	BENZ2	Output	–
CN5-102	BENZ3	Output	–
CN5-103	DQMZ0	Output	–
CN5-104	DQMZ1	Output	–
CN5-105	DQMZ2	Output	–
CN5-106	DQMZ3	Output	–
CN5-107	GND	–	–
CN5-108	GND	–	–
CN5-109	SDCLK	Output	–
CN5-110	CKE	Output	–
CN5-111	GND	–	–
CN5-112	SELFREF	Input	47 kΩ pull-down
CN5-113	REFRQZ	Output	–
CN5-114	SDCASZ	Output	–

Table 2-22. CPU Connector 5 (CN5) (4/4)

CPU Connector	Signal Name	I/O	Remark
CN5-115	SDRASZ	Output	–
CN5-116	SDWEZ	Output	–
CN5-117	GND	–	–
CN5-118	GND	–	–
CN5-119	GND	–	–
CN5-120	GND	–	–

2.12 Connector for Motherboard (JGBUS1)

JGBUS1 is a bus connector of 32-bit data width for connecting a motherboard. For details, refer to **CHAPTER 3 GBUS-SPECIFIC SPECIFICATIONS** and **CHAPTER 4 GBUS COMMON SPECIFICATIONS**.

CHAPTER 3 GBUS-SPECIFIC SPECIFICATIONS

This chapter explains how GBUS is used with SolutionGear-CPU-NU85ET. For the general GBUS specifications, refer to **CHAPTER 4 GBUS COMMON SPECIFICATIONS.**

3.1 General

The following table shows the GBUS signal lines used by SolutionGear-CPU-NU85ET.

Table 3-1. List of GBUS Signal Functions

GBUS Signal Name	Function
GADDR[31:2]	Used as address lines. GADDR[26:31] are not connected.
GDATA[31:0]	Used as data lines. In a read cycle, the signal that is latched at the rising edge of VBCLK is supplied to the CPU.
GCS-[6:0]	Used as chip select lines.
GCLK	Connects the clock fixed to 33 MHz asynchronous to the CPU clock.
GRESETI-	Outputs the reset request generated on the main board.
GRESETO-	Not connected
GADS-, GREADY-, GBLAST-, GW/R-	Used as bus control signal
GWAITI-	Not connected
GBTERM-	Not connected
GRD-, GWR-	Connects RD- and WR- signals generated from the GBUS control signals.
GHOLD-, GHLDA-	Not connected
GBREQ-	Not connected
GDMARQ-[3:0]	Used as DMA request signals. Invert the logic of the DMARQ request from GBUS and connect it to the CPU. GDMARQ-[3:0] → DMARQ[3:0]
GDMAAK-[3:0]	Used as DMA acknowledge signals. Invert the logic of the signal output from the CPU and connect it to the GBUS. GDMAAK-[3:0] → DMACTV[3:0]
GINTO-[3:0]	Used as interrupt request signals.
GINTI-[1:0]	Connects OUT0 and OUT1 of TIC (μPD71054) to GINTI0- and GINTI1-, respectively.
GETC[7:0]	Not connected
GAHI_EN-	Not connected
GMOTHER_DETECT-	Motherboard detection signal.
GUSE_DIRECT_ACC-	Not connected
GCLK_LOW-	Not connected
GLOCK-[10]	Not connected

3.2 Bus Cycle

A 33 MHz clock that is asynchronous to the CPU clock is connected to GCLK of GBUS. In addition, because GAHI_EN- is not connected, GADDR[26:31] are not connected. GADDR[24:25] are always [0,0].

A read cycle from GBUS can be executed on GBUS without a wait cycle (0-wait operation).

The bus cycle is shown in Figure 3-1.

In Figure 3-1, a CPU_xxx signal indicates a CPU signal and a Gxxx signal indicates a GBUS signal.

Figure 3-1. Bus Cycles (1/2)

(a) Read cycle

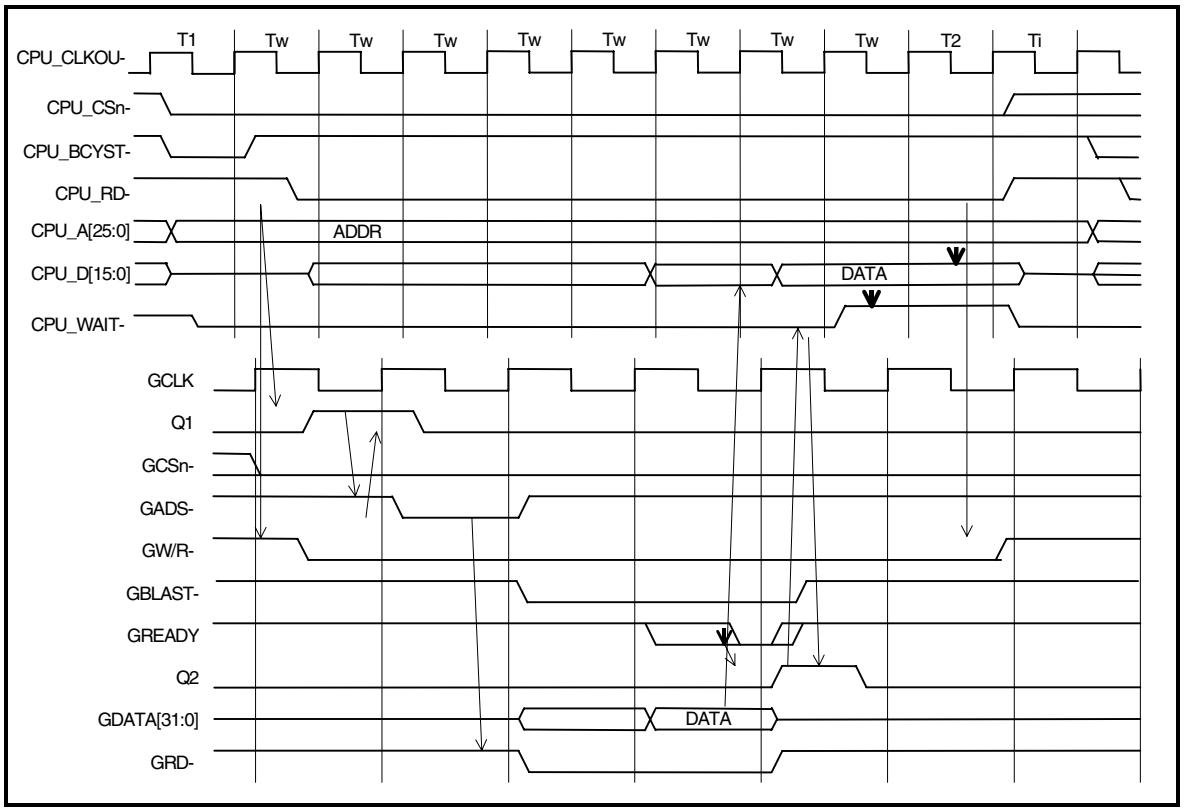
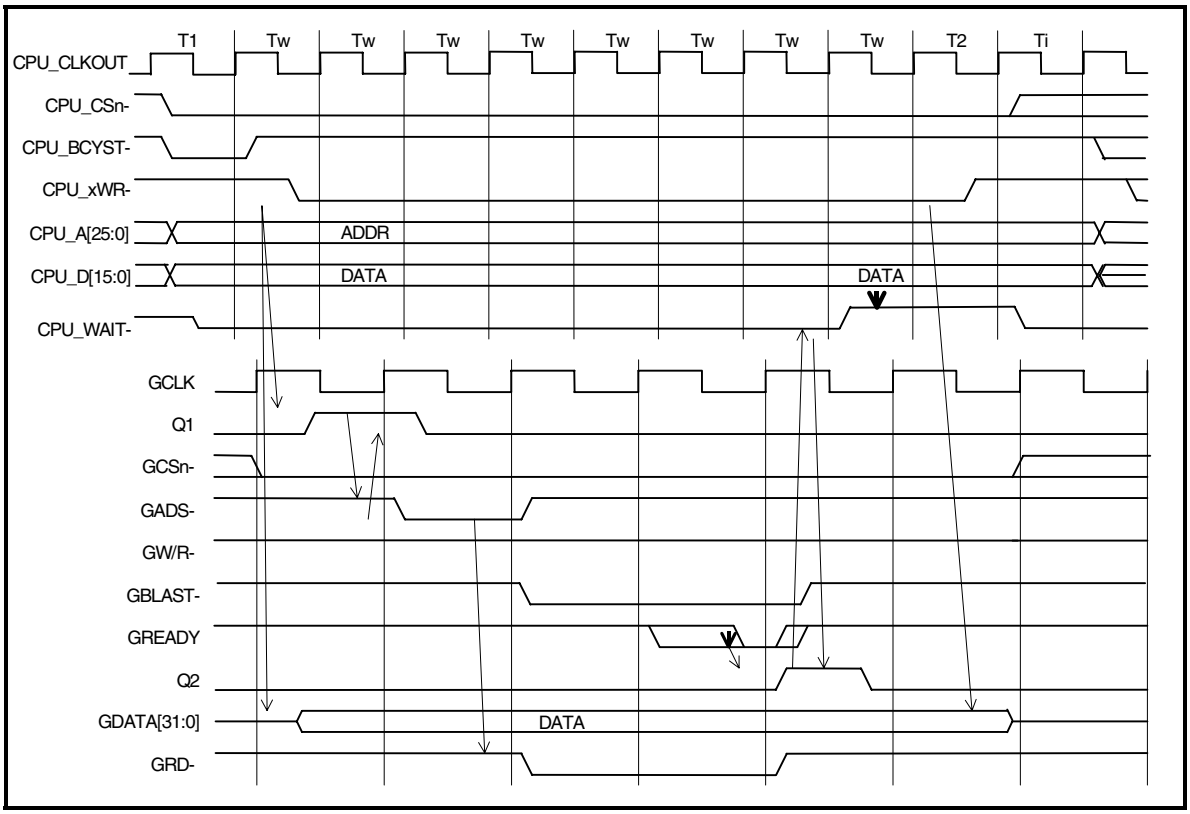


Figure 3-1. Bus Cycles (2/2)

(b) Write cycle



3.3 Chip Select

On this board, the spaces shown in Table 3-2 are assigned to GBUS chip select signals.

For how to set the CPU on-chip bus configuration register in all the spaces shown in Table 3-2, refer to **5.3 Setting of MEMC and μPD703193 Registers.**

Table 3-2. Chip Select

GBUS Signal Name	CPU Address Space	Physical Address Range	RTE-MB-A Resources
GCS0-	CS2 space	0400000H to 05FFFFFH	Common SRAM (2M)
GCS1-	CS4 space, or CS0 space when SW2 and SW1 (FBOOT) are ON	1000000H to 17FFFFFH 0000000H to 03FFFFFH	Flash ROM (8M)
GCS2-	CS6 space	3100000H to 317FFFFH	IO register
GCS3-	CS3 space	1800000H to 1FFFFFFH	EXT-bus: memory space
GCS4-	CS6 space	3600000H to 37FFFFFH	EXT-bus: IO space
GCS5-	CS1 space	0800000H to 0FFFFFFH	PCI bus space
GCS6-	CS6 space	3180000H to 318FFFFH	PCI-Cont register
GCS7-	CS6 space	3000000H to 300FFFFH	PCI bus space

CHAPTER 4 GBUS COMMON SPECIFICATIONS

This chapter explains the GBUS specifications that are independent of the type of board.

4.1 Terminology

Terminology used in this chapter is explained below.

Table 4-1. Terminology

Terminology	Meaning
CPU board and motherboard	A board in the RTE-CB series is called a CPU board and an NEC Electronics board connected to GBUS of the CPU board is called a motherboard.
Bus cycle and micro cycle	GBUS is a general bus that can be accessed in burst mode. A bus cycle is a complete series of cycles, including when burst access is used (asserting GADS- is necessary to mark the end of a bus cycle). One cycle for each data transfer in a burst cycle is called a micro cycle. Bus cycles are classified into single cycles and a burst cycles. A single cycle is a bus cycle in which data transfer occurs only once. A burst cycle is a bus cycle in which data transfer occurs two or more times.

4.2 Signals

The GBUS signals are listed in Table 4-2. The input/output direction of each GBUS signal is indicated as viewed from the motherboard. Therefore, the column “I/O” in Table 4-2 indicates the following.

“Input” means that a signal output from the CPU board is input to the motherboard (this also applies to signal names).

“Bidirectional” signals change direction depending on the status of the bus cycle.

“Input/output” signals also change direction depending on whether the bus master is the CPU board or motherboard. The direction written first is the signal direction when the CPU board is the bus master, and the direction written later is the signal direction when the motherboard is the bus master.

A GBUS signal is a +5 V TTL level signal. The motherboard is always little endian.

Table 4-2. GBUS Signals (1/4)

Signal Name	I/O	Function
GCLK	Input	• Synchronization clock of GBUS. The maximum frequency is 33.33 MHz, and the minimum frequency is 10.0 MHz. GBUS operates synchronized with the rising edge of this clock. • Since, on the motherboard, this clock is terminated at 330 Ω with respect to + 5V and GND, the circuit on the CPU board must be able to drive this resistance. • If GCLK is less than 16.67 MHz, GCLK_LOW- goes low. In this way, the motherboard can adjust the number of wait cycles. • Because a PLL (Phase Lock Loop) zero delay buffer may be used, if the frequency of GCLK is changed, the motherboard must not be accessed for at least 1 ms after the frequency has been changed to allow the PLL to be locked.
GRESETI-	Input	• Reset signal of GBUS. If a reset occurs on the CPU board, this signal goes low. The motherboard is reset by this signal (the motherboard can also be reset by other factors on the motherboard).
GRESETO-	Output	• This signal goes low if the motherboard is reset. • The motherboard ORs the reset signal on the motherboard with GRESETI- as GRESETO-. Accordingly, the CPU board resets the circuits on the CPU board by ORing GRESETI- and GRESETO- (GRESETI- and GRESETO- are ORed because there is a possibility that the motherboard is not connected).
GADDR[31:2]	Input/Output	• Address signals of GBUS. These signals are driven by a valid value during the bus cycle. • GADDR[31] is ignored on the motherboard if the CPU is the bus master. • The lower addresses A1 and A0 use a byte enable signal. • GADDR[31:26] from the CPU board can be treated as 0 by using the GAHI_EN- signal. • If the bus master is the motherboard and if GADDR[25] is 0, the resources on the motherboard are selected; if GADDR[25] is 1, the resources on the CPU board are selected.
GBEN-[3:0]	Input/Output	• Byte enable signals of GBUS. These signals are always driven by a valid value during the bus cycle. • GBEN0-, GBEN1-, GBEN2-, and GBEN3- correspond to byte lanes GDATA[7:0], GDATA[15:8], GDATA[23:16], and GDATA[31:24], and the corresponding byte lane is valid if GBENx- is low.
GDATA[31:0]	Bidirectional	• Bus data signals of GBUS. • These signals are pulled up to 10 kΩ on the motherboard. • The direction of these signals is determined by GW/R-.
GADS-	Input/Output	• Address strobe signal of GBUS. If this signal is sampled low on the rising edge of GCLK, the start of a bus cycle is indicated. • The motherboard ignores GADS- if none of the chip select signals (GCS-[7:0]) is active.
GREADY-	Output/Input	• Ready signal of GBUS. If this signal is sampled low and GWAITI is sampled high on the rising edge of GCLK during a micro cycle, the end of the micro cycle is indicated. • Time-over ready when the CPU board accesses the motherboard is generated by the motherboard. The reason is to avoid collision with the GREADY- signal.

Table 4-2. GBUS Signals (2/4)

Signal Name	I/O	Function
GWAITI-	Input	• Wait request signal. This signal is sampled on the rising edge of GCLK. • If the CPU board cannot support a cycle with only a few wait cycles, the CPU board samples GWAITI- low at the sampling timing of GREADY- so that the motherboard cannot handle GREADY- as a ready signal even though it is low at the time. Usually, this signal is used if the CPU board cannot support zero wait burst (see **4.6.3 GWAITI-**). • This signal is valid only in a cycle in which the CPU board is the bus master.
GBLAST-	Input/Output	• Bus cycle completion notification signal. This signal is sampled on the rising edge of GCLK. • This signal is asserted low by the bus master when a micro cycle that completes the bus cycle starts. • The bus cycle is completed if the low level of GBLAST-, low level of GREADY-, and high level of GWAITI- are sampled on the rising edge of GCLK
GBTERM-	Output/Input	• Bus cycle completion request signal. This signal is sampled on the rising edge of GCLK. • If the accessed side requests completion of the bus cycle, the GREADY- and GBTERM- signals go low. GBTERM- must be asserted at the same time as GREADY-. If the bus master samples GBTERM- as low not simultaneously with when it samples GREADY- as low, it must complete the bus cycle even though GBLAST- has not been asserted, and start the bus cycle again by asserting GADS- again • This signal is used to complete the bus cycle if the accessed side does not support burst cycles or if a burst cycle exceeding the supported number of bursts is requested.
GW/R-	Input/Output	• Write/Read signal. This signal indicates the direction of the data bus. It is always driven by a valid value during the bus cycle. • This signal indicates the direction of the data bus for the bus master.
GCS-[7:0]	Input	• Chip select signals. Valid values these signals are always driven during the bus cycle. • The CPU board makes the corresponding chip select signal active to specify the resources on the motherboard when the CPU board is the bus master. • Each chip select signal specifies the width of the space for the memory/I/O space (see **4.5 Assigning GCS-[7:0]**).
GRD-	Input	• Read timing signal. This signal is asserted when the CPU board is the bus master. • This signal is not used by the motherboard. • If the CPU has an RD- command signal, that signal is usually connected.
GWR-	Input	• Write timing signal. This signal is asserted when the CPU board is the bus master. • This signal is not used by the motherboard. • If the CPU has a WR- command signal, that signal is usually connected.
GHOLD-	Output	• Bus hold request signal. • This signal is asserted low when the motherboard accesses the resources on the CPU board to acquire bus mastership. • If the GUSE_DIRECT_ACC- signal is high, the GHOLD- signal indicates to the CPU board that the motherboard has no resources that can be accessed. In this case, the CPU board does not have to support GHOLD-.

Table 4-2. GBUS Signals (3/4)

Signal Name	I/O	Function
GHLDA-	Input	• Bus hold acknowledge signal. • This signal indicates that the CPU board passes bus mastership of GBUS to the motherboard. It is then asserted low. • The GHLDA- signal can be disconnected on a CPU board that asserts the GUSE_DIRECT_ACC- signal high.
GBREQ-	Input	• Bus mastership return request signal • When the motherboard has bus mastership from asserting GHLDA- low, the CPU board asserts GBREQ- low when it requires bus mastership. • If GBREQ- is asserted low and the motherboard is in bus cycle, GBLAST- must be asserted in the next micro cycle, the bus cycle must be completed in the next micro cycle, and GHOLD- must be deasserted. • GBREQ- is used to return bus mastership to the CPU board temporarily if the number of bursts in the bus cycle is large when the motherboard is the bus master, or if a bus cycle with a high priority such as a refresh cycle is pending on the CPU board.
GDMARQ-[3:0]	Output	• DMA request signals. Only two-cycle DMA is supported. Flyby DMA is not supported. • These signals are asserted low if a DMA request is generated on the motherboard. • The CPU board must support all four DMA signals. The number of DMA signals that can be asserted at the same time and can be supported by the GDMAAK- signal depends on the CPU board. • The CPU board uses the DMAAK signal in preference to DMAAK-[3:2] if correspondence between all four GDMARQ- signals and GDMAAK- signals cannot be established.
GDMAAK-[3:0]	Input	• DMA acknowledge signals. • These signals are asserted low to acknowledge DMA requests from the motherboard. • The CPU board uses the DMAAK signal in preference to DMAAK-[3:2] if correspondence between all four GDMARQ- signals and GDMAAK- signals cannot be established. • The motherboard is designed to operate even if there is no GDMAAK- signal.
GINTO-[3:0]	Output	• Interrupt request signals. • GINTO0- can be used as a level-sensitive signal. • Whether GINTO-[3:1] can be used as level-sensitive signals or edge-sensitive signals depends on the CPU board (since they may be directly connected to the CPU). The motherboard can support both level- and edge-sensitive signals. • Occurrence of an interrupt is indicated when these signals are low or at the falling edges of these signals.
GINTI-[1:0]	Input	• Interrupt request signals. • These interrupt signals are used to combine an interrupt on the CPU board with an interrupt on the other motherboard and return the combined signal to GINTO-[3:0]. • Usually, OUT0 and OUT1 of TIC (μPD71054) on the CPU board are connected. The motherboard can select the type of sensitivity and polarity of these interrupt signals.
GETC[7:0]	–	• CPU board dependent signals. • The contents of GETC[7:0], including the direction and contents of the signals, are determined by the CPU board. The CPU board uses these signals to exchange special signals with the motherboard.

Table 4-2. GBUS Signals (4/4)

Signal Name	I/O	Function
GAHI_EN-	Input	• Upper address valid signal. • If this signal is low and if the CPU board is the bus master, the CPU board drives a valid value on GADDR[31:26]. If this signal is high, the CPU board does not drive a valid signal on GADDR[31:26], and the circuits on the motherboard perform processing with all of GADDR[31:26] low.
GMOTHER_DETECT-	Output	• Motherboard detection signal. • This signal is pulled up on the CPU board, and is connected to GND on the motherboard. The CPU board uses this signal when it must determine if the motherboard is connected.
GUSE_DIRECT_ACC-	Input	• If this signal is low, the CPU board has resources that can be accessed by the motherboard.
GCLK_LOW-	Input	• If this signal is low, the frequency of GCLK is 16.67 MHz or less. If it is high, the frequency of GCLK is 16.67 to 33.33 MHz. • The circuits on the motherboard use this signal to determine the number of wait cycles required for accessing the resources on the motherboard.
GBLOCK-[1:0]	Input	• Bus lock signals. These signals must be valid during a bus cycle and for bus cycles that must be locked. • If a bus lock signal is output by the CPU, the bus lock signal is connected to the motherboard using these pins. • The GBLOCK0- signal is valid for the GCS0- space. GBLOCK1- is valid for the GCS5- and GCS7- spaces.
+5 V	Output	• Power supply. Supplies +5 V ±5% from the motherboard to the CPU board.
+12 V	Output	• Power supply. Supplies +12 V ±10% from the motherboard to the CPU board. However, if the CPU board does not require +12 V, the motherboard does not have to supply +12 V.

4.3 Pin Assignment

The following table shows the GBUS pin assignments. “Reserve” indicates a reserved pin. N/C indicates that a pin is not connected.

Table 4-3. GBUS Pin Assignment (1/2)

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
1	+12 V	2	+12 V	3	GND	4	+5 V
5	GADDR2	6	GADDR3	7	GADDR4	8	GADDR5
9	GADDR6	10	GADDR7	11	GND	12	+5 V
13	GADDR8	14	GADDR9	15	GADDR10	16	GADDR11
17	GADDR12	18	GADDR13	19	GADDR14	20	GADDR15
21	GND	22	+5 V	23	GADDR16	24	GADDR17
25	GADDR18	26	GADDR19	27	GADDR20	28	GADDR21
29	GADDR22	30	GADDR23	31	GND	32	+5 V
33	GADDR24	34	GADDR25	35	GADDR26	36	GADDR27
37	GADDR28	38	GADDR29	39	GADDR30	40	GADDR31
41	GND	42	+5 V	43	GBEN3-	44	GBEN2-
45	GBEN1-	46	GBEN0-	47	GND	48	+5 V
49	GDATA31	50	GDATA30	51	GDATA29	52	GDATA28
53	GDATA27	54	GDATA26	55	GDATA25	56	GDATA24
57	GND	58	+5 V	59	GDATA23	60	GDATA22
61	GDATA21	62	GDATA20	63	GDATA19	64	GDATA18
65	GDATA17	66	GDATA16	67	GND	68	+5 V
69	GDATA15	70	GDATA14	71	GDATA13	72	GDATA12
73	GDATA11	74	GDATA10	75	GDATA9	76	GDATA8
77	GND	78	+5 V	79	GDATA7	80	GDATA6
81	GDATA5	82	GDATA4	83	GDATA3	84	GDATA2
85	GDATA1	86	GDATA0	87	GND	88	+5 V
89	GND	90	GW/R-	91	GBTERM-	92	GREADY-
93	GRESETI-	94	GADS-	95	GBLAST-	96	GWAITI-
97	GND	98	GCLK	99	GND	100	+5 V
101	GCS0-	102	GCS1-	103	GCS2-	104	GCS3-
105	GCS4-	106	GCS5-	107	GCS6-	108	GCS7-
109	Reserve	110	Reserve	111	Reserve	112	Reserve
113	GRD-	114	GWR-	115	GND	116	+5 V
117	GHOLD-	118	GHLDA-	119	GBREQ-	120	N/C
121	GDMARQ0-	122	GDMARQ1-	123	GDMARQ2-	124	GDMARQ3-
125	GDMAAK0-	126	GDMAAK1-	127	GDMAAK2-	128	GDMAAK3-
129	Reserve	130	Reserve	131	Reserve	132	Reserve

Table 4-3. GBUS Pin Assignment (2/2)

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
133	GND	134	+5 V	135	GINTO0-	136	GINTO1-
137	GINTO2-	138	GINTO3-	139	GINTI0-	140	GINTI1-
141	GETC0	142	GETC1	143	GETC2	144	GETC3
145	GETC4	146	GETC5	147	GETC6	148	GETC7
149	Reserve	150	Reserve	151	GAHI_EN-	152	GMOTHER_DETECT-
153	GND	154	+5 V	155	GUSE_DIRECT_ACC-	156	GCLK_LOW-
157	GRESETO-	158	GBLOCK0-	159	GBLOCK1-	160	N/C
161	N/C	162	N/C	163	N/C	164	N/C
165	N/C	166	N/C	167	N/C	168	N/C
169	N/C	170	N/C	171	N/C	172	N/C
173	N/C	174	N/C	175	N/C	176	N/C
177	GND	178	+5 V	179	+12 V	180	+12 V

Remark The following connectors are used:
CPU board side connector: KEL Corporation 8817-180-170L
Motherboard side connector (straight): KEL Corporation 8807-180-170S
Motherboard side connector (right angle): KEL Corporation 8807-180-170L

4.4 Handling of Unused Pins

Signals that are not input to the GBUS motherboard are pulled up or down on the motherboard and can be unconnected on the CPU board. Signals that can be unconnected and the processing performed on the motherboard for those pins are shown below.

Table 4-4. Signals That Can Be Unconnected to CPU Board

Signal Name	Handling
GADDR[31:26]	If GADDR[31:26] are not used, GADDR[31:26] can be unconnected by making the GAHI_EN- signal high or by disconnecting it. In this case, if the CPU is the bus master, all the bits of GADDR[31:26] are treated as 0 on the motherboard.
GWAITI-	Pull-up processing is performed.
GBLAST-	Pull-up processing is performed.
GBTERM-	Pull-up processing is performed.
GCS-[7:0]	Pull-up processing is performed.
GHLDA-	Pull-up processing is performed.
GBREQ-	Pull-up processing is performed.
GDMAAK-[3:0]	Pull-up processing is performed.
GINTI-[1:0]	Pull-up processing is performed.
GAHI_EN-	Pull-up processing is performed.
GUSE_DIRECT_ACC-	Pull-up processing is performed.
GCLK_LOW-	Pull-up processing is performed.
GBLOCK-[1:0]	Pull-up processing is performed.

4.5 Assigning GCS-[7:0]

The following table shows the allocation of the chip select signals (GCS-[7:0]). All of the spaces can be accessed in a burst cycle. The meanings of the items in Table 4-5 are as follows.

A space marked “I/O” under the heading “Recommended Space” means that, if the CPU has an I/O space, it is recommended that the space be allocated as an I/O space. “Minimum Range” indicates that the CPU board must allocate at least the indicated area for the corresponding chip select space. “Maximum Range” indicates that, if the CPU board has an extra address range, addresses can be allocated for the indicated range.

Table 4-5. Chip Select Signal (GCS-[7:0]) Assignment

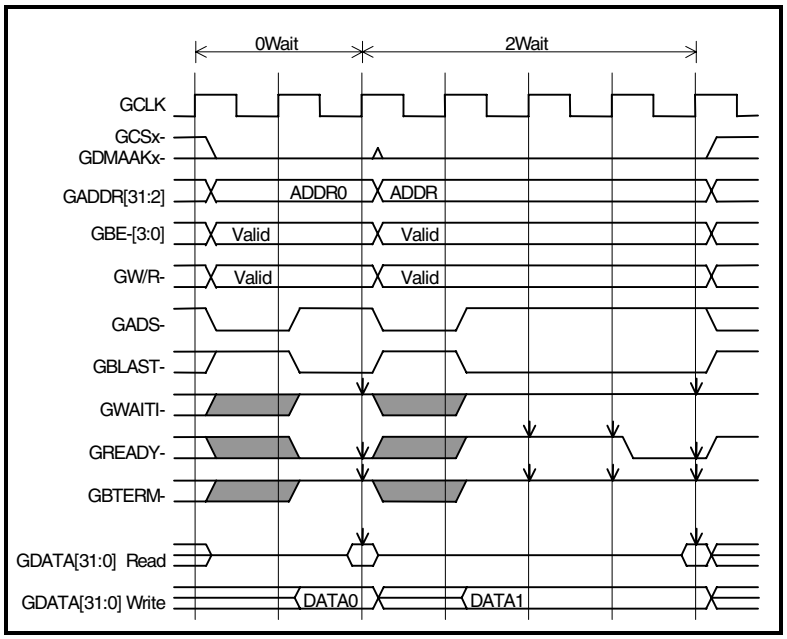
Signal Name	Recommended Space	Minimum Range	Maximum Range	Remark
GCS0-	Memory	1 MB	–	Bus lock possible with GLOCK0-
GCS1-	Memory	2 MB	–	Because a flash memory is allocated to this space on the motherboard, the program must be able to be booted from this space, instead of from UV-EPROM on the CPU board, via a switch.
GCS2-	I/O	64 KB	–	–
GCS3-	Memory	64 KB	16 MB	–
GCS4-	I/O	64 KB	16 MB	–
GCS5-	Memory	1 MB	2 GB	Bus lock possible with GLOCK1-
GCS6-	I/O	512 bytes		–
GCS7-	I/O	64 KB	2 GB	Bus lock possible with GLOCK1-

4.6 Bus Cycle

4.6.1 Single cycle

The following chart shows the single cycle when GBWAITI- and GBTERM- are always inactive and the CPU board is the bus master. If the motherboard is the bus master, the GCSx- , GDMAAK- , and GWAITI- signals are not used.

Figure 4-1. Single Cycle



4.6.2 Burst cycle

The following rules apply to a burst cycle.

The addresses in the burst cycle can be in any sequence allowed by the GBUS specifications. However, the address sequence may be specified according to what is to be accessed.

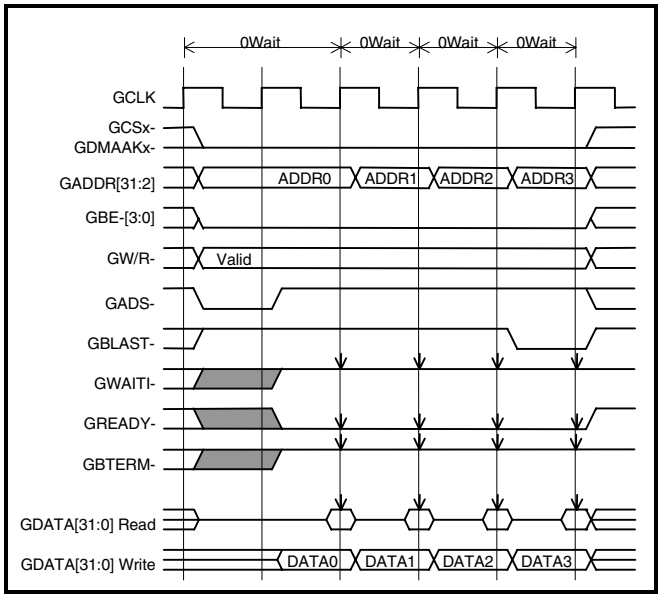
In a burst cycle, all of GBE-[3:0] must be active.

The number of bursts (the number of micro cycles) is not limited. If the target of the access limits the number of bursts, use the GBTERM- signal (see **4.6.4 GBTERM-**) to request canceling of the burst.

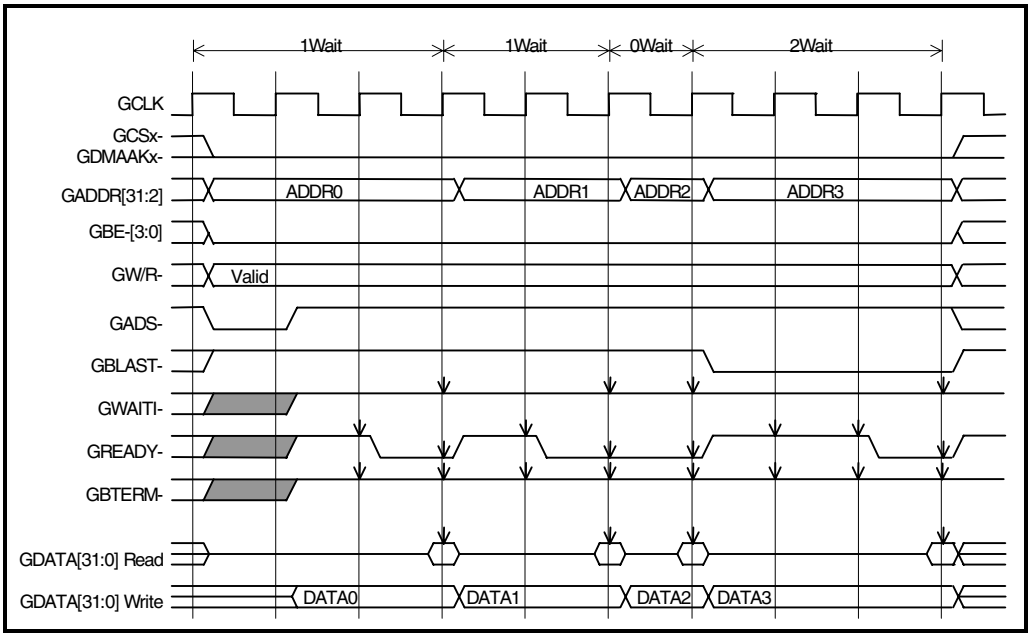
The following charts show the burst cycle when GBWAITI- and GBTERM- are always inactive and the CPU board is the bus master. If the motherboard is the bus master, the GCSx- , GDMAAK- , and GWAITI- signals are not used.

Figure 4-2. Burst Cycle

(a) 0 waits



(b) 1 wait/2 waits



4.6.3 GWAITI-

The GWAITI- signal can be used as follows in a cycle in which the CPU board is the bus master.

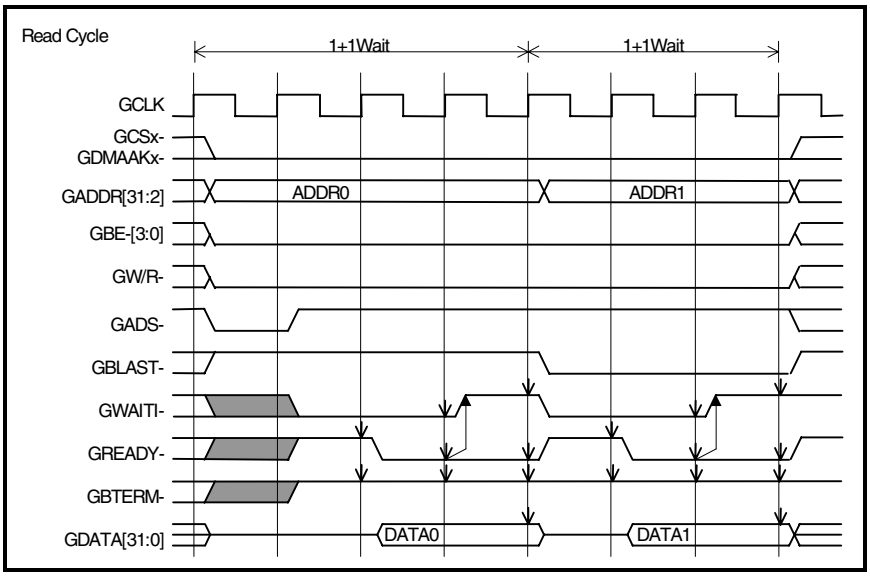
- To delay sampling of data by a specific number of clocks because the data cannot be sampled in the read cycle.
- To hold the target of an access by the specific number of clocks because data for the next micro cycle is not ready immediately after completion of the first micro cycle in the burst cycle of a write cycle.

In other words, the roles are switched between the read cycle and write cycle, but GREADY- and GWAITI- serve as data transmission ready and data reception ready signals.

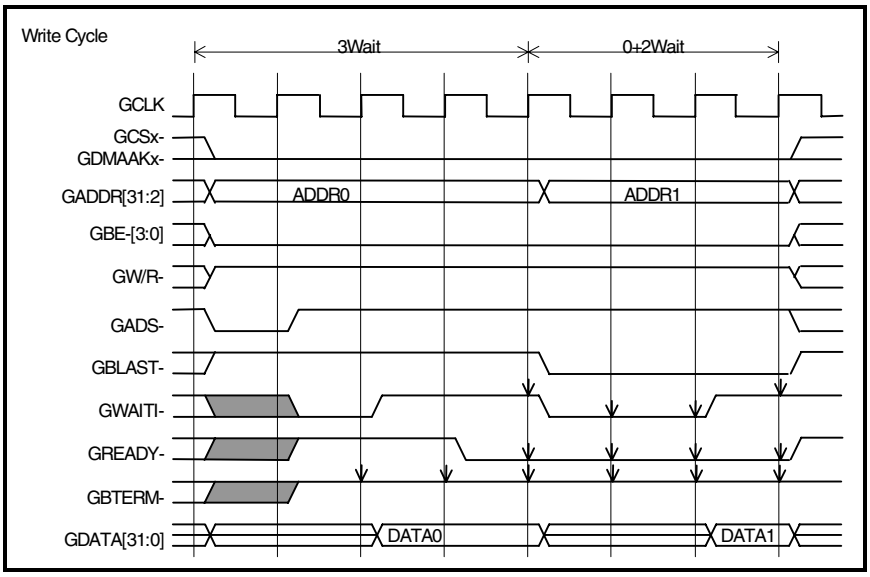
The following charts show that a wait cycle is inserted by the GWAITI- signal.

Figure 4-3. Wait Insertion by GWAITI- Signal

(a) Read cycle



(b) Write cycle



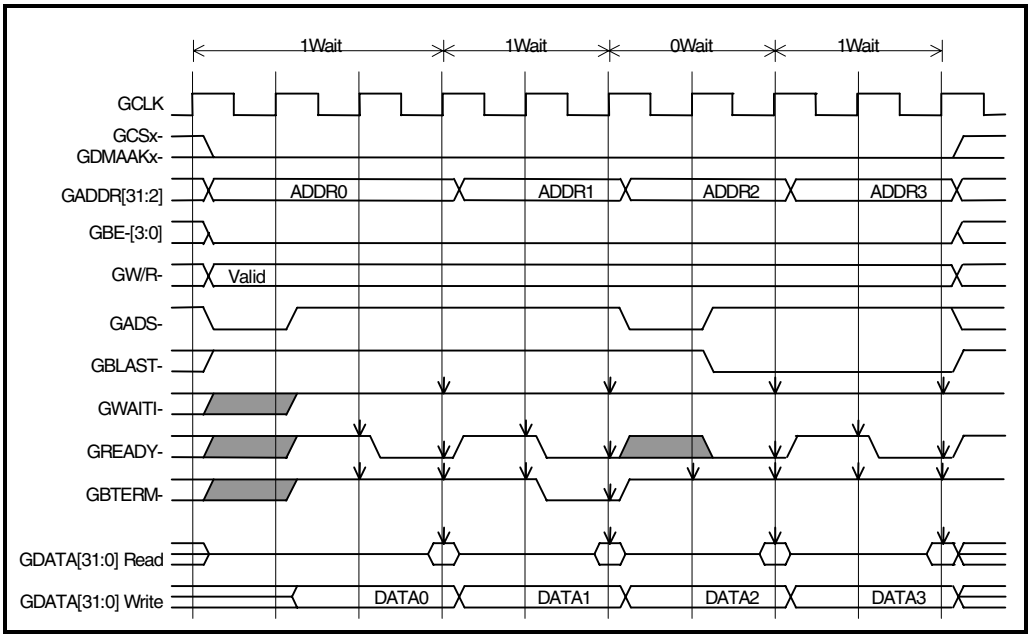
4.6.4 GBTERM-

If both the GBTERM- signal and GREADY- signal become active at the same time, the bus master completes the bus cycle after the current micro cycle ends, and then starts the burst cycle again by asserting GADS-.

The GBTERM- signal is asserted if the target of the access does not support burst cycles or accesses are made for more than the supported number of bursts. Asserting only the GBTERM- signal without asserting the GREADY- signal is not allowed.

The following chart shows the burst cycle suspended by the GBTERM- signal.

Figure 4-4. Burst Cycle Suspension by GBTERM- Signal



4.7 Timing

This chapter describes the timing of the NEC Electronics motherboard. The CPU board is designed to satisfy this timing.

4.7.1 Setup time

Figure 4-5. Setup Time

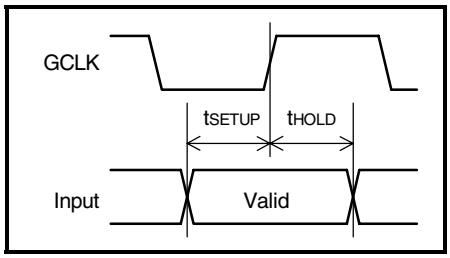


Table 4-6. Setup Time (Minimum)

Signal Name	t_{SETUP} (ns)	t_{HOLD} (ns)
GADDR[31:2]	12	0
GBEN-[3:0]	8	0
GDATA[31:0]	7	0
GADS-	14	0
GREADY-	9	1
GWAITI-	14	0
GBLAST-	8	0
GBTERM-	8	1
GW/R-	10	0
GCS-[7:0]	14	0
GBREQ-	15	0
GDMAAK-[3:0]	6	0
GLOCK-[1:0]	12	0

4.7.2 Delay time

Figure 4-6. Delay Time

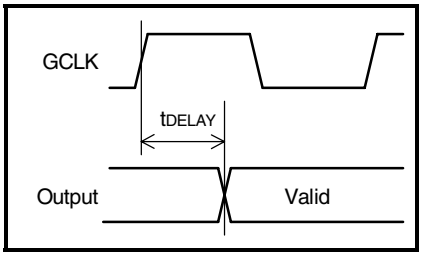


Table 4-7. Delay Time (Maximum)

Signal Name	$T_{DELAY\ (ns)}$
GADDR[31:2]	21
GBEN-[3:0]	17
GDATA[31:0]	21
GADS-	15
GREADY-	15
GBLAST-	17
GBTERM-	16
GW/R-	15

CHAPTER 5 HARDWARE REFERENCE

This chapter explains the hardware of the CPU board.

5.1 Memory Map

The CSn areas are explained below (n = 7 to 0).
Table 5-1 shows the memory space. Note that the GBUS space supports only the 64M mode.

(1) CS7

SRAM is mapped to this area. The bus size can be set to 16 or 32 bits by using SW2-4 (BSIZE16Z).

(2) CS6

This area is used in the GBUS spaces (GCS2, 4, 6, 7).

(3) CS5

This area is used as an I/O space. It has a space reserved for I/O on the CPU board. For the I/O map, refer to **5.5 I/O**.

(4) CS4

SDRAM is mapped to this area. The bus size can be set to 16 or 32 bits using SW2-4 (BSIZE16Z). If the bus size is set to 16 bits, the capacity of the area is 8 MB, and an 8 MB area starting from the lower side of the addresses can be used.

(5) CS3

This area is used in the GBUS spaces (GCS1, 3).

(6) CS2

This area is used in the GBUS space (GCS0).

(7) CS1

This area is used in the GBUS space (GCS5).

(8) CS0

In this area, flash memory is mapped to the areas other than the internal ROM space is allocated in single-chip mode 0/1. If single-chip mode 0/1 is set, an emulation memory is mapped to the internal ROM space (000000H to 0FFFFFH or 100000H to 1FFFFFH).
Turning ON SW2 and SW1 switches from the flash memory on the CPU board to the flash memory in the GBUS space (GCS1).

Table 5-1. Memory I/O Space (1/2)

Bank/Area 256M Mode	Address 256M Mode	CPU Board Resources	Bank/Area 64M Mode	Address 64M Mode	CS	GCS	GBUS Resources
Bank 15 2 MB	FFFFFFFH to FE00000H	Unused	Bank 15 2 MB	3FFFFFFH	CS6	–	–
				3E00000H			
Bank 14 2 MB	FDFFFFFH to FD00000H	Access prohibited	Bank 14 2 MB	3DFFFFFH to 3D00000H	CS7	–	–
	FCFFFFFH to FC00000H	SRAM (1 MB)		3CFFFFFH to 3C00000H			
Bank 13 2 MB	FBFFFFFH to FA00000H	Unused	Bank 13 2 MB	3BFFFFFH to 3A00000H	CS5	–	–
Bank 12 2 MB	F9FFFFFH to F900000H		Bank 12 2 MB	39FFFFFH to 3900000H			
	F8FFFFFH to F800000H	On-board I/O		38FFFFFH to 3800000H			
Area 3 56 MB	F7FFFFFH to F600000H	GBUS used area	Bank 11 4 MB	37FFFFFH to 3600000H	CS6	GCS4	EXT-bus: I/O space 2 MB
	F5FFFFFH to F190000H			35FFFFFH to 3400000H		–	–
	F18FFFFH to F180000H		Bank 10 4 MB	33FFFFFH to 3190000H		–	–
	F17FFFFH to F100000H			318FFFFH to 3180000H		GCS6	PCI-Cont register 64 KB
	F0FFFFFH to F010000H			317FFFFH to 3100000H		GCS2	I/O register 512 KB
	F00FFFFH to F000000H			30FFFFFH to 3010000H		–	–
	EFFFFFFH to C000000H			300FFFFH to 3000000H		GCS7	PCI bus space 64KB
Area 2 64 MB	BFFFFFFH to 9000000H	Access prohibited	Bank 9 8 MB	2FFFFFFH to 2800000H	CS4	–	–
	8FFFFFFH to 8000000H	SDRAM (16 MB)	Bank 8 8 MB	27FFFFFH to 2000000H			

Table 5-1. Memory I/O Space (2/2)

Bank/Area 256M Mode	Address 256M Mode	CPU Board Resources	Bank/Area 64M Mode	Address 64M Mode	CS	GCS	GBUS Resources
Area 1 64 MB	7FFFFFFH to 4000000H	Area used by GBUS	Bank 7 8 MB	1FFFFFFH to 1800000H	CS3	GCS3	EXT-bus: Memory space 8 MB
Area 0 56 MB	3FFFFFFH to 1800000H		Bank 6 8 MB	17FFFFFH to 1000000H		GCS1	Flash memory 8 MB
	17FFFFFH to 1000000H		Bank 5 4 MB	0FFFFFFH to 0C00000H	CS1	GCS5	PCI bus space 8 MB
	0FFFFFFH to 0800000H		Bank 4 4 MB	0BFFFFFH to 0800000H			
Bank 3 2 MB	07FFFFFH to 0600000H		Bank 3 2 MB	07FFFFFH to 0600000H	CS2	–	–
Bank 1 2 MB	05FFFFFH to 0400000H		Bank 2 2 MB	05FFFFFH to 0400000H		GCS0	Shared SRAM 2 MB
Bank 1 2 MB	03FFFFFH to 0200000H	Reserved	Bank 1 2 MB	03FFFFFH to 0200000H	CS0	GCS1	Flash memory 4 MB
Bank 0 2 MB	01FFFFFH to 0100000H	Single-chip mode 1: Internal ROM (1 MB) Single-chip mode 0 and ROMless mode: Flash memory (1 MB)	Bank 0 2 MB	01FFFFFH to 0100000H			
	00FFFFFH to 0000000H	Single-chip mode 0[Note]: Internal ROM (1 MB) Single-chip mode 1 and ROMless mode: Flash memory (1 MB)		00FFFFFH to 0000000H			

Note In single-chip mode 0, the last 4 bytes of the internal ROM emulation RAM cannot be used.
Mapping is performed in the following priority order.
Internal ROM > GBUS flash memory > CPU board flash memory

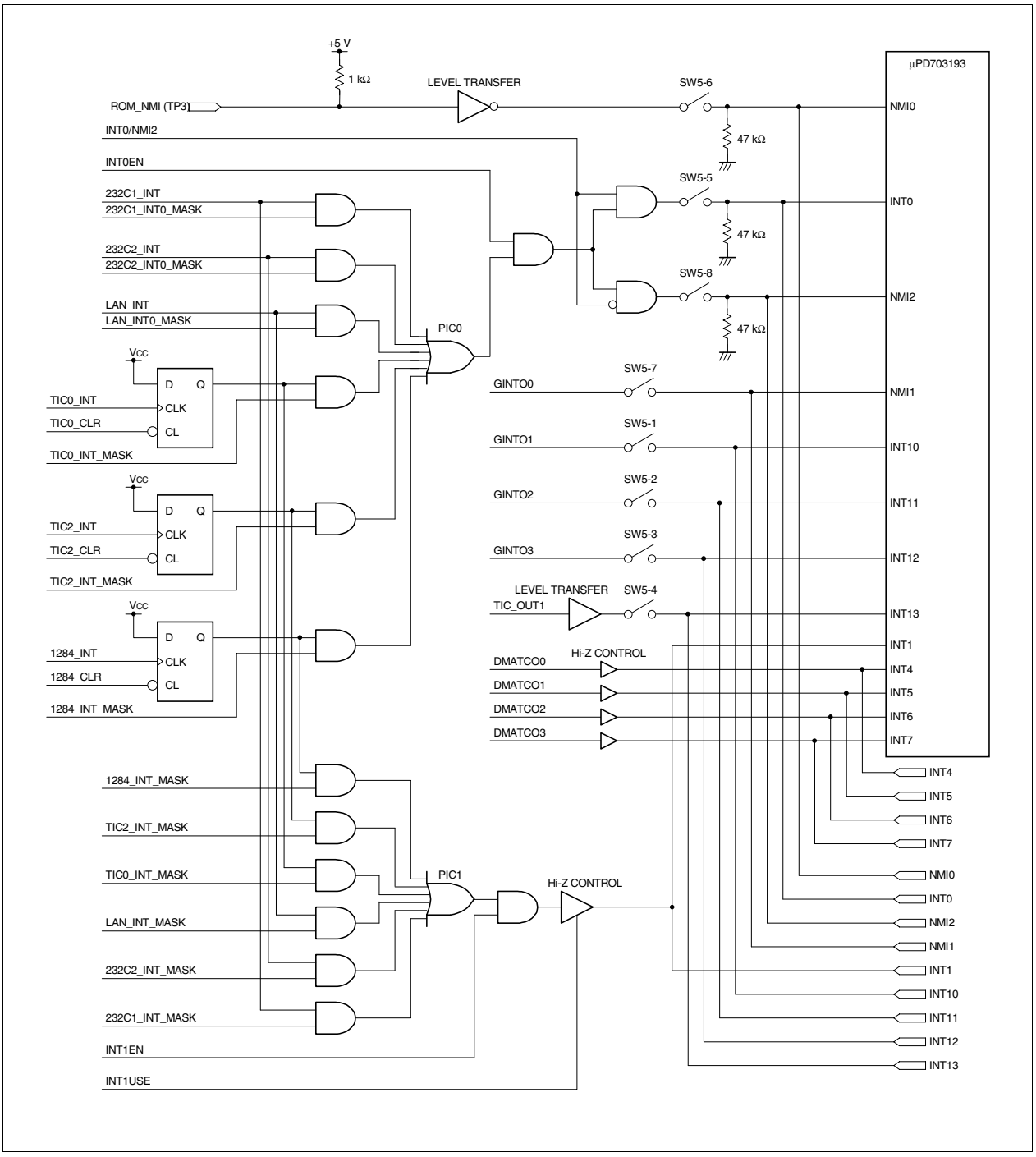
5.2 Interrupt List

The following table lists the interrupts used by the system and interrupt sources (signal names).

Table 5-2. Interrupt List

Type of Interrupt	Interrupt Source
NMI0	Interrupt request from ROM emulator
NMI1	Interrupt request from GINTO0
NMI2	Interrupt request from PIC0
INT0	Interrupt request from PIC0
INT1	Interrupt request from PIC1
INT4	Interrupt request from DMATCO0
INT5	Interrupt request from DMATCO1
INT6	Interrupt request from DMATCO2
INT7	Interrupt request from DMATCO3
INT10	Interrupt request from GINTO1
INT11	Interrupt request from GINTO2
INT12	Interrupt request from GINTO3
INT13	Timer 1 output

Figure 5-1. Interrupt Generation Logic



5.3 Setting of MEMC and μPD703193 Registers

This section describes the recommended set value of each register related to accessing the resources of the memory and I/O. Set the system bus as indicated in Table 5-3 (note that some settings differ depending on the operation mode and clock of the μPD703193, and the setting of SW2-4 (BSIZE16Z)).

Table 5-3. Setting of MEMC and μPD703193 Registers

Register Name		Address	Set Value	Remark
BCT0		FFFFF480H	8888H	CS0 to 3: SRAM, I/O
BCT1		FFFF482H	888BH	CS4: SDRAM CS5 to 7: SRAM, I/O
DWC0	86 to 100 MHz	FFFF484H	1116H	CS0: 6 WAIT CS1 to 3: 1 WAIT
	50 to 85 MHz		1115H	CS0: 5 WAIT CS1 to 3: 1 WAIT
	Less than 50 MHz		1114H	CS0: 4 WAIT CS1 to 3: 1 WAIT
DWC1	86 to 100 MHz	FFFF486H	1161H	CS5: 6 WAIT CS4, 6, 7: 1 WAIT
	50 to 85 MHz		1151H	CS5: 5 WAIT CS4, 6, 7: 1 WAIT
	Less than 50 MHz		0141H	CS5: 6 WAIT CS4, 6: 1 WAIT CS7: 0 WAIT
VSWC		FFFF06EH	77H	–
BCC		FFFF488H	4401H	CS0, 5, 7: 1 WAIT CS1 to 4, 6: 0 WAIT
ASC		FFFF48AH	5D57H	CS0, 5: 3 WAIT CS1 to 4, 6, 7: 1 WAIT
BCP		FFFF48CH	00H	Normal bus cycle
CSC0		FFFF060H	CCC3H	–
CSC1		FFFF062H	CCD2H	–
BSC (VSB data bus width = 32 bits)	BSIZE16Z = OFF	FFFF066H	AAAAH	CS0 to 7: 32 bits
	BSIZE16Z = ON		69AAH	CS0 to 3, 5, 6: 32bits CS4, 7: 16 bits
BSC (VSB data bus width = 16 bits)	BSIZE16Z = OFF		9A55H	CS4, 5, 7: 32 bits CS0 to 3, 6: 16 bits
	BSIZE16Z = ON		5955H	CS5: 32 bits CS0 to 4, 6, 7: 16 bits
BEC		FFFF068H	0000H	CS0 to 7: Little endian
SCR4	BSIZE16Z = OFF	FFFF4B0H	20A4H	SDRAM (LTM = 2, BCW = 2, SS0 = 2 bits, RAW = 12 bits, SAW = 8 bits)
	BSIZE16Z = ON		2094H	SDRAM (LTM = 2, BCW = 2, SS0 = 1 bit, RAW = 12 bits, SAW = 8 bits)
RFS4	100 to 50 MHz	FFFF4B2H	8018H	50 MHz (refresh interval: 15.36 μs)
	49 to 25 MHz		800CH	25 MHz (refresh interval: 15.36 μs)
	Less 25 MHz		8000H	2.5 MHz (refresh interval: 12.8 ms)
RSZ		FFFF7FCH	40H	Internal RAM = 60 KB Internal ROM interleave mode
DCC[Note]		FFFF078H	0000H	Data cache prohibited
CSZ		FFFF7FEH	00H	8 KB 2-way set associative
BHC[Note]		FFFF06AH	0000H	Cache prohibited

Note The internal RAM and data cache cannot be used at the same time.

5.4 Memory

The CPU board has SDRAM, SRAM, flash memory, and internal ROM as on-board memory resources. This section explains these memories.

5.4.1 SDRAM (CS4 area)

Two SDRAMs of 1 Mword × 16 bits × 4 banks are provided and a total capacity of 16 MB is available. The data bus width can be selected from 16 bits or 32 bits, depending on the set value of SW2-4 (BSIZE16Z). If the 16-bit bus width is used, the memory capacity is halved and only the lower 8 MB can be used.

5.4.2 SRAM (CS7 area)

Two SRAMs of 256 Kwords × 16 bits are provided and a total capacity of 1 MB is available.

If the bus clock exceeds 33 MHz, the SRAM can be accessed with 1 wait state; otherwise it can be accessed with 0 wait states.

The data bus width can be selected from 16 bits or 32 bits, depending on the set value of SW2-4 (BSIZE16Z). The memory capacity is the same regardless of whether a 16-bit or 32-bit bus width is selected.

5.4.3 Flash memory (CS0 area)

One MBM29LV160T (Fujitsu flash memory (1 Mword × 16 bits, top boot type)) or equivalent is provided, and a capacity of 2 MB is available.

To rewrite the contents of the flash memory, set the CS0 space in the 16-bit bus mode by using the BSC register (refer to the document of the flash memory to be used).

The flash memory can be read regardless of whether the μPD703193 is in the 16-bit bus mode or 32-bit bus mode. In the 32-bit bus mode, the 16-bit flash memory is read twice

When the flash memory is accessed, a wait time of about 150 ns is automatically inserted. In the 32-bit bus mode, however, the wait time is doubled because the memory is read twice

When the ROM emulator is used, the flash memory cannot be used because the emulator is mapped to the same addresses as the flash memory.

5.4.4 Internal ROM

An emulation memory that can be fetched in the same access time as the internal ROM is mapped to the internal ROM area, and the program stored in the internal ROM can be executed without having to modify the addresses.

The capacity of the emulation memory is 1 MB. Usually, the emulation memory is read-only. Data can be written to this memory only if it is downloaded from the debugger. This can be done, however, only if the debugger has an internal ROM download function (refer to the user's manual of the debugger to be used).

5.5 I/O

The CPU board has a serial/parallel controller (TL16PIR552), timer (μPD71054), LEDs, and switches as on-board I/O devices. This section explains these devices.

Table 5-4 lists the I/Os (the addresses shown in this table are in the 64 MB mode. Read "38xxxxxH" as "F8xxxxxH" in the 256 MB mode).

When the I/O is accessed, wait time (about 140 ns) is automatically inserted.

Table 5-4. I/O List (1/2)

Address	I/O		Bit Width	Read/Write	
				Read	Write
3800000H	SW1		8 bits	√	–
3801000H	SW2		8 bits	√	–
3802000H	7SEG-LED		32 bits	–	√
3804000H	PIC	INT_MASK	8 bits	√	√
3804010H		INT_STATUS	8 bits	√	√
3804020H		INT_ENABLE	8 bits	√	√
3807000H	RS232C_1	RBR/DLL	8 bits	√	√
		THR/DLL	8 bits	√	√
3807010H		IER/DLM	8 bits	√	√
3807020H		IIR	8 bits	√	√
		FCR	8 bits	√	√
3807030H		LCR	8 bits	√	√
3807040H		MCR	8 bits	√	√
3807050H		LSR	8 bits	√	√
3807060H		MSR	8 bits	√	√
3807070H		SCR	8 bits	√	√
3808000H	TIC	Counter #0	8 bits	√	√
3808010H		Counter #1	8 bits	√	√
3808020H		Counter #2	8 bits	√	√
3808030H		Control word register	8 bits	–	√
3809000H	SW6		8 bits	√	–
380A000H	OP_SW1		8 bits	√	–
380B000H	RS232C_2	RBR/DLL	8 bits	√	√
		THR/DLL	8 bits	√	√
380B010H		IER/DLM	8 bits	√	√
380B020H		IIR	8 bits	√	√
		FCR	8 bits	√	√
380B030H		LCR	8 bits	√	√
380B040H		MCR	8 bits	√	√
380B050H		LSR	8 bits	√	√

Table 5-4. I/O List (2/2)

Address	I/O		Bit Width	Read/Write	
				Read	Write
380B060H	RS232C_2	MSR	8 bits	√	√
380B070H		SCR	8 bits	√	√
380C000H	IEEE1284	DATA	8 bits	√	√
380C010H	EPP	ECPAFIFO	8 bits	√	√
380C020H	(PPCS)	DSR	8 bits	√	√
380C030H		DCR	8 bits	√	√
380C040H		EPPADDR	8 bits	√	√
380C050H		EPPDATA	8 bits	√	√
380C100H	IEEE1284	ECPDFIFO	8 bits	√	√
	ECP	PP DATA FIFO	8 bits	√	√
	(ECPCS)	TEST INFO	8 bits	√	√
		CNFGA	8 bits	√	√
380C110H		CNFGB	8 bits	√	√
380C120H		ECR	8 bits	√	√
380F000H	SW3		8 bits	√	–
3810000H	SW4		8 bits	√	–
3811000H	RESET		8 bits	–	√
3812000H	STAT		8 bits	√	–

5.5.1 SW1 (SW1 read port) … 3800000H (read-only)

This port is used to read the status of SW1. The data format is shown below.

Table 5-5. SW1 Read Port

Address	Data Bus								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
3800000H	SW1-8	SW1-7	SW1-6	SW1-5	SW1-4	SW1-3	SW1-2	SW1-1	0 = ON 1 = OFF

SW1-n corresponds to switch “n” of SW1 (n = 1 to 8).

When a switch corresponding to a bit is ON, “0” is read; when it is OFF, “1” is read.

Note, however, that when using a monitor ROM, the settings of SW1 have almost all been assigned. For the settings of the monitor ROM, refer to the manual of the monitor ROM.

5.5.2 SW2 (SW2 read port) … 3801000H (read-only)

This port is used to read the status of SW2. The data format is shown below.

Table 5-6. SW2 Read Port

Address	Data Bus								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
3801000H	SW2-8	SW2-7	SW2-6	SW2-5	SW2-4	SW2-3	SW2-2	SW2-1	0 = ON 1 = OFF

SW2 is used to select the operation of the hardware (for details, refer to **2.2.2 Switch 2 (SW2)**).

SW2-n corresponds to switch “n” of SW2 (n = 1 to 8).

When a switch corresponding to a bit is ON, “0” is read; when it is OFF, “1” is read.

5.5.3 SW3 (SW3 read port) … 380F000H (read-only)

This port is used to read the status of SW3. The data format is shown below.

Table 5-7. SW3 Read Port

Address	Data Bus								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
380F000H	0	SW3-7	SW3-6	SW3-5	SW3-4	SW3-3	SW3-2	SW3-1	0 = ON 1 = OFF

SW3 is used to select the operation of the board (for details, refer to **2.2.3 Switch 3 (SW3)**).

SW3-n corresponds to switch “n” of SW3 (n = 1 to 7).

When a switch corresponding to a bit is ON, “0” is read; when it is OFF, “1” is read.

5.5.4 SW4 (SW4 read port) … 3810000H (read-only)

This port is used to read the status of SW4. The data format is shown below.

Table 5-8. SW4 Read Port

Address	Data Bus								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
3810000H	SW4-8	SW4-7	SW4-6	SW4-5	SW4-4	SW4-3	SW4-2	SW4-1	0 = ON 1 = OFF

SW4 is used to select the operation of the board (for details, refer to **2.2.4 Switch 4 (SW4)**).

SW4-n corresponds to switch “n” of SW4 (n = 1 to 8).

When a switch corresponding to a bit is ON, “0” is read; when it is OFF, “1” is read.

5.5.5 SW6 (SW6 read port) … 3809000H (read-only)

This port is used to read the status of SW6. The data format is shown below.

Table 5-9. SW6 Read Port

Address	Data Bus								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
3809000H	SW6-8	SW6-7	SW6-6	SW6-5	SW6-4	SW6-3	SW6-2	SW6-1	0 = ON 1 = OFF

SW6 is used to select the operation of the μPD703193 and the VSB data bus size (for details, refer to **2.2.6 Switch 6 (SW6)**).

SW6-n corresponds to switch “n” of SW6 (n = 1 to 8).

When a switch corresponding to a bit is ON, “0” is read; when it is OFF, “1” is read.

5.5.6 OP_SW1 (OP_SW1 read port) … 380A000H (read-only)

This port is used to read the status of OP_SW1. The data format is shown below.

Table 5-10. OP_SW1 Read Port

Address	Data Bus								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
380A000H	OP_SW1-8	OP_SW1-7	OP_SW1-6	OP_SW1-5	OP_SW1-4	OP_SW1-3	OP_SW1-2	OP_SW1-1	0 = ON 1 = OFF

5.5.7 7SEG-LED (7SEG-LED display data output port) … 3802000H (write-only)

This port is used to set data to be displayed on the four 7SEG-LEDs. Table 4-11 shows the data format.

The corresponding segment lights when 0 is set to the corresponding bit.

Each segment (7SEGn-A to 7SEGn-G, and 7SEGn-DP) is located as follows (n = 1 to 4).

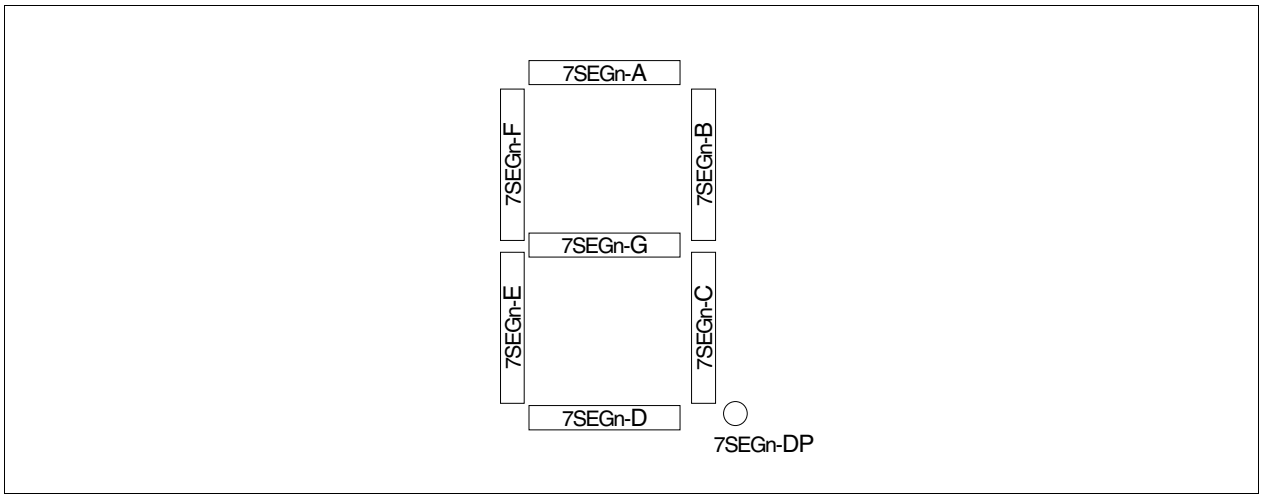


Table 5-11. 7SEG-LED Display Data Output Port

(a) 7SEG1

Address	Data Bus								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
3802000H	7SEG1-DP	7SEG1-G	7SEG1-F	7SEG1-E	7SEG1-D	7SEG1-C	7SEG1-B	7SEG1-A	0 = Lit 1 = Extinguished

(b) 7SEG2

Address	Data Bus								Description
	D15 (D7)	D14 (D6)	D13 (D5)	D12 (D4)	D11 (D3)	D10 (D2)	D9 (D1)	D8 (D0)	
3802000H (3802001H)	7SEG2-DP	7SEG2-G	7SEG2-F	7SEG2-E	7SEG2-D	7SEG2-C	7SEG2-B	7SEG2-A	0 = Lit 1 = Extinguished

(c) 7SEG3

Address	Data Bus								Description
	D23 (D7)	D22 (D6)	D21 (D5)	D20 (D4)	D19 (D3)	D18 (D2)	D17 (D1)	D16 (D0)	
3802000H (3802002H)	7SEG3-DP	7SEG3-G	7SEG3-F	7SEG3-E	7SEG3-D	7SEG3-C	7SEG3-B	7SEG3-A	0 = Lit 1 = Extinguished

(d) 7SEG4

Address	Data Bus								Description
	D31 (D7)	D30 (D6)	D29 (D5)	D28 (D4)	D27 (D3)	D26 (D2)	D25 (D1)	D24 (D0)	
3802000H (3802003H)	7SEG4-DP	7SEG4-G	7SEG4-F	7SEG4-E	7SEG4-D	7SEG4-C	7SEG4-B	7SEG4-A	0 = Lit 1 = Extinguished

5.5.8 PIC (interrupt controller) … 3804000H to 3804020H (read/write)

PIC supports the interrupts necessary for the operation of the monitor program. The following interrupts are connectable:

(1) Timer interrupt by OUT0 of TIC (μPD71054)
(2) Communication interrupt of RS-232-C and parallel (TL16PIR552) interfaces
(3) Interrupt of LAN (RTL8019AS)

Table 5-12. Registers of PIC

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
3804000H	INT0_MASK	×	×	×	IM04	IM03	IM02	IM01	IM00
3804008H	INT1_MASK	×	×	×	IM14	IM13	IM12	IM11	IM10
3804010H	INT_STATUS	×	×	×	IR4	IR3	IR2	IR1	IR0
3804020H	INT0_ENABLE	×	×	×	×	×	×	INT0/NMI2	INT0EN
3804028H	INT1_ENABLE	×	×	×	×	×	×	INT1USE	INT1EN

Remark ×: Undefined when read. Write 0 to this bit.

(1) INTm_MASK

This register is used to mask an input interrupt. The interrupt is enabled when the IMn bit is "1". If two or more bits are selected, the interrupt is asserted by the logical sum (OR) of the bits (n = 5 to 0). The default value is undefined.

The interrupt source assigned to each bit is shown below.

Table 5-13. Relationship Between Each Bit of INT_MASK Register and Corresponding Interrupt Source

Bit Name	Interrupt Source	Request Level
IMm0	Timer interrupt by OUT0 of TIC (μPD71054)	Edge
IMm1	Timer interrupt by OUT2 of TIC (μPD71054)	Edge
IMm2	Communication interrupt of RS232C_1 (TL16PIR)	Level
IMm3	Communication interrupt of RS232C_2 (TL16PIR)	Level
IMm4	Communication interrupt of 1284 (TL16PIR)	Edge

(2) INT_STATUS

This is an interrupt status register whose bits correspond to the bits of the INTm_MASK register. "1" can be read from a bit of this register if an interrupt request is issued, regardless of the mask status of the INTm_MASK register. To cancel (clear) an edge interrupt request, write "1" to the corresponding bit of this register (m = 1, 0). The default value is undefined.

Clear a level interrupt request using the device of the request source.

(3) INT0_ENABLE

This register is used to enable or disable all the interrupts.
When the board is reset, INT0_ENABLE is cleared to 0.

(a) INT0EN

This bit can be used to disable an interrupt by hardware. At this time, the interrupt pin goes low.

0: Masks INT0/NMI2 (default value).
1: Does not mask INT0/NMI2.

If two or more interrupt sources are generated, this bit is used to generate an edge for the interrupt signal to the μPD703193 when one interrupt servicing has been completed. If the interrupt input of the μPD703193 detects an edge, set this bit to 1 at the last step of the interrupt handler, and then clear it to 0. In this way, an interrupt that has been held pending will be acknowledged.

(b) INT0/NMI2

This bit selects the interrupt to be used for monitoring.

0: NMI2 used (default value).
1: INT0 used.

(4) INT_ENABLE

This register is used to enable or disable all the interrupts.
When the board is reset, INT1_ENABLE is cleared to 0.

(a) INT1EN

This bit can be used to disable an interrupt by hardware. At this time, the interrupt pin goes low.

0: Masks INT0/NMI2 (default value).
1: Does not mask INT0/NMI2.

If two or more interrupt sources are generated, this bit is used to generate an edge for the interrupt signal to the μPD703193 when one interrupt servicing has been completed. If the interrupt input of the μPD703193 detects the edge, set this bit to 1 at the last step of the interrupt handler, and then clear it to 0. In this way, an interrupt that has been held pending will be acknowledged.

(b) INT1USE

This bit enables output to INT1.

0: Sets output to INT1 to Hi-Z (default value).
1: INT1 used.

5.5.9 TIC (timer/counter) … 3808000H to 3808030FH

The μPD71054 is used as TIC. The μPD71054 has three channels of timers/counters that generate interrupts.

Each register of TIC is allocated as shown below.

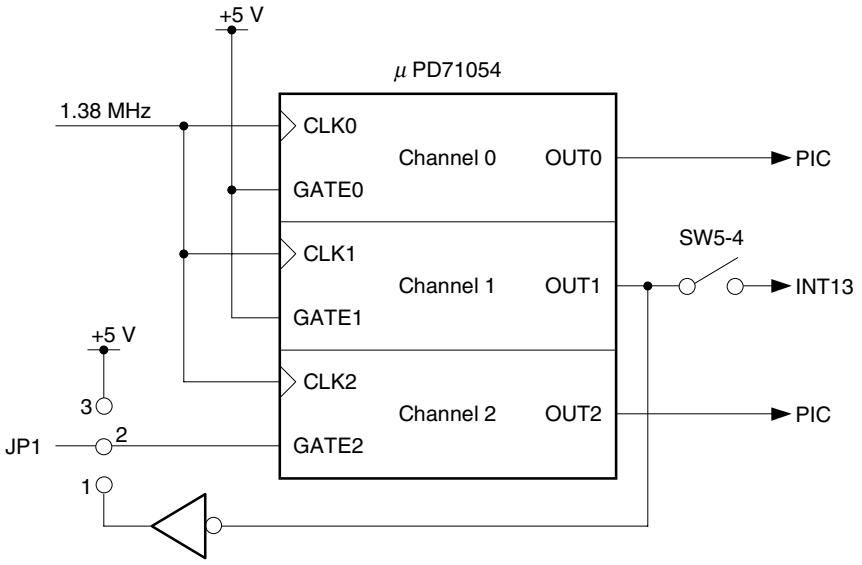
Table 5-14. Registers of TIC

Address	Read	Write
3808000H	Counter#0	Counter#0
3808010H	Counter#1	Counter#1
3808020H	Counter#2	Counter#2
3808030H	–	Control word register

The channels of TIC are connected as shown in Figure 5-2.

Channels 0 to 2 are used freely by the user program (channels 2 and 1 can be connected in cascade).

Figure 5-2. Connection of TIC Channels



Remark Example of use

Channel 0: Mode 2 (rate generator)

Channel 1: Mode 2 (rate generator)

Channel 2: Mode 0 (down counter)

5.5.10 RS232C_1 (RS-232-C interface) … 3807000H to 3807070H

TL16PIR552 is used as the RS232C_1 interface. TL16PIR552 has one RS-232-C channel, a 16-character FIFO buffer for the transmission/reception block of RS232C_1, and a function to automatically control the RTS/CTS flow, so that it can suppress communication overrun errors using minimum interrupts.

The registers of TL16PIR552 are allocated as shown below (for the function of each register, refer to the document of TL16PIR552).

Table 5-15. Registers of TL16PIR552 (RS232C_1)

Address	Read	Write
3807000H	RBR/DLL	THR/DLL
3807010H	IER/DLM	IER/DLM
3807020H	IIR	FCR
3807030H	LCR	LCR
3807040H	MCR	MCR
3807050H	LSR	LSR
3807060H	MSR	MSR
3807070H	SCR	SCR

A clock of 22.118 MHz is connected to the XIN input of TL16PIR552.

RS232C_1 is connected to the RS-232-C1 connector.

TL16PIR552 is reset when the system is reset.

5.5.11 RS232C_2 (RS-232-C interface) … 380B000H to 380B070H

TL16PIR552 is used as the RS232C_2 interface. TL16PIR552 has one RS-232-C channel, a 16-character FIFO buffer for the transmission/reception block of RS232C_2, and a function to automatically control the RTS/CTS flow, so that it can suppress communication overrun errors using minimum interrupts.

The registers of TL16PIR552 are allocated as shown below (for the function of each register, refer to the document of TL16PIR552).

Table 5-16. Registers of TL16PIR552 (RS232C_2)

Address	Read	Write
380B000H	RBR/DLL	THR/DLL
380B010H	IER/DLM	IER/DLM
380B020H	IIR	FCR
380B030H	LCR	LCR
380B040H	MCR	MCR
380B050H	LSR	LSR
380B060H	MSR	MSR
380B070H	SCR	SCR

A clock of 22.118 MHz is connected to the XIN input of TL16PIR552.

RS232C_2 is connected to the RS-232-C2 connector.

TL16PIR552 is reset when the system is reset.

5.5.12 IEEE1284 (parallel interface) … 380C000H to 380C120H

Connect a 22.118 MHz clock to the XIN input of TL16PIR552.

For details, refer to the document of TL16PIR552.

Table 5-17. Registers of TL16PIR552 (IEEE1284)

(a) PPCS access

Address	Register Name
380C000H	DATA
380C010H	ECPAFIFO
380C020H	DSR
380C030H	DCR
380C040H	EPPADDR
380C050H	EPPDATA

(b) ECPCS access

Address	Register Name
380C100H	ECPDFIFO/PP DATA FIFO/TEST FIFO/CNFGA
380C110H	CNFGB
380C120H	ECR

5.5.13 RESET (software reset port) … 3811000H (write-only)

When A9 is written to 3811000H, a software reset is executed.

Table 5-18. Software Reset Port

Address	Data Bus							
	D7	D6	D5	D4	D3	D2	D1	D0
3811000H	1	0	1	0	1	0	0	1

5.5.14 STAT (connection status read port) … 3812000H (read-only)

This port is used to read the connection status of the base board and ADP board, and the status of the READY pin of the flash memory. The data format is shown below.

Table 5-19. Connection Status Read Port

Address	Data Bus							
	D7	D6	D5	D4	D3	D2	D1	D0
3812000H	0	0	ON MOTHER BOARD	ON GBUS BOARD	x	x	x	USER FLASH READY

D5: “0” when motherboard is connected, “1” when motherboard is not connected

D4: “0” when GBUS board is connected, “1” when GBUS board is not connected

D0: The status of the READY pin of the flash memory can be read (a pull-up resistor is connected to the READY pin).

CHAPTER 6 PIN CONNECTIONS OF μPD703193

6.1 Pin List

(1/3)

Pin Name	Status
VPD15 to VPD0	47 kΩ pull-down
VPRETR	47 kΩ pull-down
VPDACT	10kΩ pull-up
VAREQ	47 kΩ pull-down
VBDI31 to VBDI0	47 kΩ pull-down
VMWAIT	47 kΩ pull-down
VMLAST	47 kΩ pull-down
VMAHLD	47 kΩ pull-down
STOPZ	10kΩ pull-up
HLDRQZ	10kΩ pull-up
SELFREF	47 kΩ pull-down
A25 to A0	Used as system bus
D31 to D0	Used as system bus (47 kΩ pull-down)
CSZ7, CSZ5, CSZ4, CSZ0	Used as system bus (47 kΩ pull-up)
WR3 to WR0	Used as system bus
RDZ	Used as system bus (10 kΩ pull-down)
WAITZ	Used as system bus (10 kΩ pull-up), only when CSZ5 or CSZ0 is accessed
BENZ3 to BENZ0	Used as system bus
SDCLK	Used as system bus
SDRASZ	Used as system bus
SDCASZ	Used as system bus
SDWEZ	Used as system bus
CKE	Used as system bus
DQMZ3 to DQMZ0	Used as system bus
NMI2 to NMI0	Used by system (47 kΩ pull-down), can be disconnected by SW
INT13, INT0	Used by system (47 kΩ pull-down), can be disconnected by SW
INT1	Used by system (47 kΩ pull-down), high-impedance output when system is not used
INT63 to INT14, INT12 to INT2	47 kΩ pull-down
RESETZ	Used by system (input to μPD703193 via reset integration circuit)
CLKIN	Clock supplied from clock socket
EXCLKIN	Clock supplied from clock socket
CKSEL1, CKSEL0	Selectable by SW
IFIMAEN	Selectable by SW

(2/3)

Pin Name	Status
MODE5 to MODE0	Selectable by SW
PWAIT2 to PWAIT0	Selectable by SW
IDMASTP	47 kΩ pull-down
DMARQ3 to DMARQ0	47 kΩ pull-down
IROMAA19 to IROMAA2	SRAM connection for internal ROM emulation (chip select validated by MODE5)
IROMAB19 to IROMAB3	SRAM connection for internal ROM emulation (chip select validated by MODE5)
IROMAZ31 to IROMAZ0	SRAM connection for internal ROM emulation (chip select validated by MODE5)
IROMBZ31 to IROMBZ0	SRAM connection for internal ROM emulation (chip select validated by MODE5)
IROMWEA	SRAM connection for internal ROM emulation (chip select validated by MODE5)
IROMWEB	SRAM connection for internal ROM emulation (chip select validated by MODE5)
IROMOEA	SRAM connection for internal ROM emulation (chip select validated by MODE5)
IROMOEB	SRAM connection for internal ROM emulation (chip select validated by MODE5)
IROMCLKA	SRAM connection for internal ROM emulation (chip select validated by MODE5)
IROMCLKB	SRAM connection for internal ROM emulation (chip select validated by MODE5)
DCK	Used for interface for N-Wire in-circuit emulator
DMS	Used for interface for N-Wire in-circuit emulator
DDI	Used for interface for N-Wire in-circuit emulator
DDO	Used for interface for N-Wire in-circuit emulator
DRSTZ	Used for interface for N-Wire in-circuit emulator
TRCCLK	Used for interface for N-Wire in-circuit emulator
TRCDATA3 to TRCDATA0	Used for interface for N-Wire in-circuit emulator
TRCEND	Used for interface for N-Wire in-circuit emulator
EVTTRG	Used for interface for N-Wire in-circuit emulator
DBINT	Used for interface for N-Wire in-circuit emulator
ECCENB	Fixed to high level
BISTTEB	Not used (use prohibited)
BISTTIN	Not used (use prohibited)
BISTTOUT2, BISTTOUT1	Not used (use prohibited)
PORT3 to PORT0	Not used (use prohibited)
TRG1, TRG0	Not used (use prohibited)
IDBR2 to IDBR0	Not used (use prohibited)
EVASTB	Not used (use prohibited)
EVDSTB	Not used (use prohibited)
EVAD15 to EVAD0	Not used (use prohibited)
EVLKRT	Not used (use prohibited)
EVIREL	Not used (use prohibited)
EVCLRIP	Not used (use prohibited)
EVINTAK	Not used (use prohibited)
EVINTRQ	Not used (use prohibited)

(3/3)

Pin Name	Status
EVINTLV6 to EVINTLV0	Not used (use prohibited)
ICACHEHIT	Not used (use prohibited)
ICACHEACK	Not used (use prohibited)
DCACHEHIT	Not used (use prohibited)
DCACHEACK	Not used (use prohibited)
TEST	Not used (use prohibited)
BUNRI	Not used (use prohibited)
TBI39 to TBI0	Not used (use prohibited)
TBO34 to TBO0	Not used (use prohibited)
VSA13 to VSA0	Not used (use prohibited)
VSSTZ	Not used (use prohibited)
VSBENZ1	Not used (use prohibited)
VSWRITE	Not used (use prohibited)
VSLOCK	Not used (use prohibited)
VSWAIT	Not used (use prohibited)
VSLAST	Not used (use prohibited)
VSAHLD	Not used (use prohibited)
VSSELPZ	Not used (use prohibited)
Other than above	Not processed

6.2 Reset

The μPD703193 is reset by the sources listed in Table 6-1.

These reset sources reset not only the μPD703193 but also function as a system reset for the entire CPU board.

Figure 6-1 shows an outline of the reset generation logic.

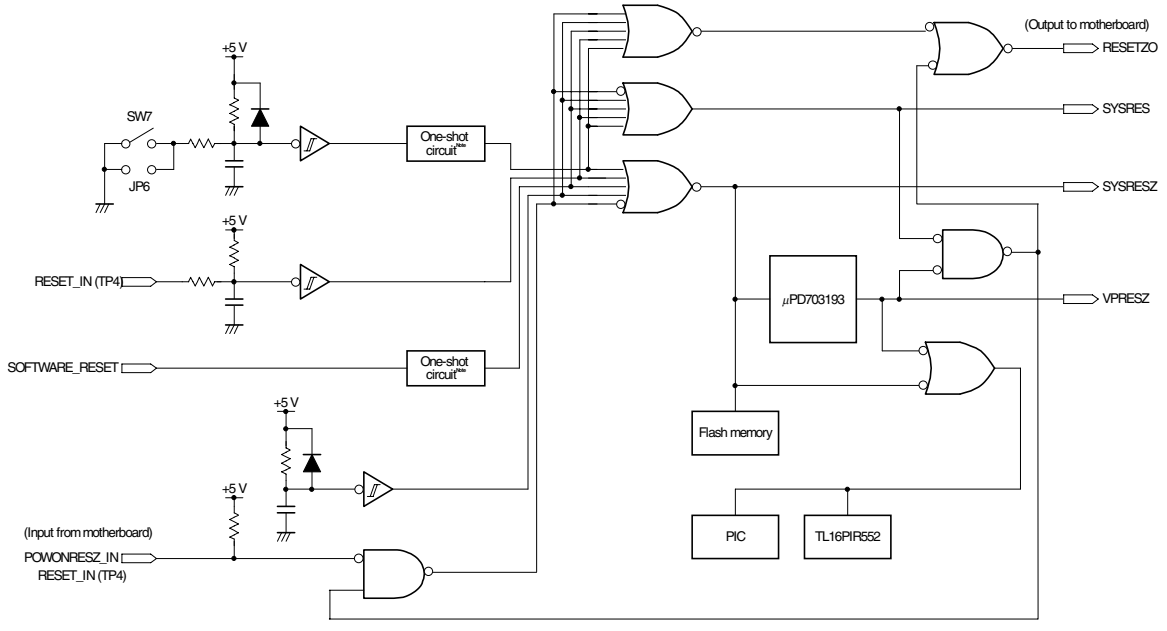
Table 6-1. Reset Source

Reset Source	Reset Signal		On-Board Device		
	SYSRESZ, SYSRES	VPRESZ	PIC, Flash Memory	TL16PIR552	RTL8019AS
Power-on reset (on power application)	Reset	Reset[Note 1]	Reset	Reset	Reset
Reset switch (SW7, JP6)	Reset	Reset[Note 1]	Reset	Reset	Reset
Software reset (I/O 3811000H)	Reset	Reset[Note 1]	Reset	Reset	Reset
Check pin reset input (TP4)	Reset	Reset[Note 1]	Reset	Reset	Reset
External reset input (POWONRESZ_IN pin)	Reset	Reset[Note 1]	Reset	Reset	Reset
Reset command by N-Wire in-circuit emulator	Reset[Note 2]	Reset	Reset[Note 2]	Reset	Reset

Notes 1. When the N-Wire in-circuit emulator is used, resetting the μPD703193 may be masked during a break by the debugger. In this case, the system will be completely reset. Press the reset switch and then execute the reset command on the debugger.

2. Reset is not executed when the motherboard is not connected.

Figure 6-1. Reset Generation Logic



Note This circuit outputs a one-shot pulse ( ) for about 10 μs from the falling edge.

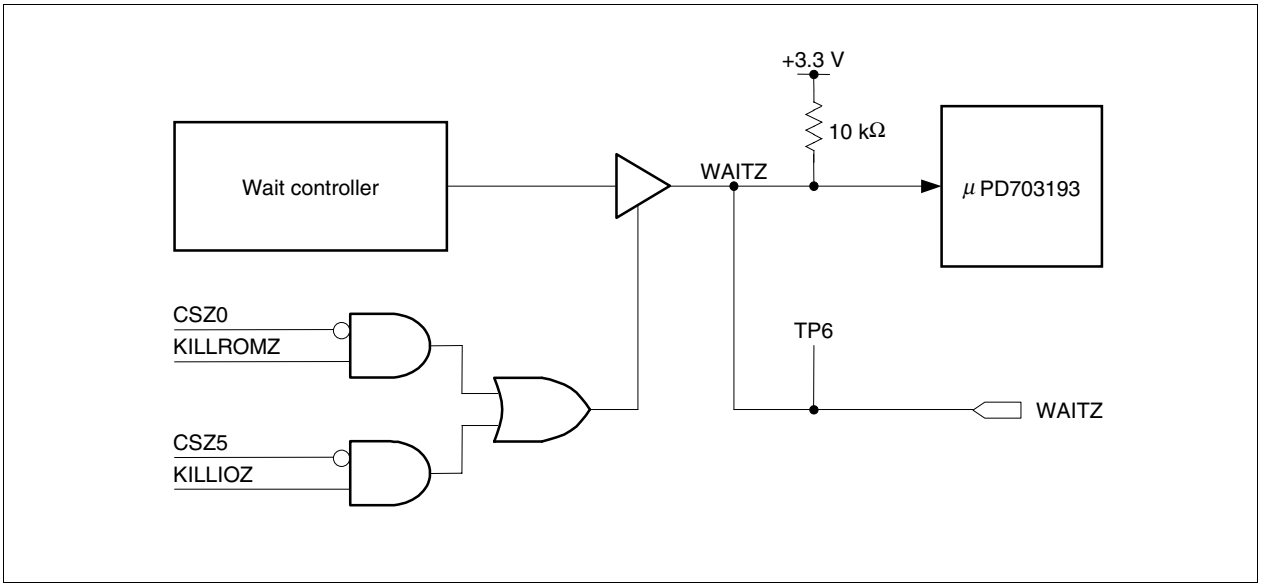
6.3 WAITZ Signal

The FPGA on the CPU board drives the WAITZ signal when the flash memory or on-board I/O of the CPU board is accessed. Because the WAITZ signal is output after RDZ and WRZ3 to WRZ0 have been asserted low, a wait state must be set by using the programmable function of the memory controller (MEMC) until the WAITZ signal is output.

For how to set the registers of the memory controller (MEMC), refer to **5.3 Setting of MEMC and μPD703193 Registers**.

Figure 6-2 shows the configuration of the WAITZ signal driver.

Figure 6-2. Configuration of WAITZ Signal Driver



APPENDIX A REGISTERS OF μPD703193

A.1 ROM/RAM Configuration Register (RSZ)

This is an 8-bit register that sets the RAM size and the interface mode of the VFB.
This register can be read or written in 8-bit units.

Figure A-1. ROM/RAM Configuration Register (RSZ)

	7	6	5	4	3	2	1	0	Address	After reset
RSZ	0	IRAMS2	IRAMS1	IRAMS0	0	0	0	ITLV	FFFFF7FCH	00H

Bit position	Bit name	Description
6 to 4	IRAMS2 to IRAMS0	Sets RAM size.
0	ITLV	Sets the interface mode of VFB (RAM/ROM emulation expansion pin for internal ROM emulation). 0: Interleave mode (When internal ROM emulation RAM is used: 256 KB can be used.) 1: Non-interleave mode (When internal ROM emulation RAM is used: 128 KB can be used.)

IRAMS2	IRAMS1	IRAMS0	RAM size	Mapping	
				64 MB mode	256 MB mode
0	0	0	4 KB	3FFE000H to 3FFF000H	FFFE000H to FFFF000H
0	0	1	12 KB	3FFC000H to 3FFF000H	FFFC000H to FFFF000H
0	1	0	28 KB	3FF8000H to 3FFF000H	FFF8000H to FFFF000H
1	0	0	60 KB	3FF0000H to 3FFF000H	FFF0000H to FFFF000H
Other than above			Reserved for future function expansion		

A.2 Cache Size Control Register (CSZ)

This is an 8-bit register that sets the size of the instruction cache and data cache.

This register can be read or written in 8-bit or 1-bit units.

Figure A-2. Cache Size Control Register (CSZ)

	7	6	5	4	3	2	1	0	Address	After reset
CSZ	0	0	DSZ	DTYP	0	0	ISZ1	ISZ0	FFFFF7FEH	00H

Bit position	Bit name	Description
5	DSZ	Sets the size of the data cache. 0: 8 KB, 2-way set associative 1: 4 KB direct mapping
4	DTYP	Selects the refill mode of the data cache. 0: Critical first mode 1: Sequential mode
1, 0	ISZ1, ISZ0	Sets the size of the instruction cache.

ISZ1	ISZ0	Instruction cache size
0	0	8 KB 2-way set associative
0	1	4 KB 2-way set associative
1	0	4 KB direct mapping[Note]
1	1	2 KB direct mapping[Note]

Note This is not supported by the currently released macros (NB85E212 and NB85E213).

APPENDIX B OPERATION MODES OF μPD703193

B.1 Operation Modes

The μPD703193 has the following three operation modes. The default value of the data bus width can be set in each mode (however, only 32-bit and 16-bit widths are selectable for the μPD703193). The mode can be specified by using the MODE3 to MODE0 pins.

- ROMless mode
- Single-chip mode 0
- Single-chip mode 1

The following functions can be enabled or disabled depending on the input level of the MODE4 and MODE5 pins:

- Memory controller (MEMC)
- ROM emulation expansion pin (to select RAM used as ROM area for VFB connection)

B.1.1 ROMless mode

In this mode, the program ROM area is mapped starting from address 0000000H of the external memory. Instructions cannot be fetched and data cannot be accessed in the ROM area for VFB connection.

ROMless mode can be either 64 MB or 256 MB mode.

B.1.2 Single-chip mode 0

In this mode, the ROM area for VFB connection can be accessed.

The ROM area is mapped from address 0000000H.

B.1.3 Single-chip mode 1

In this mode, the ROM area for VFB connection can be accessed.

The ROM area is mapped from address 0100000H.

B.2 Setting Operation Mode

B.2.1 Setting operation mode

The operation mode is set by the input levels of the MODE3 to MODE0 pins.

Table B-1. Setting of Operation Mode

MODE 3	MODE 2	MODE 1	MODE 0	Mode	VSB Data Bus Width
L	L	L	L	Single-chip mode 0 (64 MB mode) (ROM area is allocated from address 0000000H.)	16 bits
L	L	L	H	Single-chip mode 1 (64 MB mode) (ROM area is allocated from address 0100000H.)	16 bits
L	L	H	L	ROMless mode (64 MB mode)	16 bits
L	L	H	H	Setting prohibited	
L	H	L	L	Single-chip mode 0 (64 MB mode) (ROM area is allocated from address 0000000H.)	32 bits
L	H	L	H	Single-chip mode 1 (64 MB mode) (ROM area is allocated from address 0100000H.)	32 bits
L	H	H	L	ROMless mode (64 MB mode)	32 bits
L	H	H	H	Setting prohibited	
H	L	H	L	ROMless mode (256 MB mode)	16 bits
H	H	H	L	ROMless mode (256 MB mode)	32 bits
Other than above				(Reserved for future function expansion)	

Remark L: Low level input, H: High level input

B.2.2 Enabling/disabling operation of memory controller (MEMC)

The operation of the memory controller (MEMC) is enabled or disabled depending on the input level of the MODE4 pin.

Table B-2. Enabling/Disabling Operation of Memory Controller (MEMC)

MODE4	Memory Controller (MEMC)
High-level input	Enables operation.
Low-level input	Disables operation.

B.2.3 Selecting RAM used as ROM area for VFB connection

The RAM used as ROM area for VFB connection can be selected in accordance with the MODE5 pin input level. Function of the VSB/ROM emulation expansion pin can be selected in accordance with the MODE5 pin input level.

Table B-3. Selecting RAM Used as ROM Area for VFB Connection

MODE5	Function	Single-Chip Mode 0	Single-Chip Mode 1	Pin Function for VSB/ROM Emulation Expansion	ROMless Mode[Note]
High-level input	External memory connected to ROM emulation expansion pins is valid.	0000000H to 1 MB	0100000H to 1 MB	ROM emulation expansion	–
Low-level input	Internal ROM emulation RAM of μPD703193 is valid.	0100000H to 256 KB	0100000H to 256 KB	VSB	VFB is disabled. External memory is valid.

Note Input a low level to the MODE5 pin in the ROMless mode.