User Manual

TPS-1 Low-cost Solution Kit

TPS-1 Low-cost Solution Kit - Hardware Manual

YCONNECT-IT-TPS-1L

Renesas Electronics
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1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.

   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.

   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Preface

Readers This manual is intended for users who want to understand the functions of the concerned microcontrollers.

Purpose This manual presents the hardware manual for the concerned microcontrollers.

Organisation This system specification describes the following sections:

- Pin function
- CPU function
- Internal peripheral function

Module instances These microcontrollers may contain several instances of a dedicated module. In general the different instances of such modules are identified by the index “n”, where “n” counts from 0 to the number of instances minus one.

Legend Symbols and notation are used as follows:

• Weight in data notation:	Left is high order column, right is low order column
• Active low notation:	$\overline{xxx}$ (pin or signal name is over-scored) or /xxx (slash before signal name) or _xxx
• Memory map address:	High order at high stage and low order at low stage

Note Additional remark or tip

Caution Item deserving extra attention

Numeric notation

Binary:	xxxx or xxxB
Decimal:	xxxx
Hexadecimal	xxxxH or 0x xxxx

Numeric prefixes representing powers of 2 (address space, memory capacity):

K (kilo):	$2^{10} = 1024$
M (mega):	$2^{20} = 1024^2 = 1,048,576$
G (giga):	$2^{30} = 1024^3 = 1,073,741,824$

Register contents X, x = don’t care

Diagrams Block diagrams do not necessarily show the exact wiring in hardware but the functional structure. Timing diagrams are for functional explanation purposes only, without any relevance to the real hardware implementation.

How to Use This Manual

(1) Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions of the TPS-1 solution kit. It is intended for users evaluating the TPS-1. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual. The manual comprises an overview of the product; descriptions of the board hardware, configuration possibilities, connectors and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the TPS-1 Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	TPS-1 Datasheet	R19DS0069EJ0107
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description. Note: Refer to the application notes for details on using peripheral functions.	TPS-1 User Manual for Hardware	R19UH0081ED0110
User's manual for development environment	Operation instructions for hard- and software tools	TPS-1 Low-cost Solution Kit User Manual Hardware	R21UT0239ED0103 (this manual)
	Description of tool installation and initial set up	TPS-1 Low-cost Solution Kit – Getting started	R21UT0236ED0106 R21UT0237ED0105 R21UT0238ED0105 R21UT0243ED0104 R21UT0247ED0102

(2) List of Abbreviations and Acronyms

Abbreviation	Full Form
PHY	Physical Layer Device, Physical Layer Entity (acc. to. IEEE)
ASSP	Application Specific Standard Product
SMI	Serial Management Interface
MDI	Media Dependent Interface
GPIO	General Purpose Input/Output
POR	Power-on Reset
REG	Regulator
LED	Light Emitting Diode

(3) List of related Documents

Document Title	Description
R19UH0081ED0110	User Manual TPS-1 device
TPS_Update_Manual_EN.pdf	Application Note for TPS-1 firmware update
PROFINET Configurator - Quick Start Guide.pdf	Quick start guide for the PROFINET Configurator tool
R21UT0239ED0103	User Manual TPS-1 Low-cost Solution Kit (this manual)
R21UT0236ED0106	Getting started for TPS-1 Low-cost Solution Kit with RX630
R21UT0237ED0105	Getting started for TPS-1 Low-cost Solution Kit with RX231
R21UT0238ED0105	Getting started for TPS-1 Low-cost Solution Kit with Synergy S7G2
R21UT0247ED0102	Getting started for TPS-1 Low-cost Solution Kit with RX66T
R21UT0243ED0104	Getting Started for TPS-1 Low-cost Solution Kit in Parallel IO-Mode

Table of Contents

Chapter 1 Introduction

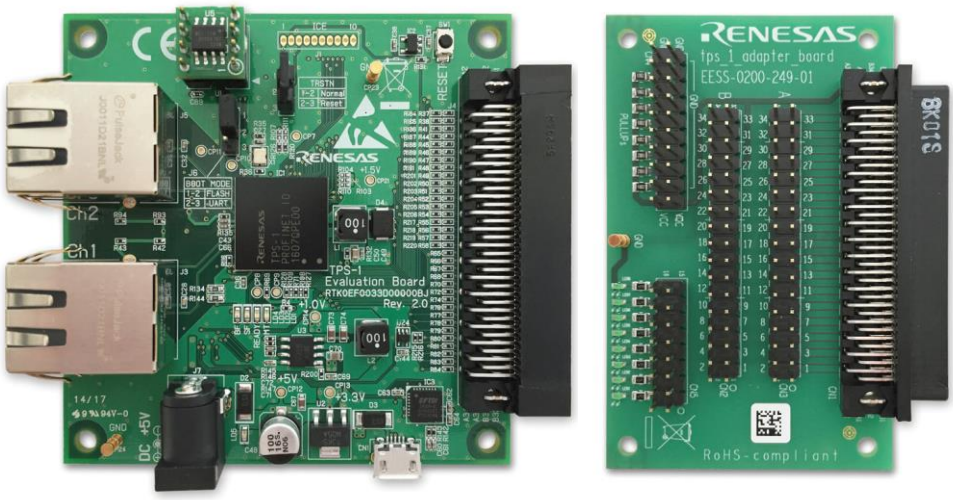
This manual describes the usage of the TPS-1 Low-cost Solution Kit. The intention of the TPS-1 Low-cost Solution Kit is to give customers a comfortable opportunity to evaluate the TPS-1 device with individual target host CPUs.

The TPS-1 Low-cost Solution Kit is made up of two boards shown in. The TPS-1 main board can be connected to an adapter board used to evaluate parallel I/O operation, as well as CPU parallel and serial host communication.

The boards are

1. TPS-1 board: dedicated board for PROFINET communication
2. Adapter board: Used to check operation of the parallel I/O interface and to connect individual host CPUs via serial (preferred) or parallel interface

Figure 1-1: Hardware boards included in the TPS-1 Low-cost Solution Kit



The board set does not include a CPU board. It is prepared for easy connection to customer's target CPU boards with a couple of wires plugged to the multi-pin connectors.

Usage examples for three different Renesas CPUs (RX630, RX66T, RX231 and Synergy S7G2) are described in separate <Getting started> documents. Connection to non-Renesas CPU boards is customer's responsibility but easily possible based on the functional descriptions given in this document.

Chapter 2 General Specifications

2.1 Electrical Specifications

This chapter describes the electrical specifications and performance of the board, in table format.

Table 2-1: Electrical specifications

Item		Specification
Power supply	Rated voltage	5V DC
	Current	app. 300 mA (only TPS-1 board)
	Status LED(PWR)	Red

2.2 Functional Specifications

Table 2-2: Functional specifications

Item	Specification		
Main LSI	TPS-1 (Operating frequency 100MHz)		
Interface	Ethernet	2ch	RJ-45(w/ built-in pulse-transformers)
	USB	1ch(Micro-B)	Virtual COM port(UART)
	JTAG	1ch	10-pin half pitch for ICE connection (not assembled)
	External I/F	68pins	FX2-68P-1.27DSL (71) by HIROSE
LED	Power	1bit	Red LED
	PROFINET	4bits	Red LED / Green LED/Yellow LED
	PHY link-up	1 each (2 ch)	Green LED
	PHY Activity	1 each (2 ch)	Yellow LED
Power supply	DC jack/USB	+5.0V	
Operating temperature	0 to +55℃		

2.3 Environmental Specifications and Weight

Table 2-3: Environmental Specifications

Item		Specification
Physical environment	Ambient operating temperature	0 to +55℃
	Ambient storage temperature	-25 to +70℃
	Ambient operating humidity	30 to 90%RH (no condensation)
	Ambient storage humidity	30 to 90%RH (no condensation)
	Usage atmosphere	No corrosive gas
Weight	Main board	50 g
	Adapter board	25 g
Dimensions	Main board	74mm(W)×74mm(D)×34mm(H)
	Adapter board	74mm(W)×74mm(D)×10mm(H)

2.4 Communication Specifications

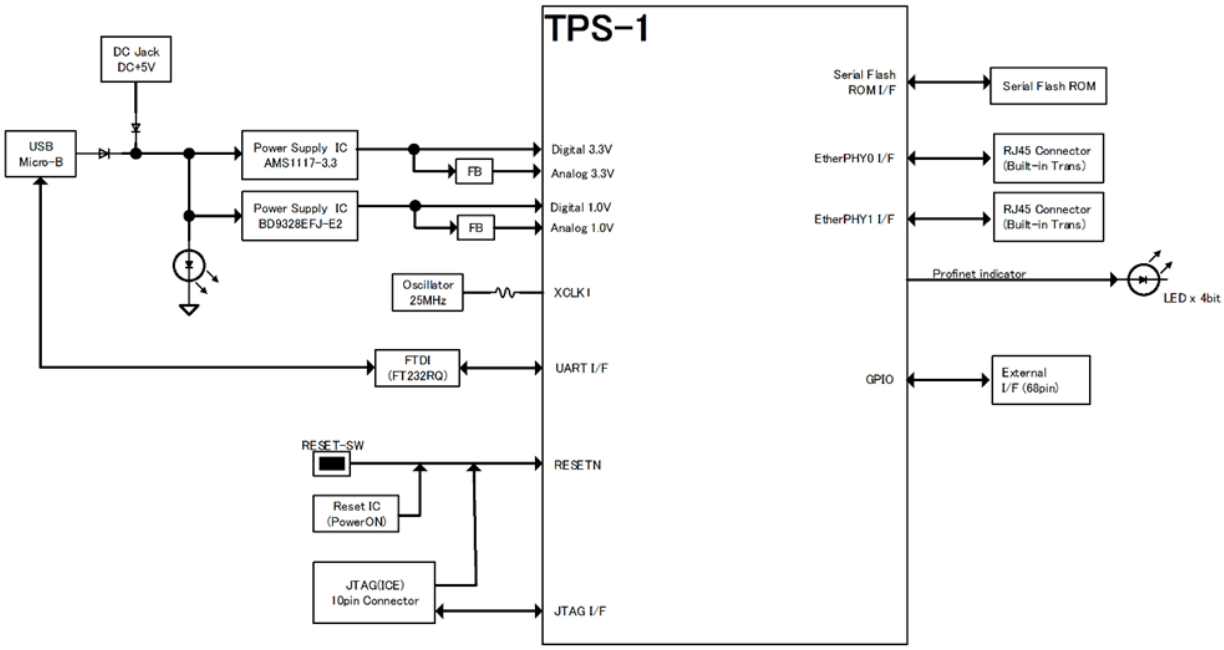
Item		Specification
Communication protocol		PROFINET IO
Communication control IC		TPS-1
PROFINET	PHY	Internal
	Communication system	IEEE802.3u(100base-TX)
	Insulation system	Pulse transformer insulation
	External interface	RJ45 x 2ch
Status LEDs		BF (red), SF (red), READY (green), MT (yellow) ACT0 (yellow), ACT1 (yellow), Link0 (green), Link1 (green)

Chapter 3 TPS-1 Board Blocks and Descriptions

Note: Some components of the circuit may have been replaced by functional equivalent components during assembly of the boards due to easier supply.

3.1 TPS-1 Board Block Diagram

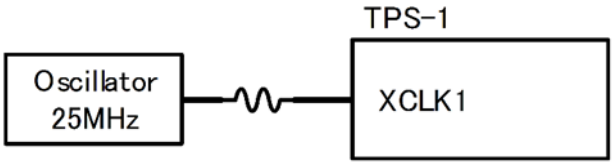
Figure 3-1: TPS-1 board block diagram



3.2 TPS-1 System Clock

An oscillator supplies 25 MHz as the TPS-1 standard clock. This clock is internally quadrupled to the system clock of 100 MHz.

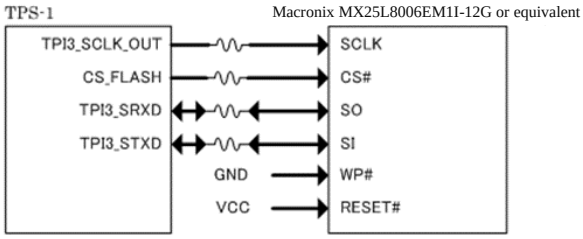
Figure 3-2: Clock circuit



3.3 External Memory (Serial Flash Memory)

A serial flash (1 Mbyte) memory is mounted using a small daughter PCB and a socket, storing the PROFINET IO stack and device information. Changes to other serial flash devices are made easy with these compatible sockets.

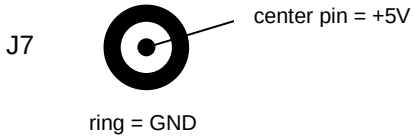
Figure 3-3: Serial flash memory



3.4 Power Supply

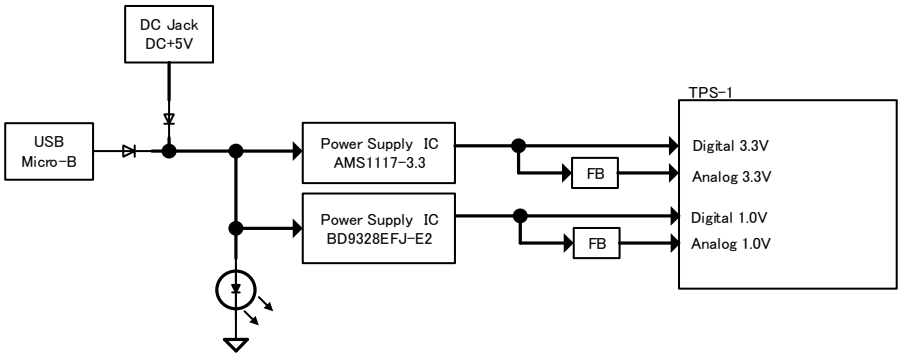
A 5V DC power supply can be input through the DC jack J7 to power the TPS-1 board; alternatively 5V can as be supplied with the USB micro-B connector CN1. The power LED LD5 (red) lights up when 5.0V is supplied. The DC jack is a HEC0470-01-630 from Hosiden and +5V is supplied on the center pin (see Figure 3-4).

Figure 3-4: Power supply connector J7 (board front view)



Caution: We urgently recommend checking polarity of any power supply before connecting it to J7.

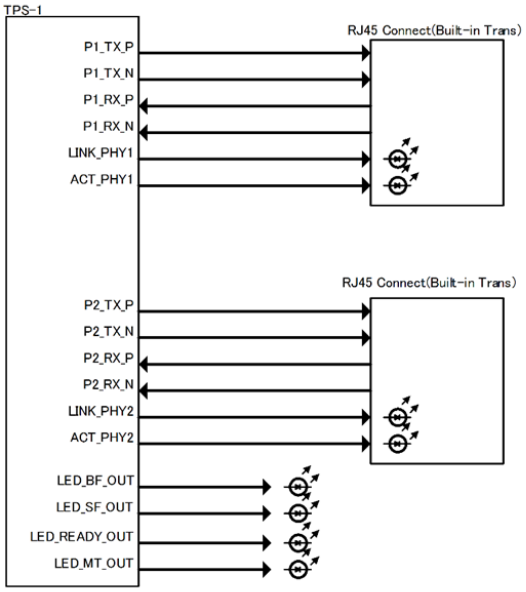
Figure 3-5: Power supply



3.5 PROFINET IO

PROFINET IO communication from the TPS-1 is carried out via a built-in PHY. The link and activity status are visualized with LEDs in the connectors, while the PROFINET status is indicated with four LEDs on the board.

Figure 3-6: PROFINET IO Communication



On the network side two standard RJ-45 connectors with integrated magnetics are provided. J0011D21BNL type from Pulse Engineering is used. The pin assignment on the connector is “uplink style” with TX on pins 1 and 2. Figure 3-7 illustrates the connector and Table 3-1 shows the detailed pin assignment.

Figure 3-7: Ethernet RJ-45 connector J3 and J5

Table 3-1: Pin assignment for Ethernet RJ-45 connectors J3 and J5

Pin No.	J3 and J5
1	Tx+
2	Tx-
3	Rx+
4	to GND via common 75Ω resistor
5	
6	Rx-
7	to GND via common 75Ω resistor
8	

3.6 UART connector CN1

A UART to USB conversion LSI (FT 232 RQ) is provided on the TPS-1 board and so the TPS-1 board performs asynchronous communication with a PC by connecting a USB connector. The board is equipped with a USB micro-B connector CN1. The pin assignment for this connector is illustrated in Table 3-2.

You can use a standard terminal emulation program like Teraterm to communicate with the TPS-1 via USB, allowing the TPS-1 to be configured or firmware updated.

Figure 3-8: UART

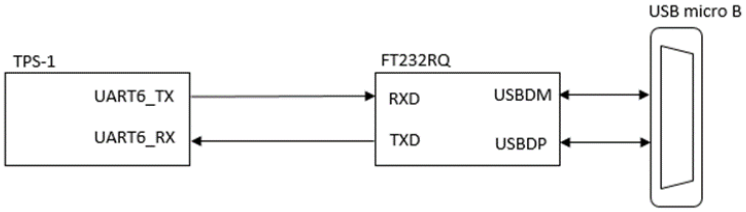
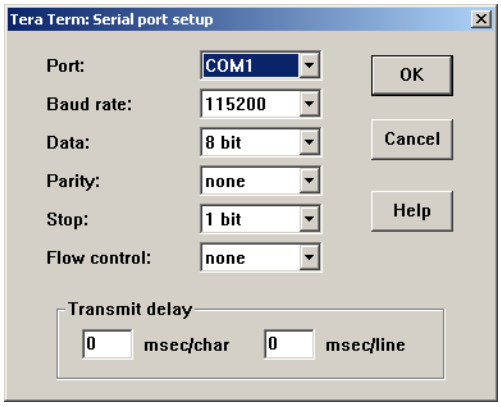


Table 3-2: UART connector CN1 pin assignment

Pin	Signal name
1	VBUS
2	USB_DM
3	USB_DP
4	GND
5	GND

The communication settings for the serial interface are fixed; Figure 3-9 shows how the parameters must be set in the TeraTerm terminal emulation program.

Figure 3-9: TeraTerm serial port setup



3.7 JTAG Connector J1

For the connection of a JTAG tool an access to the TPS-1 JTAG interface is provided through 10-pin connector J1. Note that this connector is not assembled, as access to the JTAG interface is normally not required. The connector used here, is a standard 1-row, 10-pin, 1.27mm pitch connector from HARWIN (M52-040023V1045); Table 3-3 shows the pin assignment

Table 3-3: JTAG connector J1 pin assignment

J1 Pin	Signal	J1 Pin	Signal
1	VDD33	6	TDO
2	RESETN	7	TMS
3	TRSTN	8	TDI_CB12
4	n. c.	9	GND
5	TCK	10	

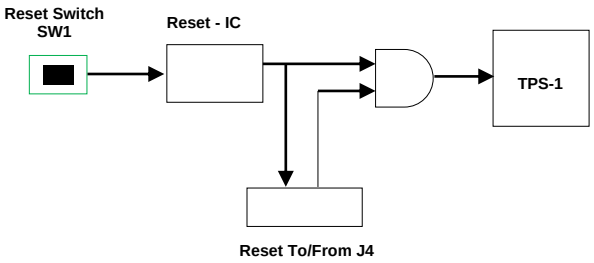
3.8 Reset Circuit

A Reset IC triggers a reset of TPS-1 when the power is turned on; additionally pressing the reset switch SW1 while the power is on resets the system through the reset IC.

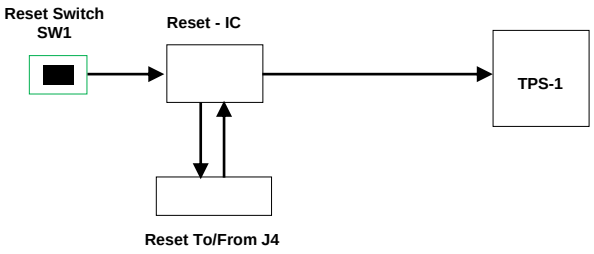
The output of the reset-IC is made available on connector J4 so that external hardware is aware that TPS-1 is reset. On the other hand the TPS-1 can as well be reset by the external hardware.

Figure 3-10: Reset circuit

Board Rev. 2.0



Board Rev. 3.0



3.9 LEDs

3.9.1 PROFINET indicators

Reference No.: LD1, LD2, LD3, LD4

Part Model No.: BR1111C-TR, PG1111C-11-TR, FY1111C-TR

These are red, green and yellow LEDs used to check PROFINET operations. They are directly connected to the respective TPS-1 outputs. Table 3-4 shows the details; shows the position of the LEDs on the TPS-1 board.

Table 3-4: PROFINET LED indicators

LED	Name	Description	Colour
LD4	BF	bus failure	red
LD3	SF	system failure	red
LD2	READY	device ready	green
LD1	MT	maintenance	yellow

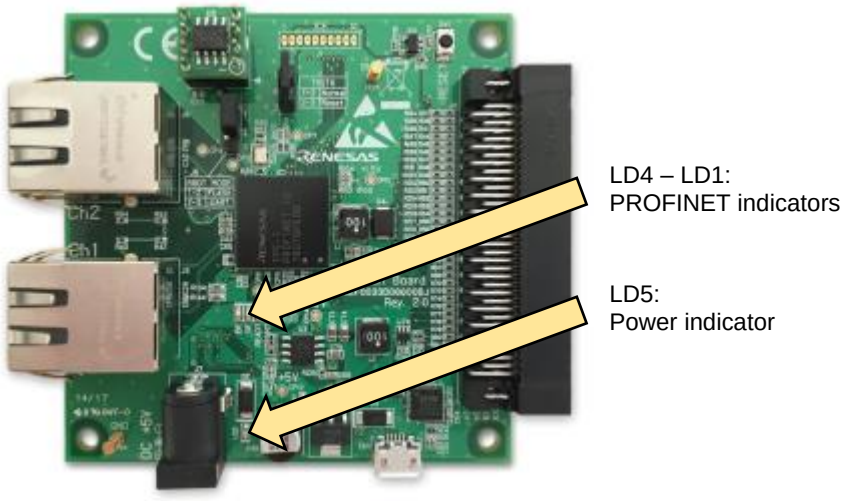
3.9.2 Power indicator

Reference No.: LD5

Part Model No.: BR1111C-TR

This is a single red LED used to monitor the power supply.

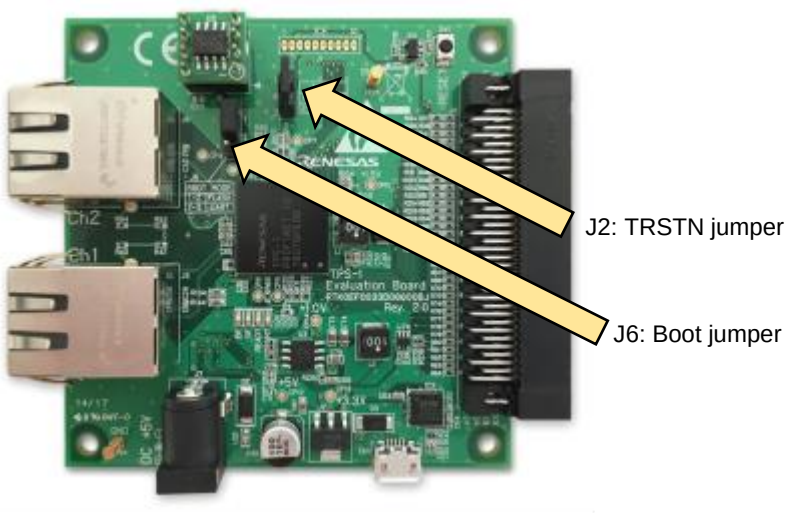
Figure 3-11: LED positions on TPS-1 main board



3.10 Configuration Jumpers

This section describes the configuration jumpers on the board that are shown in Figure 3-12:.

Figure 3-12: Configuration jumpers on TPS-1 main board



3.10.1 TRSTN jumperJ2

This is the switching jumper for the JTAG interface. Set Jumper J2 to position 2-3 because the JTAG interface is not used with this board. In position 2-3 the TRSTN input of the TPS-1 is permanently kept active and thus the JTAG interface is kept in reset.

Table 3-5: TRSTN jumper positions

J2 position	JTAG operation
1-2	JTAG interface used
2-3	JTAG interface unused (default)

3.10.2 Boot mode switching jumper J6

This is the switching jumper for the boot mode. Normally, this jumper is set to the Flash mode position (1-2). If there is no data written in the flash memory, the TPS-1 starts up in UART mode regardless of the boot mode setting.

Switch to the UART mode (position 2-3) in order to force TPS-1 to boot in UART mode even when there is data in the flash. This may be needed for example to erase the flash memory.

Table 3-6: Boot mode switching jumper positions

J6 position	Boot mode
1-2	Flash (default)
2-3	UART

3.11 Multi-board Interface J4

The 68-pin connector in Figure 3-13 enables connection to I/O and CPU boards. It provides access to all GPIO pins of the TPS-1, to reset, interrupt and watchdog signals, to the IRT synchronization signals and power (3.3V) and GND.

Connection can either be made with a customer board that carries the mating connector or – and this will be the usual method – with the adapter board that provides mechanically easy access to these signals, as they are wired to multipin connectors.

Note: The order code for the mating connector is FX2-68S-1.27DSL from Hirose (https://www.hirose.com/product/en/products/search/?keyword=FX2-68S-1.27DSL&search_type=)

Figure 3-13: Multi-interface Connector (TPS-1 main board)

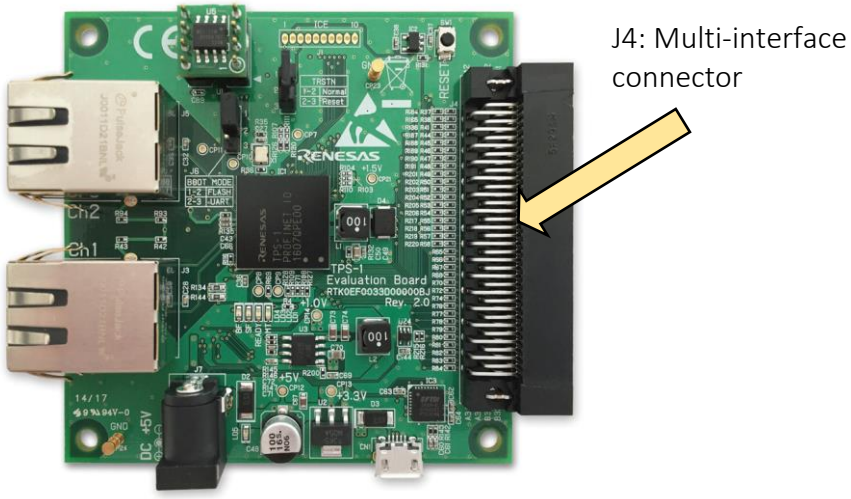


Table 3-7 shows the pin assignment of connector J4 in detail.

Table 3-7: Multi-board connector J4 pin assignment

J4 pin/ CN1 pin	TPS-1 board	Adapter board	J4 pin CN1 pin	TPS-1 board	Adapter board
A1	GPIO0	GPIO0	B1	GPIO34	GPIO34
A2	GPIO1	GPIO1	B2	GPIO35	GPIO35
A3	GPIO2	GPIO2	B3	GPIO36	GPIO36
A4	GPIO3	GPIO3	B4	GPIO37	GPIO37
A5	GPIO4	GPIO4	B5	GPIO38	GPIO38
A6	GPIO5	GPIO5	B6	GPIO39	GPIO39
A7	GPIO6	GPIO6	B7	GPIO40	GPIO40
A8	GPIO7	GPIO7	B8	GPIO41	GPIO41
A9	GPIO8	GPIO8	B9	GPIO42	GPIO42
A10	GPIO9	GPIO9	B10	GPIO43	GPIO43
A11	GPIO10	GPIO10	B11	GPIO44	GPIO44
A12	GPIO11	GPIO11	B12	GPIO45	GPIO45
A13	GPIO12	GPIO12	B13	GPIO46	GPIO46
A14	GPIO13	GPIO13	B14	GPIO47	GPIO47
A15	GPIO14	GPIO14	B15	INT_OUT	INT_OUT
A16	GPIO15	GPIO15	B16	WD_IN	WD_IN
A17	GPIO16	GPIO16	B17	WD_OUT	WD_OUT
A18	GPIO17	GPIO17	B18	n. c.	no signal
A19	GPIO18	GPIO18	B19	TPS1_RST_IN	TPS1_RST_IN
A20	GPIO19	GPIO19	B20	RESETN	RESETN
A21	GPIO20	GPIO20	B21	TPS1-T1	TPS1-T1
A22	GPIO21	GPIO21	B22	TPS1-T2	TPS1-T2
A23	GPIO22	GPIO22	B23	TPS1-T3	TPS1-T3
A24	GPIO23	GPIO23	B24	TPS1-T4	TPS1-T4
A25	GPIO24	GPIO24	B25	TPS1-T5	TPS1-T5
A26	GPIO25	GPIO25	B26	TPS1-T6	TPS1-T6
A27	GPIO26	GPIO26	B27	VDD33	VDD33
A28	GPIO27	GPIO27	B28	VDD33	VDD33
A29	GPIO28	GPIO28	B29	VDD33	VDD33
A30	GPIO29	GPIO29	B30	VDD33	VDD33
A31	GPIO30	GPIO30	B31	GND	GND
A32	GPIO31	GPIO31	B32	GND	GND
A33	GPIO32	GPIO32	B33	GND	GND
A34	GPIO33	GPIO33	B34	GND	GND

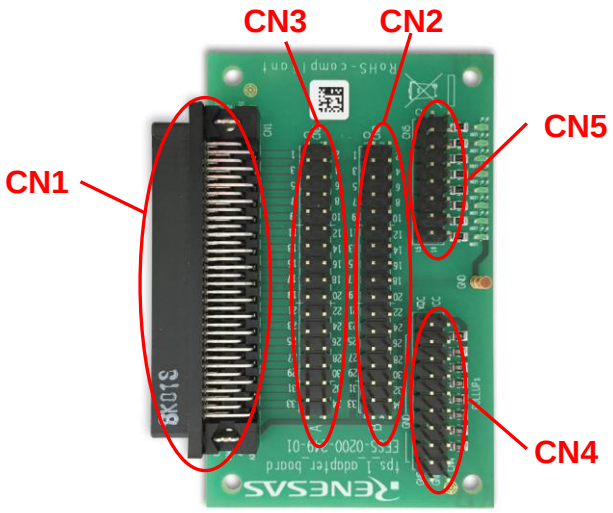
Chapter 4 Adapter Board Description

The adapter board consists mainly of connectors and some passive components. There are two use cases for this board:

1. If TPS-1 is operated in parallel IO mode, the level of 8 GPIOs of the TPS-1 can visualized with a set of 8 green LEDs. On the other hand 8 other GPIOs can be pulled to GND or 3.3V.
2. If TPS-1 is operated in host serial or parallel mode, all interface signals are routed to two multipin connectors (CN2 and CN3) from which CPU boards can be wired using the wire bundle that is delivered with the TPS-1 low-cost Solution Kit.

Figure 4-1 shows the position of the connectors that are described in the subsequent chapters.

Figure 4-1: Connector position on adapter board



4.1 Multi-board Connector CN1

As adapter board and TPS-1 board are normally operated plugged together, the adapter board has another 68-pin connector that matches its counterpart on the TPS-1 board. All CN1 pins are directly routed to CN2 respectively CN3; you can therefore access any CN1 signal for measurement or control purposes on CN2 and CN3. The pin assignment for CN1 is the same as for J4 on the TPS-1 board and shown in Table 3-7.

4.2 CPU Board Connectors CN2 and CN3

While CN1 is primarily used for hooking up the TPS-1 board, CN2 and CN3 are used for plugging connections to your target CPU boards. You can, but do not have to use the wire set that is delivered together with the TPS-1 Low-cost Solution Kit.

Simple 2.54mm pitch 2-row connectors are used for CN2 and CN3. The silkscreen on the adapter board indicates to which CN1 pin the CN2/3 pins are routed; Table 4-1 and Table 4-2 show which signals hence are available where.

Table 4-1: CPU board connector CN2 pin assignment

J4 pin	TPS-1 signal	CN2 pin		TPS-1 signal	J4 pin
B1	GPIO34	1	2	GPIO35	B2
B3	GPIO36	3	4	GPIO37	B4
B5	GPIO38	5	6	GPIO39	B6
B7	GPIO40	7	8	GPIO41	B8
B9	GPIO42	9	10	GPIO43	B10
B11	GPIO44	11	12	GPIO45	B12
B13	GPIO46	13	14	GPIO47	B14
B15	INT_OUT	15	16	WD_IN	B16
B17	WD_OUT	17	18	No signal	B18
B19	TPS1_RST_IN	19	20	RESETN	B20
B21	TPS1-T1	21	22	TPS1-T2	B22
B23	TPS1-T3	23	24	TPS1-T4	B24
B25	TPS1-T5	25	26	TPS1-T6	B26
B27	VDD	27	28	VDD	B28
B29	VDD	29	30	VDD	B30
B31	GND	31	32	GND	B32
B33	GND	33	34	GND	B34

Table 4-2: CPU board connector CN3 pin assignment

J4 pin	TPS-1 signal	CN3 pin		TPS-1 signal	J4 pin
A1	GPIO0	1	2	GPIO1	A2
A3	GPIO2	3	4	GPIO3	A4
A5	GPIO4	5	6	GPIO5	A6
A7	GPIO6	7	8	GPIO7	A8
A9	GPIO8	9	10	GPIO9	A10
A11	GPIO10	11	12	GPIO11	A12
A13	GPIO12	13	14	GPIO13	A14
A15	GPIO14	15	16	GPIO15	A16
A17	GPIO16	17	18	GPIO17	A18
A19	GPIO18	19	20	GPIO19	A20
A21	GPIO20	21	22	GPIO21	A22
A23	GPIO22	23	24	GPIO23	A24
A25	GPIO24	25	26	GPIO25	A26
A27	GPIO26	27	28	GPIO27	A28
A29	GPIO28	29	30	GPIO29	A30
A31	GPIO30	31	32	GPIO31	A32
A33	GPIO32	33	34	GPIO33	A34

4.3 LED Connector CN5

The LED connector CN5 is another simple 2.54mm pitch 2-row connector with 16 pins. Circuit-wise CN5 is separated from the rest of the circuit. Each CN5 pin pair is connected to a green LED (via series resistor) and then to GND. Thus a logical high level on the pin pair lights the LED. A total of 8 LEDs are provided. Table 4-3 shows the assignment of LEDs to pins.

Table 4-3: LED connector CN5 pin assignment

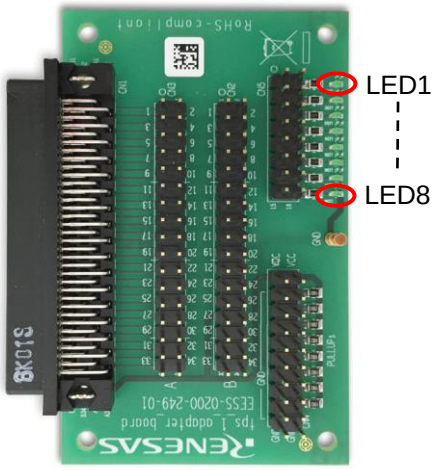
LED	CN5 pin		LED
LED1	1	2	LED1
LED2	3	4	LED2
LED3	5	6	LED3
LED4	7	8	LED4
LED5	9	10	LED5
LED6	11	12	LED6
LED7	13	14	LED7
LED8	15	16	LED8

The separation of the CN5-related circuit of the rest allows a more flexible usage of the limited number of LEDs. If you want to check TPS-1 output data in a simple parallel IO-mode application, you can wire the 8 LEDs with the jumper cables in the kit between CN5 and CN2/3 to arbitrary GPIOs of TPS-1 according to Table 4-1 andTable 4-2.

If desired the LEDs can as well be used as a primitive “logic analyser” if you tap signals between TPS-1 and the host CPU with one of the provided LEDs. If you do this, make sure that the signal timing is sufficiently uncritical to drive an LED.

Figure 4-2 illustrates the position of the LEDs.

Figure 4-2: LED position on adapter board



4.4 Pull Resistor Connector CN4

The pull resistor CN4 is another simple 2.54mm pitch 2-row connector with 20 pins. Circuit-wise CN4 is separated from the rest of the circuit. CN4 has eight 10kΩ pull-up resistors that are connected to 3.3V and eight hard GND connections. Some remaining pins are connected to 3.3V and GND for optional supply of external circuitry.

Table 4-4 shows the pin assignment for CN4.

Note: If you draw current from connector CN4, please make sure that the power supply circuitry on the TPS-1 main board is not overloaded.

Table 4-4: Pull resistor connector CN4 pin assignment

Signal	CN4 pin		Signal
3.3V	1	2	3.3V
GND	3	4	10kΩ pull-up
GND	5	6	10kΩ pull-up
GND	7	8	10kΩ pull-up
GND	9	10	10kΩ pull-up
GND	11	12	10kΩ pull-up
GND	13	14	10kΩ pull-up
GND	15	16	10kΩ pull-up
GND	17	18	10kΩ pull-up
GND	19	20	GND

Revision History

Revision	Issue Date	Major changes
R21UT0239ED0100	May 31st 2017	Initial release
R21UT0239ED0101	August 3rd, 2018	added operating current to Table 2-1 rearranged table in chapter 2.4 clarified power supply alternatives in chapter 3.4 Table 3-1**:** cleaned up clarified wording in chapter 3.10.2 removed text after Table 4-4 various minor corrections
R21UT0239ED0102	April 12th, 2019	minor changes update the list of related documents table added RX66T host CPU info in Chapter 1 various minor corrections
R21UT0239ED0103	September 12th, 2023	minor changes update the list of related documents table; in chapter 3.8 reset circuit (added reset diagram for board revision 3.0).

YCONNECT-IT-TPS-1L

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