# User Manual

## DA14580 Range Extender v.2 Reference Application

### UM-B-045


**Abstract**

*This document describes the Bluetooth Range Extender v.2 module, based on the DA14580 SoC. Target hardware: 580 RD QFN40 Module_RF PA_vC – Board Number: 078-56-C.*

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# 1 Terms and Definitions

| | |
|---|---|
| BLE | Bluetooth® Low Energy |
| BOM | Bill Of Materials |
| DUT | Device Under Test |
| ERP | Effective Radiated Power |
| FW | Firmware |
| LPF | Low Pass Filter |
| PA | Power Amplifier |
| PCBA | Printed Circuit Board Assembled |
| PCB | Printed Circuit Board |
| RF | Radio Frequency |
| SoC | System on Chip |
| SPDT | Single Pole Double Throw |

# 2 References

[1] DA14580 Low Power Bluetooth Smart SoC, Datasheet, Dialog Semiconductor

[2] SKY66111-11 Datasheet

[3] AN-B-020 End product testing and programming guidelines.(This document is susceptible to be replaced)

[4] UM-B-012 DA14580/581/583 Creation of a secondary boot loader

# 3 Introduction

The DA14580 Range Extender v.2 module design is based on the Dialog Semiconductor DA14580 BLE Smart SoC, where enhanced RF transmitted power is presented. This module serves as reference design to potential customers requesting BLE functionality with Nominal RF Output power up to +9.3 dBm (Peak RF Output Power +9.8 dBm). From physical perspective, the module is a two layer PCBA where the digital and power interfaces of the DA14580 are accessible to the user. This document presents the system, technical specifications, physical dimensions and test results.

**Figure 1: DA14580 Range Extender v.2 module**

# 4 System overview

## 4.1 Features

- Highly integrated Dialog Semiconductor DA14580 *Bluetooth ® Smart SoC*
- Module can be used as either stand-alone or as a data pump on a system with an external processor
- Module satisfies all Bluetooth requirements
- No external crystal or additional passive components are required for module operation, as the module is equipped with two crystal oscillators one at 16MHz (XTAL16M) and a second at 32.738KHz (XTAL32K). The 32.738 KHz is used as the clock of Extended/ Deep Sleep modes.
- Access to processor via JTAG, SPI, UART or I2C
- 22 GPIOs available on module at a 1.27 mm pitch, suitable for keyboard designs
- Operating voltage: 2.4 V to 3.3 V. Suitable for operation from a single coin cell battery.
- On-board printed inverted F-type antenna (Figure 1)
- RF connector for conducted measurements( Figure 1)
- Up to +9.3 dBm Nominal Maximum Output Power (+9.8dBm Peak Maximum Output Power).
- Rx sensitivity: better than -90 dBm
- *Supply current:*

  -Tx : less than 17 mA peak current @ 3.0 V

  -Rx: less than 6 mA peak current @ 3.0 V

  -Extended - Sleep current: less than 1.6µA @ 3.0 V
- 15.25 mm x 24 mm, 37 pins, two layer PCBA
- Operating temperature: –40 ˚C to +85 ˚C
- Test FW based on DA14580_581_583_SDK_3.0.10.1

**Table 1: Electrical characteristics**

| Characteristic | Value | Comments |
|---|---|---|
| Battery voltage ($V_{BAT\_3V}$) | 2.4 V to 3.3 V | Specification tested at typical voltage of 3.0 V |
| Operating frequency range | 2400 MHz to 2483.5 MHz | |
| Conducted output power | +9.3 dBm | $V_{BAT\_3V}$ = 3 V, $T_A$ = +15 to +35 °C |
| Maximum bypass loss | 0.6 dB | $V_{BAT\_3V}$ = 3 V, $T_A$ = +15 to +35 °C |
| Receiver sensitivity | Better than -90 dBm | $V_{BAT\_3V}$ = 3 V, $T_A$ = +15 to +35 °C |
| Peak Tx current | <17mA | Tx Power = +9.3 dBm, $V_{BAT\_3V}$ = 3 V, $T_A$ = +15 to +35 °C |
| Peak extended-sleep current | <1.6µA | $V_{BAT\_3V}$ = 3 V, $T_A$ = +15 to +35 °C |

## 4.2 General description

The system consists of the DA14580 Bluetooth Low power SoC, the SKY6611-11 Front-end module and a discrete low pass filter. The radio front end is connected to a PCB trace antenna as Figure 2 shows.

The power amplifier is controlled by the CTRL1 and CTRL2 signals. CTRL1 is generated from pin P0_3 and CTRL2 is generated from P0_2 of the DA14580. On pin P0_3 and pin P0_2 the internal Radio_TXEN and Radio_RXEN signals are software allocated.

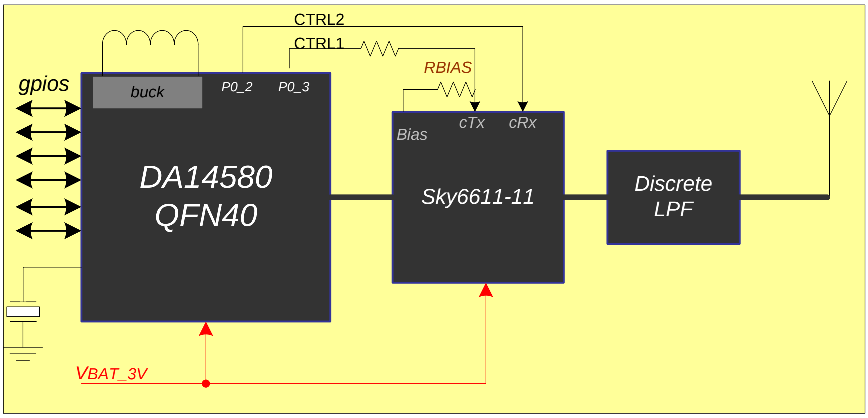



**Figure 2: Block diagram**

The amplifier circuit is the SKY66111-11 from Skyworks. The CTX pin is used as the TX control signal and amplifier bias voltage. CTX pin is connected to the amplifier BIAS pin via resistor RBIAS. The resistor value is adjusted in order to get a Nominal RF Output Power of +9.3 dBm. More information for the power output adjustment can be found in Sky66111-11 datasheet[2].

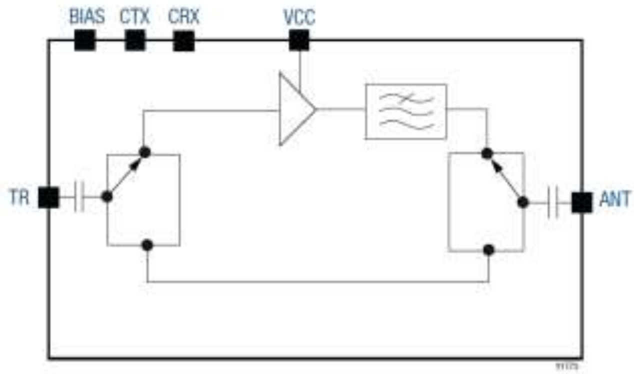



**Figure 3: Sky66111-11 Power Amplifier**

## 4.3 Bluetooth SoC

The DA14580 integrated circuit has a fully integrated radio transceiver and baseband processor for B*luetooth ® Smart*. It can be used as an application processor as well as a data pump in systems with an external processor.

The DA14580 contains an embedded One-Time-Programmable (OTP) memory for storing Bluetooth profiles as well as custom application code. The qualified *Bluetooth® Smart* protocol stack, which is stored in a dedicated ROM, and the customer application software which is stored in system RAM, run on the embedded ARM Cortex M0 processor. Low leakage Retention RAM is used to store sensitive data and connection information while in Deep Sleep mode.

The Radio Transceiver implements the RF part of the Bluetooth Smart protocol. Together with the Bluetooth 4.0 PHY layer, it provides a 93 dB RF link budget for reliable wireless communication. All RF blocks are supplied by on-chip low drop out regulators (LDOs). The RF port is single ended 50 Ω, so no external balun is required.

The DA14580 has dedicated hardware for the Link Layer implementation of *Bluetooth® Smart* and interface controllers for enhanced connectivity capabilities.

The reset line of the DA14580 (pin RST) is active high. On this module the RST pin is available on module pin 21.

Main debug port for the DA14580 is the JTAG. JTAG consists of two signals, SWDIO and SWCLK.

The frequency tolerance specification for BLE is 50 ppm. In order to compensate ageing and offset effects, an external crystal shall have an accuracy of ±15 ppm or better. The DA14580 crystal (Y1) has a fundamental frequency of 16 MHz and load capacitance not higher than 10 pF. The crystal is located on the module itself. Also, an internal programmable capacitance bank is available in the DA14580. In this way, the crystal oscillator frequency can be tuned.

For sleep mode the on chip RCX oscillator is utilized. In addition, a 32 kHz crystal (Y2) with a tolerance of 50 ppm (500 ppm max) can be assembled on the module. The crystal load capacitance shall not be higher than 10 pF.

The external digital interfaces available for the module are:

- 2 UARTs with hardware flow control up to 1 MBd
- SPI interface
- I2C bus at 100 kHz, 400 kHz

- 3-axis capable Quadrature Decoder

There is also a 4-channel 10-bit ADC available externally to the module.

The module includes 22 GPIOs (including JTAG signals) that are available externally. The interfaces are multiplexed with the GPIOs and can be enabled by appropriate programming.

The DA14580 is equipped with a DC-DC converter that can be configured as either Buck or Boost. For this module, the DC-DC converter is configured as a Buck converter (C5, C2, L1, C3).

The DA14580 is available in three packages: WLCSP34, QFN40 and QFN48. In this reference application the QFN40 has been used.

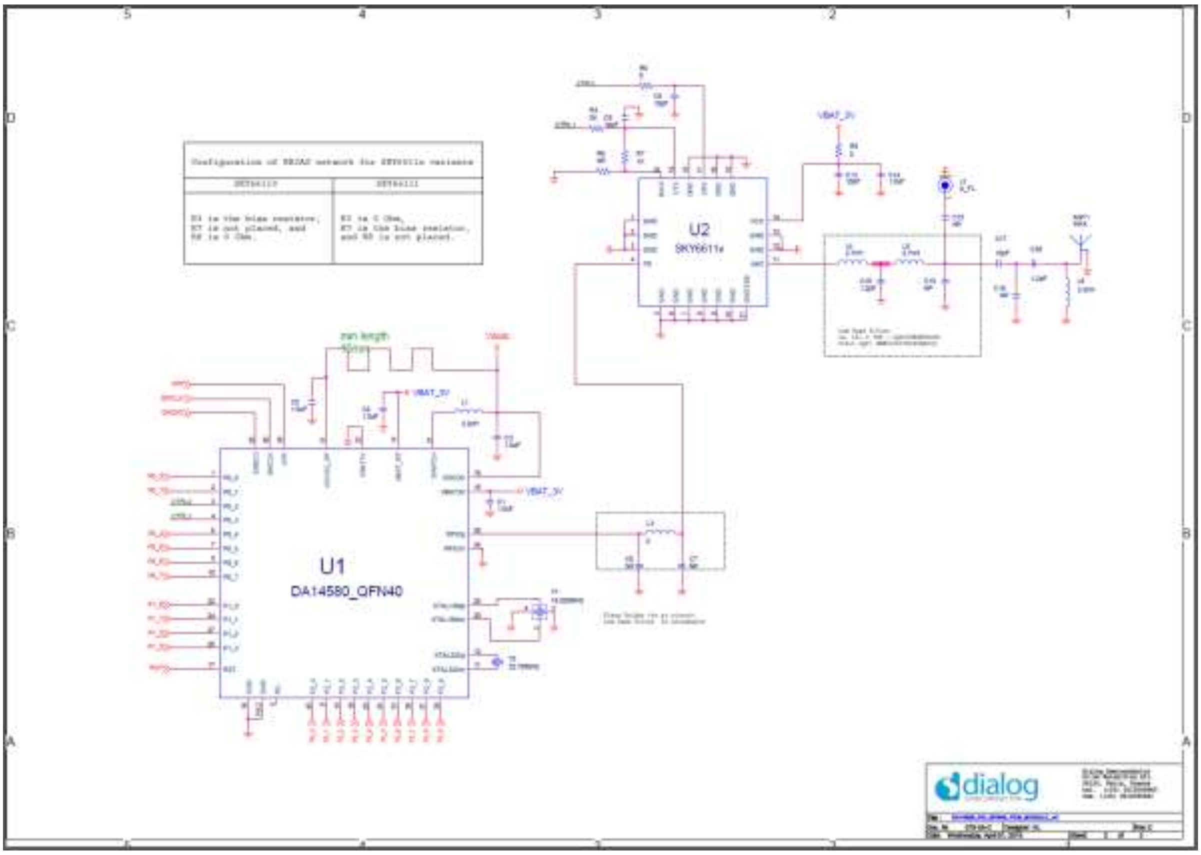



**Figure 4: DA14580 QFN40 SoC, Range Extender ver.2 module**

## 4.4 RF front end

This part of the design is implementing the amplification of the RF transmitted signal while the transmitted harmonics as well as the Tx spurious emissions remain within the FCC/ETSI specification.

The operation of the RF front end is controlled by the DA14580. There are two RF paths: one through the amplifier and one bypass path. The amplifier path is enabled during transmission. The RF signal passes through the PA, the low pass filter and the RF matching network. In the bypass path, the RF signal received at the antenna is driven directly to the BLE transceiver.

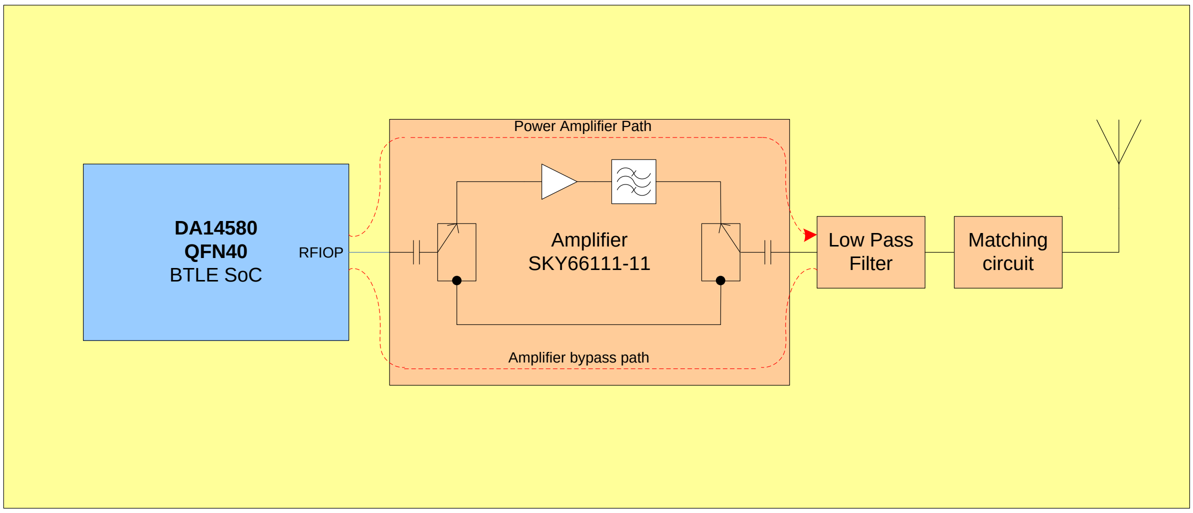



Figure 5: RF front end signal paths

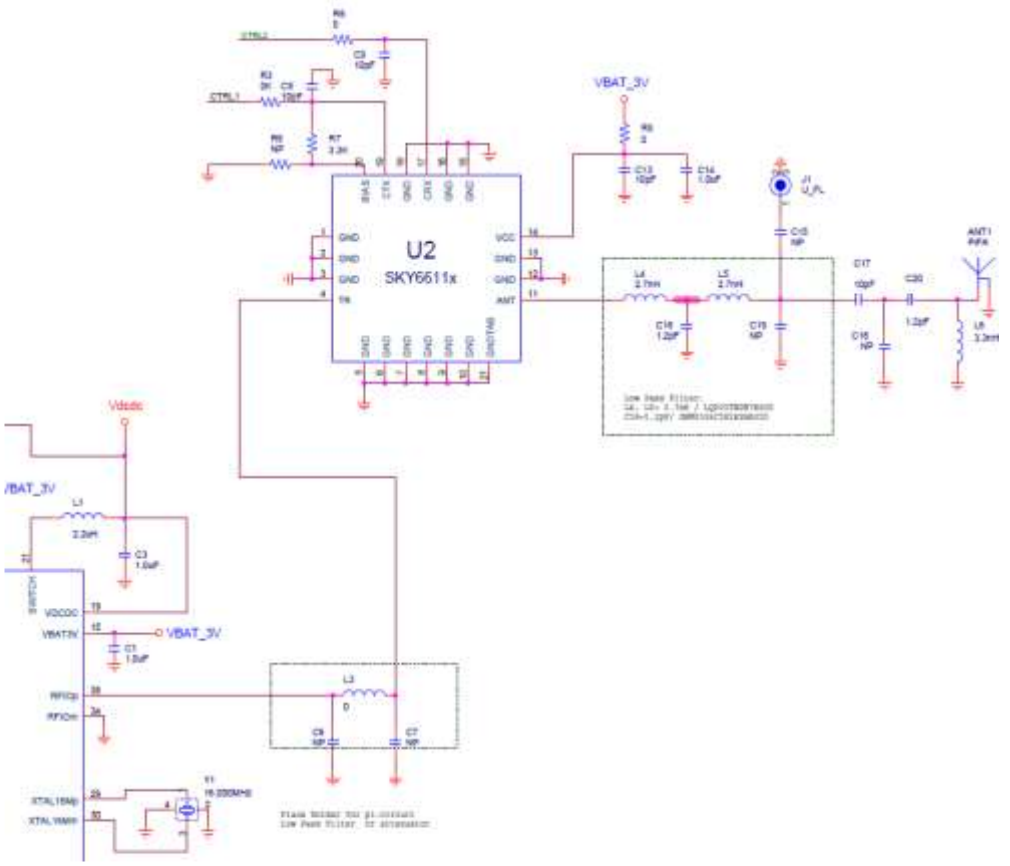



Figure 6: RF front end schematic

### 4.4.1 Radio front end control signals

#### 4.4.1.1 Radio front end control signals

In general, three different radio control signal can be extracted from DA14580:

- extrc_txen, it can be used as Tx_En control signal of the RF front end.
- extrc_rxen or radcntl_rxen radio. Both signals are of the same duration. They can be used as Rx_En control signals for the RF front end.
- event_in_process that can be used for wlan co-existence signal.

The signals are extracted by using the BLE diagnostic port. Two registers need to be programmed:

- BLE_DIAGCNTL_REG where it is defined which signals will be extracted from each port. Register specification of BLE_ DIAGCNTL_REG

**Table 2: BLE_ DIAGCNTL_REG (0x40000050) register specification**

| Bit | Mode | Symbol | Description | Reset |
|---|---|---|---|---|
| 31 | R/W | DIAG3_EN | 0: Disable diagnostic port 3 output. All outputs are set to 0.<br>1: Enable diagnostic port 3 output. | 0x0 |
| 30 | - | - | Reserved | 0x0 |
| 29:24 | R/W | DIAG3 | Only relevant when DIAGEN3 = 1.<br>Selection of the outputs that must be driven to the diagnostic port 3. | 0x0 |
| 23 | R/W | DIAG2_EN | 0: Disable diagnostic port 2 output. All outputs are set to 0.<br>1: Enable diagnostic port 2 output. | 0x0 |
| 22 | - | - | Reserved | 0x0 |
| 21:16 | R/W | DIAG2 | Only relevant when DIAGEN2 = 1.<br>Selection of the outputs that must be driven to the diagnostic port 2. See chapter 2.15 for a detailed description. | 0x0 |
| 15 | R/W | DIAG1_EN | 0: Disable diagnostic port 1 output. All outputs are set to 0.<br>1: Enable diagnostic port 1 output. | 0x0 |
| 14 | - | - | Reserved | 0x0 |
| 13:8 | R/W | DIAG1 | Only relevant when DIAGEN1 = 1.<br>Selection of the outputs that must be driven to the diagnostic port 1. See chapter 2.15 for a detailed description. | 0x0 |
| 7 | R/W | DIAG0_EN | 0: Disable diagnostic port 0 output. All outputs are set to 0.<br>1: Enable diagnostic port 0 output. | 0x0 |
| 6 | - | - | Reserved | 0x0 |
| 5:0 | R/W | DIAG0 | Only relevant when DIAGEN0 = 1.<br>Selection of the outputs that must be driven to the diagnostic port 0. | 0x0 |

- BLE_CNTL2_REG where the BLE diagnostic port is enabled and the straight or reverse pin assignment is defined. This function is controlled by two register bit-fields, DIAGPORT_SEL and DIAGPORT_REVERSE. Description presented below on Table 3.

**Table 3: BLE_CNTL2_REG (0x40000200) register specification**

| Bit | Mode | Symbol | Description | Reset |
|---|---|---|---|---|
| 5 | R/W | DIAGPORT_REVERSE | BLE/RADIO Diagnostic Port Reverse order.<br><br>When this bit is "1", the mapping of the diagnostic bus DIAGPORT[7:0] (controlled by DIAGPORT_SEL) to GPIOs (controlled by Pxy_MODE_REG[PID]) is reversed. The mapping is:<br><br>If "0" then DIAGPORT[7] is mapped to P0[7], etc.<br>DIAGPORT[4] is mapped to P0[4],<br>DIAGPORT[3] is mapped to P0[3] and P1[3], etc. and<br>DIAGPORT[0] is mapped to P0[0] and P1[0].<br>If "1" then DIAGPORT[7] is mapped to P0[0] and P1[0], etc.<br>DIAGPORT[4] is mapped to P0[3] and P1[3],<br>DIAGPORT[3] is mapped to P0[4], etc. and<br>DIAGPORT[0] is mapped to P0[7]. | 0 |
| 4:3 | R/W | DIAGPORT_SEL | BLE/RADIO Diagnostic Port Selection.<br><br>Controls the multiplexing of the internal diagnostic signals towards the 8-bit diagnostic bus DIAGPORT[7:0]. The DIAGPORT[7:0] bit order may or may not be reversed by using the DIAGPORT_REVERSE bitfield and then it will be directed to the GPIOs P0[7:0] and P1[3:0]. (Note that the P1[3:0] diagnostic signals are the same with P0[3:0] signals.)<br><br>The DIAGPORT[7:0] value, depending on the DIAGPORT_SEL value, is:<br>00: {BLE_DIAG2[7:5], BLE_DIAG1[4:3], BLE_DIAG0[2:0]}<br>01: {BLE_DIAG2[7:5], BLE_DIAG1[4:3], BLE_DIAG0[2]<br>, wakeup_lp_irq, deep_sleep_stat_32k}<br>10: RADIO_DIAG0[7:0]<br>11: RADIO_DIAG1[7:0] | 0x0 |

In BLE_CNTL2_REG the port and the pins assignment order is defined. Only port 0 (P0_[0:7]) and port 1 (P1_[0:3]) of the chip can be utilized.

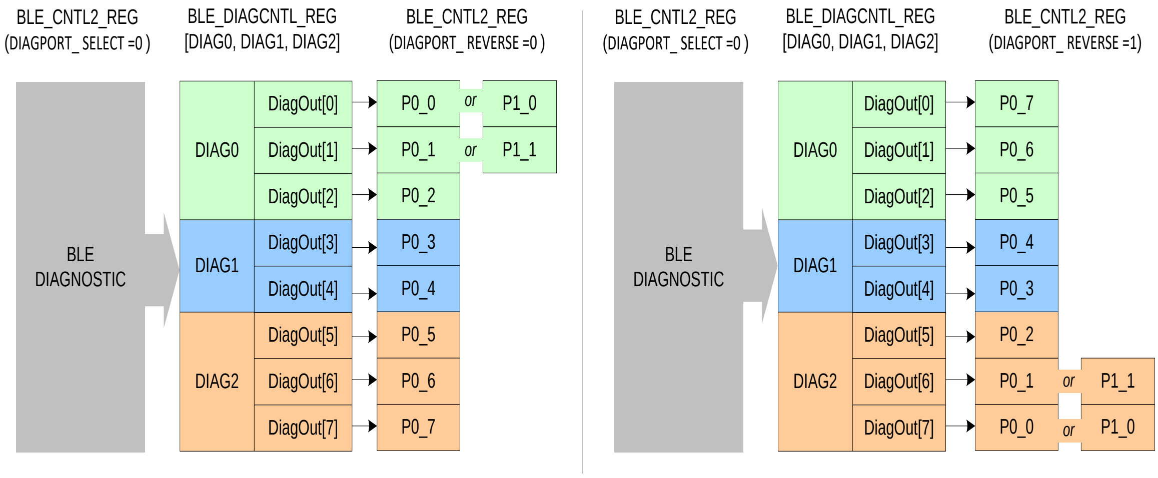



**Figure 7: Diagnostic port to pins assignment and register settings**

For having all pins extracted in parallel, a combination of register setting and pin availability must be arranged. For example it is preferable to avoid assigning P0_4 and P0_5 to RF control signals. P0_4 and P0_5 are used for UART ports in testing and production tests.

The available pins are presented below:

**Table 4: Diagnostic port availability and settings for control pins**

| Function | Diagnostic port settings | | DA14580 assigned Pins | |
|---|---|---|---|---|
| | BLE_DIAGCNTL_REG | | BLE_CNTL2_REG | |
| | DIAG port | DIAGx | DIAGPORT_ REVERSE = **0** | DIAGPORT_ REVERSE = **1** |
| **Tx**_Enable | DIAG1 | 0x28 | P0_3 | P0_4 |
| | | | | |
| **Rx**_Enable | DIAG1 | 0x28 | P0_4 | P0_3 |
| | DIAG2 | 0x08 | P0_5 | P0_2 |
| | DIAG2 | 0x0c | P0_6 | P0_1, P1_1 |
| | DIAG0 | 0x1F | P0_2 | P0_5 |
| | | | | |
| Wlan coexist | DIAG2 | 0x08 | P0_7 | P0_0, P1_0 |
| | DIAG2 | 0x0D | P0_7 | P0_0, P1_0 |
| | DIAG2 | 0x1F | P0_6 | P0_1, P1_1 |

#### 4.4.1.2 Suggested pin assignment

A suggested pin assignment for extracting all rf control signals at the same time is presented below

**Table 4: Suggested pin assignment for extracting all RF control signals**

| function | Signal used | Diagnostic port settings | | DA14580 assigned Pins |
|---|---|---|---|---|
| | | BLE_DIAGCNTL_REG | | BLE_CNTL2_REG |
| | | DIAG port | DIAGx | DIAGPORT_ REVERSE = **0** |
| PA_**Tx** Enable | extrc_txen | DIAG1 | 0x28 | P0_3 |
| | | | | |
| PA_**Rx** Enable | radcntl_rxen | DIAG0 | 0x1F | P0_2 |
| | | | | |
| Wlan coexist | event_in_ process | DIAG2 | 0x08 | P0_7 |

For more options on the pin assignment please read paragraph 4.8: Development mode-peripheral pin mapping.

Below, screenshots from the radio control signals during operation are presented. The proximity reporter_fh application was used.

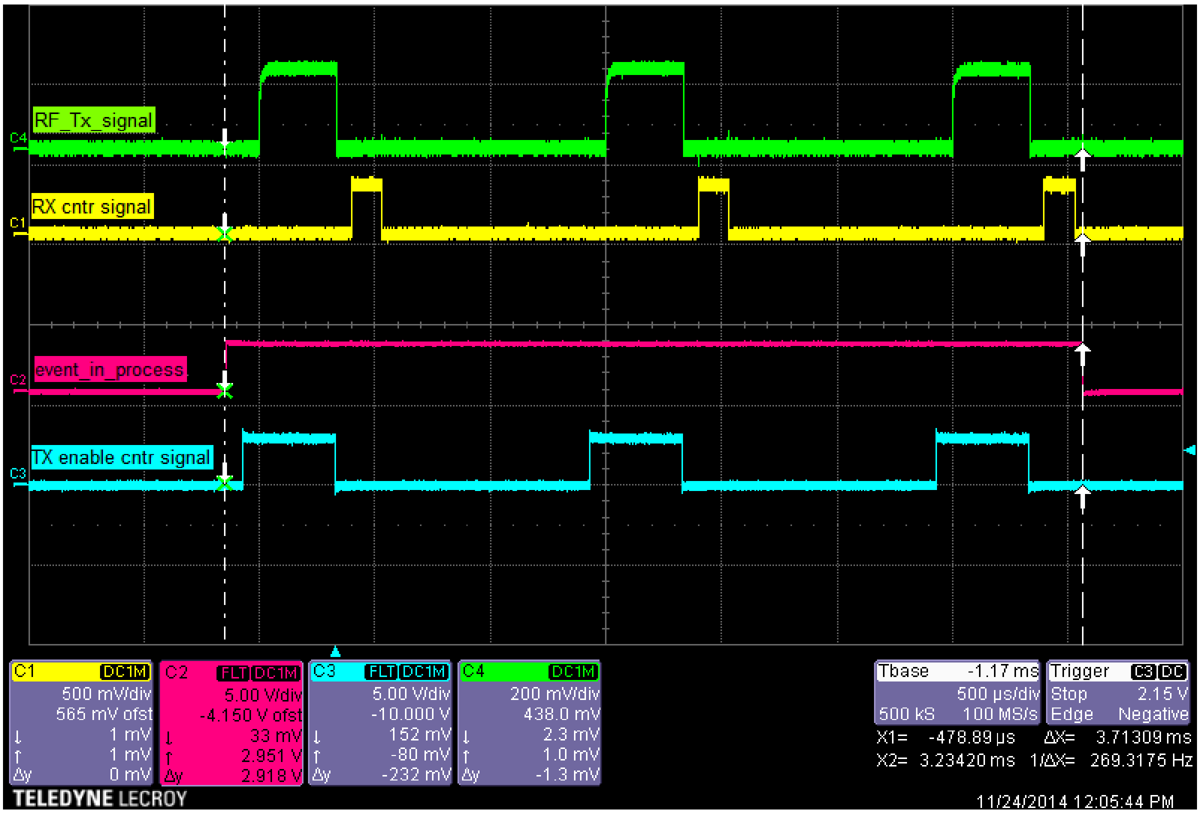



**Figure 8: The RF control signals**

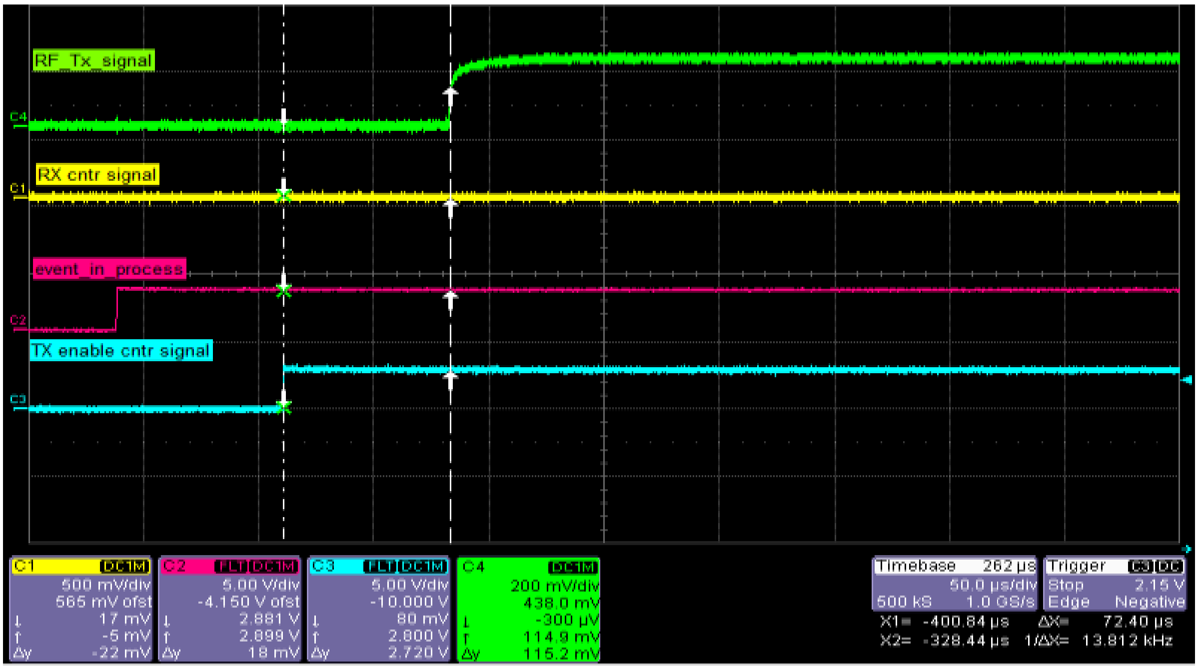



**Figure 9: Rising edge of Tx_En control signal**

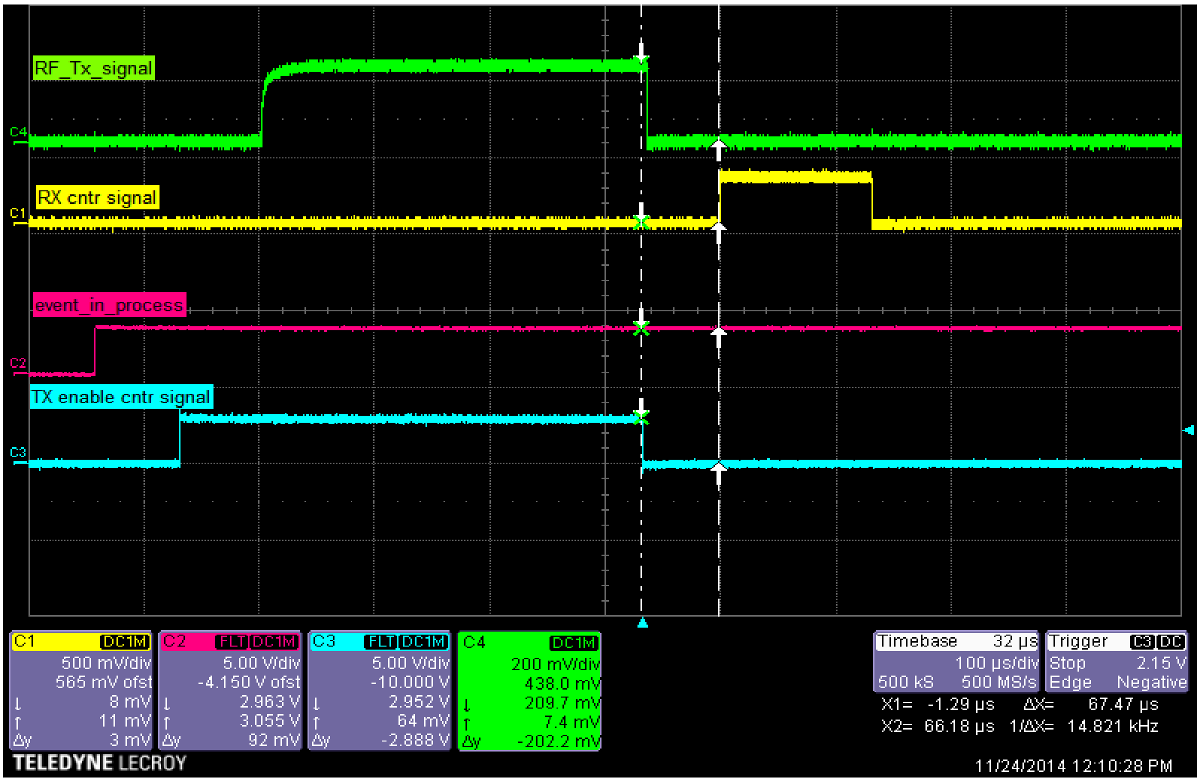



**Figure 10: Detail from Tx_En to Rx_En signal**

### 4.4.2 Power amplifier

The amplifier circuit is the SKY66111-11[2] from Skyworks. The VBIAS pin is connected to the bias voltage via resistor R7. The resistor value is adjusted so that the +9.3 dBm output power is achieved at maximum 16.15 mA current consumption.

There are two Low Pass Filters options for the power amplifier. The first one is at the input of the Skyworks amplifier and is formed by C6, C7 and L3 and the second is at the output of the Skyworks amplifier and is formed by L4, L5, C18 and C19. The second LPF is used in the current design.

The power amplifier is supplied from pin VBAT_3V directly.

### 4.4.3 Low pass filter

The low pass filter is placed after the amplifier matching network in order to suppress the harmonics generated due to the amplifier's nonlinearity. The filter presents low losses in the 2.4 GHz to 2.5 GHz frequency range (max. loss: 0.5 dB). The ripple on the pass band was chosen equal to 0.1dB.

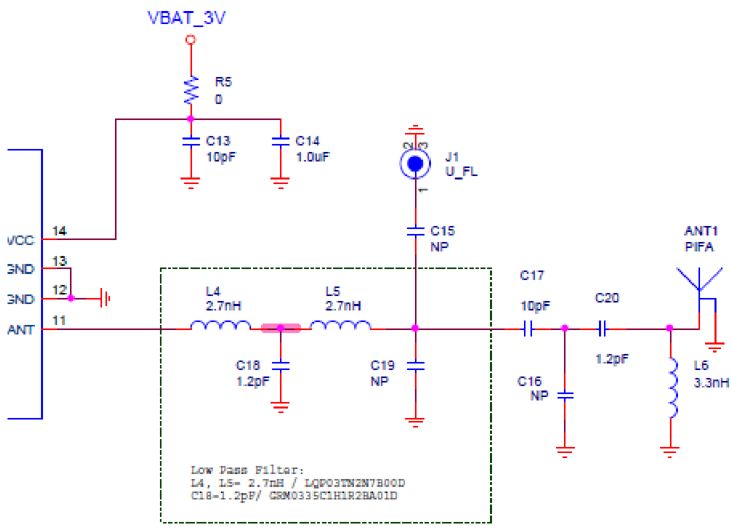



**Figure 11: Low pass filter**

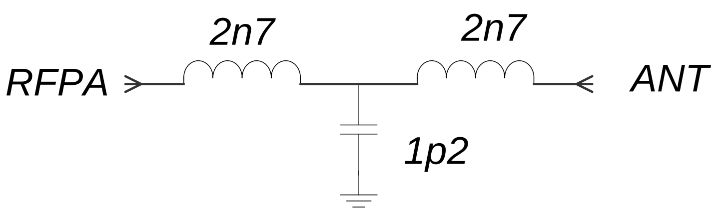



**Figure 12: T- shaped, 3-poles, Low Pass Filter**

The filter is a T- type Chebyshev 3rd order low pass filter. The filter configuration is presented in Figure 12.

Component value:

- 2,7nH : LQG15HN2N7S02 / Murata
- 1.2pF: GRM1555C1H1R2CZD1/ Murata

Frequency response measurements are presented in Figure 13.

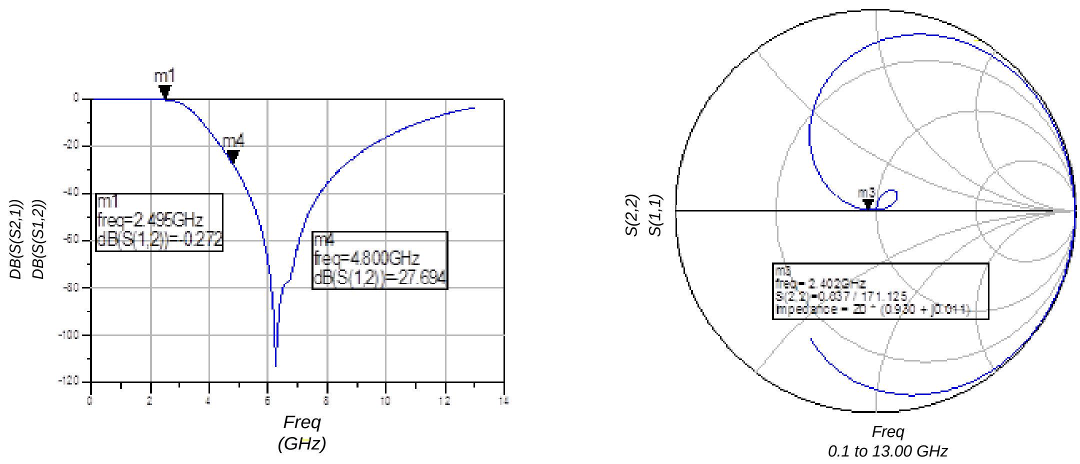



**Figure 13: Simulation results of LPF response**

## 4.4.4 Antenna

### 4.4.4.1 Range Extender v.2 on Interposer

The antenna is a printed Inverted F Antenna (IFA). The antenna was designed according to the size of the module and the available antenna space (15.24 mm x 24 mm). The measurements for the characterization of the antenna radiation pattern were performed with Range Extender v.2 module mounted on an interposer board. The matching components values for the antenna measurement are: C20= 1.2pF and L6=3.3nH.


**Figure 14: Range Extender v.2 on interposer**

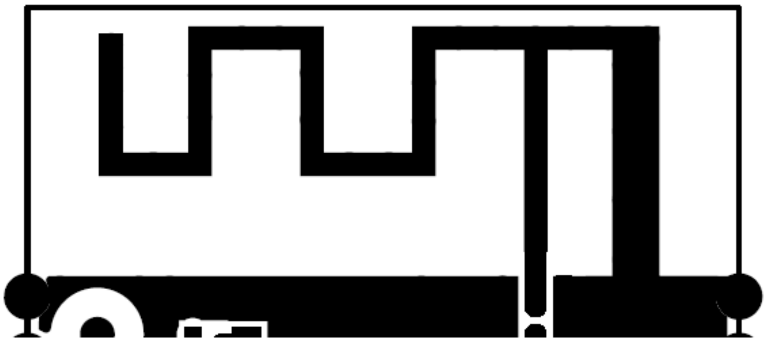


Figure 15: Antenna geometry on Range Extender v.2

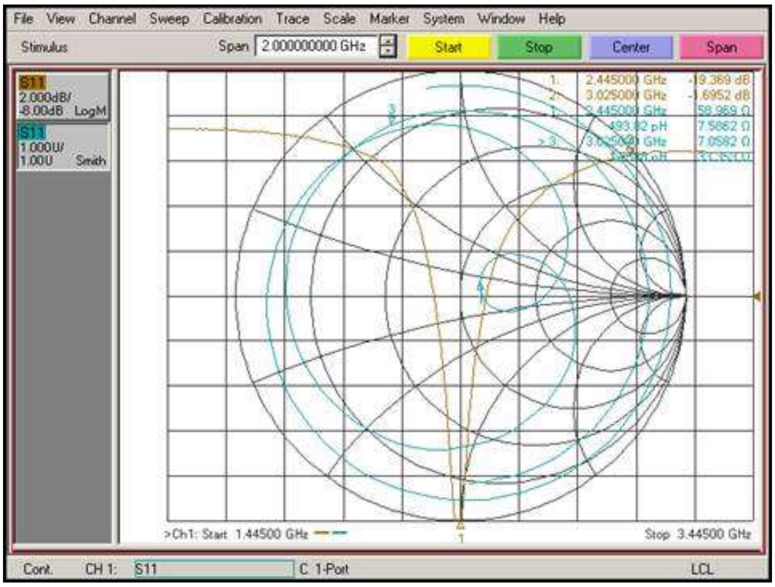



Figure 16: Measured S11 paramater for IFA

Gain measurements were performed in an anechoic chamber. The maximum gain was measured at 0 dBi.

**Table 5: Antenna gain Range Extender v.2 with interposer**

| Parameter | G (dBi) |
|---|---|
| Maximum gain | 0 |

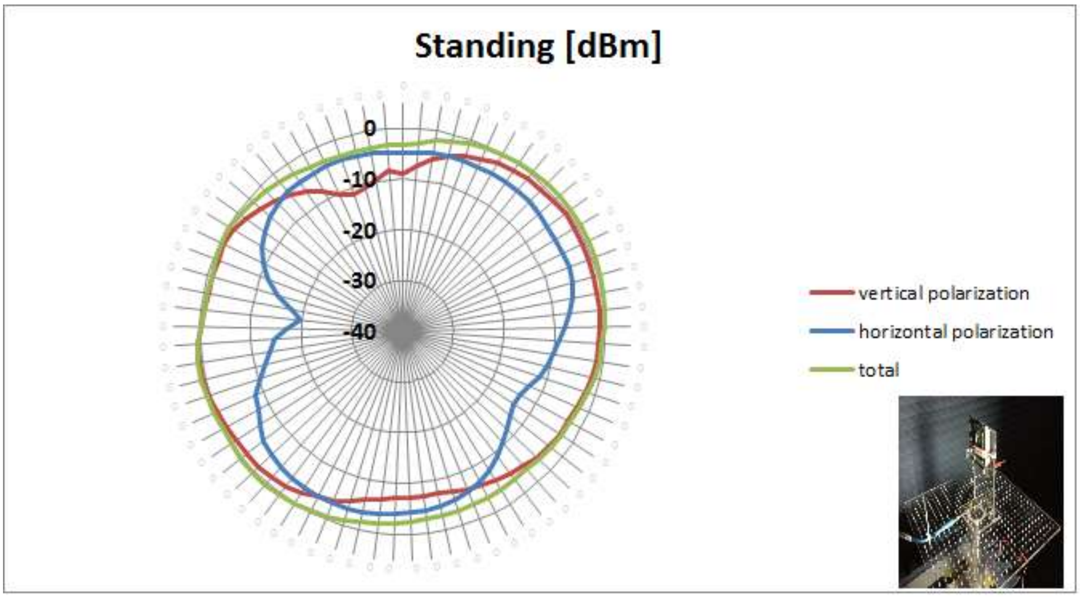



**Figure 17: Radiation diagram for the board placed vertically on the short edge**

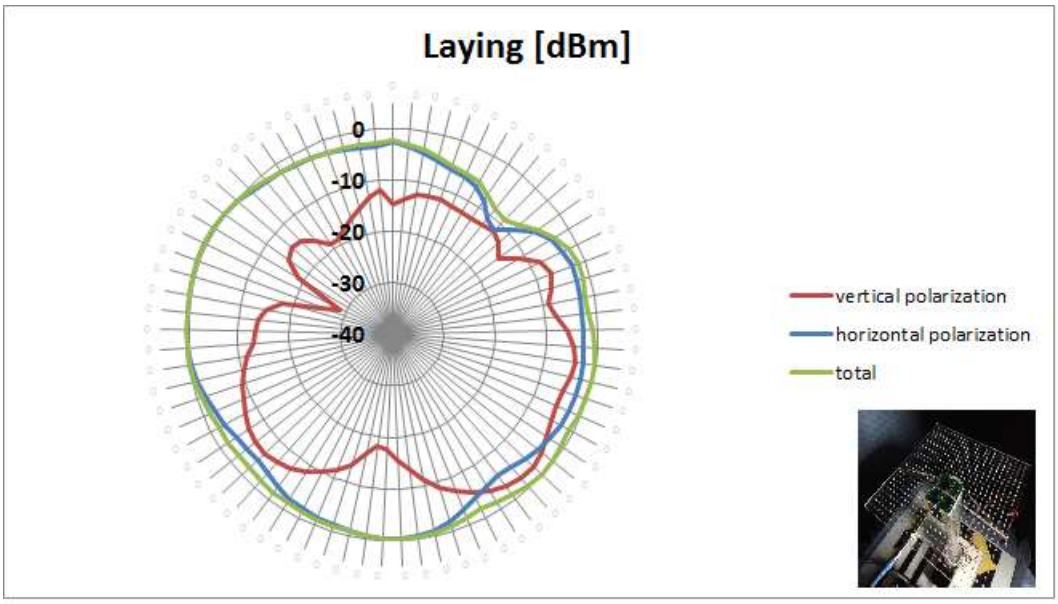



**Figure 18: Radiation diagram for the board placed horizontally**

### 4.4.4.2 Range Extender v.2 stand alone

Measurements for the characterization of the antenna radiation pattern were also performed with Range Extender v.2 not soldered on interposer. In this case the matching components values differ from the values of the module on the interposer. The matching values of the components are: C20= 1.2pF and C16=1pF.

**Figure 19: Range Extender v.2 stand-alone**

Gain measurements were performed in an anechoic chamber. The maximum gain was measured at -10 dBi.

**Table 6: Antenna gain Range Extender v.2 stand-alone**

| Parameter | G (dBi) |
|---|---|
| Maximum gain | -10 |

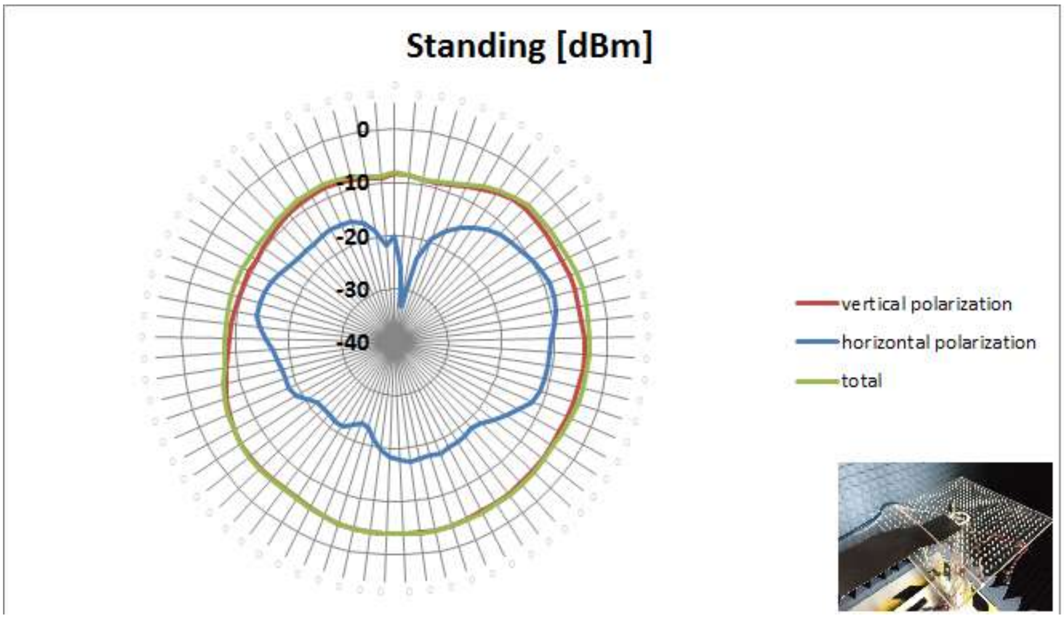



**Figure 20: Radiation diagram for the board placed vertically on the short edge**

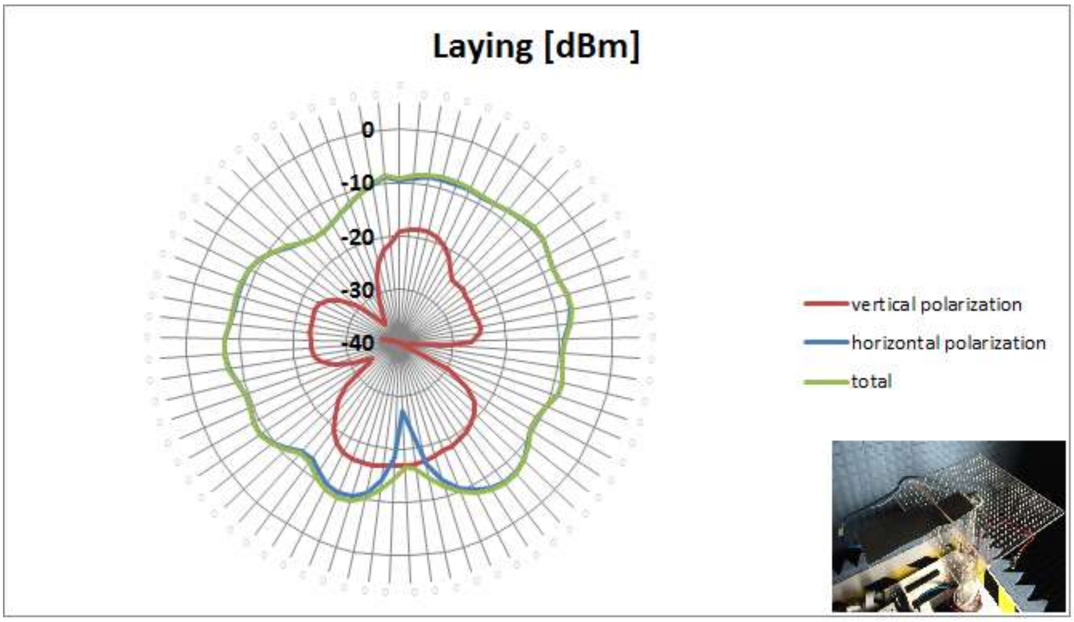



**Figure 21: Radiation diagram for the board placed horizontally**

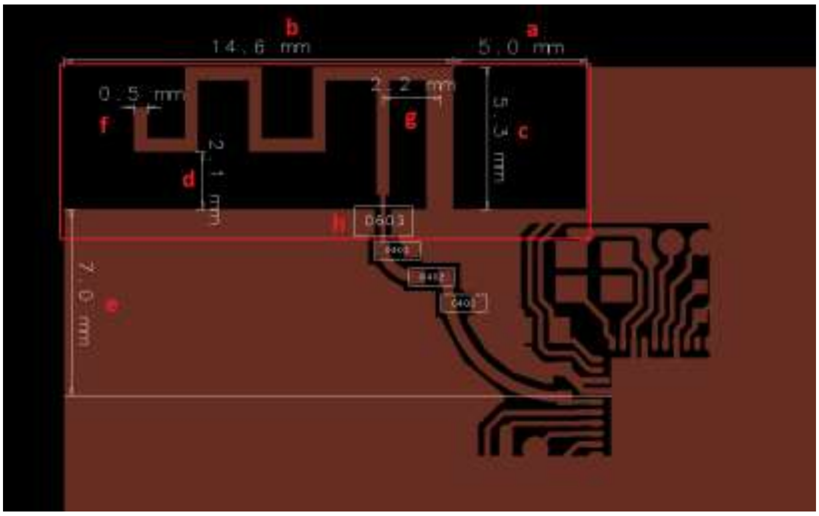



**Figure 22: IFA antenna implementation**

The dimensions above are given for a typical FR1 PCB substrate, 1mm thick. The antenna length is adjusted for resonance including a 1mm plastic enclosure placed in contact with the PCB antenna. The red outline indicates the antenna footprint, i.e. required allocation of PCB space. The footprint of the antenna is available per request in dxf format.

Legend (Figure 22):

Clearance between antenna arm and GND plane right a.

Antenna width b.

Antenna height c.

Clearance between the antenna arm and GND plane below d.

Minimum GND plane size required for correct operation of the antenna e.

Antenna traces width f.

## 4.5 Power system and requirements

The Range Extender v.2 module is supplied by a single power supply through pins VBAT_3V. For the DA14580 SoC, the VBAT_3V voltage variations are handled by the internal DC-DC converter. The DC-DC converter's external components are an inductor L1 (2.2 uH) and three capacitors C3, C1 and C2 (all three capacitors are equal to 1 uF).

The RF power amplifier and its circuitry are supplied directly from the external power source. The module is intended for use with a +3 V coin cell battery (e.g CR2450 type). The $V_{BAT\_3V}$ voltage range is 2.4 V to 3.0 V, whereas the absolute maximum voltage is 3.6 V.

The overall current consumption in Tx mode does not exceed 17 mA @ 3.0 V supply. The current consumption by the front end circuits (amplifier) does not exceed 11 mA, whereas in extended- sleep mode the consumption of the system is expected to be in less than 1.6 uA.


**Figure 23: Current consumption for Advertisement frame**

## 4.6 Trimming the 16MHz Xtal

For ensuring best operation of the Module, the 16MHz XTAL must be trimmed. The frequency is trimmed by two on-chip variable capacitor banks. Both capacitor banks are controlled by the same register. For trimming the XTAL apply procedure described on AN-B-020[3]: End product testing and programming guidelines.

## 4.7 PCBA

A 2-layer FR4 PCB with 1.024 mm standard thickness is used. The PCB size is 15.25x24 mm. There are 37 connection pads which are made as castellation (1/2 open drill) with 1.27 mm pitch.

The connection pad assignment is shown in Table 7 below. The pin numbering is counter clockwise, as seen from the PCB top starting in the top left corner. Schematic and BOM are presented in Figure 25 and Table 8.

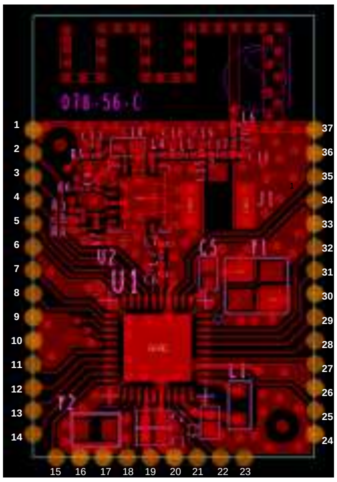



**Figure 24: Top view of PCBA**

**Table 7: Module Pin assignment**

| Pin | Signal name (Left side of the PCB seen from the top) | Pin | Signal name (Bottom side of the PCB seen from the top) | Pin | Signal name (Right side of the PCB seen from the top) |
|---|---|---|---|---|---|
| 1 | GND | 15 | P0_7 | 29 | SWCLK |
| 2 | P2_7 | 16 | GND | 30 | GND |
| 3 | P2_8 | 17 | GND | 31 | P1_2 |
| 4 | VPP | 18 | P2_2 | 32 | P1_3 |
| 5 | P2_9 | 19 | VBAT_3V | 33 | GND |
| 6 | P2_0 | 20 | GND | 34 | P2_5 |
| 7 | P0_0 | 21 | RST | 35 | P2_6 |
| 8 | P0_1 | 22 | P2_3 | 36 | GND |
| 9 | GND | 23 | P2_4 | 37 | GND |
| 10 | GND | 24 | GND | | |
| 11 | P0_4 | 25 | P1_0 | | |

| Pin | Signal name<br>(Left side of the PCB seen from the top) | Pin | Signal name<br>(Bottom side of the PCB seen from the top) | Pin | Signal name<br>(Right side of the PCB seen from the top) |
|---|---|---|---|---|---|
| 12 | P0_5 | 26 | GND | | |
| 13 | P2_1 | 27 | P1_1 | | |
| 14 | P0_6 | 28 | SWDIO | | |

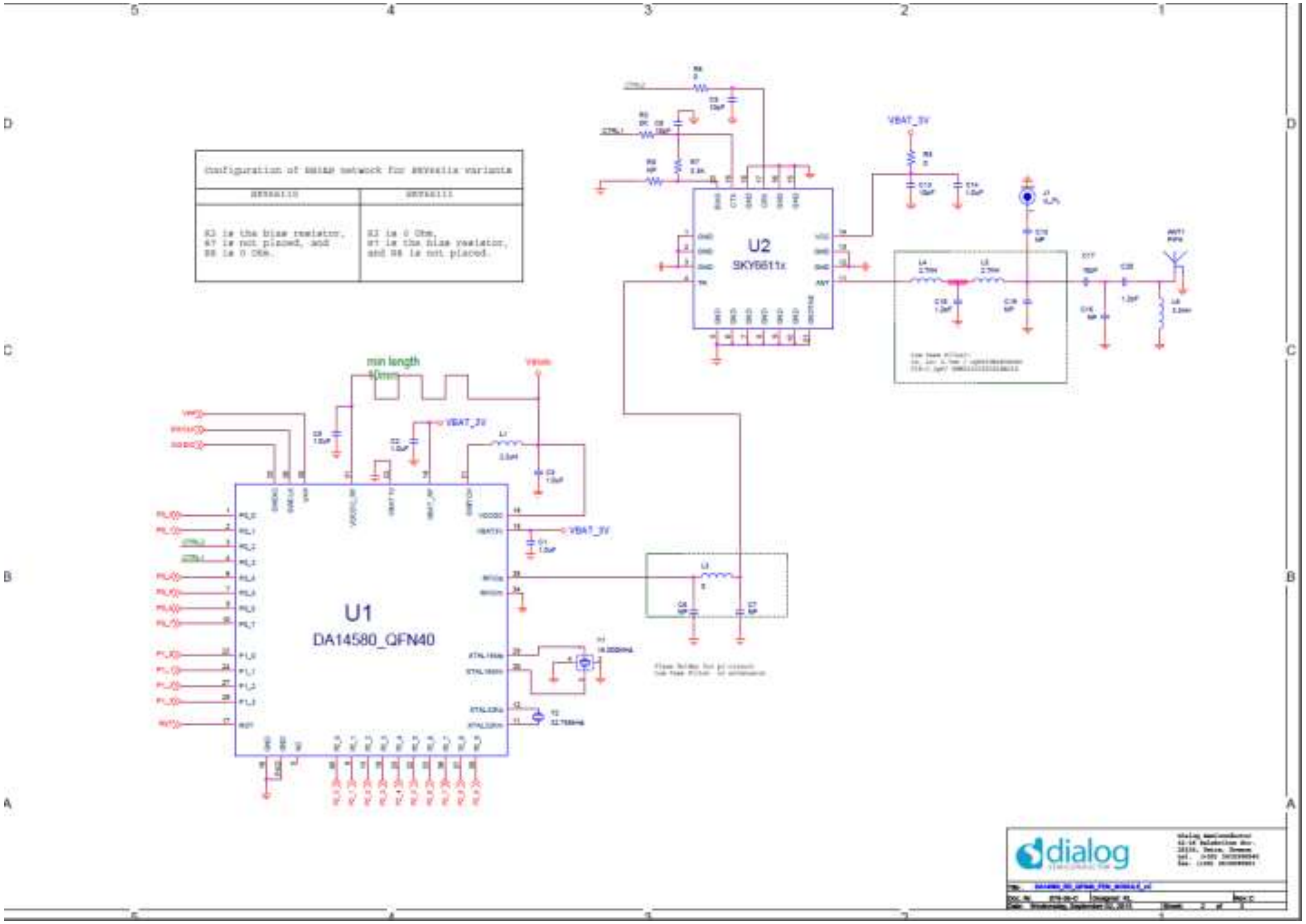



**Figure 25: Schematic of DA14580 Range Extender v.2 Module**

**Table 8: Bill of Materials**

| Ref. | Value | Description | Manuf. | MPN | Footpr. |
|---|---|---|---|---|---|
| U1 | DA14580_QFN40 | BT Low Energy System on a Chip | Dialog Semiconductor | DA14580-01AT1 | QFN40 |
| U2 | SKY66111 | Front-End Module, 2.4GHz-2.485GHz | Skyworks Solutions, Inc. | SKY66111-11 | MCM |
| L3, R3, R5, R6 | 0 | RES 0.0 OHM 1/20W 0201 SMD | Vishay/Dale | CRCW02010000Z0ED | 0201 |
| R7 | 3.3K | RES 3.3K OHM 50mW 1% 0201 SMD | Vishay/Dale | CRCW02013K30FKED | 0201 |
| Y1 | 16.000MHz | CRYSTAL 16MHZ 10PF SMD | TXC Corporation | 7M-16.000MEEQ-T | |
| Y2 | 32.768kHz | CRYSTAL 32.768KHZ 7PF SMD | Abracon Corporation | ABS07-32.768KHZ-7-T | |
| C1, C2, C3, C5, C14 | 1.0uF | CAP MLCC 1.0uF 10V X5R 10% | TDK Corporation | C1005X5R1A105K050BB | 0402 |
| C8, C9, C13, C17 | 10pF | CAP MLCC 0201 10pF 25volts C0G | Murata | GRM0335C1E100JA01D | 0201 |
| C18, C20 | 1.2pF | CAP MLCC 0201 1.2pF 25volts C0G +/-0.25pF | Murata | GRM0335C1E1R2CA01D | 0201 |
| L1 | 2.2uH | INDUCTOR Power 2.2uH, 500mA, 400MHz | Taiyo Yuden | BRL1608T2R2M | 0603 |
| L4,L5 | 2.7nH | Fixed Inductors 2.7 NH +-.1NH | Murata | LQP03TN2N7B00D | 0201 |
| L6 | 3.3nH | Fixed Inductors 3.3nH 0.1nH 500MHz | Murata | LQP03TN3N3B02D | 0201 |
| **Not Populated Components** | | | | | |
| **Ref.** | **Value** | **Description** | **Manuf.** | **MPN** | **Footpr.** |
| C6,C7,C15,C16,C19 | NP | Capacitors | | | |
| R8 | NP | Resistors | | | |
| ANT1 | | Printed Antenna | | | |
| TP1,TP2 | | Test Points | | | |
| J1 | NP | RF Connectors / Coaxial Connectors UMC STRT JACK RECEP SURFACE MOUNT | Johnson / Cinch Connectivity Solutions | 128-0711-201 | UMC |

## 4.8 Development Mode-Peripheral Pin Mapping

On the following table the pins used for development/ testing are described.

**Table 9: Development/ testing mode pin mapping**

| SoC Pin # | DA14580 assigned Pins | Function | SoC Pin # | DA14580 assigned Pins | Function |
|---|---|---|---|---|---|
| 1 | P0_0 | Available External Use | 21 | SWITCH | Connection for the external DCDC-converter inductor. |
| 2 | P0_1 | Available External Use | 22 | P1_0 | Available External Use |

| SoC Pin # | DA14580 assigned Pins | Function | SoC Pin # | DA14580 assigned Pins | Function |
|---|---|---|---|---|---|
| 3 | P0_2 | PA_Rx Enable | 23 | VBAT1V | |
| 4 | P0_3 | PA_Tx Enable | 24 | P1_1 | Available External Use |
| 5 | NC | | 25 | P1_5 | SWDIO |
| 6 | P0_4 | UART TX | 26 | P1_4 | SWCLK |
| 7 | P0_5 | UART RX | 27 | P1_2 | Available External Use |
| 8 | P2_1 | Available External Use | 28 | P1_3 | Available External Use |
| 9 | P0_6 | Available External Use | 29 | XTAL16Mp | |
| 10 | P0_7 | WLAN coexist | 30 | XTAL16Mm | |
| 11 | XTAL32Km | | 31 | VDCDC_RF | |
| 12 | XTAL32Kp | | 32 | P2_5 | Available External Use |
| 13 | P2_2 | Available External Use | 33 | P2_6 | Available External Use |
| 14 | VBAT_RF | | 34 | RFIOm | |
| 15 | VBAT3V | | 35 | RFIOp | |
| 16 | GND | | 36 | P2_7 | Available External Use |
| 17 | RST | RESET | 37 | P2_8 | Available External Use |
| 18 | P2_3 | Available External Use | 38 | VPP | |
| 19 | VDCDC | | 39 | P2_9 | Available External Use |
| 20 | P2_4 | Available External Use | 40 | P2_0 | Available External Use |
| *Note: Any available pin can be used for interfacing external SPI data Flash. See secondary boot loader document for further details[4] | | | | | |

By default in the secondary boot loader[4] all the SPI GPIO signals are assigned to Port0. However as it has been mentioned in paragraph 4.4.1, P0_2 and P0_3 pins are utilized to extract the radio control signals. So if SPI communication with a peripheral is needed, a modification in the configuration settings for the peripherals contained in header file periph_setup.h can be made.

```
// SPI Flash settings
// SPI Flash Manufacturer and ID
#define W25X10CL_MANF_DEV_ID (0xEF10)      // W25X10CL Manufacturer and ID
#define W25X20CL_MANF_DEV_ID (0xEF11)      // W25X10CL Manufacturer and ID
// SPI Flash options
#define W25X10CL_SIZE 131072               // SPI Flash memory size in bytes
#define W25X20CL_SIZE 262144               // SPI Flash memory size in bytes
#define W25X10CL_PAGE 256                  // SPI Flash memory page size in bytes
#define W25X20CL_PAGE 256                  // SPI Flash memory page size in bytes
#define SPI_FLASH_DEFAULT_SIZE 131072      // SPI Flash memory size in bytes
#define SPI_FLASH_DEFAULT_PAGE 256         // SPI Flash memory page size in bytes
//SPI initialisation parameters
#define SPI_WORD_MODE  SPI_8BIT_MODE
#define SPI_SMN_MODE   SPI_MASTER_MODE
#define SPI_POL_MODE   SPI_CLK_INIT_HIGH
#define SPI_PHA_MODE   SPI_PHASE_1
#define SPI_MINT_EN    SPI_NO_MINT
#define SPI_CLK_DIV    SPI_XTAL_DIV_2
// UART GPIOs assignment
#define UART_GPIO_PORT  GPIO_PORT_0
#define UART_TX_PIN     GPIO_PIN_4
#define UART_RX_PIN     GPIO_PIN_5
#define UART_BAUDRATE   baudrate_57K6
// SPI GPIO assignment
#define SPI_GPIO_PORT   GPIO_PORT_0
#define SPI_CS_PIN      GPIO_PIN_3
#define SPI_CLK_PIN     GPIO_PIN_0
#define SPI_DO_PIN      GPIO_PIN_6
#define SPI_DI_PIN      GPIO_PIN_5
// EEPROM GPIO assignment
#define I2C_GPIO_PORT   GPIO_PORT_0
#define I2C_SCL_PIN     GPIO_PIN_2
#define I2C_SDA_PIN     GPIO_PIN_3
```

**Figure 26: DA14580/581/583 configuration settings for peripherals, periph_setup.h**

## 4.9 Software

The following instructions are based DA14580_581_583_SDK_3.0.10.1. Instructions are valid for both Keil 4 and Keil 5 projects. Screenshots shown are in Keil 5.

**Inserting in a project (example in proximity reporter)**

1. Copy app_range_extender folder to dk_apps\src\modules\app\src\app_utils
2. Open the project and add `app_range_extender.c` in app group of the keil project
3. Right click 'apps' and select "Add existing files to Group 'app' ". Add `app_range_extender.c`

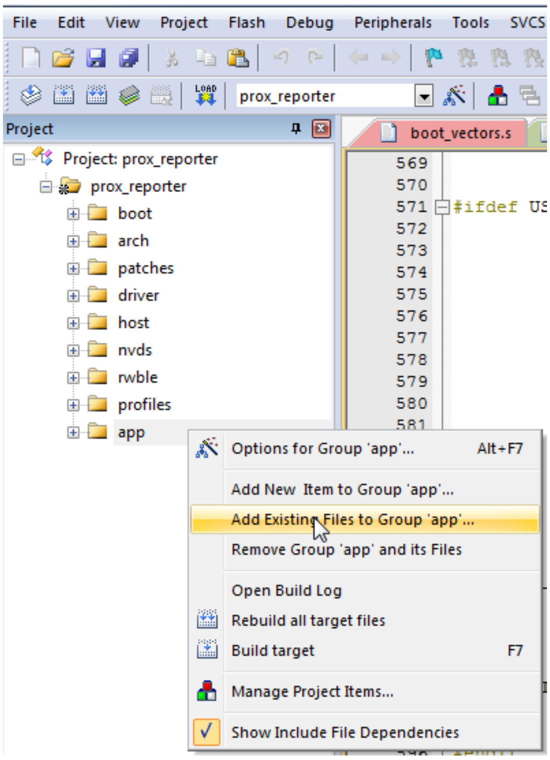



**Figure 27: Step 2 of adding app_range_extender**

4. Add the app_range_extender folder in the compiler include paths.

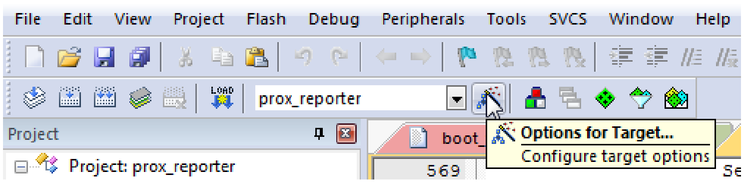



**Figure 28: Step 3a of adding app_range_extender**

In the target options, select the C/C++ tab and in the end add:
`.\..\..\..\..\ src\modules\app\src\app_utils\app_range_extender`
(separate from the previous path with a semicolon)

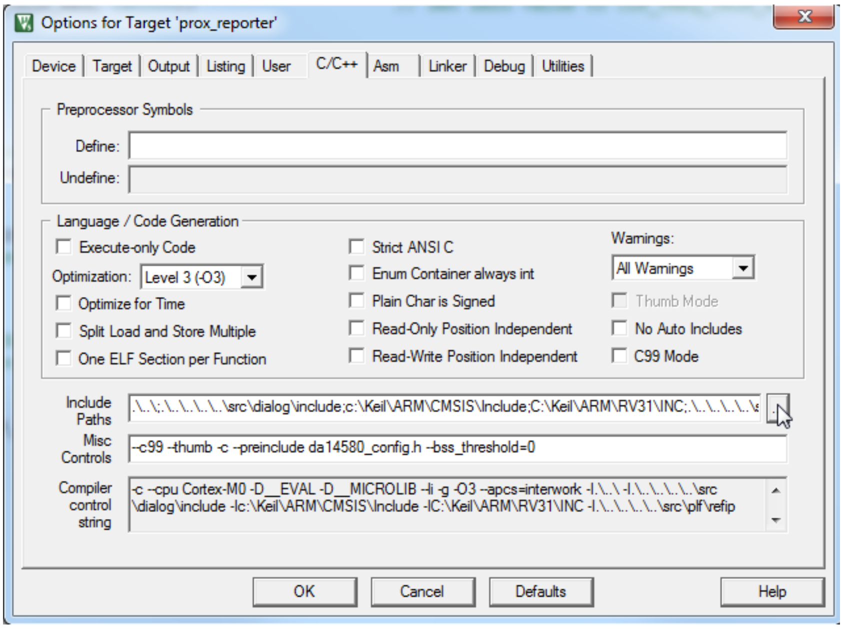



Figure 29: Step 3b of adding app_range_extender

5. In app_<project>_proj file, add the line:

   #include "app_range_ext.h" in the Include files section

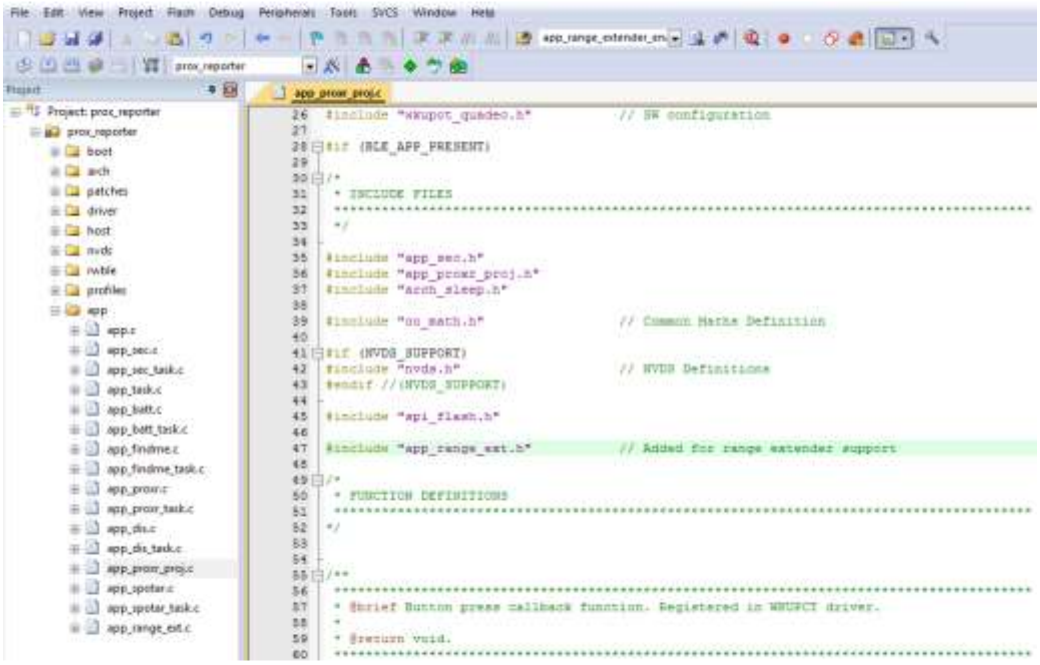


Figure 30: Step 4a of adding app_range_extender

and call app_range_extender_enable() in app_init_func()

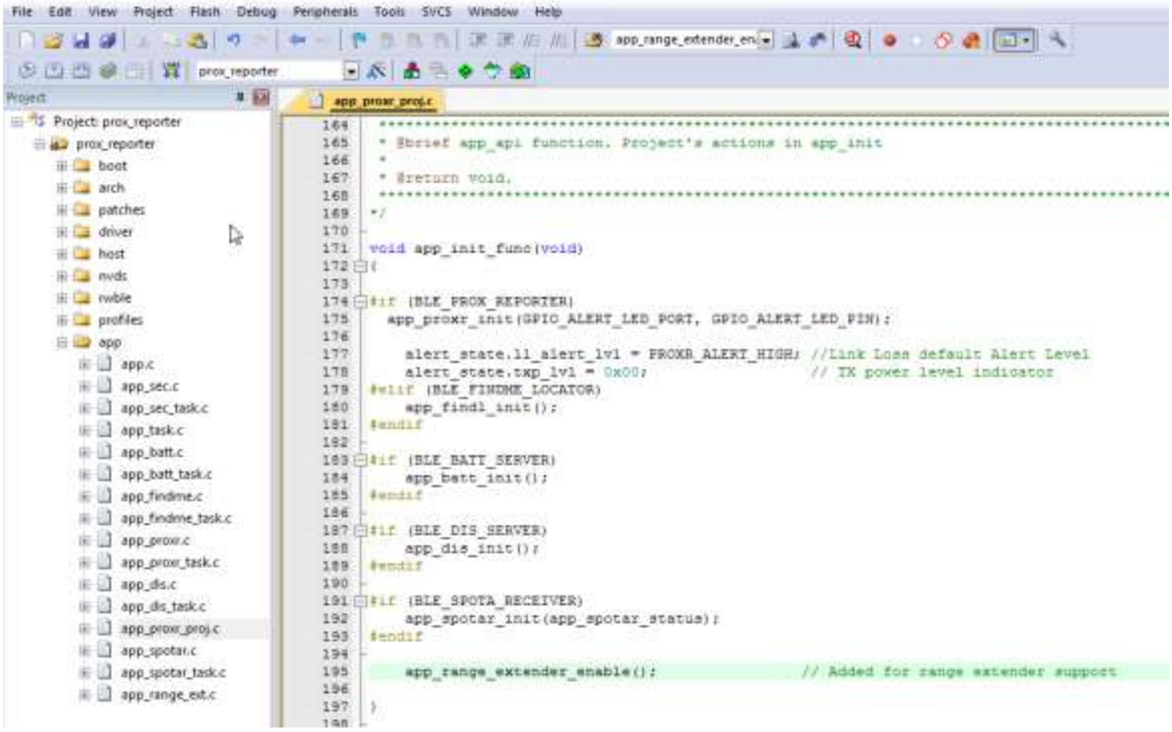



**Figure 31: Step 4b of adding app_range_extender**

6. In `periph_setup.c`, add the line:
   `#include "app_range_ext.h"` in the Include files section

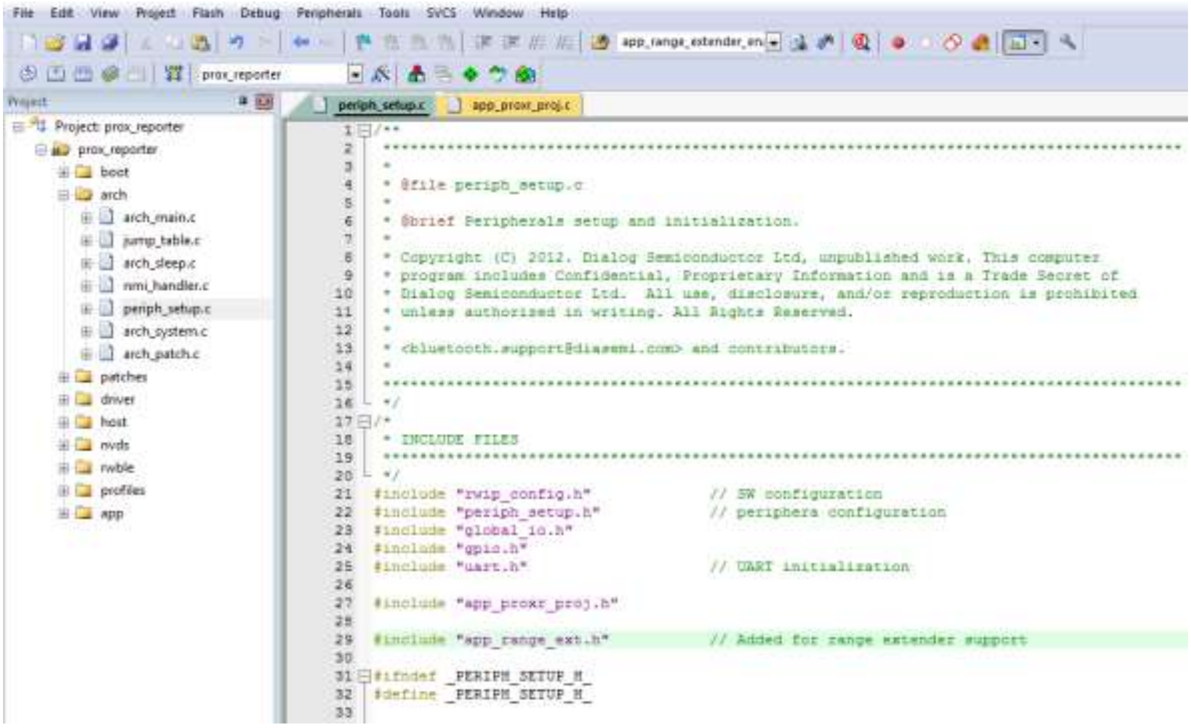



**Figure 30: Step 5a of adding app_range_extender**

and call `app_range_extender_enable()` at the end of `periph_init()`

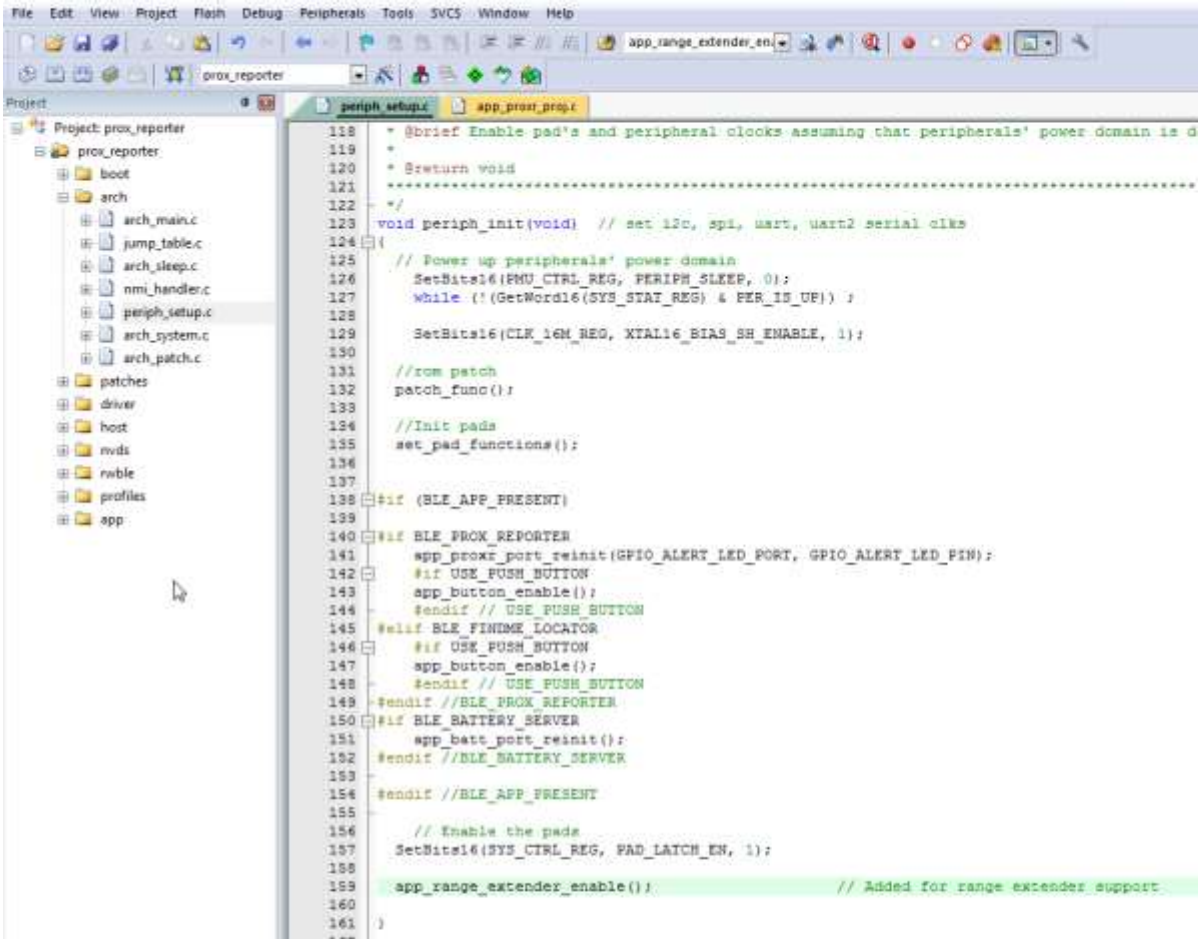


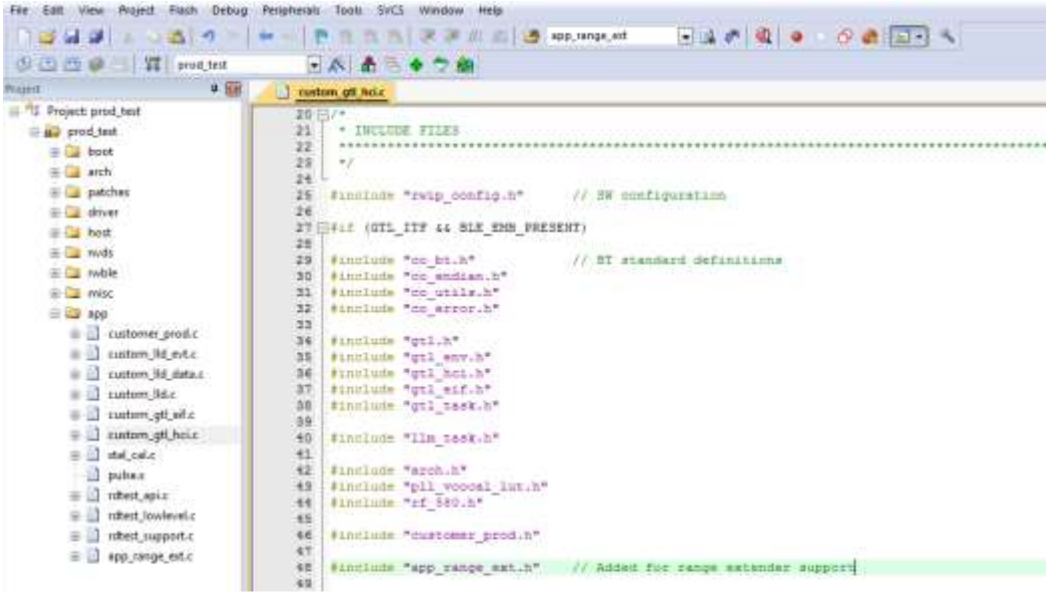

**Figure 31: Step 5b of adding app_range_extender**

### Inserting in the production test tool

1. Follow above steps **1-3**
2. In `custom_gtl_hci.c`, add the line:

   `#include "app_range_ext.h"` in the Include files section




and call app_range_extender_enable()in gtl_hci_rx_header_func()

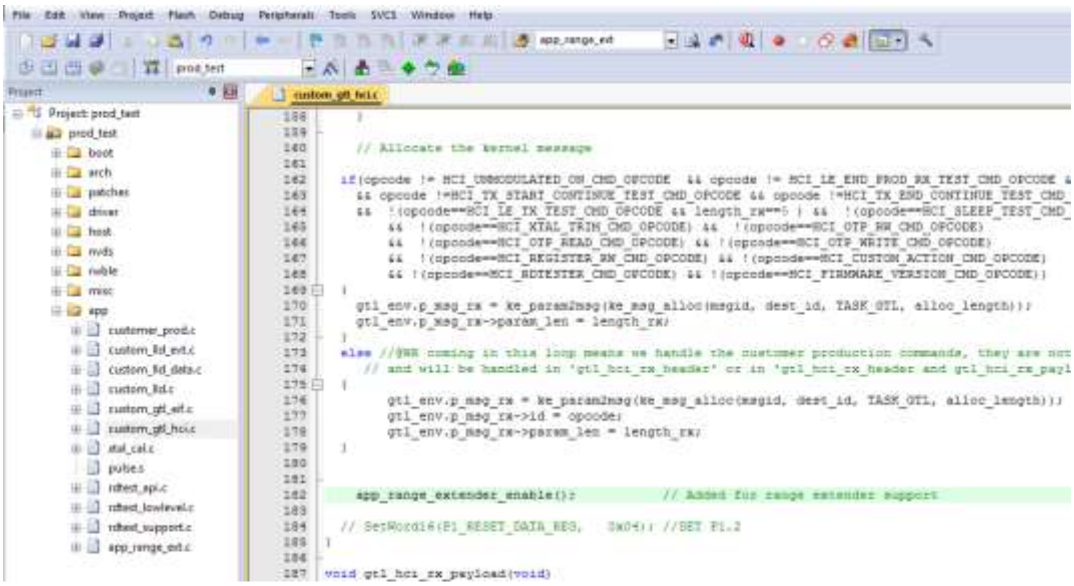



**Figure 32: Inserting app_range_extender in the production test tool**

# 5 Measurements

## 5.1 Basic performance measurements

### 5.1.1 Receiver sensitivity (conducted)

#### 5.1.1.1 Test description

In this test the Rx sensitivity of Range Extender v.2 Module was measured.

#### 5.1.1.2 Test setup

The Range Extender v.2 Module was mounted on a DK Development Board with the use of an intermediate interposer board. The R&S®CBT Bluetooth® Tester from Rohde & Schwarz was used. An RF cable assembly was connected to J1 connector (UMC RF Series) and at the other end through an attenuator to the R&S®CBT Bluetooth® Tester from Rohde & Schwarz. The results from a dirty transmitter on one of the boards are reported below.

#### 5.1.1.3 Test results

The conducted RF sensitivity with dirty transmitter shows that the sensitivity is better than -90 dBm for the most of the channels.

**Table 10: Conducted Rx sensitivity**

**Bluetooth Low Energy PER Search**

*TX Start Level: -96.0 dBm, Packets: 1500, Payload: PRBS 9, Length: 37 Bytes, Dirty Transmitter: specification table*

*Channelscan: from Ch. 00 to Ch. 39, with detailed values*

| | | |
|---|---|---|
| RX Level @ *Ch: 00, PER: 28.93%, Count: 13* | -91.40 dBm | ✔ |
| RX Level @ *Ch: 01, PER: 29.33%, Count: 06* | -91.40 dBm | ✔ |
| RX Level @ *Ch: 02, PER: 30.33%, Count: 12* | -91.40 dBm | ✔ |
| RX Level @ *Ch: 03, PER: 31.20%, Count: 07* | -90.60 dBm | ✔ |
| RX Level @ *Ch: 04, PER: 30.60%, Count: 07* | -91.50 dBm | ✔ |
| RX Level @ *Ch: 05, PER: 29.67%, Count: 11* | -91.40 dBm | ✔ |
| RX Level @ *Ch: 06, PER: 31.53%, Count: 08* | -91.40 dBm | ✔ |
| RX Level @ *Ch: 07, PER: 31.47%, Count: 09* | -91.10 dBm | ✔ |
| RX Level @ *Ch: 08, PER: 31.07%, Count: 06* | -91.40 dBm | ✔ |
| RX Level @ *Ch: 09, PER: 28.93%, Count: 09* | -91.10 dBm | ✔ |
| RX Level @ *Ch: 10, PER: 31.13%, Count: 11* | -91.00 dBm | ✔ |
| RX Level @ *Ch: 11, PER: 32.47%, Count: 10* | -90.70 dBm | ✔ |
| RX Level @ *Ch: 12, PER: 29.93%, Count: 12* | -91.10 dBm | ✔ |
| RX Level @ *Ch: 13, PER: 28.80%, Count: 09* | -91.10 dBm | ✔ |
| RX Level @ *Ch: 14, PER: 28.93%, Count: 09* | -91.10 dBm | ✔ |
| RX Level @ *Ch: 15, PER: 31.60%, Count: 14* | -89.20 dBm | ✔ |
| RX Level @ *Ch: 16, PER: 29.27%, Count: 13* | -91.20 dBm | ✔ |
| RX Level @ *Ch: 17, PER: 29.33%, Count: 09* | -91.10 dBm | ✔ |
| RX Level @ *Ch: 18, PER: 31.40%, Count: 12* | -91.30 dBm | ✔ |
| RX Level @ *Ch: 19, PER: 29.40%, Count: 09* | -90.40 dBm | ✔ |
| RX Level @ *Ch: 20, PER: 30.07%, Count: 10* | -91.20 dBm | ✔ |
| RX Level @ *Ch: 21, PER: 29.60%, Count: 05* | -91.20 dBm | ✔ |
| RX Level @ *Ch: 22, PER: 29.33%, Count: 09* | -91.20 dBm | ✔ |
| RX Level @ *Ch: 23, PER: 29.00%, Count: 11* | -90.80 dBm | ✔ |
| RX Level @ *Ch: 24, PER: 29.80%, Count: 05* | -91.20 dBm | ✔ |
| RX Level @ *Ch: 25, PER: 31.53%, Count: 06* | -91.40 dBm | ✔ |
| RX Level @ *Ch: 26, PER: 29.93%, Count: 10* | -90.90 dBm | ✔ |
| RX Level @ *Ch: 27, PER: 29.93%, Count: 09* | -90.40 dBm | ✔ |
| RX Level @ *Ch: 28, PER: 29.40%, Count: 18* | -90.90 dBm | ✔ |
| RX Level @ *Ch: 29, PER: 30.20%, Count: 11* | -91.00 dBm | ✔ |
| RX Level @ *Ch: 30, PER: 29.73%, Count: 18* | -90.90 dBm | ✔ |
| RX Level @ *Ch: 31, PER: 28.87%, Count: 06* | -88.80 dBm | ✔ |
| RX Level @ *Ch: 32, PER: 31.00%, Count: 09* | -91.10 dBm | ✔ |
| RX Level @ *Ch: 33, PER: 29.93%, Count: 05* | -91.20 dBm | ✔ |
| RX Level @ *Ch: 34, PER: 29.33%, Count: 10* | -90.90 dBm | ✔ |
| RX Level @ *Ch: 35, PER: 29.53%, Count: 07* | -90.60 dBm | ✔ |
| RX Level @ *Ch: 36, PER: 31.13%, Count: 05* | -91.20 dBm | ✔ |
| RX Level @ *Ch: 37, PER: 29.40%, Count: 11* | -91.00 dBm | ✔ |
| RX Level @ *Ch: 38, PER: 31.13%, Count: 12* | -91.10 dBm | ✔ |
| RX Level @ *Ch: 39, PER: 29.07%, Count: 10* | -90.30 dBm | ✔ |

### 5.1.2 Transmitter output power (conducted)

#### 5.1.2.1 Test description

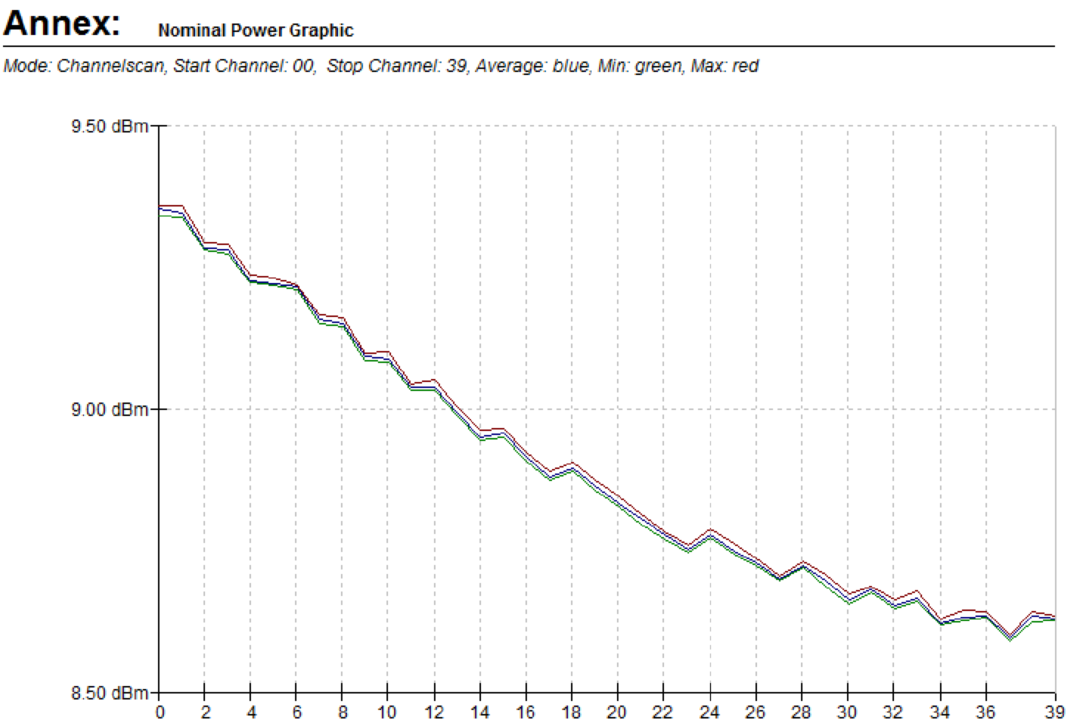
In this test the conducted RF output power of Range Extender v.2 Module was measured.

#### 5.1.2.2 Test setup

The Range Extender v.2 Module was mounted on a DK Development Board with the use of an intermediate interposer board. In order to evaluate the TX output power, production test firmware was used. Conducted transmitted output power was measured by using the R&S®CBT Bluetooth® Tester from Rohde & Schwarz. An RF cable assembly was connected to J1 connector (UMC RF Series) and at the other end through an attenuator to the R&S®CBT Bluetooth® Tester. Bursts of 10 packets were transmitted by the DA14580. The packet length was 37 and the pattern was “01010101”. Three channels were recorded, channels 0, 19 and 39.

#### 5.1.2.3 Test results

Measurements were performed on a number of samples.




**Red**: maximum

**Blue**: average

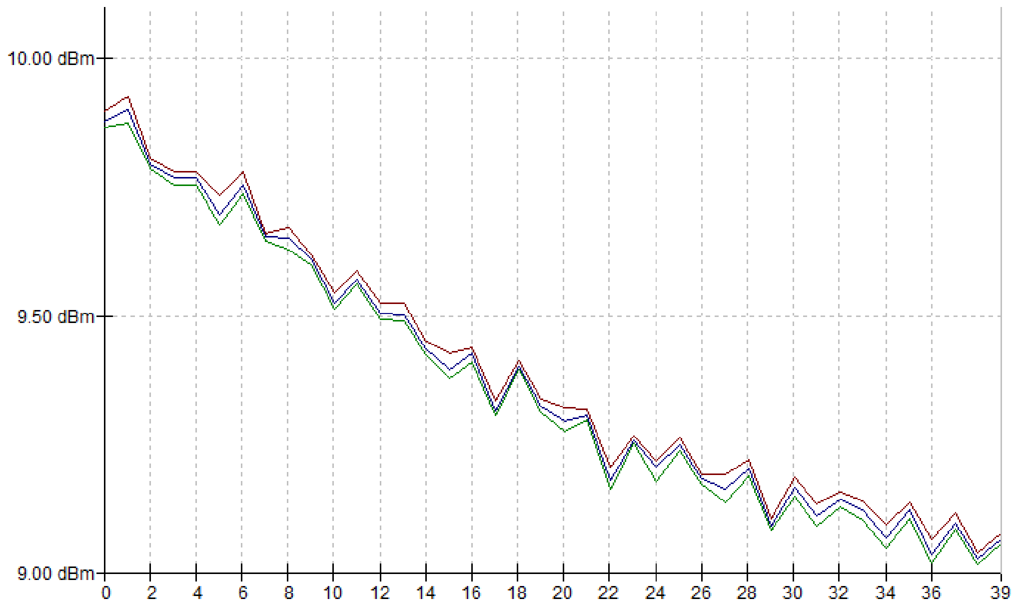
**Green**: minimum

**Figure 33: Nominal conducted output power per channel**

# Annex: Peak Power Graphic

Mode: Channelscan, Start Channel: 00, Stop Channel: 39, Average: blue, Min: green, Max: red




**Red**: maximum

**Blue**: average

**Green**: minimum

**Figure 34: Peak conducted output power per channel**

**Table 11: Tx output power**

| Parameter | $V_{BAT\_3V}$ (V) | $P_{OUT}$ (dBm) | | |
|---|---|---|---|---|
| | | CH00 | CH19 | CH39 |
| Nominal Tx output power, average | +3.0 | 9.35 | 8.87 | 8.57 |
| Peak Tx output power, average | +3.0 | 9.88 | 9.34 | 9.03 |

### 5.1.3 Current consumption

#### 5.1.3.1 Test setup

The board used in the test presented optimal RF performance. The integrated printed antenna was used to perform the measurements.

Following instruments were used for the test:

- Multimeter
- 3 V, 100 mA power source
- Agilent N6705B

The current profiles were evaluated using proximity reporter firmware with embedded PA control. During this test the Advertisement, Connection and Extended Sleep modes were evaluated.

#### 5.1.3.2 Advertisement mode

For this measurement the DUT was supplied by 3 V. FW was downloaded and the JTAG programmer and then it was disconnected.

**Table 12: Peak current during Advertisement mode**

| Channel | Frequency (MHz) | Parameter | $I_{PEAK}$ (mA) |
|---|---|---|---|
| 0 | 2402 | Ipeak0, TX | 16.15 |
| 12 | 2440 | Ipeak12, TX | 15.91 |
| 39 | 2480 | Ipeak39, TX | 14.68 |


**Figure 35: Supplu current during an Advertisement frame**

#### 5.1.3.3 Connection mode

For this measurement the DUT was supplied by 3 V. FW was downloaded and the JTAG programmer was disconnected and connection with an iPhone 4S was established.

**Table 13: Peak current during Connection mode**

| Parameter | $I_{PEAK}$ (mA) |
|---|---|
| Ipeak, TX | 16.74 |


**Figure 36: Supply current during a Connection frame**

#### 5.1.3.4 Extended sleep mode

For this measurement the DUT was supplied by 3 V. FW was downloaded and the JTAG programmer was disconnected. FW was setting the RF path to Rx.

**Table 14: Average current in Extended Sleep mode**

| Parameter | $I_{AV}$ (µA) |
|---|---|
| Imean | 1.58 |


Figure 37: Supply current during Extended Sleep mode

## 5.2 FCC/ ETSI Measurements

### 5.2.1 Emission limitation conducted (transmitter)

#### 5.2.1.1 Test description

In this test the level of the harmonics produced by the Tx path was measured.

#### 5.2.1.2 Test setup

The Range Extender v.2 Module was mounted on a DK Development Board with the use of an intermediate interposer board. In order to evaluate the harmonics levels production, the production test firmware with embedded PA signal control was used. The boards under test, were set into continuous transmit mode. An RF cable assembly was connected to J1 connector (UMC RF Series) and in the other end were connected to the spectrum analyser. Three channels were tested, channels 0, 19 and 39.

#### 5.2.1.3 Test results

**Table 15: Conducted Tx harmonics at $V_{BAT\_3V}$ = 3.0 V @ CH00, CH19, CH39**

| Parameter (dBm) | CH00 – 2402MHz | CH19 – 2440MHz | CH39 – 2480 MHz |
|---|---|---|---|
| 2nd harmonic power | -52.40 | -52.56 | -52.40 |
| 3rd harmonic power | -58.54 | -58.04 | -56.76 |
| 4th harmonic power | -55.70 | -55.64 | -56.81 |
| 5th harmonic power | -59.52 | -58.06 | -56.66 |

All measurements comply with the limits specified in FCC 15.247/ Sub clause (d). Please note that the second harmonic power is has a 11.2 dBm margin to the FCC limits (-41.2 dBm).

### 5.2.2 Emission limitation radiated (transmitter)

#### 5.2.2.1 Test description

In this test the level of radiated spurious emissions produced in the Tx mode was measured in the certified semi-anechoic RF chamber at AT4W labs.

#### 5.2.2.2 Test setup

For the measurements, the device under test comes with its OTP preloaded with the production test firmware with embedded PA signal control. This software can be configured to generate the required test patterns. The hardware configuration for the test is shown in Figure 38.

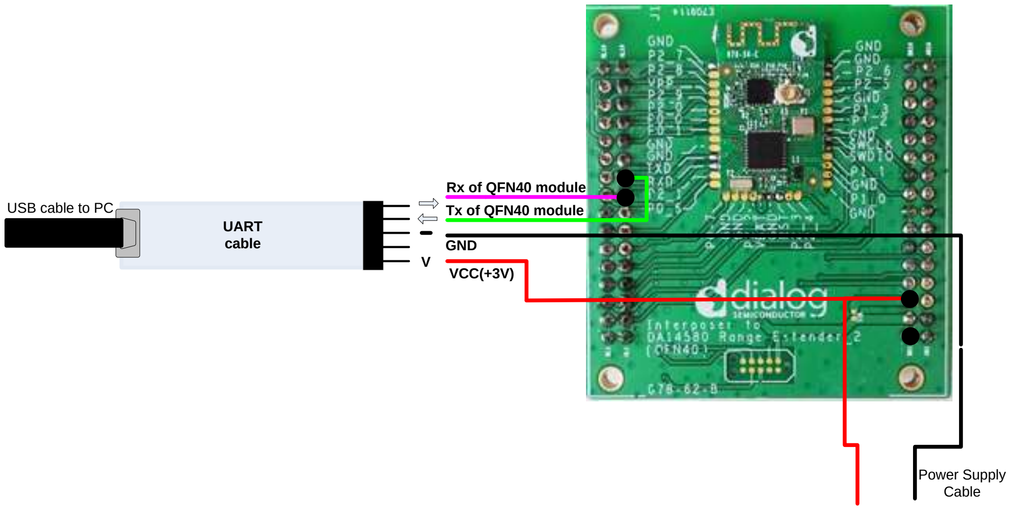



**Figure 38: Range Extender v.2 mounted on the interposer board for radiated measurements**

The board was set to continuous transmission mode with a 100% duty cycle.

The measurements were conducted for the range of 30 to 1000MHz, 1 GHz to 3 GHz and from 3GHz to 18 GHz according to FCC Part 15C and for the range of 30 to 1000 MHz and 1 to 12.75 GHz for ETSI EN 300 328 1.8.1.

A board with Nominal RF Output Power equal to +9.3 dBm was used for this test.

The situation and orientation was varied to find the maximum radiated emission. It was also rotated 360° and the antenna height was varied from 1 to 4 meters to find the maximum radiated emission. Measurements were made in both horizontal and vertical planes of polarization. All tests were performed in a semi-anechoic chamber at a distance of 3 m for the frequency range 30 MHz-1000 MHz and at distance of 1m for the frequency ranges above 1 GHz.

### 5.2.2.3 Test results

The results of the radiated measurements are given on Figure 39 to Figure 51. All measured FCC values comply with the emission limits specified in FCC 14.247/ Sub-clause (d). Additionally radiated emissions limits which fall in restricted bands, as defined in FCC 15.205(a) also comply with the radiated emissions limits specified in 15.209.

As far as ETSI transmitter unwanted emission in the spurious domain, they all comply to the limits described in ETSI 300 328 1.8.1 paragraph 4.3.1.9.2.

FREQUENCY RANGE 30 MHz-1000 MHz.

Highest Channel.

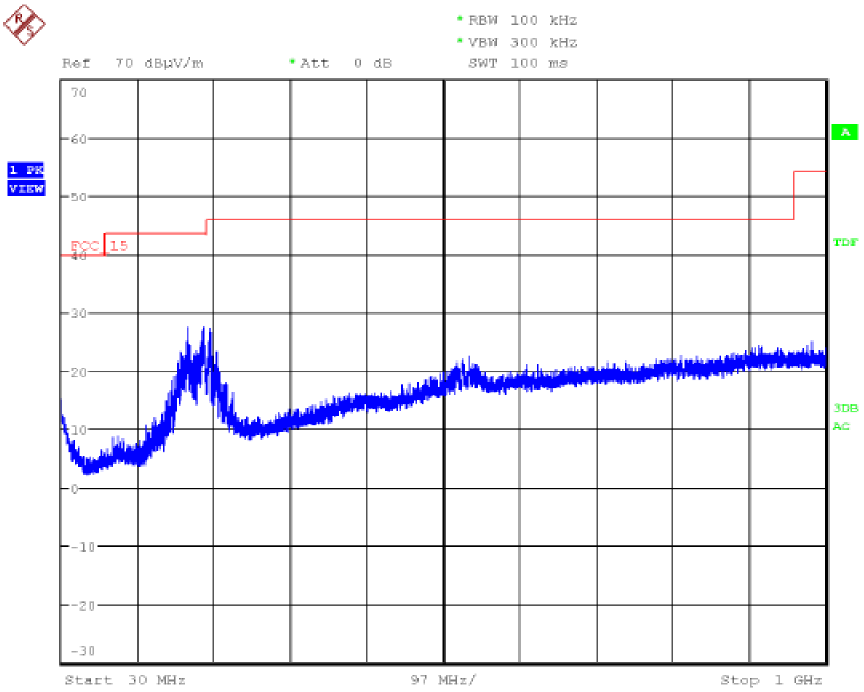
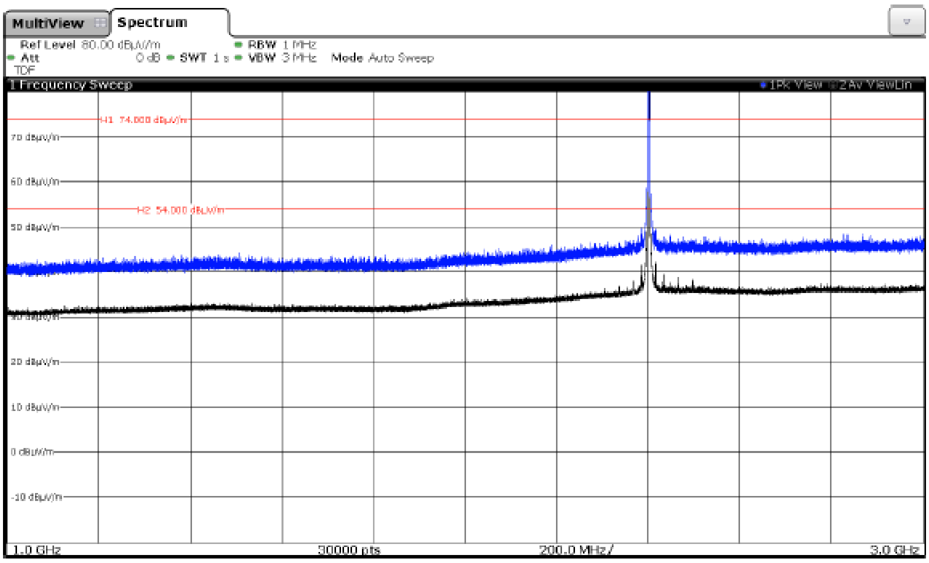



**Figure 39: FCC, Frequency Range from 30MHz to 1 GHz, CH39**

FREQUENCY RANGE 1 GHz to 3 GHz.

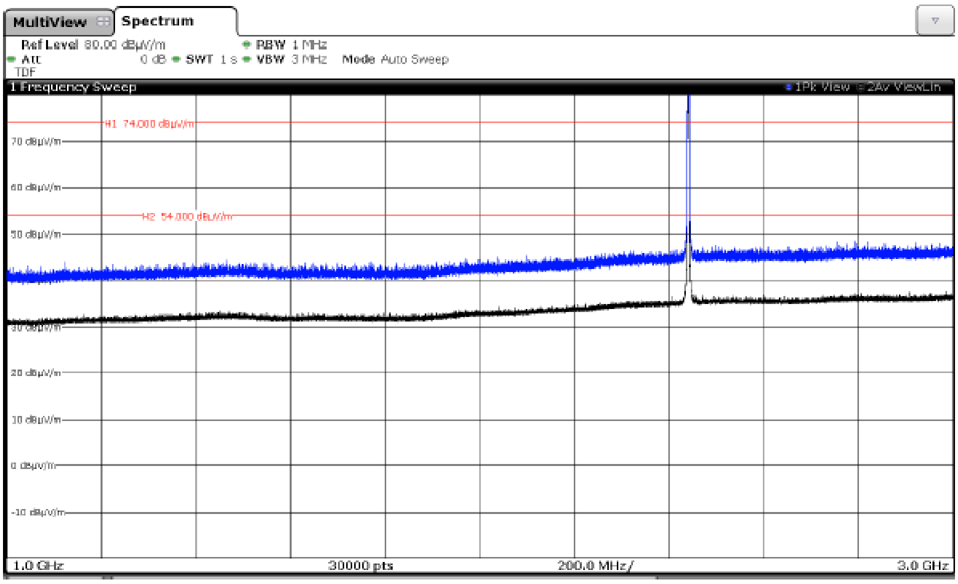
**CHANNEL:** Lowest (2402 MHz).




Note: The peak shown in the plot above the limit is the carrier frequency.

**Figure 40: FCC, Frequency from 1GHz to 3GHz, CH00**

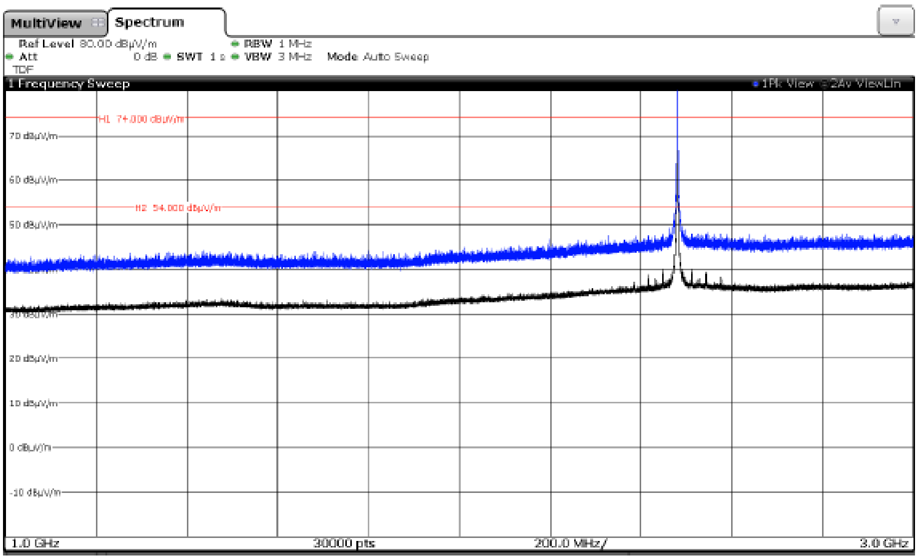
CHANNEL: Middle (2440 MHz).




Note: The peak shown in the plot above the limit is the carrier frequency.

**Figure 41: FCC, Frequency from 1GHz to 3GHz, CH19**

CHANNEL: Highest (2480 MHz).




Note: The peak shown in the plot above the limit is the carrier frequency.

**Figure 42: FCC, Frequency from 1GHz to 3GHz, CH39**

FREQUENCY RANGE 3 GHz to 18 GHz.

CHANNEL: Lowest (2402 MHz).

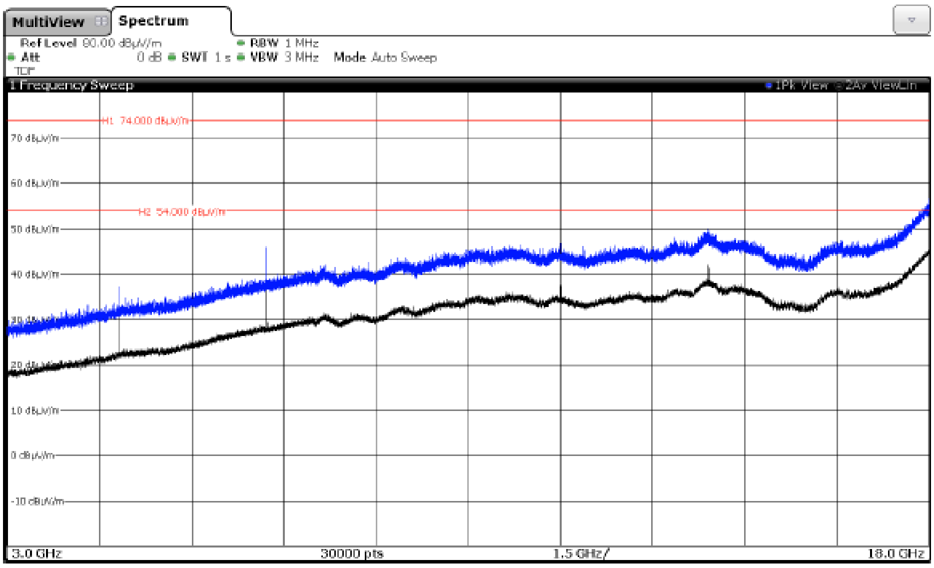



**Figure 43: FCC, Frequency from 3GHz to 18GHz, CH00**

CHANNEL: Middle (2440 MHz).

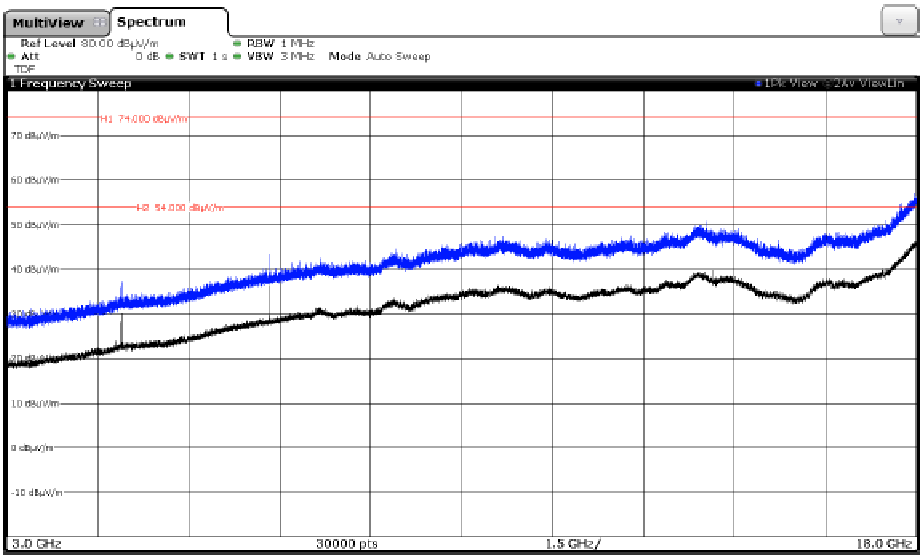



**Figure 44: FCC, Frequency from 3GHz to 18GHz, CH19**

CHANNEL: Highest (2480 MHz).

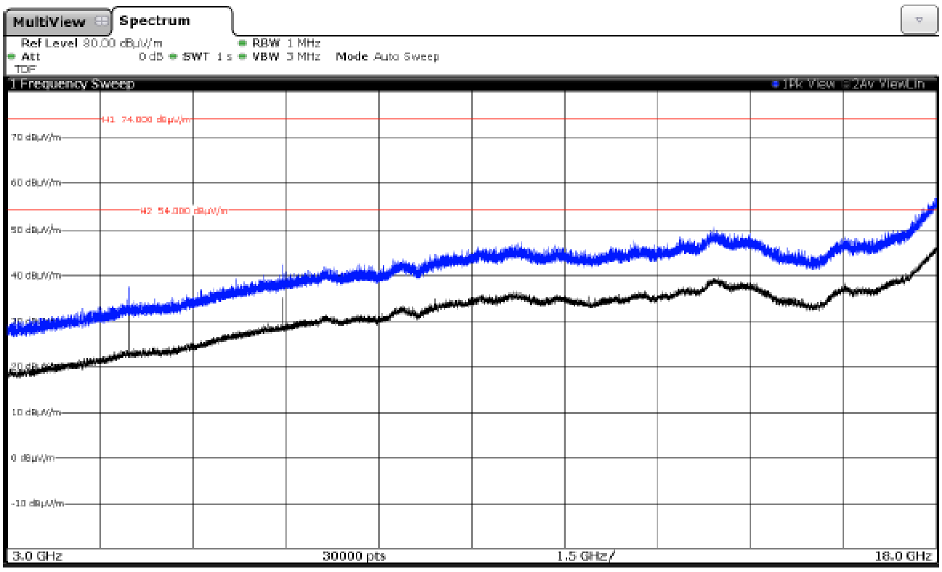



**Figure 45: FCC, Frequency from 3GHz to 18GHz, CH39**

FREQUENCY RANGE 2.31 GHz to 2.39 GHz. (RESTRICTED BAND)

CHANNEL: Lowest (2402 MHz).

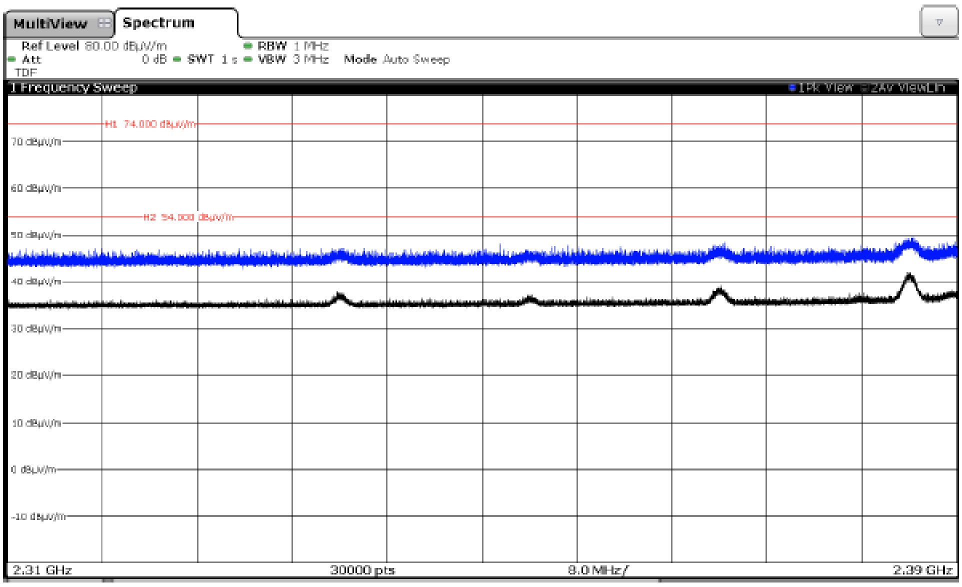



**Figure 46: FCC, Frequency Range 2.31 GHz to 2.39 GHz (Restricted band- CH00)**

CHANNEL: Middle (2440 MHz).

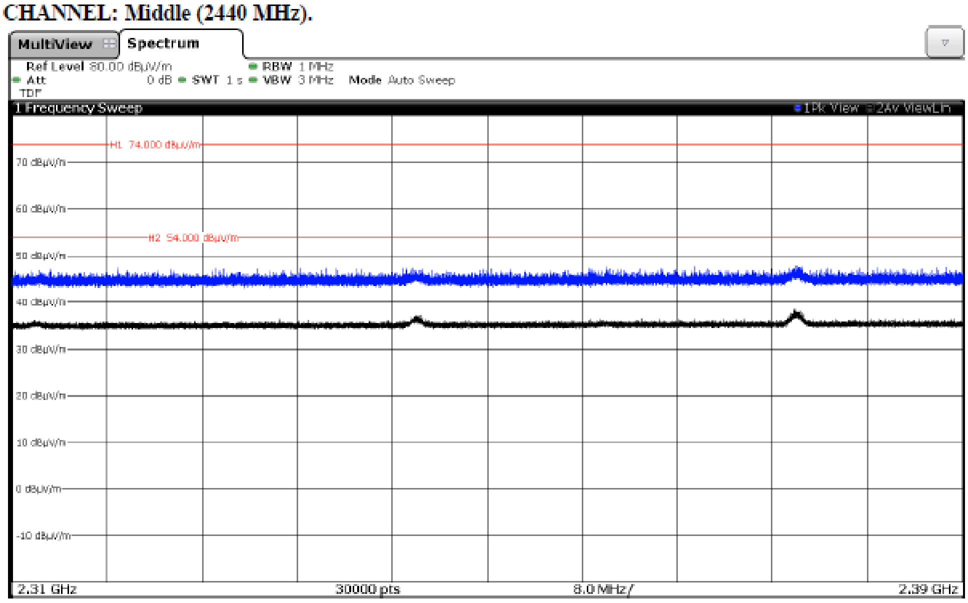



Figure 47: FCC, Frequency Range 2.31 GHz to 2.39 GHz (Restricted band- CH19)

CHANNEL: Highest (2480 MHz).

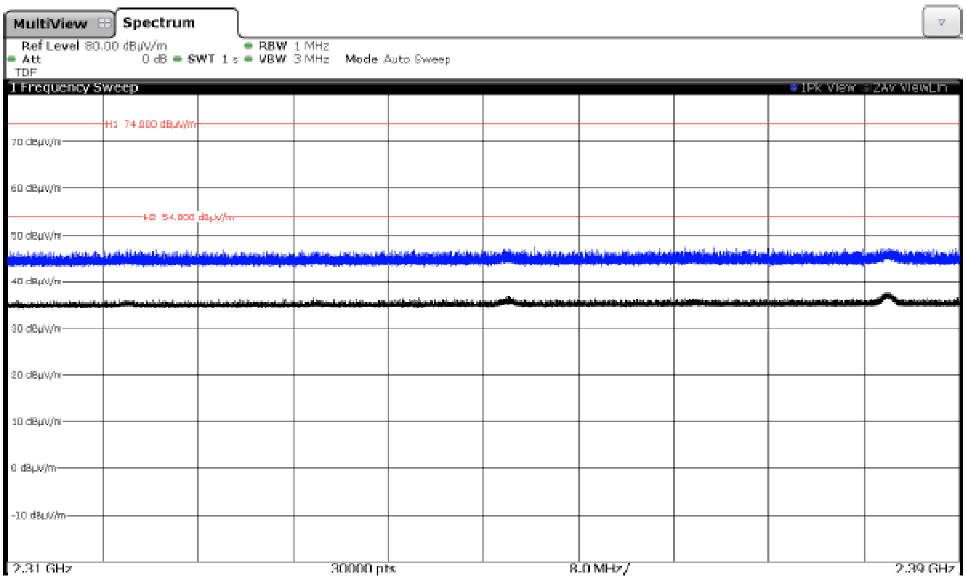



Figure 48: FCC, Frequency Range 2.31 GHz to 2.39 GHz (Restricted band- CH39)

FREQUENCY RANGE 2.4835 GHz to 2.5 GHz. (RESTRICTED BAND)

**CHANNEL: Lowest (2402 MHz).**

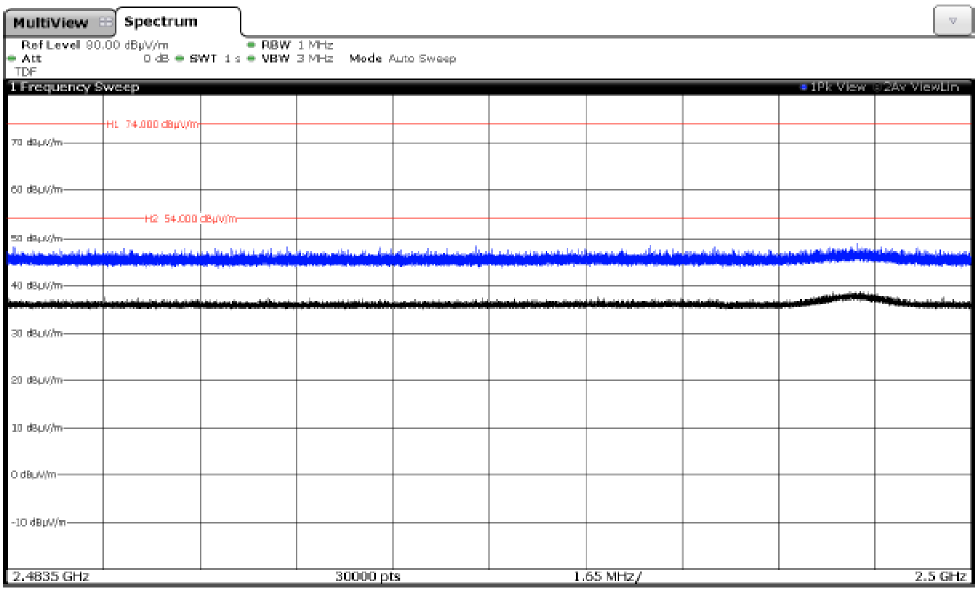



**Figure 49: FCC, Frequency Range 2.4385 GHz to 2.5 GHz (Restricted band- CH00)**

**CHANNEL: Middle (2440 MHz).**

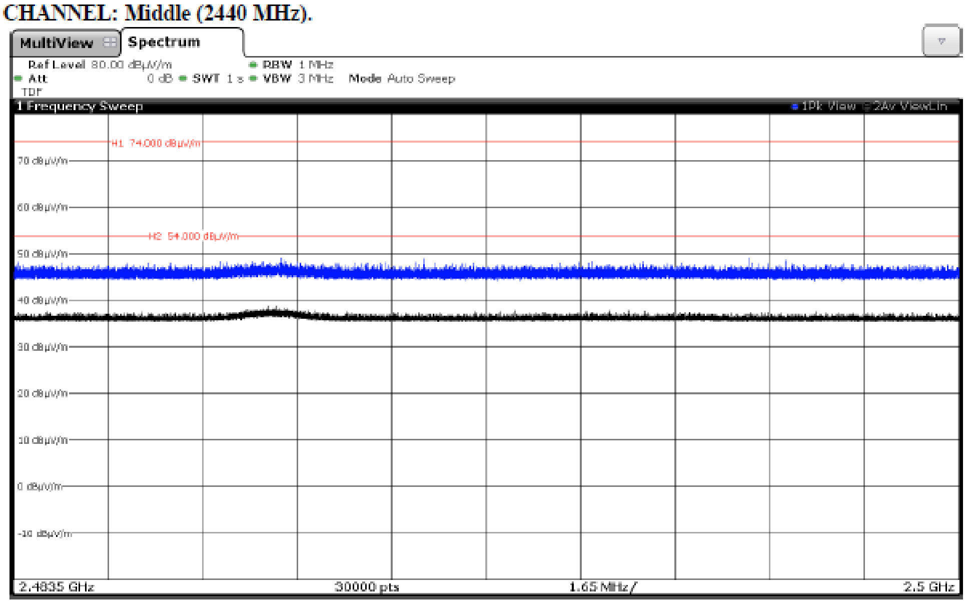



**Figure 50: FCC, Frequency Range 2.4385 GHz to 2.5 GHz (Restricted band- CH19)**

CHANNEL: Highest (2480 MHz).

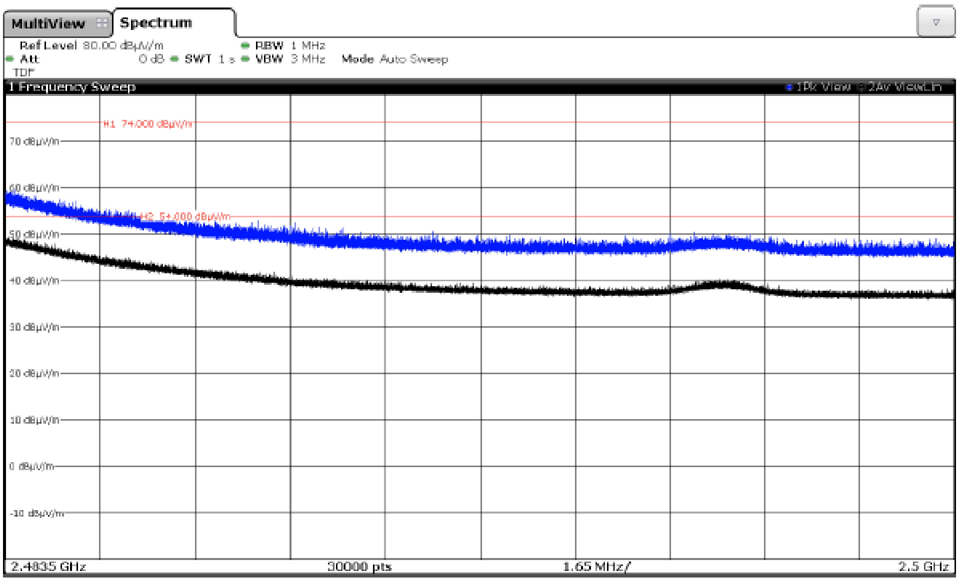



**Figure 51: FCC, Frequency Range 2.4385 GHz to 2.5 GHz (Restricted band-CH39)**

# 6 FCC/IC Certification and CE marking

## 6.1 Standards and conformity assessment

## 6.2 FCC requirements regarding the end product and end user

### 6.2.1 End product marking

### 6.2.2 End product literature

## 6.3 Permissive changes

## 6.4 Industry Canada requirements regarding the end product and end user

### 6.4.1 End product marking

### 6.4.2 End product literature

# 7 Appendix A: Range Extender v.2 with SPI Data Flash

Range Extender v.2 can be used with external SPI Data Flash Memory. Any available pins can be used to interface the external data Flash. The appropriate configuration settings for peripherals must be set in secondary boot loader as described in paragraph 4.8. The following application example schematic contains Range Extender v.2 with external SPI Data Flash.

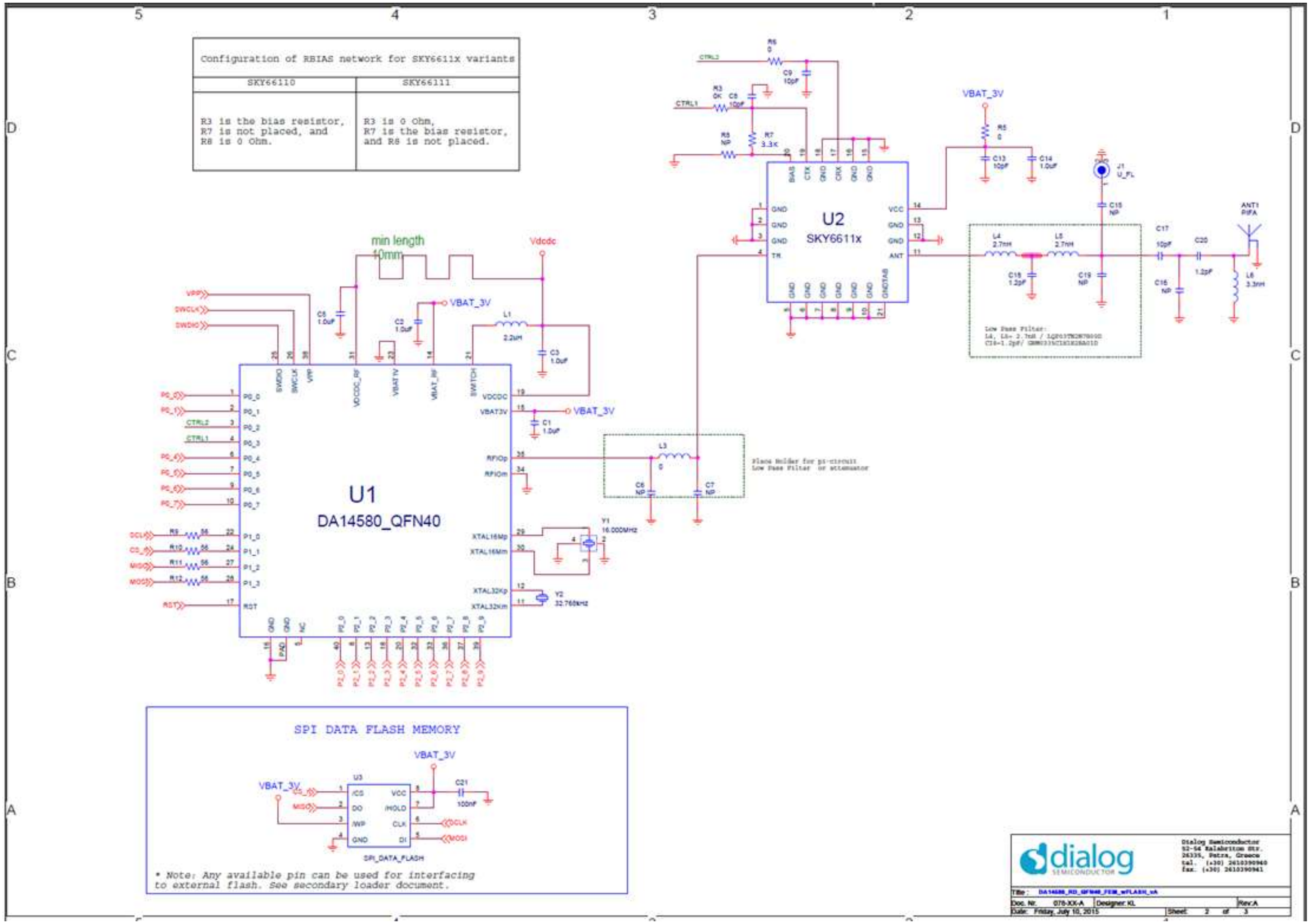



Figure 52: Range Extender v.2 Module with external SPI Flash

# 8 Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | 16-07-2015 | **Initial version**. *FCC/ETSI final certification reports pending for end of September 2015. All measurement regarding compliance to FCC/ETSI will be updated from the final certification reports. All FCC/ ETSI tests have been found to pass.* |
| 1.1 | 14-09-2015 | **Initial version:** *modification related to reduction of the output power.* |
| 2.0 | With final FCC/ETSI reports | **The document will be updated in the following sections.**<br>● Chapter 4.9: Software: upgrade with version SDK 5.02<br>● Chapter 4.10: Test platform (future chapter): PRO DK Interposer Description<br>● Chapter 5.3: FCC/ETSI Measurements: upgrade with final results<br>● Chapter 6: FCC/IC Certification and CE marking |
| 2.1 | 29-Dec-2021 | Updated logo, disclaimer, copyright. |

# DA14580 Range Extender v.2 Reference Application

## Status Definitions

| Status | Definition |
|---|---|
| DRAFT | The content of this document is under review and subject to formal approval, which may result in modifications or additions. |
| APPROVED<br>or unmarked | The content of this document has been approved for publication. |

## RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.