User Manual

DA1468x Range Extender Daughterboard

UM-B-074

Abstract

This document describes the hardware system setup of a range extender daughterboard based on the Dialog DA14680/681 Bluetooth® low energy SoC and the Skyworks SKY66112-11 Front End Module. Target hardware: DA1468x/DA1510x_db_aQFN60 – Board Number: 224-23-D. Target silicon: DA14680/681.

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1 Terms and Definitions

BLE	Bluetooth low energy
BOM	Bill of Materials
CIB	Communication Interface Board
CLI	Command Line Interface
CSA5	(Bluetooth) Core Specification Addendum 5
DCF	Dynamic Control Function
DCR	Direct Current Resistance
DCXO	Digitally Controlled Crystal Oscillator
DUT	Device Under Test
EIRP	Effective Isotropic Radiated Power
FEM	Front End Module
FSM	Finite State Machine
FW	Firmware
HW	Hardware
IFA	Inverted-F Antenna
LNA	Low Noise Amplifier
LPM	Low Power Mode
LPF	Low Pass Filter
PA	Power Amplifier
PCBA	Printed Circuit Board Assembled
PCB	Printed Circuit Board
RF	Radio Frequency
RFCU	RF Control Unit
RMS	Root Mean Square
RX	receive(r)
SoC	System on Chip
SWD	Serial Wire Debug (interface)
TX	transmit(ter)
n.a.	not available

2 References

[1] Bluetooth Core Specification Addendum 5, 15 December 2015, Bluetooth SIG.

[2] UM-B-060, DA1468x/DA1510x Pro-Development Kit, User Manual, Dialog Semiconductor.

[3] DA14681 Low Power Bluetooth Smart 4.2 SoC, Datasheet, Dialog Semiconductor.

[4] UM-B-065, Bluetooth Smart Communication Interface Board, User Manual, Dialog Semiconductor.

[5] SKY66112-11, Datasheet, Skyworks Inc.

[6] AN-B-061, DA1468x Application hardware design guidelines, Application Note, Dialog Semiconductor.

3 Introduction

The DA1468x/DA1510x_db_aqfn60_FEM_vD (224-23-D) is a reference design for extending the range of a Bluetooth® low energy system based on the Dialog Semiconductor DA14681 SoC, where enhanced RF transmitted power is presented. The DA14680/681 Range Extender daughterboard serves as a reference design to potential customers requesting enhanced BLE RF Output Power up to +13.5 dBm. Physically, the daughterboard consists of a 4-layer PCBA where the digital and power interfaces of the DA14680/681 are accessible to the user.

This document presents the system, technical specifications, physical dimensions and test results.

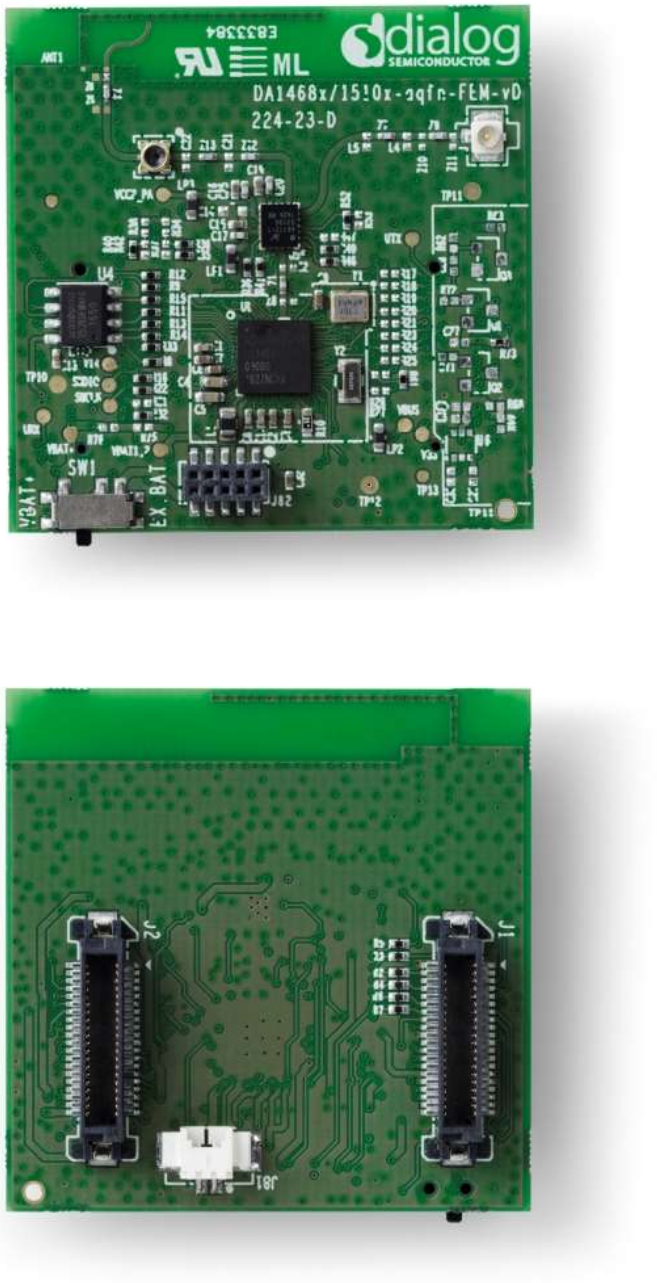


Figure 1: PCB of the DA14680/681 Range Extender (224-23-D)

4 System Overview

4.1 Features

- Highly integrated DA14680 or DA14681 Bluetooth low energy 4.2 SoC
- Can be used stand-alone or as a data pump on a system with an external processor
- Complies to Bluetooth v4.2, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)
- BLE transmit output power > +10 dBm, compliant with BLE v4.2 + CSA5 (see Ref. [1])
- Includes two crystal oscillators: 16 MHz (XTAL16M) and 32.738 kHz (XTAL32K)
- Access to processor via JTAG, SPI, UART or I2C interface
- 18 general purpose I/Os with programmable voltage levels
- Operating voltage: 1.7 V to 4.75 V.
- On-board printed inverted F-type antenna (Figure 4)
- uFL connector for external antennas (Figure 4)
- RF connector for conducted measurements (Figure 4)
- BLE Radio transceiver[1]:
  - +13.5 dBm transmit output power
  - -95.5 dBm receiver sensitivity
- Supply current[2]:
  - TX: max. current < 59 mA
  - RX: max. current < 10 mA
  - Extended - Sleep current: 4.5 µA
- 43 mm x 43 mm, 4 layer PCBA
- Operating temperature: –40 ºC to +85 ºC
- Test FW based on SDK 1.0.8

Table 1: Electrical Characteristics

Parameter[3]	Value
Average TX power	+13.5 dBm
RX sensitivity[4]	-95.5 dBm
Max. current consumption in TX mode	59 mA
Max. current consumption in RX mode	10 mA
Average current consumption during sleep mode	4.5 µA

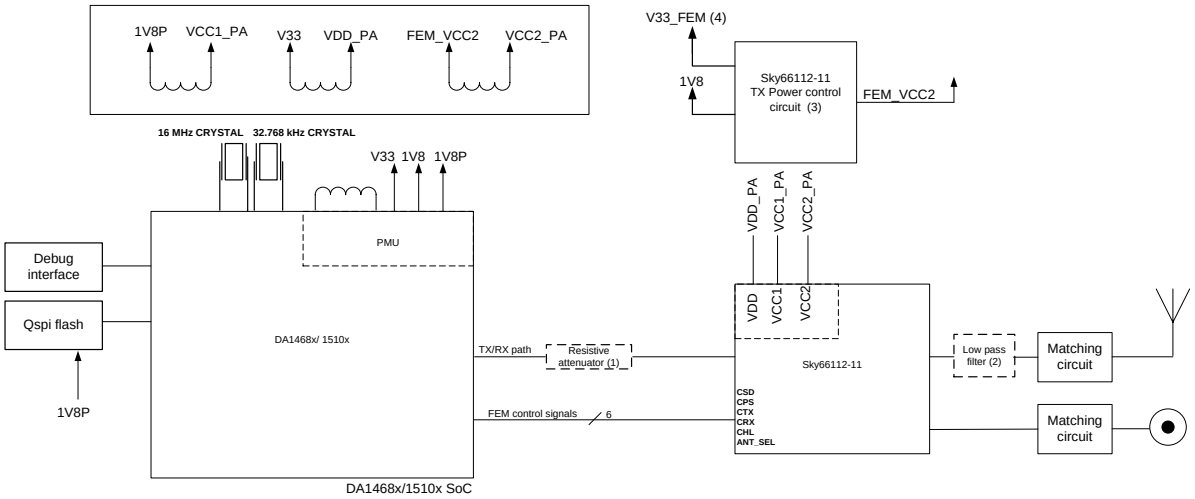
[1] FCC part 15.247,15.209 compliance.
[2] Normal operation using SDK ble_adv_demo application, TX output power +13.5 dBm.
[3] Current measured using SDK 1.0.8 ble_adv_demo, configuration CHL = 0, LPM2 (FEM_VCC2 = 1.2 V), RF_TX_PWR_REG = 2.
[4] Dirty transmitter: ON, 1500 packets, payload PRBS9 length 255 bytes.

4.2 System Description

The system consists of:

- DA14680 or DA14681 SoC in aQFN60 package (the main implementation and testing was done with DA14681)
- Sky66112-11 RF Front End Module (SKY66112-11_203225G)
- QSPI Data Flash memory (dual package wlcsp-w25q80ew, soic8-W25Q80EWSNIG-default)
- Crystals 16 MHz (or 32 MHz) and 32.768 kHz
- Can be supplied from a Li-Poly battery
- Mating headers for connecting to a DA1468x PRO Motherboard

A system overview is shown in Figure 2.



Legend:

(1) Resistive attenuator application is possible.

(2) Low pass filter application is possible.

(3) RF TX Output Control Circuit.

(4) Only for DA1510x.

Figure 2: Block Diagram of Range Extender (224-23-D)

4.3 System Interface

DA14680/681 Range Extender daughterboard is plugged on headers J1, J2 of DA1468x PRO motherboard, as shown in Figure 3.

The PRO motherboard provides UART and JTAG (SWD) interfaces to the DA14680/681, current measurement circuitry, as well as breakout headers (J3, J4) for the available GPIOs and general purpose user peripherals. For more details on the functionality and specifications of the motherboard, refer to user manual UM-B-060 (Ref. [2]).

The system is powered via the Debug USB port (USB2). The daughterboard can also be independently programmed using an external battery connected to the on board Li-Poly battery connector (see section 5 for more details). The layout and main features of the daughterboard are shown in Figure 4.

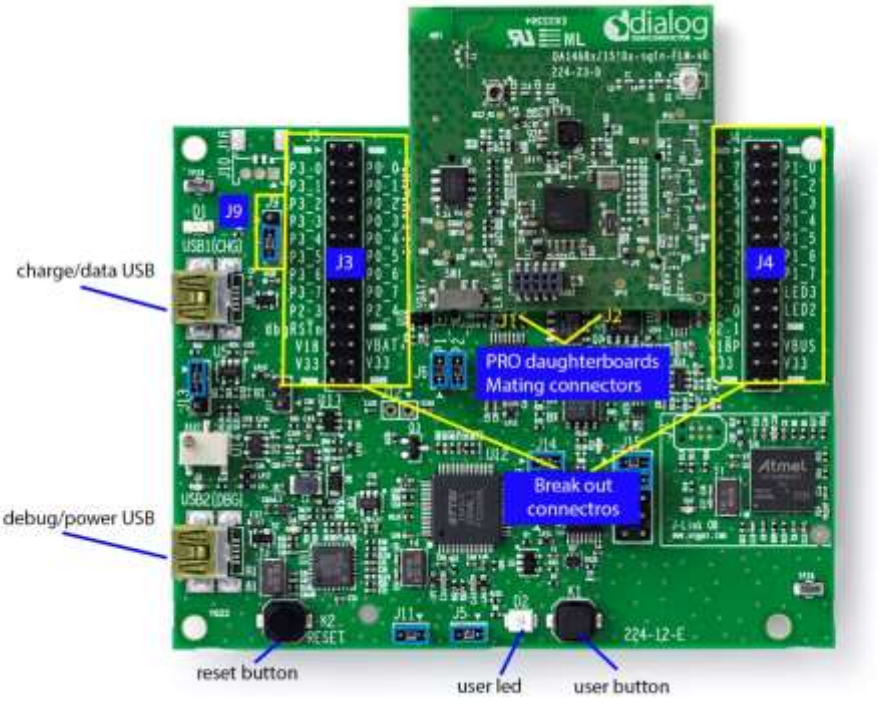


Figure 3: Range Extender (224-23-D) on a DA1468x Dev.Kit PRO Motherboard

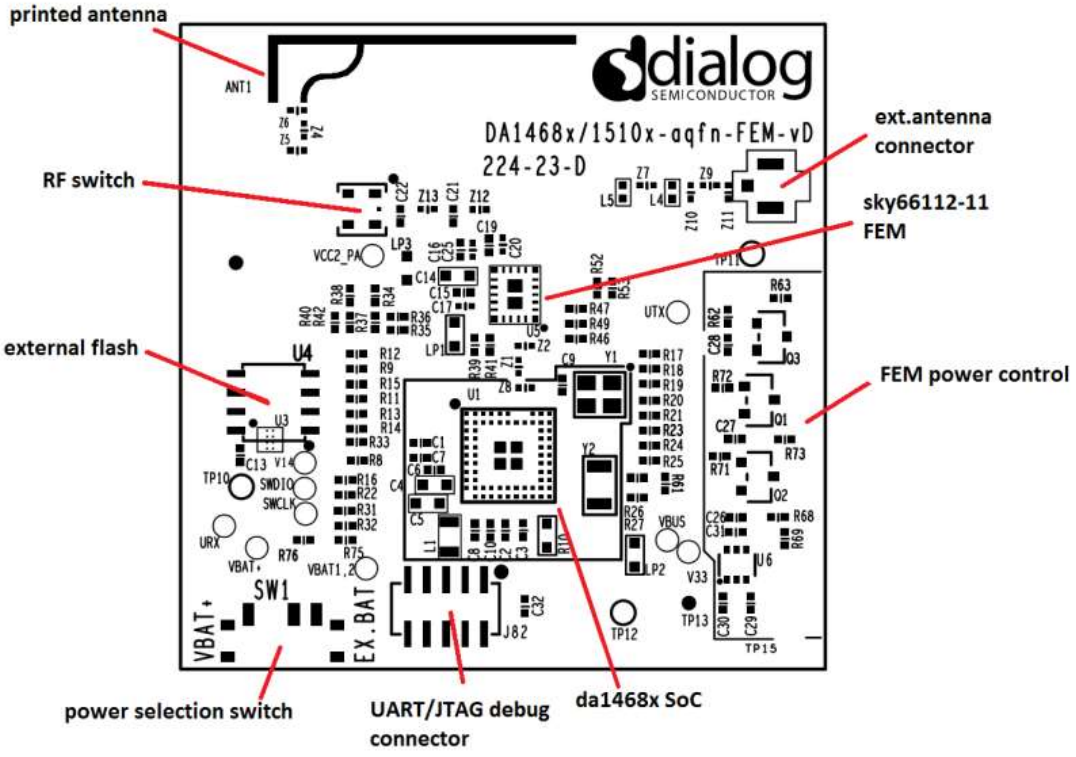


Figure 4: Layout of the Range Extender Daughterboard

DA1468x Range Extender Daughterboard

Another option for programming the DA14680/681 Range Extender is to connect the daughterboard to a CIB (Communication Interface Board) using a 2x10 cable as shown in Figure 5. The CIB provides UART and JTAG (SWD) interfaces to the DA14680/681 as well as power supply. If an external Li-Poly battery is used to supply the daughterboard, jumper J16 on the CIB must be removed. For more details on the Communication Interface Board, please refer to user manual UM-B-065 (Ref. [4]).

Figure 5: DA14680/681 Range Extender Connected to a Communication Interface Board (CIB)

5 Power

There are three options for powering the system when using DA1468x Dev.Kit PRO Motherboard:

- The PRO motherboard's voltage regulator (VLDO, see Ref. [2]) – total current capability approx. 300 mA.
- A Li-Poly rechargeable battery on the PRO motherboard.
- A Li-Poly rechargeable battery on the daughterboard of DA14680/681 range extender.

The power source to the daughterboard is selectable with SW1 as shown in Figure 6.

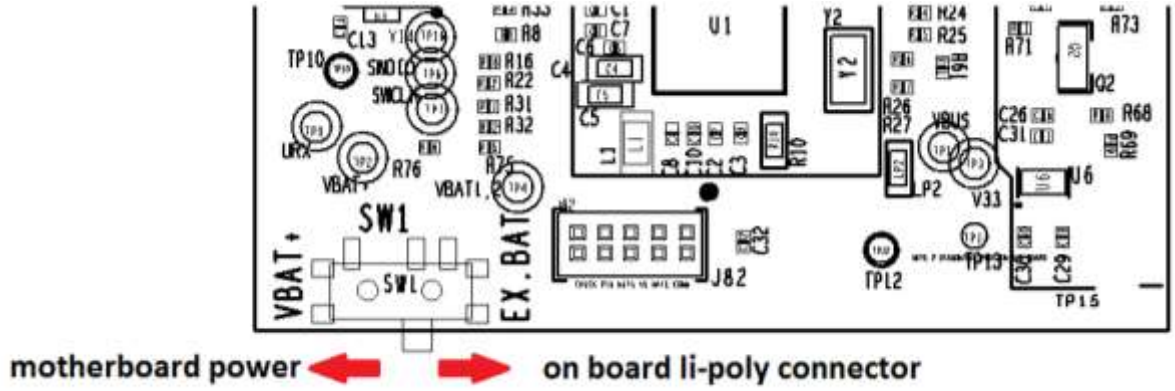


Figure 6: SW1 Position for Each Power Scheme

The different configurations for each of the power schemes using the DA1468x Dev.Kit PRO Motherboard are described in Table 2.

Table 2: Jumper/Switch Settings for Power Schemes of DA1468x Dev.Kit PRO Motherboard

Power Scheme	Indication	SW1	J9	USB1	USB2
Motherboard LDO	VBAT	Left	2-3	-	Power + debug
Li-Poly Battery mounted on motherboard	External battery	Left	1-2	Power + charge	debug
Li-Poly Battery mounted on daughterboard	External battery	Right	-	Power + charge	debug

When using the CIB board, there are two options for powering the system:

- Power supply coming from the USB of CIB.
- A Li-Poly rechargeable battery on the daughterboard of DA14680/681 range extender.

The different configurations for the power schemes using the CIB board are described in Table 3.

Table 3: Jumper/Switch Settings for Power Schemes of CIB Board

Power Scheme	Indication	SW1	J16
Power supply from CIB	VBAT or External Battery	Left or Right	connected
Li-Poly Battery mounted on daughterboard	External battery	Right	not connected

6 Bluetooth Low Energy SoC

The DA14680/681 is a flexible System-on-Chip for Bluetooth® low energy applications, combining an application processor, memories, cryptography engine, power management unit, digital and analog peripherals and a Bluetooth low energy MAC engine and radio transceiver. An overview of the basic system is shown in Figure 7.

The DA14680/681 is based on an ARM® Cortex®-M0 CPU delivering up to 84 DMIPS and provides a flexible memory architecture, enabling code execution from embedded memory (RAM, ROM) or non-volatile memory (OTP or external Quad-SPI Flash). The DA14680 incorporates a QSPI Data Flash memory in the package, whereas the DA14681 requires an external QSPI Data Flash.

The advanced power management unit of the DA14681 enables it to run from primary and secondary batteries, as well as provide power to external devices. The on-chip charger and state-of-charge fuel gauge allow the DA14680/681 to natively charge rechargeable batteries over USB.

An on-chip PLL enables on-the-fly tuning of the system clock between 16 MHz and 96 MHz to meet high processing requirements. The system runs at 32 kHz LP clock during low power sleep modes or it goes to clock less deep sleep mode to save power.

The DA14680/681 SoC power management subsystem consists of:

- VBUS: Is the battery charger input as well as the USB bus voltage. A decoupling capacitor equal or less than 4.7 μF is placed close to VBUS pin.
- VBAT1: An external battery is connected on this pin. A 1 μF decoupling capacitor (C10) is required close to the pin (0402 package, 6.3 V). Voltage range for VBAT1 is 1.7 V to 4.75 V.
- VBAT2: Is the input of the SIMO DC-DC converter. It is shorted externally with VBAT1. A 1 μF decoupling capacitor (C8) is required next to the pin (0402 package, 6.3 V).
- V33: Output voltage rail, 3.3 V. A decoupling ceramic capacitor of 4.7 μF (C3), (0402 package, 6.3 V) is placed. V33 cannot be turned off.
- SIMO DC-DC converter outputs are: V18, V18P, V12, V14. The inductor needed for DC-DC operation is placed externally. A low DCR inductor (L1) of 470 nH, 0805 is connected on pins LX/LY.
- V18 and V18P: These voltage rails can deliver power to external devices, even when the system is in sleep mode. Decoupling ceramic capacitors (C4, C5) of 10 μF (0603 package, 16 V), are placed as close as possible to the V18 and V18P pins. The current delivery capability of the V18 and V18P power rails is 75 mA in active mode, while it is 2 mA in sleep mode.
- V12: Power rail supplies the digital core of the DA14680/681 and delivers up to 50 mA at 1.2 V when in active mode. A 4.7 μF decoupling capacitor (C6) is used (0402 package, 6.3 V).
- V14: Power rail delivers up to 20 mA at 1.4 V and should not be used to supply external devices. A 4.7 μF decoupling capacitor (C7) is placed close to the V14 pin (0402 package, 6.3 V).
- V14_RF: Input pin. It is shorted to V14 on the PCB layout. V14_RF powers the RF circuits via a number of dedicated internal LDOs. A 4.7 μF decoupling capacitor (C9) is placed as close to the V14_RF pin as possible.
- VDDIO: Flash interface supply voltage. It is connected to the same power rail as the Flash memory. A 1 μF decoupling capacitor (C1), is added (0402 package, 6.3 V).

The DA14680/681 radio transceiver characteristics are:

- 2.4 GHz CMOS transceiver with integrated balun
- 50 Ω matched single wire antenna interface
- Transmit output power in the range of 0 dBm to -4 dBm
- -93 dBm BLE receiver sensitivity
- Supply current at VBAT1 (3 V) for the RF part:
  - TX: 3.4 mA
  - RX: 3.7 mA

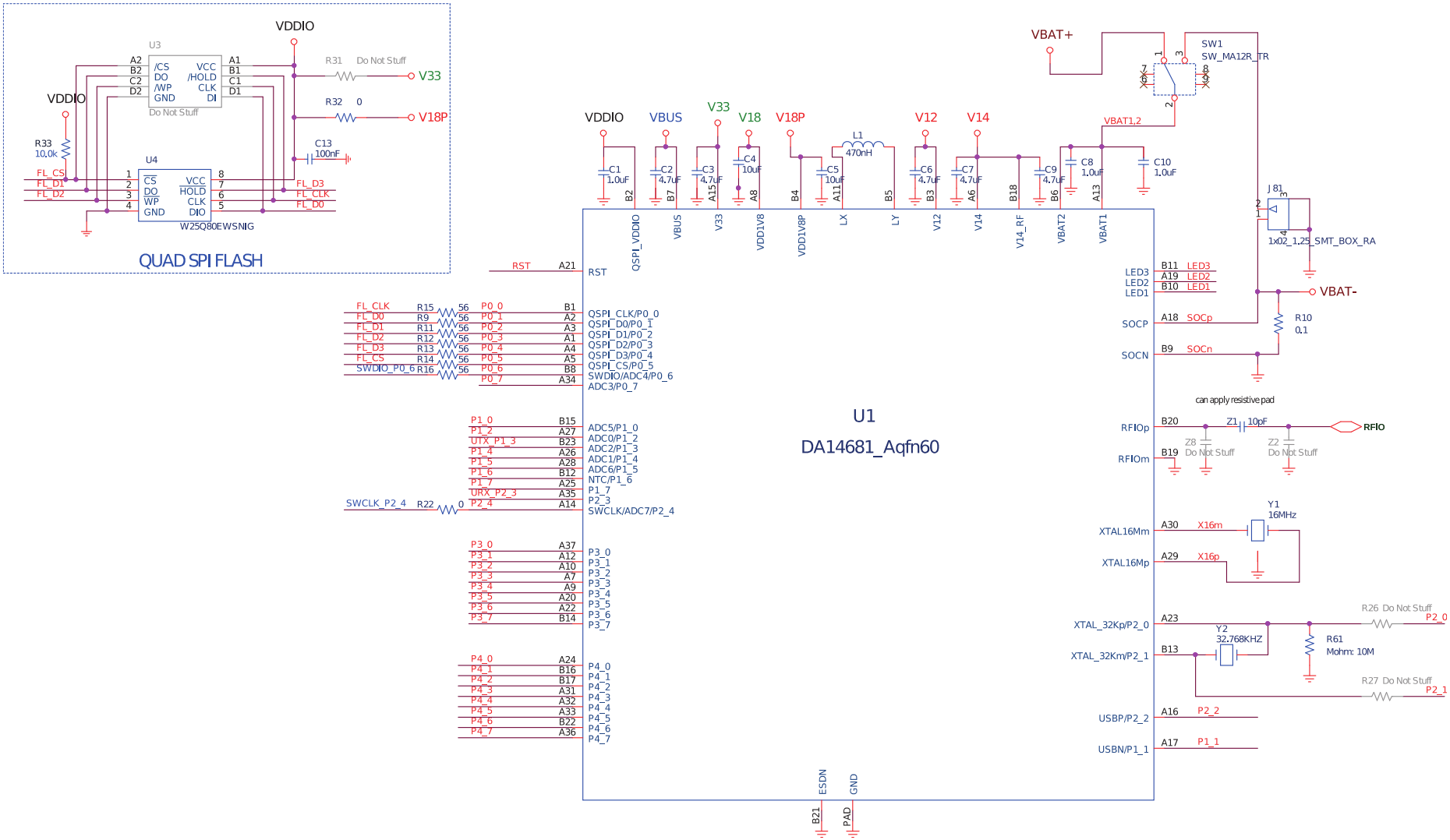


Figure 7: DA14681 Basic System with External QSPI Flash Memory - overview

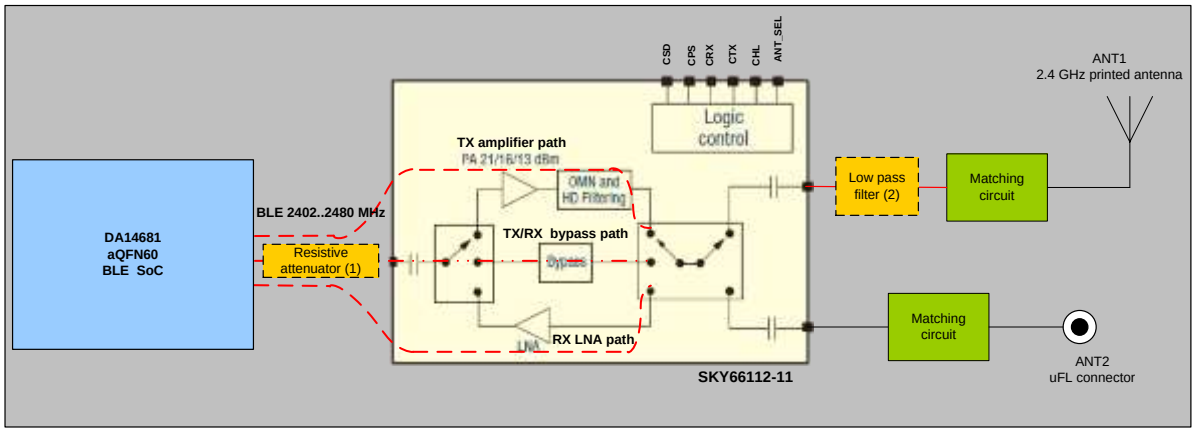
7 RF Front End

This part of the design implements the amplification of the RF transmitted signal while the transmitted harmonics as well as the TX spurious emissions remain within the FCC/ETSI specification. The RF Front End Module (FEM) used is SKY66112-11 of Skyworks (Ref. [5]).

The operation of RF front end is controlled by the DA14680/681 SoC using control signals. During the operation of the FEM there are three available RF paths:

- TX path through the amplifier
- RX path through the LNA of the PA
- TX/RX bypass path, where both PA/LNA are bypassed during transmission and reception.

The amplifier path is enabled during transmission. The RF signal passes through the PA and the RF matching network and is transmitted through one of the two available antenna ports. A resistive attenuator and a low pass filter can also be included in the amplifier path if needed. In the bypass path, the RF signal received at the antenna is driven directly to the BLE transceiver. In the RX LNA path the received signal passes through SKY66112-11 LNA, which has a receive gain of 11 dB.



Legend:

(1) Resistive attenuator application is possible.

(2) Low pass filter application is possible.

Figure 8: RF Front End Signal Paths

The amplifier has three different voltage rails (VCC1, VCC2 and VDD). The TX power output is tuned by modifying the VCC2 supply rail voltage as well as the power level at its input. The basic power levels for the PA are:

- TX P_{OUT} = +21 dBm @ VCC2 = 3.0 V, P_{IN} = -1 dBm
- TX P_{OUT} = +16 dBm @ VCC2 = 1.8 V, P_{IN} = -3 dBm
- TX P_{OUT} = +13 dBm @ VCC2 = 1.2 V, P_{IN} = -3 dBm

7.1.1 Control Signals

The SKY66112-11 has a number of digital control signals that need to be set/reset by the DA14680/681. They are currently being controlled by Dynamic Control Function (DCF) signals of the DA14680/681 RF control unit. The DCF signals are normal GPIOs controlled by timers within the radio. Their functionality is explained in Table 4, while their timing is shown in Figure 9.

The digital control signals are compatible with 1.6 V to 3.6 V CMOS levels and are supplied from the VDD voltage rail.

Table 4: SKY66112-11 Control Signal Description

Control Signal	Function	Mode of Operation
CSD	FEM Enable signal	0: all off (sleep mode) 1: FEM enabled
CRX	RX enable	0: RX off 1: RX on with LNA
CPS	Bypass mode	0: Bypass disabled 1: Bypass mode for TX or RX
CTX	TX Enable	0: TX off 1: TX on (Low or High power)
CHL	TX Power level	0: TX Low power level 1: TX High power level
ANT_SEL	Antenna select signal	0: ANT1 1: ANT2

Table 5: Truth Table for SKY66112-11

Mode	Description	CSD	CPS	CRX	CTX	CHL
0	All off (sleep mode) (Note 1)	0	X	X	X	X
1	Receive LNA mode	1	0	1	0	X
2	Transmit high power mode	1	0	X	1	1
3	Transmit low power mode	1	0	X	1	0
4	Receive Bypass mode	1	1	1	0	X
5	Transmit Bypass mode	1	1	X	1	X
6	All off (sleep mode)	1	X	0	0	X

Note 1 All controls must be at logic 0 to achieve the specified sleep current.

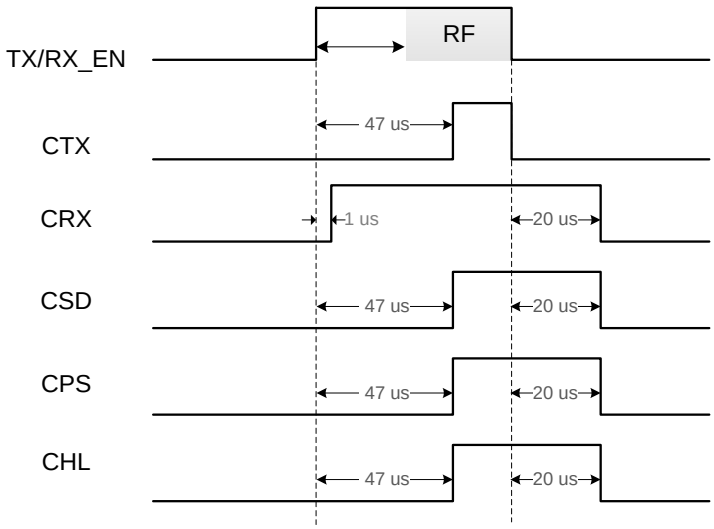


Figure 9: SKY66112-11 Control Signal Timing

The control signal timing aims to keep the signals at logic 0 as long as possible to achieve better power results. This can be achieved by assigning the control signals to DCF timers (see Table 7)

Decoding of the signals results in the following signal description:

- CTX: Enable any TX related operation
- CRX: Enable any RX related operation
- CHL: Define TX High (1) or Low (0) power mode
- CPS: Enable bypass TX/RX mode
- CSD: Enable FEM

7.1.2 GPIO Setup

The RF Control Unit (RFCU) of DA14680/681 provides the capability of controlling five signals which can be used for controlling the SKY66112-11. The DCFs can be output on any GPIO by using PID numbers 55 to 59. The five DCF signals can be extracted from the RFCU to any pin by programming the PID values in the Pxx_MODE_REG registers, as follows:

Table 6: DCF Signal Configuration

Function	PORT0_DCF	PORT1_DCF	PORT2_DCF	PORT3_DCF	PORT4_DCF
PID	55	56	57	58	59

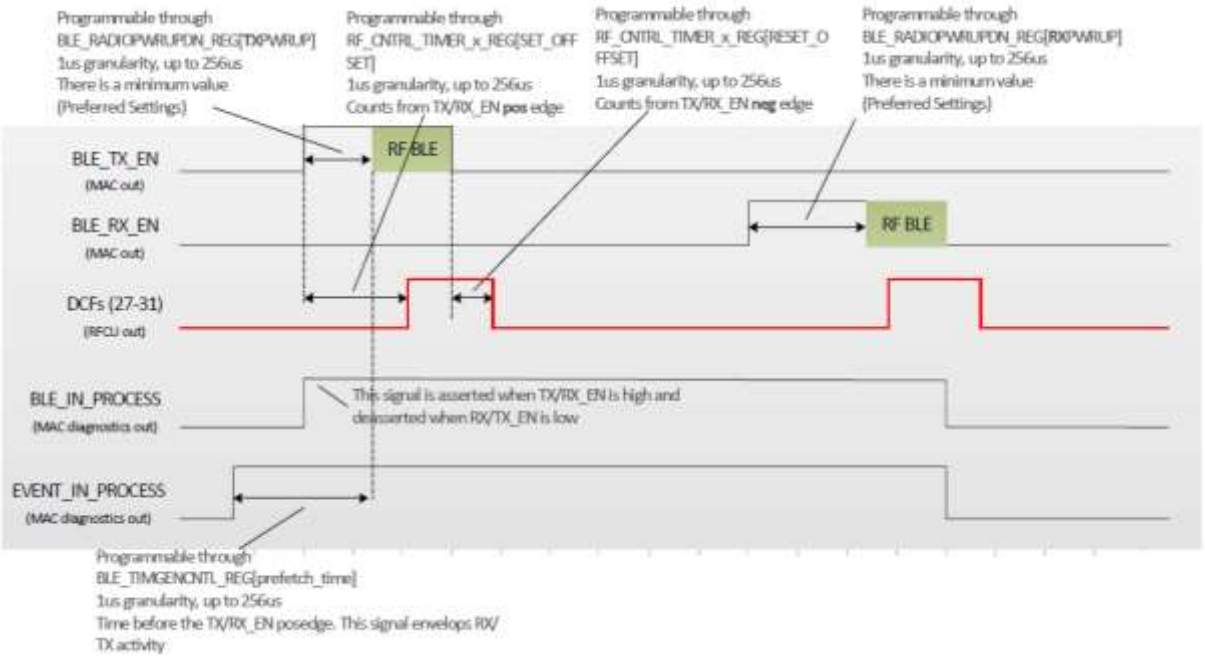


Figure 10: DCF Signal Programming

Table 7: SKY66112-11 Control Signal and DCF Timer Configuration

Mode	DA1468x GPIO	SKY66112-11	Comments
FEM enable	P4_3	CSD	GPIO or DCF timer 29 (PORT2_DCF)
TX enable	P4_5	CTX	DCF timer 27 (PORT0_DCF)
PA High Gain	P4_4	CHL	GPIO or DCF timer 31 (PORT4_DCF)
RX enable	P4_2	CRX	DCF timer 28 (PORT1_DCF)
PA or LNA Bypass	P4_6	CPS	GPIO or DCF timer 30 (PORT3_DCF) This signal can be fixed at logic 0 or 1 through

Mode	DA1468x GPIO	SKY66112-11	Comments
			a pull-down or pull-up resistor.
ANT_SEL	P4_0	ANT_SEL	GPIO This signal can be fixed at logic 0 through a pull-down resistor.

7.1.3 Power Amplifier

The SKY66112-11 is a fully integrated RF Front End Module (FEM) designed for Smart Energy applications. The device provides PA, LNA, an integrated inter-stage matching and harmonic filter, and digital controls compatible with 1.6 V to 3.6 V CMOS levels.

The RF blocks operate over a wide supply voltage range from 1.2 V to 3.6 V that allows the SKY66112-11 to be used in battery powered applications over a wide spectrum of the battery discharge curve. The basic characteristics for the SKY66112-11 are:

- Three voltage rails (VCC1, VCC2 and VDD)
- TX power output tuning thru power rail voltage modification
  - TX P_{OUT} = +21 dBm @ VCC2 = 3.0 V / 115 mA, Pin = -1 dBm
  - TX P_{OUT} = +16 dBm @ VCC2 = 1.8 V / 60 mA, Pin = -3 dBm
  - TX P_{OUT} = +13 dBm @ VCC2 = 1.2 V / 45 mA, Pin = -3 dBm
- LNA with gain 11 dB
- Receive Noise Figure = 2 dB
- Bypass mode of operation (-2 dB)
- Two Antennas Ports

An overview of the SKY66112-11 Front End Module is shown in Figure 11.

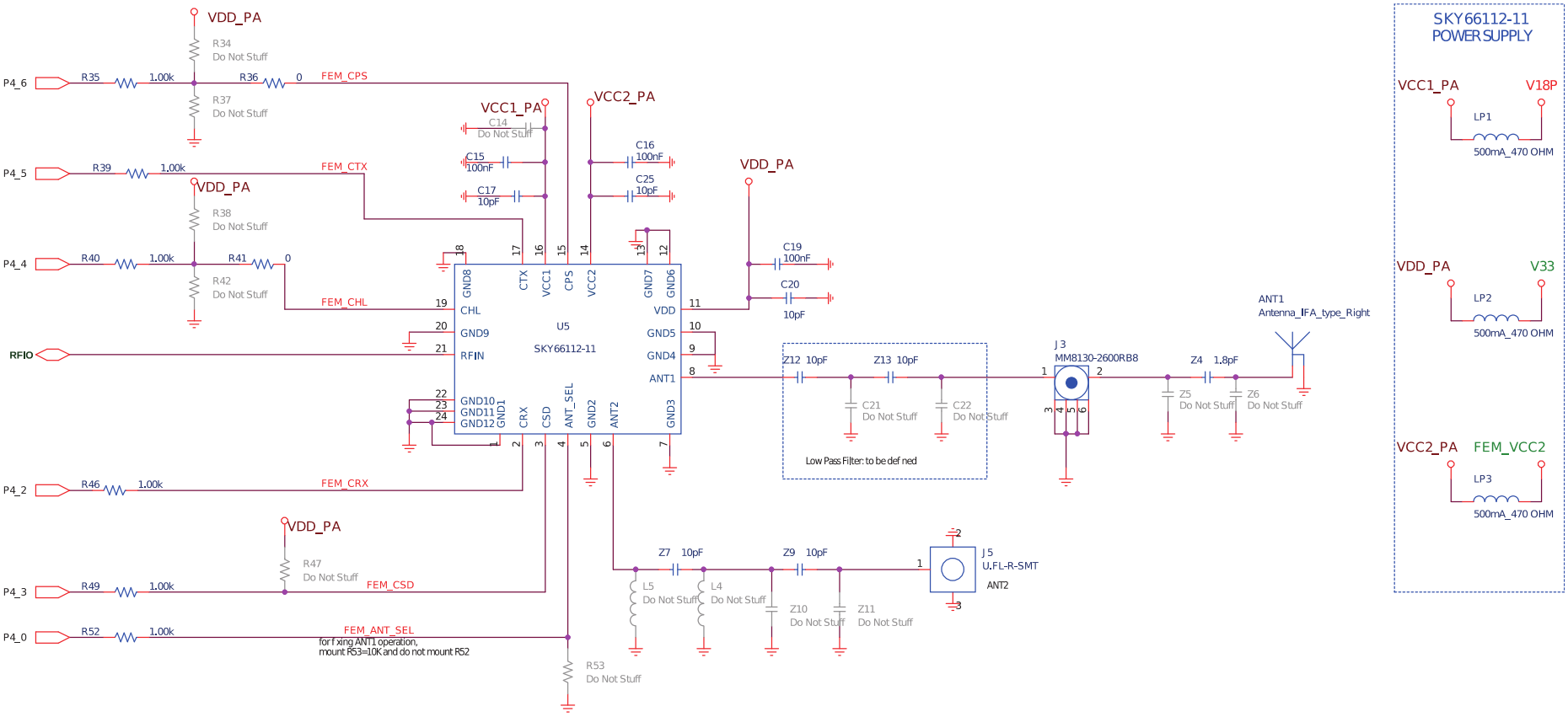


Figure 11: SKY66112-11 Front End Module - overview

7.1.3.1 Power Modes

The SKY66112-11 FEM supports three different power modes:

- **HPM1:** High Power Mode 1, where VCC2 = 3.0 V, VCC1 = 1.8 V and VDD = 3.0 V @ P_{OUT} = +21 dBm, P_{IN} = -1 dBm.
- **LPM1:** Low Power Mode 1, where VCC2 = 1.8 V, VCC1 = 1.8 V and VDD = 3.0 V @ P_{OUT} = +16 dBm, P_{IN} = -3 dBm.
- **LPM2:** Low Power Mode 2, where VCC2 = 1.2 V, VCC1 = 1.8 V and VDD = 3.0 V @ P_{OUT} = +13 dBm, P_{IN} = -3 dBm (see Figure 12).

In the current design due to FCC compliance[5] reasons, Low Power Mode 2 is used. VCC2 voltage level is connected to V18 and it is configured to 1200 mV using a series resistor R73=16.5 Ω. The DA14680/681 TX output power is set to -2 dBm and it is programmed using RF_TX_PWR_REG (0x500020C0).

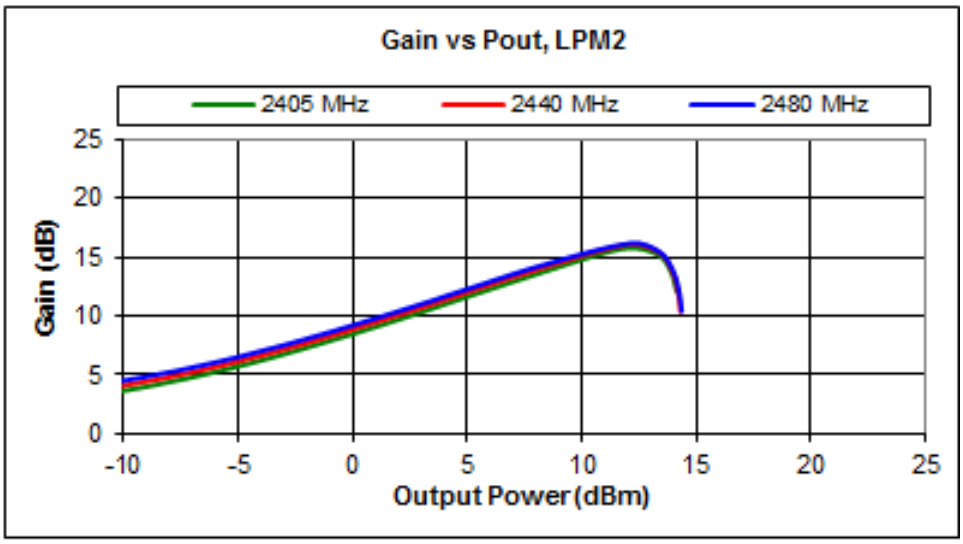


Figure 12: SKY66112-11 Gain vs. P_{OUT}, LPM2

The use of a hardware resistive attenuator between DA14680/681 and SKY66112-11 may be considered to provide an extra low RF input power range to SKY66112-11 when a lower TX output power is needed (see Figure 8). Of course, addition of the resistive attenuator leads to a current consumption increment for the same RF power output.

Given the lowest power level that DA14680/681 can provide at the input of the PA which is -4 dBm and that the PA gain in bypass mode is -2 dB, the Range Extender can deliver a minimum output power of -6 dBm and a maximum of +13.5 dBm.

[5] Emission limitations in restricted area of 2483.5 MHz to 2500 MHz.

7.1.3.2 Power Supply

The SKY66112-11 requires three different supply voltages:

- **VCC1:** Supplies the first stage of the PA as well as the LNA.
- **VCC2:** Supplies the second stage of the PA.
- **VDD:** Supplies the logic (switches, bias enable, etc.).

Table 8: SKY66112-11 TX Output Characteristics

Voltage Rail	FEM Pin	FEM Specification (V)			Comments
		Min	Typ	Max	
VCC1	16	1.7	1.8	3.3	VCC1 = 1.8 V, VCC2 = 3.0 V, ICC = 115 mA, P_{OUT} = +21 dBm, P_{IN} = -1 dBm
VCC2	14	0.6	3.0	3.3	VCC1 = 1.8 V, VCC2 = 3.0 V , ICC = 90 mA, P_{OUT} = +20 dBm, P_{IN} = -2 dBm
VDD	11	1.8	3.0	3.3	VCC1 = 1.8 V, VCC2 = 1.8 V , ICC = 60 mA, P_{OUT} = +16 dBm, P_{IN} = -3 dBm VCC1 = 1.8 V, VCC2 = 1.2 V, ICC = 45 mA, P_{OUT} = +13 dBm, P_{IN} = -3 dBm

VDD is supplied by V33 of the DA14680/681.

VCC1 is connected to the V18P voltage rail of DA14680/681. Current consumption and voltage regulation requirements must be taken under consideration. VCC1 supplies the LNA or the first stage of the PA with a power consumption of 6 mA or 25 mA (max.) respectively. The V18P output must present very low ripple and low noise. The V18P power rail has a driving current capability of 75 mA.

The VCC2 voltage level is critical, as it affects the RF PA output level. VCC2 supplies the second stage of the PA and draws most of the TX current. VCC2 is connected to the V18 power rail[6]. The VCC2 voltage can be changed using a series resistor R73. The V18 power rail has a current driving capability of 75 mA.

7.1.4 Transmit (TX) Path

The RF PA TX Power output level is defined primarily by the VCC2 voltage level and secondly by the control signal settings.

The CPS signal is used to enable the bypass operating mode of the FEM. Enabling CPS provides a direct path between antenna and DA14680/681 chip.

The CHL functionality is intended to be used to increase efficiency at the lower output power levels by reducing the PA bias. It is not intended for power control. However at constant VCC2, toggling CHL will increase/decrease P_{OUT} by 0.5 dB to 0.75 dB.

The TX power output is determined based on:

- VCC2 level which is connected to V18 via a series resistor R73.
- DA14680/681 TX power set using RF_TX_PWR_REG (0x500020C0). This register can be programmed from 0 to 4 (0 dBm to -4 dBm).
- Resistive attenuator populated before or after the PA (optional).

[6] This configuration differs from the DA1468x development kit. GPIOs configured to operate at 1.8 V are supplied from the V18P rail while the ones configured to operate at 3.3 V are supplied from the V33 rail. This means that V18P could only be used for VCC2 if there are no GPIOs configured to operate at 1.8 V. Therefore, instead of V18P the V18 power rail is used to supply VCC2.

Table 9: SKY66112-11 TX RF Power Output (Note 1)

VCC2 (V)	Input Power (dBm)	Control Signal	PA Mode of Operation	Output Power at ANT1 or ANT2 (dBm)	PA Current Consumption (mA)
1.2	0	CPS = 1	Bypass	-2	0.025
1.8	0			-2	0.025
3.0	0			-2	0.025
1.2	-3	CPS = 0 CHL = 0	Low Power	+13	45
1.8	-3			+16	60
3.0	-2 -1			+20 +21	90 115
1.2	-3	CPS = 0 CHL = 1	High Power	+13.5	<TBD>
1.8	-3			+16.5	<TBD>
3.0	-2 -1			+20.5 +21.5	<TBD>

Note 1 Datasheet: SKY66112-11_203225G, VCC1 = 1.8 V, VDD = 3 V, T = 25 °C, 2440 MHz.

The default configuration is shown in Table 10.

Table 10: Default Configuration

VCC2 (V)	Input Power (dBm)	Control Signal	PA Mode of Operation	Output power at ANT1 (dBm)	PA Current Consumption typical (mA)
1.2	-2	CPS = 0 CHL = 0	Low Power	+13.5	50

7.1.5 Receive (RX) Path

There are two receive modes:

- **Receive LNA:** Additional gain is provided by the LNA: gain = 11 dB, NF = 2. The LNA improves the sensitivity by approximately 5 dB.
- **Receive Bypass:** The LNA is removed from the RX path.

Table 11: LNA Modes (Note 1)

Control Signal	LNA Mode of Operation	Gain (dB)	Noise Figure (dB)	LNA Current Consumption (mA)
CRX = 1 CPS = 0	Receive LNA	11	2	6
CRX = 1 CPS = 1	Receive Bypass	-2		0.025

Note 1 Datasheet: SKY66112-11_203225G, VCC1 = 1.8 V, VCC2 = 3.0 V, VDD = 3.0 V, T = 25 °C.

7.1.6 Filtering (Optional)

No external filtering is needed. However, there are positions to add filter components in case it is needed.

7.1.7 Antenna

DA14680/681 provides a single ended RFIO port, matched to 50 Ω. The RF port consists of the RFIOp and RFIOm pins, where RFIOm is connected to ground. A copper trace with impedance of 50 Ω interconnects the RF port and the RFIN of SKY66112-11.

SKY66112-11 FEM provides two antenna outputs controlled by the ANT_SEL pin (GPIO P4_0) or it can be hardware configured using a pull-down resistor (R53).

Table 12: SKY66112-11 Antenna Select Logic

Antenna Port	SKY66112-11 Pin	Antenna Select Signal	Usage
ANT1	8	ANT_SEL = 0	Connected to printed antenna
ANT2	6	ANT_SEL = 1	Connected to uFl connector

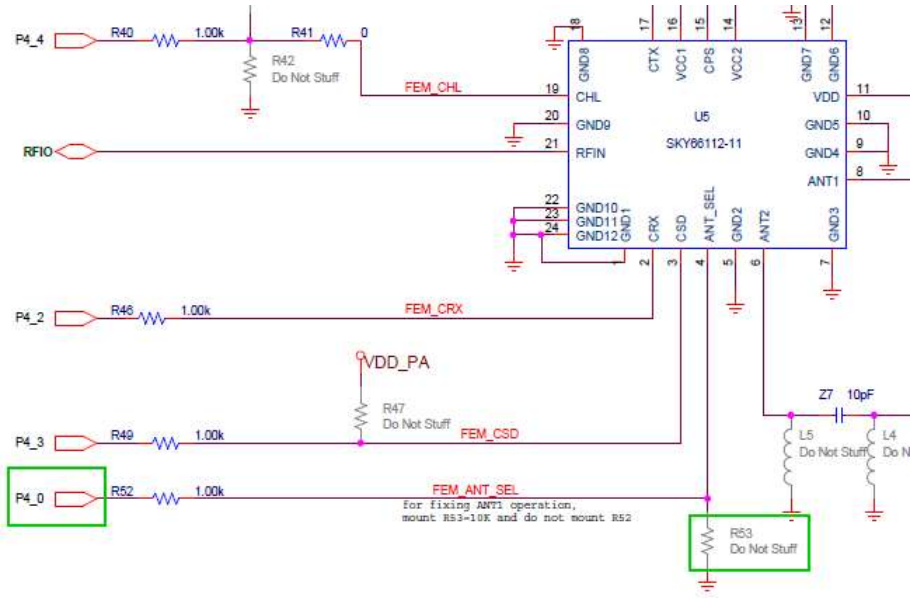


Figure 13: Antenna Selection Using P4_0 or a R53 Pull-Down Resistor

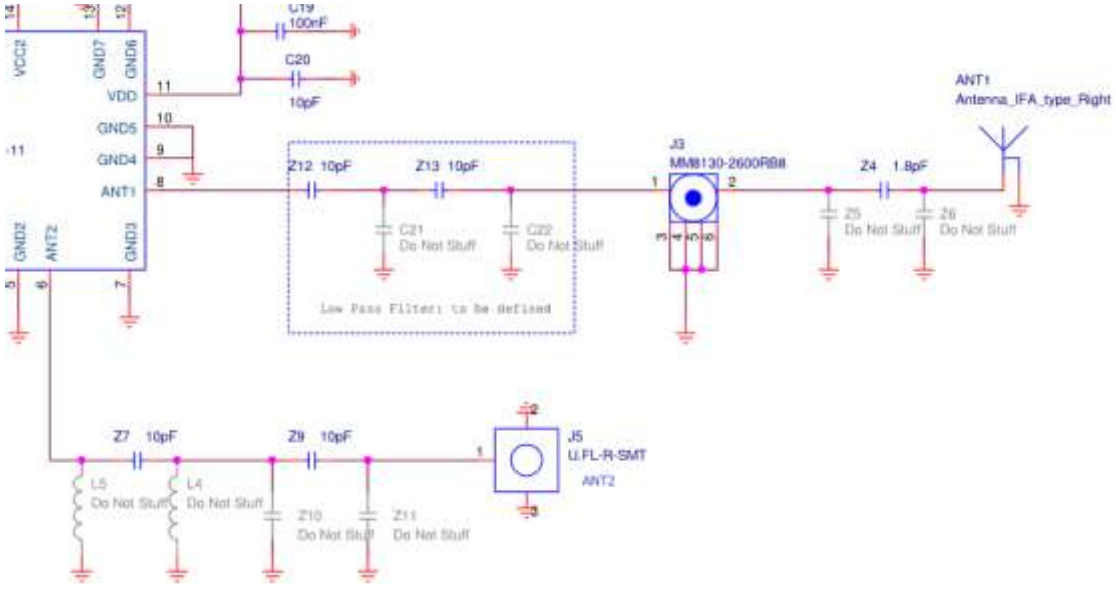


Figure 14: SKY66112-11 Antenna Ports

At the ANT1 port a printed Inverted-F Antenna (IFA) with 0 dBi gain is used. At the ANT2 port a uFL connector (J5) is used for connecting external antennas. Pi-networks Z4, Z5, Z6 and Z9, Z10, Z11 can be used for matching purposes on both antenna ports.

For the ANT1 port a series capacitor of Z4 = 1.8 pF is used for optimum power transfer.

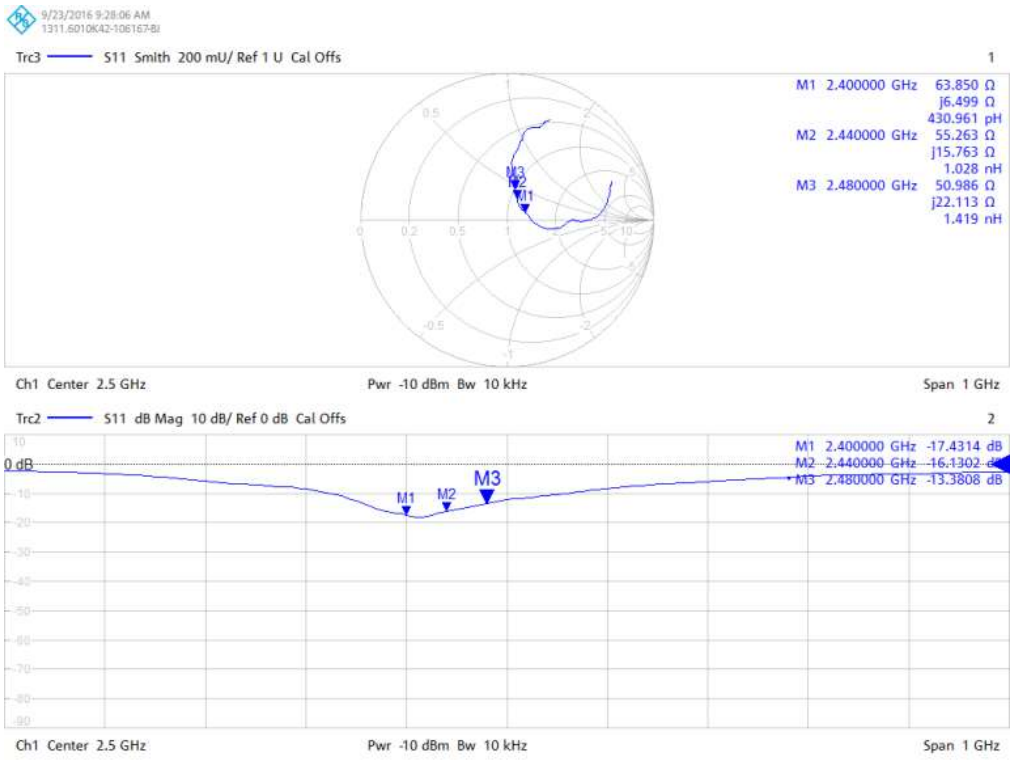


Figure 15: ANT1, Printed IFA Antenna and Matching Network (Z4 = 1.8 pF)

The reference design provides an SMD RF switch (J3) in series to the printed IFA antenna. The SMD RF switch is used for conducted RF evaluation/testing. The RF switch type is MM8130-2600 supplied by Murata. Verification of the circuit performance is accomplished by inserting an external plug in the board mounted receptacle. This action re-directs the circuit from normal condition to the plug side. Removing the plug restores circuit back to its normal condition.

7.1.8 Resistive Attenuator (Optional)

Between DA14680/681 and SKY66112-11 a resistive attenuator circuit can be added if needed. Capacitors Z1, Z2 and Z8 must then be replaced by suitable resistors to achieve the desired attenuation, while matching the 50 Ω impedance.

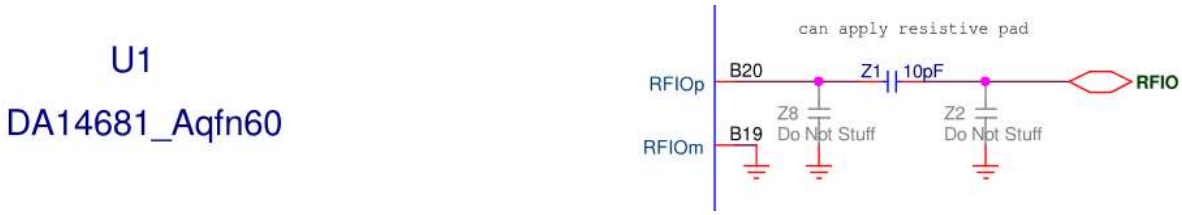


Figure 16: Resistive Attenuator Between DA14681 and SKY66112-11

8 Crystals

DA14680/681 SoC has two Digitally Controlled Crystal Oscillators (DXCO) one at 16 MHz (XTAL16M) and a second at 32.768 kHz (XTAL32K). The 32.738 kHz oscillator is the Low Power (LP) clock, which is used for the HW FSM during power-up/wake-up, for the TIMER1 upon which is based the system timer and it is used in Extended/Deep Sleep low power modes of the DA1468x. The 32.768 kHz oscillator has no trimming capabilities. The 16 MHz oscillator can be trimmed.

The crystals used are specified in Table 13 and Table 14:

Table 13: Y1 16 MHz Crystal Characteristics

Reference Designator	Value
Part Number	7M-16.000MEEQ-T
Frequency	16 MHz
Accuracy	±10 ppm
Load Capacitance (C_L)	10 pF
Shunt Capacitance (C_0)	3 pF
Equivalent Series Resistance (ESR)	100 Ω
Drive Level (P_D)	50 µW

Table 14: Y2 32 kHz Crystal Characteristics

Reference Designator	Value
Part Number	ABS07-32.768KHZ-7-T
Frequency	32.768 kHz
Accuracy	±20 ppm
Load Capacitance (C_L)	7 pF
Shunt Capacitance (C_0)	0.9 pF to 1.2 pF
Equivalent Series Resistance (ESR)	70 kΩ
Drive Level (P_D)	0.5 µW

9 QSPI Flash Memory

An 8 Mbit QSPI Data Flash memory (W25Q80EW) is provided to store user code. Its connection to the DA14681 is fixed, as it interfaces directly with the chip's Quad SPI Controller. The memory is powered by the V18P rail. See section 7.1.3.2 for details on the power supply scheme.

Refer to the DA14681 datasheet (Ref. [3]) for more details on connecting an external Flash memory.

An external QSPI Data Flash memory is not required when the DA14680 SOC is used. Please note that the current implementation is done with DA14681.

10 TX Output Power Control Circuit

For DA14680/681 the FEM_VCC2 is tied to the V18 power rail via resistor R73. The TX output power of the FEM is controlled by series resistor R73 = 16.5 Ω, as well as the power level at the input. The default output of V18 is 1.8 V, using this series resistor the voltage for FEM_VCC2 of the SKY66112-11 is regulated to 1.2 V. For lower power output this series resistor can be further increased.

11 Reference Design Pin Assignment

The pin assignment for the Range Extender is shown in Table 15.

Table 15: DA14680/681 aQFN60 Pin Assignment

GPIO Name	aQFN60 Function	Range Extender Function	Comments
P0_0	FL_CLK	FL_CLK	Range Extender QSPI Flash
P0_1	FL_D0	FL_D0	Range Extender QSPI Flash
P0_2	FL_D1	FL_D1	Range Extender QSPI Flash
P0_3	FL_D2	FL_D2	Range Extender QSPI Flash
P0_4	FL_D3	FL_D3	Range Extender QSPI Flash
P0_5	FL_CS	FL_CS	Range Extender QSPI Flash
P0_6	SWDIO	SWDIO	
P0_7	SOFT_TRIG	SOFT_TRIG	
P1_0	ML8511_OUT (analog in)	Not assigned	I/O is not usable during RF transmission (see AN-B-061, Ref. [6])
P1_1	USBN	Not assigned	
P1_2	I2C_SDA	I2C_SDA	
P1_3	UTX	UTX	
P1_4	PDM_DATA/NTC bias	Not assigned	
P1_5	URTS/LED	URTS/LED	I/O is not usable during RF transmission (see AN-B-061, Ref. [6])
P1_6	UCTS/button	UCTS/button	
P1_7	PDM_CLK	Not assigned	
P2_0	XTAL32p	XTAL32p	
P2_1	XTAL32m	XTAL32m	
P2_2	USBP	Not assigned	
P2_3	URX	URX	
P2_4	SWCLK / ML8511_EN	SWCLK	
P3_0	GPIO	Not assigned	
P3_1	GPIO	Not assigned	
P3_2	GPIO	Not assigned	
P3_3	GPIO	Not assigned	
P3_4	GPIO	Not assigned	
P3_5	I2C_SCL	Not assigned	
P3_6	GPIO	Not assigned	
P3_7	GPIO	Not assigned	
P4_0	GPIO	FEM_ANT_SEL	
P4_1	GPIO	FEM_PWR_CTRL	
P4_2	GPIO	FEM_CRX	
P4_3	GPIO	FEM_CSD	

GPIO Name	aQFN60 Function	Range Extender Function	Comments
P4_4	GPIO	FEM_CHL	
P4_5	GPIO	FEM_CTX	
P4_6	GPIO	FEM_CPS	
P4_7	GPIO	Not assigned	
-	RST	RST	
-	XTAL16Mp	XTAL16Mp	
-	XTAL16Mm	XTAL16Mm	

12 Development Mode - Peripheral Pin Mapping

The pins used for development and testing are described in Table 16.

Table 16: DA1468x Development/Test Mode Pin Mapping

Pin No.	Assigned Function	Development/Test Function	Pin No.	Assigned Function	Development/Test Function
B1	P0_0/ QSPI_CLK	QSPI_CLK	A16	P2_2/USBP	External use
A2	P0_1/ QSPI_D0	QSPI_D0	A35	P2_3	UART RX
A3	P0_2/ QSPI_D1	QSPI_D1	A14	P2_4/SWCLK/ADC7	SW_CLK Input JTAG clock signal
A1	P0_3/ QSPI_D1	QSPI_D1	A37	P3_0	External use
A4	P0_4/ QSPI_D1	QSPI_D1	A12	P3_1	External use
A5	P0_5/ QSPI_D1	QSPI_D1	A10	P3_2	External use
B8	P0_6/ SWDIO/ PWM5/ADC4	SWDIO JTAG Data Input/output. Bidirectional data and control communication.	A7	P3_3	External use
A34	P0_7/ ADC3	External use	A9	P3_4	External use
B15	P1_0/ADC5	External use	A20	P3_5	External use
A17	P1_1/USBN	External use	A22	P3_6	External use
A27	P1_2/ADC0	External use	B14	P3_7	External use
B23	P1_3/ADC2	UART TX	A24	P4_0	FEM_ANT_SEL
A26	P1_4/ADC1	External use	B16	P4_1	FEM_PRW_CTRL
A28	PA1_5/ADC6	External use	B17	P4_2	FEM_CRX
B12	P1_6/NTC	External use	A31	P4_3	FEM_CSD
A25	P1_7	External use	A32	P4_4	FEM_CHL
A23	P2_0/XTAL32Kp	Input of the 32.768 kHz XTAL oscillator	A33	P4_5	FEM_CTX
B13	P2_1/XTAL32Km	Output of the 32.768 kHz XTAL oscillator	B22	P4_6	FEM_CPS
A29	XTAL16Mp	Input of the 16 MHz XTAL oscillator	A36	P4_7	External use
A30	XTAL16Mm	Output of the 16 MHz XTAL oscillator	A21	RST	Reset

13 PCB Assembly

A 4-layer FR4 PCB with 1.49 mm standard thickness is used. The PCB size is 43 mm x 43 mm. All available GPIOs are accessible via the two connectors placed on the bottom of the PCB. Schematics and Bill of Materials are presented in the following sections.

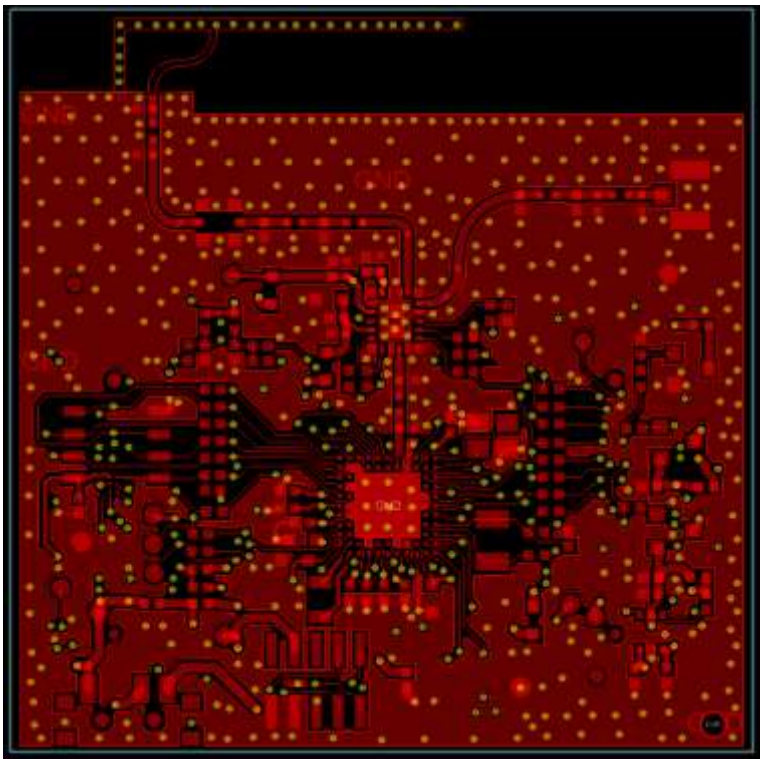


Figure 17: Top View of PCBA

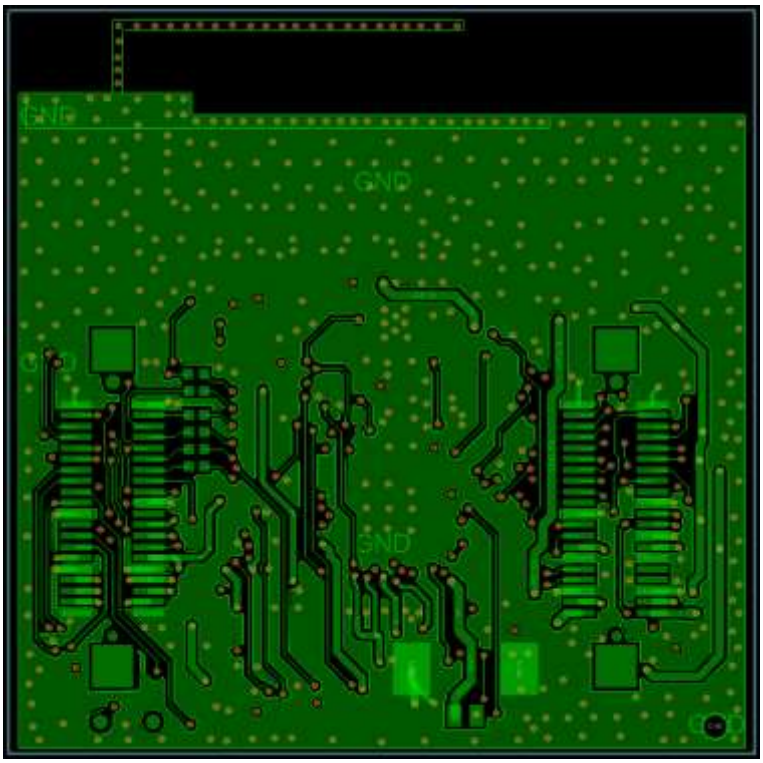
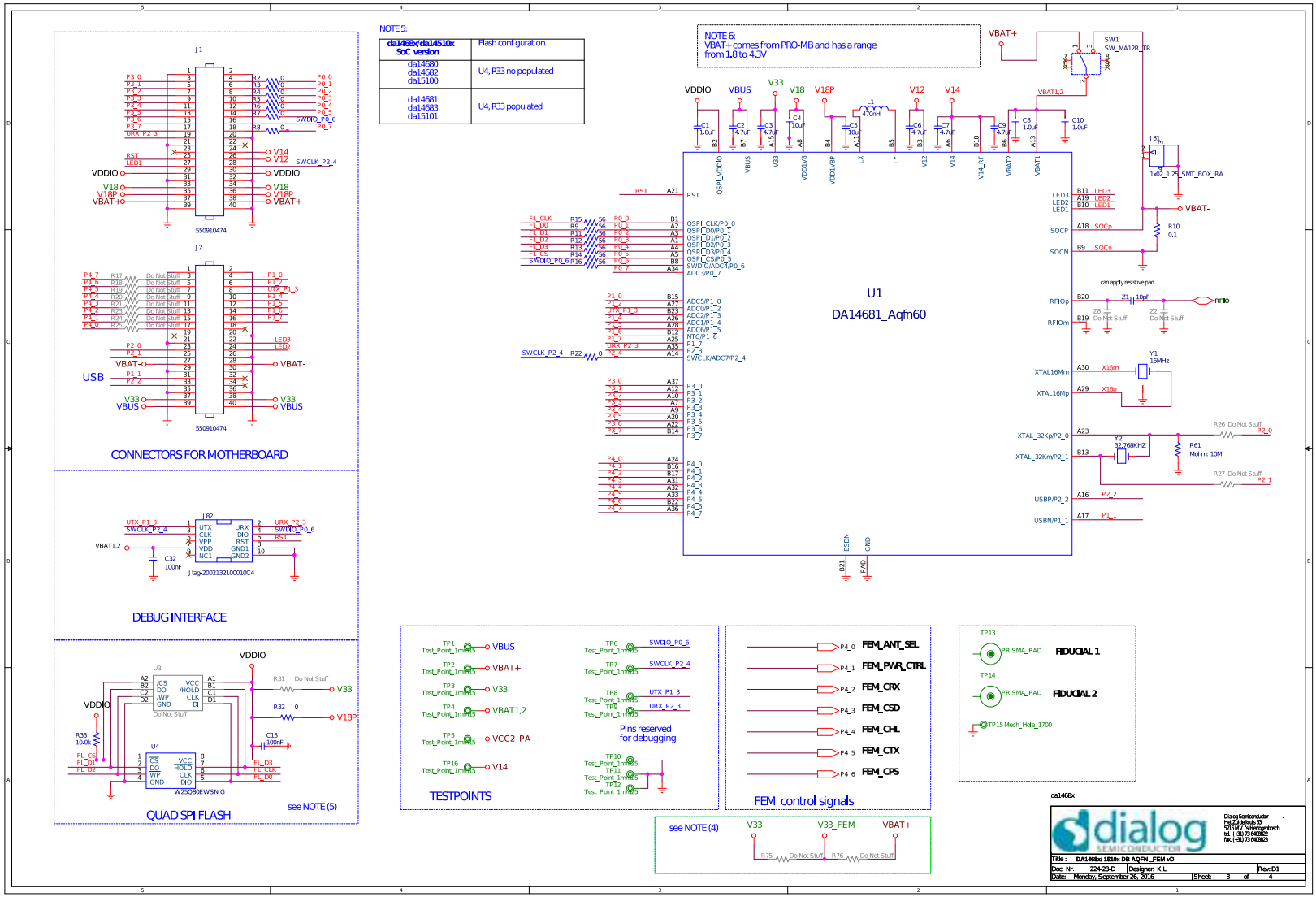
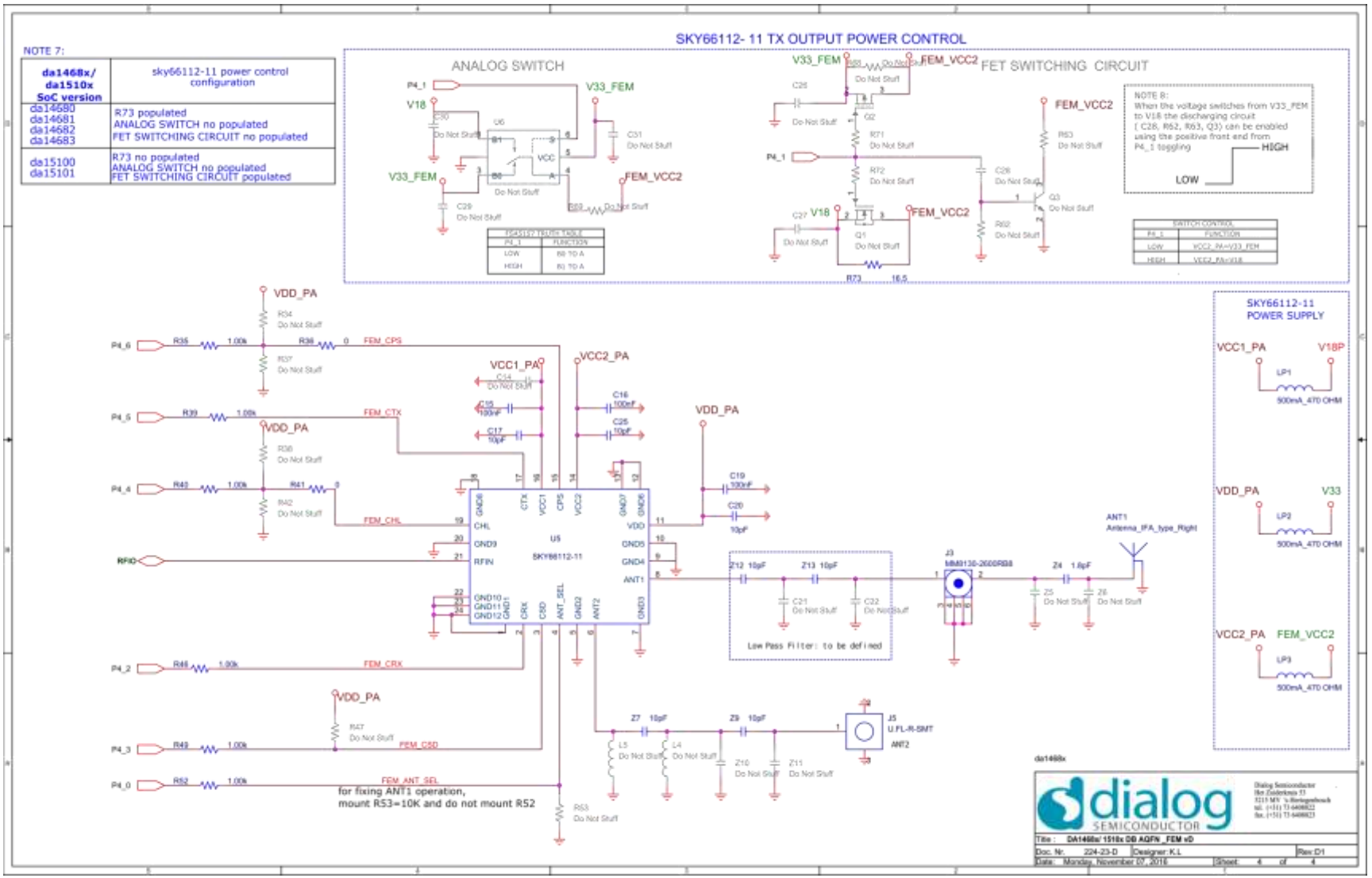


Figure 18: Bottom View of PCBA

13.1 DA14681 Range Extender Schematic



13.2 SKY66112-11 Front End Module Schematic



13.3 Bill of Materials

Table 17: BOM of DA14681 Range Extender

Ref.	Value	Description	Manufacturer	Manufacturer Part Number	Footprint
U1	DA14681_ Aqfn60	Low Power Bluetooth Smart 4.2 SoC	Dialog Semiconductor	DA14681_aQFN60	aqfn60mp
U4	W25Q80EW SNIG	IC FLASH 8MBIT 104MHz 8SOIC 150 mil	Winbond	W25Q80EWSNIG	SOIC127P600X175-8N
U5	SKY66112-11	IC 2.4 GHz ZigBee®/ Smart Energy Front-End Module	Skyworks Solutions, Inc.	SKY66112-11	RF_SKY66112
R2 R3 R4 R5 R6 R7 R8 R22 R32 R36 R41	0	RES 0.0 OHM 1/16W 5% 0402 SMD	Vishay/Dale	CRCW04020000Z0ED	R1005
R9 R11 R12 R13 R14 R15 R16	56	RES 56 OHM 1/16W 0402 SMD	Vishay/Dale	CRCW040256R0JNED	R1005
R10	0.1 Ω	RES 0.1 OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3RSFR10V	R1608
R33	10.0 kΩ	RES 10.0K OHM 1/16W 1% 0402 SMD	Vishay/Dale	CRCW040210K0FKED	R1005
R35 R39 R40 R46 R49 R52	1.00 kΩ	RES 1.0K OHM 1/16W 5% 0402 SMD	Vishay/Dale	CRCW04021K00JNED	R1005
R61	10 MΩ	RES SMD 10M OHM 1% 1/16W 0402	Vishay Beyschlag	CRCW040210M0FKED	R1005
R73	16.5 Ω	RES SMD 16.5 OHM 1% 1/16W 0402	Vishay/Dale	CRCW040216R5FKED	R1005
Y1	16 MHz	CRYSTAL 16.000MHZ 10PF SMT	TXC	7M-16.000MEEQ-T	xtal4p25x20
Y2	32.768 kHz	CRYSTAL 32.768KHZ 7PF SMD	Abracon Corporation	ABS07-32.768KHZ-7-T	xtal_abs07
C1 C8 C10	1.0 µF	CAP CER 1.0UF 6.3V 10% X5R 0402	Murata	GRM155R60J105KE19D	C1005
C2 C3 C6 C7	4.7 µF	CAP CER 4.7uF 6.3volts X5R 20% 0402	Murata	GRM155R60J475ME47D	C1005

Ref.	Value	Description	Manufacturer	Manufacturer Part Number	Footprint
C9					
C4 C5	10 µF	CAP CERAMIC 10uF 6.3V X5R 0603 SMD	Murata	GRM188R60J106ME47D	C1608
C13 C15 C16 C19 C32	100 nF	CAP CER .1UF 16V X7R 0402	Murata	GRM155R71C104KA88D	C1005
C17 C20 C25 Z1 Z7 Z9 Z12 Z13	10 pF	CAP CER 10PF 50V 2% NP0 0402	Murata	GRM1555C1H100GA01D	Z1005
Z4	1.8 pF	Cap Cer. 1.8pF 50V C0G, NP0 0402	Murata	GRM1555C1H1R8CA01D	C1005
L1	470 nH	FIXED IND 470NH 1.2A, DCr: 0.06 OHM 20% (0805)	Taiyo Yuden	CKP2012NR47M-T	L2012
LP1 LP2 LP3	500 mA_ 470 Ω	EMI FB Universal (Power & Signal Lines) 470 OHM±25% 0.5A DCr:0.21 OHM (0603)	Murata Electronics	BLM18EG471SN1D	L1608
J1 J2	550910474	B2B & Mezzanine Connectors .635 HEADER SURFACE MNT 40 CKT	Molex	550910474	MOLEX_ 550910474
SW1	SW_MA12R _TR	SWITCH SLIDE SPDT 300MA 4V	Apem	MA12R/TR	SW_ MA12R_TR
J5	U.FL-R-SMT	CONN RECPT ULTRA-MINI COAX SMD	Hirose Electric Co Ltd	U.FL-R-SMT	UFL_R_ SMT
J3	MM8130- 2600RB8	RF CONN SWF JACK STR 50 OHM SMD Push-Pull	Murata	MM8130-2600	RF_CON_ MM8130- 2600
J81	1x02_1.25_ SMT_BOX_ RA	Headers & Wire Housings Right-Angle HDR SMT 2P 1.25 mm	Molex	53261-0271	Molex_ 532610271
J82	Jtag- 2002132100 010C4	MECH Connector Jtag_2x5 SMD 1.27mm pitch	FCI	20021321-00010C4LF	Jtag- 200213210 0010C4
ANT 1	Antenna_IFA _type_Right	MECH Antenna Printed F type used on RCU boards Right Orientation	NA_ Mechanical Part	NA_Mechanical Part	da14580_ ant_ifa_ right

14 Application Software Guide: ble_external_host

The following instructions are based on DA1468x SDK 1.0.12 and SmartSnippets™ Studio version 2.0.0.952. The following steps describe how the FEM driver can be enabled in a BLE application project. The described software application is `ble_external_host`. With the configuration described in the following steps the `ble_external_host` is configured with DC-DC operation (default settings) when the radio is active and a programmed TX power level of `RF_TX_PWR_REG = 2`.

1. Enable the FEM driver in file `custom_config_qspi.h`

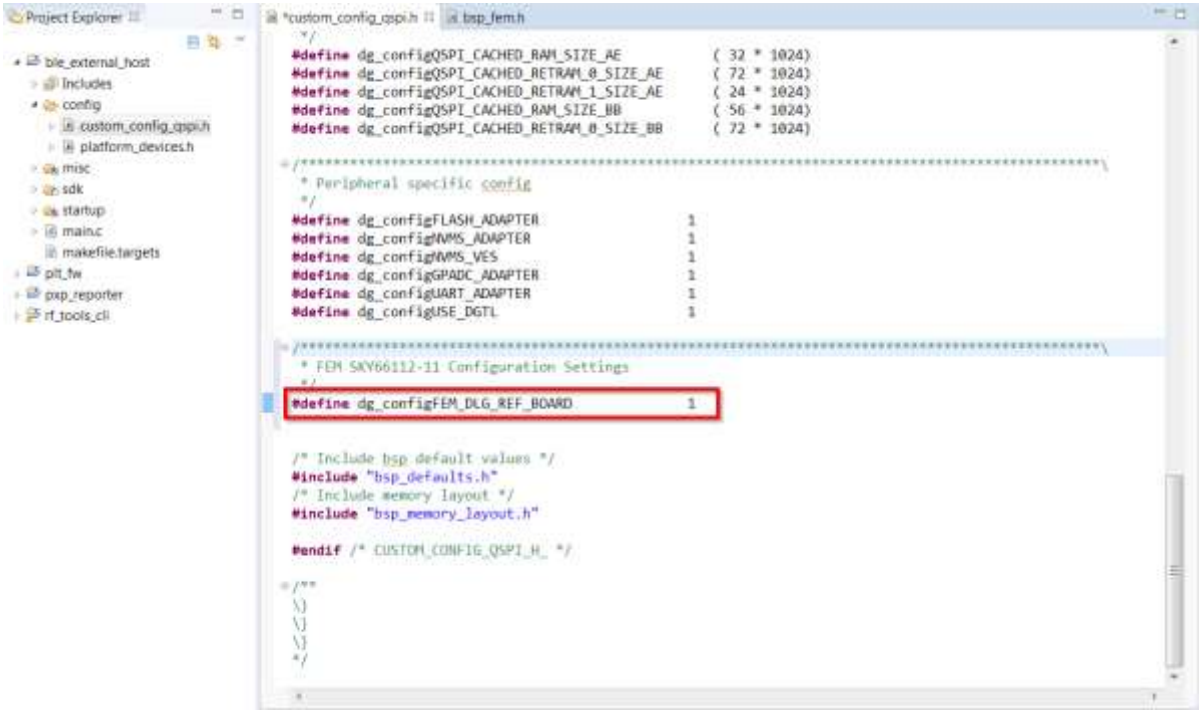


Figure 19: Enable FEM Driver in custom_config_qspi.h

2. Configure Flash connection to V18P power rail in custom_config_qspi.h.

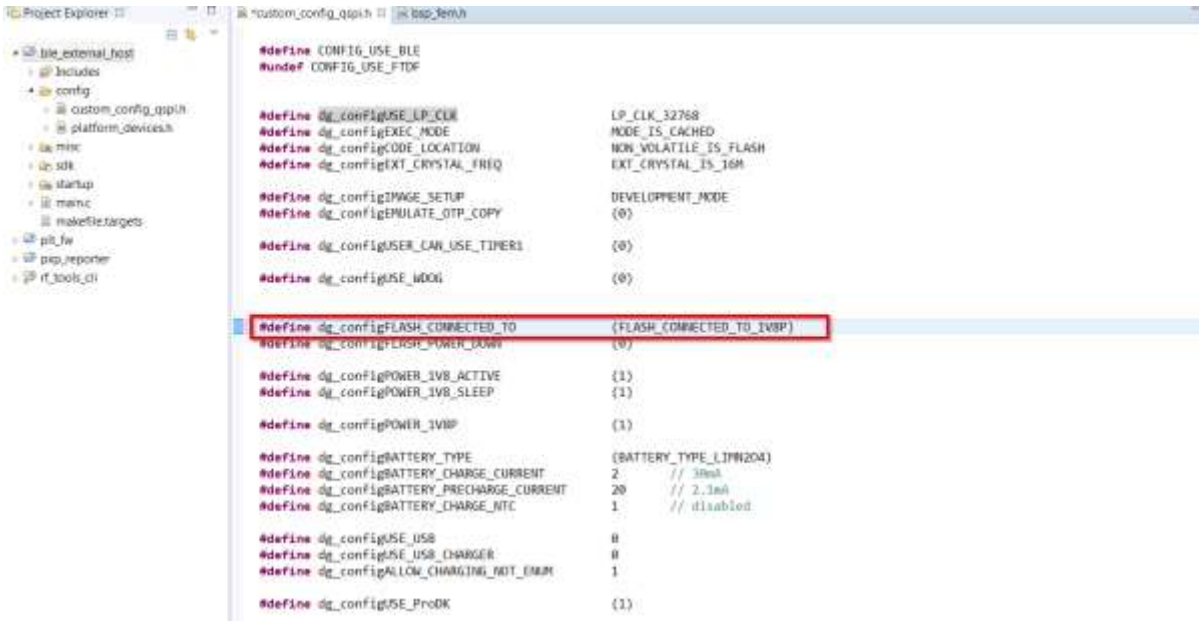


Figure 20: Flash Connection to V18P Power Rail in custom_config_qspi.h

3. Configure DA14681 power output to -2 dBm by adding the statement `hw_rf_set_tx_power(HW_RF_PWR_LUT_m2dbm);` in function `system_init()` in file `main.c`.

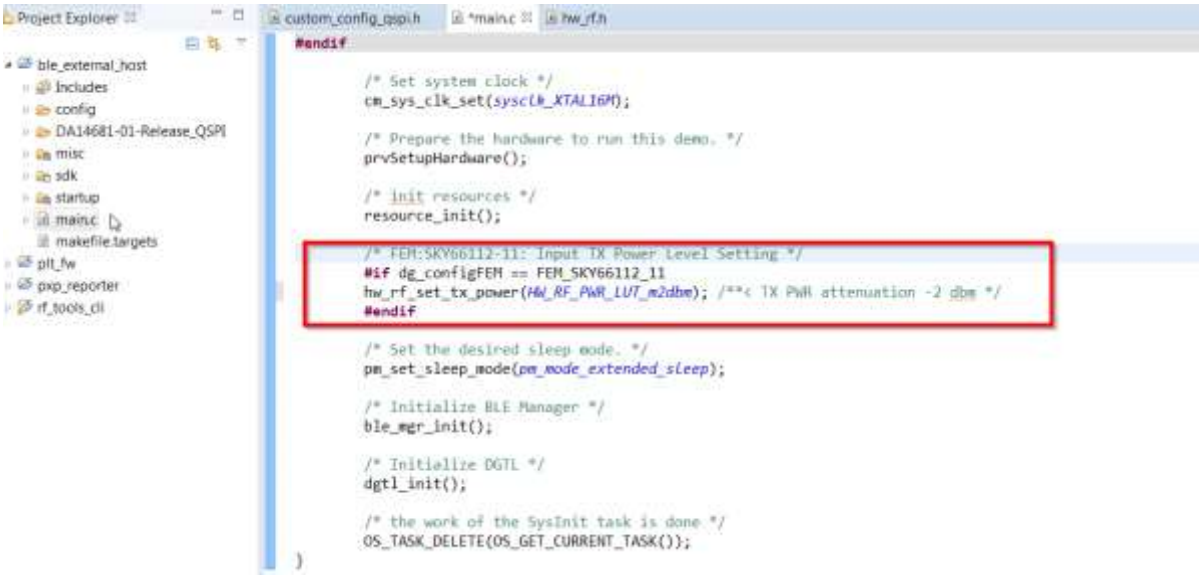


Figure 21: Configure DA14681 Power Output Level at -2 dBm

4. Include `hw_rf.h` in file `main.c`.

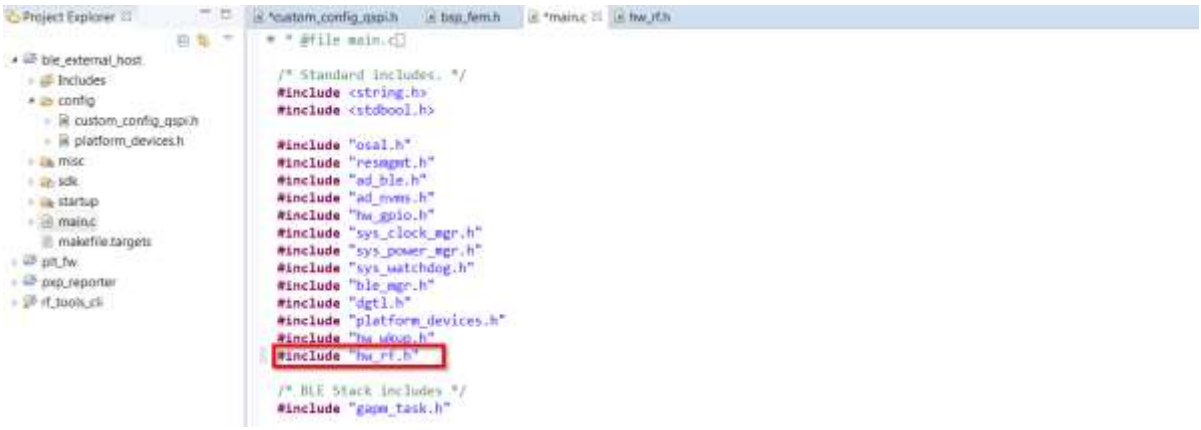


Figure 22: Include hw_rf.h in main.c

5. Select build configuration, e.g. for DA14681 and external Flash it is DA14681-01 release_QSPI.

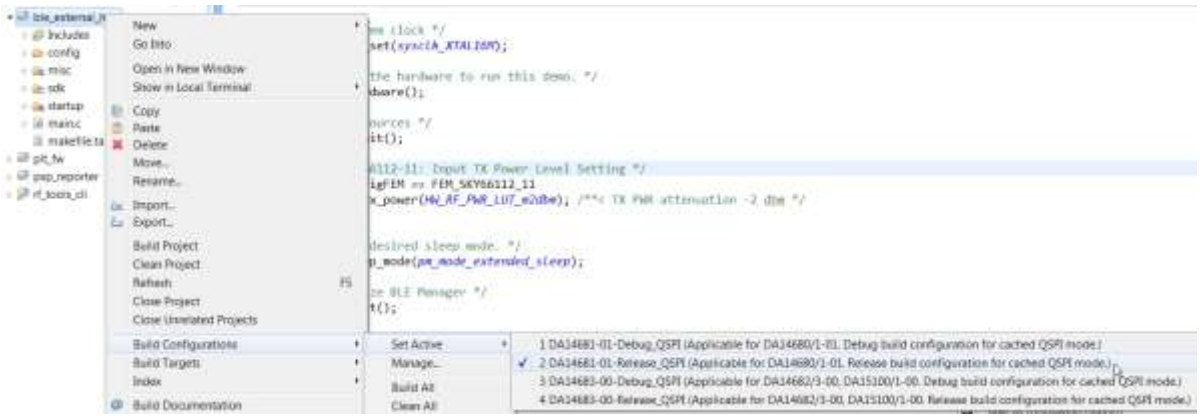


Figure 23: Set Build Configuration

6. Build the project.

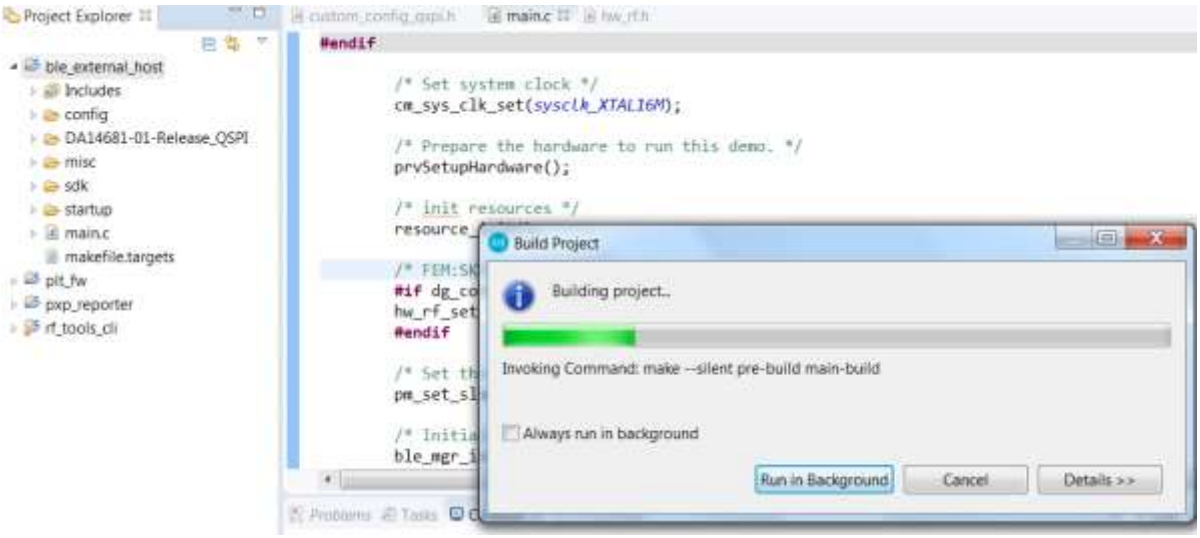


Figure 24: Building Project ble_external_host

7. Before writing the Flash, select the DA14680/1-01 product id configuration using the program_qspi_config_win script.

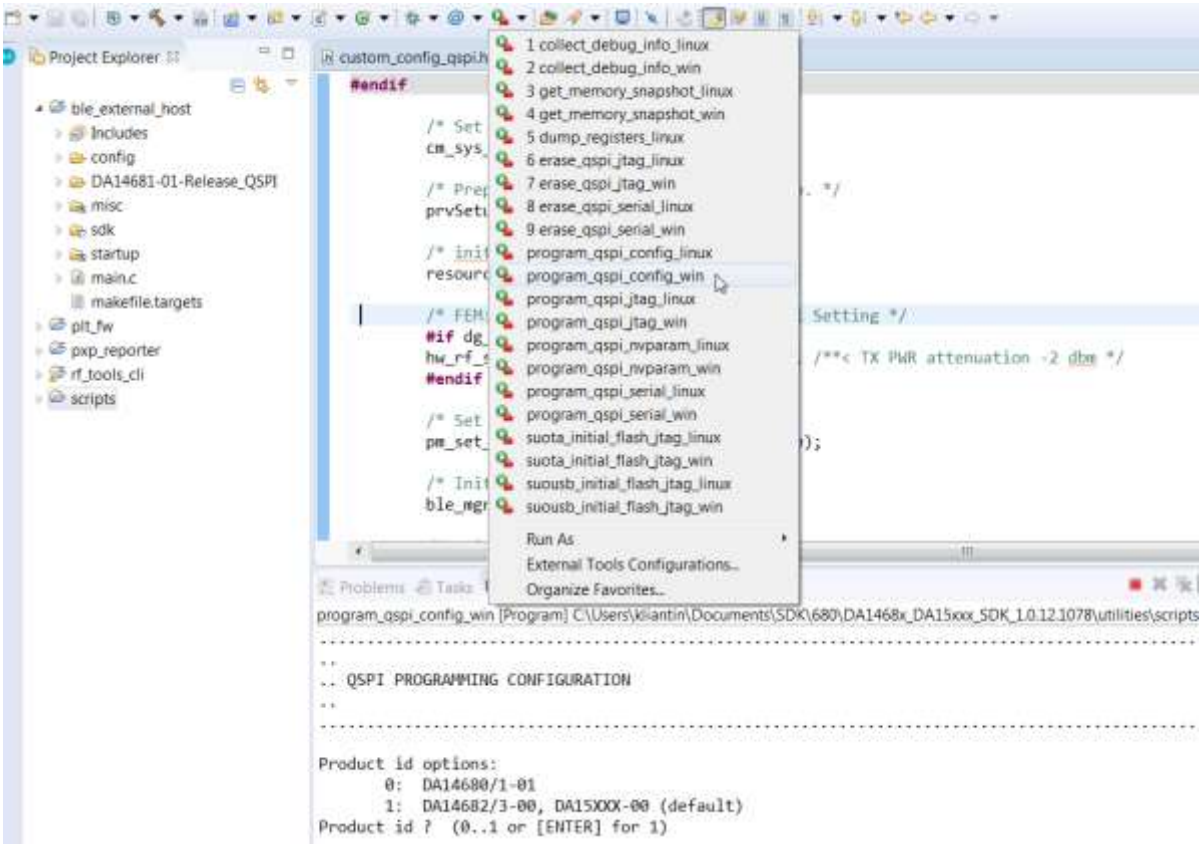


Figure 25: Configuration of correct product id DA14680/1-01

8. Use the produced binary output file for Flash memory programming.

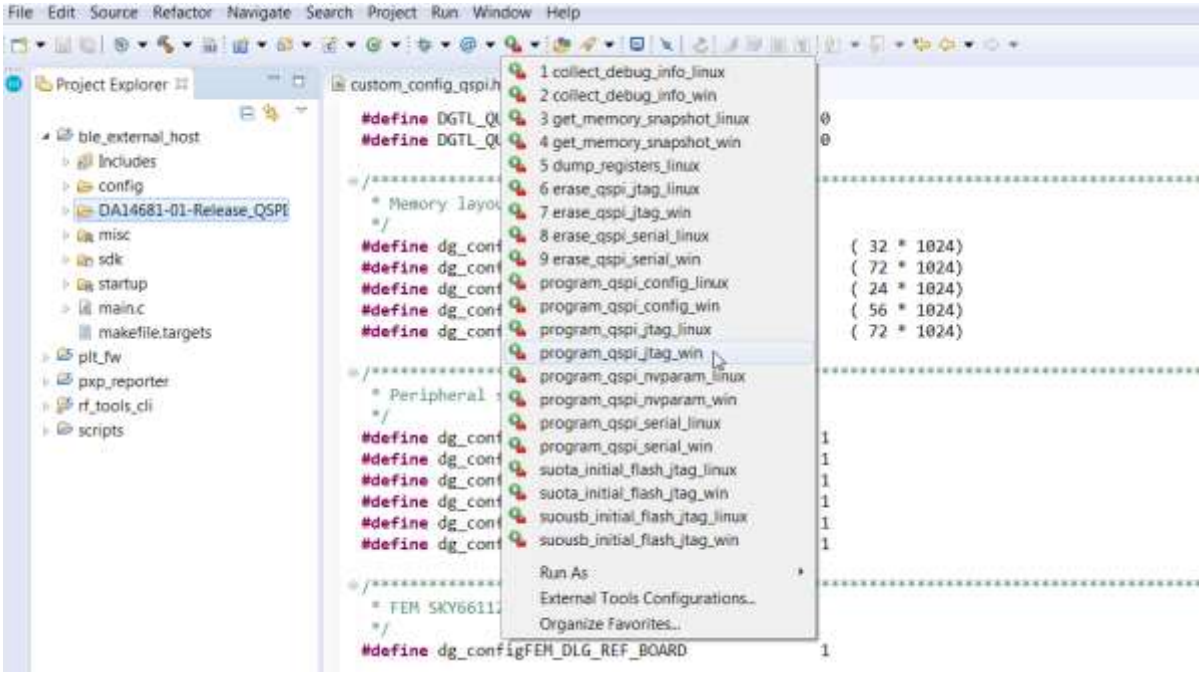


Figure 26: Programming External Flash Using ble_external_host.bin

15 BLE Measurements

15.1 Basic Performance Measurements

All measurements reported here use the following parameters:

Operating Conditions:

- T = 21 °C
- VBAT = 3 V

Equipment:

- Signal analyzer: Rohde & Schwarz FSV Spectrum analyzer
- R&S CBT - CBT go PC testing software
- Agilent N6705B DC power analyzer – Keysight 14585A Control and Analysis Software

Tools:

- SmartSnippets Toolbox v4.3.3.1378
- SmartSnippets Studio v1.3.2.636
- SDK RF Tools Command Line Interface Application

Test Procedure:

- The board is set to continuous modulated transmission mode for spectrum analyzer measurements.
- Continuous packet transmission mode was used for R&S CBT measurements.

Test Configuration:

All tests are performed with the following settings:

- DCDC_V18_VOLTAGE=0x16 default value (0x5000008C).
- R73=16.5 Ω. Sets the VCC2 level to 1200 mV.
- RF_TX_PWR_REG = 2 (0x500020C0). Sets the DA14680/681 TX output power to -2 dBm.

Measurements:

- Receiver sensitivity (section 15.1.1)
- Transmitter output power (section 15.1.2)
- Current consumption (section 15.1.3)

15.1.1 Receiver Sensitivity

15.1.1.1 Test Description

In this test the BLE RX sensitivity of DA14680/681 range extender (224-23-D) was measured.

15.1.1.2 Test Setup

The DA14680/681 range extender was mounted on a PRO-motherboard. The R&S® CBT Bluetooth® Tester from Rohde & Schwarz was used. An RF cable assembly was connected to the J3 RF Switch connector (MM8130-2600 by Murata) and at the other end through an attenuator to the R&S CBT Bluetooth Tester. In order to evaluate the RF sensitivity, `ble_external_host` firmware was used. The results from a dirty transmitter are reported below.

The RX tests were performed using the maximum payload length: 255 bytes.

15.1.1.3 Test Results

The conducted RF sensitivity with a dirty transmitter shows that the sensitivity is better than -94 dBm for all channels for maximum payload of 255 bytes.

Table 18: RX Sensitivity for VCC2 = 1.2 V (Note 1)

RX Sensitivity (dBm)		
Channel 0	**Channel 19**	**Channel 39**
-95.50	-95.20	-94.50

Note 1 VCC1 = 1.8 V, VDD = 3 V, P_{IN} = -2 dBm, Payload size = 255.

Test Name and Condition	Lower Limit	Upper Limit	Measured Value	P/F
RX Level @ *Ch: 00, PER: 29.40%, Count: 09*			-95.50 dBm	✓
RX Level @ *Ch: 01, PER: 30.13%, Count: 10*			-95.60 dBm	✓
RX Level @ *Ch: 02, PER: 31.47%, Count: 09*			-95.40 dBm	✓
RX Level @ *Ch: 03, PER: 29.33%, Count: 04*			-95.30 dBm	✓
RX Level @ *Ch: 04, PER: 29.47%, Count: 10*			-95.30 dBm	✓
RX Level @ *Ch: 05, PER: 31.07%, Count: 04*			-95.30 dBm	✓
RX Level @ *Ch: 06, PER: 31.60%, Count: 09*			-95.40 dBm	✓
RX Level @ *Ch: 07, PER: 29.00%, Count: 11*			-95.30 dBm	✓
RX Level @ *Ch: 08, PER: 29.67%, Count: 04*			-95.30 dBm	✓
RX Level @ *Ch: 09, PER: 31.60%, Count: 10*			-95.50 dBm	✓
RX Level @ *Ch: 10, PER: 31.80%, Count: 05*			-95.50 dBm	✓
RX Level @ *Ch: 11, PER: 31.07%, Count: 04*			-95.30 dBm	✓
RX Level @ *Ch: 12, PER: 32.60%, Count: 08*			-95.50 dBm	✓
RX Level @ *Ch: 13, PER: 29.20%, Count: 04*			-95.30 dBm	✓
RX Level @ *Ch: 14, PER: 32.80%, Count: 04*			-95.30 dBm	✓
RX Level @ *Ch: 15, PER: 30.67%, Count: 04*			-95.30 dBm	✓
RX Level @ *Ch: 16, PER: 31.87%, Count: 13*			-95.30 dBm	✓
RX Level @ *Ch: 17, PER: 31.13%, Count: 11*			-95.30 dBm	✓
RX Level @ *Ch: 18, PER: 31.53%, Count: 09*			-95.30 dBm	✓
RX Level @ *Ch: 19, PER: 30.33%, Count: 09*			-95.20 dBm	✓
RX Level @ *Ch: 20, PER: 32.13%, Count: 09*			-95.20 dBm	✓
RX Level @ *Ch: 21, PER: 31.27%, Count: 13*			-95.30 dBm	✓
RX Level @ *Ch: 22, PER: 30.40%, Count: 09*			-95.30 dBm	✓
RX Level @ *Ch: 23, PER: 29.93%, Count: 07*			-94.90 dBm	✓
RX Level @ *Ch: 24, PER: 31.80%, Count: 10*			-95.20 dBm	✓
RX Level @ *Ch: 25, PER: 29.13%, Count: 10*			-95.20 dBm	✓
RX Level @ *Ch: 26, PER: 32.40%, Count: 11*			-95.10 dBm	✓
RX Level @ *Ch: 27, PER: 31.87%, Count: 08*			-95.10 dBm	✓
RX Level @ *Ch: 28, PER: 32.60%, Count: 04*			-95.30 dBm	✓
RX Level @ *Ch: 29, PER: 30.07%, Count: 13*			-95.10 dBm	✓
RX Level @ *Ch: 30, PER: 31.07%, Count: 05*			-95.10 dBm	✓
RX Level @ *Ch: 31, PER: 30.33%, Count: 12*			-95.10 dBm	✓
RX Level @ *Ch: 32, PER: 29.60%, Count: 08*			-95.10 dBm	✓
RX Level @ *Ch: 33, PER: 29.40%, Count: 05*			-95.10 dBm	✓
RX Level @ *Ch: 34, PER: 29.27%, Count: 05*			-95.10 dBm	✓
RX Level @ *Ch: 35, PER: 30.20%, Count: 05*			-95.10 dBm	✓
RX Level @ *Ch: 36, PER: 31.80%, Count: 05*			-95.10 dBm	✓
RX Level @ *Ch: 37, PER: 32.00%, Count: 10*			-95.20 dBm	✓
RX Level @ *Ch: 38, PER: 30.80%, Count: 05*			-95.10 dBm	✓
RX Level @ *Ch: 39, PER: 29.67%, Count: 06*			-94.50 dBm	✓
Avg. Step Count @ *40 tests with totally 311 steps*			7.78	

Figure 27: RX Sensitivity, Dirty Transmitter, Payload = 255, VCC2 = 1.2 V, P_{IN} = -2 dBm

15.1.2 Transmitter Output Power

15.1.2.1 Test Description

In this test the conducted RF output power of DA14680/681 range extender was measured.

15.1.2.2 Test Setup

The DA14680/681 range extender was mounted on a PRO-motherboard. In order to evaluate the TX output power, `ble_external_host` firmware was used. Conducted transmitted output power was measured by using the R&S® CBT Bluetooth® Tester. An RF cable assembly was connected to J3 RF Switch connector (MM8130-2600 by Murata) and at the other end through an attenuator to the R&S CBT Bluetooth Tester.

- Bursts of 10 packets were transmitted by the DA14680/681.
- The packet length was 255 and the pattern was “01010101”.
- Three channels were recorded: channels 0, 19 and 39.

15.1.2.3 Test Results

Measurements were performed on a number of samples.

Table 19: Nominal Average TX Power, VCC2 = 1.2 V (Note 1)

Nominal Average TX Power (dBm)		
Channel 0	**Channel 19**	**Channel 39**
+13.55	+13.26	+13.07

Note 1 VCC1 = 1.8 V, VDD = 3 V, P_{IN} = -2 dBm.

Annex: **Nominal Power Graphic**

Mode: Channelscan, Start Channel: 00, Stop Channel: 39, Average: blue, Min: green, Max: red

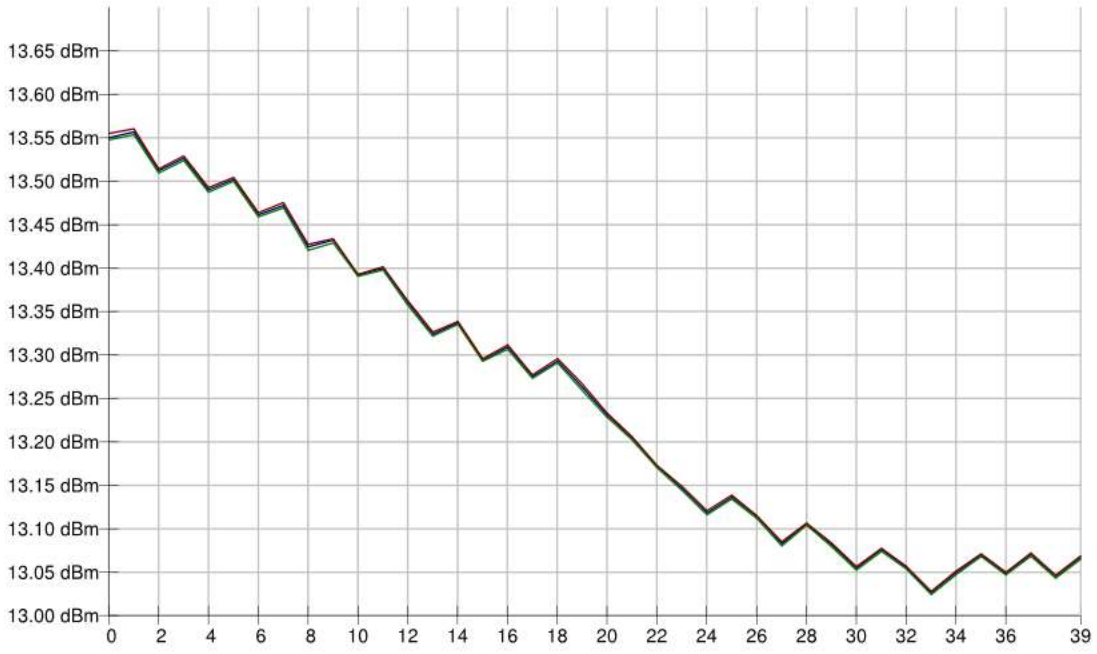


Figure 28: Nominal Average TX Power, VCC2_FEM = 1.2 V

15.1.3 Current Consumption

15.1.3.1 Test Setup

The board used in the test presented optimal RF performance. The integrated printed antenna was used to perform the measurements.

The following instruments were used for the test:

- Multimeter
- 3 V, 200 mA power source
- Agilent N6705B DC Power Analyzer

The current profiles were evaluated using advertising demo firmware with embedded PA control. During this test the Advertising, Connection and Extended Sleep modes were evaluated.

15.1.3.2 Advertising Mode

For this measurement the DUT was supplied by 3 V. FW was downloaded and the JTAG programmer and then it was disconnected.

Table 20 Typical Peak Current During Advertising Mode (Note 1)

Channel	Frequency (MHz)	Parameter	I_{PEAK} (mA)
0	2402	Ipeak0, TX	58.6
12	2426	Ipeak12, TX	56.2
39	2480	Ipeak39, TX	53.34

Note 1 VCC1 = 1.8 V, VCC2 = 1.2 V, VDD = 3 V, P_{IN} = -2 dBm.

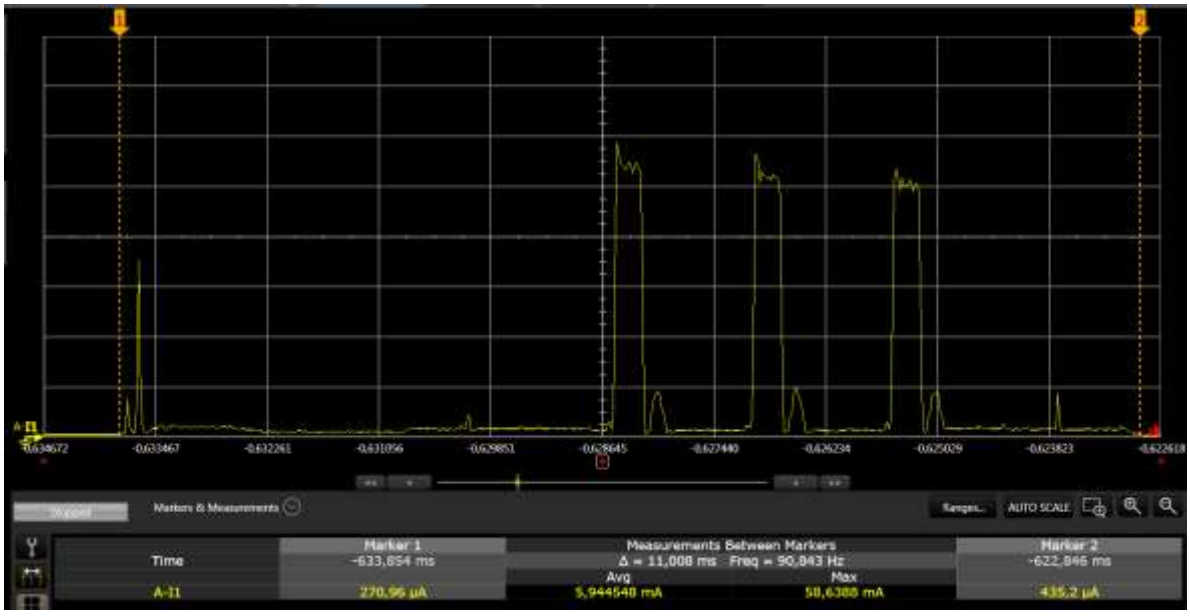


Figure 29: Peak Current During a BLE Advertising Event

15.1.3.3 Connection Mode

For this measurement the DUT was supplied by 3 V. FW was downloaded and the JTAG programmer was disconnected and connection with an iPhone 4S was established.

Table 21: Typical Peak Current during Connection Mode (Note 1)

Parameter	I_{PEAK} (mA)
Ipeak, TX	9.9

Note 1 VCC1 = 1.8 V, VCC2 = 1.2 V, VDD = 3 V, P_{IN} = -2 dBm.

Figure 30: Peak Current During a BLE Connection Event

15.1.3.4 Extended Sleep Mode

For this measurement the DUT was supplied by 3 V. FW was downloaded and the JTAG programmer was disconnected.

Table 22: Typical Average Current in Extended Sleep Mode (Note 1)

Parameter	I_{AV} (µA)
Imean	4.5

Note 1 VCC1 = 1.8 V, VCC2 = 1.2 V, VDD = 3 V, P_{IN} = -2 dBm.

Figure 31: Average Current During Extended Sleep Mode

15.2 BLE FCC Measurements

The measurements described below are in the context of pre-test FCC measurements. All measurements reported here use the following parameters:

Operating Conditions:

- T = 21 °C
- VBAT = 3 V

Test Configuration:

In order to comply with 15.247 FCC limits all tests are performed with the following settings:

- DCDC_V18_VOLTAGE = 0x16. Default value (0x5000008C).
- R73 = 16.5 Ω. Sets the VCC2 level to 1200 mV.
- RF_TX_PWR_REG = 2 (0x500020C0). Sets the DA14680/681 TX output power to -2 dBm.

Equipment:

- Signal analyzer Rohde & Schwarz FSV Spectrum analyzer

Tools:

- CLI programmer
- SDK RF Tools Command Line Interface Application for RF Test Commands

Test procedure:

Measurement method according to point 9.1.1 of Guidance for Performing Compliance: Measurements on Digital Transmission Systems (DTS) operating under 15.247.

Measurements:

- Maximum output power (section 15.2.1)
- Emission limitations conducted (harmonic level) (section 15.2.2)
- Band edge emissions (conducted) (section 15.2.3)
- Emission limitations radiated (restricted band edge) (section 15.2.4)
  - RA 2.31 GHz to 2.39 GHz
  - RB 2.4835 GHz to 2.5 GHz

The values mentioned below are for FCC compliance with Digital Transmission Systems (DTS) operating under 15.247.

Table 23: FCC 15.247 Compliance Pre-Tests Performed

Section	Subclause	Test Description	Verdict
Emission limitations conducted (transmitter)			
15.247	(a)	6 dB Bandwidth	PASS
15.247	(b)	Maximum output power and antenna gain	PASS
15.247	(d)	Emission limitations conducted (transmitter)	PASS
15.247	(d)	Band edge emissions conducted (transmitter)	PASS
15.247	(e)	Power spectral density (conducted)	PASS
Emission limitations radiated (transmitter)			
15.247	(d)	Frequency range 30 MHz to 1000 MHz	n.a.
		Frequency range 1 GHz to 25 GHz	n.a.
		RA 2.31 GHz to 2.39 GHz	PASS
		RB 2.4835 GHz to 2.5 GHz	PASS

15.2.1 Maximum Output Power and Antenna Gain (Transmitter)

15.2.1.1 Test Specification

For systems using digital modulation in the 2400 MHz to 2483.5 MHz band: 1 W (30 dBm).
The EIRP shall not exceed 4 W (36 dBm) (Canada).

15.2.1.2 Test Setup

The DA14680/681 range extender was mounted on a PRO-mb Development Board. In order to evaluate the maximum output power, the `SDK RF_Tool_CLI` was used. The boards under test were set into continuous wave modulation transmit mode, using the following command:
`ble_txstream \<FREQUENCY_MHz\> \<POWER\> \<PAYLOAD_TYPE\>`.

An RF cable was connected to the J3 RF Switch connector (MM8130-2600 by Murata) and at the other end to the spectrum analyzer. Three channels were tested: channels 0, 19 and 39.

15.2.1.3 Test Results

The maximum peak conducted power was measured using the method according to point 9.1.1 of Guidance for Performing Compliance Measurements on Digital Transmission Systems (DTS) operating under 15.247.

Maximum output power: see next plots.

Maximum declared antenna gain: 0 dBi.

Table 24: Maximum (Peak) Output Power (dBm), VCC2 = 1.2 V, CH00, CH19, CH39

Parameter (dBm)	CH00 – 2402 MHz	CH19 – 2440 MHz	CH39 – 2480 MHz
Maximum conducted power	+13.26	+13.27	+13.22
Maximum EIRP power	+13.26	+13.27	+13.22

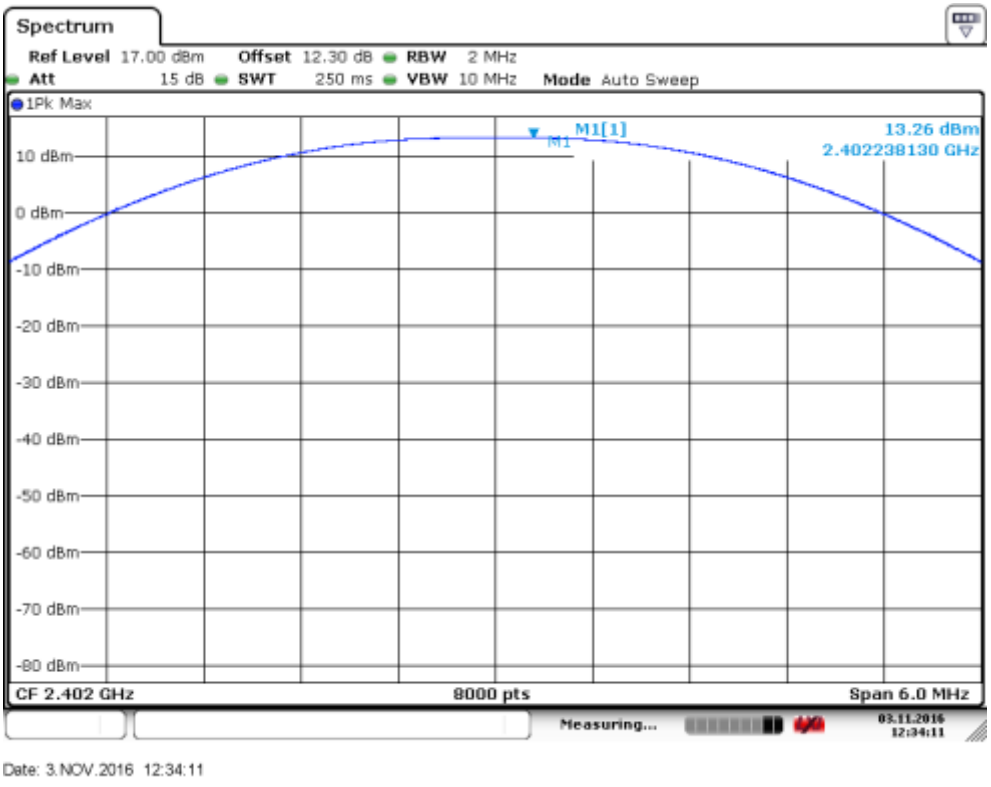


Figure 32: Maximum Output Power, CH00, VCC2 = 1.2 V

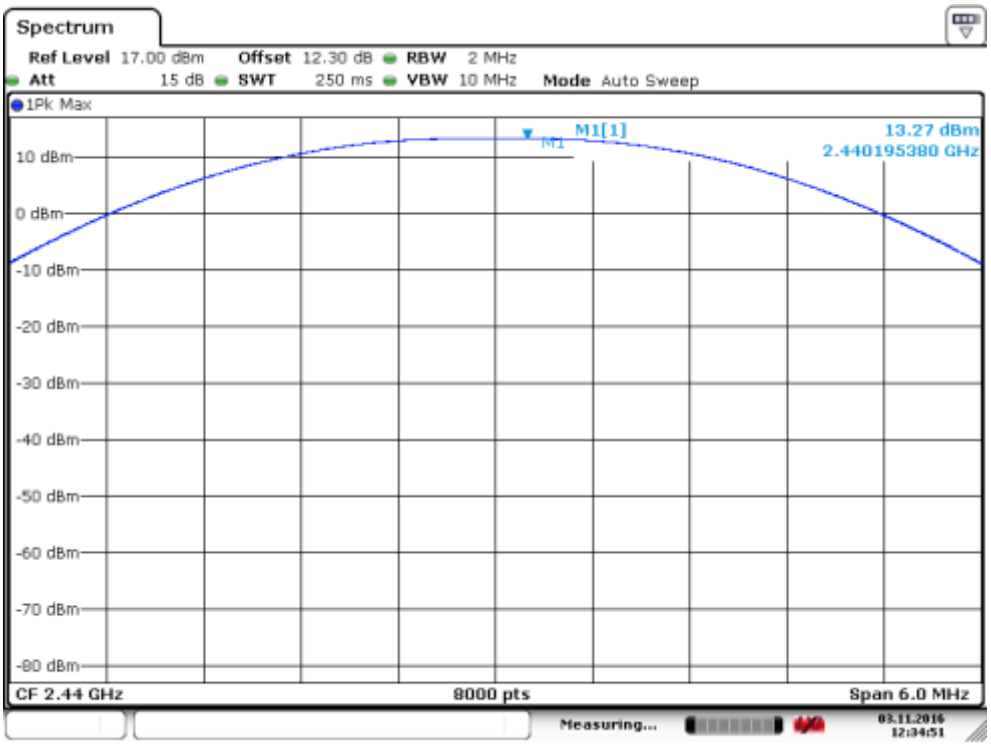


Figure 33: Maximum Output Power, CH19, VCC2 = 1.2 V

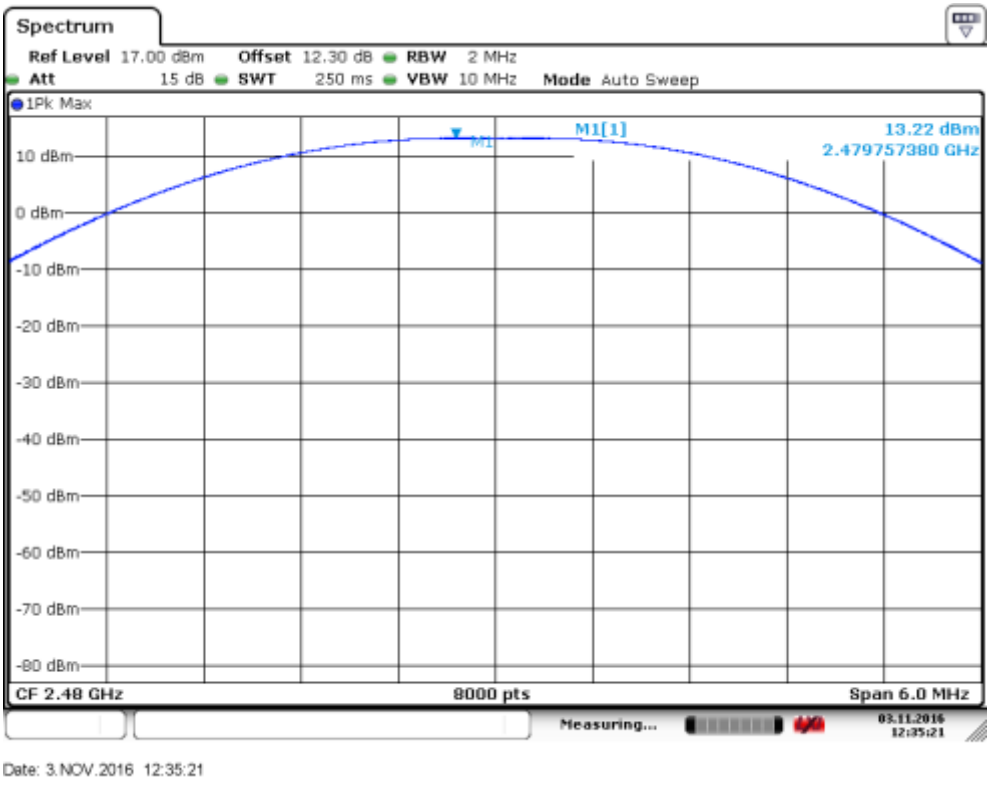


Figure 34: Maximum Output Power, CH39, VCC2 = 1.2 V

Verdict: All measurements comply with the limits specified in FCC 15.247, Subclause (b).

15.2.2 Emission Limitations Conducted (Transmitter)

15.2.2.1 Test Specification

In any 100 kHz bandwidth outside the frequency band in which the digitally modulated intentional radiator is operating, the radio frequency power that is produced by the intentional radiator shall be at least 20 dB below that in 100 kHz bandwidth within the band that contains the highest level of the desired power. If the transmitter complies with the conducted power limits based on the RMS averaging over a time interval, the attenuation required shall be 30 dB instead of 20 dB.

15.2.2.2 Test Setup

The DA14680/681 range extender was mounted on a PRO-motherboard. In order to evaluate the harmonic levels production, the `SDK RF_Tool_CLI` was used. The boards under test were set into continuous wave modulation transmit mode using the following command:
`ble_txstream \<FREQUENCY_MHz\> \<POWER\> \<PAYLOAD_TYPE\>`

An RF cable assembly was connected to J3 RF Switch connector (MM8130-2600 by Murata) and at the other end to the spectrum analyzer. Three channels were tested: channels 0, 19 and 39.

15.2.2.3 Test Results

Table 25: Measured Reference Level

Parameter (dBm)	CH00 – 2402 MHz	CH19 – 2440 MHz	CH39 – 2480 MHz
Reference Level	12.21	12.18	11.90
Limit (20 dB below peak)	-7.79	-7.82	-8.1

Table 26: Conducted TX Harmonics at CH00, CH19, CH39

Parameter (dBm)	CH00 – 2402 MHz	CH19 – 2440 MHz	CH39 – 2480 MHz
2nd harmonic power	-54.87	-53.54	-54.28
3rd harmonic power	-54.15	-49.51	-55.58
4th harmonic power	-	-	-60.84
5th harmonic power	-60.09	-58.98	-59.90

Lowest frequency: 2402 MHz

All peaks are more than 20 dB below the limit.

Middle frequency: 2440 MHz

All peaks are more than 20 dB below the limit.

Highest frequency: 2480 MHz

All peaks are more than 20 dB below the limit.

Verdict: All measurements comply with the limits specified in FCC 15.247, Subclause (d).

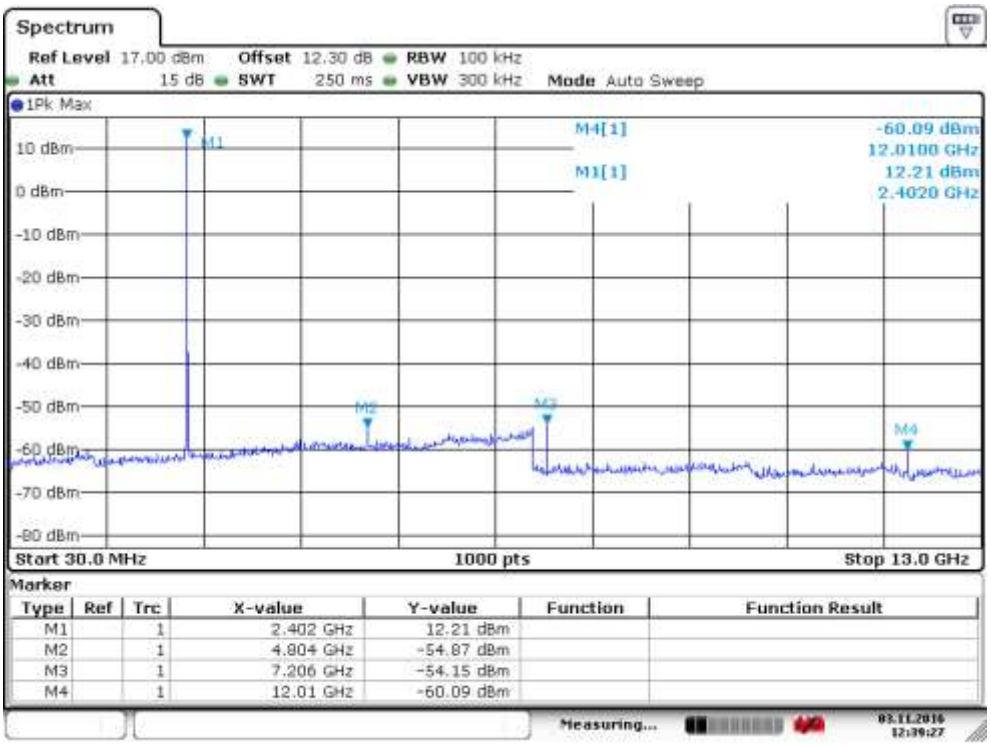


Figure 35: Harmonics Level, Lowest Frequency, CH00

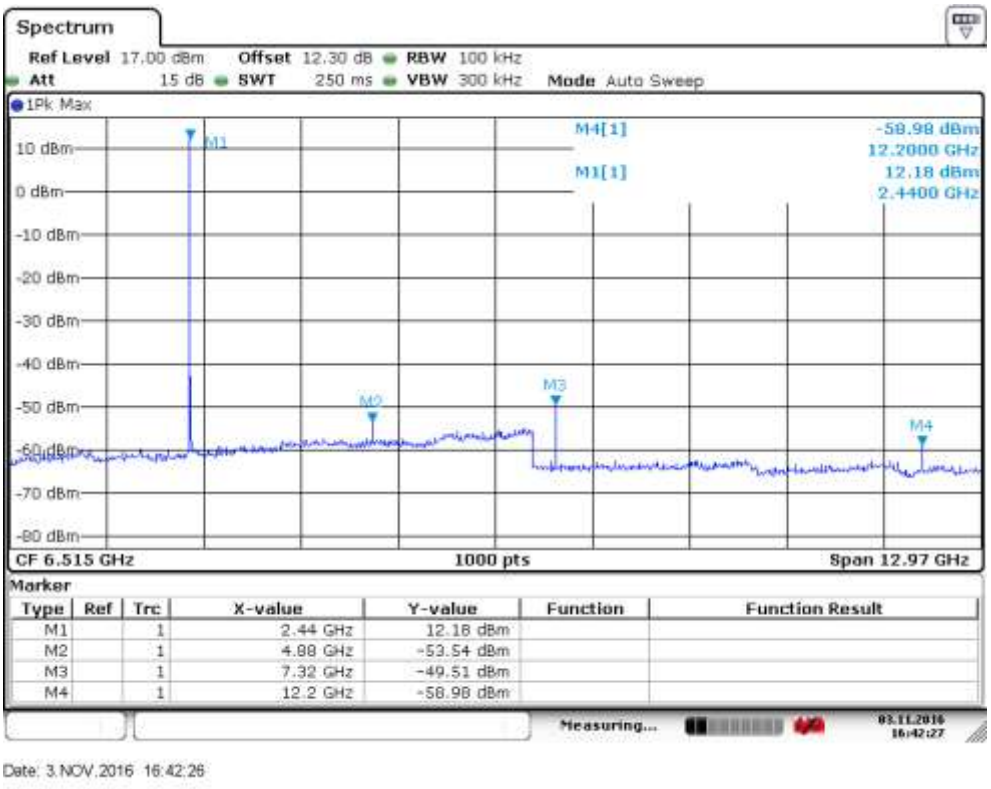


Figure 36: Harmonics Level, Middle Frequency, CH19

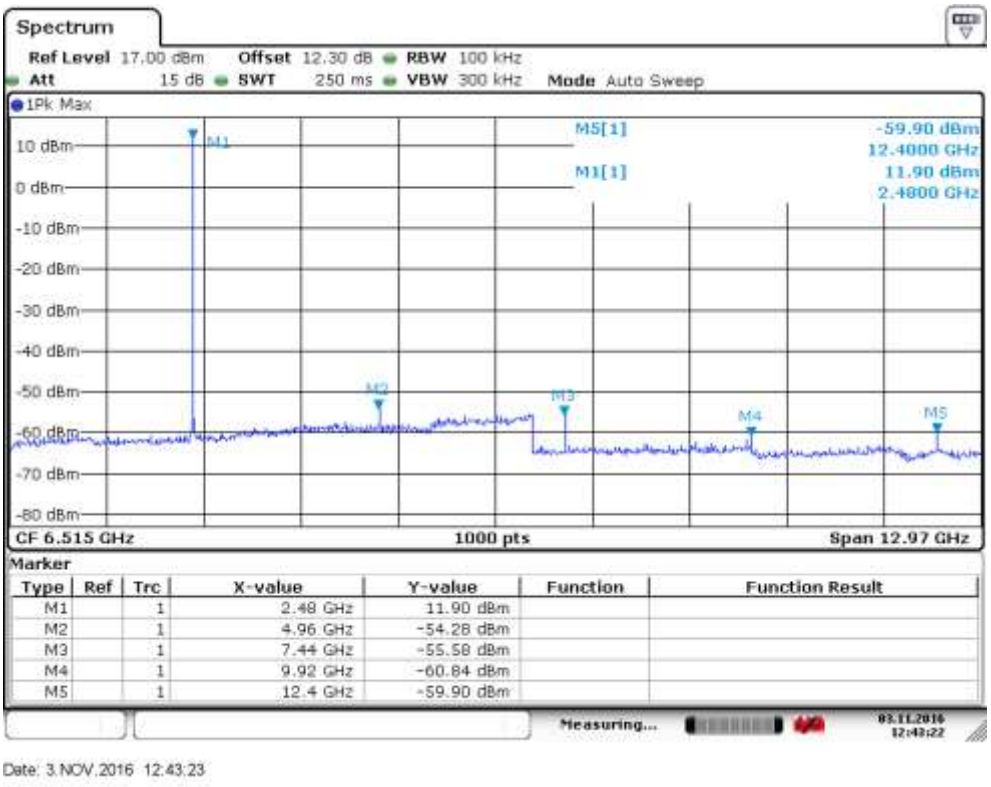


Figure 37: Harmonics Level, Highest Frequency, CH39

Verdict: All measurements comply with the limits specified in FCC 15.247, Subclause (d).

15.2.3 Band Edge Emissions Compliance (Transmitter)

15.2.3.1 Test Specification

In any 100 kHz bandwidth outside the frequency band in which the digitally modulated intentional radiator is operating, the radio frequency power that is produced by the intentional radiator shall be at least 20 dB below that in 100 kHz bandwidth within the band that contains the highest level of the desired power. If the transmitter complies with the conducted power limits based on the RMS averaging over a time interval, the attenuation required shall be 30 dB instead of 20 dB.

15.2.3.2 Test Setup

The DA14680/681 range extender was mounted on a PRO-motherboard. In order to evaluate the band edge emission levels for the upper and lower channels, the `SDK RF_Tools_CLI` was used. The boards under test, were set into continuous wave modulation transmit mode using the command: `ble_txstream \<FREQUENCY_MHz\> \<POWER\> \<PAYLOAD_TYPE\>`.

An RF cable assembly was connected to the J3 RF Switch connector (MM8130-2600 by Murata) and at the other end to the spectrum analyzer. Two channels were tested: channels 0 and 39.

15.2.3.3 Test Results

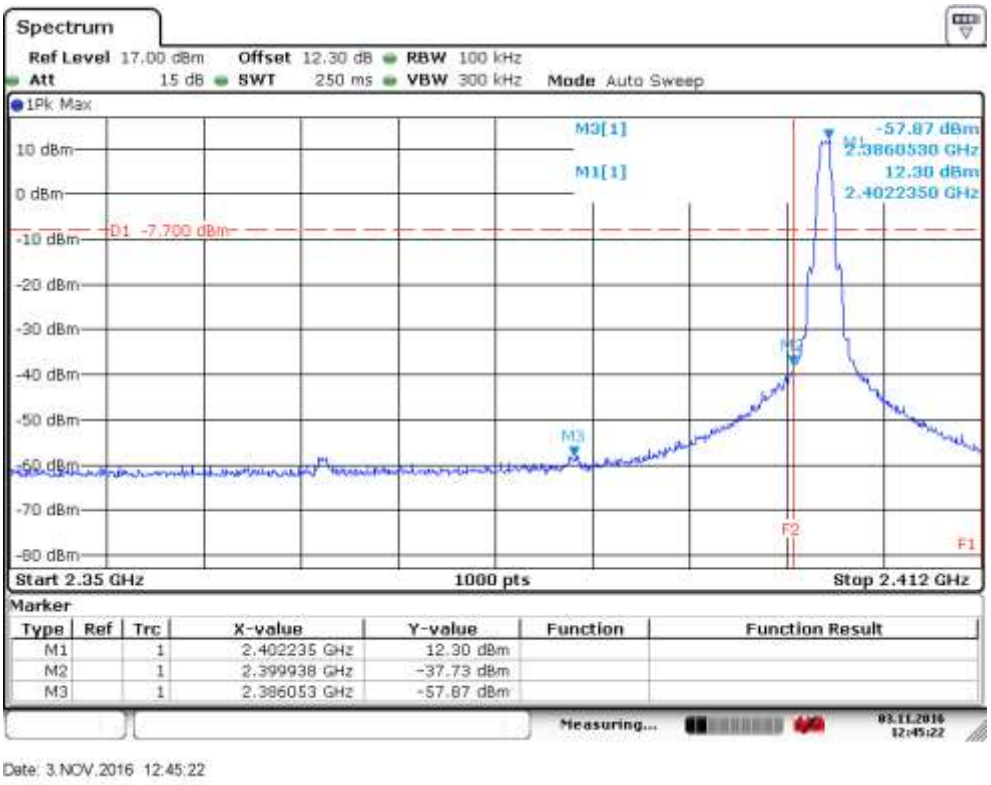


Figure 38: Lower Band Edge, CH00

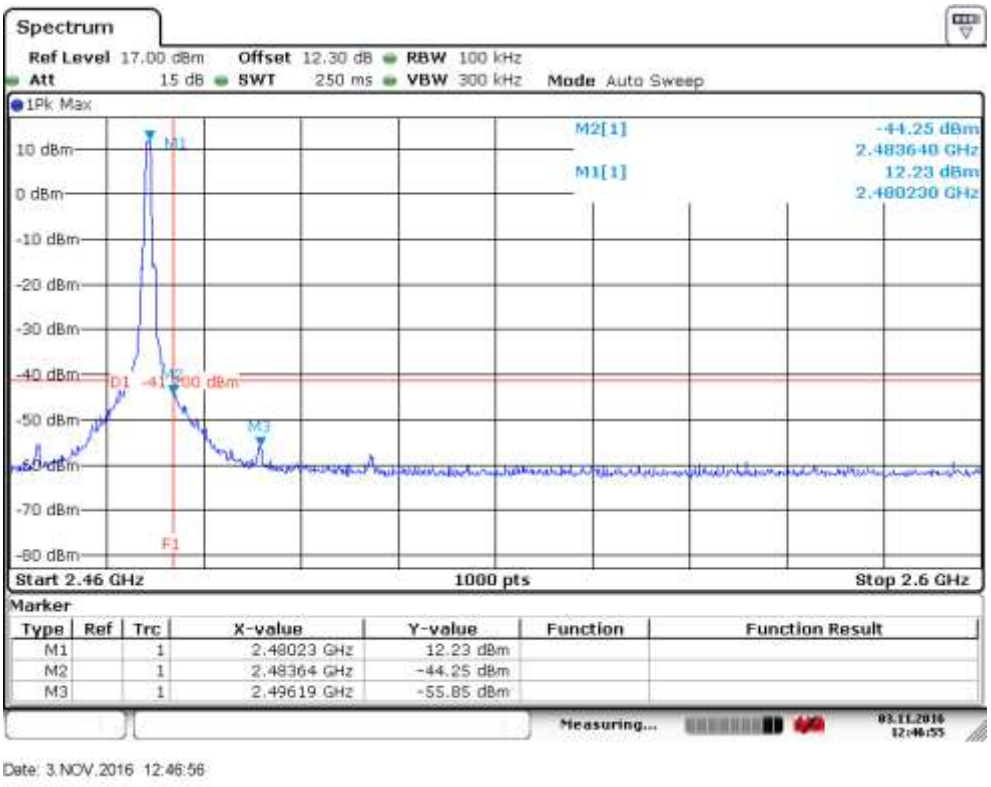


Figure 39: Upper Band Edge, CH39

Verdict: All measurements comply with the limits specified in FCC 15.247, Subclause (d).

15.2.4 Emission Limitations Radiated (Transmitter)

15.2.4.1 Test Specification

Radiated emissions which fall in restricted bands, as defined in FCC 15.205 must also comply with the radiated emission limits specified in FCC 15.209. See Figure 40.

Frequency Range (MHz)	Field strength (µV/m)	Field strength (dBµV/m)	Measurement distance (m)
0.009-0.490	2400/F(kHz)	-	300
0.490-1.705	24000/F(kHz)	-	30
1.705 - 30.0	30	-	30
30 - 88	100	40	3
88 - 216	150	43.5	3
216 - 960	200	46	3
960 - 25000	500	54	3

Figure 40: FCC Radiated Emission Limits

The emission limits shown in the table above are based on measurements employing a CISPR quasi–peak-detector, except for frequency bands 9 kHz to 90 kHz, 110 kHz to 490 kHz and above 1000 MHz. Radiated emission limits in these three bands are based on measurements employing an average detector.

For average radiated emission measurements above 1000 MHz, there is also a limit corresponding to 20 dB above the specified values, which applies when measuring with a peak detector function.

15.2.4.2 Test Setup

The measurement was performed in a conducted way, using the measurement settings for the radiated test. These results may differ from the radiated ones.

Only the emissions for the frequency range of 2.31 GHz to 2.39 GHz (Restricted Band A) and 2483.5 GHz to 2.5 GHz (Restricted Band B) were measured.

The DA14680/681 range extender was mounted on a PRO-motherboard. In order to evaluate the emissions in the restricted bands for the upper and lower channel, the `SDK RF_Tools_CLI` was used. The boards under test were set into continuous wave modulation transmit mode using the command: `ble_txstream \<FREQUENCY_MHz\> \<POWER\> \<PAYLOAD_TYPE\>`.

An RF cable assembly was connected to the J3 RF Switch connector (MM8130-2600 by Murata) and at the other end to the spectrum analyzer. Three channels were tested: channels 0, 19 and 39.

15.2.4.3 Test Results

Lower Restricted Area of 2.31 GHz to 2.39 GHz (RA)

Both peak and RMS values are more than 16 dB below the limit.

Upper Restricted Area of 2.4835 GHz to 2.5 GHz (RB)

Both peak and RMS values are below the limit. Peak values have a worst case margin of more than 10 dBm while RMS has a margin of more than 1 dBm from the limit. See Table 27.

Only the channels closest to the Restricted Areas are shown in the plots, because the present the highest emission values.

Table 27: Emissions Levels in Restricted Areas RA and RB for CH00, CH19 and CH39

f_{CH} (MHz)	M1 (peak)	M2 (RMS)	Peak Limit	RMS Limit	Peak Margin	RMS Margin	Conditions
Restricted Area RA: 2.31 GHz to 2.39 GHz							
2402	-44.86	-55.54	-21.2	-41.2	23.66	14.34	RF_TX_PWR_REG = 2 (-2 dBm), VCC2 = 1200 mV, CHL = 0
2440	-45.33	-56.92	-21.2	-41.2	24.13	15.72	RF_TX_PWR_REG = 2 (-2 dBm), VCC2 = 1200 mV, CHL = 0
2480	-45.61	-56.98	-21.2	-41.2	24.41	15.78	RF_TX_PWR_REG= 2 (-2 dBm), VCC2 = 1200 mV, CHL = 0
Restricted Area RB: 2.4835 GHz to 2.5 GHz							
2402	-39.67	-51.17	-21.2	-41.2	18.47	9.97	RF_TX_PWR_REG = 2 (-2 dBm), VCC2 = 1200 mV, CHL = 0
2440	-39.32	-50.76	-21.2	-41.2	18.12	9.56	RF_TX_PWR_REG = 2 (-2 dBm), VCC2 = 1200 mV, CHL = 0
2480	-32	-42.33	-21.2	-41.2	10.8	1.13	RF_TX_PWR_REG = 2 (-2 dBm), VCC2 = 1200 mV, CHL = 0

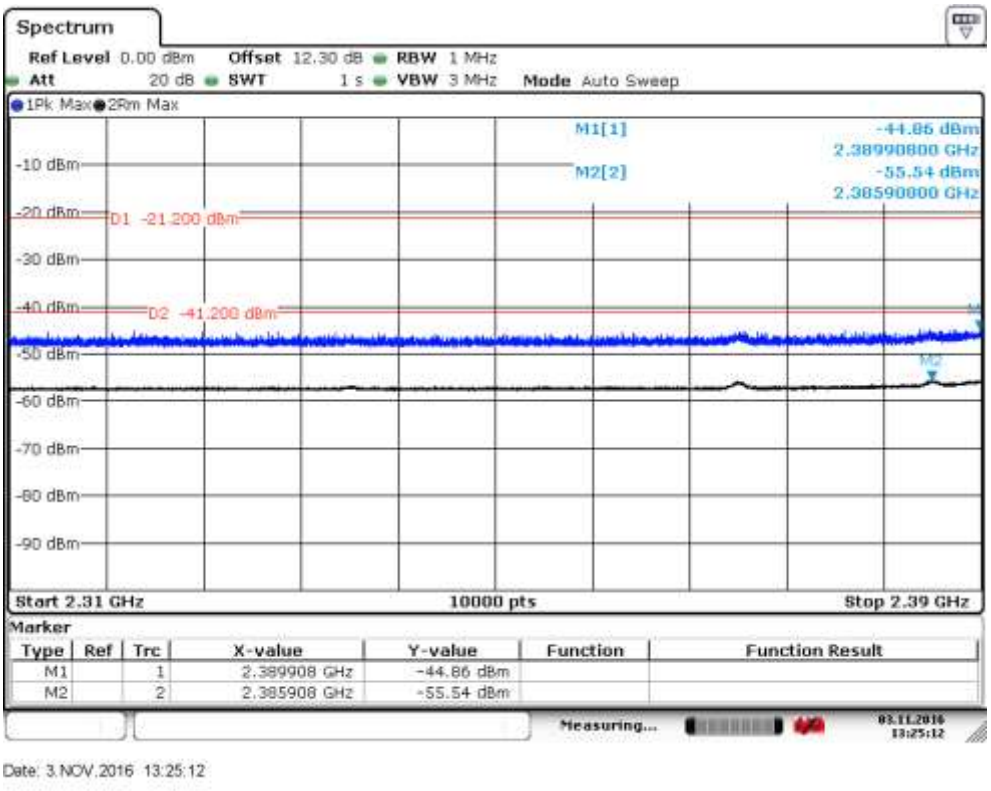


Figure 41: Emissions in Restricted Band RA 2.31 GHz to 2.39 GHz, CH00

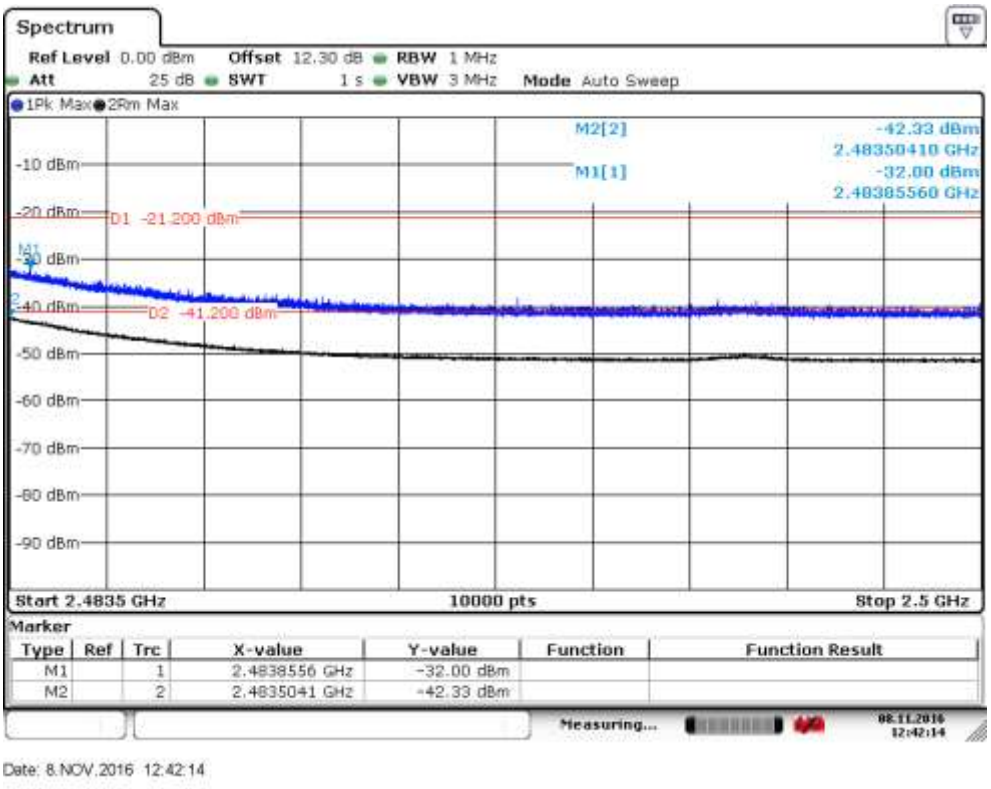


Figure 42: Emissions in Restricted Band RB 2.4835 GHz to 2.5 GHz, CH39

Appendix A Application Software Guide: ble_adv_demo

The following instructions are based on DA1468x SDK 1.0.12 and SmartSnippets™ Studio version 2.0.0.952. The described software application is `ble_adv`. With the configuration described in the following steps the `ble_adv` is configured with DC-DC operation (default settings) when the radio is active and a programmed TX power level of `RF_TX_PWR_REG = 2`.

1. Enable the FEM driver in file `custom_config_qspi.h`.

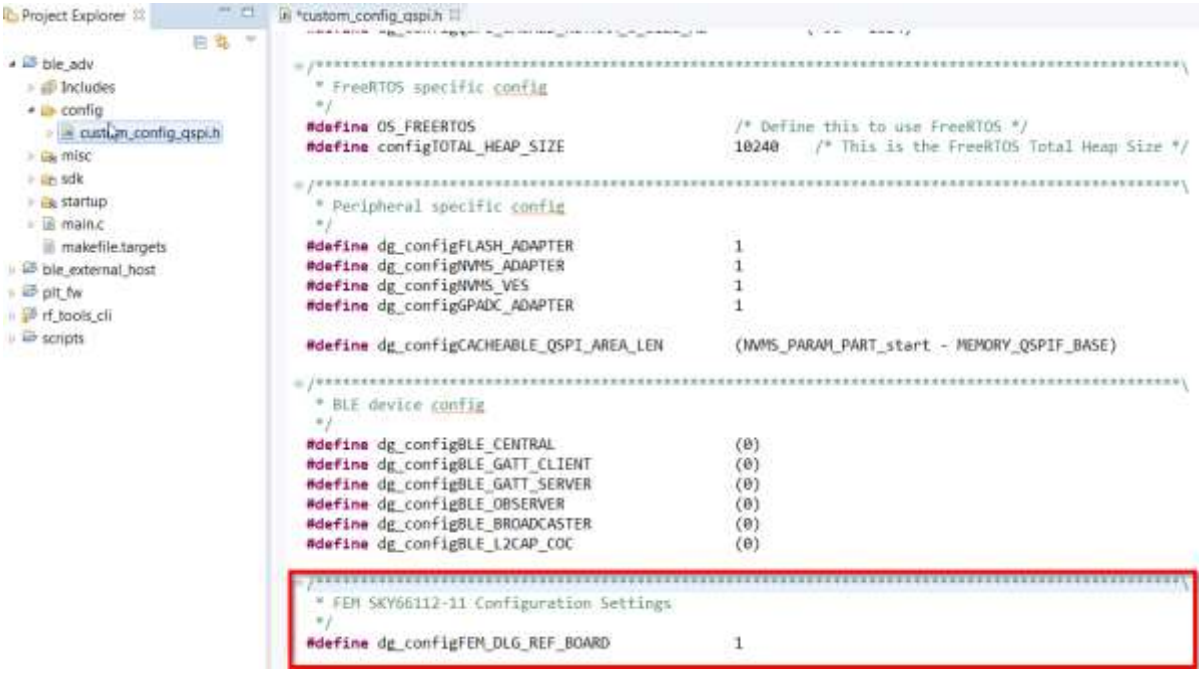


Figure 43: Enable FEM Driver in custom_config_qspi.h

2. Configure Flash connection to V18P power rail in custom_config_qspi.h.

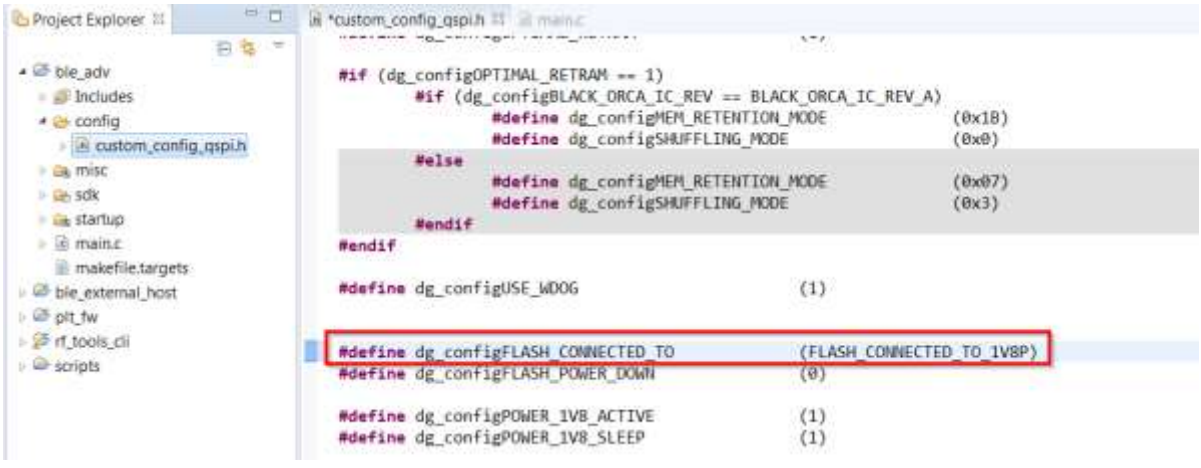


Figure 44: Flash Connection to V18P Power Rail in custom_config_qspi.h

3. Configure the DA14681 power output to -2 dBm by adding the statement `hw_rf_set_tx_power(HW_RF_PWR_LUT_m2dbm);` in function `system_init()` in file `main.c`.

Figure 45: Configure DA14681 Power Output Level at -2 dBm

4. Include `hw_rf.h` in file `main.c`.

Figure 46: Include hw_rf.h in main.c

5. Select build configuration, e.g. for DA14681 and external Flash it is DA14681-01 release_QSPI.

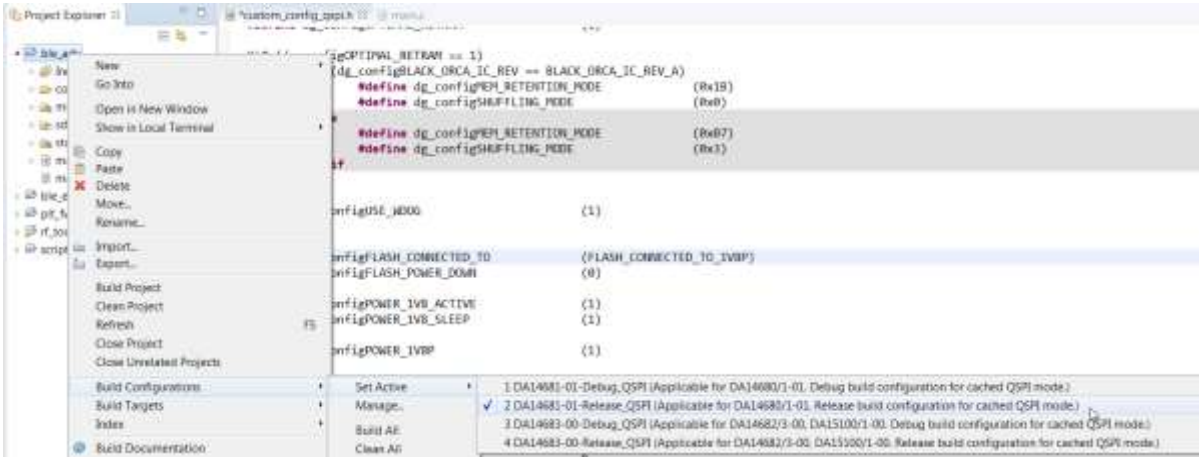


Figure 47: Set Build Configuration

6. Build the project.

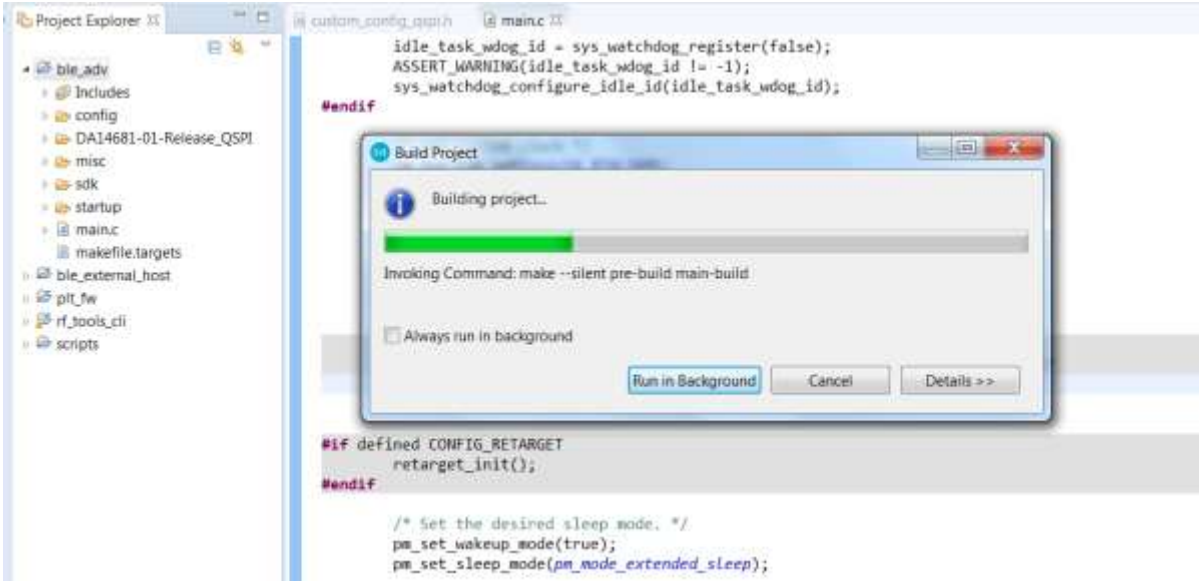


Figure 48: Building Project ble_adv

7. Use the produced binary output file for Flash memory programming.

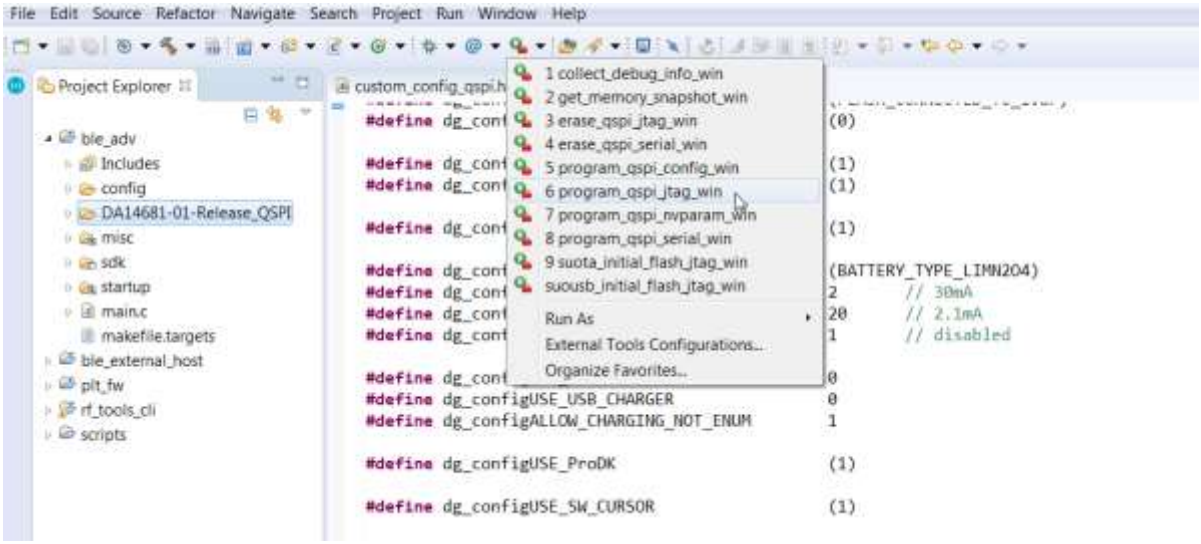


Figure 49: Programming External Flash Using ble_adv.bin

Revision History

Revision	Date	Description
1.2	09-Nov-2016	Updated logo, disclaimer, copyright.
1.1	17-Apr-2018	Updated instructions on software guide based on SDK 1.0.12.1078 -Chapter 14: Application Software Guide: ble_external_host -Appendix A: Application Software Guide. ble_adv
1.0	09-Nov-2016	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.