User Manual

DA14585 Range Extender Reference Application

UM-B-089

Abstract

This document describes the hardware system setup of a range extender daughterboard based on the Dialog DA14585 Bluetooth® low energy SoC and the Skyworks SKY66111-11 Front End Module. Target hardware: DA14585_rd_qfn40_fem_module_vB – Board Number: 321-13-B. Target silicon: DA14585

Contents

Figures

Tables

1 Terms and Definitions

ADC	Analog to Digital Converter
BLE	Bluetooth® Low Energy
BOM	Bill of Materials
dBm	decibel-milliwatts
dBµV/m	decibel-microvolts per meter
EIRP	Effective Isotropic Radiated Power
FEM	Front End Module
FW	Firmware
GPIO	General Purpose Input/ Output
I2C	Inter-Integrated Circuit
IFA	Inverted-F Antenna
LPF	Low Pass Filter
MBd	Megabaud
PA	Power Amplifier
PCBA	Printed Circuit Board Assembled
PCB	Printed Circuit Board
RF	Radio Frequency
RFCU	RF Control Unit
RX	receive(r)
SoC	System on Chip
SPI	Serial Peripheral Interface
TX	transmit(ter)

2 References

[1] UM-B-034, DA14580_581_583 Bluetooth Smart Development Kit - Pro_v1.4, User Manual, Dialog Semiconductor.

[2] SKY66111-11, Datasheet, Skyworks Inc.

[3] DA14585 Bluetooth 5.0 SoC with Audio Interface, Datasheet, Dialog Semiconductor.

[4] UM-B-008, DA14580_581_583 Production Line Tool reference CLI_v1.7, User Manual, Dialog Semiconductor.

[5] AN-B-020, End Product testing and programming guidelines, Application Note, Dialog Semiconductor.

[6] AN-B-027, Designing Printed Antennas for Bluetooth® Smart, Application Note, Dialog Semiconductor.

3 Introduction

The DA14585 Range Extender (321-13-B) is a reference design based on DA14585 Bluetooth Low Energy 5.0 SoC, where enhanced RF transmitted power is presented. The DA14585 Range Extender board serves as a reference design to potential customers requesting enhanced BLE RF Programmable Output Power up to +9.3 dBm. From physical perspective, the board consists of a 2-layer PCBA where the digital and power interfaces of the DA14585 are accessible to the user. This document presents the system, technical specifications, physical dimensions and test results.

Figure 1: PCB of the DA14585 Range Extender (321-13-B)

4 System Overview

4.1 Features

- Highly integrated DA14585 Bluetooth Low Energy 5.0 SoC
- Can be used stand-alone or as a data pump on a system with an external processor
- Complies to Bluetooth v5.0, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)
- Buck mode operation
- Operating voltage: 1.8 V to 3.6 V
- Maximum BLE transmit output power +9.3 dBm (See Note 1)
- Programmable transmit output power with steps of 2dBm
- Includes two crystal oscillators: 16 MHz (XTAL16M) and 32.738 kHz (XTAL32K)
- Access to processor via JTAG, SPI, UART or I2C interface
- 21 general purpose I/Os with programmable voltage levels
- On-board printed inverted F-type antenna (Figure 4)
- U.FL connector for conducted measurements (Figure 4)
- BLE Radio transceiver (See Note 2):
  - receiver sensitivity better than -91 dBm (See Note 3)
- Supply current (See Note 4):
  - TX: max. current < 17 mA
  - RX: max. current < 6 mA
  - Extended - Sleep current: <5 µA
- 34 mm x 42 mm, 2 layer PCBA
- Operating temperature: –40 ºC to +85 ºC
- Test FW based on 585 SDK 6.0.6

Note 1 Conducted power

Note 2 FCC part 15.247, 15.209 compliance.

Note 3 Dirty transmitter: ON, 1500 packets, payload PRBS9 length 37bytes.

Note 4 Normal operation, using SDK proximity reporter application, TX output power +9.3 dBm, peak values.

Table 1: Electrical Characteristics (Note 6)

Parameter	Value
TX Output Power	BYPASS: -1.5 dBm ZERO_DBM: 0 dBm TWO_DBM: +2 dBm FOUR_DBM :+4 dBm SIX_DBM: +6 dBm EIGHT_DBM: +8 dBm MAX_POWER: +9.3 dBm
RX Sensitivity(See Note 3)	better than -91 dBm
Maximum current consumption in TX mode	BYPASS< 6 mA ZERO_DBM<10.5 mA TWO_DBM<11.5 mA FOUR_DBM <12.5 mA SIX_DBM<13.5 mA EIGHT_DBM<15 mA MAX_POWER <17 mA
Maximum current consumption in RX mode	< 6 mA
Average current consumption during sleep mode	< 5 µA

Note 6 Peak Maximum Ratings

4.2 System Description

The system consists of DA14585 SoC in aQFN40 package (see Ref.[3]), the SKY66111-11 RF Front End Module (see Ref. [2]), external crystals of 16 MHz and 32.768 kHz, a discrete low pass filter and an external circuit that controls the power supply of the SKY66111-11. The radio front end is connected to a PCB trace antenna.

The power amplifier is controlled by CTRL_TX and CTRL_RX control signals. CTRL_TX is generated from pin P0_1 and CTRL_RX is generated from pin P0_2 of DA14585 SoC. On pin P0_1 and P0_2 the internal Radio_TXEN and Radio_RXEN signals are allocated by software.

An external TX power control circuit is used for adjusting the voltage level of SKY66111-11 VCC power supply pin. By adjusting VCC the output power of the PA can be regulated. Two control signals generated from pins P2_1 and P2_7 drive the external power control circuit.

The system can be configured to operate in three different modes:

- Programmable Output Power Mode: 0 to +8dBm in steps of 2 dBm
- Maximum Output Power Mode: +9.3 dBm
- Bypass Mode: -1.5 dBm

External connections provide access to Supply, DC/DC configuration, available Peripheral IO, Test, Software Development and OTP Programming.

The amplifier circuit is the SKY66111-11 from Skyworks. The CTX pin is used as the TX control signal and amplifier bias voltage. CTX pin is connected to the amplifier BIAS pin via resistor RBIAS. The resistor value is adjusted in order to get the maximum allowed output power (+9.3dBm, see Note 7).

Note 7 FCC part 15.247, 15.209 compliance

A system overview is shown in Figure 2.

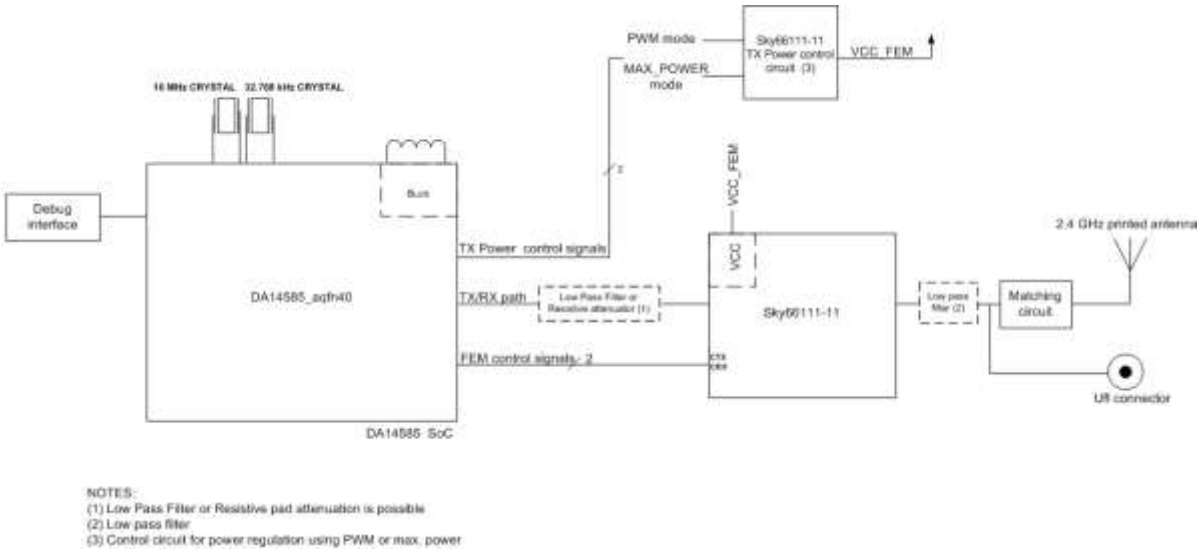


Figure 2: Block Diagram of Range Extender (321-13-B)

4.3 System Interface

DA14585 Range Extender daughterboard is plugged into header J4 of the DA14580 PRO-Dev.Kit Motherboard, as shown in Figure 3.

The PRO-motherboard provides UART and JTAG (SWD) interfaces to the DA14585, current measurement circuitry, as well as breakout headers (J5, J7) for the available GPIOs and general purpose user peripherals. For more details on the functionality and specifications of the motherboard, refer to user manual UM-B-034 (see Ref. [1]).

The system is powered via the Debug USB port (J12). The daughterboard can also be independently programmed, using an external battery connected on the board coin cell connector (see Section 5 for more details). The layout and main features of the daughterboard are shown in Figure 4.

Figure 3: DA14585 Range Extender (321-13-B) on a DA14580 PRO-Dev.Kit Motherboard

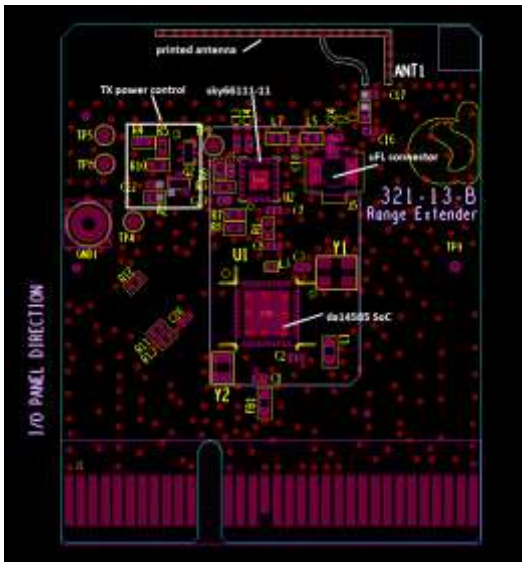


Figure 4: Layout of the DA14585 Range Extender daughterboard

5 System Power Supply

There are three options for powering the system when using the DA14580 PRO-Dev.Kit Motherboard.

- The PRO motherboard's voltage regulator (VDD_3V3_PERF, see Ref. [1]), which is powered from USB (J12).
- A coin cell battery on the PRO motherboard (BT1).
- A coin cell battery on the daughterboard of DA14585 Range Extender.

The power source is selectable with jumper header J11 from PRO Dev.Kit to either coin cell on PRO Dev.Kit or USB (Figure 3).

The different configurations for each of the power schemes using the DA14580 PRO-Dev.Kit Motherboard are described in Table 2.

Table 2: Jumper Settings for Power Schemes of DA14580 PRO-Dev.Kit Motherboard

Power Scheme	Indication DA14580 Power	J11	USB
Motherboard LDO	USB	1-2	Power + programming
Coin cell Battery mounted on motherboard (BT1)	BAT	2-3	Programming
Coin cell Battery mounted on daughterboard	-	**open**	Programming

Warning: If the coin cell on the daughterboard is used then jumper J11 should be left open.

6 Bluetooth® Low Energy SoC

The DA14585 integrated circuit (see Ref.[3]), is an optimized version of the DA14580, offering a reduced boot time and supporting up to 8 connections. It has a fully integrated radio transceiver and baseband processor for Bluetooth® Low Energy. It can be used as a standalone application processor or as a data pump in hosted systems.

The Bluetooth Low Energy firmware includes the L2CAP service layer protocols, Security Manager (SM), Attribute Protocol (ATT), the Generic Attribute Profile (GATT) and the Generic Access Profile (GAP). All profiles published by the Bluetooth SIG as well as custom profiles are supported.

The transceiver interfaces directly to the antenna and is fully compliant with the Bluetooth 5.0 standard.

The DA14585 has dedicated hardware for the Link Layer implementation of Bluetooth Low Energy and interface controllers for enhanced connectivity capabilities.

The DA14585 is based on an ARM Cortex M0 CPU and provides 0.9dMIPS/MHz. It is used for assisting the Bluetooth LE protocol implementation, as well as providing processing power for calculations or data fetched, that may be required by the application. Finally, it is used for housekeeping, including control of the system's power scheme.

It has a 128KB ROM containing the Bluetooth Smart protocol stack as well as the boot code sequence, a 64 kB OTP (One-Time Programmable) memory array, used to store the application code and 94kB total RAM. Storage of this data ensures secure and quick configuration of the BLE Core after the system wakes up. Every cell can be powered on or off according to the application needs for retention area when in Extended Sleep mode.

The DA14585 has an audio interface that comprises three separate blocks: a PDM block, a PCM/I2S block and a Sample Rate Converter (SRC block) with DMA support.

The main debug port for the DA14585 is the JTAG. JTAG consists of two signals, SWDIO and SWCLK.

The external digital interfaces available for the module are:

- 2 UARTs with hardware flow control up to 1 MBd
- SPI+™ interface
- I2C bus at 100 kHz or 400 kHz
- 3-axis capable Quadrature Decoder

There is also a 4-channel 10-bit ADC; it is available externally on the module.

The module includes 25 GPIOs (including JTAG signals) that are externally available. The interfaces are multiplexed with the GPIOs and can be enabled by appropriate programming.

The DA14585 SoC has a complete power management function integrated with Buck or Boost DC-DC converter and separate LDOs for the different power domains of the system. For this module, the DC-DC converter is configured as a Buck converter (C2, L1 and C3).

The DA14585 SoC is available in three packages: WLCSP34, QFN40 and QFN48. In this reference application the QFN40 is used.

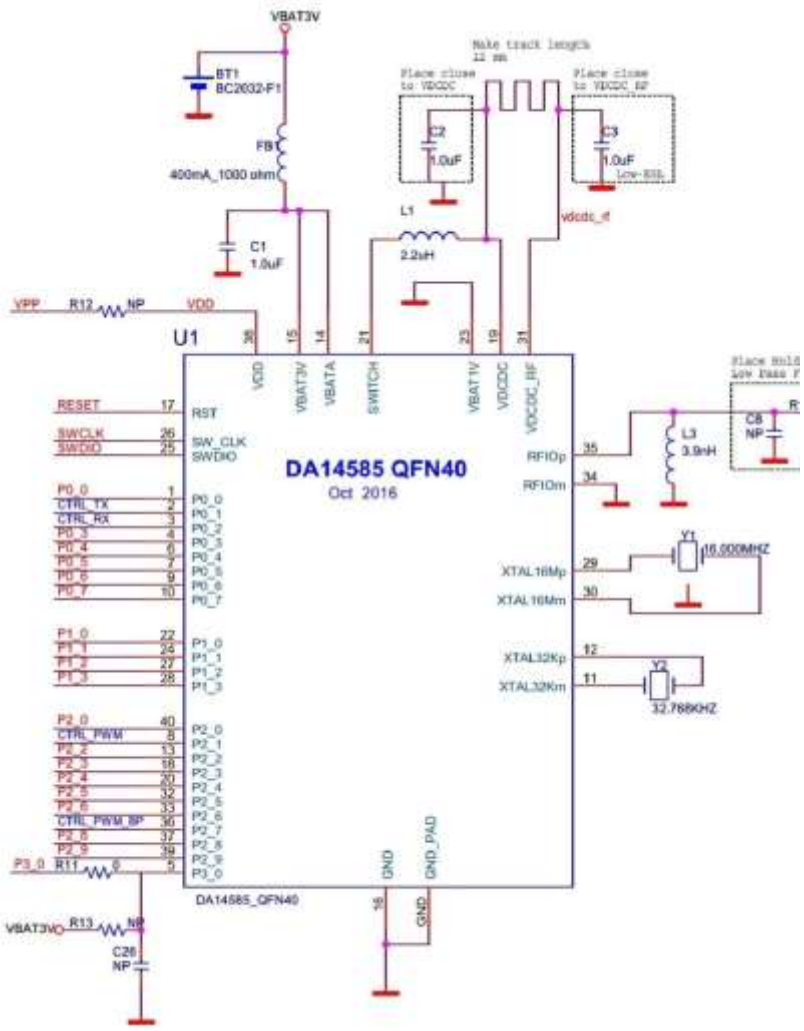


Figure 5:DA14585 QFN40 SoC DA14585 Range Extender

7 RF Front End

This part of the design is implementing the amplification of the RF transmitted signal while the transmitted harmonics as well as the TX spurious emissions remain within the FCC/ ETSI specification.

The operation of the RF Front End Module (FEM) is controlled by the DA14585 SoC. During the operation of the FEM there are two available RF paths:

- TX path through the amplifier
- TX/RX bypass path

The amplifier path is enabled during transmission. The RF signal passes through the PA, the low pass filter and the RF matching network. In the bypass path, the RF signal received at the antenna is driven directly to the BLE transceiver. The bypass path can be also used from the TX. In this case the PA of the FEM is not used. Insertion loss in the reception mode is 0.9dBm (see Ref. [2]).

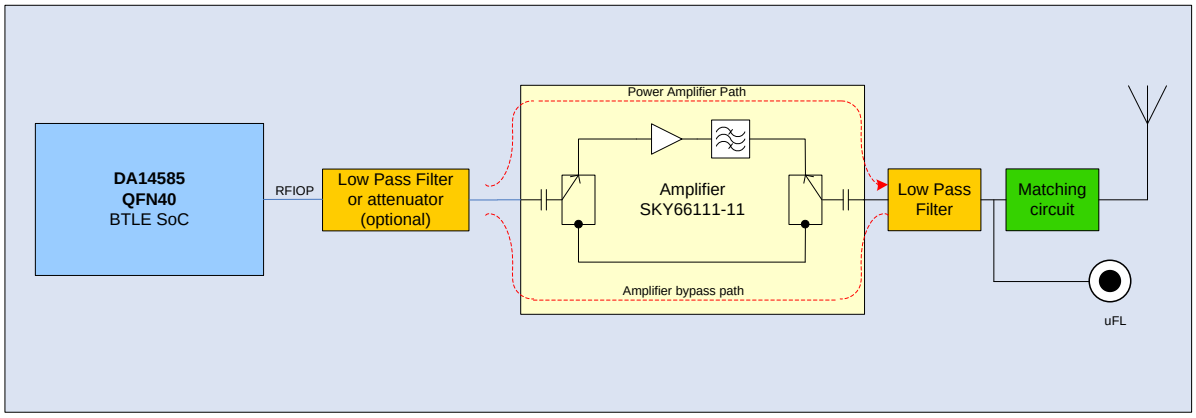


Figure 6: RF Front End signal paths

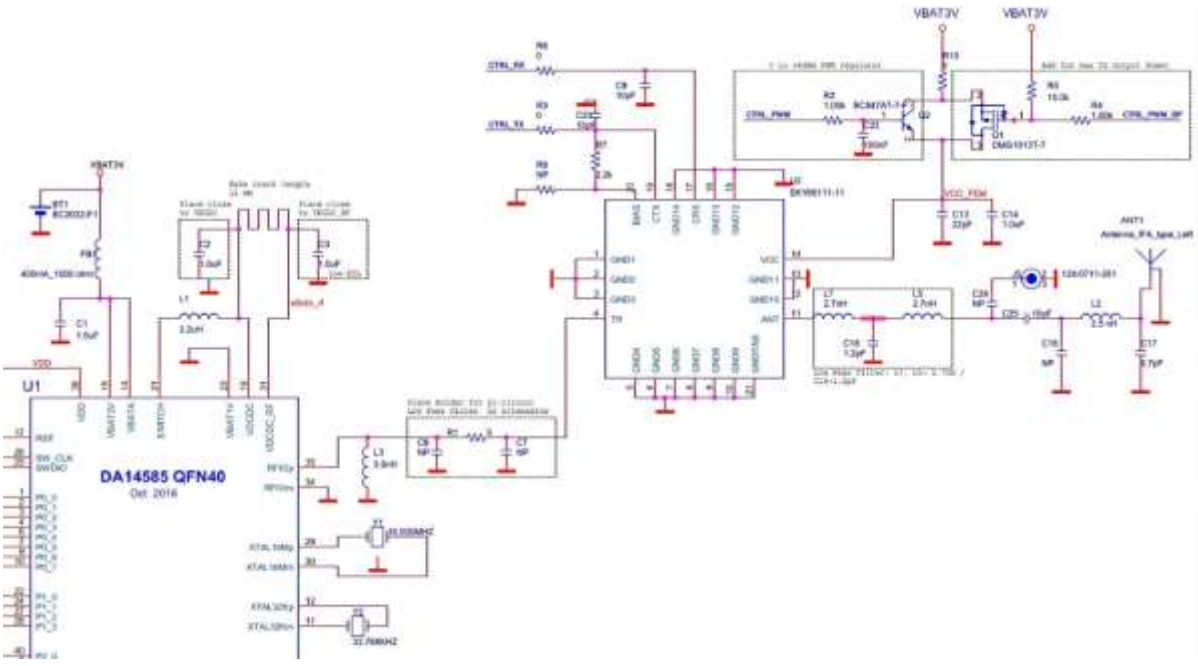


Figure 7: RF Front End schematic

7.1 Power amplifier

The amplifier circuit is the SKY66111-11 from Skyworks (see Ref.[2]). The SKY66111-11 is a fully integrated RF Front End Module (FEM) designed for Smart Energy applications. The device provides a PA and digital controls compatible with 1.7 V to 5 V CMOS levels. The basic characteristics for the SKY66111-11 are:

- TX Power:10 dBm
- TX current: 10mA
- RX sensitivity: SoC+1 (see Note 8)
- RX current: 1 µA
- Sleep current< 1 µA
- Supply operation:1.8 to 5 V
- CTX and CRX control signals
- RX bypass
- One antenna port

Note 8 The FEM presents around 1dBm insertion loss when receiving signals than the SoC alone.

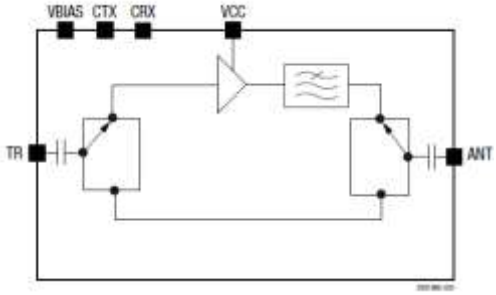


Figure 8: SKY66111-11 Power Amplifier

The SKY66111-11 CTX pin is used as the TX control signal and amplifier bias voltage while CRX pin is used as the RX control signal.

The SKY66111-11 BIAS pin supplies the bias to the internal PA. By varying the voltage at this pin, PA operating parameters including gain, supply current, and efficiency can be adjusted. The desired bias voltage can also be generated by connecting BIAS to the GPIO controlling CTX with a resistor. In the current design, the BIAS pin is connected to the CTX via resistor R7, providing a constant voltage of VBIAS=1.8 V when the PA is enabled. The resistor value is adjusted so that the maximum +9.3 dBm output power is achieved.

More information regarding the output power adjustment of the PA can be found in SKY66111-11 datasheet (see Ref. [2]).

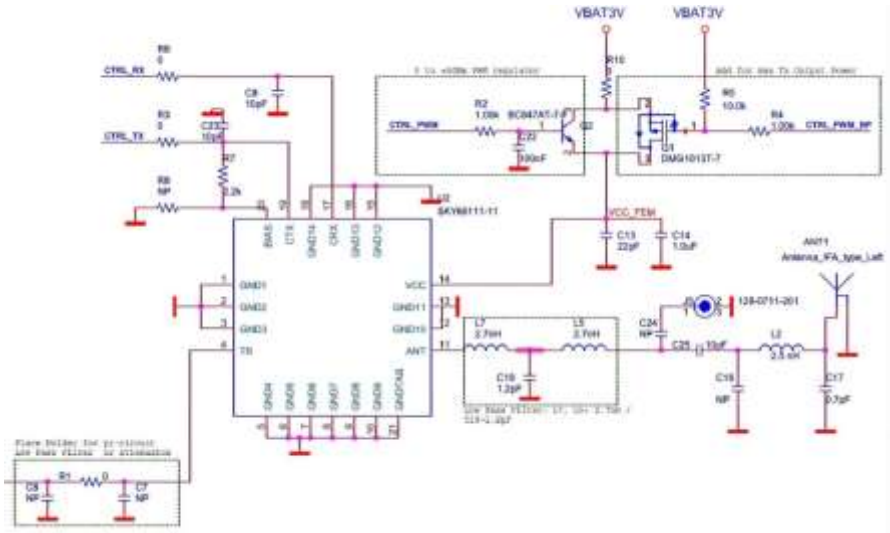


Figure 9: SKY66111-11 Front End Module - overview

7.2 Control Signals

7.2.1 RF Control Signals

The SKY66111-11 is controlled by CTX and CRX control signals. Their functionality is explained in Table 3.

Table 3: Truth Table for SKY66111-11

Mode	CTX	CRX	BIAS
Sleep mode	0	0	0
Receive (RX) mode	0	1	0
Transmit (TX) mode	1	0	1 (See Note 9)
Non- permissible state (See Note 10)	1	1	X

Note 9 Analog voltage control for PA output power.

Note 10 This state will enable both the TX and RX paths. It is not permitted to operate in this state.

These control signals are extracted by the DA14585 BLE diagnostic port, as they have to be synchronized with the radio on/ off of the DA14585 SoC.

In general, three different radio control signals can be extracted from DA14585 SoC:

- extrc_txen or radcntl_txen that can be used as TX_En control signal for the RF front end
- extrc_rxen or radcntl_rxen that can be used as RX_En control signals for the RF front end. Also extrc_txen inverted or radcntl_txen inverted can be used (See Note 11).
- event_in_process that can be used for wlan co-existence signal

Note 11 As long as BLE radio is active, FEM does not enter Sleep Mode.

The signals are extracted using the BLE diagnostic port. To do so, the following registers need to be programmed:

- BLE_DIAGCNTL_REG, BLE_DIAGCNTL2_REG where the diagnostic ports to be enabled are defined
- BLE_ DIAGCNTL3_REG where the desired control signals will be forwarded to the BLE diagnostic ports

BLE_DIAGCNTL_REG (0x40000050)

Bit	Mode	Type	Symbol	Description	Reset
31	r/w	reg_rw	DIAG3_EN	0: Disable diagnostic port 0 output. All outputs are set to 0x0. 1: Enable diagnostic port 0 output.	0x0
29:24	r/w	reg_rw	DIAG3	Only relevant when DIAG3_EN = 1. Selection of the outputs that must be driven to the diagnostic port BLE_DIAG3.	0x0
23	r/w	reg_rw	DIAG2_EN	0: Disable diagnostic port 0 output. All outputs are set to 0x0. 1: Enable diagnostic port 0 output.	0x0
21:16	r/w	reg_rw	DIAG2	Only relevant when DIAG2_EN = 1. Selection of the outputs that must be driven to the diagnostic port BLE_DIAG2.	0x0
15	r/w	reg_rw	DIAG1_EN	0: Disable diagnostic port 0 output. All outputs are set to 0x0. 1: Enable diagnostic port 0 output.	0x0
13:8	r/w	reg_rw	DIAG1	Only relevant when DIAG1_EN = 1. Selection of the outputs that must be driven to the diagnostic port BLE_DIAG1.	0x0
7	r/w	reg_rw	DIAG0_EN	0: Disable diagnostic port 0 output. All outputs are set to 0x0. 1: Enable diagnostic port 0 output.	0x0
5:0	r/w	reg_rw	DIAG0	Only relevant when DIAG0_EN = 1. Selection of the outputs that must be driven to the diagnostic port BLE_DIAG0.	0x0

Figure 10: BLE_DIAGCNTL_REG (0x40000050) register specification

BLE_DIAGCNTL2_REG (0x4000020C)

Bit	Mode	Type	Symbol	Description	Reset
31	r/w	reg_rw	DIAG7_EN	0: Disable diagnostic port 0 output. All outputs are set to 0x0. 1: Enable diagnostic port 0 output.	0x0
30	-	reg_ro	-	Reserved	0x0
29:24	r/w	reg_rw	DIAG7	Only relevant when DIAG7_EN = 1. Selection of the outputs that must be driven to the diagnostic port BLE_DIAG7.	0x0
23	r/w	reg_rw	DIAG6_EN	0: Disable diagnostic port 0 output. All outputs are set to 0x0. 1: Enable diagnostic port 0 output.	0x0
22	-	reg_ro	-	Reserved	0x0
21:16	r/w	reg_rw	DIAG6	Only relevant when DIAG6_EN = 1. Selection of the outputs that must be driven to the diagnostic port BLE_DIAG6.	0x0
15	r/w	reg_rw	DIAG5_EN	0: Disable diagnostic port 0 output. All outputs are set to 0x0. 1: Enable diagnostic port 0 output.	0x0
14	-	reg_ro	-	Reserved	0x0
13:8	r/w	reg_rw	DIAG5	Only relevant when DIAG5_EN= 1. Selection of the outputs that must be driven to the diagnostic port BLE_DIAG5.	0x0
7	r/w	reg_rw	DIAG4_EN	0: Disable diagnostic port 0 output. All outputs are set to 0x0. 1: Enable diagnostic port 0 output.	0x0
6	-	reg_ro	-	Reserved	0x0
5:0	r/w	reg_rw	DIAG4	Only relevant when DIAG4_EN = 1. Selection of the outputs that must be driven to the diagnostic port BLE_DIAG4.	0x0

Figure 11: BLE_DIAGCNTL2_REG (0x4000020C) register specification

BLE_DIAGCNTL3_REG (0x40000210)

Bit	Mode	Type	Symbol	Description	Reset
31	r/w	reg_rw	DIAG7_INV	If set, then the specific diagnostic bit will be inverted.	0x0
30:28	r/w	reg_rw	DIAG7_BIT	Selects which bit from the DIAG7 word will be forwarded to bit 7 of the BLE Diagnostic Port.	0x0
27	r/w	reg_rw	DIAG6_INV	If set, then the specific diagnostic bit will be inverted.	0x0
26:24	r/w	reg_rw	DIAG6_BIT	Selects which bit from the DIAG6 word will be forwarded to bit 6 of the BLE Diagnostic Port.	0x0
23	r/w	reg_rw	DIAG5_INV	If set, then the specific diagnostic bit will be inverted.	0x0
22:20	r/w	reg_rw	DIAG5_BIT	Selects which bit from the DIAG5 word will be forwarded to bit 5 of the BLE Diagnostic Port.	0x0
19	r/w	reg_rw	DIAG4_INV	If set, then the specific diagnostic bit will be inverted.	0x0
18:16	r/w	reg_rw	DIAG4_BIT	Selects which bit from the DIAG4 word will be forwarded to bit 4 of the BLE Diagnostic Port.	0x0
15	r/w	reg_rw	DIAG3_INV	If set, then the specific diagnostic bit will be inverted.	0x0
14:12	r/w	reg_rw	DIAG3_BIT	Selects which bit from the DIAG3 word will be forwarded to bit 3 of the BLE Diagnostic Port.	0x0
11	r/w	reg_rw	DIAG2_INV	If set, then the specific diagnostic bit will be inverted.	0x0
10:8	r/w	reg_rw	DIAG2_BIT	Selects which bit from the DIAG2 word will be forwarded to bit 2 of the BLE Diagnostic Port.	0x0
7	r/w	reg_rw	DIAG1_INV	If set, then the specific diagnostic bit will be inverted.	0x0
6:4	r/w	reg_rw	DIAG1_BIT	Selects which bit from the DIAG1 word will be forwarded to bit 1 of the BLE Diagnostic Port.	0x0
3	r/w	reg_rw	DIAG0_INV	If set, then the specific diagnostic bit will be inverted.	0x0
2:0	r/w	reg_rw	DIAG0_BIT	Selects which bit from the DIAG0 word will be forwarded to bit 0 of the BLE Diagnostic Port.	0x0

Figure 12: BLE_DIAGCNTL3_REG (0x40000210) register specification

BLE diagnostics can be used only with P 0[0:7] and P1 [0:3] of DA14585 SoC.

7.2.2 Power Control Signals

An external circuit is used for adjusting the voltage level of SKY66111-11 VCC power supply pin. By adjusting VCC the output power of the PA can be regulated.

In general, the system can be configured to operate in three different modes:

1. **Programmable Output Power Mode**: a PWM signal with programmable duty cycle is driving the external circuit. The system operates in the range of 0 to +8dBm defined by the duty cycle used.
2. **Maximum Output Power Mode**: the system operates at maximum power as defined by the RBIAS.
3. **Bypass Mode**: the PA is bypassed.

To configure modes 1 and 2, the following two control signals are used:

- CTRL_PWM: a PWM generated from DA14585 SoC with programmable duty cycle. Uses timer0.
- CTRL_PWM_BP: normal GPIO configured low or high

For the configuration of the Bypass mode CTX, CRX inverted signals are used (See Note 12).

The signal configuration for each of the modes described can be seen in Table 4.

Table 4: Power control Signals Configuration

Mode	CTRL_PWM	CTRL_PWM_BP	CTX	CRX
Programmable Output Power Mode	PWM	1	1	0
Maximum Power Mode	0	0	1	0
Bypass mode	Input pull-down	0	0 (See Note 12)	1 (See Note 12)

Note 12 CTX, CRX are configured as normal GPIO and not extracted from diagnostic port. CTX is configured LOW and CRX HIGH during transmission.

7.3 GPIO setup

A suggested pin assignment for extracting the necessary RF control signals (CTX, CRX) from the diagnostic port is described in Table 5.

In the current implementation the extrc_txen_inverted signal is used for controlling CRX. The implementation improves the receiver characteristics as the FEM remains active during BLE radio active time.

Table 5: Suggested pin assignment for extracting all RF control signals

Function	Signals used	Diagnostic port settings				DA14585 assigned pins
		BLE_DIAGCNTL_REG		BLE_DIAGCNTL3_REG		
		DIAG PORT	DIAG[x]	DIAG[x]_BIT	DIAG[x]_INV	
PA_TX Enable	Extrc_txen	DIAG1	0x28	3	0	P0_1
PA_RX Enable	Extrc_txen	DIAG2	0x28	3	1	P0_2
Wlan_coexist (See Note 13)	Event_in_process	DIAG3	0x03	4	0	P1_3

Note 13 Used for coexistence purposes, optional use for the RF controls

For the power control signals any two available GPIOs can be used. It is suggested though, for the PWM signal to use a GPIO that is not close to the RF output of the DA14585 SoC.

In the current system the GPIOs described in Table 6 are used.

Table 6: GPIO setup of FEM power control signals

Control Signals Name	GPIOs	Operation
CTRL_PWM	P2_1	PWM active
CTRL_PWM_BP	P2_7	Maximum power mode

7.4 Filtering

The low pass filter is placed after the amplifier matching network to suppress the harmonics generated due to the amplifier's nonlinearity. The filter presents low losses in the 2.4 GHz to 2.5 GHz frequency range (max. loss: 0.5 dB). The ripple on the pass band was chosen equal to 0.1dB.

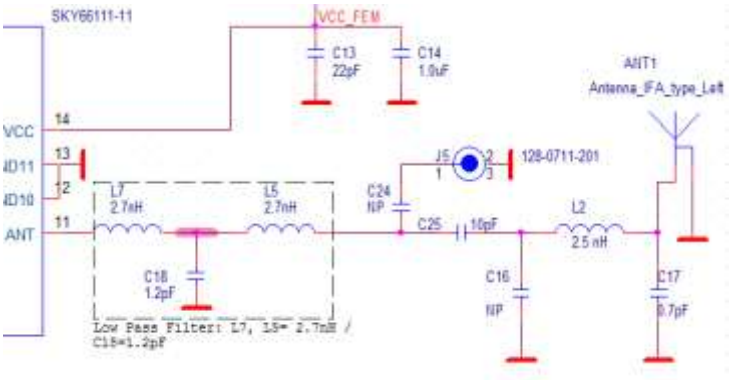


Figure 13: Low Pass Filter (L7&L5=2.7nH, C18=1.2pF)

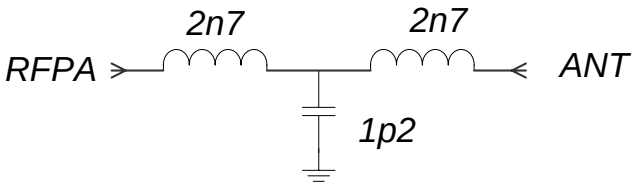


Figure 14: T-shaped, 3-poles, Low Pass Filter

The filter is a T- type Chebyshev 3rd order low pass filter. The filter configuration is presented in Figure 14.

Component value:

2.7nH: LQP15MN2N7B02D / Murata

1.2pF: GJM1555C1H1R2CB01D/ Murata

7.5 Antenna

DA14585 SoC provides a single ended RFIO port, matched to 50 Ohm. The RF port consists of RFIOp and RFIOm pins, where RFIOm is connected to ground. A copper trace with impedance of 50 Ohm interconnects the RF port and the RFIN of SKY66111-11.

SKY66111-11 provides one antenna output. At this port a printed Inverted F Antenna (IFA) is used.

Figure 15: Printed Inverted F Antenna geometry

A Pi-network composed of C16, L2 and C17 is available for matching purposes. For the current design the matching components values for optimum power transfer are: C17= 0.7pF and L2=2.5nH.

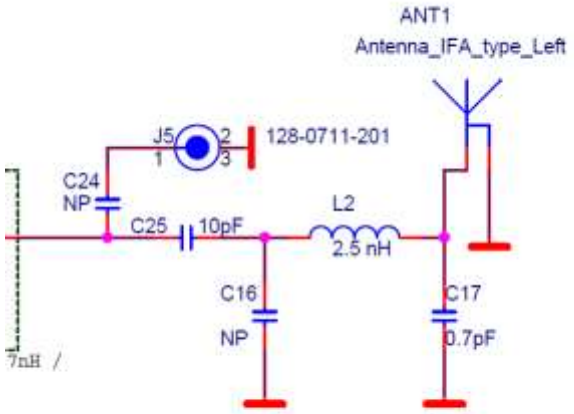


Figure 16: Matching network for printed antenna

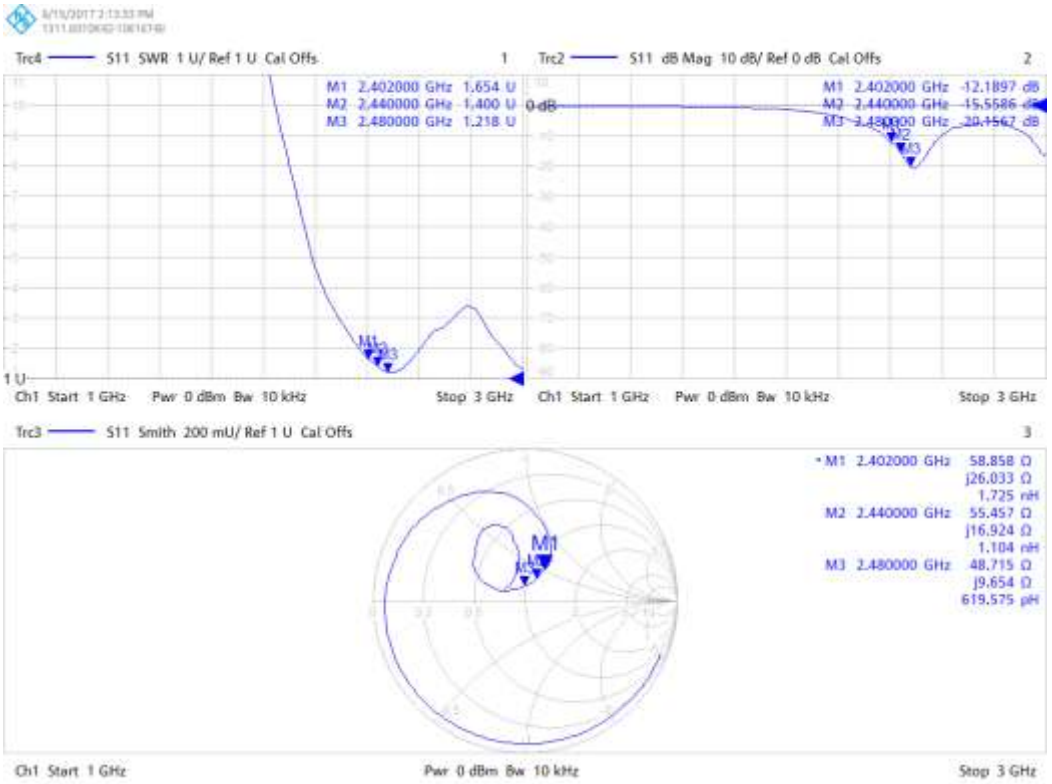


Figure 17: S parameters of Printed IFA and Matching Network

Antenna Gain measurements were performed in an anechoic chamber. The maximum gain was measured at 2.1 dBi.

Table 7: Antenna gain

Parameter	G(dBi)
Maximum gain	2.1

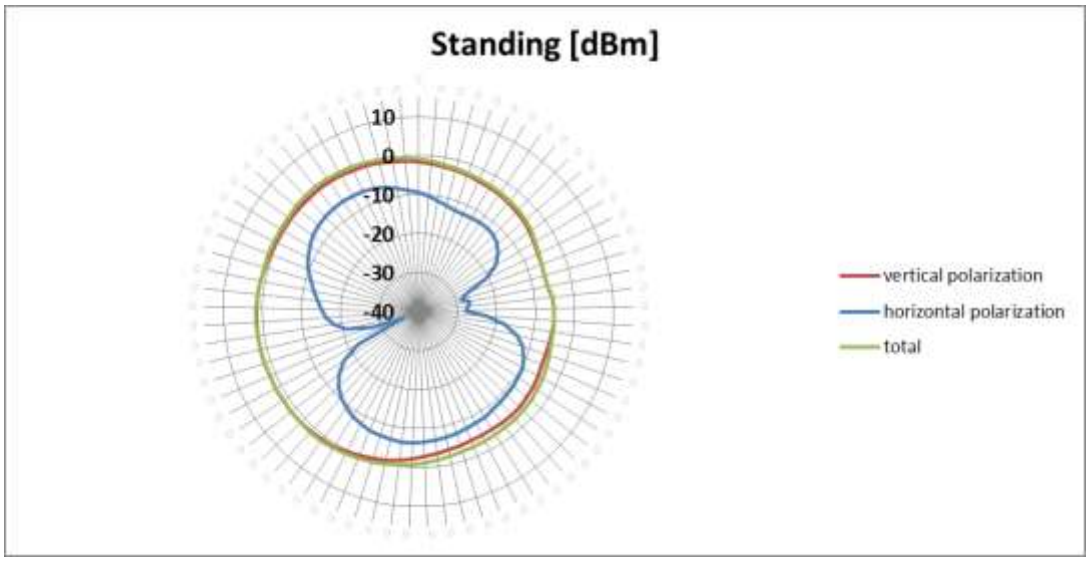


Figure 18: Radiation diagram for the board placed vertically

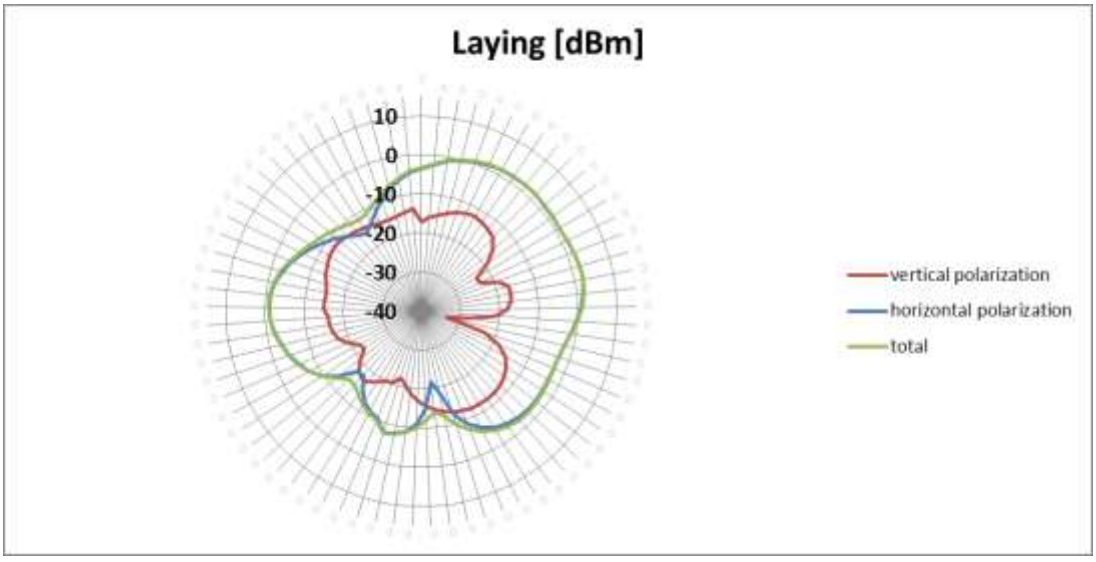


Figure 19: Radiation diagram for the board placed horizontally

7.6 Resistive attenuator (optional)

Between DA14585 SoC and SKY66111-11 a resistive attenuator circuit can be added if needed. Components of C7, C8 and R1 must then be replaced by suitable resistors to achieve the desired attenuation, while matching the 50 impedance. In the present design no extra attenuation was used at the input of the PA.

8 TX Output Power Control Circuit

By modifying the voltage level of VCC pin for a fixed VBIAS level, the TX output power of SKY66111-11 can change as shown in Figure 20 (see Ref. [2]). In the current design VBIAS=1.8V.

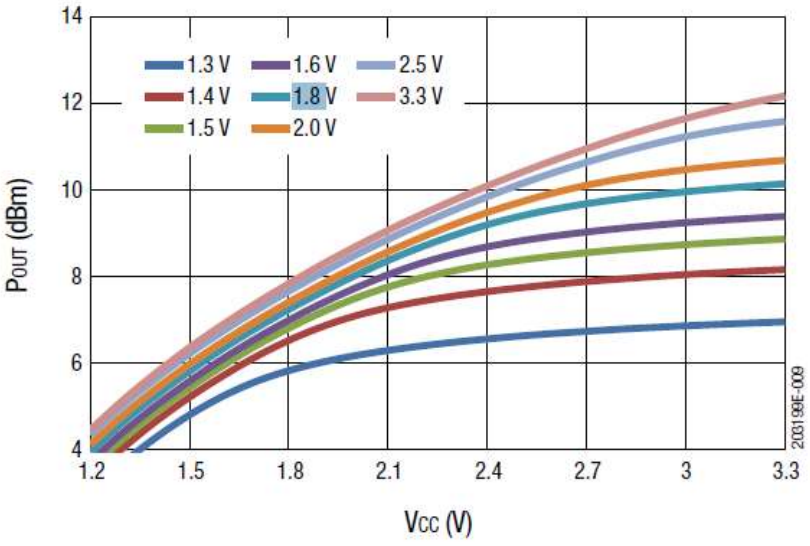


Figure 20: SKY66111-11 P_{OUT} vs VCC & V_{BIAS} (P_{IN}=-1dBm)

In order to achieve a configurable TX output power, an external circuit consisting of NPN transistor (Q2) and a p-FET (Q1) is used to control the power supply level of SKY66111-11. A PWM signal, CTRL_PWM, generated by the DA14585 SoC at frequency of 160 kHz, is filtered by R2/C22. The filtered voltage drives Q2 NPN transistor which produces VCC up to 2.2V for the SKY66111-11 based on the PWM duty cycle. The power regulation to be achieved is from 0 to +8 dBm in steps of 2dB.

CTRL_PWM_BP control signal is used to control the operation of Q1 p-FET and configure VCC to maximum level of 3.0V for maximum power operation.

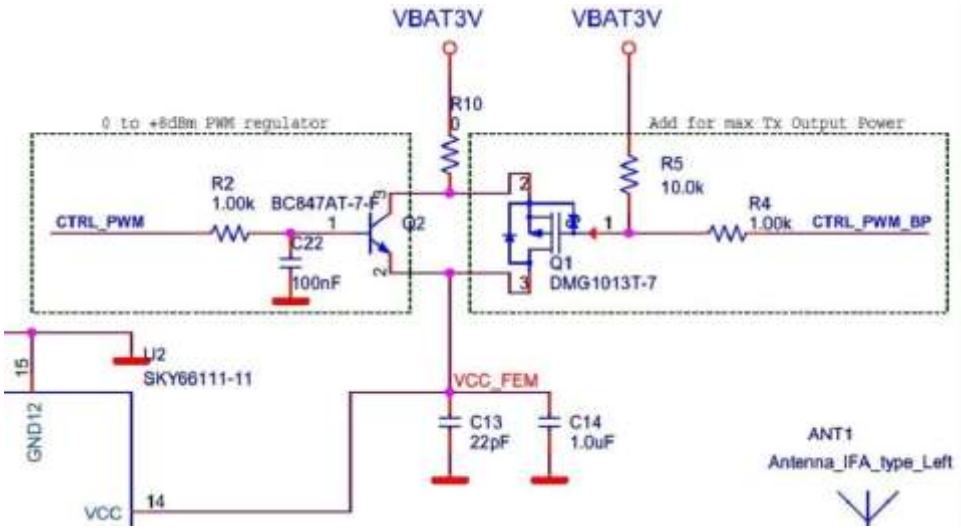


Figure 21: Power regulation circuit

Using the two control signals described above, allows the SKY66111-11 to be operated in two different modes:

- **Maximum Output Power Mode**: +9.3dBm
- **Programmable Output Power Mode**: 0 to +8dBm

An extra mode, of bypassing the SKY66111-11, is also possible by configuring CTX, CRX signals.

- Bypass Power Mode: where the PA is bypassed

For more details please see section 7.2.2.

As far as the PWM operation, the TX output power versus duty cycle at normal temperature was measured. The results can be seen in Figure 22.

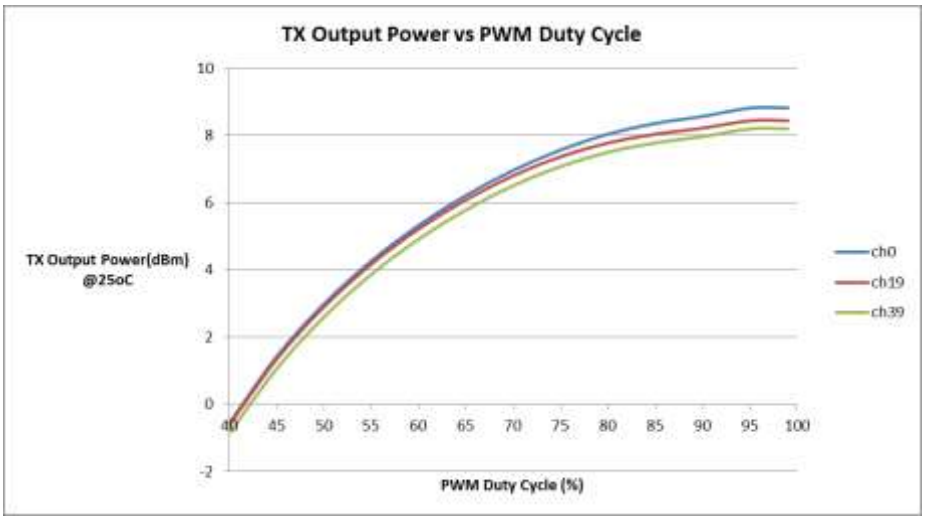


Figure 22: TX Output Power using PWM mode, 3 channels

The duty cycle values used to get power steps of 2dBm from 0 to +8dBm using the PWM can be seen in Table 8. In the same table the typical values of the TX output power for each power level as well as accuracy are also included.

Maximum power and bypass operation mode values can also be seen in the same Table (Table 8).

For more on power distribution tendency over channels please see Section 13.1.2.

Table 8: SKY66111-11 TX Output Power Typical values and Accuracy over PWM Duty Cycle (Note 14)

Power Mode	PWM Operation	Duty Cycle (%)	TYPICAL VALUE (dBm)	Accuracy (dB)
BYPASS	No	-	-1.65	±0.2
ZERO_DBM	Yes	42	-0.02	±0.4
TWO_DBM	Yes	48	2.07	±0.4
FOUR_DBM	Yes	55	3.94	±0.4
SIX_DBM	Yes	65	5.9	±0.3
EIGHT_DBM	Yes	82	7.88	±0.2
MAX_POWER	No	-	8.89	±0.2

Note 14 The typical values listed in the table represent statistic average values across all 40 channels. Bursts of 10 packets, packet length 37 and the pattern were “01010101”.

The utilized duty cycle is from 40% and above resulting in powers in the range of 0 to +8dBm and VCC voltages in the range of 0.6 to 1.8V.

In Figure 23 the TX output power dependence and VCC voltage level changes over PWM duty cycle can be seen.

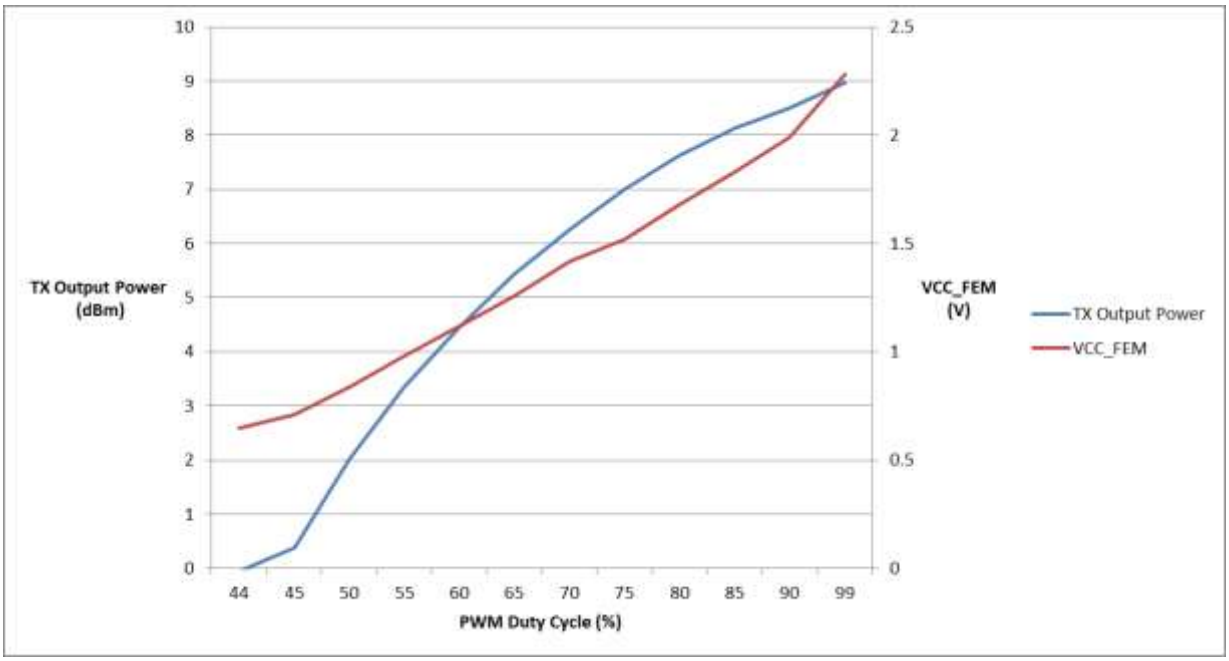


Figure 23: PWM Duty Cycle vs TX Output Power and VCC

In Table 9 the changes in VCC of SKY66111-11 for all power steps can be found.

Table 9: SKY66111-11 VCC voltage level for all power modes

Power Mode	VCC (Volts)	VBIAS (Volts)
BYPASS	3.0	0
ZERO_DBM	0.6	1.8
TWO_DBM	0.8	1.8
FOUR_DBM	1.0	1.8
SIX_DBM	1.4	1.8
EIGHT_DBM	1.8	1.8
MAX_POWER	3.0	1.8

9 Crystals

DA14585 SoC has two crystal oscillators, one at 16 MHz (XTAL16M) and a second at 32.768 kHz (XTAL32K). The 32.768 kHz oscillator has no trimming capabilities and is used as the clock of the Extended Sleep mode. The 16 MHz oscillator can be trimmed.

For ensuring best operation of the DA14585 Range Extender, the 16MHz XTAL must be trimmed. The frequency is trimmed by two on-chip variable capacitor banks. Both capacitor banks are controlled by the same register.

For trimming the XTAL apply procedure described on AN-B-020: End product testing and programming guidelines (see Ref.[5]).

The crystals used are specified in Table 10 and Table 11.

Table 10: Y1 16 MHz Crystal Characteristics

Reference Designator	Value
Part Number	7M-16.000MEEQ-T
Frequency	16 MHz
Accuracy	±10 ppm
Load Capacitance (C_L)	10 pF
Shunt Capacitance (C_0)	3 pF
Equivalent Series Resistance (ESR)	100 Ω
Drive Level (P_D)	50 μW

Table 11: Y2 32 kHz Crystal Characteristics

Reference Designator	Value
Part Number	9HT11-32.768KDZB-T
Frequency	32.768 kHz
Accuracy	±20 ppm
Load Capacitance (C_L)	6 pF
Shunt Capacitance (C_0)	1.3pF
Equivalent Series Resistance (ESR)	90 kΩ
Drive Level (P_D)	0.5 μW

10 Reference Design Pin Assignment

The pin assignment for the DA14585 Range Extender is shown in Table 12.

Table 12: DA14585 aQFN40 Pin Assignment

GPIO Name	aQFN40 Function	Range Extender Function	Comments
P0_0	GPIO	Not assigned	
P0_1	GPIO	CTRL_TX	FEM CTX control signal
P0_2	GPIO	CTRL_RX	FEM CRX control signal
P0_3	GPIO	Not assigned	
P0_4	GPIO	Not assigned	
P0_5	GPIO	Not assigned	
P0_6	GPIO	Not assigned	
P0_7	GPIO	Not assigned	
P1_0	GPIO	Not assigned	
P1_1	GPIO	Not assigned	
P1_2	GPIO	Not assigned	
P1_3	GPIO	Not assigned	
P2_0	GPIO	Not assigned	
P2_1	GPIO	CTRL_PWM	Programmable Output Power control signal
P2_2	GPIO	Not assigned	
P2_3	GPIO	Not assigned	
P2_4	GPIO	Not assigned	
P2_5	GPIO	Not assigned	
P2_6	GPIO	Not assigned	
P2_7	GPIO	CTRL_PWM_BP	Maximum Power operation control signal
P2_8	GPIO	Not assigned	
P2_9	GPIO	Not assigned	
P3_0	GPIO	Not assigned	
-	SWDIO	SWDIO	
-	SW_CLK	SW_CLK	
-	XTAL16Mp	XTAL16Mp	
-	XTAL16Mm	XTAL16Mm	
-	XTAL32kp	XTAL32kp	
-	XTAL32km	XTAL32km	
-	RST	RST	

11 Development mode - Peripheral Pin Mapping

On the following table the pins used for development/ testing are described.

Table 13: Development/ testing mode pin mapping

SoC Pin #	DA14585 assigned Pins	Function	SoC Pin #	DA14585 assigned Pins	Function
1	P0_0	Available External Use	21	SWITCH	Connection for the external DCDC-converter inductor.
2	P0_1	FEM Tx Enable	22	P1_0	Available External Use
3	P0_2	FEM Rx Enable	23	VBAT1V	
4	P0_3	Available External Use	24	P1_1	Available External Use
5	P3_0	Available External Use	25	SWDIO	SWDIO
6	P0_4	UART TX	26	SW_CLK	SWCLK
7	P0_5	UART RX	27	P1_2	Available External Use
8	P2_1	FEM Power Control Signal - PWM	28	P1_3	Wlan_coexistence (optional)/ Available External Use
9	P0_6	Available External Use	29	XTAL16Mp	
10	P0_7	Available External Use	30	XTAL16Mm	
11	XTAL32Km		31	VDCDC_RF	
12	XTAL32Kp		32	P2_5	Available External Use
13	P2_2	Available External Use	33	P2_6	Available External Use
14	VBATA		34	RFIOm	
15	VBAT3V		35	RFIOp	
16	GND		36	P2_7	FEM Power Control Signal- Max Power
17	RST	RESET	37	P2_8	Available External Use
18	P2_3	Available External Use	38	VDD	
19	VDCDC		39	P2_9	Available External Use
20	P2_4	Available External Use	40	P2_0	Available External Use
*Note: For interfacing external SPI data Flash. See chapter 4.4.3 BootROM Sequence of DA14585_datasheet (See Ref.[3])					

12 PCB Assembly

A 2-layer FR4 PCB with 1.6mm standard thickness is used. The PCB size is 34x42mm and follows the 58x daughterboard form factor. All available GPIOs are accessible via the card edge connector (PCI-E). Schematic and BOM are presented in the following sections.

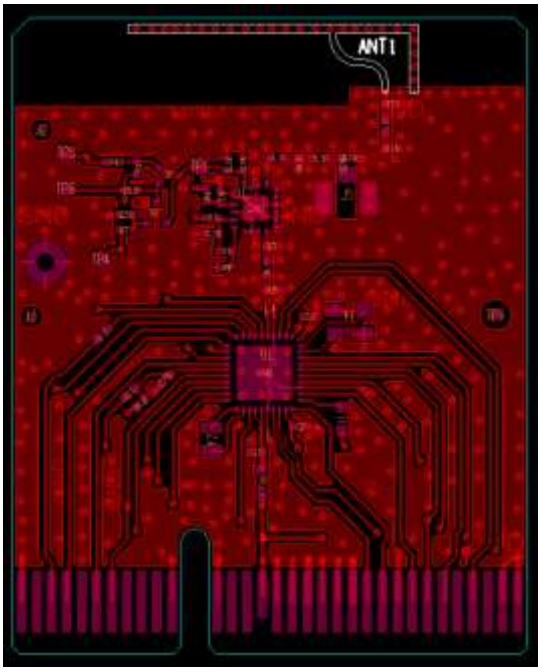


Figure 24: Top view of PCBA

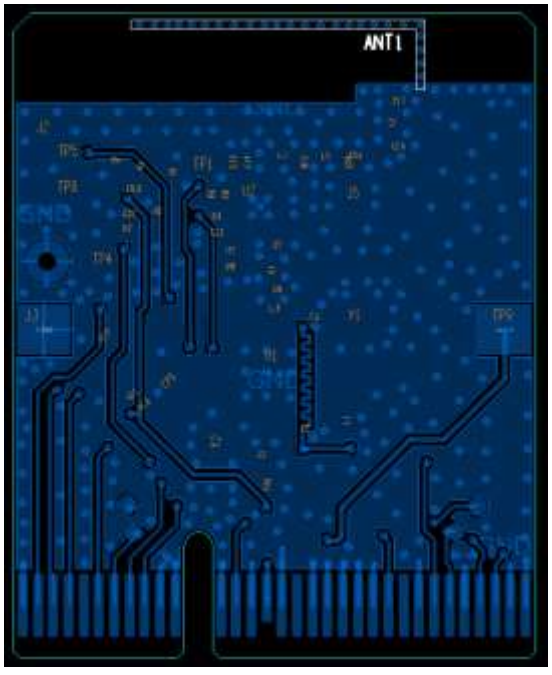
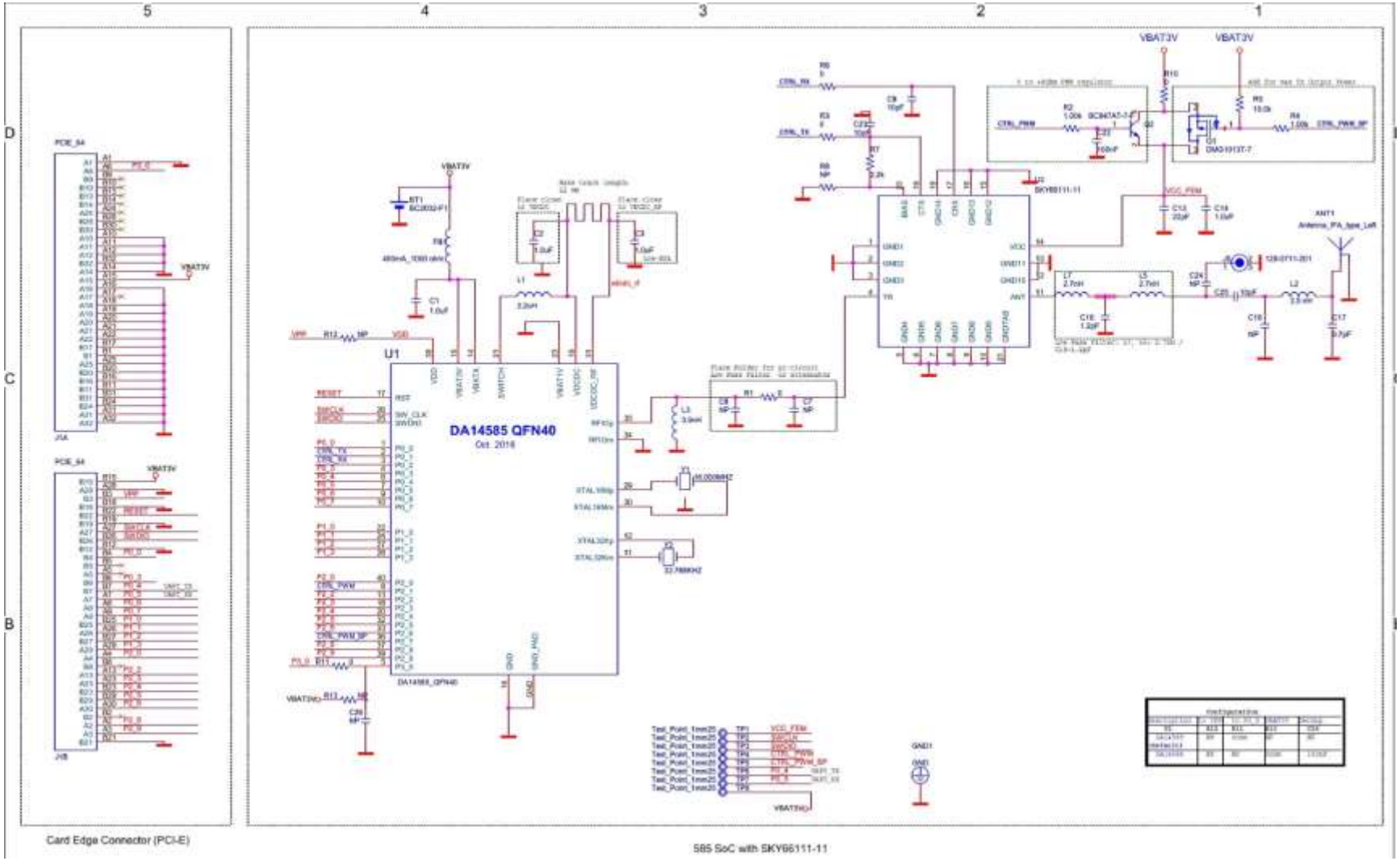


Figure 25: Bottom view of PCBA

12.1 DA14585 Range Extender Schematic



12.2 Bill of Materials

Table 14: Bill of Materials

Ref.	Value	Description	Manuf.	MPN	Footprint
C1 C2 C3 C14	1.0uF	CAP CER 1UF 10V X5R 20% 0402 -RoHS	Murata	GRM155R61A105ME15D	C1005
C9 C23 C25	10pF	CAP CER 10PF 50V 2% NP0 0402	Murata	GRM1555C1H100GA01D	Z1005
C13	22pF	CAP CER 22PF 50V C0G 0402 -RoHS	Murata	GRM1555C1H220JA01J	C1005
C17	0.7pF	CAP CERAMIC 0.7pF 50volts C0G +/-0.1pF 0402 -RoHS	Murata	GJM1555C1HR70BB01D	C1005
C18	1.2pF	CAP CERAMIC 1.2PF 50V C0G 0402 -RoHS	Murata	GJM1555C1H1R2CB01D	C1005
C22	100nF	CAP CER .1UF 16V X7R 0402	Murata	GRM155R71C104KA88D	C1005
R1 R3 R6 R10 R11	0	RES 0.0 OHM 1/16W 0402 - RoHS	Vishay	CRCW04020000Z0ED	R1005
R2 R4	1.00k	RES 1.0 Kohm 1/16W 5% 0402 -RoHS	Vishay	CRCW04021K00JNED	R1005
R5	10.0k	RES 10.0 Kohm 1/16W 1% 0402 -RoHS	Vishay/ Dale	CRCW040210K0FKED	R1005
R7	2.2k	RES 2.2 Kohm 1/16watt 1% 50V 0402 -RoHS	Vishay/ Dale	CRCW04022K20FKED	R1005
L1	2.2uH	INDUCTOR Power 2.2uH, 500mA, 400MHz (0603)	Taiyo Yuden	BRL1608T2R2M	L1608
L2	2.5nH	INDUCTOR RF 2.5nH ±0.05nH 220mA DCr:0.3 ohm (0402)	Murata Electronics	LQP15MN2N5W02D	L1005
L3	3.9nH	CHIP INDUCTOR 3.9nH, 400mA 300 mOhm Max 0201 (0603 Metric)	Murata Electronics	81-LQP03TN3N9C02D	L0603mm
L5 L7	2.7nH	INDUCTOR RF 2.7nH ±0.1nH 220MA DCr:0.30ohm (0402)	Murata Electronics	LQP15MN2N7B02D	L1005_L
FB1	400mA_1000 ohm	EMI FB General Lines 1 Kohm±25% 400mA DCr:0.50 ohm (0603)	Murata Electronics	BLM18AG102SN1D	L1608
Q1	DMG1013T-7	MOSFET P-Channel 20V 0.46A SOT-523	Diodes Inc.	DMG1013T-7	SOT50P160X90-3N
Q2	BC847AT-7-F	TRANS NPN 45V 0.1A SOT-523-3 -RoHS	Diodes Inc.	BC847AT-7-F	SOT523
U1	DA14585_QFN40	IC BLE RF 4.2 SoC with Audio Interface qfn40 5X5mm	Dialog Semiconductor	DA14585-00000AT2	QFN40P500X500X90-41L

Ref.	Value	Description	Manuf.	MPN	Footprint
U2	SKY66111-11	IC Low-Power Bluetooth Low Energy Front-End Module, Output: +10 dBm	Skyworks Solutions, Inc.	SKY66111-11	RF_SKY66111-11
J5	128-0711-201	RF Connectors / UMC RCPT STR 50 OHM SMD	Johnson	128-0711-201	RF_128-0711-201
Y1	16.000MHZ	CRYSTAL 16.000MHZ 10PF SMT	TXC	7M-16.000MEEQ-T	xtal3200x2500x70

13 BLE Measurements

13.1 Basic Performance Measurements

All measurements reported here use the following parameters:

Operating Conditions:

- T = 25 °C
- VBAT = 3 V

Equipment:

- Signal analyzer: Rohde & Schwarz FSV Spectrum analyzer
- R&S CBT - CBT go PC testing software
- Agilent N6705B DC power analyzer – Keysight 14585A Control and Analysis Software

Tools:

- SmartSnippets Toolbox v5.0.0.1808
- SmartSnippets Studio v2.0.0.952

Test Procedure:

- Continuous packet transmission mode was used for R&S CBT measurements.
- For current measurements proximity reporter application was used. The current was measured during advertisement, connection and sleep intervals.

Test Configuration:

Tests were performed for all power levels.

Measurements:

- Receiver sensitivity (section 13.1.1)
- Transmitter output power (section 13.1.2)
- Current consumption (section 13.1.3)

13.1.1 Receiver Sensitivity

13.1.1.1 Test Description

For this test the BLE RX sensitivity of DA14585 Range Extender (321-13-B) was measured.

13.1.1.2 Test Setup

The DA14585 Range Extender was mounted on a PRO-motherboard. The R&S® CBT Bluetooth® Tester from Rohde & Schwarz was used. An RF cable assembly was connected from J5 RF connector (through an attenuator) to the R&S CBT Bluetooth Tester. In order to evaluate the RF sensitivity, `prod_test` firmware was used. The results from the measurement are reported below.

The RX tests were performed using payload length: 37 bytes.

13.1.1.3 Test Results

The conducted RF sensitivity with dirty transmitter disabled shows that the sensitivity is better than -92 dBm for all channels (except known channels) for maximum payload of 37 bytes (See Note 15).

The conducted RF sensitivity with dirty transmitter enabled shows that the sensitivity is better than -91 dBm for all channels (except known channels) for maximum payload of 37 bytes (See Note 15).

Note 15 Channels 7, 15, 23, 31 and 39 are susceptible to system harmonics and may present degraded sensitivity.

Table 15: RX Sensitivity for all power levels, Dirty Transmitter OFF (Note 16)

	RX Sensitivity (dBm)		
Power Level (dBm)	**Channel 0**	**Channel 19**	**Channel 39**
BYPASS	-93.2	-92.8	-92.4
0	-93	-93	-92.4
+2	-93	-92.9	-92.4
+4	-93.10	-93	-92.5
+6	-93	-92.9	-92.4
+8	-93.10	-92.9	-92.3
+9.3	-93	-93	-92.4

Note 16 Packets 1500, Payload: PRBS 9, Length: 37, Dirty Transmitter Off.

Table 16: RX Sensitivity for all power levels, Dirty Transmitter ON (Note 17)

	RX Sensitivity (dBm)		
Power Level (dBm)	**Channel 0**	**Channel 19**	**Channel 39**
BYPASS	-92.10	-92	-91.3
0	-92.1	-91.9	-91.2
+2	-92	-91.9	-91.5
+4	-92.2	-91.9	-91.4
+6	-92.2	-92.1	-91.5
+8	-92.2	-92	-91.5
+9.3	-92	-91.8	-91.3

Note 17 Packets 1500, Payload: PRBS 9, Length: 37, Dirty Transmitter On.

Test Name and Condition	Lower Limit	Upper Limit	Measured Value	P/F
RX Level @ *Ch: 00, PER: 29.20%, Count: 09*			-93.00 dBm	✓
RX Level @ *Ch: 01, PER: 30.73%, Count: 05*			-93.00 dBm	✓
RX Level @ *Ch: 02, PER: 31.53%, Count: 05*			-93.00 dBm	✓
RX Level @ *Ch: 03, PER: 29.33%, Count: 09*			-92.90 dBm	✓
RX Level @ *Ch: 04, PER: 28.87%, Count: 04*			-92.80 dBm	✓
RX Level @ *Ch: 05, PER: 31.20%, Count: 17*			-93.00 dBm	✓
RX Level @ *Ch: 06, PER: 31.33%, Count: 09*			-92.90 dBm	✓
RX Level @ *Ch: 07, PER: 32.67%, Count: 15*			-92.60 dBm	✓
RX Level @ *Ch: 08, PER: 31.07%, Count: 12*			-92.80 dBm	✓
RX Level @ *Ch: 09, PER: 31.60%, Count: 05*			-93.00 dBm	✓
RX Level @ *Ch: 10, PER: 31.67%, Count: 04*			-92.80 dBm	✓
RX Level @ *Ch: 11, PER: 29.93%, Count: 11*			-92.80 dBm	✓
RX Level @ *Ch: 12, PER: 31.27%, Count: 04*			-92.80 dBm	✓
RX Level @ *Ch: 13, PER: 32.80%, Count: 08*			-93.00 dBm	✓
RX Level @ *Ch: 14, PER: 31.00%, Count: 09*			-92.80 dBm	✓
RX Level @ *Ch: 15, PER: 32.07%, Count: 09*			-89.50 dBm	✓
RX Level @ *Ch: 16, PER: 32.47%, Count: 08*			-93.00 dBm	✓
RX Level @ *Ch: 17, PER: 30.27%, Count: 09*			-92.90 dBm	✓
RX Level @ *Ch: 18, PER: 30.20%, Count: 16*			-92.80 dBm	✓
RX Level @ *Ch: 19, PER: 32.20%, Count: 05*			-93.00 dBm	✓
RX Level @ *Ch: 20, PER: 29.87%, Count: 04*			-92.80 dBm	✓
RX Level @ *Ch: 21, PER: 29.93%, Count: 09*			-92.90 dBm	✓
RX Level @ *Ch: 22, PER: 29.40%, Count: 12*			-92.70 dBm	✓
RX Level @ *Ch: 23, PER: 29.53%, Count: 11*			-92.50 dBm	✓
RX Level @ *Ch: 24, PER: 32.07%, Count: 06*			-92.90 dBm	✓
RX Level @ *Ch: 25, PER: 31.67%, Count: 09*			-92.80 dBm	✓
RX Level @ *Ch: 26, PER: 29.40%, Count: 11*			-92.70 dBm	✓
RX Level @ *Ch: 27, PER: 32.47%, Count: 09*			-92.80 dBm	✓
RX Level @ *Ch: 28, PER: 30.07%, Count: 17*			-92.80 dBm	✓
RX Level @ *Ch: 29, PER: 29.87%, Count: 12*			-92.80 dBm	✓
RX Level @ *Ch: 30, PER: 29.53%, Count: 08*			-92.60 dBm	✓
RX Level @ *Ch: 31, PER: 31.40%, Count: 11*			-89.50 dBm	✓
RX Level @ *Ch: 32, PER: 29.87%, Count: 05*			-92.60 dBm	✓
RX Level @ *Ch: 33, PER: 29.93%, Count: 09*			-92.70 dBm	✓
RX Level @ *Ch: 34, PER: 29.00%, Count: 05*			-92.60 dBm	✓
RX Level @ *Ch: 35, PER: 29.53%, Count: 05*			-92.60 dBm	✓
RX Level @ *Ch: 36, PER: 31.80%, Count: 09*			-92.70 dBm	✓
RX Level @ *Ch: 37, PER: 28.87%, Count: 05*			-92.60 dBm	✓
RX Level @ *Ch: 38, PER: 31.80%, Count: 05*			-92.60 dBm	✓
RX Level @ *Ch: 39, PER: 30.80%, Count: 07*			-92.40 dBm	✓
Avg. Step Count @ *40 tests with totally 342 steps*			8.55	

Figure 26: RX Sensitivity, Dirty Transmitter OFF, Payload: PRBS9, Length: 37, MAX_POWER

Test Name and Condition	Lower Limit	Upper Limit	Measured Value	P/F
RX Level @ *Ch: 00, PER: 30.13%, Count: 10*			-92.00 dBm	✓
RX Level @ *Ch: 01, PER: 29.60%, Count: 12*			-92.10 dBm	✓
RX Level @ *Ch: 02, PER: 30.40%, Count: 06*			-92.00 dBm	✓
RX Level @ *Ch: 03, PER: 31.67%, Count: 06*			-92.00 dBm	✓
RX Level @ *Ch: 04, PER: 31.20%, Count: 07*			-92.20 dBm	✓
RX Level @ *Ch: 05, PER: 28.93%, Count: 11*			-92.00 dBm	✓
RX Level @ *Ch: 06, PER: 29.40%, Count: 08*			-91.80 dBm	✓
RX Level @ *Ch: 07, PER: 31.07%, Count: 07*			-91.50 dBm	✓
RX Level @ *Ch: 08, PER: 28.87%, Count: 10*			-91.80 dBm	✓
RX Level @ *Ch: 09, PER: 30.33%, Count: 06*			-92.00 dBm	✓
RX Level @ *Ch: 10, PER: 29.53%, Count: 09*			-91.70 dBm	✓
RX Level @ *Ch: 11, PER: 28.80%, Count: 08*			-91.60 dBm	✓
RX Level @ *Ch: 12, PER: 29.73%, Count: 11*			-91.90 dBm	✓
RX Level @ *Ch: 13, PER: 30.60%, Count: 10*			-91.80 dBm	✓
RX Level @ *Ch: 14, PER: 29.87%, Count: 09*			-91.90 dBm	✓
RX Level @ *Ch: 15, PER: 32.27%, Count: 10*			-87.40 dBm	✓
RX Level @ *Ch: 16, PER: 31.20%, Count: 09*			-92.10 dBm	✓
RX Level @ *Ch: 17, PER: 30.87%, Count: 11*			-92.00 dBm	✓
RX Level @ *Ch: 18, PER: 30.47%, Count: 10*			-92.10 dBm	✓
RX Level @ *Ch: 19, PER: 28.87%, Count: 11*			-91.80 dBm	✓
RX Level @ *Ch: 20, PER: 29.27%, Count: 09*			-91.90 dBm	✓
RX Level @ *Ch: 21, PER: 28.87%, Count: 09*			-91.90 dBm	✓
RX Level @ *Ch: 22, PER: 30.80%, Count: 10*			-91.80 dBm	✓
RX Level @ *Ch: 23, PER: 28.87%, Count: 06*			-91.40 dBm	✓
RX Level @ *Ch: 24, PER: 30.80%, Count: 11*			-91.80 dBm	✓
RX Level @ *Ch: 25, PER: 29.20%, Count: 10*			-91.90 dBm	✓
RX Level @ *Ch: 26, PER: 29.13%, Count: 08*			-91.80 dBm	✓
RX Level @ *Ch: 27, PER: 31.53%, Count: 08*			-91.80 dBm	✓
RX Level @ *Ch: 28, PER: 31.13%, Count: 10*			-91.80 dBm	✓
RX Level @ *Ch: 29, PER: 31.60%, Count: 06*			-92.00 dBm	✓
RX Level @ *Ch: 30, PER: 29.27%, Count: 09*			-91.60 dBm	✓
RX Level @ *Ch: 31, PER: 31.80%, Count: 08*			-87.60 dBm	✓
RX Level @ *Ch: 32, PER: 30.47%, Count: 08*			-91.80 dBm	✓
RX Level @ *Ch: 33, PER: 32.07%, Count: 08*			-91.80 dBm	✓
RX Level @ *Ch: 34, PER: 31.00%, Count: 10*			-91.70 dBm	✓
RX Level @ *Ch: 35, PER: 29.73%, Count: 08*			-91.60 dBm	✓
RX Level @ *Ch: 36, PER: 29.20%, Count: 08*			-91.60 dBm	✓
RX Level @ *Ch: 37, PER: 31.20%, Count: 09*			-91.60 dBm	✓
RX Level @ *Ch: 38, PER: 31.87%, Count: 08*			-91.60 dBm	✓
RX Level @ *Ch: 39, PER: 29.80%, Count: 12*			-91.30 dBm	✓
Avg. Step Count @ *40 tests with totally 356 steps*			8.90	

Figure 27: RX Sensitivity, Dirty Transmitter, Payload: PRBS9, Length: 37, MAX_POWER

13.1.2 Transmitter Output Power

13.1.2.1 Test Description

In this test the Nominal Average TX output power (conducted) of DA14585 Range Extender was measured.

13.1.2.2 Test Setup

The DA14585 Range Extender was mounted on a PRO-motherboard. In order to evaluate the TX output power, `prod_test` firmware was used. Conducted transmitted output power was measured by using the R&S® CBT Bluetooth® Tester. An RF cable assembly was connected from J5 RF connector (through an attenuator) to the R&S CBT Bluetooth Tester.

- Bursts of 10 packets were transmitted by the DA14585.
- The packet length was 37 and the pattern was “01010101”.
- Three channels were recorded: channels 0, 19 and 39.

13.1.2.3 Test Results

Measurements were performed on a number of samples for all power levels.

Table 17: Nominal Average TX Power (Note 18)

	Nominal Average TX Power (dBm)			Accuracy (dBm)
Power Level (dBm)	**Channel 0**	**Channel 19**	**Channel 39**	
BYPASS	-1.4	-1.65	-1.7	±0.2
0	0.05	0.06	-0.1	±0.2
+2	2.16	2.15	1.97	±0.2
+4	4	4	3.8	±0.2
+6	6	5.9	5.7	±0.2
+8	8.12	7.88	7.68	±0.2
MAX_POWER	+9.31	+8.91	+8.7	±0.2

Note 18 Bursts: 10, Payload: PRBS 9, Length: 37.

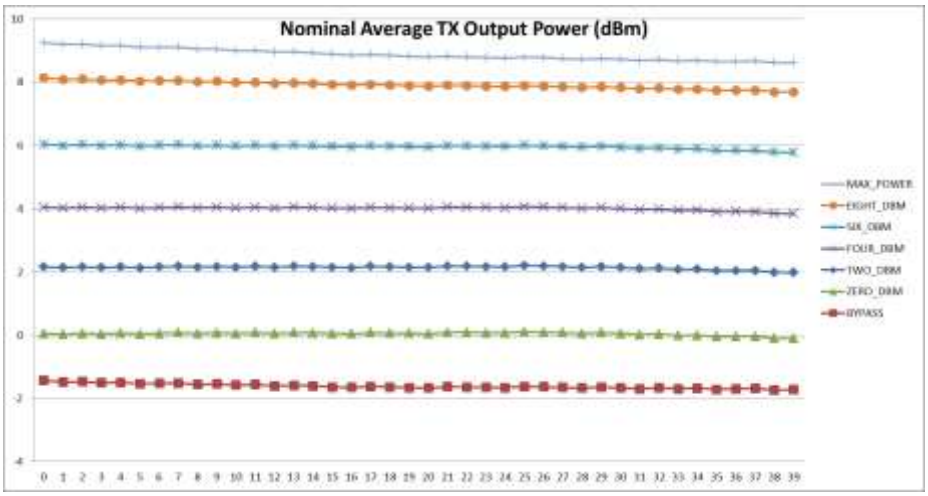


Figure 28: Nominal Average TX Output Power per channel vs all power levels

13.1.3 Current Consumption

13.1.3.1 Test Description

In this test the current consumption of DA14585 Range Extender during advertising, connection and sleep was measured for all power levels. The power consumption presented in this chapter is not optimized for the PWM mode. For PWM optimizations please refer to Appendix B.

13.1.3.2 Test Setup

The board used in the test presented optimal RF performance. The integrated printed antenna was used to perform the measurements.

The following instruments were used for the test:

- 3 V, 400 mA power source
- Agilent N6705B DC Power Analyzer
- Thermostreamer

The current profiles were evaluated using proximity reporter demo firmware with embedded PA control. During this test the Advertising, Connection and Extended Sleep modes were evaluated.

A two minutes capture was taken using Agilent Power Analyzer for each power mode.

Results from all power levels are presented in Table 18, Table 19 and Table 20.

13.1.3.3 Test Results

Advertising Mode

For this measurement the DUT was supplied by 3 V. FW was downloaded using JTAG programmer and then it was disconnected from the motherboard.

Table 18: Current consumption during Advertising Mode (Note 19)

Power Level (dBm)	Average charge per active state per interval (uC)	Average current for capture (uA)	Peak current (mA)	Peak power (uW)
BYPASS	12.59	10.86	5.61	0.02
0	21.30	16.70	10.05	0.03
+2	24.53	18.87	10.90	0.03
+4	25.75	19.64	11.86	0.04
+6	24.37	19.20	13.27	0.04
+8	26.03	19.82	14.29	0.04
+9.3	23.23	18.40	15.43	0.05

Note 19 Power supply= 3V, T=25ºC, advertising interval=1500ms, adv_pdu=9 bytes, intervals captured=80.

Connection Mode

For this measurement the DUT was supplied by 3 V. FW was downloaded using JTAG programmer and then it was disconnected from the motherboard. Connection with an iPhone 4S was established with 400ms connection interval.

Table 19: Current consumption during Connection Mode (Note 20)

Power Level (dBm)	Average charge per active state per interval (uC)	Average current for capture (uA)	Peak current (mA)	Peak power (uW)
BYPASS	7.81	22.06	5.68	0.02
0	11.26	30.75	10.03	0.03
+2	11.47	31.28	10.80	0.03
+4	11.58	31.53	11.51	0.03
+6	11.32	30.90	12.68	0.04
+8	10.32	28.38	14.19	0.04
+9.3	9.03	25.13	15.34	0.05

Note 20 Power supply= 3C, T=25ºC, connection interval=400ms, mtu= 23 bytes, intervals captured=300.

Sleep Mode

For this measurement the DUT was supplied by 3 V. FW was downloaded using JTAG programmer and then it was disconnected from the motherboard. Sleep current was measured between both adverting and connection intervals.

Table 20: Current consumption during Sleep Mode

	Average sleep current per interval (uA) advertising	Average sleep current per interval (uA) connection	I_{PEAK}(uA)
Power Level (dBm)			
BYPASS	2.50	2.54	4.48
0	2.55	2.61	4.39
+2	2.54	2.61	4.39
+4	2.54	2.58	4.48
+6	2.53	2.59	4.28
+8	2.54	2.52	4.27
+9.3	2.52	2.56	4.94

13.2 BLE FCC Measurements

13.2.1 Maximum Output Power and Antenna Gain (Transmitter)

13.2.1.1 Test Specification

For systems using digital modulation in the 2400 MHz to 2483.5 MHz band: 1 W (30 dBm).
The EIRP shall not exceed 4 W (36 dBm) (Canada).

13.2.1.2 Test Setup

In order to evaluate the maximum output power, the `SDK prod_test` was used. The boards under test were set into continuous wave modulation transmit mode, using the following command (see Ref.[4]):

Syntax: `prodtest -p <COM_PORT_NUMBER> start_cont_tx <FREQUENCY>  <PAYLOAD_TYPE>`

An RF cable was connected from J5 RF connector to the spectrum analyzer. Three channels were tested: channels CH00=2402 MHz, CH19=2440 MHz and CH39=2480 MHz.

13.2.1.3 Test Results

The maximum peak conducted power was measured using the method according to point 9.1.1 of Guidance for Performing Compliance Measurements on Digital Transmission Systems (DTS) operating under 15.247.

Maximum output power: see next plots.

Maximum declared antenna gain: 2.1 dBi.

Table 21: Maximum (Peak) Output Power (dBm), RBIAS = 2.2k, CH00, CH19, CH39

Parameter (dBm)	CH00 – 2402 MHz	CH19 – 2440 MHz	CH39 – 2480 MHz	Accuracy (dBm)
Maximum conducted power	+9.37	+8.89	+8.62	±0.2
Maximum EIRP power	+11.47	+10.99	+10.72	±0.2

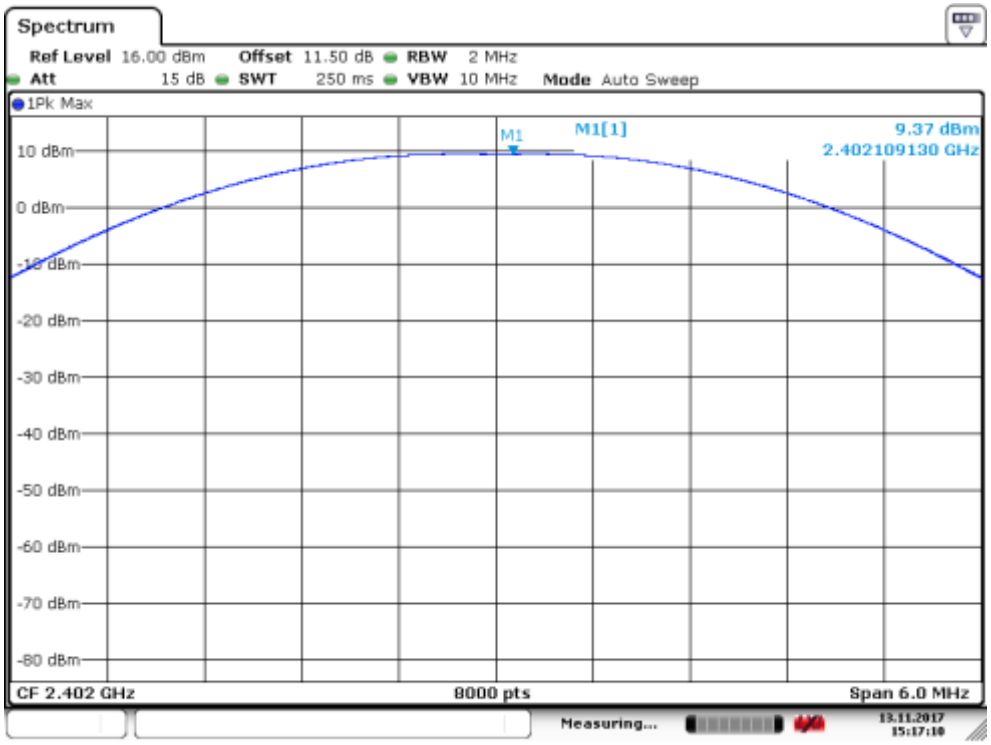


Figure 29: Maximum Output Power, CH00

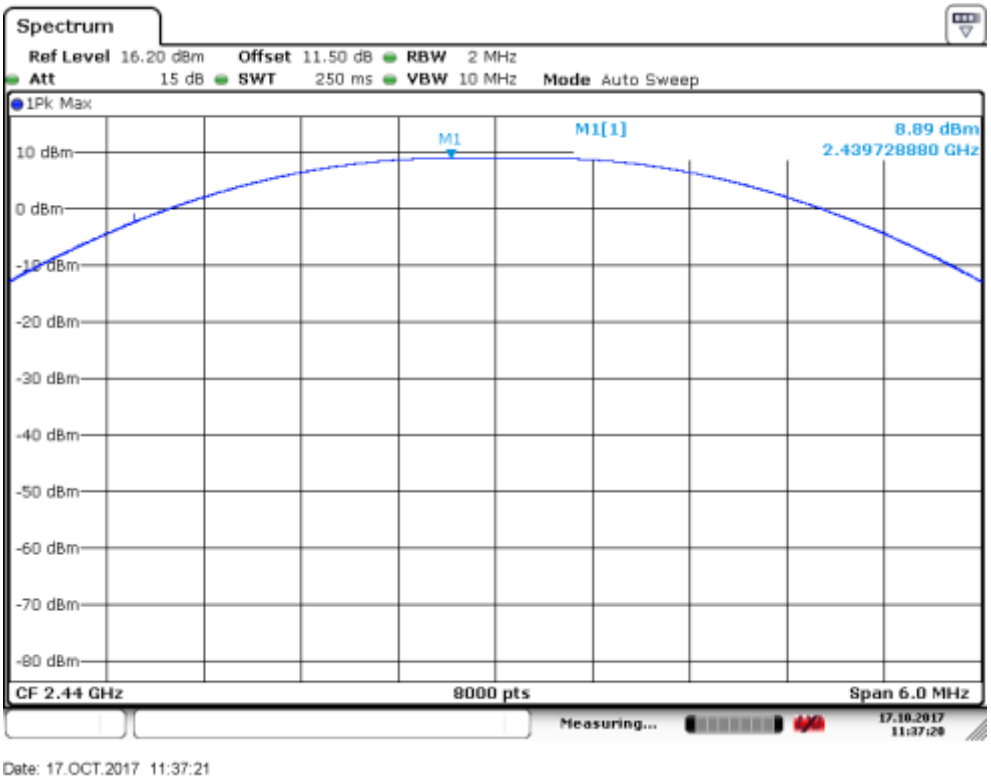


Figure 30: Maximum Output Power, CH19

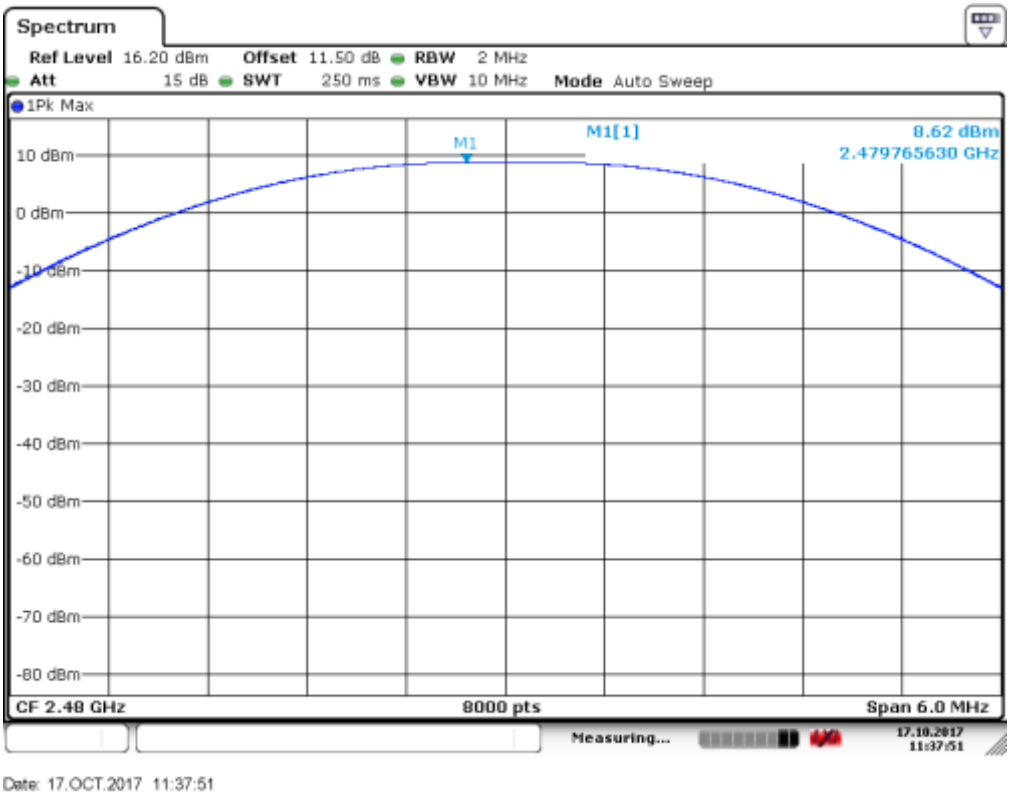


Figure 31: Maximum Output Power, CH39

13.2.2 Emissions Limitations Conducted (Transmitter)

13.2.2.1 Test Specification

In any 100 kHz bandwidth outside the frequency band in which the digitally modulated intentional radiator is operating, the radio frequency power that is produced by the intentional radiator shall be at least 20 dB below that in 100 kHz bandwidth within the band that contains the highest level of the desired power. If the transmitter complies with the conducted power limits based on the RMS averaging over a time interval, the attenuation required shall be 30 dB instead of 20 dB.

13.2.2.2 Test Setup

In order to evaluate the harmonic level production, the `SDK prod_test` was used. The boards under test were set into continuous wave modulation transmit mode, using the following command (see Ref.[4]):

Syntax: `prodtest –p <COM_PORT_NUMBER> start_cont_tx <FREQUENCY>  <PAYLOAD_TYPE>`

An RF cable was connected from J5 RF connector to the spectrum analyzer. Three channels were tested: channels CH00=2402 MHz, CH19=2440 MHz and CH39=2480 MHz.

13.2.2.3 Test Results

Table 22: Measured Reference Level

Parameter (dBm)	CH00 – 2402 MHz	CH19 – 2440 MHz	CH39 – 2480 MHz
Reference Level	8.32	7.86	7.62
Limit (20 dB below peak)	-11.68	-12.14	-12.38

Table 23: Conducted TX Harmonics at CH00, CH19, CH39

Parameter (dBm)	CH00 – 2402 MHz	CH19 – 2440 MHz	CH39 – 2480 MHz
2nd harmonic power	-58.03	-49.63	-59.03
3rd harmonic power	-65.67	-54.93	-64.61
4th harmonic power	-	-	-64.74
5th harmonic power	-	-56.25	-64.38

Lowest frequency: 2402 MHz

All peaks are more than 20 dB below the limit.

Middle frequency: 2440 MHz

All peaks are more than 20 dB below the limit.

Highest frequency: 2480 MHz

All peaks are more than 20 dB below the limit.

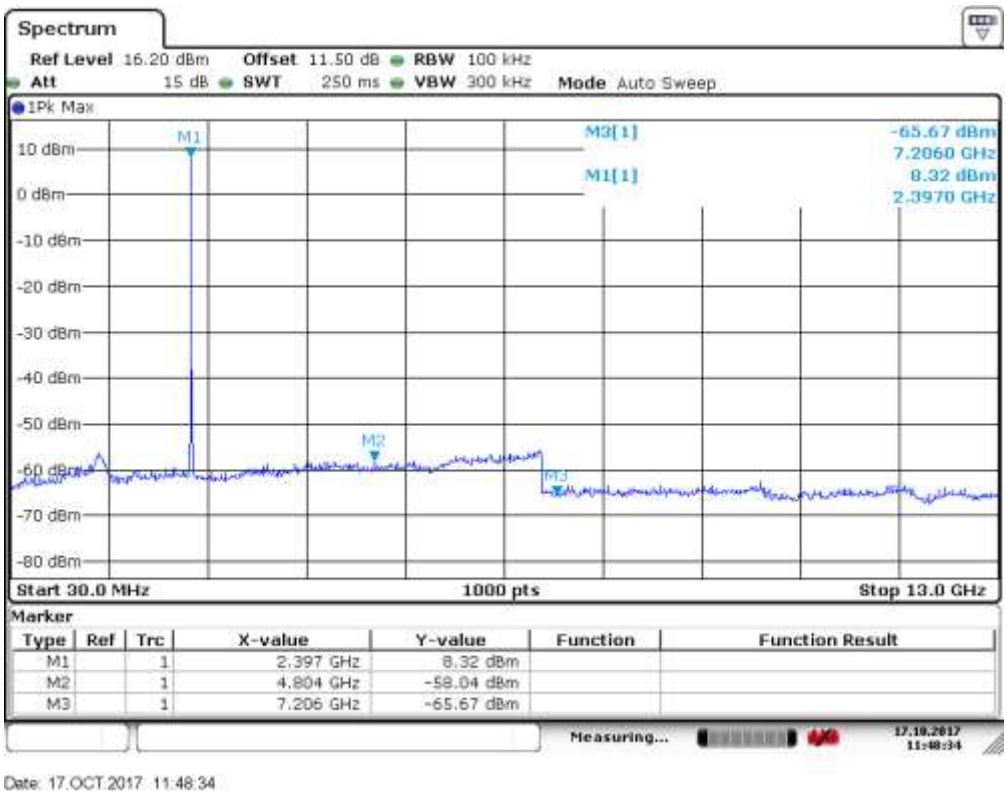


Figure 32: Harmonics Level, Lowest Frequency, CH00

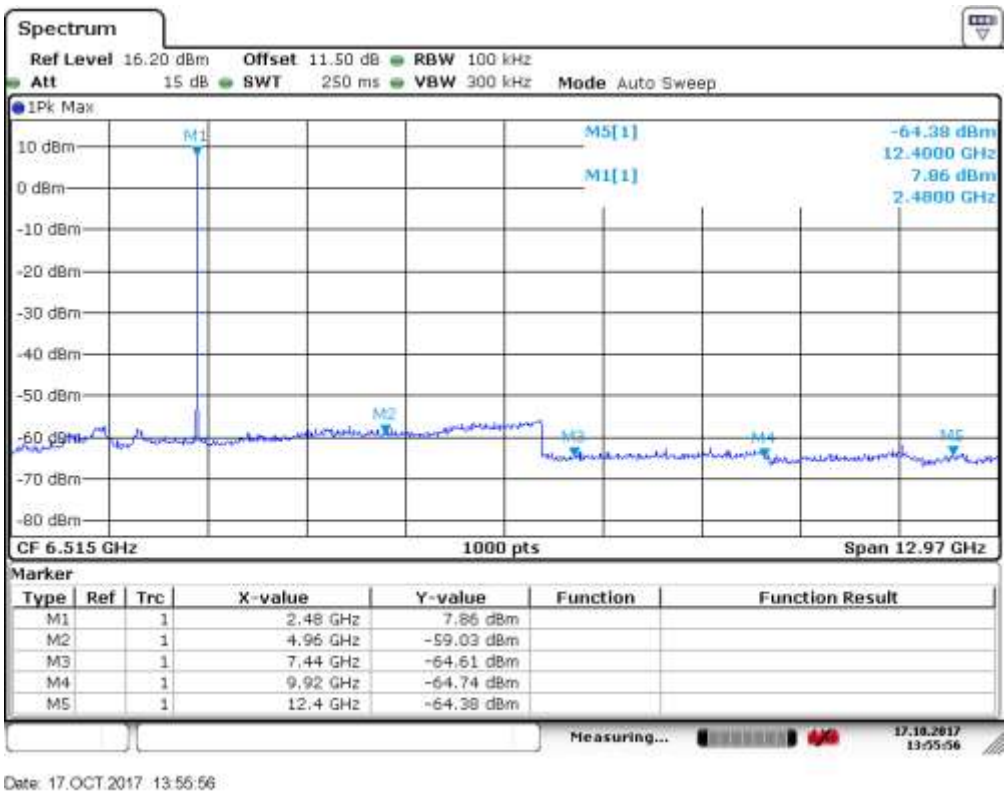


Figure 33: Harmonics Level, Lowest Frequency, CH19

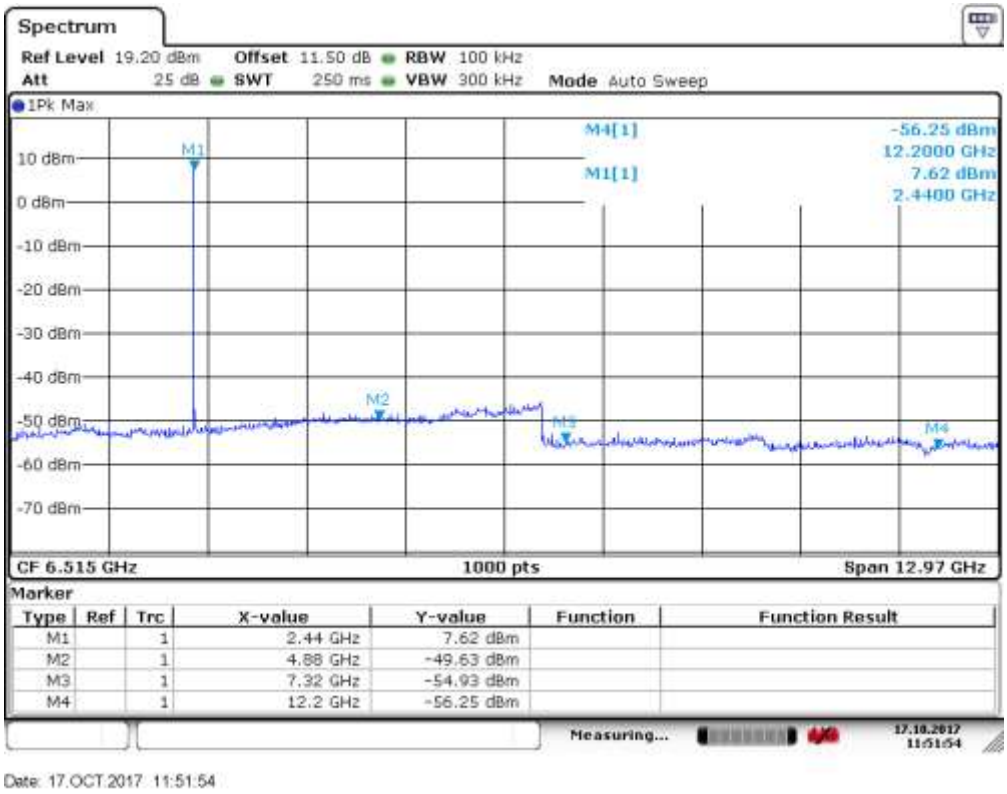


Figure 34: Harmonics Level, Lowest Frequency, CH39

Verdict: All measurements comply with the limits specified in FCC 15.247, Subclause (d).

13.2.3 Band Edge Compliance Radiated (Transmitter)

13.2.3.1 Test Specification

In any 100 kHz bandwidth outside the frequency band in which the spread spectrum or digitally modulated intentional radiator is operating, the radio frequency power that is produced by the intentional radiator shall be at least 20 dB below that in the 100 kHz bandwidth within the band that contains the highest level of the desired power, based on either an RF conducted or a radiated measurement. Attenuation below the general limits specified in Section 15.209(a) is not required.

In addition, radiated emissions which fall in the restricted bands, as defined in Section 15.205(a), must also comply with the radiated emission limits specified in Section 15.209(a) (see Section 5.205(c)).

Limits: 54 dBµV/m AVG

74 dBµV/m Peak

13.2.3.2 Test Setup

Measurement of the radiated band edge compliance. The DA14585 Range Extender is turned in the position that results in the maximum level at the band edge. Then a sweep over the corresponding restricted band is performed. The DA14585 Range Extender is set to single channel mode and the transmit frequency CH00=2402 MHz for the lower restricted band and CH39=2480 MHz for the upper restricted band. Measurement distance is 3m.

In order to evaluate the emissions in the restricted bands for the upper and lower channel, the `SDK prod_test` was used. The boards under test were set into continuous wave modulation transmit mode, using the following command (see Ref.[4]):

Syntax: `prodtest –p <COM_PORT_NUMBER> start_cont_tx <FREQUENCY>  <PAYLOAD_TYPE>`

13.2.3.3 Test Results

Table 24: Band edge compliance radiated

Scenario	Band edge compliance radiated
Modulation	GFSK
Lower restricted band	51.2 dBµV/m (Peak) 39.6 dBµV/m (AVG)
Upper restricted band	60.9 dBµV/m (Peak) 49.3 dBµV/m (AVG)

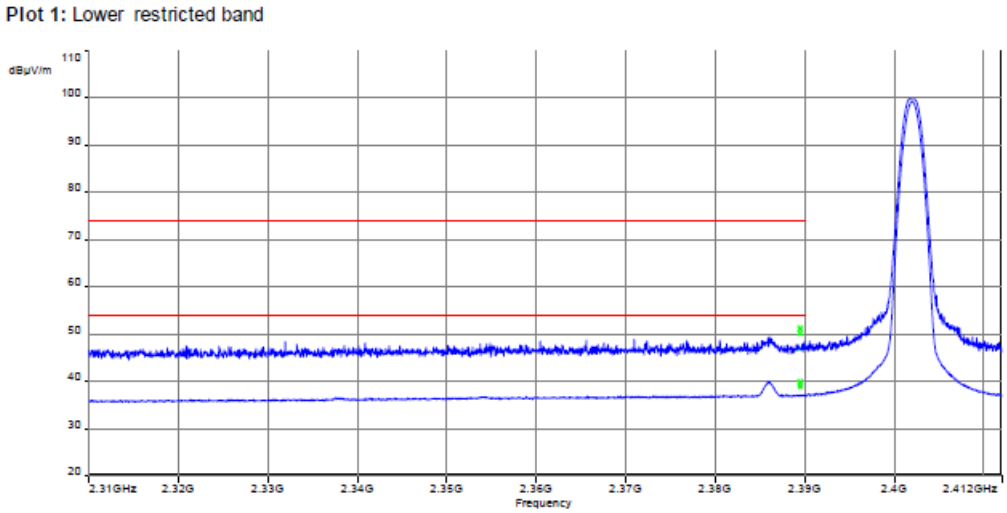


Figure 35: Radiated Emissions in Lower Restricted Band, CH00

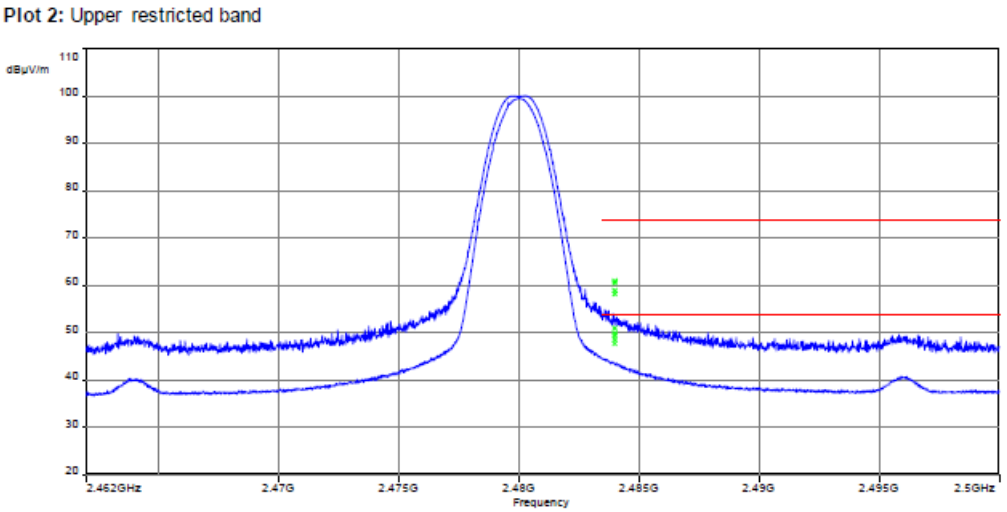


Figure 36: Radiated Emissions in Upper Restricted Band, CH39

13.2.4 Band Edge Compliance Conducted (Transmitter)

13.2.4.1 Test Specification

Measurement of the radiated band edge compliance with a conducted test setup.
Limit: -41.26 dBm

13.2.4.2 Test Setup

In order to evaluate the band edge emission levels for the upper and lower channels, the `SDK prod_test` was used. The boards under test were set into continuous wave modulation transmit mode, using the following command (see Ref.[4]):

Syntax: `prodtest -p <COM_PORT_NUMBER> start_cont_tx <FREQUENCY>  <PAYLOAD_TYPE>`

An RF cable was connected from J5 RF connector to the spectrum analyzer. The DA14585 Range Extender is set to single channel mode and the transmit frequency CH00=2402 MHz for the lower restricted band and CH39=2480 MHz for the upper restricted band.

13.2.4.3 Test Results

Table 25: Band edge compliance conducted

Scenario	Band edge compliance [dBm] (excluded antenna gain)
Modulation	GFSK
Max. lower band edge power	-52.1
Max. upper band edge power	-42.8

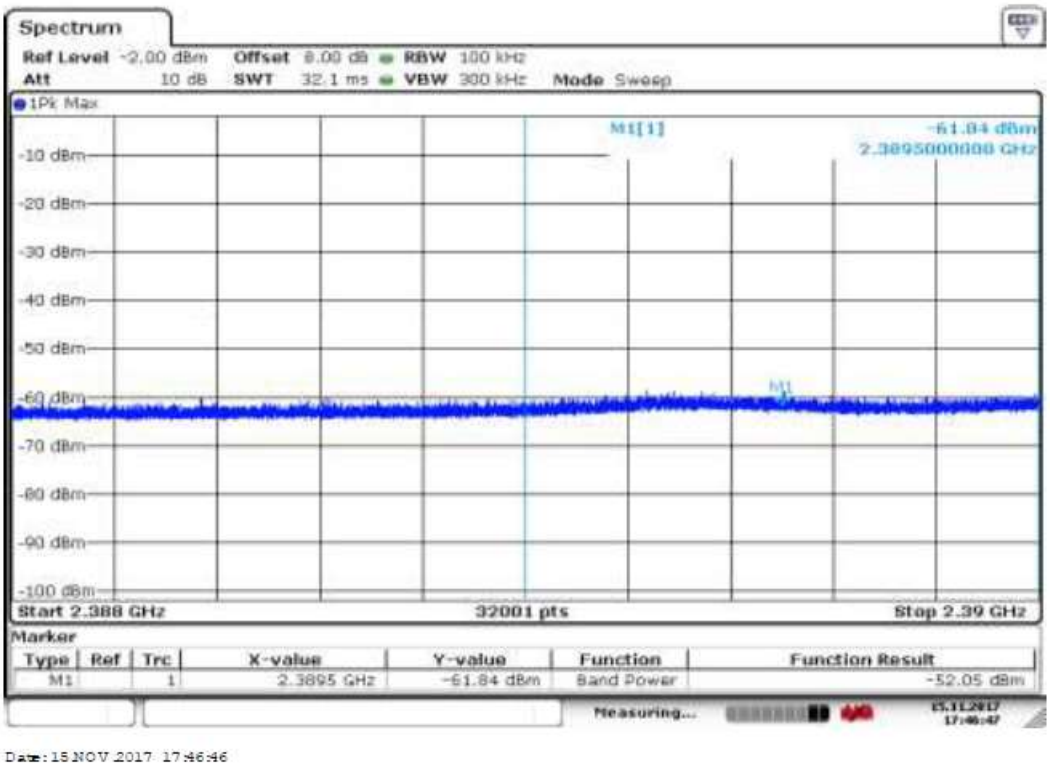


Figure 37: Conducted Emissions in Lower Band Edge, CH00

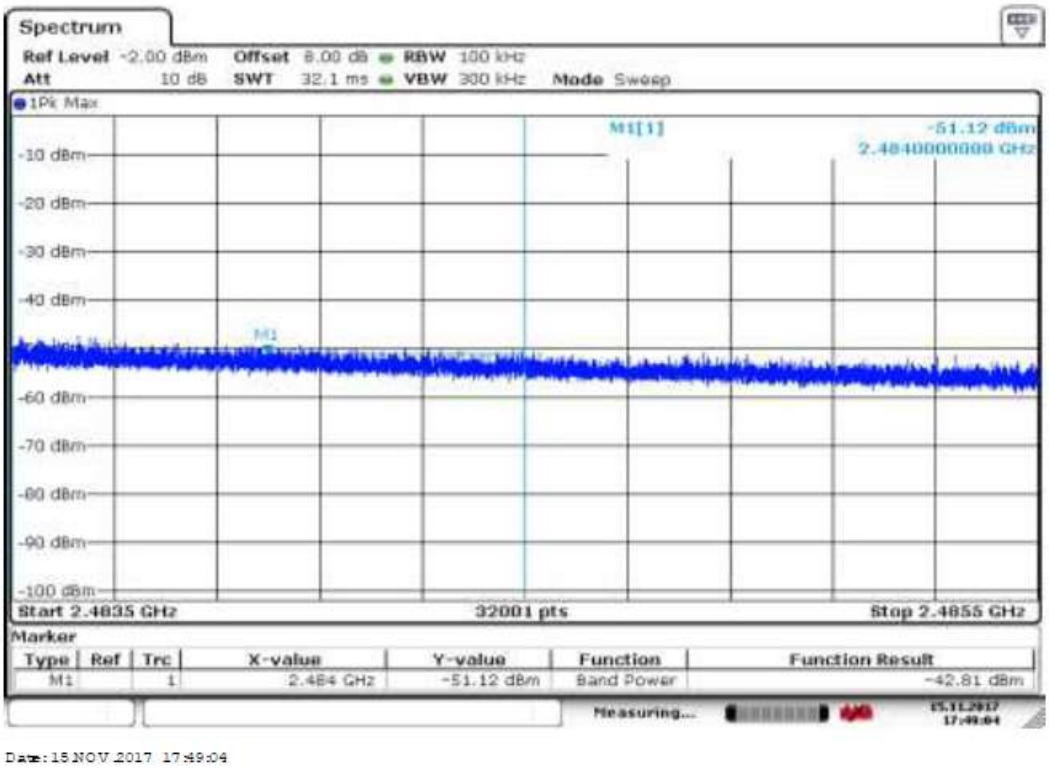


Figure 38: Conducted Emissions in Upper Band Edge, CH39

Verdict: All measurements comply with the limits specified in FCC 15.247, Subclause (d).

13.2.5 Spurious Emissions Radiated above 1GHz

13.2.5.1 Test Specification

In any 100 kHz bandwidth outside the frequency band in which the spread spectrum or digitally modulated intentional radiator is operating, the radio frequency power that is produced by the intentional radiator shall be at least 20 dB below that in the 100 kHz bandwidth within the band that contains the highest level of the desired power, based on either an RF conducted or a radiated measurement. Attenuation below the general limits specified in Section 15.209(a) is not required.

In addition, radiated emissions which fall in the restricted bands, as defined in Section 15.205(a), must also comply with the radiated emission limits specified in Section 15.209(a) (see Section 5.205(c)).

Table 26: TX spurious emissions radiated limits

Frequency (MHz)	Field Strength (dBµV/m)	Measurement distance(m)
Above 960	54.0 (Average)	3
Above 960	74.0 (Peak)	3

13.2.5.2 Test Setup

Measurement of the radiated spurious emissions in transmit mode. The DA14585 Range Extender is set to single channel mode and the transmit frequencies is CH00=2402 MHz. The measurement is performed in the mode with the highest output power. The modulation with the highest output power was used to perform the transmitter spurious emissions. If spurious were detected a re-measurement was performed on the detected frequency with each modulation.

13.2.5.3 Test Results

Table 27: TX spurious emissions radiated

Frequency (MHz)	TX spurious emissions radiated	
CH00	**Detector**	**Level(dBµV/m)**
4804	Peak	52.3
	AVG	47.2
7206	Peak	45.4
	AVG	36.8
12012	Peak	48.9
	AVG	39.9
14414	Peak	49.4
	AVG	38.9

Table 28: RX spurious emissions radiated

RX spurious emissions radiated [dBµV/m]		
F [MHz]	Detector	Level [dBµV/m]
4806	Peak	52.4
	AVG	47.3

Plots: Transmitter mode

Plot 1: 1 GHz to 18 GHz, TX mode, 2402 MHz, vertical & horizontal polarization

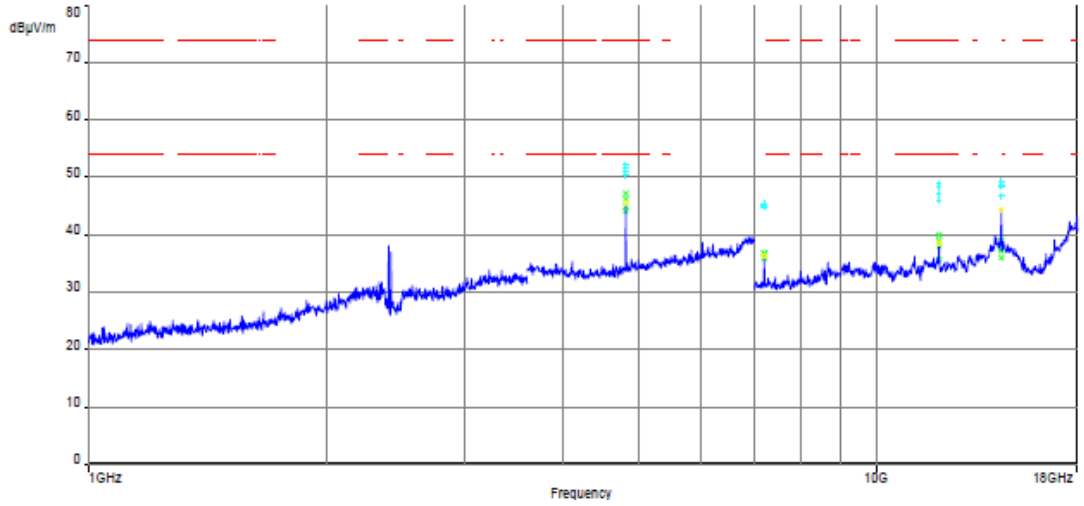


Figure 39: TX spurious emissions radiated, CH00

Plot 2: 1 GHz to 18 GHz, RX / idle – mode, vertical & horizontal polarization

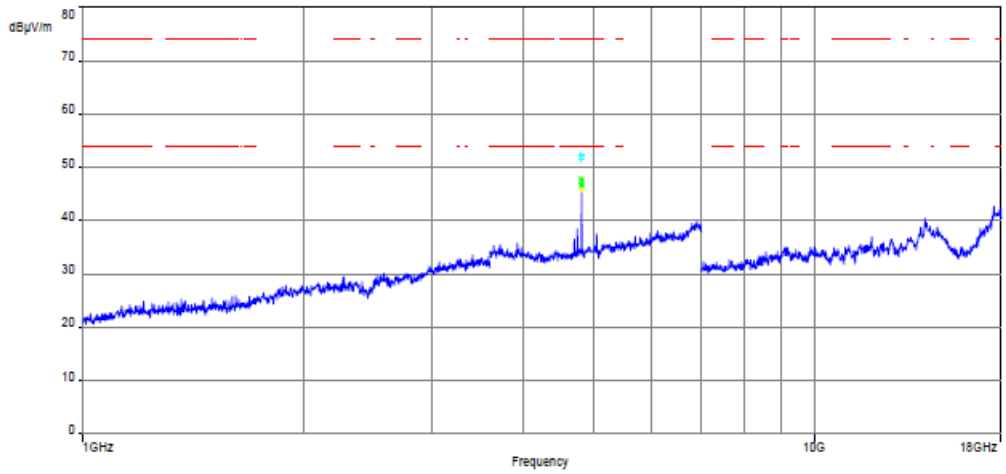


Figure 40: RX spurious emissions radiated, CH00

14 PCB Design Guidelines

14.1 Antenna Selection

The use of the printed antenna described in this reference design (see Figure 41) is optional. A number of other printed antennas with different characteristics are also available at AN-B-027 (see Ref.[6]). It is recommended to make an exact copy of the one of the reference designs, if the available board space permits such a solution. All recommended antenna designs are matched to 50 Ohms.

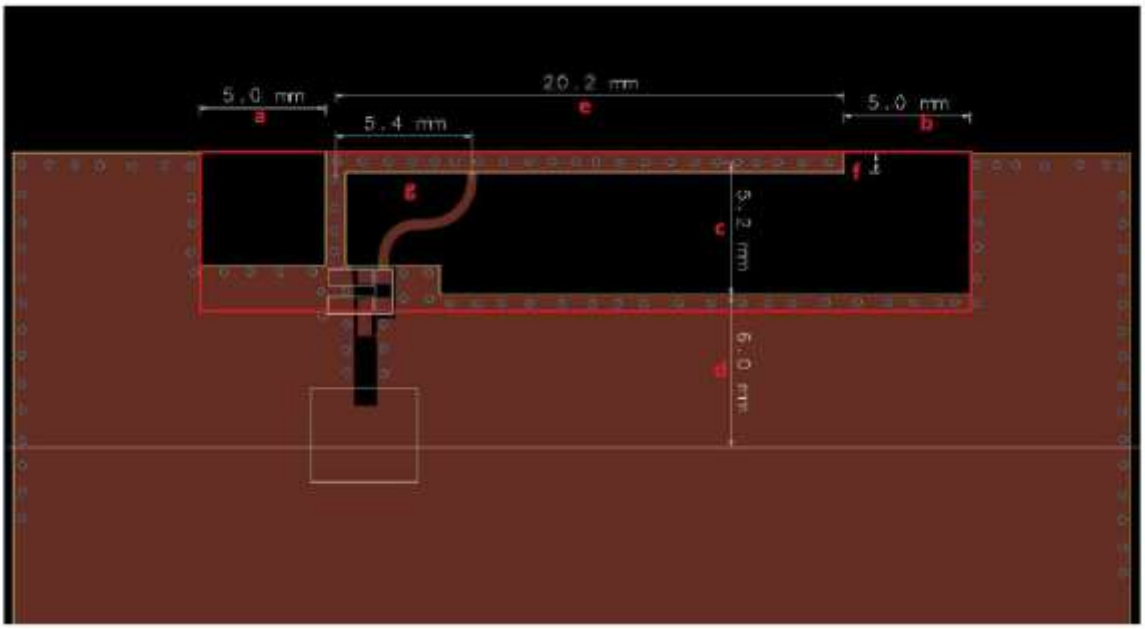


Figure 41: Full size IFA used in DA14585 Range Extender with dimensions

The red outline indicates the antenna footprint, i.e. required allocation of PCB space. The footprint of the antenna is available on request in DXF format.

Legend (see Figure 41):

- Clearance between antenna arm and GND plane left a.
- Clearance between antenna arm and GND plane right b.
  - For narrow PCBs (a) and (b) will coincide with board edges
  - The two GND pieces left and right of the antenna are NOT required for correct antenna operation
- Clearance between antenna arm and GND plane below c.
- Minimum GND plane size required for correct operation of the antenna d.
- Antenna width e.
  - The antenna is implemented on top and bottom layers and stitched together using vias
  - The feeding line (from indicated matching components) is implemented on top layer only
- Antenna trace width (0.6 mm) f.
- Feed point position g.

If the available board space is limited for the printed antenna a chip or ceramic antenna could be a good solution. This antenna type allows small size solutions at the desired frequencies. The tradeoff compared to printed antenna is that it adds BOM and mounting cost.

Also, chip antennas with no tuning often have a resonance frequency above 2.5GHz and the return loss at 2.45GHz is very poor. Therefore the antenna must be always fine-tuned for optimum performance. Finally efficiency is not exceptionally high, typically in the range of 10-50%. The reduced size comes with cost at both performance and pricing. Some parameters that suffer are:

- Reduced efficiency (or gain)
- Shorter range
- Smaller useful bandwidth
- More critical tuning

In case that some other antenna is selected it is suggested to check the peak antenna gain in comparison to the selected operation power level in terms of regulatory compliance (FCC/ETSI standards).

Table 29: Antenna types comparison

Antenna Types	Pros	Cons
Printed antenna	Very low cost Good performance Large bandwidth Simple low profile structure Suitable for size- optimized pcb in stable environment Accurate and reliable manufacturing process	Require bigger available pcb area Antenna performance and tuning sensitive to PCB design Tuning susceptible to metal structures or human contact
Chip/ ceramic antenna	Separate component Come to small sizes Less detuned due to proximity to components Less susceptible to environmental or human contact	Higher cost Medium performance Matching function of PCB size and shape of GND

14.2 RF layout design

Guidelines to consider for the general RF layout work are the following (for more details see Ref.[6]):

14.2.1 Radio IC

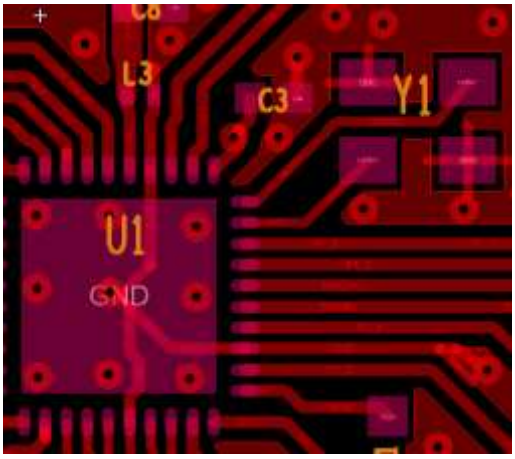


Figure 42: DA14585 Range Extender board layout snapshot

● Active components operating at high frequency should have the layout as compact as possible.

● Always provide a solid grounding to the radio IC. Use as many vias as possible to create a solid GND under the IC itself and connect it to inner (if any) and bottom GND layers.

● Place the XTAL used as reference for the RF carrier (16 MHz for the DA14585) as close as possible to the IC. This minimizes any additional capacitive load on the input pins and reduces the chance of crosstalk and interference with other signals on the board.

14.2.2 RF transmission lines

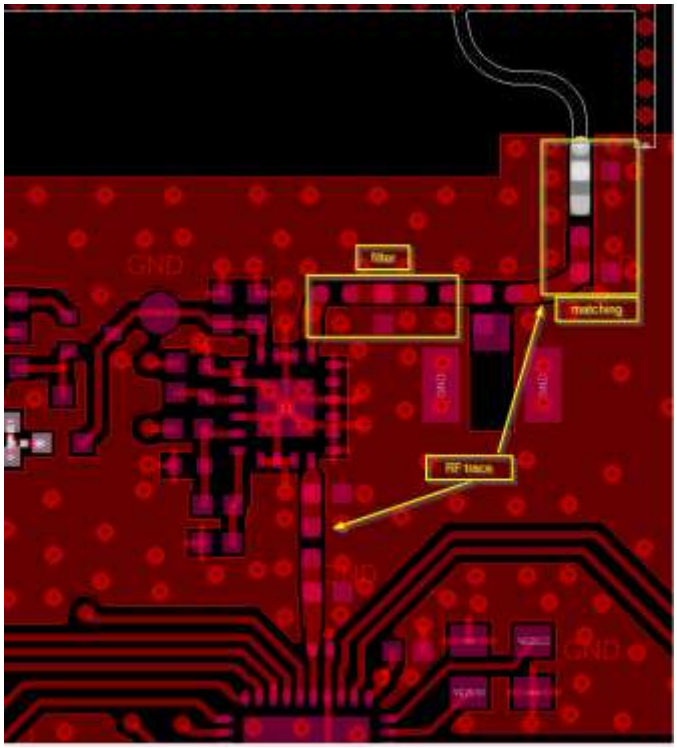


Figure 43: Placement of filter and matching network

- Place radio matching components and any RF filters as close as possible to the radio.
- Minimize transmission line length between radio IC and antenna
- Place antenna matching components as close as possible to the feeding point of the antenna
- The characteristic impedance of the transmission line should match the required radio impedance (50 Ohms for the DA14585)

14.2.3 RX Spurious Emissions

RX spurious emissions come from the RF device when it is in receive mode. This is a common effect in radios and the maximum level on these emitted frequencies is set in regulatory standards. The level of these spurious emissions depends on the actual output from the device, but layout design factors can contribute significantly.

General advices in order to keep the spurious in the limits for an end product are the following:

Decoupling capacitors

Proper decoupling is important for optimum performance and regulatory issues.

- Place decoupling capacitors on same layer as active component and in proximity to the pin it is supposed to decouple
- Route power into the decoupling capacitor and then into the active component
- All decoupling capacitors should have vias placed close to the capacitor ground pad to ensure a short path to the ground plane.

PCB layout

- Connect the ground plane on the different layer with several vias.
- The lowest impedance return path is in a plane directly underneath the signal trace since this provides the lowest inductance path. A spurious emission problem could occur when there are

discontinuities in the current return path. These discontinuities cause the return current to flow in larger loops, which increases the radiation from the board.

- Local decoupling is less hindered by parasitic impedance of board trace and shorter traces create a smaller antenna to radiate the unwanted tones. Avoid long traces.
- For complex designs it is proposed to provide solid ground planes using internal layers.

15 Safety Information

The DA14585 Range Extender Bluetooth® Low Energy (BLE) daughterboard is intended for use as a development platform for hardware or software in a laboratory environment. The board is an open system design, which does not include a shielded enclosure. The equipment is intended to operate in the operating supply voltages and temperatures specified in this guide.

The DA14585 Range Extender consists of a PCB which comply V-0 flammability class and the power supply used shall comply with clause 2.5 of EN 60950-1 standard.

The equipment has not the necessary enclosure to protect the operator against the electrical shocks, fire enclosure, and mechanical risks. Dialog Semiconductor recommends that “additional equipment must be supplied to provide the necessary protection according to the EN 60950-1 Standard”.

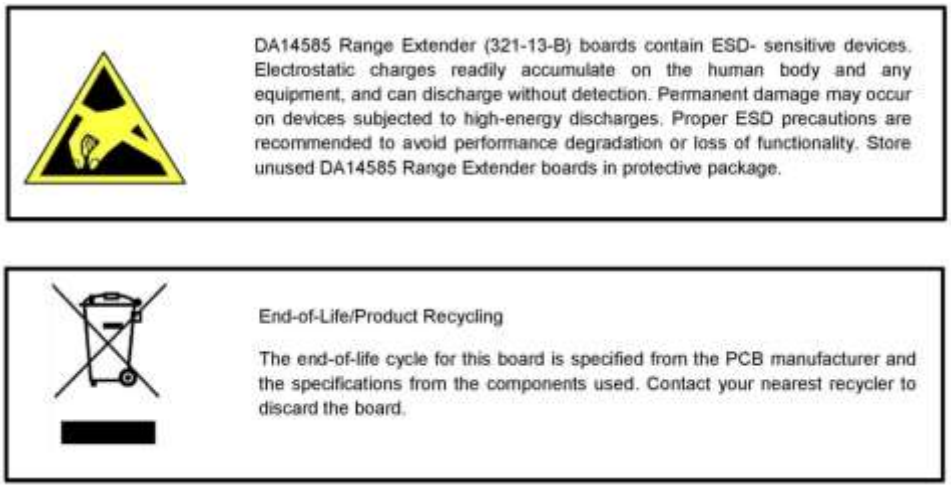


Figure 44: Safety Information of DA14585 Range Extender

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Dialog Semiconductor recommends that the user perform procedures only at an ESD workstation. If an ESD workstation is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to the chassis ground (any unpainted metal surface) on the board when handling parts.

Handling Boards

DA14585 Range Extender boards are sensitive to ESD. Hold the board only by its edges. Place it on a grounded, static-free surface. Use a conductive foam pad if available. Do not slide the board over any surface.

Battery Care and Use

The boards don’t contain any battery. However, there is a place for mounting battery holder for adding CR2032 battery. Dialog Semiconductor recommends:

- The use of correct size and type of battery specified in the user manual. Any bad use of battery is under user responsibility.
- Follow user manual guide to properly power up the board when mounted on DA14580 PRO-motherboard.
- Keep battery contacts surfaces clean.
- Do not short the battery with metal surfaces.
- Do not subject the battery to high temperatures or high humidity.
- Do not recharge battery unless it is marked “rechargeable”.

Appendix A Application Software Guide

The following instructions are based on DA14585_SDK_6.0.10. Instructions are valid for Keil 5 projects. Screenshots shown are in Keil 5.

The software driver consists of the necessary functions that need to be used from the range_ext_api.h in order to enable the operation of the SKY66111-11 to an SDK project.

In general, the necessary steps for using 585 SKY66111-11 driver are:

- Inserting the driver to a project
- Set the desired power level for the operation

A.1 Driver Implementation

The driver includes two files:

- sky66111.h
- sky66111.c

SKY66111.h contains the necessary definitions.
SKY66111.c file contains the implementation of the basic functions for SKY66111 operation.

A.1.1 SKY66111.h

1. Control pins configuration

```
/*****************************************************************************************************/
/* Control pins                                                                                      */
/*****************************************************************************************************/

#define CTRL_PWM_PORT       GPIO_PORT_2
#define CTRL_PWM_PIN        GPIO_PIN_1
#define CTRL_PMAX_PORT      GPIO_PORT_2
#define CTRL_PMAX_PIN       GPIO_PIN_7
#define CTX_PORT            GPIO_PORT_0
#define CTX_PIN             GPIO_PIN_1
#define CRX_PORT            GPIO_PORT_0
#define CRX_PIN             GPIO_PIN_2
```

Figure 45: Control pins configuration in SKY66111.h

2. Power modes definition

```
/*****************************************************************************************************/
/* Controls FEM output power                                                                         */
/* FEM_BYPASS : FEM is bypassed, xxdBm output                                                        */
/* FEM_MAXP   : FEM at max power output 9.3dBm                                                       */
/* FEM_PWM    : FEM voltage is controlled by PWM, output power variable according to the following table */
/*                                                                                                   */
/*   OUTPUT POWER          |   DUTY CYCLE                                                            */
/*      0 dBm              |      42%                                                                */
/*      2 dBm              |      48%                                                                */
/*      4 dBm              |      55%                                                                */
/*      6 dBm              |      65%                                                                */
/*      8 dBm              |      82%                                                                */
/*****************************************************************************************************/
/*
FEM_BYPASS      : FEM is bypassed, xxdBm output
FEM_MAXP        : FEM at max power output 9.3dBm
FEM_PWM         : FEM voltage is controlled by PWM, output power variable according to the following table enum range_ext_modes
*/
enum range_ext_modes
{
    FEM_BYPASS_MODE = 0,
    FEM_MAXP_MODE,
    FEM_PWM_MODE
};
```

Figure 46: Power modes definition in SKY66111.h

3. PWM Duty Cycle Preset Values

```
/*
    OUTPUT POWER        |   DUTY CYCLE
        0 dBm           |       42%
        2 dBm           |       48%
        4 dBm           |       55%
        6 dBm           |       65%
        8 dBm           |       82%

        9,3             |   (No dutycle)MAX_POWER
        BYPASS          |       BYPASS
*/
enum duty_cycle_presets
{
    ZERO_DBM  = 0,
    TWO_DBM   = 2,
    FOUR_DBM  = 4,
    SIX_DBM   = 6,
    EIGHT_DBM = 8,
    MAX_POWER,
    BYPASS
};

#define ZERO_DBM_DC     42
#define TWO_DBM_DC      48
#define FOUR_DBM_DC     55
#define SIX_DBM_DC      65
#define EIGHT_DBM_DC    82

#define T_PWM_DEFAULT       100             //PWM period T_PWM/16MHz -> set at 6.25us (160kHz)
```

Figure 47: Definition of PWM duty cycle preset values in SKY66111.h

A.1.2 SKY66111.c

4. Global variables declaration for the api.

```
/*
 * GLOBAL VARIABLE DECLARATIONS
 ****************************************************************************************
 */

struct range_ext_api range_ext      __attribute__((section("retention_mem_area0"), zero_init));
uint8_t range_ext_mode              __attribute__((section("retention_mem_area0"), zero_init));
uint16_t range_ext_power            __attribute__((section("retention_mem_area0"), zero_init));
```

Figure 48: Global variables declaration in SKY66111.c for the range_ext_api.h

5. Configure GPIOs for SKY66111 operation

```
static void configure_control_pins(void)
{
    /* Select diag signals */
    SetBits32(BLE_DIAGCNTL_REG, DIAG1, 0x28);              // extrc_txen
    SetBits32(BLE_DIAGCNTL_REG, DIAG2, 0x28);              // rxen=extrc_txen_inv
    //SetBits32(BLE_DIAGCNTL_REG, DIAG3, 0x22);            // event_in_process


    /* Map to diag port bits */
    SetBits32(BLE_DIAGCNTL3_REG, DIAG1_BIT, 3);            // extrc_txen
    SetBits32(BLE_DIAGCNTL3_REG, DIAG2_BIT, 3);            // rxen=extrc_txen_inv
    SetBits32(BLE_DIAGCNTL3_REG, DIAG2_INV, 1);            // rxen=extrc_txen_inv
    //SetBits32(BLE_DIAGCNTL3_REG, DIAG3_BIT, 0);          // event_in_process


    /* Enable diag ports */
    SetBits32(BLE_DIAGCNTL_REG, DIAG1_EN, 1);
    SetBits32(BLE_DIAGCNTL_REG, DIAG2_EN, 1);
    //SetBits32(BLE_DIAGCNTL_REG, DIAG3_EN, 1);


    /* Output diag signals to P0 GPIOs */
    SetBits16(P01_MODE_REG, PID , 18);
    SetBits16(P01_MODE_REG, PUPD,  3);                     //TXEN = P0_1

    SetBits16(P02_MODE_REG, PID , 18);
    SetBits16(P02_MODE_REG, PUPD,  3);                     //RXEN = P0_2

    //SetBits16(P10_MODE_REG, PID , 18);
    //SetBits16(P10_MODE_REG, PUPD,  3);                   //wlan coexistence = P1_0
}
```

Figure 49: Configure GPIOs for SKY66111 operation

6. Configure PWM timer0 for SKY66111

```
/*****************************************************************************************
* @brief Configure PWM timer for SKY66111.
* @param[in] duty_cycle    Duty cycle
* @param[in] period        Period
* @return void
*****************************************************************************************
*/
static void timer0_conf_start(uint8_t duty_cycle, uint8_t period)
{
    set_tmr_enable(CLK_PER_REG_TMR_ENABLED);
    set_tmr_div(CLK_PER_REG_TMR_DIV_1);
    timer0_init(TIM0_CLK_FAST, PWM_MODE_ONE, TIM0_CLK_NO_DIV);
    timer0_set_pwm_on_counter(0xFFFF);
    timer0_set_pwm_high_counter(period*duty_cycle/100);
    timer0_set_pwm_low_counter(period*(period-duty_cycle)/100);
    timer0_start();
}
```

Figure 50: Function timer0_conf_start();

7. Reserve GPIO pins for the SKY66111

```
/**********************************************************************************************
* @brief Reserve GPIO pins for FEM.
* @param[in] cb        Callback function called when action is completed
* @return void
**********************************************************************************************
*/
static void declare_fem_gpios(range_ext_callback cb)
{
    RESERVE_GPIO(CTRL_PWM, CTRL_PWM_PORT, CTRL_PWM_PIN, PID_PWM0);        // CTRL_PWM = P2_1
    RESERVE_GPIO(CTRL_PWM_BP, CTRL_PMAX_PORT, CTRL_PMAX_PIN, PID_GPIO);   // CTRL_PWM_BP = P2_7
    RESERVE_GPIO(CTX, CTX_PORT, CTX_PIN, PID_GPIO);                       // SKY66111 bypass operation
    RESERVE_GPIO(CRX, CRX_PORT, CRX_PIN, PID_GPIO);                       // SKY66111 bypass operation
}
```

Figure 51: Function declare_fem_gpios();

8. Configure FEM and control signals for the specified power levels

```
/*****************************************************************************************************
* @brief Configures FEM and control signals according to global variable: range_ext_power
* @param[in] void
* @return void
*****************************************************************************************************
*/
static void app_range_extender_reinit(void)
{
    switch (range_ext_power)
    {
        case ZERO_DBM:
            GPIO_ConfigurePin(CTRL_PWM_PORT, CTRL_PWM_PIN, OUTPUT, PID_PWM0, true);    //PWM pin active
            GPIO_ConfigurePin(CTRL_PMAX_PORT, CTRL_PMAX_PIN, OUTPUT, PID_GPIO, true);  //Max power mode inactive

            timer0_conf_start(ZERO_DBM_DC,T_PWM_DEFAULT);
            configure_control_pins();

            range_ext_mode = FEM_PWM_MODE;

            break;
        case TWO_DBM:
            GPIO_ConfigurePin(CTRL_PWM_PORT, CTRL_PWM_PIN, OUTPUT, PID_PWM0, true);    //PWM pin active
            GPIO_ConfigurePin(CTRL_PMAX_PORT, CTRL_PMAX_PIN, OUTPUT, PID_GPIO, true);  //Max power mode inactive

            timer0_conf_start(TWO_DBM_DC,T_PWM_DEFAULT);
            configure_control_pins();

            range_ext_mode = FEM_PWM_MODE;
            break;
        case FOUR_DBM:
            GPIO_ConfigurePin(CTRL_PWM_PORT, CTRL_PWM_PIN, OUTPUT, PID_PWM0, true);    //PWM pin active
            GPIO_ConfigurePin(CTRL_PMAX_PORT, CTRL_PMAX_PIN, OUTPUT, PID_GPIO, true);  //Max power mode inactive

            timer0_conf_start(FOUR_DBM_DC,T_PWM_DEFAULT);
            configure_control_pins();

            range_ext_mode = FEM_PWM_MODE;

            break;

        case SIX_DBM:
            GPIO_ConfigurePin(CTRL_PWM_PORT, CTRL_PWM_PIN, OUTPUT, PID_PWM0, true);    //PWM pin active
            GPIO_ConfigurePin(CTRL_PMAX_PORT, CTRL_PMAX_PIN, OUTPUT, PID_GPIO, true);  //Max power mode inactive

            timer0_conf_start(SIX_DBM_DC,T_PWM_DEFAULT);
            configure_control_pins();

            range_ext_mode = FEM_PWM_MODE;

            break;
        case EIGHT_DBM:
            GPIO_ConfigurePin(CTRL_PWM_PORT, CTRL_PWM_PIN, OUTPUT, PID_PWM0, true);    //PWM pin active
            GPIO_ConfigurePin(CTRL_PMAX_PORT, CTRL_PMAX_PIN, OUTPUT, PID_GPIO, true);  //Max power mode inactive

            timer0_conf_start(EIGHT_DBM_DC,T_PWM_DEFAULT);
            configure_control_pins();

            range_ext_mode = FEM_PWM_MODE;
            break;
        case MAX_POWER:
            GPIO_ConfigurePin(CTRL_PWM_PORT, CTRL_PWM_PIN, OUTPUT, PID_GPIO, false);   //PWM pin inactive
            GPIO_ConfigurePin(CTRL_PMAX_PORT, CTRL_PMAX_PIN, OUTPUT, PID_GPIO, false); //Set max power mode

            configure_control_pins();

            range_ext_mode = FEM_MAXP_MODE;
      break;
        case BYPASS:
            GPIO_ConfigurePin(CTRL_PMAX_PORT, CTRL_PMAX_PIN, OUTPUT, PID_GPIO, false);//Configure VCC=3V for sky66111 during bypass
            GPIO_ConfigurePin(CTX_PORT, CTX_PIN, OUTPUT, PID_GPIO, false);      //control signal configuration -CTX low- for SKY66111 bypass
            GPIO_ConfigurePin(CRX_PORT, CRX_PIN, OUTPUT, PID_GPIO, true);       //control signal configuration -CRX high- for SKY66111 bypass

            range_ext_mode = FEM_BYPASS_MODE;
            break;
        default:
            GPIO_ConfigurePin(CTRL_PWM_PORT, CTRL_PWM_PIN, OUTPUT, PID_GPIO, false);   //PWM pin inactive
            GPIO_ConfigurePin(CTRL_PMAX_PORT, CTRL_PMAX_PIN, OUTPUT, PID_GPIO, false); //Set max power mode

            configure_control_pins();

            range_ext_mode = FEM_MAXP_MODE;
            break;
    }
}
```

Figure 52: Function app_range_extender_reinit();

9. Enable FEM

```
/*****************************************************************************************
* @brief Enables FEM with the help of app_range_extender_reinit
* @param[in] power      Power to be set
* @param[in] cb         Callback function called when action is completed
* @return void
*****************************************************************************************
*/
static void app_range_extender_enable(uint16_t power, range_ext_callback cb)
{
    range_ext_power = power;
    app_range_extender_reinit();
}
```

Figure 53: Function app_range_extender_enable();

10. Disable FEM power control signals during sleep

```
/*****************************************************************************************
* @brief Disables FEM and sets control signals to high-z state.
* @param[in] cb         Callback function called when action is completed
* @return void
*****************************************************************************************
*/
static void app_range_extender_sleep(range_ext_callback cb)
{
    switch (range_ext_mode)
    {
        case FEM_BYPASS_MODE:
            GPIO_ConfigurePin(CTRL_PMAX_PORT, CTRL_PMAX_PIN, OUTPUT, PID_GPIO, true);
            GPIO_ConfigurePin(CTRL_PWM_PORT, CTRL_PWM_PIN, OUTPUT, PID_GPIO, false);      //PWM pin inactive (output low)
            break;
        case FEM_MAXP_MODE:
            GPIO_ConfigurePin(CTRL_PMAX_PORT, CTRL_PMAX_PIN, OUTPUT, PID_GPIO, true);   //Max power mode inactive
            break;
        case FEM_PWM_MODE:
            GPIO_ConfigurePin(CTRL_PWM_PORT, CTRL_PWM_PIN, OUTPUT, PID_GPIO, false);      //PWM pin inactive (output low)
            break;
    }
}
```

Figure 54: Function app_range_extender_sleep();

11. Set the range extender output power

```
/**
*****************************************************************************************
* @brief Set the range extender output power.
* @param[in] power      Power to be set
* @param[in] cb         Callback function called when action is completed
* @return void
*****************************************************************************************
*/
static void app_set_power(uint16_t power, range_ext_callback cb)
{
    timer0_stop();
    app_range_extender_enable(power, NULL);
}
```

Figure 55: Function app_set_power();

12. Initialization of range_ext_api

Introduction of app_range_extender.reinit() into range_ext_api, enables the range extender with the value set by the user. The TX output power value is kept during sleep time.

```
252  void range_ext_init(struct range_ext_api *api)
253  {
254      api->init_gpio       = declare_fem_gpios;
255      api->enable          = app_range_extender_enable;
256      api->disable         = app_range_extender_sleep;
257      api->set_power       = app_set_power;
258      api->set_fem_rx_mode = NULL;
259      api->re_init         = app_range_extender_reinit;
260
261  }
```

Figure 56: function range_ext_init();

A.2 Insert driver to proximity reporter project

The example project used to describe the necessary steps here is proximity reporter.

A.2.1 Steps

Step 1: Copy rext_sky66111-11_v1.1 folder in the driver folder of sdk: DA14585_SDK\6.0.10.511\sdk\platform\driver

The folder contains three files:

- sky66111.c (inside sky66111 folder)
- sky66111.h (inside sky66111 folder)
- range_ext_api.h

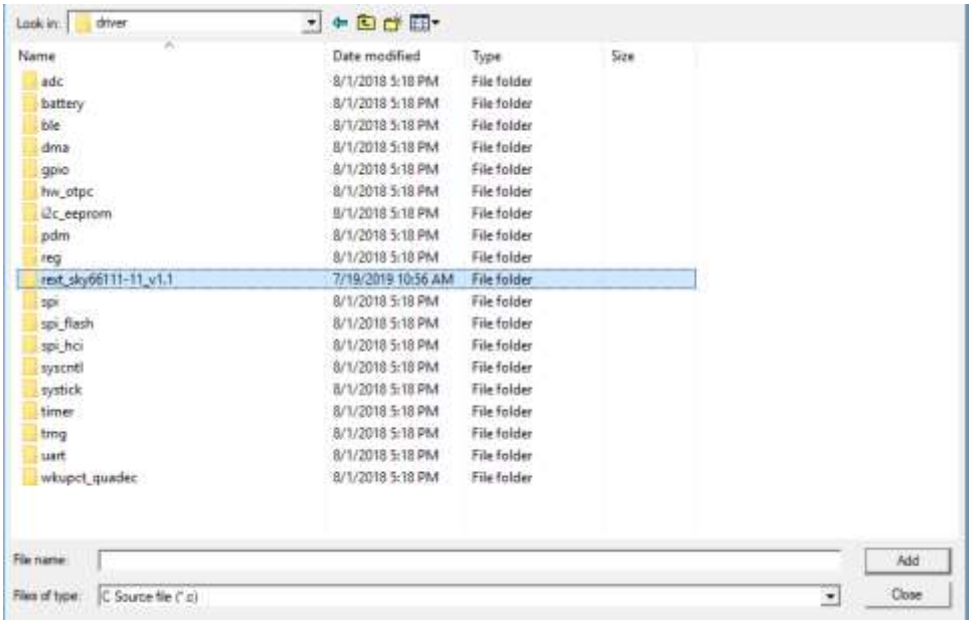


Figure 57: Copy rext_sky66111-11_v1.1 folder into sdk driver

Step 2: Open the project and add sky66111.c in sdk_driver of the keil project

Right click ‘sdk_driver’ and select “Add existing files to Group ‘app’”. Add sky66111.c

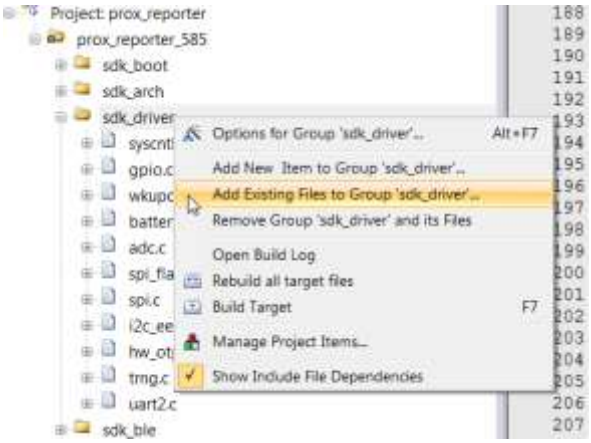


Figure 58: Step 2 of adding sky66111.c to sdk_driver

Step 3: Select target options and add the rext_sky66111-11_v1.1 folder in the compiler include paths.

In the target options, select the C/C++ tab, open the Include Paths and add the paths for:

sky66111.c:→ sdk\platform\driver\ rext_sky66111-11_v1.1\sky66111

range_ext_api.h:→ sdk\platform\driver\ rext_sky66111-11_v1.1

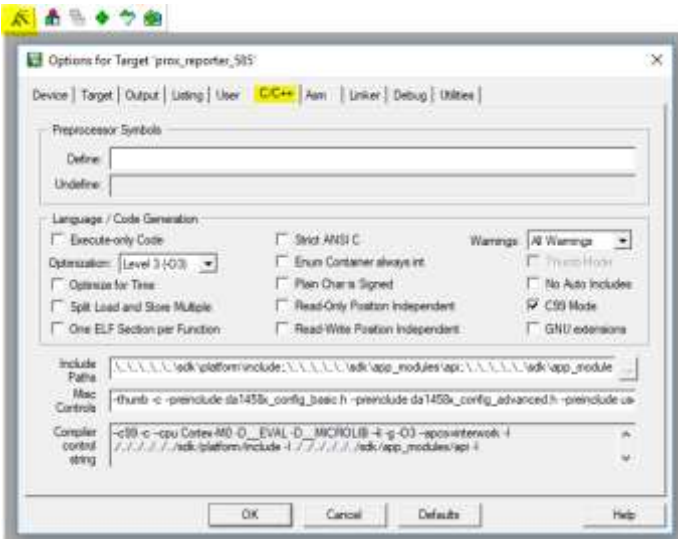


Figure 59: Step 3a, Select target options

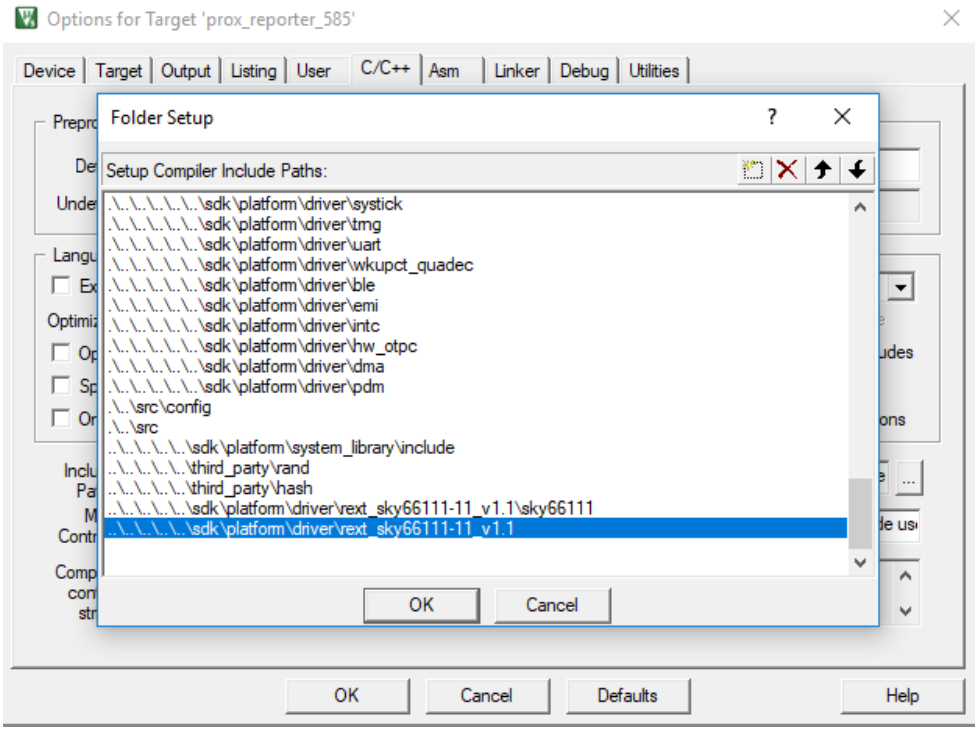


Figure 60: Step 3b, include sky6611.c and range_ext_api.h at the compiler include paths

Step 4: Repeat step 2 and 3 also for timer0.c found in SDK_585\sdk\platform\driver\timer

In the target options, select the C/C++ tab, open the Include Paths and add at the end the path for:

timer0.c → sdk\platform\driver\timer

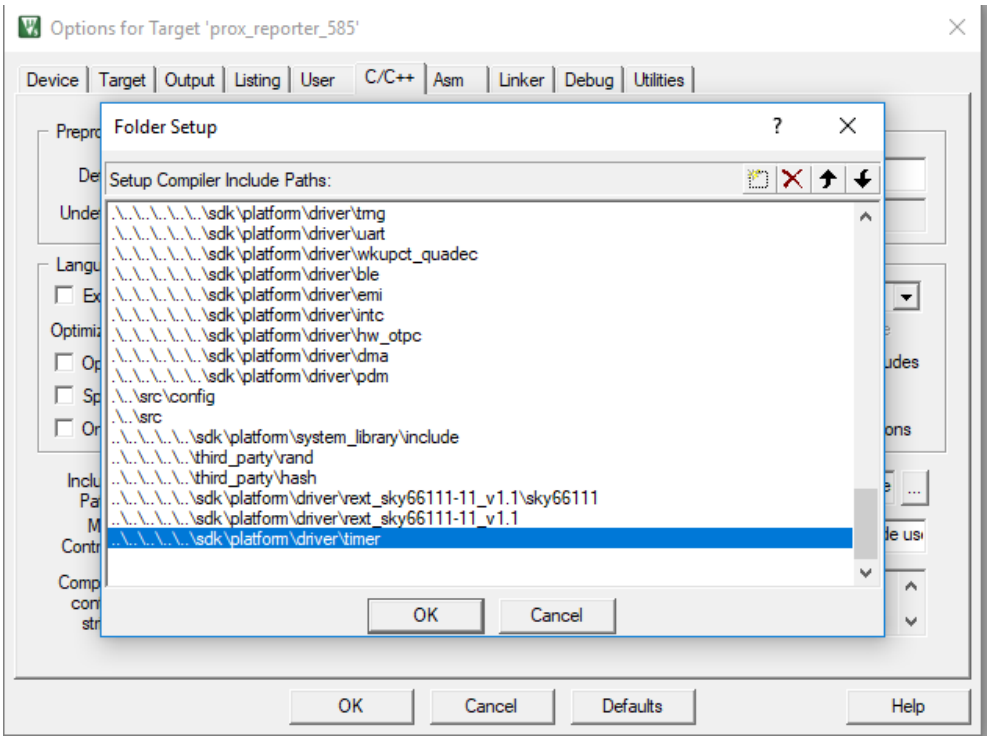


Figure 61: include timer0.c path at the end of compiler include paths

Step 5: In da1458x_config_advanced.h define the CFG_RANGE_EXT parameter. For other projects than proximity reporter this define must be added by user.

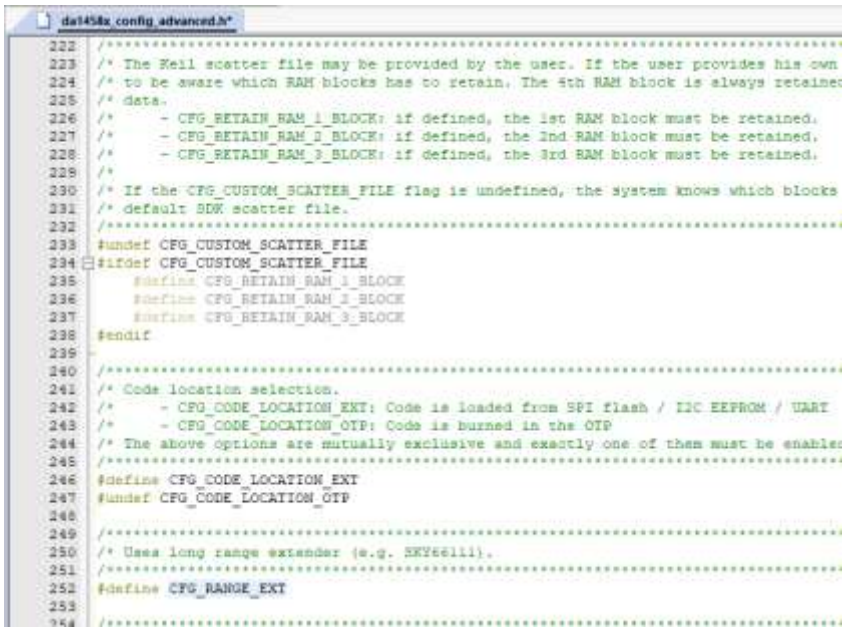


Figure 62: define CFG_RANGE_EXT in da1458x_config_advanced.h

Step 6: Use the desired power level value, as described in sky6611.h preset values, as argument in the range_ext.enable(uint16_t value, NULL). The function is called in the following places:

- Arch_system.c
- user_periph_setup.c

Default value is MAX_POWER

```
850     /*
851      ************************************************************
852      * BLE initialization
853      ************************************************************
854      */
855     init_pwr_and_clk_ble();
856
857     ble_init(_ble_base);
858
859 #if (USE_RANGE_EXT)
860     // Enable range extender
861     range_ext.enable(MAX_POWER, NULL);
862 #endif
```

Figure 63: range_ext.enable() after ble_init() in arch_system.c

```
133 #ifndef CFG_SUOTAR_I2C_DISABLE
134     // Example GPIO configuration for an I2C EEPROM.
135     GPIO_ConfigurePin(I2C_GPIO_PORT, I2C_SCL_PIN, INPUT, PID_I2C_SCL, false);
136     GPIO_ConfigurePin(I2C_GPIO_PORT, I2C_SDA_PIN, INPUT, PID_I2C_SDA, false);
137 #endif
138 #endif //BLE_SUOTA_RECEIVER
139
140 #if (USE_RANGE_EXT)
141     range_ext.enable(MAX_POWER, NULL);
142 #endif
143 }
```

Figure 64: range_ext.enable() at the end of set_pad_functions() in user_periph_setup.c

A.3 Insert driver to prod_test

For inserting the driver to other projects, e.g prod_test, the following steps need to be followed:

1. Repeat steps 1 to 4 described in A.2.

2. For Step 5: add #define CFG_RANGE_EXT in the da1458x_config_advanced.h

3. In the user_periph_setup.c: a) include sky66111.h and b) call range_ext.enable() at the end of set_pad_functions().

4. Repeat Step 6 described in A.2.

```
/*
 * INCLUDE FILES
 ****************************************************************************************
 */

#include "rwip_config.h"         // SW configuration
#include "user_periph_setup.h"   // peripheral configuration
#include "gpio.h"
#include "uart.h"                // UART initialization

#if (USE_RANGE_EXT)
#include "range_ext_api.h"
#include "sky66111.h"
#endif
```

Figure 65: Include sky66111.h in user_periph_setup.c

```
void set_pad_functions(void)
{
#ifdef __DA14586__
    // Disallow spontaneous flash wake-up
    GPIO_ConfigurePin(SPI_EN_GPIO_PORT, SPI_EN_GPIO_PIN, OUTPUT, PID_GPIO, true);
#endif

#if HAS_AUDIO
    init_audio439_gpios(app_audio439_timer_started);
#endif

if (!device_wake_up)
{
    #if defined(CONFIG_UART_GPIOS) // Ports for UART are initialized from external tool
        switch (port_sel)
        {
            case P0_0_AND_P0_1_INITIALIZED_FROM_EXT_TOOL: // Ports for UART P0_0 & P0_1 are initialized from external tool
                update_uart_pads(GPIO_PORT_0, GPIO_PIN_0, GPIO_PORT_0, GPIO_PIN_1);
                break;
            case P0_2_AND_P0_3_INITIALIZED_FROM_EXT_TOOL: // Ports for UART P0_2 & P0_3 are initialized from external tool
                update_uart_pads(GPIO_PORT_0, GPIO_PIN_2, GPIO_PORT_0,GPIO_PIN_3);
                break;
            case P0_4_AND_P0_5_INITIALIZED_FROM_EXT_TOOL: // Ports for UART P0_4 & P0_5 are initialized from external tool
                update_uart_pads(GPIO_PORT_0, GPIO_PIN_4, GPIO_PORT_0, GPIO_PIN_5);
                break;
            case P0_6_AND_P0_7_INITIALIZED_FROM_EXT_TOOL: // Ports for UART P0_6 & P0_7 are initialized from external tool
                update_uart_pads(GPIO_PORT_0, GPIO_PIN_6, GPIO_PORT_0, GPIO_PIN_7);
                break;
            default:
                break;
        }
    #elif (defined(UART1_TX_GPIO_PORT) && defined(UART1_TX_GPIO_PIN) && defined(UART1_RX_GPIO_PORT) && defined(UART1_RX_GPIO_PIN))
        update_uart_pads(UART1_TX_GPIO_PORT, UART1_TX_GPIO_PIN, UART1_RX_GPIO_PORT, UART1_RX_GPIO_PIN);

    #else
        #error "*** No UART pin configuration selected in periph_setup.h ***"
    #endif
    device_wake_up = true;
}

set_pad_uart();

#if (USE_RANGE_EXT)
    // Enable range extender
    range_ext.enable(MAX_POWER, NULL);
#endif

}
```

Figure 66: Call range_ext.enable() at the end of set_pad_functions() in user_periph_setup.c

A.4 Building for different operating modes

In order to build for the different available power levels, the user has to choose between the seven preset values found in sky66111.h and put one as an argument in the range_ext.enable().

- ZERO_DBM for 0 dBm output power
- TWO_DBM for 2 dBm output power
- FOUR_DBM for 4 dBm output power
- SIX_DBM for 6 dBm output power
- EIGHT_DBM for 8 dBm output power
- MAX_POWER for the maximum supported +9.3 dBm output power
- BYPASS for not enabling the sky66111 PA

A.4.1 Example: Building for FOUR_DBM power operation

```
850     /*
851      ********************************************************************************************
852      * BLE initialization
853      ********************************************************************************************
854      */
855     init_pwr_and_clk_ble();
856
857     ble_init(_ble_base);
858
859 #if (USE_RANGE_EXT)
860     // Enable range extender
861     range_ext.enable(FOUR_DBM, NULL);
862 #endif
```

Figure 67: Set FOUR_DBM in range_ext.enable() in arch_system.c

```
110  void set_pad_functions(void)        // set gpio port function mode
111 {
112 #ifdef __DA14586__
113     // disallow spontaneous flash wake-up
114     GPIO_ConfigurePin(SPI_EN_GPIO_PORT, SPI_EN_GPIO_PIN, OUTPUT, PID_GPIO, true);
115 #endif
116
117 #if (BLE_PROX_REPORTER)
118     GPIO_ConfigurePin(GPIO_BUTTON_PORT, GPIO_BUTTON_PIN, INPUT_PULLUP, PID_GPIO, false); // Push Button
119     GPIO_ConfigurePin(GPIO_ALERT_LED_PORT, GPIO_ALERT_LED_PIN, OUTPUT, PID_GPIO, false); //Alert LED
120 #endif
121 #if (BLE_BATT_SERVER && USE_BAT_LEVEL_ALERT)
122     GPIO_ConfigurePin(GPIO_BAT_LED_PORT, GPIO_BAT_LED_PIN, OUTPUT, PID_GPIO, false); //Battery alert LED
123 #endif
124
125 #if (BLE_SUOTA_RECEIVER)
126 #ifndef CFG_SUOTAR_SPI_DISABLE
127     GPIO_ConfigurePin(SPI_EN_GPIO_PORT,  SPI_EN_GPIO_PIN,  OUTPUT, PID_SPI_EN,  true);
128     GPIO_ConfigurePin(SPI_CLK_GPIO_PORT, SPI_CLK_GPIO_PIN, OUTPUT, PID_SPI_CLK, false);
129     GPIO_ConfigurePin(SPI_DO_GPIO_PORT,  SPI_DO_GPIO_PIN,  OUTPUT, PID_SPI_DO,  false);
130     GPIO_ConfigurePin(SPI_DI_GPIO_PORT,  SPI_DI_GPIO_PIN,  INPUT,  PID_SPI_DI,  false);
131 #endif
132
133 #ifndef CFG_SUOTAR_I2C_DISABLE
134     // Example GPIO configuration for an I2C EEPROM.
135     GPIO_ConfigurePin(I2C_GPIO_PORT, I2C_SCL_PIN, INPUT, PID_I2C_SCL, false);
136     GPIO_ConfigurePin(I2C_GPIO_PORT, I2C_SDA_PIN, INPUT, PID_I2C_SDA, false);
137 #endif
138 #endif //BLE_SUOTA_RECEIVER
139
140 #if (USE_RANGE_EXT)
141     range_ext.enable(FOUR_DBM, NULL);
142 #endif
143 }
144
```

Figure 68: Set FOUR_DBM in range_ext.enable() in user_periph_setup.c

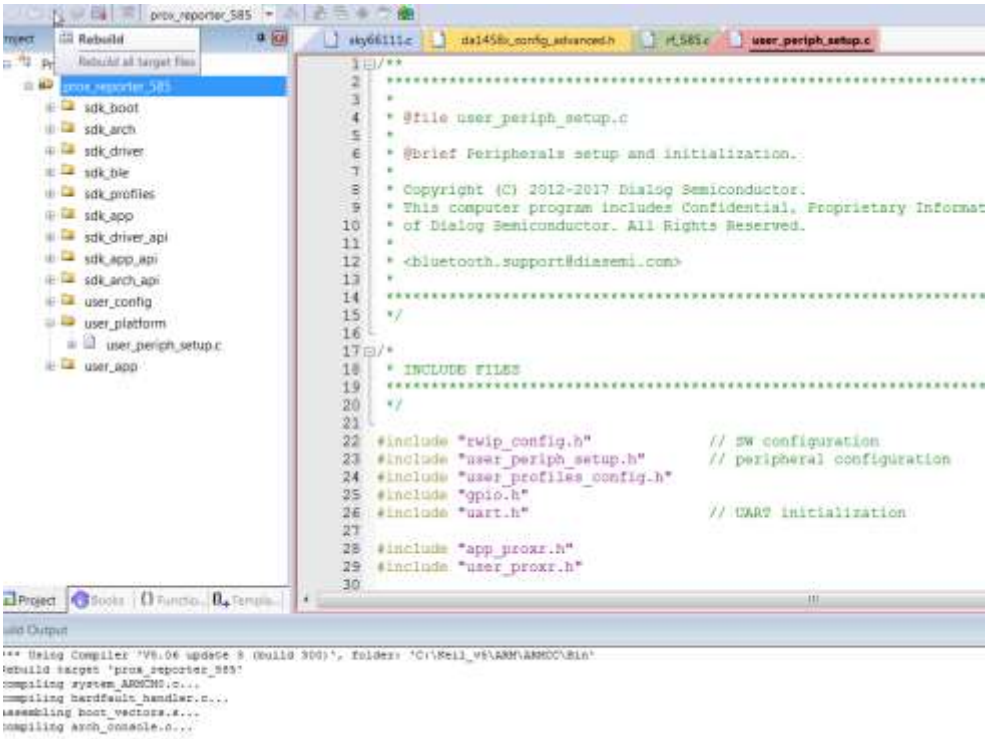


Figure 69: Build project in order to produce the FOUR_DBM hex file

Appendix B Optimizing PWM Current Consumption

For optimized power consumption during PWM mode it is proposed that the Q2 base resistor should be increased from the default value. In order to keep the same time constant of 100us R2=10K and C22=10nF can be used. For other time constants appropriate values should be chosen accordingly. The larger resistor reduces the transistor base current resulting to lower power average power consumption during PWM mode.

For the same TX output power an increase in the duty cycle is necessary (see Table 30).

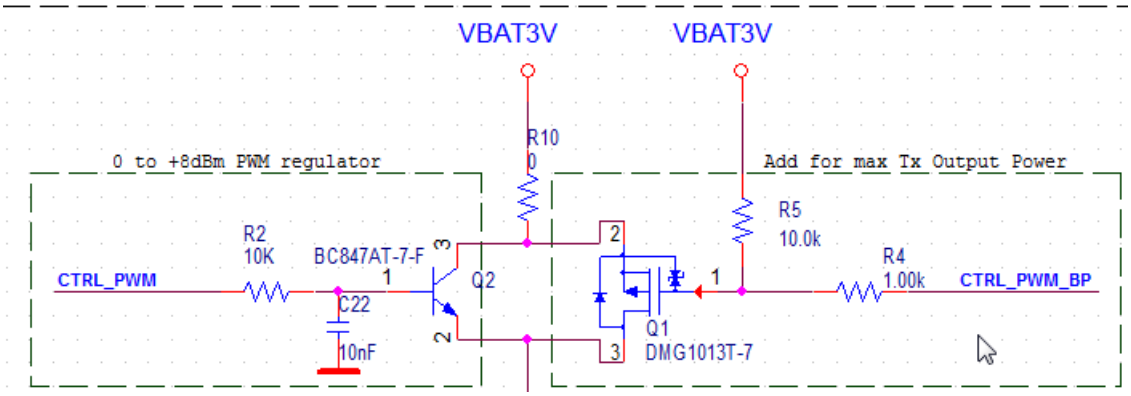


Figure 70: PWM optimized RC circuit

Table 30: SKY66111-11 modified PWM Duty Cycle for R2=10K, C22=10nF

Power Mode	PWM Operation	Duty Cycle (%)
BYPASS	No	-
ZERO_DBM	Yes	47
TWO_DBM	Yes	53
FOUR_DBM	Yes	63
SIX_DBM	Yes	75
EIGHT_DBM	Yes	92
MAX_POWER	No	-

Advertising Mode

For this measurement the DUT was supplied by 3 V. FW was downloaded and the JTAG programmer and then it was disconnected from the motherboard.

Table 31: Current consumption during Advertising Mode (R2=10K, C22=10nF) (Note 22)

	Average charge per active state per interval (uC)	Average current for capture (uA)	Peak current (mA)	Peak power (uW)
Power Level (dBm)				
BYPASS	14.12	13.10	5.54	0.02
0	17.50	15.38	8.55	0.03
+2	18.35	15.91	9.25	0.03
+4	19.23	16.46	9.92	0.03
+6	20.36	17.24	10.97	0.03
+8	22.57	18.72	12.91	0.04
+9.3	25.90	20.93	14.86	0.04

Note 22 Power supply= 3V, T=25ºC, advertising interval=1500ms, adv_pdu=9 bytes, intervals captured=80.

Connection Mode

For this measurement the DUT was supplied by 3 V. FW was downloaded and the JTAG programmer was disconnected and connection with an iPhone 4S was established with 400ms connection interval.

Table 32: Current consumption during Connection Mode (R2=10K, C22=10nF) (Note 23)

	Average charge per active state per interval (uC)	Average current for capture (uA)	Peak current (mA)	Peak power (uW)
Power Level (dBm)				
BYPASS	7.66	22.88	5.55	0.02
0	7.31	22.03	8.40	0.03
+2	7.43	22.28	8.88	0.03
+4	7.32	22.01	9.49	0.03
+6	7.39	22.21	10.54	0.03
+8	7.43	22.29	12.08	0.04
+9.3	8.89	25.98	14.85	0.04

Note 23 Power supply= 3C, T=25ºC, connection interval=400ms, mtu=23 bytes, intervals captured=300.

Revision History

Revision	Date	Description
1.0	12-Dec-2017	Initial version.
1.1	01-Aug-2019	Update Appendix A Application Software Guide with changes in sky66111 driver. Update SDK revision used to SDK 6.0.10.
1.2	19-Jan-2022	Updated logo, disclaimer, copyright.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.