

User Manual

Advanced Analog GreenPAK Evaluation Board

UM-GP-005

Abstract

This user manual provides basic information on using the evaluation board for Advanced Analog GreenPAK in order to test silicon samples from Renesas Electronics Corporation. This document provides the hardware schematic that can assist in building a variety of test circuits. In addition, it describes multiple software methodologies to interface with the system using the GreenPAK Designer software.

Contents

Abstract	1
Contents	2
Figures	3
Tables	3
1 Terms and Definitions	4
2 References	4
3 Getting Started	5
3.1 Hardware.....	5
3.2 GreenPAK Development Tools and Designer Software	5
3.3 Additional Resources	6
4 Hardware	7
4.1 Overview	7
4.1.1 Power Supply.....	7
4.1.2 Test Points.....	8
4.1.3 SLG47004 Pin Connection Header	8
4.2 EVB Section Descriptions	9
4.2.1 OpAmp 0/1 Sections.....	9
4.2.2 Rheostat 0/1 Sections.....	9
4.2.3 Analog Switch 0/1 Sections	10
4.3 Software Interfaces	11
4.3.1 Advanced Development Platform	11
4.3.2 GreenPAK Serial Debugger/I ² C.....	13
5 Application Examples	14
5.1 Instrumentation Amplifier	14
Appendix A Evaluation Board Documentation	16
A.1 Schematic	16
A.2 SLG47004 Evaluation Board Images.....	17
A.3 Dimensions	18
A.4 Bill of Materials	19
Revision History	20

Figures

Figure 1: SLG47004 Evaluation Board, Section Map	7
Figure 2: Development Platform Selector	12
Figure 3: GreenPAK ADB Debugging Controls Window	12
Figure 4: GSD Debugging Controls Window	13
Figure 5: Instrumentation Amplifier Schematic.....	14
Figure 6: Schematic Diagram	16
Figure 7: Top Silk, 3D View	17
Figure 8: Top Silk	17
Figure 9: SLG47004 Evaluation Board Dimensions.....	18

Tables

Table 1: GreenPAK Support Resources	6
Table 2: Test Point Information	8
Table 3: OpAmp TP List	9
Table 4: Rheostat TP List	10
Table 5: Analog Switch TP List	10
Table 6: SV1 & SV2 Header Functions	11
Table 7: P2 & P3 Header Functions	13
Table 8: Instrumentation Amplifier Build Configuration	15
Table 9: Bill of Materials	19

1 Terms and Definitions

AA PAK	Advanced Analog PAK
ACMP	Analog Comparator
ADB	Advanced Development Board
AS	Analog Switch
BOM	Bill of Materials
EVB	Evaluation Board
IC	Integrated Circuit
InAmp	Instrumentation Amplifier
GPAK	GreenPAK
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GSD	GreenPAK Serial Debugger
MTP	Multiple-Time Programmable
NVM	Non-Volatile Memory
OpAmp	Operational Amplifier
PCB	Printed Circuit Board
RH	Rheostat
QTY	Quantity
SMD	Surface Mounted Device
TP	Test Point
VREF	Voltage Reference

2 References

- [1] SLG47004, Datasheet - <https://www.renesas.com/SLG47004#documents>.
- [2] GreenPAK Designer User Guide - <https://www.renesas.com/software-tool/go-configure-software-hub#document>.
- [3] UM-GP-002, GreenPAK Advanced Development Platform, User Manual - <https://www.renesas.com/SLG4DVKADV#documents>.
- [4] UM-GP-004, GreenPAK Serial Debugger, User Manual - <https://www.renesas.com/SLG4DVKGSD#documents>.
- [5] I2C-Bus Specification and User Manual, User Manual UM10204–Rev.6, NXP, 4 April 2014. <https://www.nxp.com/docs/en/user-guide/UM10204.pdf>

3 Getting Started

This user manual provides information on using the AA PAK Evaluation Board.

Section 3 helps to familiarize the User with the development process by introducing the GreenPAK product family and providing additional resources on obtaining the hardware, downloading the software, and finding additional support from Renesas Electronics Corporation.

In Section 4, this document describes the evaluation board hardware by breaking down the board into sections centered around key features such as the opamps, the rheostats, and the analog switches. This section also explains some of the nuances for controlling the evaluation board using the GreenPAK software interface.

Section 5 introduces a variety of common application example configurations for the evaluation board.

3.1 Hardware

The AA PAK Evaluation Board can be purchased from Renesas's webstore. A link to the store is provided in Table 1. By default, the SLG47004 Evaluation Boards come populated with the BOM items listed in Appendix A.

3.2 GreenPAK Development Tools and Designer Software

Although one can configure the SLG47004 with any I²C controller, we recommend using the GreenPAK Designer software with either the GreenPAK Advanced Development Platform or the GreenPAK Serial Debugger for initial evaluation. Renesas's development tools and software support platform provide an easy-to-use and tested ecosystem for evaluating the functionality of the Advanced Analog GreenPAK IC.

Table 1 contains links to the GreenPAK Designer software, the GreenPAK Development Tools selector, and Renesas's webstore. Refer to Section 4.3 for more information on using the GreenPAK Advanced Development Board and the GreenPAK Serial Debugger.

For more information on using your own I²C controller to interface with the SLG47004 on the AA PAK's Evaluation Board, please refer to the I²C and NVM sections of the SLG47004's base die datasheet. For additional support, please reach out to your local FAE or contact us on Renesas's customer support forum.

3.3 Additional Resources

Renesas provides a variety of additional resources to support our customers in their GreenPAK development process. Some of these resources are tailored towards introducing mixed-signal design techniques and application spaces, while others provide a venue for technical questions and customer engagement. Refer to [Table 1](#) for more information.

Table 1: GreenPAK Support Resources

GreenPAK Resource	Description
SLG47004 Product Page	Access to the SLG47004's datasheet and errata list. Other resources found on this site include links to the webstore, the GreenPAK Designer software, the GreenPAK Development Tools selector, and a variety of AA PAK-specific application notes.
GreenPAK Designer Software	Renesas's GreenPAK development software and user guide.
GreenPAK Cookbook	Commonly used GreenPAK techniques and applications compiled into a digital notebook. The cookbook recipes are designed to be simple so that multiple techniques can be combined into more unique and complex mixed-signal solutions.
GreenPAK Application Notes	A variety of GreenPAK Application Notes containing both application examples and GreenPAK design techniques.
GreenPAK Training Videos	Video resources ranging from Renesas's "Getting Started with GreenPAK" series to in-depth webinars on applications such as motor control, sensor interfaces, and load switches. This website also contains access to Renesas Electronics Corporation's online training course.
Renesas Support Website	General technical support site for contacting Renesas Electronics Corporation. The website contains links for Renesas's support forum, information about local sales offices, and general inquiry forms for customer requests.
Renesas Forum	A support forum for customer questions monitored by Renesas Applications Engineers.

4 Hardware

4.1 Overview

When creating this tool, Renesas focused on designing a flexible solution to support the evaluation of a variety of circuit applications. Refer to Section 5 for a few examples. Strategic connections have been provided via the boards layout to integrate many of the SLG47004's key macrocells into one system. Note that this board has not been optimized to evaluate the performance of layout-dependent systems.

Figure 1 shows an image of the SLG47004 Evaluation Board with all components placed on the board. In most scenarios, customers will receive the Evaluation Boards populated only with the BOM items listed in Appendix A. This allows the customer to configure the circuit to fit the desired application.

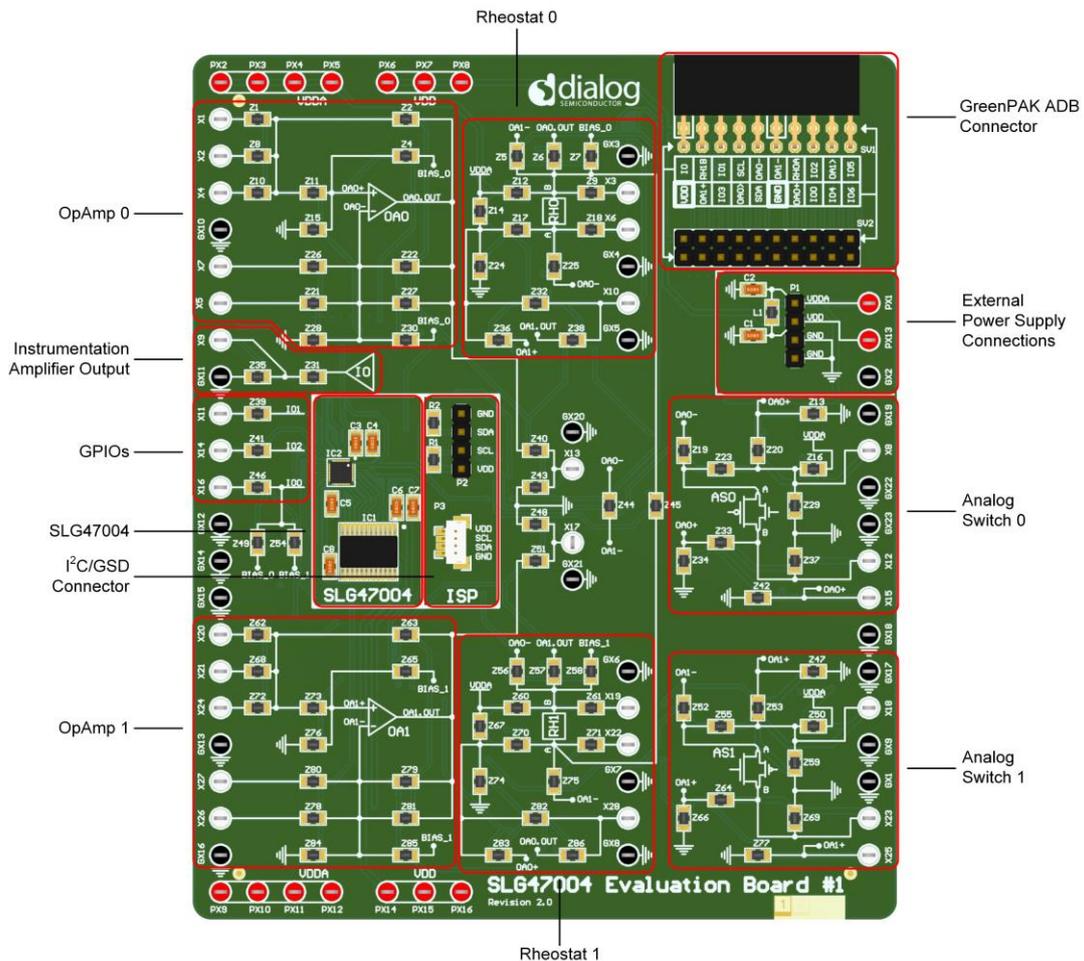


Figure 1: SLG47004 Evaluation Board, Section Map

4.1.1 Power Supply

Power can be applied to the evaluation board using the following sources:

- GreenPAK ADB - leverages the onboard power supply built into the GreenPAK Advanced Development platform to deliver up to 5.5 V. For more information, refer to the GreenPAK ADB's user guide found in Section 2.
- GreenPAK Serial Debugger - an LDO-regulated power supply ranging from 0.9 V to 5.0 V at a maximum current of 100 mA. Refer to Section 2 for the GSD's quick start guide.
- External Power Supply & "PX#" Test Points - connection headers for using an external power supply ranging from 2.5 V to 5.5 V. The P1 connection header includes an LC filter designed to isolate the analog and digital voltage rails for optimized noise performance.

4.1.2 Test Points

Various TPs spread across the PCB allow for injecting input signals and monitoring output voltages throughout the system. [Table 2](#) provides a brief summary on the TP naming scheme. Additional application-specific descriptions on the “X#” TP functions can be found throughout [Section 4.2](#).

Table 2: Test Point Information

Label	Color	Function
PX#	Red	V _{DD} & V _{DDA} power rail connections.
GX#	Black	GND reference nodes.
X#	White	Tps for signal injection and output monitoring.

4.1.3 SLG47004 Pin Connection Header

Most pins on the SLG47004 can be monitored using the SV2 header on the evaluation board. Refer to [Table 6](#) for more information on the function of each individual node.

4.2 EVB Section Descriptions

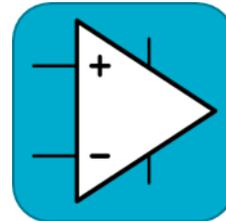
The evaluation board separates the key features of AA PAK into spatially grouped sections on the PCB. These features include the OpAmp, the rheostats, and the analog switches. The information below provides application ideas and lists the associated TP connections for each section. Note that many of these test points interact with multiple features.

Refer to Section 5 for specific application examples that demonstrate how to leverage the EVB's circuit layout to build a variety of different circuits.

4.2.1 OpAmp 0/1 Sections

The EVB layout provides easy access to configure the OpAmp devices into a variety of different common topologies including the following:

- Voltage Follower
- Inverting, Non-Inverting Amplifier
- Summing, Difference Amplifier
- Instrumentation Amplifier
- Integrator, Differentiator
- Active Filters (Sallen-Key, Multiple Feedback)
- Transimpedance Amplifier



Cross reference the list of OpAmp test points in Table 3 with the image of the EVB's silkscreen shown in Figure 1.

Table 3: OpAmp TP List

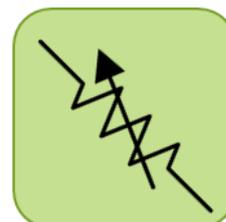
Section	IO	TP List
OpAmp 0	Input	X1, X2, X4, X5, X7, X15
	Output	X13, X28
OpAmp 1	Input	X20, X21, X24, X25, X26, X27
	Output	X10, X17
InAmp	Output	X9

4.2.2 Rheostat 0/1 Sections

The rheostat section of the EVB contains a variety of optional connections to V_{DDA} , GND, the OpAmp Inputs/Outputs, and the EVB's bias nodes. These connections can be made through the SMD footprints by using a combination of resistors and short circuits connections. For Auto-Trim applications not using the OpAmp outputs, external wires can be used to connect the rheostat TPs directly to either of the Chopper ACMP inputs at IO1 and IO4.

A few rheostat example applications include:

- Vref Generation
- Amplifier Offset Trim
- Amplifier Gain Trim
- Filter Frequency Trim



The test points associated with each rheostat are shown in Table 4.

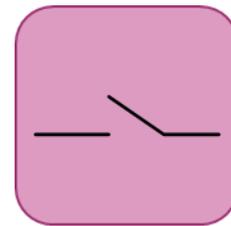
Table 4: Rheostat TP List

Section	TP List
Rheostat 0	X3, X6, X10
Rheostat 1	X19, X22, X28

4.2.3 Analog Switch 0/1 Sections

The rail-to-rail analog switches within AA PAK are unique in that AS0 has been optimized for high-side performance while AS1 has been designed for low-side applications. This flexibility provides a variety of different applications spaces including the examples listed below:

- High-Side, Low-Side Switch
- Current Source, Sink
- Voltage Regulation
- Half Bridge
- Sample and Hold Circuit



Similar to the rheostats, there are additional connection options available to connect the AS devices to V_{DDA} , GND, and the OpAmp Inputs/Outputs. Refer to [Table 5](#) for a list of test points associated with each analog switch.

Table 5: Analog Switch TP List

Section	TP List
Analog Switch 0	X8, X12
Analog Switch 1	X18, X23

Advanced Analog GreenPAK Evaluation Board
4.3 Software Interfaces

The evaluation board contains multiple avenues to interact with the SLG47004. The sections below provide more information on using Renesas's software interfaces and hardware tools to emulate and program the register cells within the SLG47004 using the I²C protocol. In addition, the GreenPAK Advanced Development Platform features on-board signal and logic generators for convenient testing of the AA PAK design configuration with the supporting external circuitry.

4.3.1 Advanced Development Platform

The AA PAK evaluation board can be connected to the GreenPAK ADB using the SV1 connector. This connector matches with the expansion connector on the GreenPAK ADB. Refer to [Table 6](#) for more information on the function of each individual node on SV1.

Table 6: SV1 & SV2 Header Functions

Header	Silk Label	Pin # (STQFN-24L)	Function
SV 1.1 SV 2.1	V _{DD}	13	Digital Power Supply
SV 1.2 SV 2.2	IO	21	GPI, InAmp Output
SV 1.3 SV 2.3	OA1+	23	OpAmp 1 - Non-inverting Input
SV 1.4 SV 2.4	RH1B	9	Digital Rheostat 1 - Terminal B
SV 1.5 SV 2.5	IO3	17	GPIO, Analog Switch 1 - Input A, ACMP 1 - Positive Input, Slave Address 2
SV 1.6 SV 2.6	IO1	15	GPIO, Chopper ACMP - Positive Input, Temperature Sensor Output, External Clock Connection, Slave Address 0
SV 1.7 SV 2.7	OA0>	5	OpAmp 0 - Output, ACMP 0 - Positive Input
SV 1.8 SV 2.8	SCL	10	I ² C Serial Clock
SV 1.9 SV 2.9	SDA	11	I ² C Serial Data
SV 1.10 SV 2.10	OA0-	3	OpAmp 0 - Inverting Input
SV 1.11 SV 2.11	GND	14	Digital Ground, Analog Ground
SV 1.12 SV 2.12	OA1-	24	OpAmp 1 - Inverting Input
SV 1.13 SV 2.13	OA0+	4	OpAmp 0 - Non-inverting Input
SV 1.14 SV 2.14	RH0A	6	Digital Rheostat 0 - Terminal A
SV 1.15 SV 2.15	IO0	12	GPIO, ACMP 0/1 - Negative Input, External Clock Connection, Vref 0 Output
SV 1.16 SV 2.16	IO2	16	GPIO, ACMP 0 - Positive Input, External Clock Connection, Slave Address 1
SV 1.17 SV 2.17	IO4	18	GPIO, Analog Switch 1 - Input B, Chopper ACMP - Negative Input, Slave Address 3
SV 1.18 SV 2.18	OA1>	22	OpAmp 1 - Output, ACMP 1 - Positive Input
SV 1.19 SV 2.19	IO6	20	GPIO, Analog Switch 0 - Input A, High Drive Buffer Output, InAmp Vref
SV 1.20 SV 2.20	IO5	19	GPIO, Analog Switch 0 - Input B

To connect the GreenPAK Designer Software to the SLG47004 evaluation board using the GreenPAK ADB, follow the procedure shown below:

1. Open an instance of the GreenPAK Designer software for the SLG47004.

Advanced Analog GreenPAK Evaluation Board

2. Connect the GreenPAK ADB to your computer with the included USB cable.
3. Attach the expansion connector on the GreenPAK ADB to the SV1 header on the SLG47004 evaluation board.
4. Open the “Debug” tool within the GreenPAK Designer software and select the “GreenPAK Advanced Development Platform”. If this window does not appear, click the “Change Platform” button in the “Debugging Controls” window.

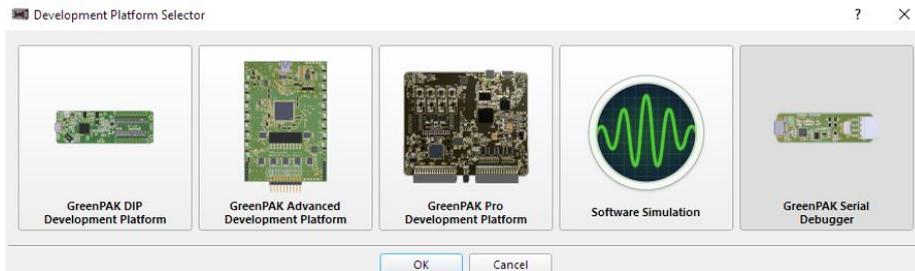


Figure 2: Development Platform Selector

5. Change the “Device:” dropdown selection to the appropriate I²C control code. By default, all SLG47004 devices are configured with a control code of 0001 which corresponds to the “External: 0001” option in the list.
6. Select “Ext. VDD” or “Va” to connect the GreenPAK ADB’s V_{DD} signal generator to the evaluation board. Note that this step should be skipped when using another voltage source to power the evaluation board.
7. Click the “Emulation” or “Program” buttons to load the GreenPAK Designer’s current configuration onto the SLG47004 device.

Figure 3 shows the baseline configuration for the “Debugging Controls” window while emulation is running. Additional connections from the GreenPAK ADB to the SLG47004 can be made by enabling the expansion connector switches for the desired pin.

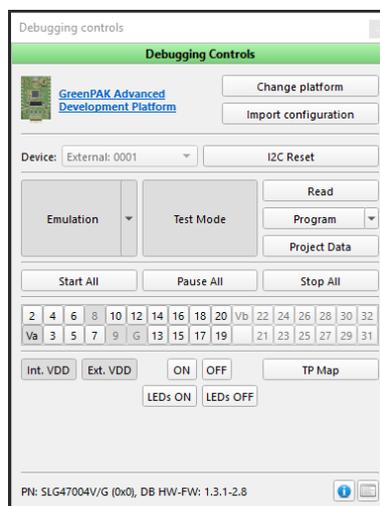


Figure 3: GreenPAK ADB Debugging Controls Window

For more information on configuring the function generators, enabling the expansion connector switches, and working with the GreenPAK Designer software, please refer to the GreenPAK Designer software and the GreenPAK Advanced Development Platform user manuals.

4.3.2 GreenPAK Serial Debugger/I²C

The GreenPAK Serial Debugger provides a simple I²C interface between the GreenPAK Designer software and the AA PAK evaluation board. The GSD tool requires four signals as shown in [Table 7](#). These connections to the evaluation board can be made using either the P2 or the P3 headers.

The GSD comes equipped with two 1 kΩ pull-up resistors. The R1 and R2 pull-up resistor footprints on the AA PAK evaluation board provide additional flexibility for using an external I²C controller.

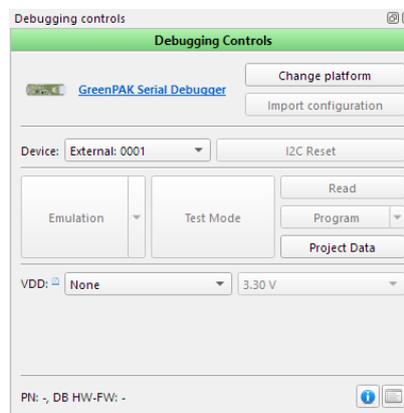
Table 7: P2 & P3 Header Functions

Header	Silk Label	Pin # (STQFN-24L)	Function
P 2.1 P 3.1	V _{DD}	13	Digital Power Supply
P 2.2 P 3.2	SCL	10	I ² C Serial Clock
P 2.3 P 3.3	SDA	11	I ² C Serial Data
P 2.4 P 3.4	GND	14	Digital Ground

Follow the procedure below to connect the GreenPAK Designer software to the SLG47004 evaluation board using the GSD:

1. Open an instance of the GreenPAK Designer software for the SLG47004.
2. Connect the GSD to your computer with the included USB cable.
3. Attach the GSD to the SLG47004 evaluation board using either the P2 or P3 headers.
4. Open the “Debug” tool within the GreenPAK Designer software and select the “GreenPAK Serial Debugger”. If the window in [Figure 2](#) does not appear, click the “Change Platform” button in the “Debugging Controls” window.
5. Change the “Device:” dropdown selection to either “Auto Detect” or to the appropriate external I²C control code. By default, all SLG47004 devices are configured with a control code of 0001 which corresponds to the “External: 0001” option in the list.
6. Select “Int. VDD” to connect the GSD’s V_{DD} signal generator to the evaluation board. The supply voltage level can then be selected in the adjacent dropdown window. When using an external V_{DD} on the AA PAK evaluation board, make sure to select “Ext. VDD” in the “Debugging Controls” window.
7. Click the “Emulation” or “Program” buttons to load the GreenPAK Designer’s current configuration onto the SLG47004 device.

[Figure 4](#) shows an example configuration for the “Debugging Controls” window while emulation is running.


Figure 4: GSD Debugging Controls Window

For more information on the hardware and software tools, please refer to the GreenPAK Designer software and the GreenPAK Serial Debugger user manuals.

5 Application Examples

The key features of the SLG47004 can be combined on a system-level to implement a variety of different applications. A few examples include instrumentation amplifiers, active filtering, digital potentiometers, voltage regulation, and variable current sources.

The sections below provide EVB configurations for a few of the examples provided above. The examples below can be tailored for specific applications by modifying the layout of the schematic or by selecting different component values.

5.1 Instrumentation Amplifier

The SLG47004 can be configured as an InAmp with trimmable gain and offset voltage. One configuration of the standard 3-OpAmp topology is implemented in the EVB's layout as shown below.

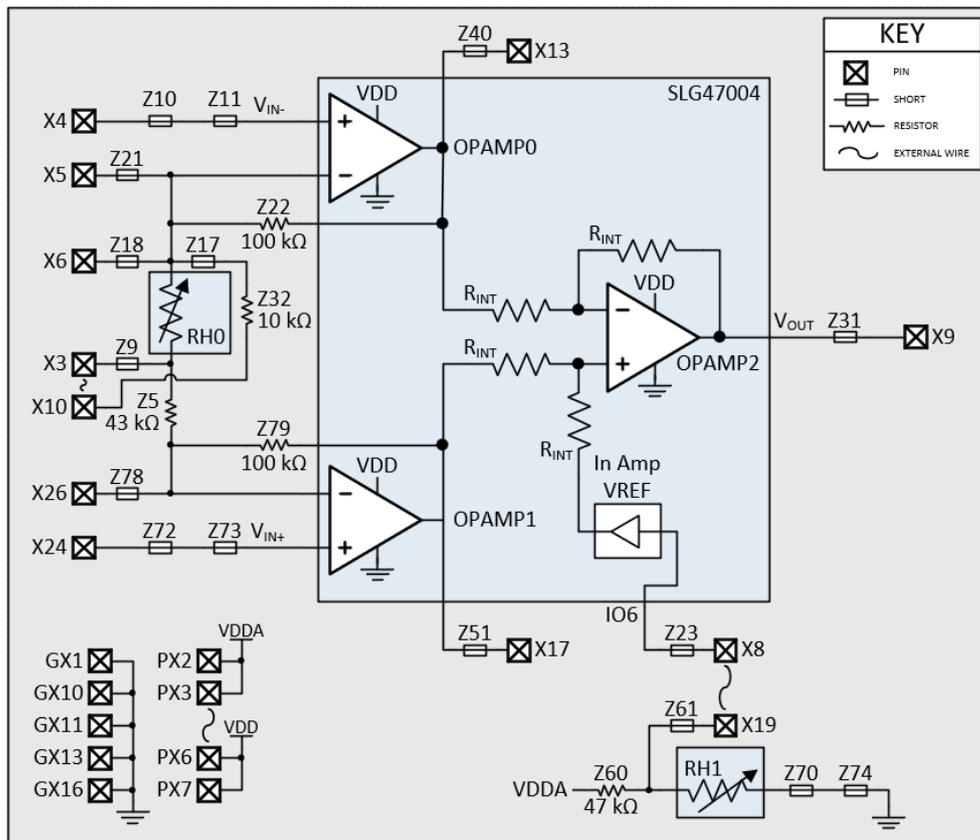


Figure 5: Instrumentation Amplifier Schematic

This Instrumentation Amplifier configuration combines the OpAmp and the digital rheostat structures into one system. RH0 impacts the differential gain, while RH1 modifies the reference voltage. The equations below can be used to calculate the output voltage of the overall system.

$$V_{OUT} = (V_{IN+} - V_{IN-}) * Gain + V_{REF}$$

$$Gain = 1 + \frac{2 * R_F}{R_G} \dots \text{where } R_F = 100 \text{ k}\Omega, R_G = 43 \text{ k}\Omega + (RH0 \parallel 10 \text{ k}\Omega)$$

$$V_{REF} = \frac{RH1}{RH1 + 47 \text{ k}\Omega}$$

The InAmp in Figure 5 is designed to introduce a differential gain of 5V/V. RH0 is placed in parallel with the 10 kΩ resistor such that the equivalent impedance can be trimmed to accommodate for circuit tolerance variations throughout the system (IE: Resistor Tolerances, Input Offset Voltage, and others).

Table 8 shows the components used to build this example. Note that the component selection and schematic layout can be modified to achieve different amounts of gain and offset.

Table 8: Instrumentation Amplifier Build Configuration

#	Function	Value	Designator	QTY
1	Non-Inverting Input (VIN+)	-	X24	1
2	Inverting Input (VIN-)	-	X4	1
3	InAmp Vref	-	X8	1
4	Output	-	X9	1
5	Gain Resistor - Series	43 kΩ	Z5	1
6	Gain Resistor - Parallel	10 kΩ	Z32	1
7	Feedback Resistor	100 kΩ	Z22, Z79	2
8	Reference Voltage Divider	47 kΩ	Z60	1
9	Shorts	-	Z9, Z10, Z11, Z17, Z18, Z21, Z23, Z31, Z40, Z51, Z61, Z70, Z72, Z73, Z74, Z78	15
10	Additional Headers	-	GX1, GX10, GX11, GX13, GX16 PX2, PX3, PX6, PX7 X3, X5, X6, X10, X13, X17, X19, X26	16

Although this implementation focuses on fine tuning the gain to a specific level, other topologies support a wider range of gain similar in functionality to that of a programmable gain amplifier. The InAmp can also be implemented without the use of the digital rheostats.

Appendix A Evaluation Board Documentation

A.1 Schematic

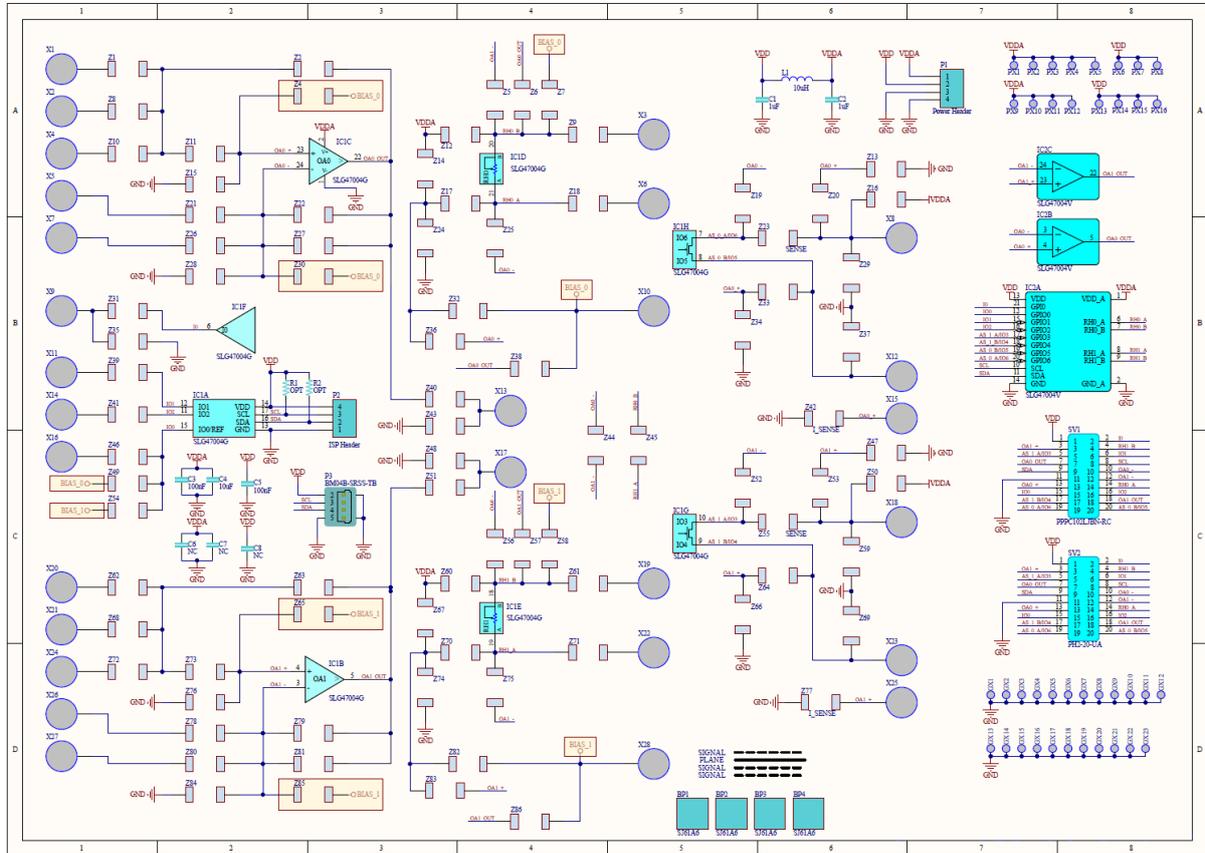


Figure 6: Schematic Diagram

A.2 SLG47004 Evaluation Board Images

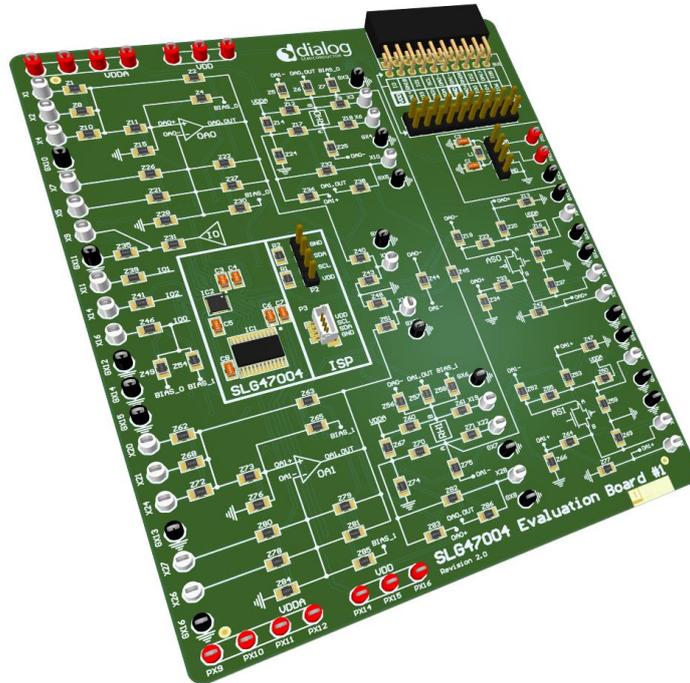


Figure 7: Top Silk, 3D View

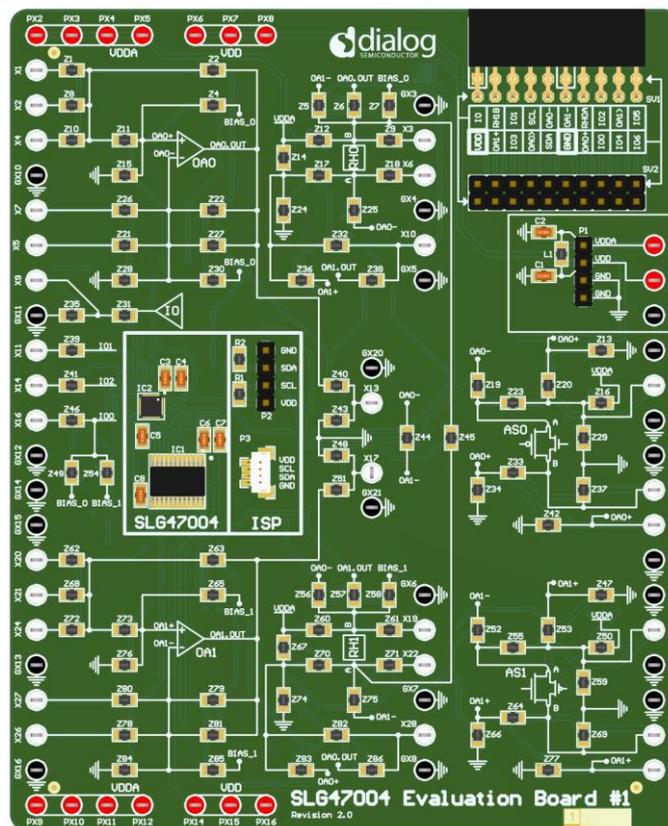


Figure 8: Top Silk

A.3 Dimensions

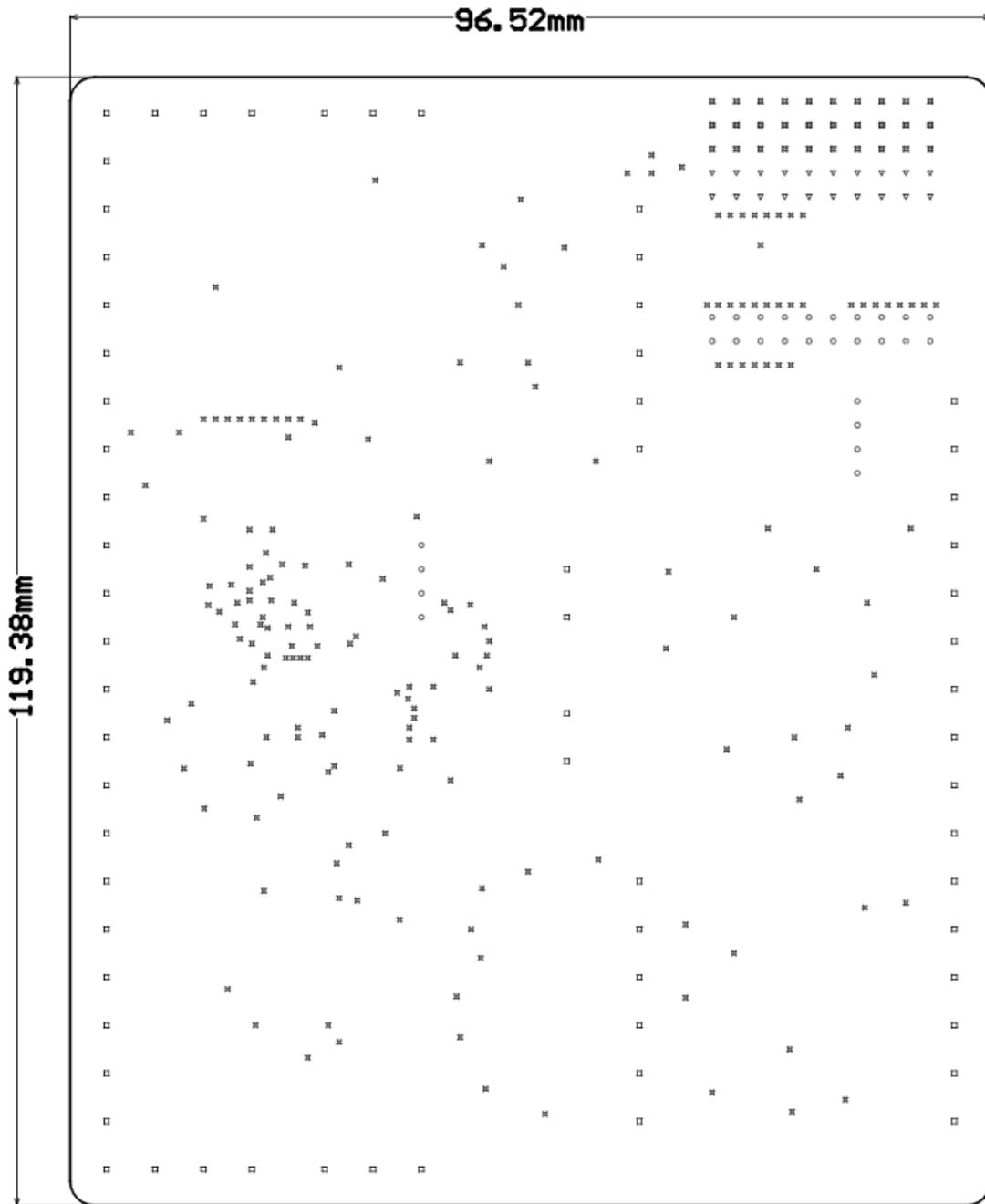


Figure 9: SLG47004 Evaluation Board Dimensions

A.4 Bill of Materials
Table 9: Bill of Materials

#	Designator	Description	Manufacturer	Part Number	Digi-Key	QTY
1	IC2	Advanced Analog GreenPAK IC, MSTQFN-24, 3.0x3.0mm	Renesas Electronics Corporation	SLG47004V	-	1
2	C3, C5	100nF Ceramic Capacitor, 50V, X7R, 0805	Kemet	C0805C104K5RACTU	399-1170-1-ND	2
3	C4	10uF Ceramic Capacitor, 16V, X5R, 0805	Murata Electronics	GRM21BR61C106KE15L	490-3886-1-ND	1
4	P1, P2	4POS Through Hole Connection Header (1x4), 0.1" (2.54mm) Spacing	TE Connectivity	826629-4	A106750-ND	2
5	P3	4POS SMD Connection Header (1x4), 0.039" (1.0mm) Spacing	JST Corporation	BM04B-SRSS-TB(LF)(SN)	455-1790-1-ND	1
6	C1, C2	1uF Ceramic Capacitor, 50V, X7R, 0805	Samsung Electro-Mechanics	CL21B105KBFNNG	1276-6470-1-ND	2
7	L1	10uH Shielded Multilayer Inductor, 500mA, 300mΩ, 0805	TDK Corporation	MLZ2012N100LT000	445-6762-1-ND	1
8	PX1, PX13	Test Point - Red, 0.04" (1.02mm) Spacing	Keystone Electronics	5000	36-5000-ND	2
9	GX2	Test Point - Black, 0.04" (1.02mm) Spacing	Keystone Electronics	5001	36-5001-ND	1
10	SV1	20POS Through Hole Connection Header - Right Angle (2x10), 0.1" (2.54mm) Spacing	Sullins Connector Solutions	PPPC102LJBN-RC	S5563-ND	1
11	SV2	20POS Through Hole Connection Header (2x10), 0.1" (2.54mm) Spacing	Adam Tech	PH2-20-UA	2057-PH2-20-UA-ND	1
12	BP1, BP2, BP3, BP4	Bumper	3M Company	SJ61A6	SJ61A6-ND	4

Note 1 Customer evaluation boards may include additional components not listed in the BOM above.

Revision History

Revision	Date	Description
1.2	21-Mar-2022	Renesas rebranding
1.1	8-Sep-2021	Updated hyperlinks
1.0	28-Oct-2020	Initial version

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

RoHS Compliance

Renesas Electronics Corporation's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.