

Register Descriptions

The register descriptions section describes the behavior and function of the customer-programmable non-volatile-memory registers in the VersaClock 6E family of clock generators. [Table 1](#) showcases the array of products under the VersaClock 6E family.

Table 1. VersaClock 6E Family Products

| Product | Description | Package |
|-----------|--|---------|
| 5P49V6965 | 5-Output VersaClock 6E | 24 pins |
| 5P49V6967 | 8-Output VersaClock 6E with 4 LP-HCSL Outputs | 40 pins |
| 5P49V6968 | 12-Output VersaClock 6E with 8 LP-HCSL Outputs | 48 pins |
| 5P49V6975 | 5-Output VersaClock 6E with Internal Crystal | 24 pins |

For details of product operation, refer to the product datasheet.

VersaClock 6E Family Register Set

The device contains volatile (RAM) 8-bit registers and non-volatile 8-bit registers ([Figure 1](#)). The non-volatile registers are One-Time Programmable (OTP), and bit values can only be changed from 1 (unburned state) to 0.

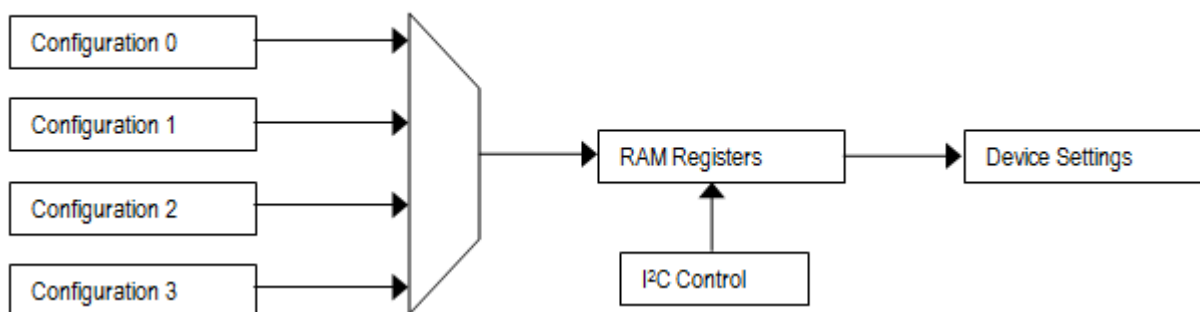
The OTP registers include factory trim data and four user configuration tables ([Figure 1](#), [Table 3](#)). This document does not describe the format or methods for programming factory trim data, which is programmed by the factory before shipment.

Each configuration table contains all the information to set up the device's output frequencies. When these configuration tables are programmed, the device will automatically load the RAM registers with the desired configuration on power-up. The device initializes in either I²C mode or selection-pin mode, depending on the state of the OUT0/SELB_I2C pin on power-up, and remains in the selected mode until power is toggled ([Table 2](#)). When powered up in I²C mode, the first configuration table, CFG0, is loaded. When powered up in selection-pin mode, the SEL0 and SEL1 inputs are decoded to select one of the four configuration tables CFG0-CFG3.

The RAM registers ([Table 4](#)) include Status registers for read-back of the device's operating conditions in I²C mode.

Figure 1. Register Maps

OTP Banks



Contents

| | |
|---|----|
| Register Descriptions | 1 |
| VersaClock 6E Family Register Set | 1 |
| User Configuration Table Selection | 3 |
| I2C Interface and Register Access | 3 |
| VersaClock 6E Family Power-Up Behavior | 4 |
| OTP Programming | 5 |
| In-System VersaClock 6E OTP Non-Volatile Programming via I2C | 7 |
| Default Register Values | 7 |
| OTP Control Register | 7 |
| Factory Reserved Registers for Internal Use Only | 8 |
| Configuration Registers | 13 |
| Configuration Register Detail and Functionality Description | 15 |
| Shutdown Function | 15 |
| Setting Up a Low-Power Shutdown Mode through I2C | 16 |
| Crystal Load Capacitor Registers | 18 |
| Short Example of Programming Crystal | 18 |
| PLL Pre-Divider Options | 20 |
| PLL Fractional Feedback Divider and Loop Filter | 21 |
| PLL Loop Filter Settings | 25 |
| Fractional Output Dividers and Spread Spectrum | 26 |
| Example of FOD calculation for SSCE = 1 | 29 |
| Output Divider Control Settings (Table 47 through Table 50) | 31 |
| Output Divider Integer Settings (Table 51 through Table 58) | 33 |
| Output Divider Fractional and Spread Settings (Table 59 through Table 94) | 35 |
| Skew | 48 |
| Output Divider Skew Integer and Fractional Part Registers Settings (Table 95 through Table 107) | 49 |
| Clock Output Configurations Registers | 54 |
| Revision History | 58 |

User Configuration Table Selection

At power-up, the voltage at OUT0_SEL_I2CB pin 24 is latched by the part and used to select the state of SEL0/SCL pin 9 and SEL1/SDA pin 8 (Table 2).

If a weak pull-up (10kΩ) is placed on OUT0_SEL_I2CB, the SEL0/SCL and SEL1/SDA pins will be configured as hardware select inputs, SEL0 and SEL1. Connecting SEL0 and SEL1 to VDDD and/or GND selects one of 4 configuration register sets, CFG0 through CFG3, which is then loaded into the non-volatile configuration registers to configure the clock synthesizer.

If a weak pull-down is placed on OUT0_SEL_I2CB (or if it is left floating to use internal pull-down), the pins SEL0 and SEL1 will be configured as a I²C interface's SDA and SCL slave bus. Configuration register set CFG0 is always loaded into the non-volatile configuration registers to configure the clock synthesizer. The host system can use the I²C bus to update the non-volatile configuration registers to change the configuration, and to read status registers.

Table 2. Power-Up Setting of Hardware Select Pin vs I²C Mode, and Default OTP Configuration Register

| OUT0_SEL_I2CB Strap at Power-Up | SEL1/SDA pin | SEL0/SCL pin | Function |
|---------------------------------|--------------|--------------|--|
| 10kΩ pull-up | 0 | 0 | OTP bank CFG0 used to initialize RAM configuration registers. |
| | 0 | 1 | OTP bank CFG1 used to initialize RAM configuration registers. |
| | 1 | 0 | OTP bank CFG2 used to initialize RAM configuration registers. |
| | 1 | 1 | OTP bank CFG3 used to initialize RAM configuration registers. |
| 10kΩ pull-down or floating | SDA | SCL | I ² C bus enabled to access registers. OTP bank CFG0 used to initialize RAM configuration registers. |

I²C Interface and Register Access

When powered up in I²C mode (Table 2), the device allows access to internal RAM registers (Table 4). The OTP registers (Table 3) are programmed by loading the desired values into the RAM registers that shadow the target OTP registers (Table 4), and initiating the internal programming sequence for the desired register range.

Users should not write to the Trim RAM in address range 0x01–0x0F, or the Test RAM in address range 0x6A–0x6F, and should only write to the OTP Control in address range 0x70–0x7F when programming the OTP.

The RAM in address range 0x80–0x8F is not used by the device and may be used for any purpose.

Table 3. OTP Register Map Summary

| Register Range | OTP Register Block Name | Register Block Description |
|----------------|-------------------------|---|
| 0x000 | OTP Control | OTP burned status & I ² C address setting. |
| 0x001–0x00F | Trim Presets | Program default settings. See page 6. |
| 0x010–0x069 | CFG0 | User configuration settings bank 0. |
| 0x06A–0x0C3 | CFG1 | User configuration settings bank 1. |
| 0x0C4–0x11D | CFG2 | User configuration settings bank 2. |
| 0x11E–0x177 | CFG3 | User configuration settings bank 3. |
| 0x178–0x1AF | Factory Use | Factory settings—do not over-program. |

Table 4. RAM Register Map Summary

| Register Range | RAM Register Block | Corresponding OTP Register Block Name | Corresponding OTP Register Block Address Range |
|----------------|-----------------------|---------------------------------------|--|
| 0x00 | OTP Control | OTP Control | 0x000 |
| 0x01–0x0F | Trim | Trim | 0x000–0x00F |
| 0x10–0x1F | Configuration–Main | CFG0 CFG1 CFG2 CFG3 | 0x010–0x069 0x06A–0x0C3 0x0C4–0x11D 0x11E–0x177 |
| 0x20–0x2F | Configuration–CLK1 | | |
| 0x30–0x3F | Configuration–CLK2 | | |
| 0x40–0x4F | Configuration–CLK3 | | |
| 0x50–0x5F | Configuration–CLK4 | | |
| 0x60–0x69 | Configuration–Outputs | | |
| 0x6A–0x6F | Factory Use | — | — |
| 0x70–0x7F | OTP Control | — | — |
| 0x80–0x8F | Unused RAM | — | — |
| 0x90–0x9F | Factory Use | — | — |

VersaClock 6E Family Power-Up Behavior

On power-up, the following RAM register loading sequence occurs:

- The RAM registers always initialize to a hard-wired set of default values, which are also the 'Default register values' for OTP shown in subsequent tables.
- If OTP_burned bit D7 = 0** in the OTP Control register (Table 7), this indicates that the both the Trim OTP tables and at least one of the four OTP user configuration tables have been programmed.
 - Factory programmed product is typically shipped in this condition. Device has factory trim performed and with required customization written into OTP memory. Renesas programs user customization at factory test. Please visit our website for device customization request.
 - Trim RAM data will be updated from the Trim OTP registers into the appropriate trim RAM registers, overwriting the initial default values.
 - Configuration data will be read from the one of the four OTP user configuration tables into the appropriate configuration RAM registers, overwriting the initial default values. When powered up in I²C mode, the first configuration table, CFG0, is loaded. When powered up in selection-pin mode, the SEL0 and SEL1 input pins are decoded to select one of the four configuration tables (Table 23).
 - Initialization is now complete, and the part will operate per the configuration settings.
- If OTP_burned bit D7 = 1** in the OTP Control register (Table 7), this indicates that the four OTP user configuration tables are unconfigured.
 - Un-programmed product is shipped in this condition and ready for user self-program and customization.
 - Configuration RAM data remains at the hard-wired set of default values.
 - Initialization is now complete, and the part will operate per the default configuration settings.
 - When powered up in I²C mode, the Configuration RAM registers can be written with the user's desired settings by the host system, and the clock generator operated without ever programming any of the four OTP user configuration tables. Alternatively, the host system (or a programming system) can program one of more of the four OTP user configuration tables, and also clear the OTP_burned bit D7 in the OTP Control register (Table 7) to 0. The VersaClock 6E device will follow the behavior according to section 0 above for subsequent power ups.

4. PLL calibration generally happens at power-up and is reliable when using a crystal as the reference clock. The Auto-Calibration at power-up is also reliable with an external reference clock overdriving XIN or at CLKIN but only when this reference clock is available and stable within 1ms after power-up. The Auto-Calibration needs a stable reference clock for the calibration to be successful. To guarantee robust and reliable operation with pre-programmed devices, the factory will perform a PLL calibration at production test and store the results in OTP, in case the configuration is using an external reference clock. Pre-programmed devices with a custom dash code in the part number will be immune to reference clock instability at power-up and there is no requirement for the reference clock to be available within a certain amount of time after power-up. The VersaClock 6E device, however, will not function properly without a reference clock but as soon as the reference clock turns on and is stable, the PLL will lock properly and output clocks will be stable and accurate.

OTP Programming

The steps for OTP programming are given in [Table 5](#). The procedure is to write the desired default data to the appropriate RAM registers, and then to instruct the part to burn a desired register address range into OTP.

The RAM registers have an 8-bit register address (0x00 to 0x9F), while the user OTP registers have a 9-bit address (0x000 to 0x177). This is because there are 4 banks of configuration data in OTP. The OTP addressing therefore extends across two RAM registers ([Table 5](#)). The 9-bit user start address is set by register 0x73[7:0] + 0x74[7]. The 9-bit user end address is set by register 0x75[7:0] + 0x76[7].

Table 5. OTP Programming Procedure

| Step | Procedure | Notes |
|------|---|--|
| 0 | Connect all VDD pins to a single 3.3V, with OUT0_SEL_I2CB pin left floating. | Power on the part in I ² C mode. |
| 1 | Wait 100ms. | Part power-up initialization. |
| 2 | Write device RAM configuration registers 0x10 to 0x69 to the desired state. | These RAM values will be programmed into OTP as new default register values. |
| 3 | Write registers 0x73 to 0x78 following the procedure in Table 5 . | Set burn register source address range and destination register bank CFG0, 1, 2, or 3. |
| 4 | Write register 0x72 = 0xF0. | Reset burn bit. |
| 5 | Write register 0x72 = 0xF8. | Burn the OTP range defined above. |
| 6 | Wait 500ms. | Wait for burn to complete. Device stops acknowledging while burning. |
| 7 | Write register 0x72 = 0xF0. | Reset burn bit. |
| 8 | Write register 0x72 = 0xF8. | Repeat the burn. |
| 9 | Wait 500ms. | Wait for burn to complete. Device stops acknowledging while burning. |
| 10 | Write register 0x72 = 0xF0. | Reset burn bit. |
| 11 | Done programming. | Programming complete. |
| 12 | Write register 0x72 = 0xF2. | Perform margin read. |
| 13 | Write register 0x72 = 0xF0. | Reset margin read bit. |
| 14 | Read register 0x9F: If bit D1 = 0, programming was successful. If bit D1 = 1, programming failed. | Test if OTP programming was successful. |
| 15 | Write register 0x9F = 0x00. | Reset margin read status bit. |

Table 5. OTP Programming Procedure (Cont.)

| Step | Procedure | Notes |
|------|---|---|
| 16 | One configuration register bank (CFG0, 1, 2, or 3) is now burned. To burn another bank, repeat the procedure from Step 2. | Burn further configuration register banks if desired. |
| 17 | When all desired configuration register bank have been burned, write device OTP Control register 0x00 with OTP_burned bit D7 clear. | Burn OTP Control register clearing OTP_burned bit D7. This sets the part to load configuration data from OTP on power-up. |
| 18 | Exit. | Done. |

Table 6. OTP Addressing For Programming

| Register | User Start Address[8:0] Part-Select Bit 0x73 | Enable Sub-block's Test Mode 0x74 | User End Address[8:0] Part-Select Bit 0x75 | User End Address[8:0] Part-Select Bits 0x76 | Burned Register Start Address 0x77 | Read Register Start Address 0x78 | Registers Burned To OTP |
|----------------------|--|-----------------------------------|--|---|------------------------------------|----------------------------------|-------------------------|
| OTP Control register | 0x00 | 0x4E | 0x00 | 0x61 | 0x00 | 0x00 | 0x00 |
| Configuration CFG0* | 0x00 | 0x4E | 0x34 | 0xE1 | 0x00 | 0x00 | 0x00 to 0x69 |
| Configuration CFG1 | 0x35 | 0x4E | 0x61 | 0xE1 | 0x10 | 0x10 | 0x10 to 0x69 |
| Configuration CFG2 | 0x62 | 0x4E | 0x8E | 0xE1 | 0x10 | 0x10 | 0x10 to 0x69 |
| Configuration CFG3 | 0x8F | 0x4E | 0xBB | 0xE1 | 0x10 | 0x10 | 0x10 to 0x69 |

* Configuration CFG0 includes the Trim presets in 0x01 to 0x0F.

Use the steps in the following example as guidelines to program configuration 0 OTP registers:

1. Write the value from register address 0x00 to 0x69 (first bank) to RAM registers.

Starting at Address 0x00, write data: 61 F3 00 00 00 00 00 00 00 FF FD 00 00 B6 B4 92 88 0C 81 80 00 03 8C 03 20 00 00 00 9F FF F0 80 00 81 00 00 00 00 00 00 00 00 00 01 01 90 00 00 8F 00 00 00 00 00 00 00 00 00 00 9C 40 00 00 81 02 00 00 00 00 00 00 00 00 00 00 C0 00 00 81 00 00 00 00 00 00 00 00 00 00 00 A0 00 3B 01 3B 00 BB 01 7B 01 FF FC

In above example, 61 is the value in register 0x00 that correspond to I²C address D4 and the trim presets are recommended defaults: 0x01–0x0F = "F3 00 00 00 00 00 00 00 FF FD 00 00 B6 B4 92".

In above example, a 25MHz crystal is expected, OUT0 is enabled, OUT1 is 50MHz LVCMOS, OUT2 is 10KHz LVCMOS, OUT3 is 100MHz LVCMOSD and OUT4 is 125MHz LVDS. In case of 5P49V6967 and 5P49V6968, the OUT3 setting will determine the frequency of the LP-HCSL outputs.

2. Write the following values to program the OTP with config0 and trim bits (Table 6):
 - Reg Address (hex): 73 74 75 76 77 78
 - Configuration 0: 00 4E 34 E1 00 00
3. Start Burn with Reg 0x72 set to F8.
4. Wait 500ms.
5. Reset Burn Start Bit 0x72 set to F0.

In-System VersaClock 6E OTP Non-Volatile Programming via I²C

For in-system programming of OTP, it is required to power the VDDA and VDDD pins from 3.3V. Other VDD pins can be powered from 1.8V, 2.5V or 3.3V, whatever is needed for the application.

Burning OTP requires a high internal voltage. The circuit responsible for generating the high internal voltage needs at least 3.3V to generate a high enough internal voltage for reliable OTP burning with good data retention.

Default Register Values

The following tables have a column “Default Value”. These are values as they show in a 5P49V69xxA000, so called “blank” device that is meant for field programming. When the device is still un-programmed, it runs a default mode with OUT0 enabled and OUT1 = 100MHz, assuming a 25MHz crystal is connected. The default values are the register settings for this default mode.

OTP Control Register

The I²C slave address can be changed from the default 0xD4 to 0xD0 by programming the I2C_ADDR bit D0. Note that the I²C address change occurs on the I²C ACK of the write transaction. An I²C write sequence to register 0x00 that changes the value of I2C_ADDR bit D0 should be followed by an I²C STOP condition. Further I²C transactions to the part use the new address.

In the OTP Control Register (Table 7) bits can be set for the OTP Burn and OTP Trim status, VC6E or MEMS use and I²C address setting. Four bits are left unused.

Table 7. RAM0 0x00 – OTP Control Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 1 | OTP_burned | It's an active low state that indicates all the OTP burn process is done. D7 = 1 tells the chip that OTP is not burned and it will run the default mode. D7 = 0 tells the chip that OTP is burned and it will transfer OTP content to the registers for operating settings. |
| D6 | 1 | OTP_TRIM | An active low state that indicates OTP trim part is burned.* |
| D5 | 1 | Unused | Unused. |
| D4 | 1 | Unused | Unused. |
| D3 | 1 | Unused | Unused. |
| D2 | 1 | Unused | Unused. |
| D1 | 1 | Unused | Unused. |
| D0 | 1 | Device I2C_ADDR | If I2C_ADDR = 0 then D0 and if I2C_ADDR = 1 then D4. |

* The trim values are commonly written with default values and the OTP_TRIM bit is left at “1”.

Factory Reserved Registers for Internal Use Only

Table 8. RAM0 – 0x01: Factory Reserved Bits - Device ID for Chip Identification

| Bits | Default Value | Name | Function |
|------|---------------|------------|---|
| D7 | 1 | CFG0_LOCK* | Set to “0” to disable burning OTP of Configuration 0. |
| D6 | 1 | CFG1_LOCK* | Set to “0” to disable burning OTP of Configuration 1. |
| D5 | 1 | CFG2_LOCK* | Set to “0” to disable burning OTP of Configuration 2. |
| D4 | 1 | CFG3_LOCK* | Set to “0” to disable burning OTP of Configuration 3. |
| D3 | 1 | Unused | Unused. |
| D2 | 1 | Unused | Unused. |
| D1 | 1 | Reserved | Factory reserved, leave at “1”. |
| D0 | 1 | Reserved | Factory reserved, leave at “1”. |

* Configuration Lock bits can be used to prevent future OTP burning that can modify OTP content.

Table 9. RAM0 – 0x02: Factory Reserved Bits - ADC Gain Setting

| Bits | Default Value | Name | Function |
|------|---------------|---------------|--|
| D7 | 0 | ADC gain[7:0] | ADC gain setting - Factory reserved bits |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 10. RAM0 – 0x03: Factory Reserved Bits - ADC Gain Setting

| Bits | Default Value | Name | Function |
|------|---------------|----------------|--|
| D7 | 0 | ADC gain[15:8] | ADC gain setting - Factory reserved bits |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 11. RAM0 – 0x04: Factory Reserved Bits - ADC OFFSET

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|------------------------------------|
| D7 | 0 | ADC offset[7:0] | ADC offset - Factory reserved bits |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 12. RAM0 – 0x05: Factory reserved bits - ADC OFFSET

| Bits | Default Value | Name | Function |
|------|---------------|------------------|------------------------------------|
| D7 | 0 | ADC offset[15:8] | ADC offset - Factory reserved bits |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 13. RAM0 – 0x06: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|------------|-----------------------|
| D7 | 0 | TEMPY[7:0] | Factory reserved bits |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 14. RAM0 – 0x07: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|------------------|------------------------------|
| D7 | 1 | OFFSET_TBIN<7:0> | Unused Factory reserved bits |
| D6 | 1 | | |
| D5 | 1 | | |
| D4 | 1 | | |
| D3 | 1 | | |
| D2 | 1 | | |
| D1 | 1 | | |
| D0 | 1 | | |

Table 15. RAM0 – 0x08: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|-----------|------------------------------|
| D7 | 1 | GAIN<7:0> | Unused Factory reserved bits |
| D6 | 1 | | |
| D5 | 1 | | |
| D4 | 1 | | |
| D3 | 1 | | |
| D2 | 1 | | |
| D1 | 1 | | |
| D0 | 1 | | |

Table 16. RAM0 – 0x09: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|-----------|-----------------------|
| D7 | 1 | test[3:0] | Factory reserved bits |
| D6 | 1 | | |
| D5 | 1 | | |
| D4 | 1 | | |
| D3 | 1 | NP[3:0] | Factory reserved bits |
| D2 | 1 | | |
| D1 | 1 | | |
| D0 | 1 | | |

Table 17. RAM0 – 0x0A: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|----------|-----------------------|
| D7 | 1 | Reserved | Factory reserved bits |
| D6 | 1 | Reserved | |
| D5 | 1 | Reserved | |
| D4 | 1 | Reserved | |
| D3 | 1 | Reserved | |
| D2 | 1 | Reserved | |
| D1 | 0 | Reserved | |
| D0 | 1 | Reserved | |

Table 18. RAM0 – 0x0B: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|--------------------------|--|
| D7 | 0 | bandgap_trim_up [5:0] | bandgap voltage trim, one step is 1.2mV higher than current. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | unused bit | |
| D0 | 0 | unused bit | |

Table 19. RAM0 – 0x0C: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|--------------------------|---|
| D7 | 0 | bandgap_trim_dn [5:0] | bandgap voltage trim, one step is 1.2mV lower than current. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | unused bit | |
| D0 | 0 | unused bit | |

Table 20. RAM0 – 0x0D: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 1 | clk1_R_trim[2:0] | clk_R_trim: trim for “R” variation, 1LSB is 10%, default is in the middle level. |
| D6 | 0 | | |
| D5 | 1 | | |
| D4 | 1 | clk2_R_trim[2:0] | clk_R_trim: trim for “R” variation, 1LSB is 10%, default is in the middle level. |
| D3 | 0 | | |
| D2 | 1 | | |
| D1 | 1 | CLK4_amp[2] | clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level. |
| D0 | 0 | CLK4_amp[1] | clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level. |

Table 21. RAM0 – 0x0E: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 1 | clk3_R_trim[2:0] | clk_R_trim: trim for “R” variation, 1LSB is 10%, default is in the middle level. |
| D6 | 0 | | |
| D5 | 1 | | |
| D4 | 1 | clk4_R_trim[2:0] | clk_R_trim: trim for “R” variation, 1LSB is 10%, default is in the middle level. |
| D3 | 0 | | |
| D2 | 1 | | |
| D1 | 0 | CLK4_amp[0] | clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level. |
| D0 | 0 | CLK3_amp[0] | clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level. |

Table 22. RAM0 – 0x0F: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|-------------|--|
| D7 | 1 | CLK1_amp[2] | clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level–Factory reserved bits. |
| D6 | 0 | CLK1_amp[1] | |
| D5 | 0 | CLK1_amp[0] | |
| D4 | 1 | CLK2_amp[2] | |
| D3 | 0 | CLK2_amp[1] | |
| D2 | 0 | CLK2_amp[0] | |
| D1 | 1 | CLK3_amp[2] | |
| D0 | 0 | CLK3_amp[1] | |

Configuration Registers

The internal RAM configuration registers occupy 0x10 to 0x69 (Table 4).

The 4 OTP configuration banks CFG0, CFG1, CFG2, and CFG3 use the same register structure and setting behavior.

The tables with register details refer to the RAM register address for simplicity. Table 23 shows the 3-digit OTP register addresses 0x010 to 0x177 for the four banks of identical configuration registers, and the corresponding RAM register address.

Table 23. RAM Configuration Registers and OTP Configuration Registers CFG0, CFG1, CFG2, CFG3 Summary

| Register Address | | | | | Function |
|------------------|-------|-------|-------|-------|--|
| RAM | CFG0 | CFG1 | CFG2 | CFG3 | |
| 0x10 | 0x010 | 0x06A | 0x0C4 | 0x11E | Primary Source and Shutdown Register |
| 0x11 | 0x011 | 0x06B | 0x0C5 | 0x11F | VCO Band and Factory Reserved Bits |
| 0x12 | 0x012 | 0x06C | 0x0C6 | 0x120 | Crystal X1 Load Capacitor Register |
| 0x13 | 0x013 | 0x06D | 0x0C7 | 0x121 | Crystal X2 Load Capacitor Register |
| 0x14 | 0x014 | 0x06E | 0x0C8 | 0x122 | Factory Reserved Register |
| 0x15 | 0x015 | 0x06F | 0x0C9 | 0x123 | Reference Divider Register |
| 0x16 | 0x016 | 0x070 | 0x0CA | 0x124 | VCO Control Register and Pre-Divider |
| 0x17 | 0x017 | 0x071 | 0x0CB | 0x125 | Feedback Integer Divider Register |
| 0x18 | 0x018 | 0x072 | 0x0CC | 0x126 | Feedback Integer Divider Bits |
| 0x19 | 0x019 | 0x073 | 0x0CD | 0x127 | Feedback Fractional Divider Register |
| 0x1A | 0x01A | 0x074 | 0x0CE | 0x128 | Feedback Fractional Divider Register |
| 0x1B | 0x01B | 0x075 | 0x0CF | 0x129 | Feedback Fractional Divider Register |
| 0x1C | 0x01C | 0x076 | 0x0D0 | 0x12A | Factory Reserved Register |
| 0x1D | 0x01D | 0x077 | 0x0D1 | 0x12B | Factory Reserved Register |
| 0x1E | 0x01E | 0x078 | 0x0D2 | 0x12C | RC Control Register |
| 0x1F | 0x01F | 0x079 | 0x0D3 | 0x12D | RC Control Register |
| 0x20 | 0x020 | 0x07A | 0x0D4 | 0x12E | Unused Factory Reserved Register |
| 0x21 | 0x021 | 0x07B | 0x0D5 | 0x12F | Output Divider 1 Control Register Settings |
| 0x22 | 0x022 | 0x07C | 0x0D6 | 0x130 | Output Divider 1 Fractional Settings |
| 0x23 | 0x023 | 0x07D | 0x0D7 | 0x131 | Output Divider 1 Fractional Settings |
| 0x24 | 0x024 | 0x07E | 0x0D8 | 0x132 | Output Divider 1 Fractional Settings |
| 0x25 | 0x025 | 0x07F | 0x0D9 | 0x133 | Output Divider1 Fractional Settings |
| 0x26 | 0x026 | 0x080 | 0x0DA | 0x134 | Output Divider 1 Step Spread Configuration Register |
| 0x27 | 0x027 | 0x081 | 0x0DB | 0x135 | Output Divider 1 Step Spread Configuration Register |
| 0x28 | 0x028 | 0x082 | 0x0DC | 0x136 | Output Divider 1 Step Spread Configuration Register |
| 0x29 | 0x029 | 0x083 | 0x0DD | 0x137 | Output Divider 1 Spread Modulation Rate Configuration Register |
| 0x2A | 0x02A | 0x084 | 0x0DE | 0x138 | Output Divider 1 Spread Modulation Rate Configuration Register |
| 0x2B | 0x02B | 0x085 | 0x0DF | 0x139 | Output Divider 1 Skew Integer Part |

Table 23. RAM Configuration Registers and OTP Configuration Registers CFG0, CFG1, CFG2, CFG3 Summary (Cont.)

| Register Address | | | | | Function |
|------------------|-------|-------|-------|-------|--|
| RAM | CFG0 | CFG1 | CFG2 | CFG3 | |
| 0x2C | 0x02C | 0x086 | 0x0E0 | 0x13A | Output Divider 1 Skew Integer Part |
| 0x2D | 0x02D | 0x087 | 0x0E1 | 0x13B | Output Divider 1 Integer Part |
| 0x2E | 0x02E | 0x088 | 0x0E2 | 0x13C | Output Divider 1 Integer Part |
| 0x2F | 0x02F | 0x089 | 0x0E3 | 0x13D | Output Divider 1 Skew Fractional part |
| 0x30 | 0x030 | 0x08A | 0x0E4 | 0x13E | Unused Factory Reserved Register |
| 0x31 | 0x031 | 0x08B | 0x0E5 | 0x13F | Output Divider 2 Control Register Settings |
| 0x32 | 0x032 | 0x08C | 0x0E6 | 0x140 | Output Divider 2 Fractional Settings |
| 0x33 | 0x033 | 0x08D | 0x0E7 | 0x141 | Output Divider 2 Fractional Settings |
| 0x34 | 0x034 | 0x08E | 0x0E8 | 0x142 | Output Divider 2 Fractional Settings |
| 0x35 | 0x035 | 0x08F | 0x0E9 | 0x143 | Output Divider2 Fractional Settings |
| 0x36 | 0x036 | 0x090 | 0x0EA | 0x144 | Output Divider 2 Step Spread Configuration Register |
| 0x37 | 0x037 | 0x091 | 0x0EB | 0x145 | Output Divider 2 Step Spread Configuration Register |
| 0x38 | 0x038 | 0x092 | 0x0EC | 0x146 | Output Divider 2 Step Spread Configuration Register |
| 0x39 | 0x039 | 0x093 | 0x0ED | 0x147 | Output Divider 2 Spread Modulation Rate Configuration Register |
| 0x3A | 0x03A | 0x094 | 0x0EE | 0x148 | Output Divider 2 Spread Modulation Rate Configuration Register |
| 0x3B | 0x03B | 0x095 | 0x0EF | 0x149 | Output Divider 2 Skew Integer Part |
| 0x3C | 0x03C | 0x096 | 0x0F0 | 0x14A | Output Divider 2 Skew Integer Part |
| 0x3D | 0x03D | 0x097 | 0x0F1 | 0x14B | Output Divider 2 Integer Part |
| 0x3E | 0x03E | 0x098 | 0x0F2 | 0x14C | Output Divider 2 Integer Part |
| 0x3F | 0x03F | 0x099 | 0x0F3 | 0x14D | Output Divider 2 Skew Fractional part |
| 0x40 | 0x040 | 0x09A | 0x0F4 | 0x14E | Unused Factory Reserved Register |
| 0x41 | 0x041 | 0x09B | 0x0F5 | 0x14F | Output Divider 3 Control Register Settings |
| 0x42 | 0x042 | 0x09C | 0x0F6 | 0x150 | Output Divider 3 Fractional Settings |
| 0x43 | 0x043 | 0x09D | 0x0F7 | 0x151 | Output Divider 3 Fractional Settings |
| 0x44 | 0x044 | 0x09E | 0x0F8 | 0x152 | Output Divider 3 Fractional Settings |
| 0x45 | 0x045 | 0x09F | 0x0F9 | 0x153 | Output Divider 3 Fractional Settings |
| 0x46 | 0x046 | 0x0A0 | 0x0FA | 0x154 | Output Divider 3 Step Spread Configuration Register |
| 0x47 | 0x047 | 0x0A1 | 0x0FB | 0x155 | Output Divider 3 Step Spread Configuration Register |
| 0x48 | 0x048 | 0x0A2 | 0x0FC | 0x156 | Output Divider 3 Step Spread Configuration Register |
| 0x49 | 0x049 | 0x0A3 | 0x0FD | 0x157 | Output Divider 3 Spread Modulation Rate Configuration Register |
| 0x4A | 0x04A | 0x0A4 | 0x0FE | 0x158 | Output Divider 3 Spread Modulation Rate Configuration Register |
| 0x4B | 0x04B | 0x0A5 | 0x0FF | 0x159 | Output Divider 3 Skew Integer Part |
| 0x4C | 0x04C | 0x0A6 | 0x100 | 0x15A | Output Divider 3 Skew Integer Part |
| 0x4D | 0x04D | 0x0A7 | 0x101 | 0x15B | Output Divider 3 Integer Part |

Table 23. RAM Configuration Registers and OTP Configuration Registers CFG0, CFG1, CFG2, CFG3 Summary (Cont.)

| Register Address | | | | | Function |
|------------------|-------|-------|-------|-------|--|
| RAM | CFG0 | CFG1 | CFG2 | CFG3 | |
| 0x4E | 0x04E | 0x0A8 | 0x102 | 0x15C | Output Divider 3 Integer Part |
| 0x4F | 0x04F | 0x0A9 | 0x103 | 0x15D | Output Divider 3 Skew Fractional part |
| 0x50 | 0x050 | 0x0AA | 0x104 | 0x15E | Unused Factory Reserved Register |
| 0x51 | 0x051 | 0x0AB | 0x105 | 0x15F | Output Divider 4 Control Register Settings |
| 0x52 | 0x052 | 0x0AC | 0x106 | 0x160 | Output Divider 4 Fractional Settings |
| 0x53 | 0x053 | 0x0AD | 0x107 | 0x161 | Output Divider 4 Fractional Settings |
| 0x54 | 0x054 | 0x0AE | 0x108 | 0x162 | Output Divider 4 Fractional Settings |
| 0x55 | 0x055 | 0x0AF | 0x109 | 0x163 | Output Divider 4 Fractional Settings |
| 0x56 | 0x056 | 0x0B0 | 0x10A | 0x164 | Output Divider 4 Step Spread Configuration Register |
| 0x57 | 0x057 | 0x0B1 | 0x10B | 0x165 | Output Divider 4 Step Spread Configuration Register |
| 0x58 | 0x058 | 0x0B2 | 0x10C | 0x166 | Output Divider 4 Step Spread Configuration Register |
| 0x59 | 0x059 | 0x0B3 | 0x10D | 0x167 | Output Divider 4 Spread Modulation Rate Configuration Register |
| 0x5A | 0x05A | 0x0B4 | 0x10E | 0x168 | Output Divider 4 Spread Modulation Rate Configuration Register |
| 0x5B | 0x05B | 0x0B5 | 0x10F | 0x169 | Output Divider 4 Skew Integer Part |
| 0x5C | 0x05C | 0x0B6 | 0x110 | 0x16A | Output Divider 4 Skew Integer Part |
| 0x5D | 0x05D | 0x0B7 | 0x111 | 0x16B | Output Divider 4 Integer Part |
| 0x5E | 0x05E | 0x0B8 | 0x112 | 0x16C | Output Divider 4 Integer Part |
| 0x5F | 0x05F | 0x0B9 | 0x113 | 0x16D | Output Divider 4 Skew Fractional Part |
| 0x60 | 0x060 | 0x0BA | 0x114 | 0x16E | Clock 1 Output Configuration |
| 0x61 | 0x061 | 0x0BB | 0x115 | 0x16F | Clock 2 Output Configuration |
| 0x62 | 0x062 | 0x0BC | 0x116 | 0x170 | Clock 1 Output Configuration |
| 0x63 | 0x063 | 0x0BD | 0x117 | 0x171 | Clock 2 Output Configuration |
| 0x64 | 0x064 | 0x0BE | 0x118 | 0x172 | Clock 1 Output Configuration |
| 0x65 | 0x065 | 0x0BF | 0x119 | 0x173 | Clock 2 Output Configuration |
| 0x66 | 0x066 | 0x0C0 | 0x11A | 0x174 | Clock 1 Output Configuration |
| 0x67 | 0x067 | 0x0C1 | 0x11B | 0x175 | Clock 2 Output Configuration |
| 0x68 | 0x068 | 0x0C2 | 0x11C | 0x176 | CLK_OE/Shutdown Function |
| 0x69 | 0x069 | 0x0C3 | 0x11D | 0x177 | CLK_OS/Shutdown Function |

Configuration Register Detail and Functionality Description

Shutdown Function

The shutdown logic offers flexible configuration of shutdown signaling and clock output enable control. The shutdown logic is summarized in [Table 24](#).

When SP bit D1 = 0 in the Shutdown register 0x00 (Table 25), the SD/OE input is active low. When SP bit D1 = 1, SD/OE is active high.

SH bit D0 in the Shutdown register 0x10 (Table 25) configures the SD/OE input's action as either output enable (OE) for the clock outputs (leaving the PLL running), or full part shutdown. SH bit D1 = 0 for OE function, or 1 for shutdown function.

In shutdown, the part is shut down, differential outputs are driven High/low, and the single-ended LVCMOS outputs are driven low. In output-disable, individual outputs can be selected to be either Hi-Z or driven high/low, depending on the configuration of the CLKx_OS and CLKx_OE bits shown in Table 24.

Table 24. Shutdown Truth Table

| SH bit | SP bit | OSn bit | OEn bit | SD/OE bit | SD/OE pin | OUTn |
|--------|--------|---------|---------|-----------|-----------|---|
| 0 | x | 1 | 0 | x | x | Output Active |
| x | 0 | 1 | 1 | x | 0 | Output Active |
| 0 | 1 | 1 | 1 | x | 1 | Output Active |
| 1 | x | 1 | 0 | x | 0 | Output Active |
| 0 | 0 | 1 | 1 | 0 | 1 | Output Driven Logic "1" (High/Low) |
| x | 1 | 1 | 1 | 0 | 0 | Output Driven Logic "1" (High/Low) |
| 1 | x | x | x | 0 | 1 | Global Shutdown, Output Driven Logic "1" (High/Low) |
| x | x | 0 | x | x | x | Output Tri-stated (Hi-Z) |
| 0 | 0 | 1 | 1 | 1 | 1 | Output Tri-stated (Hi-Z) |
| x | 1 | 1 | 1 | 1 | 0 | Output Tri-stated (Hi-Z) |

SH bit = "Shutdown Bit": Enable shutdown mode where the SD/OE pin can disable more than just outputs.

SP bit = "SD/OE pin Polarity Bit": Set the polarity of the SD/OE pin where outputs enable or disable. Only works with OE, not with SD.

OSn bit = "Output Suspend Bit": Permanently disable an output, independent of SD/OE pin.

OEn bit = "Output Enable Bit": Permanently enable an output, independent of SD/OE pin. Only works with OE, not with SD.

SDOE bit = "Output Disabled State": Set the output state to either driven High/Low or Hi-Z when disabled with the SD/OE pin.

SD/OE pin = Physical pin on the device.

SH and SP bits exist only once and affect all outputs. Other bits exist per output and affect that specific output.

Setting Up a Low-Power Shutdown Mode through I²C

1. Tristate the outputs by writing b'001ss000' to registers 0x60, 0x62, 0x64, and 0x66 where ss = 00, 10, or 11 for output clock supply voltages 1.8V, 2.5V, or 3.3V.
2. Program all outputs to single-ended CMOS by writing 0x00 to registers 0x68.
3. Enable shutdown functionality by either writing 0x83 or 0x43 to register 0x10, for crystal clock source or external clock respectively.
4. Disable all output dividers by writing 0x80 to registers 0x21, 0x31, 0x41, and 0x51.
5. Take the SD/OE input pin 7 high.

Table 25. RAM1 – 0x10: Primary Source and Shutdown Register

| Bits | Default Value | Name | Function |
|------|---------------|--------------------|--|
| D7 | 1 | en_xtal | Crystal Oscillator circuit is disabled with 0 and enabled with 1. |
| D6 | 0 | en_clkin | CLKIN differential input circuit is disabled with 0 and enabled with 1. |
| D5 | 0 | unused | Unused Factory reserved bit. |
| D4 | 0 | unused | Unused Factory reserved bit. |
| D3 | 0 | en_ref_doubler | Use “en_ref_doubler” is 1 to double the reference frequency for the Phase Frequency Detector. Use “en_ref_doubler” is 0 to bypass the doubler. |
| D2 | 0 | en_refmode | Enable path from reference clock to OUT1. Set to 1 when OUT1 is a copy of the reference clock (= OUT0). Set to 0 when using FOD1 for OUT1. |
| D1 | 0 | SP | SD/OE input pin is active low if this bit is 0 and active high if this bit is 1. (If D0 = 0 then D1 reverses SD/OE pin polarity, affecting OE bits in output polarity. If D0 = 1, SD/OE pin = 1 causes global shutdown). |
| D0 | 0 | en_global shutdown | D1 reverses SD/OE pin polarity, affecting OE bits in output buffers and SD/OE input pin is shutdown (SD) if this bit is 1. |

NOTE: Bit D6 is not used for 5P49V6967 and 5P49V6968 as these products have only a crystal input

Table 26. RAM6 – 0x68: CLK_OE/Shutdown Function

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|---|
| D7 | 1 | CLK0_OE | See Table 24 – This is bit OEn for output 0. |
| D6 | 1 | CLK1_OE | See Table 24 – This is bit OEn for output 1. |
| D5 | 1 | CLK2_OE | See Table 24 – This is bit OEn for output 2. |
| D4 | 1 | CLK3_OE | See Table 24 – This is bit OEn for output 3. |
| D3 | 1 | CLK4_OE | See Table 24 – This is bit OEn for output 4. |
| D2 | 1 | clk0_slewrte[1] | CLK0 slew rate setting bit[1] 11 = Fastest 00 = Slowest (20% slower than 11) |
| D1 | 1 | clk0_pwr_sel[1:0] | Clock output driver power supply voltage is indicated by these bits. D1 D0 = 0x indicates 1.8V D1 D0 = 10 indicates 2.5V D1 D0 = 11 indicates 3.3V |
| D0 | 1 | | |

Table 27. RAM6 – 0x69: CLK_OS/Shutdown Function

| Bits | Default Value | Name | Function |
|------|---------------|---------|---|
| D7 | 1 | CLK0_OS | CLK_OS checks the shut down truth table. See Shutdown Function section. |
| D6 | 1 | CLK1_OS | CLK_OS checks the shut down truth table. See Shutdown Function section. |
| D5 | 1 | CLK2_OS | CLK_OS checks the shut down truth table. See Shutdown Function section. |

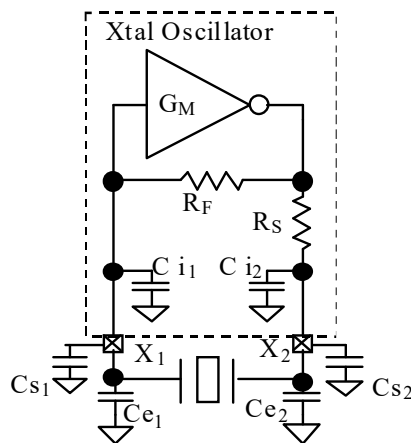
Table 27. RAM6 – 0x69: CLK_OS/Shutdown Function (Cont.)

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D4 | 1 | CLK3_OS | CLK_OS checks the shut down truth table. See Shutdown Function section. |
| D3 | 1 | CLK4_OS | CLK_OS checks the shut down truth table. See Shutdown Function section. |
| D2 | 1 | clk0_slewrte[0] | Depends on slew rate (depends on Shutdown function/truth table) – Set slew rate for clk0. |
| D1 | 0 | otp_pwr_sel[1:0] | Set Output Amplitude for OTP voltage: |
| D0 | 0 | | Factory reserved Use D1 D0 = 00. |

Crystal Load Capacitor Registers

Registers 0x12 and 0x13 are Crystal X1 and X2 Load capacitor registers respectively that are used to add load capacitance to X1 and X2 respectively. In X1 Switch mode is provided with different mode selection options and in X2 polarity selection of clock can be made whose values are given in the table.

Figure 2. Crystal Oscillator



Short Example of Programming Crystal

Ci1 and Ci2 are on-chip capacitors that are programmable.

Cs is stray capacitance in the PCB and Ce is external capacitors for frequency fine tuning or for achieving load capacitance values beyond the range of the on-chip programmability.

All these capacitors combined make the load capacitance for the crystal.

$$\text{Capacitance on pin X1: } C_{x1} = C_{i1} + C_{s1} + C_{e1}.$$

$$\text{Capacitance on pin X2: } C_{x2} = C_{i2} + C_{s2} + C_{e2}.$$

$$\text{Total Crystal Load Capacitance } C_L = C_{x1} \times C_{x2} / (C_{x1} + C_{x2}).$$

Example: For a Xtal C_L of 8pF, the registers need to be programmed with $X1 = X2 = 6.92$ pF to get a total $C_L = (6.92\text{pF} + 7.5\text{pF} + 1.5\text{pF})/2 = 7.9\text{pF}$ which is the closest value to 8pF.

Here, $C_{stray} = 1.5\text{pF}$; $\text{Package stray} = 7.5\text{pF}$

The binary settings corresponding to this value will be: $X1 = X2 = \text{“10000”}$.

Table 28. RAM1 – 0x12: Crystal X1 Load Capacitor Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------------|--------------------------------------|
| D7 | 0 | xtal_load_cap_x1[5:0] | Add 6.92pF load capacitance to X1. |
| D6 | 0 | | Add 3.46pF load capacitance to X1. |
| D5 | 0 | | Add 1.73pF load capacitance to X1. |
| D4 | 0 | | Add 0.86pF load capacitance to X1. |
| D3 | 0 | | Add 0.43pF load capacitance to X1. |
| D2 | 0 | | Add 0.43pF load capacitance to X1. |
| D1 | 0 | SM1:0] | Switch Mode |
| D0 | 1 | | Factory reserved. Use D1 D0 = 00. |

Table 29. RAM1 – 0x13: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|-----------------------|---|
| D7 | 0 | xtal_load_cap_x2[5:0] | Add 6.92pF load capacitance to X2. |
| D6 | 0 | | Add 3.46pF load capacitance to X2. |
| D5 | 0 | | Add 1.73pF load capacitance to X2. |
| D4 | 0 | | Add 0.86pF load capacitance to X2. |
| D3 | 0 | | Add 0.43pF load capacitance to X2. |
| D2 | 0 | | Add 0.43pF load capacitance to X2. |
| D1 | 0 | PRIMSRC | The PRIMSRC (primary source) bit sets the polarity of the CLKSEL pin. D1=0: When CLKSEL is Low, Crystal is selected. When CLKSEL is High, CLKIN input is selected. D1=1: When CLKSEL is Low, CLKIN input is selected. When CLKSEL is High, Crystal is selected. |
| D0 | 0 | clkok1024 | Factory reserved. |

Note: The 5P49V6975 use a pre-trimmed integrated crystal. Therefore, bits D7–D2 in registers 0x12 and 0x13 should be set to 1 to prevent inaccuracy of the output frequencies.

Table 30. RAM1 – 0x14: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|-----------------------|------------------------------|
| D7 | 0 | xtal_reg_amp_sel[3:0] | Unused Factory reserved bit. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |

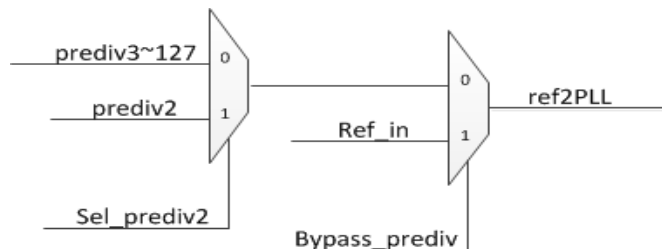
Table 30. RAM1 – 0x14: Factory Reserved Bits (Cont.)

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|------------------------------|
| D3 | 0 | xtal_l_sel[3:0] | Unused Factory reserved bit. |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

PLL Pre-Divider Options

The reference presented to the fractional PLL can be either directly connected, divided by two or divided by the any value from the range of three to 127 as set in the register Ref_Div[6:0]. The phase detector of the PLL has a maximum frequency of 150MHz, therefore the default is to bypass the pre-divider by setting Bypass_prediv = 1 (Table 32). For the functionality of Sel_prediv2 and bypass_prediv bits, see Figure 3. Table 31 and Table 32 explains the bit selections.

Figure 3. PLL Pre-Divider Options



If pre-divider is selected by selecting bypass_prediv = 0 (Table 31) then user can select divider by 2 or divider values from 3 to 127.

Table 31. RAM1 – 0x15: Reference Divider Register

| Bits | Default Value | Name | Function |
|------|---------------|--------------|--|
| D7 | 0 | Sel_prediv2 | Select the divider by 2 function; Divide by 2 if set to 1. And if bypass is set to 0. If divide bit set 0 and bypass bit set to 0 then reference divider bits (D6 to D0) will take effect. |
| D6 | 0 | Ref_div[6:0] | Reference Divider value. Use Ref_div setting for values 3 to 127. Use bit D7 for divide by 2. Use “Bypass_prediv” bit in Table 32 for divide by 1. When “Bypass_prediv” is 1, register 0x15 setting is don't care. When “Sel_prediv2” is 1, Ref_div[6:0] setting is don't care. |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 32. RAM1 – 0x16: VCO Control Register and Pre-Divider

| Bits | Default Value | Name | Function |
|------|---------------|--------------------|---|
| D7 | 1 | Bypass_prediv | Use D7 = 1 when phase frequency detector needs to be equal to the reference clock. Use D7 = 0 when the reference clock needs to be divided by at least 2 for the phase frequency detector. See Table 31 settings. |
| D6 | 0 | dither_gain_cfg[2] | Dither gain settings: Factory reserved bits. Use default values. |
| D5 | 0 | dither_gain_cfg[1] | |
| D4 | 0 | dither_gain_cfg[0] | |
| D3 | 1 | afc_en | Open loop vco control is enabled if 1 and disabled if 0–factory reserved bit. |
| D2 | 1 | cnf_afc[2:0] | Open loop vco control voltage bits–factory reserved bits. Use default values. |
| D1 | 0 | | |
| D0 | 0 | | |

Table 33. RAM1 – 0x11: VCO Band and Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|--------------------|--|
| D7 | 0 | unused | Unused Factory reserved bit. |
| D6 | 0 | unused | Unused Factory reserved bit. |
| D5 | 0 | test_mode_vco_band | “test_mode_vco_band” is 1 enables the VCO test mode. |
| D4 | 0 | vco_band[4:0] | When bit D5 is 1, it forces the VCO to use the VCO band value in bits D0–4 and ignore the VCO band (auto) calibration. |
| D3 | 1 | | |
| D2 | 1 | | |
| D1 | 0 | | |
| D0 | 0 | | |

PLL Fractional Feedback Divider and Loop Filter

Only use the 12-bit integer portion of the PLL Feedback Divider M. The setting FB_intdiv[11:0] is spread out over 2 registers.

The value of M is $FVCO / FREF2PLL$ and care must be taken that M is an integer value.

Example: The circuit uses a 25MHz crystal and we want the VCO to be 2500MHz.

The value of M needs to be $2500 / 25 = 100$.

FB_intdiv[11:0] = DEC2HEX(100) = 0 64 or 0000 0110 0100 binary.

Table 34. RAM1 – 0x17: Feedback Integer Divider Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | FB_intdiv[11:4] | The Feedback Integer Divider Register has 12 bits spread on 2 registers 0x17 and 0x18. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 1 | | |
| D1 | 1 | | |
| D0 | 1 | | |

Table 35. RAM1 – 0x18: Feedback Integer Divider Bits

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | FB_intdiv[3:0] | The Feedback Integer Divider Register has 12 bits spread on 2 registers 0x17 and 0x18. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | sdm_order_cfg[1] | Factory Reserved bits. These both bits are for Sigma Delta Modulator setting. D3 D2 = 00: sdm bypass, D3 D2 = 01: selects 1st order, D3 D2 = 10: selects 2nd order, D3 D2 = 11: selects 3rd order. |
| D2 | 0 | sdm_order_cfg[0] | |
| D1 | 0 | i2c_ssce | Factory reserved bit. |
| D0 | 0 | unused | Unused Factory reserved bit. |

Table 36. RAM1 – 0x19: Feedback Fractional Divider Registers

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | FB_frdiv[23:16] | The Feedback fractional divider has 24 bits divided amongst 3 registers (0x19, 0x1A and 0x1B). |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 37. RAM1 – 0x1A: Feedback Fractional Divider Bits

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | FB_frctdiv[15:8] | The Feedback fractional divider has 24 bits divided amongst 3 registers (0x19, 0x1A and 0x1B). |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 38. RAM1 – 0x1B: Feedback Fractional Divider Registers

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | FB_frctdiv[7:0] | The Feedback fractional divider has 24 bits divided amongst 3 registers (0x19, 0x1A and 0x1B). |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 39. RAM1 – 0x1C: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|---|
| D7 | 1 | calibration_start | Forces VCO band calibration manually. Needs to be toggled from 0 to 1 to activate the VCO calibration. |
| D6 | 0 | cnf_vreg[1:0] | LDO output voltage adjustment (00, 01, 10, 11). D6 D5 = 00 or 01 sets LDO to 1.1V, D6 D5 = 10 sets LDO to 1.2V, D6 D5 = 11 sets the LDO to 1.25V. |
| D5 | 0 | | |
| D4 | 0 | cnf_vreg_vco[1:0] | VCO regulator voltage adjustment (00, 01, 10, 11). D4 D3 = 00 or 01 sets LDO to 1.1V, D4 D3 = 10 sets LDO to 1.2V, D4 D3 = 11 sets the LDO to 1.25V. |
| D3 | 0 | | |

Table 39. RAM1 – 0x1C: Factory Reserved Bits (Cont.)

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|---|
| D2 | 1 | cnf_vco_bias[1:0] | VCO bias control (00, 01, 10, 11). |
| D1 | 0 | | D2 D1 = 00 or 01 sets LDO to 1.1V, D2 D1 = 10 sets LDO to 1.2V, D2 D1 = 11 sets the LDO to 1.25V. |
| D0 | 1 | | en_cp |

Note: The Timing Commander software sets more aggressive values in the 0x1C register for slightly improved performance. The Timing Commander software uses 0x1C = 9F# (1001 1111).

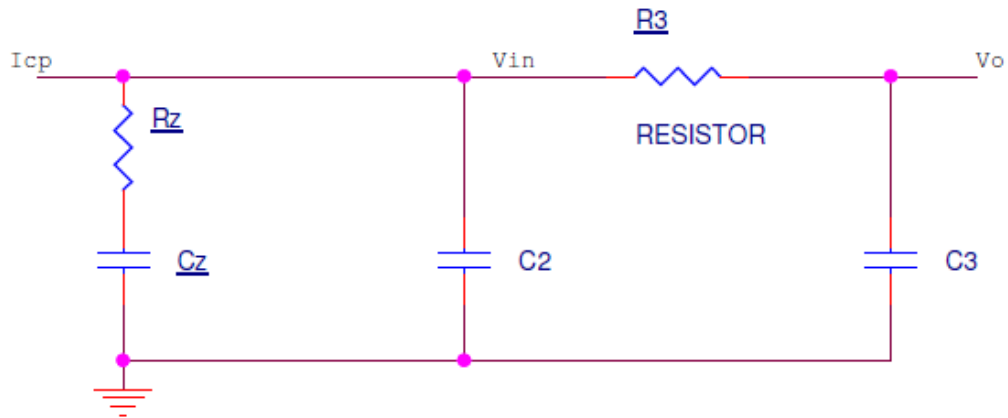
Table 40. RAM1 – 0x1D: Factory Reserved Bits

| Bits | Default Value | Name | Function |
|------|---------------|----------------|---|
| D7 | 0 | cfg_cp[3:0] | Charge-pump current control–Factory reserved bits. 30uA step from 0 to 450uA. |
| D6 | 1 | | |
| D5 | 1 | | |
| D4 | 0 | | |
| D3 | 1 | en_vco | Enable or disable the VCO block.VCO needs to be enabled by default. |
| D2 | 1 | i2c_bypb_dl | Bypass global reset. 0 means the reset is bypassed. 1 means the part will reset. Used to re-synchronize the outputs when reprogramming of the device is performed (default value). |
| D1 | 1 | vco_monitor_en | Enable VCO monitoring and select automatically the VCO band. |
| D0 | 1 | en_pll_bias | Enable or disable biasing blocks in the PLL. Active high. Enable by default. |

PLL Loop Filter Settings

Figure 4 below shows the Loop Filter components that are programmable via the RC control registers.

Figure 4. PLL Loop Filter Components



where

Rz is programmable with register 0x1E.

Cz is fixed and not programmable. Cz = 500pF.

C2 is the 2nd Pole capacitor and programmable with Register 0x1E.

R3 and C3 are the 3rd pole RC values programmable with register x1F.

The Icp charge pump current is programmable in register x1D.

Table 41. RAM1 – 0x1E: RC Control Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 1 | lpf_cnf_rz[4:0] | LPF resistor control, $R_z = (31 - \text{cnf_rz}) * 1.5\text{K}$. 1.5K = 11110. 46.5K = 00000. Setting 11111 is not allowed. |
| D6 | 0 | | |
| D5 | 1 | | |
| D4 | 1 | | |
| D3 | 1 | | |
| D2 | 0 | lpf_cnf_cp[2:0] | LPF 2nd pole capacitance control. 000 = 12pF to 100 = 28pF step of 4pF. Settings above 100 are not allowed. |
| D1 | 1 | | |
| D0 | 0 | | |

Table 42. RAM1 – 0x1F: RC Control Register

| Bits | Default Value | Name | Function |
|------|---------------|-------------|--|
| D7 | 0 | p3byp | Enable or disable bypass 3rd pole filter |
| D6 | 0 | cnf_p3[5:0] | 3rd pole RC configuration. Following values are programmable with bits D1 through D6: D3D2D1 = 001 → 2kOhm D6D5D4 = 001 → 1.8pF D3D2D1 = 010 → 8kOhm D6D5D4 = 011 → 3.6pF D3D2D1 = 011 → 1.6kOhm D6D5D4 = 111 → 5.4pF D3D2D1 = 100 → 1kOhm. D3D2D1 = 101 → 7kOhm. D3D2D1 = 110 → 5.3kOhm. D3D2D1 = 111 → 1.45kOhm. |
| D5 | 1 | | |
| D4 | 1 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 1 | | |
| D0 | 0 | cnf_pfdly | Phase Frequency Detector delay configuration bit |

Fractional Output Dividers and Spread Spectrum

The output dividers are composed of a 12 bit integer portion, ODx_intdiv[11:0] and a 24 bit fractional portion, ODx_frctdiv[23:0]. “x” is the output number.

$$ODx = INT(ODx) + FRAC(ODx) = FVCO / 2 / OUTx \quad (1)$$

Convert FRAC(ODx) to hex with Eq.2 where ROUND2INT means to round to the nearest integer. The round-off error of ODx in ppm is the output frequency error in ppm.

$$ODx_frctdiv[23:0] = DEC2HEX(ROUND2INT[224 * FRAC(ODx)]) \quad (2)$$

Example: The VCO is 2500MHz and the output needs to be 40MHz.

The output divider value needs to be $2500 / 2 / 40 = 31.25$.

Then $INT(ODx) = 31$ and $FRAC(ODx) = 0.25$ that gives:

$$2^{24} \times FRAC(ODx) = 2^{24} \times 0.25 = 4194304$$

$$ROUND2INT(4194304) = 4194304$$

$$ODx_frctdiv[23:0] = DEC2HEX(4194304) = 40\ 00\ 00$$

Spread spectrum capability is contained within the Fractional-N output dividers associated with each output clock. When applied, triangle wave modulation of any spread spectrum amount, SS%AMT, from ±0.25% to ±2.5% center spread and -0.5% to -5% down spread between 30 and 63kHz may be generated, independent of the output clock frequency. Five variables define spread spectrum in FODx (see [Table 43](#)).

Table 43. Spread Spectrum Variables in FODx

| Name | Function | RAM Register (see Table 23) | Register Length | Note |
|------------|---|---|-----------------|--|
| ODx_ssce | Spread spectrum control enable. | 0x25,0x35,0x45,0x55 | 1 | If ODx_ssce = 0, contents of ODx_period and ODx_step are Don't Care. |
| ODx_intdiv | Integer portion of the FODx divider, N. | 0x2D, 0x2E,0x3D,0x3E, 0x4D, 0x4E,0x5D,0x5E | 12 | |
| ODx_period | Spread spectrum modulation period. | 0x29,0x2A,0x39,0x3A, 0x49,0x4A,0x59,0x5A | 13 | Defined as half the reciprocal of the modulation frequency and measured in cycles of the FODx output frequency. See equation below. |
| ODx_step | Modulation step size. | 0x26,0x27,0x28,0x36, 0x37,0x38,0x46,0x47, 0x48,0x56,0x57,0x58 | 24 | Sets the time rate of change or time slope of the output clock frequency. |
| ODx_offset | Spread spectrum modulation offset, which defines down spread or center spread and is the fractional portion of the divider. | 0x22,0x23,0x24,0x25, 0x32,0x33,0x34,0x35, 0x42,0x43,0x44,0x45, 0x52,0x53,0x54,0x55 | 30 | ODx_offset is the actual spread spectrum offset subtracted from the Fractional portion of the FODx divider N. It is the fractional portion of the FODx divider and accounts for the fact that there is no ODx_frctdiv in the Memory map. |

To calculate the spread spectrum registers (fractional portion), first determine the value in decimal of the FOD output divider, N, for the nominal output frequency without spread spectrum. The VCO frequency is divided by two to account for a fixed divide by 2 between the VCO output and the input to the FOD. Convert the integer portion into hex to define ODx_intdiv.

$$N(dec) = INT(N) + FRAC(N) = \frac{(F_{VCO}/2)}{F_{OUT}} \tag{3}$$

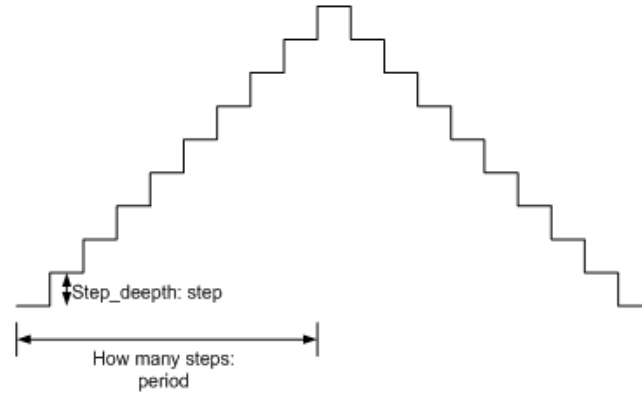
$$ODx_intdiv[11:0] = DEC2HEX(INT(N)) \tag{4}$$

If no spread is to be applied to FODx (ODx_ssce = 0) then ODx_period and ODx_step registers are don't Care and it is permissible to skip to Eq.9. Convert FRAC(N) to 30 bits as per Eq.10.

When the ODx_period and ODx_step registers are calculated below, ODx_period and ODx_step are explicitly set to 0 if ODx_ssce will always be 0. This is done for reasons of style, it reinforces the fact that there is no spread spectrum invoked when ODx_ssce = 0. If down spread is to be turned on by just setting ODx_ssce = 1, then ODx_period and ODx_step must be calculated and registered. See Eq.9 to see why changing only ODx_ssce works only for down spread.

Consider one cycle of down spread triangular modulation; the output divider, N, is ramped up linearly from the non-spread value of N followed by a linear ramp back down to the non-spread value of N. N is always greater than or equal to the non-spread value of N, therefore the output frequency is always less than or equal to the non-spread frequency.

Figure 5. Spread Step and Period



As normally defined, ODx_period (dec) would be $1/ F_{SS}$, but the modulation period is defined instead as $\frac{1}{2} * 1/ F_{SS}$ for the most direct calculation of ODx_step as will be seen below in the following Equations. An added benefit is that the up ramp and the down ramp are guaranteed to be symmetric. Note that ODx_period does not have units of time; it is the dimensionless number of F_{OUT} periods that fit in a half period of F_{SS} .

$$ODx_period(dec) = \begin{cases} 0 & \text{if } ssce = 0 \\ \frac{1}{2} * \frac{F_{OUT}}{F_{SS}} & \text{if } ssce = 1 \end{cases} \quad (5)$$

$$ODx_period[12:0] = DEC2HEX(ROUND2INT(ODx_period(dec))) \quad (6)$$

Calculate the step size.

$$ODx_step(dec) = \begin{cases} 0 & \text{if } ssce = 0 \\ \frac{SS\%AMT/100 * N}{ODx_period} & \text{if } ssce = 1 \end{cases} \quad (7)$$

$$ODx_step[23:0] = DEC2HEX(ROUND2INT(2^{24} * ODx_step(dec))) \quad (8)$$

Since the spread spectrum ramp as implemented only decreases the frequency of F_{OUT} , then the actual offset for down spread is zero. But if the spread is to be centered, an offset equal to half the peak modulation, $SS\%AMT * N$, is to be subtracted from the value of $FRAC(N)$.

$$ODx_offset(dec) = \begin{cases} FRAC(N) & \text{if } ssce = 0 \text{ or Down spread} \\ FRAC(N) - \frac{SS\%AMT/100 * N}{2} & \text{if } ssce = 1 \text{ and Center spread} \end{cases} \quad (9)$$

$$ODx_offset[29:0] = DEC2HEX(ROUND2INT[2^{24} * ODx_offset(dec)]) \quad (10)$$

If $FRAC(N)$ is a small positive value, it is possible that after the center spread offset is subtracted ODx_offset will be negative. In this case, retain only the lower 30 bits of the 32 bit hex value and assign them to $ODx_offset[29:0]$.

In this manner it can be seen that ODx_offset is the value of $FRAC(N)$, appropriately adjusted should center spread be enabled.

Example of FOD calculation for SSCE = 1

Out1 of clock1 = 99MHz, spread enabled with total spread 0.5% and SS 31.5KHz.

Feedback divider = 112.4, and VCO = 2810MHz. Let's calculate the FOD 1 value according to the equations above.

$F_{vco}/2 = 2810/2 = 1405$, and $F_{OUT} = 99\text{MHz}$ (given).

$(F_{vco}/2) / F_{OUT} = 1405/99 = 14.19191919$.

OD1 Integer = 14 then $ODx_intdiv[11:0] = E$.

As $ssce = 1$, $ODx_period(dec) = (\frac{1}{2}) * (F_{OUT} / FSS)$.

$F_{ss} = 31.5\text{kHz}$ and $F_{out} = 99\text{MHz}$ then **ODx_period(dec) = 1571.42857143**.

Now, from Eq.6, **ODx_period [12:0] = 623**.

From Eq.7, **ODx_Step(dec) = $[(0.5/100)*(14.19191919)] / 1571 = 0.00004516842$** .

From Eq.8 → $(0.00004516842 * 2^{24}) = 757.800338719$ then **ODx_Step [23:0] = 2F5**.

From Eq.9, **ODx_offset(dec) = $0.19191919 - ((0.5 / 100) * 14.19191919) / 2 = 0.15643939$** .

From Eq.10, $(2^{24} * 0.15643939) = 2624617.502$ → **Odx_offset [29:0] = 280C69**.

Some calculated examples with SSCE = 0 for frequency margining purposes:

Table 44. Table for PLL Configured Values

| | |
|-------------------|-----|
| input clock (MHz) | 25 |
| ref_div (real) | 0 |
| ref_div (Hex) | 0 |
| bypass_pre_div | 1 |
| Ref for PLL (MHz) | 25 |
| VCO (GHz) | 2.8 |
| FB_div (real) | 112 |
| FB_intdiv (Hex) | 70 |
| FB_frdiv (Hex) | 0 |

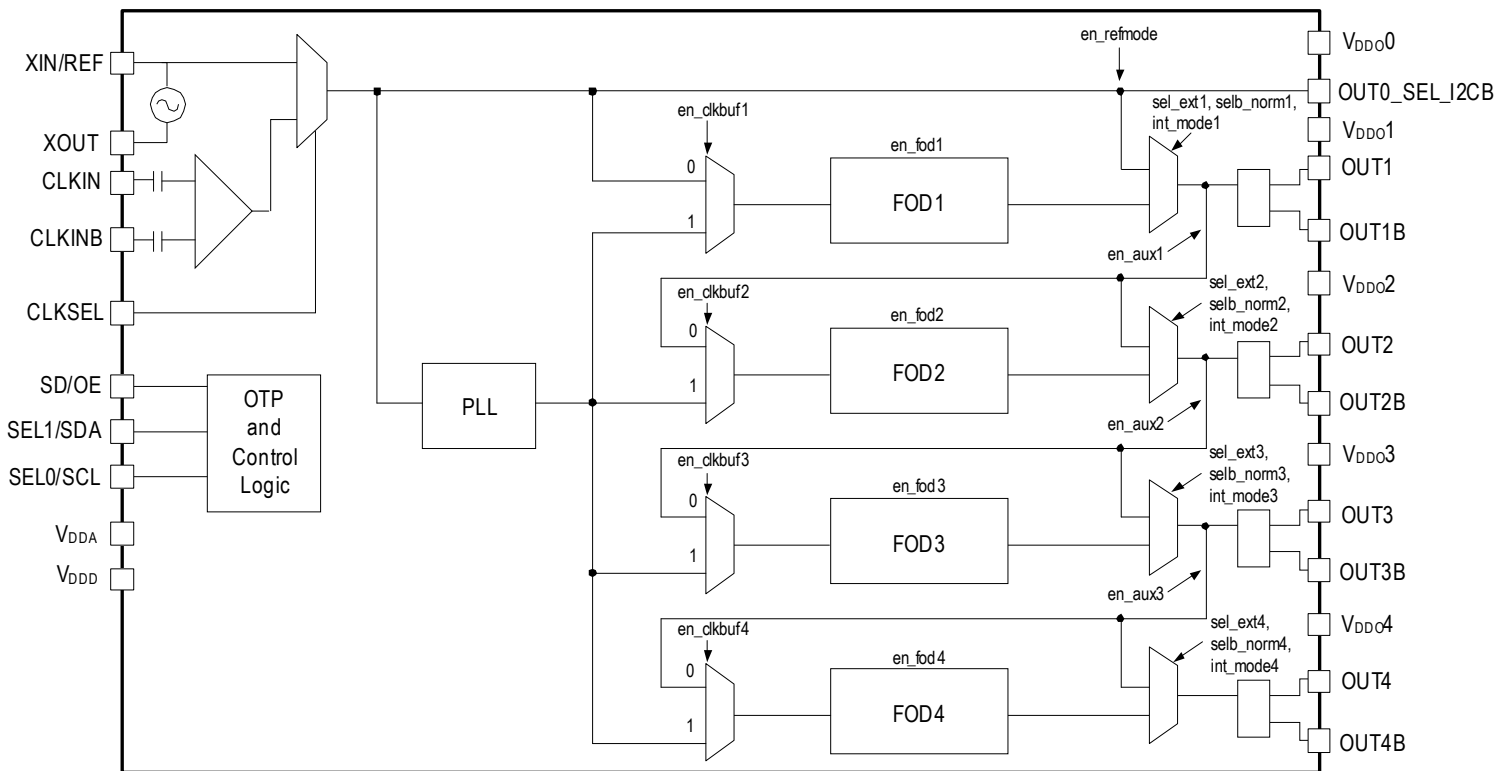
Table 45. Output Values with SSCE = 0

| Frequency Margining | Output (MHz) | ssce | Divider (real) | out_intdiv (HEX) | Period (Hex) | Step (real) | Step (HEX) | Offset (real) | Offset (HEX) | skew_int (HEX) | skew_frac (HEX) |
|---------------------|--------------|------|----------------|------------------|--------------|-------------|------------|---------------|--------------|----------------|-----------------|
| -3% | 97.1455 | 0 | 14.41137 | D | 0 | 0 | 0 | 1.411373 | 1694FB7 | 1 | 0 |
| -2% | 98.147 | 0 | 14.26432 | D | 0 | 0 | 0 | 1.264318 | 143AA55 | 0 | 0 |
| -1% | 99.1485 | 0 | 14.12023 | D | 0 | 0 | 0 | 1.120234 | 11EC7A4 | 0 | 0 |
| 0% | 100.15 | 0 | 13.97903 | D | 0 | 0 | 0 | 0.979031 | FAA1CE | 0 | 0 |
| 1% | 101.1515 | 0 | 13.84063 | D | 0 | 0 | 0 | 0.840625 | D73337 | 0 | 0 |
| 2% | 102.153 | 0 | 13.70493 | D | 0 | 0 | 0 | 0.704933 | B4767A | 0 | 0 |
| 3% | 103.1545 | 0 | 13.57188 | D | 0 | 0 | 0 | 0.571875 | 92666A | 0 | 0 |

Table 46. FOD1 Register Table

| Output (MHz) | Register Offsets | | | | | | | | | | | | | |
|--------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| | 0x22 | 0x23 | 0x24 | 0x25 | 0x26 | 0x27 | 0x28 | 0x29 | 0x2A | 0x2B | 0x2C | 0x2C | 0x2E | 0x2F |
| 97.1455 | 5 | A5 | 3E | DC | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 0 | D0 | 00 |
| 98.147 | 5 | 0E | A9 | 54 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 0 | D0 | 00 |
| 99.1485 | 4 | 7B | 1E | 90 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 0 | D0 | 00 |
| 100.15 | 3 | EA | 87 | 38 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 0 | D0 | 00 |
| 101.1515 | 3 | 5C | CC | DC | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 0 | D0 | 00 |
| 102.153 | 2 | D1 | D9 | E8 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 0 | D0 | 00 |
| 103.1545 | 2 | 49 | 99 | A8 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 0 | D0 | 00 |

Figure 6. Output Divider Control Settings Block Diagram



There are a number of MUX circuits to route clocks around and/or through certain fractional output dividers. For example, the output from FOD1 can be channeled to outputs 1 through 4 so only FOD1 needs to be enabled when all output frequencies are the same. There are also channeling options to use the output of one FOD to be the input of the following FOD so the output of that second FOD can be a very low frequency, for example a few kHz. Only when an FOD gets its input clock from the PLL can the fractional part of the divider be used. When using the clock from a previous output, the FOD can only be used in integer mode. The following pages explain how to set up the MUX.

Output Divider Control Settings (Table 47 through Table 50)

These bits are for Output divider's control register settings and are reserved in general. The reset bit for the FOD is active low. The combination of en_fod (fractional output divider enable bit), sel_ext (the output from previous channel FOD) and selb_norm (the output from current FOD), will set the divider mode. The integer mode only can be enabled with int_mode bit.

Table 47. RAM2 – 0x21: Output Divider 1 Control Register Settings

| Bits | Default Value | Name | Function |
|------|---------------|--------------------|---|
| D7 | 1 | i2c_resetb1 | Reset Fractional Output Divider 1 (FOD1) circuit when set to 0. |
| D6 | 0 | en_pi_out_cap<2:0> | Factory reserved /unused bits. |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | selb_norm1 | 0000: FOD1 and OUT1 are not used. |
| D2 | 0 | sel_ext1 | 00x1: FOD1 uses clock from PLL and OUT1 uses clock from FOD1. |
| D1 | 0 | int_mode1 | 1100: FOD1 disabled and OUT1 uses clock from OUT0. En_refmode needs to be 1. |
| D0 | 1 | en_fod1 | 1111: FOD1 uses clock from OUT0 and OUT1 uses clock from FOD1. En_refmode needs to be 1. "int_mode1" sets integer mode for FOD1 (fractional settings will be ignored). |

Table 48. RAM3 – 0x31: Output Divider 2 Control Register Settings

| Bits | Default Value | Name | Function |
|------|---------------|--------------------|--|
| D7 | 0 | i2c_resetb2 | Reset Fractional Output Divider 2 (FOD2) circuit when set to 0. |
| D6 | 0 | en_pi_out_cap<2:0> | Factory reserved /unused bits |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | selb_norm2 | 0000: FOD2 and OUT2 are not used. |
| D2 | 0 | sel_ext2 | 00x1: FOD2 uses clock from PLL and OUT2 uses clock from FOD2. |
| D1 | 0 | int_mode2 | 1100: FOD2 disabled and OUT2 uses clock from OUT1. En_aux1 needs to be 1. |
| D0 | 0 | en_fod2 | 1111: FOD2 uses clock from OUT1 and OUT2 uses clock from FOD2. En_aux1 needs to be 1. "int_mode2" sets integer mode for FOD2 (fractional settings will be ignored). |

Table 49. RAM4 – 0x41: Output Divider 3 Control Register Settings

| Bits | Default Value | Name | Function |
|------|---------------|--------------------|--|
| D7 | 0 | i2c_resetb3 | Reset Fractional Output Divider 3 (FOD3) circuit when set to 0. |
| D6 | 0 | en_pi_out_cap<2:0> | Factory reserved /unused bits. |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | selb_norm3 | 0000: FOD3 and OUT3 are not used. |
| D2 | 0 | sel_ext3 | 00x1: FOD3 uses clock from PLL and OUT3 uses clock from FOD3. |
| D1 | 0 | int_mode3 | 1100: FOD3 disabled and OUT3 uses clock from OUT2. En_aux2 needs to be 1. |
| D0 | 1 | en_fod3 | 1111: FOD3 uses clock from OUT2 and OUT3 uses clock from FOD3. En_aux2 needs to be 1. "int_mode3" sets integer mode for FOD3 (fractional settings will be ignored). |

Table 50. RAM5 – 0x51: Output Divider 4 Control Register Settings

| Bits | Default Value | Name | Function |
|------|---------------|--------------------|--|
| D7 | 0 | i2c_resetb4 | Reset Fractional Output Divider 4 (FOD4) circuit when set to 0. |
| D6 | 0 | en_pi_out_cap<2:0> | Factory reserved /unused bits. |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | selb_norm4 | 0000: FOD4 and OUT4 are not used. |
| D2 | 0 | sel_ext4 | 00x1: FOD4 uses clock from PLL and OUT4 uses clock from FOD4. |
| D1 | 0 | int_mode4 | 1100: FOD4 disabled and OUT4 uses clock from OUT3. En_aux3 needs to be 1. |
| D0 | 0 | en_fod4 | 1111: FOD4 uses clock from OUT3 and OUT4 uses clock from FOD4. En_aux3 needs to be 1. "int_mode4" sets integer mode for FOD1 (fractional settings will be ignored). |

Output Divider Integer Settings (Table 51 through Table 58)

Output divider's integer part consists of 12 bits spread on 2 consecutive registers. The 4 dividers are assigned to respectively to each output 1, 2, 3, 4.

Table 51. RAM2 – 0x2D: Output Divider 1 Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD1_intdiv[11:4] | Output divider 1 integer part has 12 bit spread over 2 registers x2D and x2E. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 52. RAM2 – 0x2E: Output Divider 1 Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 1 | OD1_intdiv[3:0] | Output divider 1 integer part has 12 bit spread over 2 registers x2D and x2E. |
| D6 | 1 | | |
| D5 | 1 | | |
| D4 | 0 | | |
| D3 | 0 | unused bits | Unused Factory reserved bit. |
| D2 | 0 | unused bits | Unused Factory reserved bit. |
| D1 | 0 | unused bits | Unused Factory reserved bit. |
| D0 | 0 | unused bits | Unused Factory reserved bit. |

Table 53. RAM3 – 0x3D: Output Divider 2 Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD2_intdiv[11:4] | Output divider 2 integer part has 12 bit spread over 2 registers x3D and x3E. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 54. RAM3 – 0x3E: Output Divider 2 Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 0 | OD2_intdiv[3:0] | Output divider 2 integer part has 12 bit spread over 2 registers x3D and x3E. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | unused bits | Unused Factory reserved bit. |
| D2 | 0 | unused bits | Unused Factory reserved bit. |
| D1 | 0 | unused bits | Unused Factory reserved bit. |
| D0 | 0 | unused bits | Unused Factory reserved bit. |

Table 55. RAM4 – 0x4D: Output Divider 3 Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD3_intdiv[11:4] | Output divider 3 integer part has 12 bit spread over 2 registers x4D and x4E. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 56. RAM4 – 0x4E: Output Divider 3 Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 0 | OD3_intdiv[3:0] | Output divider 3 integer part has 12 bit spread over 2 registers x4D and x4E. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | unused bits | Unused Factory reserved bit. |
| D2 | 0 | unused bits | Unused Factory reserved bit. |
| D1 | 0 | unused bits | Unused Factory reserved bit. |
| D0 | 0 | unused bits | Unused Factory reserved bit. |

Table 57. RAM5 – 0x5D: Output Divider 4 Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD4_intdiv[11:4] | Output divider 4 integer part has 12 bit spread over 2 registers x5D and x5E. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 58. RAM5 – 0x5E: Output Divider 4 Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 0 | OD4_intdiv[3:0] | Output divider 4 integer part has 12 bit spread over 2 registers X5D and x5E. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | unused bits | Unused Factory reserved bit. |
| D2 | 0 | unused bits | Unused Factory reserved bit. |
| D1 | 0 | unused bits | Unused Factory reserved bit. |
| D0 | 0 | unused bits | Unused Factory reserved bit. |

Output Divider Fractional and Spread Settings (Table 59 through Table 94)

ODx_offset is the actual spread spectrum offset subtracted from the Fractional portion of the FODx divider N. It is the fractional portion of the FODx divider. 30 bits spread over 4 registers. MSB is a sign bit. Set to 1 for negative numbers.

ODx_period bits are used to tune the spread rate from 30KHz to 63KHz according to the output frequency (period = Fout/Fss/2). 13 bits spread on 2 registers.

ODx_step is the Modulation step size; it sets the time rate of change or time slope of the output clock frequency. 24 bits spread on 3 registers.

If ODx_ssce = 0, contents of ODx_period and ODx_step are don't care only the ODx_offset are taken into account.

If ODx_ssce = 1, means the spread is enabled for center spread offset. (See example of spread calculation “[Example of FOD calculation for SSCE = 1](#)”)

Table 59. RAM2 – 0x22: Output Divider 1 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|---|
| D7 | 0 | OD1_offset[29:22] | 30 bits to configure the fraction value of FOD1 in register address. x22, x23, x24 and x25. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 60. RAM2 – 0x23: Output Divider 1 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|--|
| D7 | 0 | OD1_offset[21:14] | 30 bits to configure the fraction value of FOD1 in register address x22, x23, x24 and x25. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 61. RAM2 – 0x24: Output Divider 1 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD1_offset[13:6] | 30 bits to configure the fraction value of FOD1 in register address x22, x23, x24 and x25. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 62. RAM2 – 0x25: Output Divider 1 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | OD1_offset[5:0] | 30 bits to configure the fraction value of FOD1 in register address x22, x23, x24 and x25. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | OD1_ssce | Enable spread spectrum with center spread offset. Active High. |
| D0 | 0 | Unused | Unused Factory reserved bit. |

Table 63. RAM2 – 0x26: Output Divider 1 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|---------------|--|
| D7 | 0 | OD1_step[7:0] | 24 bits used for modulation step size in register x26 x27 and x28. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 64. RAM2 – 0x27: Output Divider 1 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|----------------|--|
| D7 | 0 | OD1_step[15:8] | 24 bits used for modulation step size in register x26 x27 and x28. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 65. RAM2 – 0x28: Output Divider 1 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | OD1_step[23:16] | 24 bits used for modulation step size in register x26 x27 and x28. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 66. RAM2 – 0x29: Output Divider 1 Spread Modulation Rate Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD1_period[12:5] | 13 bits used to configure spread modulation period in register x29 and x2A. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 67. RAM2 – 0x2A: Output Divider 1 Spread Modulation Rate Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 0 | OD1_period[4:0] | 13 bits used to configure spread modulation period in register x29 and x2A. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | Unused Bits | Unused Factory reserved bit. |
| D1 | 0 | Unused Bits | Unused Factory reserved bit. |
| D0 | 0 | Unused Bits | Unused Factory reserved bit. |

Table 68. RAM3 – 0x32: Output Divider 2 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD2_offset[29:6] | 30 bits to configure the fraction value of FOD2 in register address x32, x33, x34 and x35. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 69. RAM3 – 0x33: Output Divider 2 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD2_offset[29:6] | 30 bits to configure the fraction value of FOD2 in register address x32, x33, x34 and x35. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 70. RAM3 – 0x34: Output Divider 2 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD2_offset[29:6] | 30 bits to configure the fraction value of FOD2 in register address x32, x33, x34 and x35. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 71. RAM3 – 0x35: Output Divider 2 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | OD2_offset[5:0] | 30 bits to configure the fraction value of FOD2 in register address x32, x33, x34 and x35. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | OD2_ssce | Enable spread spectrum with center spread offset. Active High. |
| D0 | 0 | unused Bit | Unused Factory reserved bit. |

Table 72. RAM3 – 0x36: Output Divider 2 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|---------------|--|
| D7 | 0 | OD2_step[7:0] | 24 bits used for modulation step size in register x36 x37 and x38. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 73. RAM3 – 0x37: Output Divider 2 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|----------------|--|
| D7 | 0 | OD2_step[15:8] | 24 bits used for modulation step size in register x36 x37 and x38. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 74. RAM3 – 0x38: Output Divider 2 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | OD2_step[23:16] | 24 bits used for modulation step size in register x36 x37 and x38. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 75. RAM3 – 0x39: Output Divider 2 Spread Modulation Rate Configuring Register

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD2_period[12:5] | 13 bits used to configure spread modulation period in register x39 and x3A. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 76. RAM3 – 0x3A: Output Divider 2 Spread Modulation Rate Configuring Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 0 | OD2_period[4:0] | 13 bits used to configure spread modulation period in register x39 and x3A. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | unused bit | Unused Factory reserved bit. |
| D1 | 0 | unused bit | Unused Factory reserved bit. |
| D0 | 0 | unused bit | Unused Factory reserved bit. |

Table 77. RAM4 – 0x42: Output Divider 3 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD3_offset[29:6] | 30 bits to configure the fraction value of FOD3 in register address x42, x43, x44 and x45. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 78. RAM4 – 0x43: Output Divider 3 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD3_offset[29:6] | 30 bits to configure the fraction value of FOD3 in register address x42, x43, x44 and x45. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 79. RAM4 – 0x44: Output Divider 3 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD3_offset[29:6] | 30 bits to configure the fraction value of FOD3 in register address x42, x43, x44 and x45 |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 80. RAM4 – 0x45: Output Divider 3 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | OD3_offset[5:0] | 30 bits to configure the fraction value of FOD3 in register address x42, x43, x44 and x45. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | OD3_ssce | Enable spread spectrum with center spread offset. Active High. |
| D0 | 0 | unused | Unused Factory reserved bit. |

Table 81. RAM4 – 0x46: Output Divider 3 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|---------------|--|
| D7 | 0 | OD3_step[7:0] | 24 bits used for modulation step size in register x46 x47 and x48. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 82. RAM4 – 0x47: Output Divider 3 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|----------------|--|
| D7 | 0 | OD3_step[15:8] | 24 bits used for modulation step size in register x46 x47 and x48. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 83. RAM4 – 0x48: Output Divider 3 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | OD3_step[23:16] | 24 bits used for modulation step size in register x46 x47 and x48. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 84. RAM4 – 0x49: Output Divider 3 Spread Modulation Rate Configuring Register

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD3_period[12:5] | 13 bits used to configure spread modulation period in register x49 and x4A. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 85. RAM4 – 0x4A: Output Divider 3 Spread Modulation Rate Configuring Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 0 | OD3_period[4:0] | 13 bits used to configure spread modulation period in register x49 and x4A. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | unused | Unused Factory reserved bit. |
| D1 | 0 | unused | Unused Factory reserved bit. |
| D0 | 0 | unused | Unused Factory reserved bit. |

Table 86. RAM5 – 0x52: Output Divider 4 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD4_offset[29:6] | 30 bits to configure the fraction value of FOD4 in register addr. x52, x53, x54 and x55 |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 87. RAM5 – 0x53: Output Divider 4 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD4_offset[29:6] | 30 bits to configure the fraction value of FOD4 in register address X52, x53, x54 and x55. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 88. RAM5 – 0x54: Output Divider 4 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD4_offset[29:6] | 30 bits to configure the fraction value of FOD4 in register address x52, x53, x54 and x55. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 89. RAM5 – 0x55: Output Divider 4 Fractional Settings

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | OD4_offset[5:0] | 30 bits to configure the fraction value of FOD4 in register address x52, x53, x54 and x55. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | OD1_ssce | Enable spread spectrum with center spread offset. Active High. |
| D0 | 0 | Unused bits | Unused Factory reserved bit. |

Table 90. RAM5 – 0x56: Output Divider 4 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|---------------|--|
| D7 | 0 | OD4_step[7:0] | 24 bits used for modulation step size in register x56 x57 and x58. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 91. RAM5 – 0x57: Output Divider 4 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|----------------|--|
| D7 | 0 | OD4_step[15:8] | 24 bits used for modulation step size in register x56 x57 and x58. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 92. RAM5 – 0x58: Output Divider 4 Step Spread Configuration Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | OD4_step[23:16] | 24 bits used for modulation step size in register x56 x57 and x58. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 93. RAM5 – 0x59: Output Divider 4 Spread Modulation Rate Configuring Register

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD4_period[12:5] | 13 bits used to configure spread modulation period in register x59 and x5A. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 94. RAM5 – 0x5A: Output Divider 4 Spread Modulation Rate Configuring Register

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 0 | OD4_period[4:0] | 13 bits used to configure spread modulation period in register x59 and x5A. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | unused bits | Unused Factory reserved bit. |
| D1 | 0 | unused bits | Unused Factory reserved bit. |
| D0 | 0 | unused bits | Unused Factory reserved bit. |

Skew

Skew is not implemented with a parallel load of the count of the output divider as is commonly done with non-fractional divides. Instead skew is accomplished by increasing the value of the fractional output divider for only the very first clock cycle. The divide is increased by the number of VCO cycles required to delay the completion of the first output clock cycle by the desired skew. For the second and all subsequent output cycles, hardware changes the output divider to the value for the proper steady state output frequency. The integer and fractional components of skew are calculated as follows:

$$INT(Skew)(dec) = INT \left(\left[1 + \frac{Degrees\ of\ Skew}{360} \right] * N \right) - INT(N) \quad (11)$$

$$ODx_intskew[11:0] = DEC2HEX(INT(Skew)) \quad (12)$$

$$FRAC(Skew)(dec) = \left[1 + \frac{Degrees\ of\ Skew}{360} \right] * N - INT(N) - INT(skew) \quad (13)$$

$$ODx_frcskew[5:0] = DEC2HEX(INT[2^6 * FRAC(Skew)]) \quad (14)$$

There are 12 bits for an integer value and 6 bits for a fraction. The unit used for the skew is degrees of delay of the edge.

The VCO frequency is first divided by 2 before it goes to the Output Divider. The number programmed for skew is the amount of cycles of the VCO/2 frequency that is needed to achieve the skew amount.

Let's use an example of OUT1 = 100MHz, OUT2 = 100MHz and we want to delay OUT1 with 1.3ns versus OUT2. The total cycle is 10ns so 1.3ns represents $360 \times 1.3/10 = 46.8^\circ$ of skew. Let's also say that we used VCO = 2800MHz so the Output Divider value N = $(2800/2)/100 = 14$. Each cycle of the VCO/2 = 1400MHz signal represents $360/14 = 25.7^\circ$. That means the skew number will be $46.8/25.7 = 1.82$. The integer part of the skew will be 1 and the fractional setting will be $INT(0.82 \times 2^6) = 52$ or 34 hex.

The formulas for skew are as follows:

Formula for the integer value:

$$INT(Skew)(dec) = INT \left(\left[1 + \frac{Degrees\ of\ Skew}{360} \right] * N \right) - INT(N)$$

Formula for the fraction:

$$FRAC(Skew)(dec) = \left[1 + \frac{Degrees\ of\ Skew}{360} \right] * N - INT(N) - INT(skew)$$

$$INT(Skew) = INT((1+46.8/360)*14) - INT(14) = 15 - 14 = 1.$$

$$FRAC(Skew) = (1+46.8/360)*14 - INT(14) - 1 = 0.82.$$

Translating these two values to register settings:

$$ODx_intskew[11:0] = DEC2HEX(INT(Skew)) = 001 \text{ (hex)}$$

$$ODx_frcskew[5:0] = DEC2HEX(INT[2^6 * FRAC(Skew)]) = 34 \text{ (hex)}$$

To apply the 1.3ns skew on OUT1, write the following values:

Addr – Byte

0x2B – 00

0x2C – 10

0x2F – 74

After writing these values all counters need to be restarted to insert the 1.3ns delay in OUT1 versus the other outputs. The restarting can be done by toggling the I²C global reset in bit 5 of register 0x76. First read register 0x76 to know the setting of all bits. Bit 5 will be “1” when the outputs are running. Commonly the value of 0x76 will be E3 (hex) and I am assuming this value in the example code below. The full code to set the 1.3ns skew on the fly will look as follows:

Addr – Byte

0x2B – 00 (OD1_intskew[11:4] = 00, most likely it is already 00; if so, skip this line)

0x2C – 10 (OD1_intskew[3:0] = 1)

0x2F – 74 (OD1_frskew[5:0] = 74)

0x76 – C3 (Set I2C_Global_Reset)

0x76 – E3 (Release I2C_Global_Reset)

Removing the skew again:

0x2B – 00

0x2C – 00

0x2F – 00

0x76 – C3

0x76 – E3

After writing these values on the fly, all counters need to be restarted to insert the 1.3ns delay in OUT1 versus the other outputs.

Output Divider Skew Integer and Fractional Part Registers Settings (Table 95 through Table 107)

The 12 bits integer part of the skew are spread over 2 registers for each output divider and 6 bits are used to configure the fractional part of the skew.

Table 95. RAM2 – 0x2B: Output Divider 1 Skew Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|---|
| D7 | 0 | OD1_intskew[11:4] | 12 bits are used to set Output Divider 1 skew integer part in register x2B and x2C. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 96. RAM2 – 0x2C: Output Divider 1 Skew Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|------------------|---|
| D7 | 0 | OD1_intskew[3:0] | 12 bits are used to set Output Divider 1 skew integer part in register x2B and x2C. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | unused bits | Unused Factory reserved bit. |
| D2 | 0 | unused bits | Unused Factory reserved bit. |
| D1 | 0 | unused bits | Unused Factory reserved bit. |
| D0 | 0 | en_aux | Factory reserved bit. |

Table 97. RAM2 – 0x2F: Output Divider 1 Skew Fractional Part

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|---|
| D7 | 0 | unused bits | Unused Factory reserved bit. |
| D6 | 0 | unused bits | Unused Factory reserved bit. |
| D5 | 0 | OD1_frskew[5:0] | 6 bits are used to set Output Divider 1 Skew fractional part. |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 98. RAM3 – 0x3B: Output Divider 2 Skew Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|---|
| D7 | 0 | OD2_intskew[11:4] | 12 bits are used to set Output Divider 2 skew integer part in register x3B and x3C. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 99. RAM3 – 0x3C: Output Divider 2 Skew

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD2_intskew[3:0] | 12 bits are used to set Output Divider2 skew integer part in register x3B and x3C. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | unused bits | Unused Factory reserved bit. |
| D2 | 0 | unused bits | Unused Factory reserved bit. |
| D1 | 0 | unused bits | Unused Factory reserved bit. |
| D0 | 0 | en_aux | Factory reserved bit. |

Table 100. RAM3 – 0x3F: Output Divider 2 Skew Fractional Part

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | unused bits | Unused Factory reserved bit. |
| D6 | 0 | unused bits | Unused Factory reserved bit. |
| D5 | 0 | OD2_frskew[5:0] | 6 bits are used to set Output Divider2 skew fractional part. |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 101. RAM4 – 0x4B: Output Divider 3 Skew Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|--|
| D7 | 0 | OD3_intskew[11:4] | 12 bits are used to set Output Divider3 skew integer part in register x4B and x4C. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 102. RAM4 – 0x4C: Output Divider 3 Skew

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD3_intskew[3:0] | 12 bits are used to set Output Divider3 skew integer part in register x4B and x4C. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | unused bits | Unused Factory reserved bit. |
| D2 | 0 | unused bits | Unused Factory reserved bit. |
| D1 | 0 | unused bits | Unused Factory reserved bit. |
| D0 | 0 | en_aux | Factory reserved bit. |

Table 103. RAM4 – 0x4F: Output Divider 3 Skew Fractional Part

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | unused bits | Unused Factory reserved bit. |
| D6 | 0 | unused bits | Unused Factory reserved bit. |
| D5 | 0 | OD3_frskew[5:0] | 6 bits are used to set Output Divider3 skew fractional part. |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 104. RAM5 – 0x50: Unused Factory Reserved Register

| Bits | Default Value | Name | Function |
|------|---------------|------------------------------|-------------------------------|
| D7 | 0 | unused factory reserved bits | Unused Factory reserved bits. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 105. RAM5 – 0x5B: Output Divider 4 Skew Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|--|
| D7 | 0 | OD4_intskew[11:4] | 12 bits are used to set Output Divider4 skew integer part in register x5B and x5C. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Table 106. RAM5 – 0x5C: Output Divider 4 Skew Integer Part

| Bits | Default Value | Name | Function |
|------|---------------|------------------|--|
| D7 | 0 | OD4_intskew[3:0] | 12 bits are used to set Output Divider4 skew integer part in register x5B and x5C. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | unused bits | Unused Factory reserved bit. |
| D2 | 0 | unused bits | Unused Factory reserved bit. |
| D1 | 0 | unused bits | Unused Factory reserved bit. |
| D0 | 0 | en_aux | Factory reserved bit. |

Table 107. RAM5 – 0x5F: Output Divider 4 Skew Fractional Part

| Bits | Default Value | Name | Function |
|------|---------------|-----------------|--|
| D7 | 0 | unused bits | Unused Factory reserved bit. |
| D6 | 0 | unused bits | Unused Factory reserved bit. |
| D5 | 0 | OD4_frskew[5:0] | 6 bits are used to set Output Divider4 skew fractional part. |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | | |
| D1 | 0 | | |
| D0 | 0 | | |

Clock Output Configurations Registers

In Clock Output Configuration registers described in the tables below, the CLKx_pwr_sel bits must be configured to match the clock outputs' supply voltages applied externally. The bits don't adjust the clock output signal swings. CMOSX2 provides two phase-coherent single ended CMOS outputs while CMOSD provides 2 signals out of phase by 180degree. In Clock2 Output Configuration, bits are for disabling/enabling clock output/value and slew rate for differential outputs.

Table 108. RAM6 – 0x60: Clock1 Output Configuration

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|--|
| D7 | 1 | CLK1_cfg[2] | These bits give us the output type configuration mode. For D7, D6, D5 respectively: (D7, D6, D5) = 000: low-voltage positive/pseudo emitter-coupled logic (LVPECL); (D7, D6, D5) = 001: CMOS; (D7, D6, D5) = 010: HCSL33; (D7, D6, D5) = 011: Low Voltage Differential Signal (LVDS); (D7, D6, D5) = 100: CMOS2; (D7, D6, D5) = 101: CMOSD; (D7, D6, D5)= 110: HCSL25. |
| D6 | 0 | CLK1_cfg[1] | |
| D5 | 1 | CLK1_cfg[0] | |
| D4 | 1 | clk1_pwr_sel[1:0] | Output Drive Voltage is set by those bits. D4 D3 = 00 sets 1.8V. D4 D3 = 10 sets 2.5V. D4 D3 = 11 sets 3.3V. |
| D3 | 1 | | |
| D2 | 0 | unused bits | Factory reserved unused bits. |
| D1 | 1 | CLK1_slew[1] | Slew rate control for CMOS single-ended. D1 D0 = 00 then output slew rate is 0.8*Normal. D1 D0 = 01 then output slew rate indicates 0.85*Normal. D1 D0 = 10 then output slew rate indicates 0.9*Normal. D1 D0 = 11 then output slew rate indicates 1*Normal. |
| D0 | 1 | CLK1_slew[0] | |

Table 109. RAM6 – 0x61: Clock1 Output Configuration

| Bits | Default Value | Name | Function |
|------|---------------|---------------------|--|
| D7 | 0 | CLK1_slew_diff[5:0] | Unused register bits. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | SDOE_CLK1 | SDOE_CLK1 = 1 causes OUT1 to disable to Hi-Z when disabled with SD/OE pin. SDOE_CLK1 = 0 causes OUT1 to disable to High/Low when disabled with SD/OE pin. |
| D1 | 0 | clk1_amuxen2 | This bit is used to disable the output value. Active High (1) to disable output. |
| D0 | 1 | en_clkbuf1 | This bit is used to enable the clock output. Active High (1) to enable the clock output. |

Table 110. RAM6 – 0x62: Clock2 Output

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|---|
| D7 | 0 | CLK2_cfg[2] | These bits give us the output type configuration mode. For D7, D6, D5 respectively: (D7, D6, D5) = 000: low-voltage positive/pseudo emitter-coupled logic (LVPECL); (D7, D6, D5) = 001: CMOS; (D7, D6, D5) = 010: HCSL33; (D7, D6, D5) = 011: Low Voltage Differential Signal (LVDS); (D7, D6, D5) = 100: CMOS2; (D7, D6, D5) = 101: CMOSD; (D7, D6, D5) = 110: HCSL25. |
| D6 | 1 | CLK2_cfg[1] | |
| D5 | 0 | CLK2_cfg[0] | |
| D4 | 1 | clk2_pwr_sel[1:0] | Output Drive Voltage is set by those bits. D4 D3 = 00 sets 1.8V. D4 D3 = 10 sets 2.5V. D4 D3 = 11 sets 3.3V. |
| D3 | 1 | | |
| D2 | 0 | unused bit | Unused Factory reserved bit. |
| D1 | 1 | CLK2_slew[1] | Slew rate control for CMOS single-ended. D1 D0 = 00 then output slew rate is 0.8*Normal. D1 D0 = 01 then output slew rate indicates 0.85*Normal. D1 D0 = 10 then output slew rate indicates 0.9*Normal. D1 D0 = 11 then output slew rate indicates 1*Normal. |
| D0 | 1 | CLK2_slew[0] | |

Table 111. RAM6 – 0x63: Clock2 Output Configuration

| Bits | Default Value | Name | Function |
|------|---------------|---------------------|--|
| D7 | 0 | CLK2_slew_diff[5:0] | Unused register bits. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | SDOE_CLK2 | SDOE_CLK2 = 1 causes OUT2 to disable to Hi-Z when disabled with SD/OE pin. SDOE_CLK2 = 0 causes OUT2 to disable to High/Low when disabled with SD/OE pin. |
| D1 | 0 | clk2_amuxen2 | This bit is used to disable the output value. Active High (1) to disable output. |
| D0 | 0 | en_clkbuf2 | This bit is used to enable the clock output. Active High (1) to enable the clock output. |

Table 112. RAM6 – 0x64: Clock3 Output

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|--|
| D7 | 0 | CLK3_cfg[2] | These bits give us the output type configuration mode. For D7, D6, D5 respectively: (D7, D6, D5) = 000: low-voltage positive/pseudo emitter-coupled logic (LVPECL); (D7, D6, D5) = 001: CMOS; ((D7, D6, D5) = 010: HCSL33; (D7, D6, D5) = 011: Low Voltage Differential Signal (LVDS); (D7, D6, D5) = 100: CMOS2; (D7, D6, D5) = 101: CMOSD; (D7, D6, D5) = 110: HCSL25. |
| D6 | 1 | CLK3_cfg[1] | |
| D5 | 1 | CLK3_cfg[0] | |
| D4 | 1 | clk3_pwr_sel[1:0] | Output Drive Voltage is set by those bits. D4 D3 = 00 sets 1.8V. D4 D3 = 10 sets 2.5V. D4 D3 = 11 sets 3.3V. |
| D3 | 1 | | |
| D2 | 0 | unused bit | Unused Factory reserved bit. |
| D1 | 1 | CLK3_slew[1] | Slew rate control for CMOS single-ended. D1 D0 = 00 then output slew rate is 0.8*Normal. D1 D0 = 01 then output slew rate indicates 0.85*Normal. D1 D0 = 10 then output slew rate indicates 0.9*Normal. D1 D0 = 11 then output slew rate indicates 1*Normal. |
| D0 | 1 | CLK3_slew[0] | |

VersaClock 6E products 5P49V6967 and 5P49V6968 have LVCMOS outputs on output 3. Therefore, bits D7, D6 and D5 in registers 0x64 should be set to 001 and D4 and D3 set to 00 to implement the same.

Table 113. RAM6 – 0x65: Clock3 Output Configuration

| Bits | Default Value | Name | Function |
|------|---------------|---------------------|--|
| D7 | 0 | CLK3_slew_diff[5:0] | Unused register bits. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | SDOE_CLK3 | SDOE_CLK3 = 1 causes OUT3 to disable to Hi-Z when disabled with SD/OE pin. SDOE_CLK3 = 0 causes OUT3 to disable to High/Low when disabled with SD/OE pin. |
| D1 | 0 | clk3_amuxen2 | This bit is used to disable the output value. Active High (1) to disable output. |
| D0 | 0 | en_clkbuf3 | This bit is used to enable the clock output. Active High (1) to enable the clock output. |

Table 114. RAM6 – 0x66: Clock4 Output

| Bits | Default Value | Name | Function |
|------|---------------|-------------------|---|
| D7 | 0 | CLK4_cfg[2] | These bits give us the output type configuration mode. For D7,D6,D5 respectively: (D7,D6,D5) = 000: low-voltage positive/pseudo emitter-coupled logic (LVPECL); (D7,D6,D5) = 001: CMOS; (D7,D6,D5) = 010: HCSL33; (D7,D6,D5) = 011: Low Voltage Differential Signal (LVDS); (D7,D6,D5) = 100: CMOS2; (D7,D6,D5) = 101: CMOSD; (D7,D6,D5) = 110: HCSL25. |
| D6 | 0 | CLK4_cfg[1] | |
| D5 | 0 | CLK4_cfg[0] | |
| D4 | 1 | clk4_pwr_sel[1:0] | Output Drive Voltage is set by those bits. D4 D3 = 00 sets 1.8V. D4 D3 = 10 sets 2.5V. D4 D3 = 11 sets 3.3V. |
| D3 | 1 | | |
| D2 | 0 | Unused Bit | Unused Factory reserved bit. |
| D1 | 1 | CLK4_slew[1] | Slew rate control for CMOS single-ended. D1 D0 = 00 then output slew rate is 0.8*Normal. D1 D0 = 01 then output slew rate indicates 0.85*Normal. D1 D0 = 10 then output slew rate indicates 0.9*Normal. D1 D0 = 11 then output slew rate indicates 1*Normal. |
| D0 | 1 | CLK4_slew[0] | |

Table 115. RAM6 – 0x67: Clock4 Output Configuration

| Bits | Default Value | Name | Function |
|------|---------------|---------------------|--|
| D7 | 0 | CLK4_slew_diff[5:0] | Unused register bits. |
| D6 | 0 | | |
| D5 | 0 | | |
| D4 | 0 | | |
| D3 | 0 | | |
| D2 | 0 | SDOE_CLK4 | SDOE_CLK4 = 1 causes OUT4 to disable to Hi-Z when disabled with SD/OE pin. SDOE_CLK4 = 0 causes OUT4 to disable to High/Low when disabled with SD/OE pin. |
| D1 | 0 | clk4_amuxen2 | This bit is used to disable the output value. Active High (1) to disable output. |
| D0 | 0 | en_clkbuf4 | This bit is used to enable the clock output. Active High (1) to enable the clock output. |

Table 116. Power Up VDD check

VersaClock 6E products verify that all VDDs have ramped up before starting the configuration of circuits with settings from OTP. Because of this feature, any VDD sequence can be used. For every output there is 1 bit to tell the chip to skip the verification of that output's VDD. This bit can be used when the output is not used and the VDD will not be connected. It is still recommended to connect the VDD, but no longer mandatory to allow the chip to start.

| Register | Bits | Default Value | Name | Function |
|----------|------|---------------|--------------|--|
| 0x20 | D7 | 0 | bypass_sync1 | “bypass_sync1” = 0: Include VDDO1 in VDD verification. “bypass_sync1” = 1: Skip VDDO1 verification. |
| 0x30 | D7 | 0 | bypass_sync2 | “bypass_sync2” = 0: Include VDDO2 in VDD verification. “bypass_sync2” = 1: Skip VDDO2 verification. |
| 0x40 | D7 | 0 | bypass_sync3 | “bypass_sync3” = 0: Include VDDO3 in VDD verification. “bypass_sync3” = 1: Skip VDDO3 verification. |
| 0x50 | D7 | 0 | bypass_sync4 | “bypass_sync4” = 0: Include VDDO4 in VDD verification. “bypass_sync4” = 1: Skip VDDO4 verification. |

Revision History

| Revision Date | Description of Change |
|------------------|---|
| November 5, 2024 | <ul style="list-style-type: none"> ▪ Updated Address 0x00 write data register values in Table 6. ▪ Changed default value for bit D5 to 0 from 1 in Table 25. ▪ Changed default value for bits D7 and D6 to 0 from 1 in Table 33. ▪ Updated hex values from 116 and 74 to 52 and 34 in Skew section. |
| July 1, 2022 | <ul style="list-style-type: none"> ▪ Added note 4 in VersaClock 6E Family Power-Up Behavior section. |
| August 30, 2018 | <ul style="list-style-type: none"> ▪ Removed references for 5P49V60. ▪ Added value for Cz in PLL Loop Filter Settings section. |
| November 6, 2017 | Initial release. |

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TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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