Connecting a Neuron® 5000 Processor to an External Transceiver

July 2011 **LonWorks® Engineering Bulletin**

The Echelon® Neuron® 5000 Processor provides a media-independent communications port that can be configured to interface to a wide variety of media interfaces (network transceivers). The communications port consists of five pins (named CP0 through CP4) and can operate over a wide range of data rates. This Engineering Bulletin describes how to connect a Neuron 5000 Processor's communications port to external transceivers for TP/XF-1250 channels or for EIA-485 networks, using an external transceiver circuit. It also describes how to connect a Neuron 5000 Processor to a link-power TP/FT-10 channel using a LONWORKS LPT-11 Link Power Transceiver. Use an FT 5000 Smart Transceiver for a standard (non-link-powered) TP/FT-10 channel or for a locally powered device on a link-power TP/FT-10 channel.

The Neuron 5000 Processor's communications port can be configured to operate in one of two modes: single-ended mode or special-purpose mode. Single-ended mode is most commonly used with external active transceivers that interface to media such as RF, IR, fiber optics, twisted-pair cable, and coaxial cable. Special-purpose mode is used for custom transceivers that require unencoded data and that perform their own data formatting and packet management. For standard TP/XF-1250 channels, EIA-485 networks, or for the LONWORKS LPT-11 Link Power Transceiver, the Neuron 5000 Processor's communications port is configured to operate in 3.3 V single-ended mode.

Table 1 lists the pin assignments for the communications port pins for single-ended mode. Data communication occurs through the single-ended (with respect to GND) input and output buffers on pins CP0 and CP1.

Table 1. Communications Port Pin Assignments for Single-Ended Mode

Pin	Name	Drive Current	Single-Ended Mode (3.3 V)	Connect To
32	CP0	N/A	Data input	Transceiver RXD
34	CP1	8 mA	Data output	Transceiver TXD
37	CP2	8 mA	Transmit Enable output	Transmit Enable
38	CP3	N/A	Do Not Connect	
39	CP4	N/A	Collision Detect input	10 kΩ pullup resistor

Before programming, a Neuron 5000 Processor uses its default communications parameters, which define a simplified single-ended mode 78 kbps channel. The default communications parameters allow you to load an application image over a 78 kbps network, for example during device manufacturing. Devices that use a 78 kbps transceiver (such as a 78 kbps EIA-485 transceiver or a TP/FT-10 LPT-11 Link Power Transceiver) can use the default communications parameters within development or manufacturing test networks. For production networks (networks with many devices), you should ensure that each device has communications parameters defined for the channel; use the NodeBuilder FX Development Tool or the Mini FX Evaluation Kit to develop applications with the correct communications parameters. Note that devices defined for a TP/XF-1250 channel cannot use the default communications parameters; each device's external serial non-volatile memory must be loaded with the correct communications parameters before connecting to the network.

See Chapter 2 of the *Series 5000 Chip Data Book* (005-0199-01B) for more information about the communications port and single-ended mode.

TPT/XF-1250 Transceivers

You can use the Neuron 5000 Processor with an Echelon TPT Twisted Pair Transceiver Module for a TP/XF-1250 channel. However, because the Neuron 5000 Processor does not include an on-chip differential transceiver (that is, the Neuron 5000 Processor does not support the differential mode of operation that Neuron 3120® Chips and Neuron 3150® Chips support), you must:

- Select "TP/XF-1250" as the transceiver type within the Hardware Template Editor of the NodeBuilder® FX Development Tool or the Mini FX Evaluation Kit. Within this template, select "Neuron 5000" as the Neuron Chip Model. Using the TP/XF-1250 template causes the Neuron firmware to configure the Neuron 5000 Processor's communications port to operate in 3.3 V single-ended mode.

  Important: Select a clock multiplier of at least 2 (to use a 20, 40, or 80 MHz system clock).

- Add a single-ended mode to differential mode converter circuit, as described in *Differential Driver Circuit* on page 3, and a differential comparator circuit as described in *Comparator Circuit* on page 4. These circuits convert the Neuron 5000 Processor's 3.3 V single-ended mode signals to the 5 V differential mode signals required for the TPT/XF-1250 transceiver.

Figure 1 on page 3 shows the basic configuration for connecting a Neuron 5000 Processor to a TPT/XF-1250 transceiver.

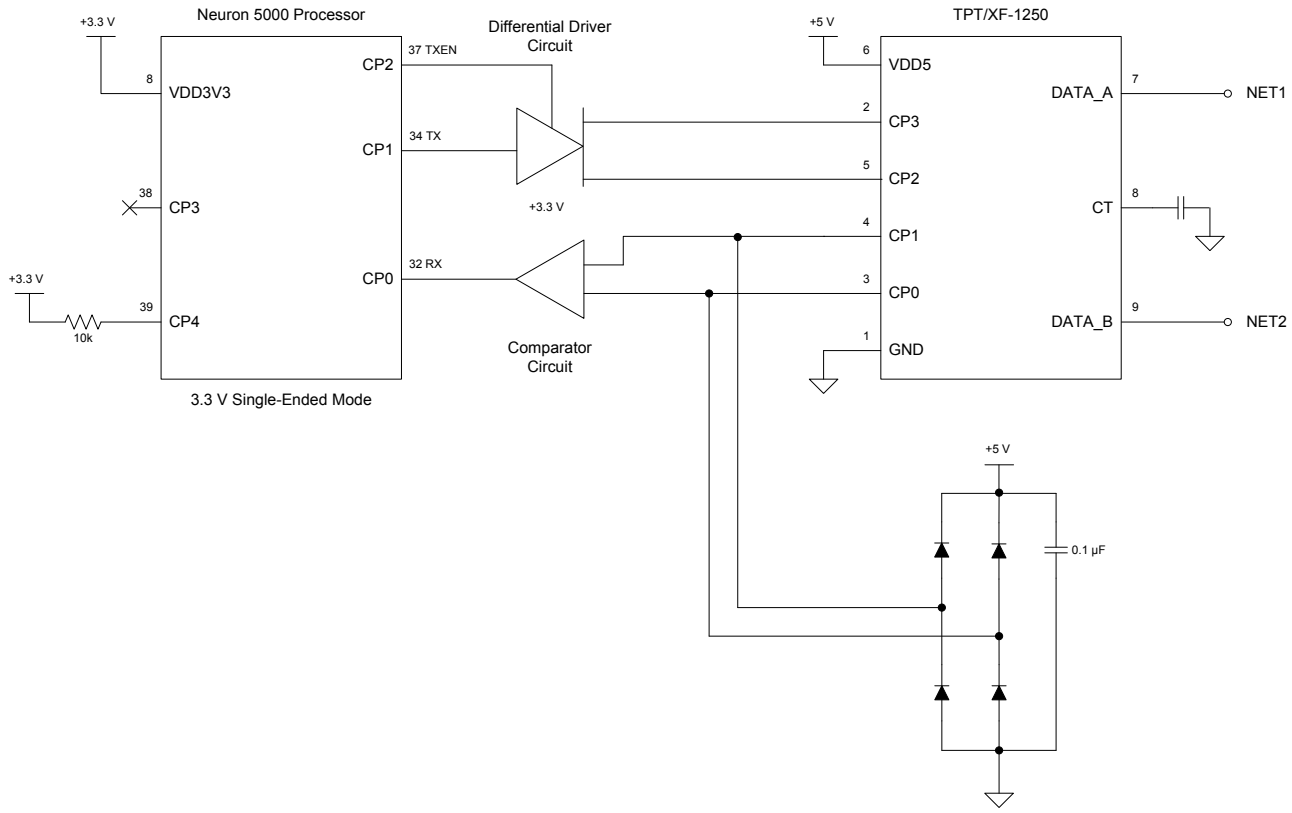

Figure 1. Connecting a Neuron 5000 Processor to a TP/XF-1250 Transceiver

In the figure, the pullup resistor for the Neuron 5000 Processor's CP4 pin is optional, but helps prevent contention on the CP4 pin if the Neuron Processor is incorrectly configured to operate in special-purpose mode (for which the CP4 pin is an output). The diode clamps for the TPT/XF-1250 transceiver's CP0 and CP1 signals are high-speed switching diodes, such as Fairchild Semiconductor® 1N4148 small-signal diodes. The value of the capacitor on the TPT/XF-1250 transceiver's transformer center tap (CT) pin depends on the device's PCB layout and EMI characteristics. A typical value is 100 pF rated for 1000 V.

See the *LonWorks TPT Twisted Pair Transceiver Module User's Guide* (078-0025-01C) for information about the TPT/XF-1250 Transceiver.

Differential Driver Circuit

Figure 2 on page 4 shows a differential driver circuit for connecting a Neuron 5000 Processor to a TPT/XF-1250 transceiver. The differential driver circuit buffers the Neuron 5000 Processor's transmit (CP1) signal and transmit enable (CP2) signal to generate the TPT/XF-1250 transceiver's differential transmit signals (CP2 and CP3).

The heart of the differential driver circuit is a pair of 4-bit buffers/drivers in a single 74HCT240 octal inverting buffer/line driver (such as the Texas Instruments™ SN74HCT240 Octal Buffer and Line Driver with 3-State Outputs).

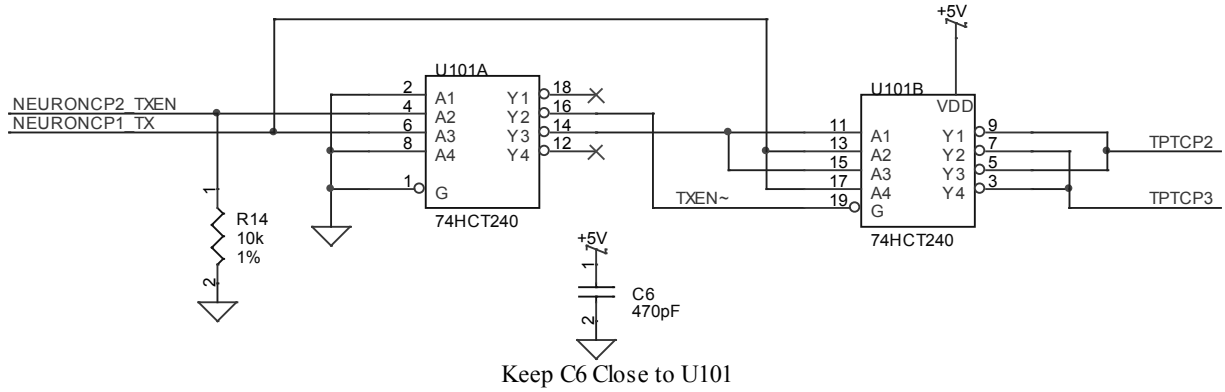

Figure 2. Differential Driver Circuit

Table 2. Bill of Materials for the Differential Driver Circuit

Designator	Value
C6	470 pF
R14	10 kΩ, 1%
U101	SN74HCT240

Comparator Circuit

Figure 3 on page 5 shows a differential comparator circuit for connecting a Neuron 5000 Processor to a TPT/XF-1250 transceiver. The differential comparator circuit drives the Neuron 5000 Processor's receive (CP0) signal based on the TPT/XF-1250 transceiver's differential receive signals (CP0 and CP1).

The heart of the differential comparator circuit is a dual, high speed voltage feedback operational amplifier (such as an Analog Devices AD826 Low Cost, High Speed, Low Power Dual Operational Amplifier) and a high-speed comparator (such as a Linear Technology LT1016 Ultra Fast Precision 10ns Comparator). The operational amplifiers buffer the differential receive signal and form a low-pass filter. The comparator interfaces directly to TTL/CMOS logic while operating off the same 5 V power supply as the TPT/XF-1250 transceiver or a separate 5 V analog power supply (VA).

Important: Because capacitor C4 with resistors R7 and R8 act as a low-pass filter for the differential signal, be sure to keep the traces between them and U103 as short as possible. Excessive trace capacitance can lower the filter's cutoff frequency, which can cause signal loss from the TPT/XF-1250 transceiver.

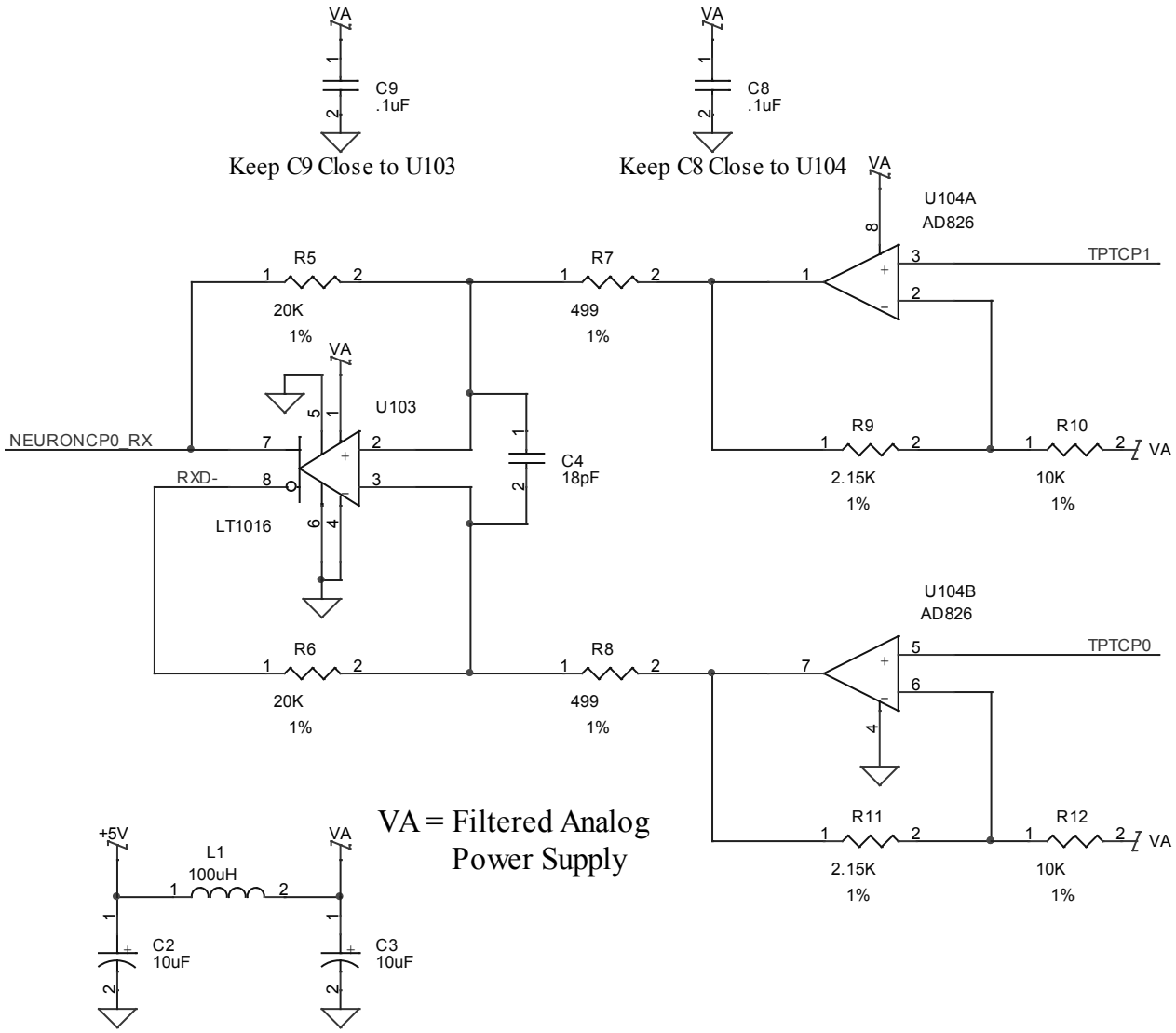

Figure 3. Differential Comparator Circuit

Table 3. Bill of Materials for the Differential Comparator Circuit

Designator	Value
C2, C3	10 μF
C4	18 pF
C8, C9	0.1 μF
L1	100 μH, ±20%, I_{sat} ≥ 100 mA, DCR ≤ 0.5 Ω
R5, R6	20 kΩ, 1%
R7, R8	499 Ω, 1%
R9, R11	2.15 kΩ, 1%
R10, R12	10 kΩ, 1%
U103	LT1016CN8
U104	AD826AN

PCB Layout Guidelines

Printed circuit board (PCB) layout for a Neuron 5000 Processor should include the following general features:

- Star-Ground Configuration: Arrange the various blocks of the device that directly interface with off-board connections (the network, any external I/O, and the power supply cable) so that they are together along one edge of the PCB.
- ESD Keepout Area: Consider the area around the network connection traces and components as "ESD Hot". The PCB layout should be designed so that substantial ESD hits from the network discharge directly to the star-ground center point.
- Clamp Diodes: Four diodes clamp the TPT/XF-1250 transceiver's differential receive signals to ground during ESD and surge transients, as shown in Figure 1 on page 3.
- Ground Return for a Neuron 5000 Processor: A Neuron 5000 Processor has internal protection circuitry built into its CP[4..0] pins. When an ESD or surge transient comes in from the network, the portion of the transient that makes it to the Neuron 5000 Processor is clamped to the chip's V_{DD33} power pins and ground

pins. Be sure to provide a short and wide ground path from the Neuron 5000 Processor back to the center of the star ground.

- Ground Planes: As ground is routed from the center of the star out to the function blocks on the board; planes or very wide traces should be used to lower the inductance (and therefore the impedance) of the ground distribution system.
- V_{DD33} Decoupling Capacitors: A good rule of thumb is to provide at least one V_{DD33} decoupling capacitor to ground for each V_{DD33} power pin on an IC in the design. For SMT devices like a Neuron 5000 Processor, each decoupling capacitor should be placed on the top layer with the chip, and placed as close as possible to the chip to minimize the length of V_{DD33} trace between the capacitor and the chip's V_{DD33} pad.
- Host Microprocessor Kept Away From Network Connection: The (optional) host microprocessor (for a ShortStack device) is a potential source of digital noise that could cause radiated EMI problems if that noise is allowed to couple onto the external network, power, or I/O wiring. To help prevent this coupling, the host microprocessor and any other noisy digital circuitry should be kept away from the network side of the Neuron 5000 Processor.

Figure 4 on page 8 shows a portion of the top layer of a 4-layer PCB layout for the Neuron 5000 Processor, the differential driver circuit, and the comparator circuit, along with the other building blocks of a PCB design. The figure shows a rectangle for the placement of the TPT/XF-1250 transceiver PCB, which is mounted above the main board.

See Chapters 3 and 4 of the *Series 5000 Chip Data Book* (005-0199-01B) for additional information about PCB layout and electromagnetic compatibility (EMC) design guidelines for a Series 5000 Chip.

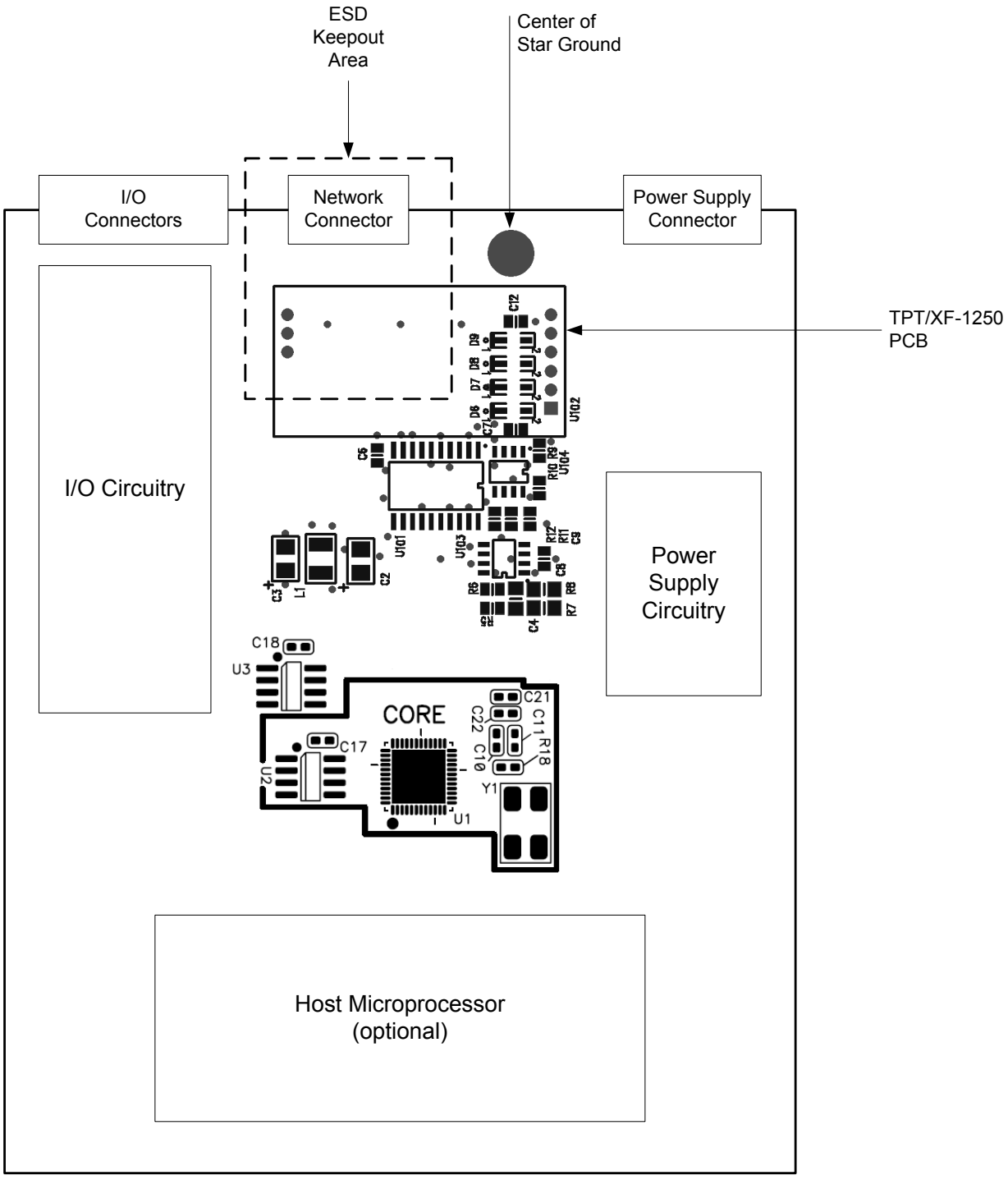

Figure 4. Example PCB Layout for a Neuron 5000 Processor with a TPT/XF-1250 Transceiver

In the figure, the area marked CORE represents the essential circuitry for the Neuron 5000 Processor, its serial EEPROM memory chip, its crystal, and associated capacitors and resistors. Outside the CORE area is the Neuron 5000 Processor's optional serial flash memory chip.

The differential driver circuit is shown as U101 and associated parts. The comparator circuit is shown as U103, U104, and associated parts. The TPT/XF-1250 transceiver is shown as U102, although the transceiver itself resides on a separate sub-assembly PCB, above the main board and is connected to it by two headers (one 6-pin header and one 3-pin header). Below the TPT/XF-1250 transceiver PCB are the clamping diodes (D6-D9) for the transceiver's receive signals.

Related Documentation

- *Series 5000 Chip Data Book* (005-0199-01B) for information about the Neuron 5000 Processor.
- *LonWorks TPT Twisted Pair Transceiver Module User's Guide* (078-0025-01C) for information about the TPT/XF-1250 Transceiver.
- *Junction Box and Wiring Guidelines for Twisted Pair LonWorks Networks* (005-0023-01M) for information about the different types of junction boxes and interconnections that can be used in twisted pair LONWORKS networks in building and industrial control applications.

EIA-485 Transceivers

You can use the Neuron 5000 Processor with commercially available EIA-485 transceivers. A number of wire types can be supported, along with multiple data rates (up to 1.25 Mbps), as listed in Table 4.

Table 4. Neuron 5000 Sysclock Settings for Specified Data Rates

	Neuron 5000 Sysclock Frequency				
Data Rate	**5 MHz**	**10 MHz**	**20 MHz**	**40 MHz**	**80 MHz**
625 kbps (and lower)	Supported	Supported	Supported	Supported	Supported
1.25 Mbps	*Not Supported*	*Not Supported*	Supported	Supported	Supported

With an EIA-485 transceiver, the common-mode network voltage can range between –7 V to +12 V. To implement an EIA-485 device, the Neuron 5000 Processor's communications port runs in single-ended mode.

Available industry standards that describe EIA-485 specifications provide details on unit loads, data rate, wire size, and wire distances. To ensure interoperability between devices, the LONMARK® interoperability guidelines require a data rate of 39 kbps for devices that use EIA-485 transceivers. In addition, the EIA-485 transceiver must have TTL-compatible inputs for the connection to the 3.3 V Neuron 5000 Processor. A typical circuit configuration, shown in **Figure 5**, can support up to 32 loads.

An EIA-485 network works best with a common power source. Individual device power sources can create problems when the network common-mode voltage exceeds –7 V to + 12 V, or when ground faults cause damage to devices.

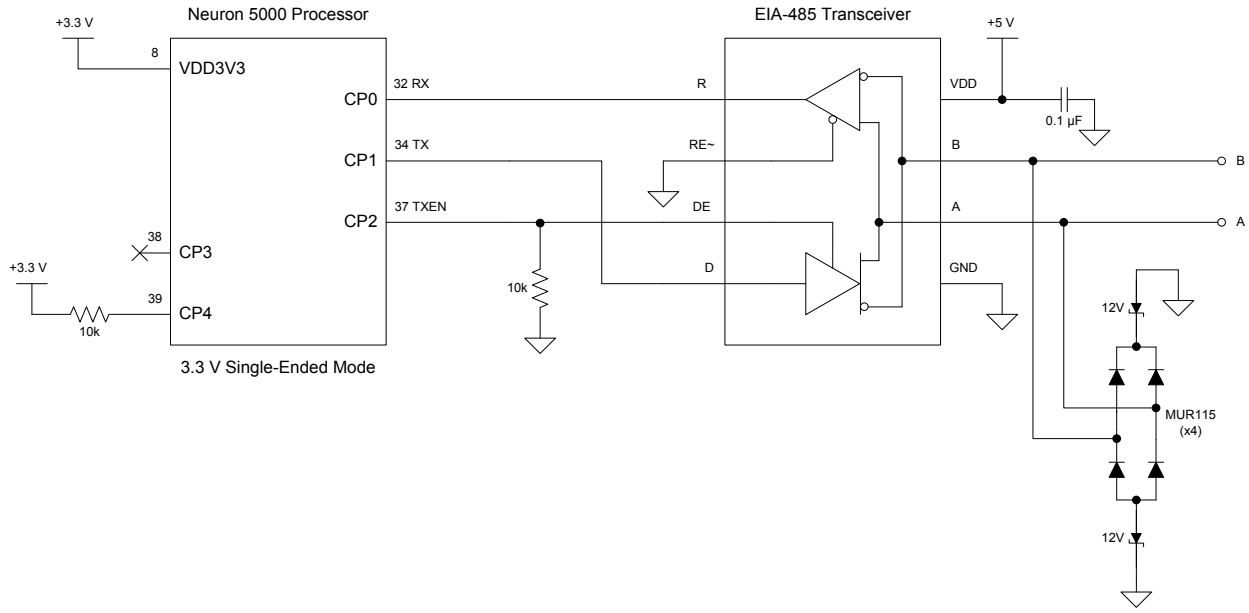

Figure 5. EIA-485 Twisted-Pair Interface (Uses Single-Ended Mode)

The EIA-485 specification requires a common ground reference for all transceivers. This common ground reference can be provided by adding a third conductor in the network cable or a separate connection to common ground at each device.

LPT-11 Link Power Transceivers

The Echelon LONWORKS LPT-11 Link Power Twisted Pair Transceiver provides a simple, cost effective method for adding a network-powered LONWORKS transceiver to any Neuron Chip-based sensor, activator, display, lighting device, or general purpose

I/O controller. The LPT-11 transceiver consists of a Single In-Line Package (SIP) that contains a 78 kbps differential Manchester coded communications transceiver, a switching power supply that draws power from the twisted-pair network, and connections for the Neuron Chip Communications Port (CP) lines and for the twisted pair network. The LPT-11 transceiver eliminates the need to use a local power supply for each device, because device power is supplied by a central power supply over the same twisted wire pair that handles network communications. A single network segment can support up to 128 LPT-11 based devices.

The LPT-11 transceiver includes an integral switching power supply that can furnish +5 VDC at up to 100 mA. The LPT-11 transceiver derives its power directly from the switching power supply, leaving up to 100 mA of current for a Neuron 5000 Processor, application electronics, sensors, actuators, and displays. If a high-current or high-voltage device must be controlled, then the +5 VDC power can be used to trigger an isolating high-current triac, relay, or contactor.

The link-power system uses a single point of Earth ground, at the LPI-10 module, and all of the LPT-11 transceivers electrically float relative to the local ground. Differential transmission minimizes the effects of common-mode noise on signal transmission. If grounded sensors or actuators are used, then either the communication port (CP) or the I/O lines of the Neuron 5000 Processor must be electrically isolated.

The LPT-11 transceiver receives its clock input from the Neuron 5000 Processor through its CMOS input CLK pin. This pin is driven by the XOUT output of the Neuron 5000 Processor, buffered with a standard bus buffer/line driver that supports TTL-compatible input and 5V CMOS output. Clock traces should be kept short (≤2 cm) to minimize noise coupling. In addition, a logic ground guard must be added for the CLK trace to minimize clock noise and to help keep EMI levels low. However, this ground guard should not be used as a ground source for digital circuitry.

The LPT-11 transceiver can operate at 20, 10, or 5 MHz. When coupled to a Neuron 5000 Processor, the LPT-11 transceiver operates at 10 MHz. The operating frequency is automatically detected on the LPT-11 transceiver's CLK pin.

Figure 6 on page 12 shows the basic configuration for connecting a Neuron 5000 Processor to an LPT-11 Twisted-Pair Link Power Transceiver.

The major differences between connecting a Series 3100 Neuron Chip to an LPT-11 transceiver (see the *LONWORKS LPT-11 Link Power Transceiver User's Guide*) and connecting a Neuron 5000 Processor to an LPT-11 transceiver are:

- The connection between the LPT-11 VCC pin and the Neuron 5000 VDD3V3 pin requires the addition of a low drop-out linear regulator to convert the +5 V output from the LPT-11 transceiver to the +3.3 V input for the Neuron 5000 Processor.

- The connection between the LPT-11 TXD pin and the Neuron 5000 CP1 pin requires the addition of a non-inverting bus buffer/line driver that supports TTL-compatible input and 5V CMOS output. The output of the Neuron RST~ pin is also connected to the buffer/line driver to allow the Neuron 5000 Processor to propagate a device reset to the LPT-11 transceiver by setting the buffer/line driver to a tri-state impedance state. An example part for the buffer/line driver is an NXP® 74AHCT1G126 bus buffer/line driver.
- The connection between the LPT-11 CLK pin and the Neuron 5000 XOUT pin requires the addition of a standard (inverting or non-inverting) bus buffer/line driver that supports TTL-compatible input and 5V CMOS output.

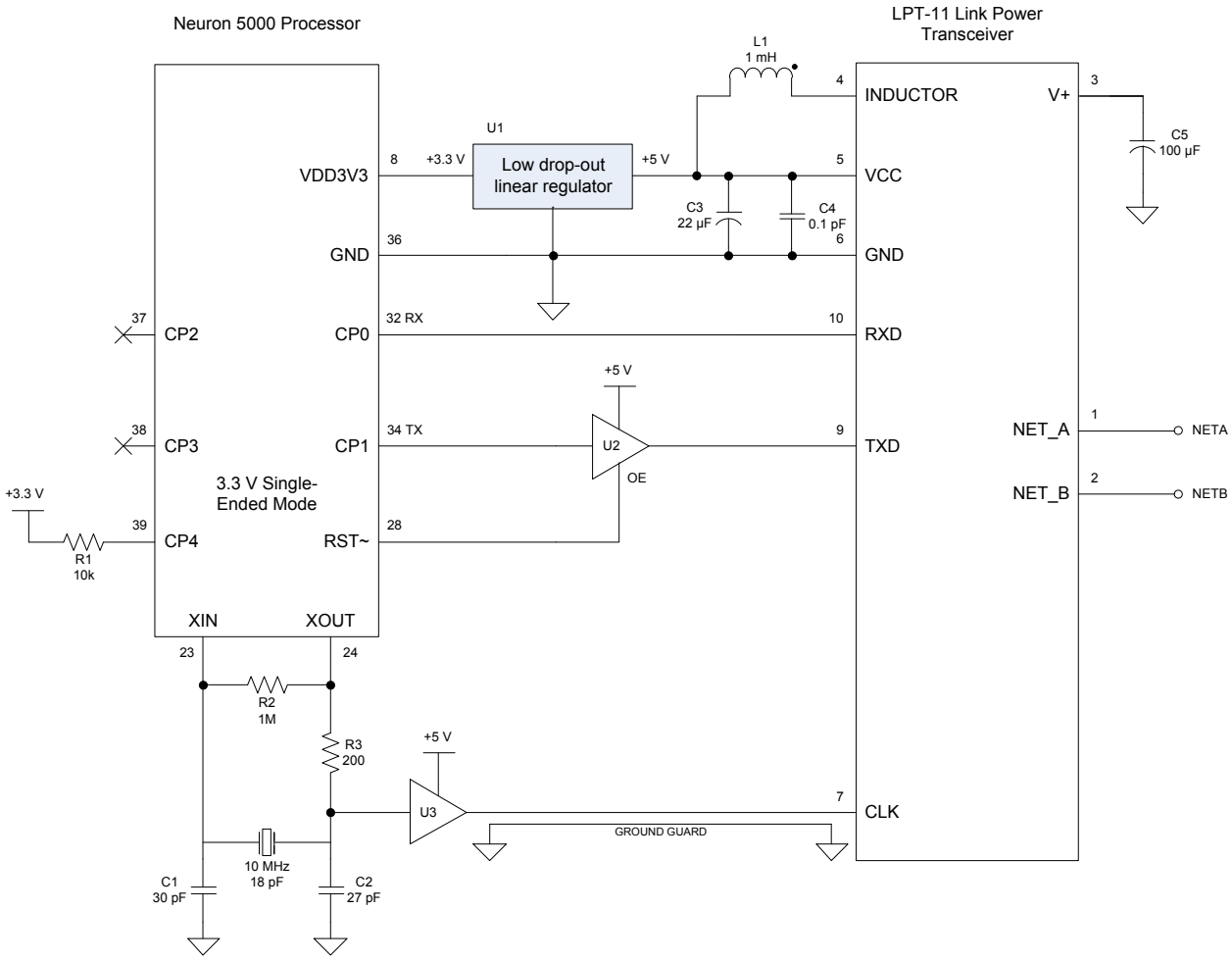

Figure 6. Connecting a Neuron 5000 Processor to an LPT-11 Link Power Transceiver

Table 5. Example Bill of Materials for the LPT-11 Circuit

Designator	Value
C1	30 pF
C2	27 pF
C3	22 µF, DCWV ≥10 V, I_{ripple} ≥200 mA_{rms} @ 100 kHz, ESR ≤1.2 Ω
C4	0.1 µF
C5	100 µF, DCWV ≥63 V, I_{ripple} ≥100 mA_{rms} @ 100 kHz
L1	1 mH, DCR ≤4 Ω, I_{sat} ≥200 mA, F_{res} ≥800 kHz
R1	10 kΩ
R2	1 MΩ
R3	200 Ω
R4	10 kΩ
U1	TDA3663 (or similar LDO regulator)
U2	74AHCT1G126
U3	74AHCT1G04 (or a 74AHCT1G126 with OE tied high)

Important: Because the Neuron 5000 XOUT pin drives the LPT-11 CLK signal, the value of C2 does not match the value of C1. The value for C2 is specified as 27 pF based on an input capacitance for the buffer/line driver of 3 pF at 25 ºC (so that the total capacitance for the XOUT pin is 30 pF). For the 74AHCT1G126 part, input capacitance can vary over temperature, up to 10 pF. If your device is likely to experience extreme temperatures, consider changing the value of C2 to 22 pF to allow for the change in capacitance over temperature.

See the *LONWORKS LPT-11 Link Power Transceiver User's Guide* for additional information about selecting appropriate parts for capacitors C3 and C5 and for inductor L1.

See the *LONWORKS LPT-11 Link Power Transceiver User's Guide* for PCB layout guidelines for the LPT-11 transceiver; see *PCB Layout Guidelines* on page 6 and the *Series 5000 Chip Data Book* for PCB layout guidelines for the Neuron 5000 Processor.

Related Documentation

- *Series 5000 Chip Data Book* (005-0199-01B) for information about the Neuron 5000 Processor.
- *LONWORKS® LPT-11 Link Power Transceiver User's Guide* (078-0198-01A) for information about the LPT-11 Link Power Transceiver.

Conclusion

You can use a Neuron 5000 Processor with an external transceiver for a TP/XF-1250 channel, an EIA-485 network, or a link-power network. In all cases, the Neuron 5000 Processor's communications port operates in 3.3 V single-ended mode. For a TP/XF-1250 channel, you also add a differential driver and comparator circuit. For an EIA-485 network, you connect the Neuron 5000 Processor to an EIA-485 transceiver. For a link-power network, you connect the Neuron 5000 Processor to an LPT-11 Twisted-Pair Link Power Transceiver.

Table 6. Document Revision History

Revision	Description
005-0202-01A	Initial release.
005-0202-01B	Added information about connecting to a LONWORKS LPT-11 Twisted Pair Link Power Transceiver.
005-0202-01C	Clarified Neuron 5000 sysclock requirement for TP/XF-1250 channels and EIA-485 transceivers.
005-0202-01D	Corrected TX connection to LPT-11 transceiver in figure 6.

Part Number 005-0202-01D

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