DA1458x
Known Limitations

Family:	DA1458x
Date:	19-Jan-18

Item Nr	Date	Applicable devices	Description	Solution/workaround
75	13-Apr-13	DA14580 DA14581 DA14582 DA14583 DA14585 DA14586	Due to a mismatch between PA and 50Ohm antenna there is a decrease in Tx power of about 0.7dB.	**Fix:** Will not be fixed. Specification is changed **SW Workaround:** N/A **HW Workaround:** The output power can be increased by ~0.7dB when matching is optimised. For a 50Ohm antenna this works best with a 3.3nH shunt inductor to ground for the WLCSP-34 package and a 3.9nH for the QFN40 and QFN48 packages.
95	28-Aug-13	DA14580 DA14581 DA14582 DA14583 DA14585 DA14586	An increased Packet Error rate might occur if GPIO P1-2 and P1-3 is toggling. The root cause of this problem is the close location of a few GPIO pins to the on-chip 16MHz XTAL oscillator circuitry. Toggling of these GPIOs might corrupt the clock, which will be visible in the Packet Error Rate. The following pins are affected by this: P1-2, P1-3.	**Fix:**Will not be fixed **SW Workaround:** N/A **HW Workaround:** Carefull PCB design. These pins should only be used for waking up the device and not while the XTAL 16MHz is running. An application note explaining how to design the PCB is available on the Dialog support website.
101	19-Nov-13	DA14580 DA14581 DA14582 DA14583 DA14585 DA14586	The ADC pins are multiplexed with P0_0, P0_1, P0_2 and P0_3. The voltage on any of these pins cannot be higher than VBAT3V, otherwise the ADC will not work correctly, even if the ADC is measuring an internal voltage. Since these pins can also be used as UART or SPI or I2C pins, there is a risk that this will happen in an application. Be aware that this is not allowed.	
104	5-Feb-14	DA14580 DA14581 DA14582 DA14583 DA14585 DA14586	The ADC consists of some blocks which have to be enabled with enough wait-time in between. To make this easier for the customer, there is a hardware function implemented to guarantee these wait-times. This is enabled with the bit GP_ADC_CTRL2_REG[GP_ADC_DELAY_EN]. Unfortunately, this function only works once (GP_ADC_DELAY_EN needs to set to '0' to reset the internal counter that defines the waiting). The correct procedure is: Function Read_from_ADC make GP_ADC_CTRL2_REG[GP_ADC_DELAY_EN]='0' (to be sure counters are reset) make GP_ADC_CTRL2_REG[GP_ADC_DELAY_EN]='1' do the conversion by setting GP_ADC_CTRL_REG (as long as ADC_LDO is not disabled, it is safe to perform any ADC conversion	
	1-Dec-14	DA14580 DA14581 DA14585	The RCX can not be used as low power clock in Boost mode. Due to supply switching when waking up from sleep the RCX frequency will have an unpredictable error. This will impact the time of the next wake-up and as a consequence the Bluetooth link will be dropped. *(This is not applicable to DA14582, DA14583, DA14586 because these devices can only operate in Buck mode)*	**Fix:** Will not be fixed. **SW Workaround:** N/A **HW Workaround:** Applications running in Boost mode and using sleep must run on 32kHz in stead of the RCX. The Buck mode is not suffering from this limitation
	1-Dec-14	DA14580 DA14581 DA14582 DA14583 DA14585 DA14586	The DA1458x devices can go into a locked state caused by a bouncing supply voltage. An external pulse on the Reset pin or a power cycle is required to get out of this mode. To prevent the locked state to happen it is adviced to use a battery holder with strong spring contacts or for coin cell batteries to use a holder with a minimum of 2 spring contacts	**Fix:** Will not be fixed. **SW Workaround:** N/A **HW Workaround:** • In Buck mode add a 1uF capacitor between VBAT3V and RESET. • In Boost mode ad a 1uF capacitor between VBAT1V and RESET. • Use an external reset circuitry: http://www.silego.com/applications/reset-ic.html
	1-Dec-14	DA14580 DA14581 DA14582 DA14583 DA14585 DA14586	A clarification to the datasheet: GPIO's that are configured for I2C (SDA or SCL) will automatically be configured as open drain with an internal 25kΩ pull-up resistor connected to VBAT3V (Buck mode) or VBAT1V (Boost mode)	**Fix:** Will not be fixed. **SW Workaround:** N/A **HW Workaround:** N/A
	1-Dec-14	DA14580 DA14581 DA14582 DA14583 DA14585 DA14586	The input of the ADC is multiplexed on 4 different GPIO's. For input voltages higher than the Full Scale voltage (1.2V) an on-chip 1:3 resistive scaler is available. In combination with the ESD resistor in the IO pad this scaler gives a small measurement error: @Vin = 3.0V P0_0 and P0_3 will measure ~20mV lower P0_1 and P0_2 will measure ~25mV lower The following workaround is suggested: Measurements of voltages above 1.2V that require high accuracy should use an external resistive scaler. This will eliminate the measurement error. Measurements on the VBAT3V can be performed using the internal connection between VBAT3 and the ADC. This will also eliminate the measurement error.	**Fix:** Will not be fixed. **SW Workaround:** N/A **HW Workaround:** use and external 1:3 scaler or perform VBAT3V measurement on the internal VBAT connection.