Application note

DA9212 PCB Layout recommendation

AN-PM-045

Abstract

This application note provides recommendations how to place and route the DA9212 device as well as the passive components needed for proper functioning of the device. Application developers should treat this document as a guideline, not as a hard requirement, since the target applications may have different requirements

Contents

Figures

1 Terms and definitions

PCB	Printed Circuit Board
TH	Through-Hole
Cap	Capacitors

2 References

1. DA9211(2), Data sheet, Dialog Semiconductor

3 Introduction

DA9212 integrates two dual-phase buck converters each capable of delivering up to 6 A output current.

The output voltage is configurable in the range 0.3 - 1.57 V. The input voltage range of 2.8 – 5.5 V makes DA9212 suited for a wide variety of low voltage systems, including all Li-Ion battery supplied applications. The basic recommended components and connections are shown in Figure 1, 2 and 3.

The following chapters deal with layout recommendations related to these schematics.

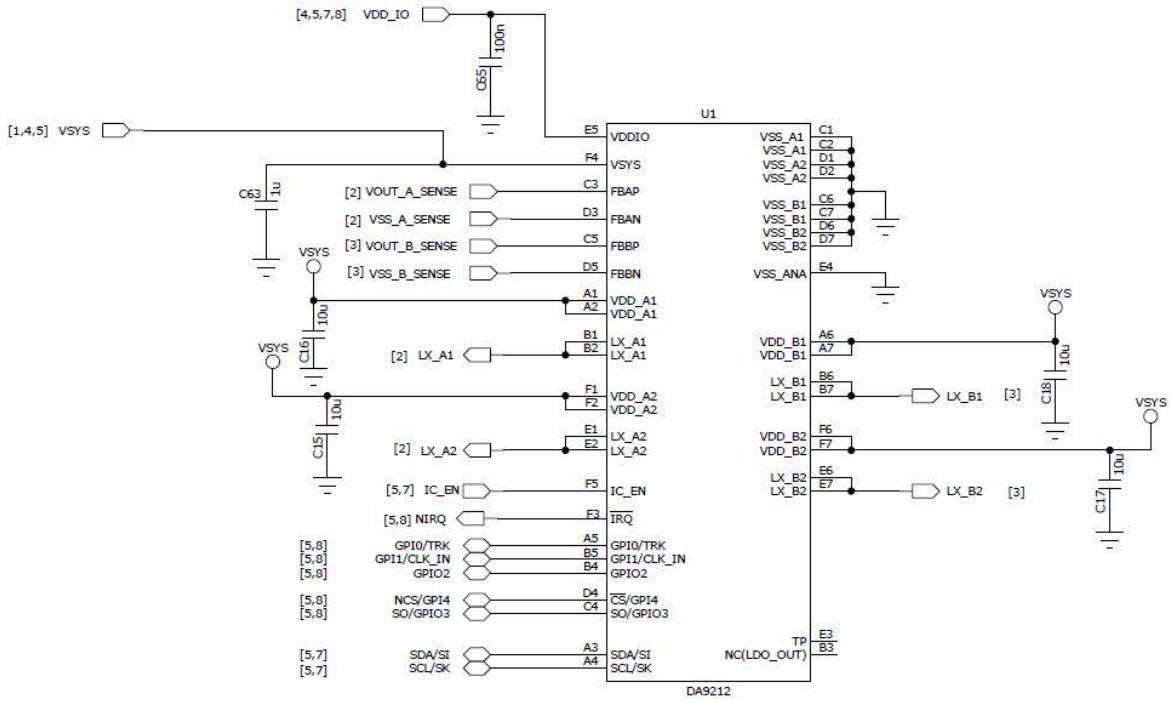


Figure 1: Schematic Drawing DA9212

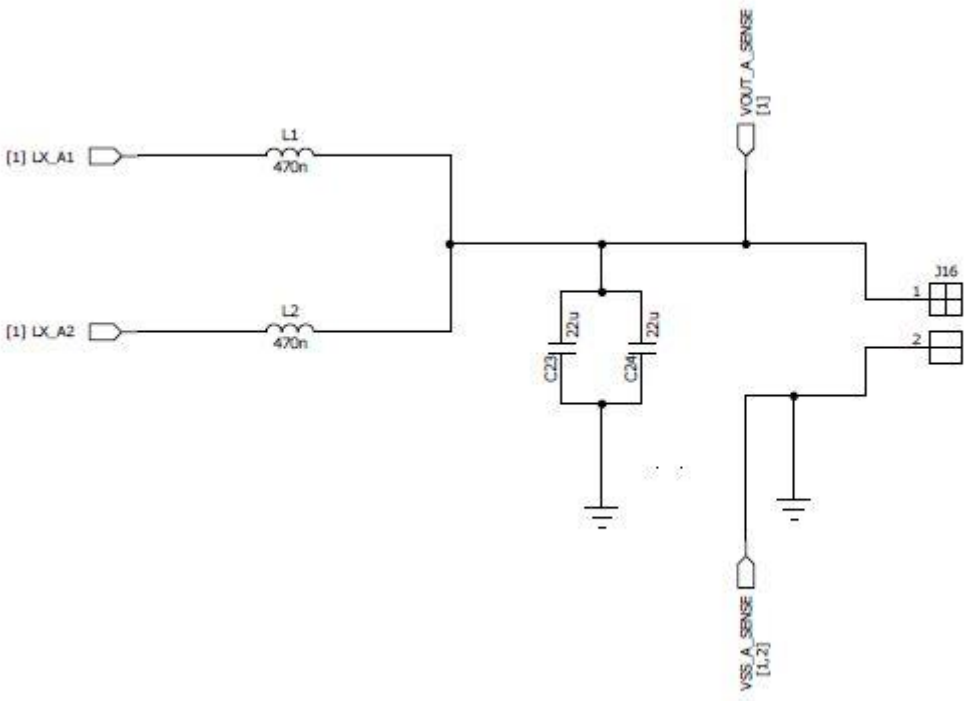


Figure 2: Schematic Drawing Buck_A

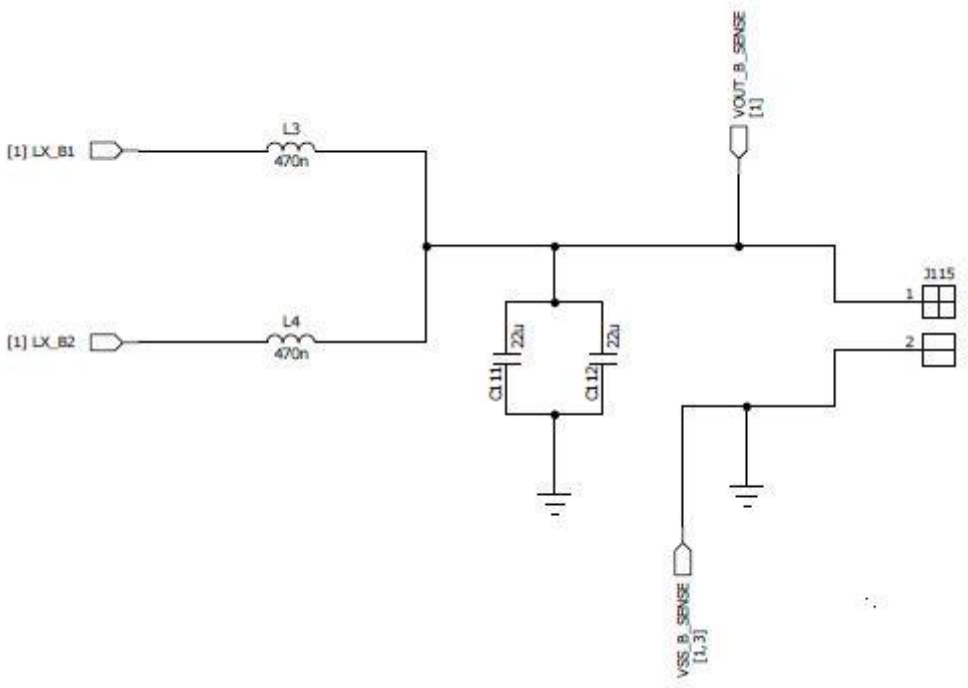


Figure 3: Schematic Drawing Buck_B

4 Layout Recommendations

The DA9212 is a 42 pin WL-CSP device with 0.4 mm pitch.

The PCB layout can be properly done with a 6 layers or a 4 layers PCB stack-up. Dialog evaluation Board is based on a 6 layers PCB stack-up and this is the assumption in the rest of the document., but when the device is part of a complex system with probably “more PCB - demanding” ICs, the number of routing layers and other PCB parameters are determined by the other devices in the system.

For better understanding, this document is organised into sections, the first ones covering the most critical layout aspects to consider:

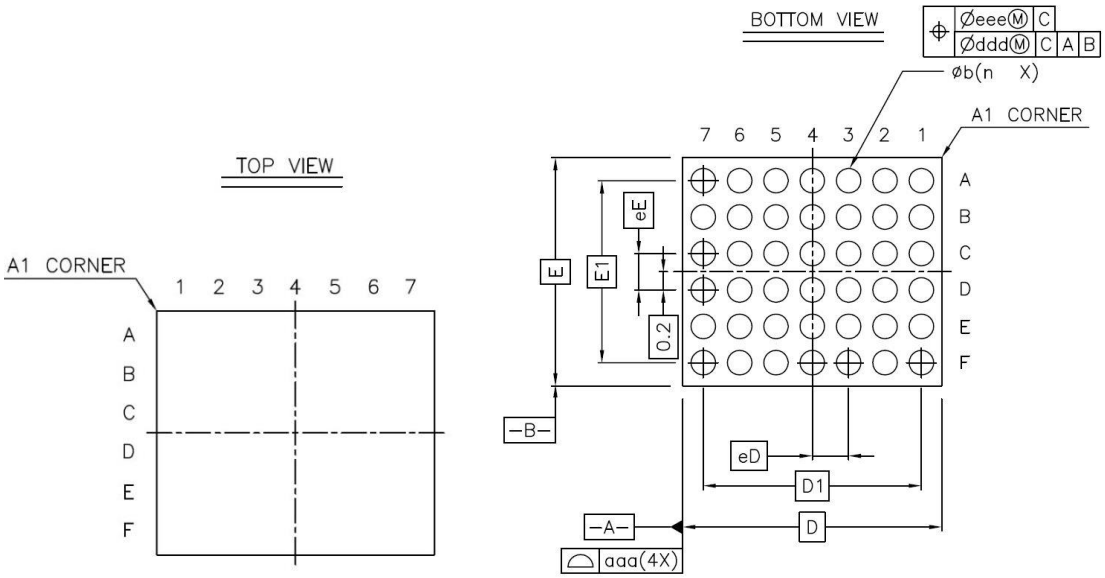
- Package information
- Multiphase buck
- Reference voltage
- Communication interfaces
- GPIOs and control signals

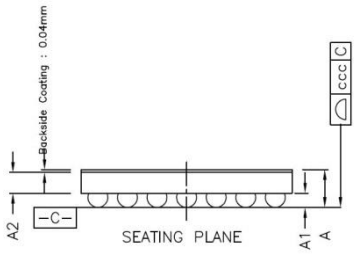
4.1 DA9212 Package information

4.1.1 DA9212 Ball Map

Figure 4: DA9212 Ball Map

4.1.2 Package outline drawing





	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	0.471	0.511	0.551
Stand Off	A1	0.177	–	0.205
Wafer Thickness	A2	0.279 ±0.025		
Body Size	D	2.850 BSC		
	E	2.509 BSC		
Ball Diameter (Size)		0.25		
Ball/Bump Width	b	0.255	0.270	0.285
Ball/Bump Pitch	eD	0.4		
	eE	0.4		
Ball/Bump Count	n	42		
Edge Ball Center to Center	D1	2.4 BSC		
	E1	2.0 BSC		
Package Edge Tolerance	aaa	0.03		
Coplanarity (whole wafer)	ccc	0.03		
Ball/Bump Offset (Package)	ddd	0.05		
Ball/Bump Offset (Ball)	eee	0.015		

Figure 5: DA9212(1) Package Drawing

4.2 Multiphase BUCK

DA9212 supports remote voltage sensing with the output capacitors placed as close as possible to the load/processor. Due to the high currents that the device can deliver, a wide output trace is highly desirable to minimize the parasitic impedance and comply to the specific PCB manufacturing rules (material, copper thickness, etc.).

The differential feedback lines must be taken from the point of load and carefully routed back to DA9212.

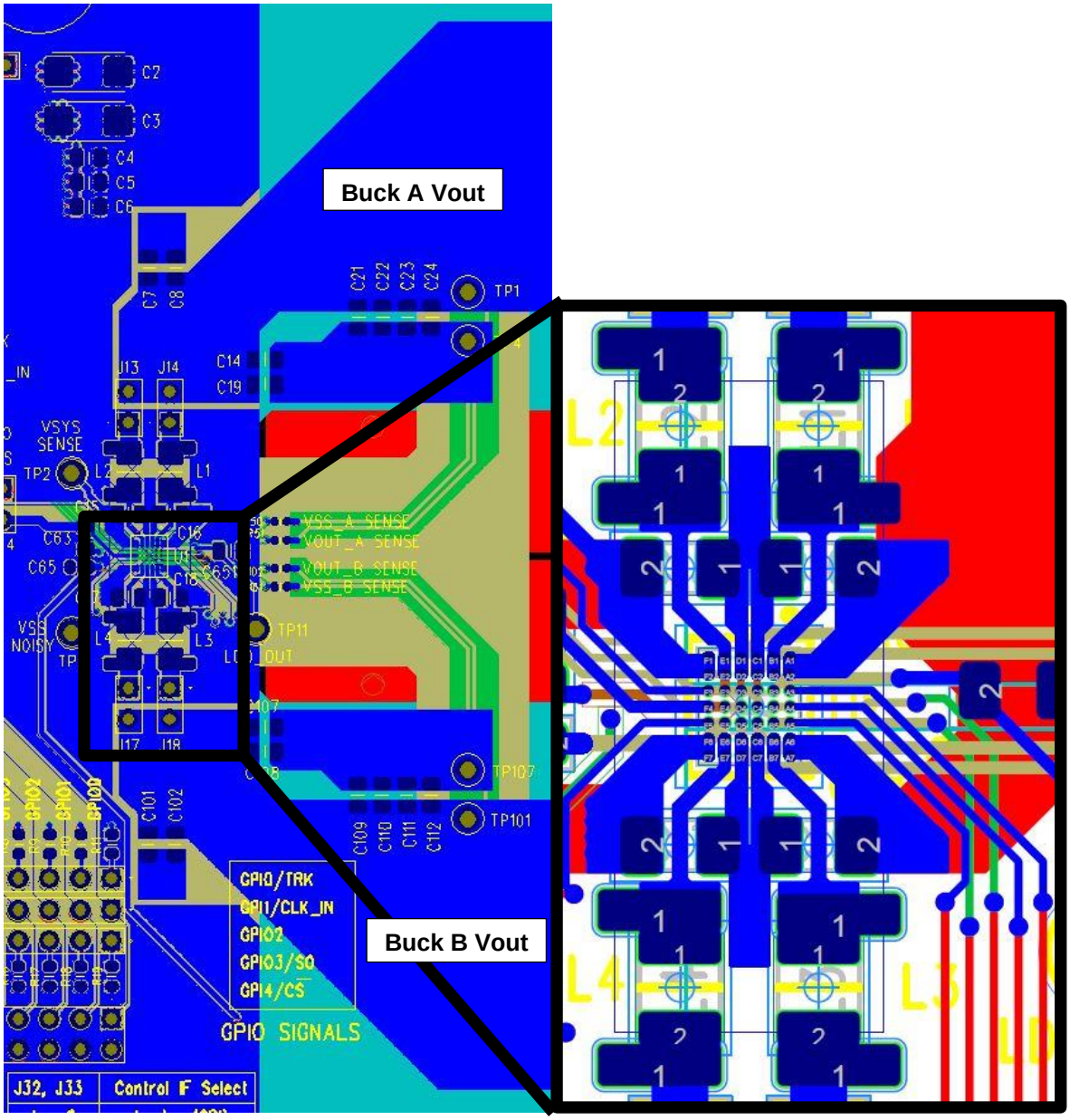


Figure 6: Example of components placement on 6-Layer PCB using µVIAs technics

Figure 6 shows a detail of Dialog Evaluation Board 212-04-C. Note that the jumpers and test points are not necessary in a real application PCB. Those components are aimed only for Dialog internal evaluations.

4.2.1 Device Grounding

Due to the high levels of current supported by DA9212, special care should be taken when planning the ground connection strategy.

The ground connections (VSS_Ax) for Buck_A are placed in the upper side between the coils and the input capacitors, as shown in Figure 7. The ground connection (VSS_Bx) for Buck_B is placed in the bottom side symmetrical to Buck A, as shown in Figure 7. You should keep the ground pattern of Buck_A and Buck_B separated, in order to reduce interference from one channel to the other in case of ground bounce or switching noise. They should be connected together to the main system ground (layer 2 in the PCB we consider now). Note that it is always recommended to use copper plugged via in order to achieve the minimum parasitic via impedance. A ground plane in layer 2 (just below the device) ensures a good stability and noise reduction.

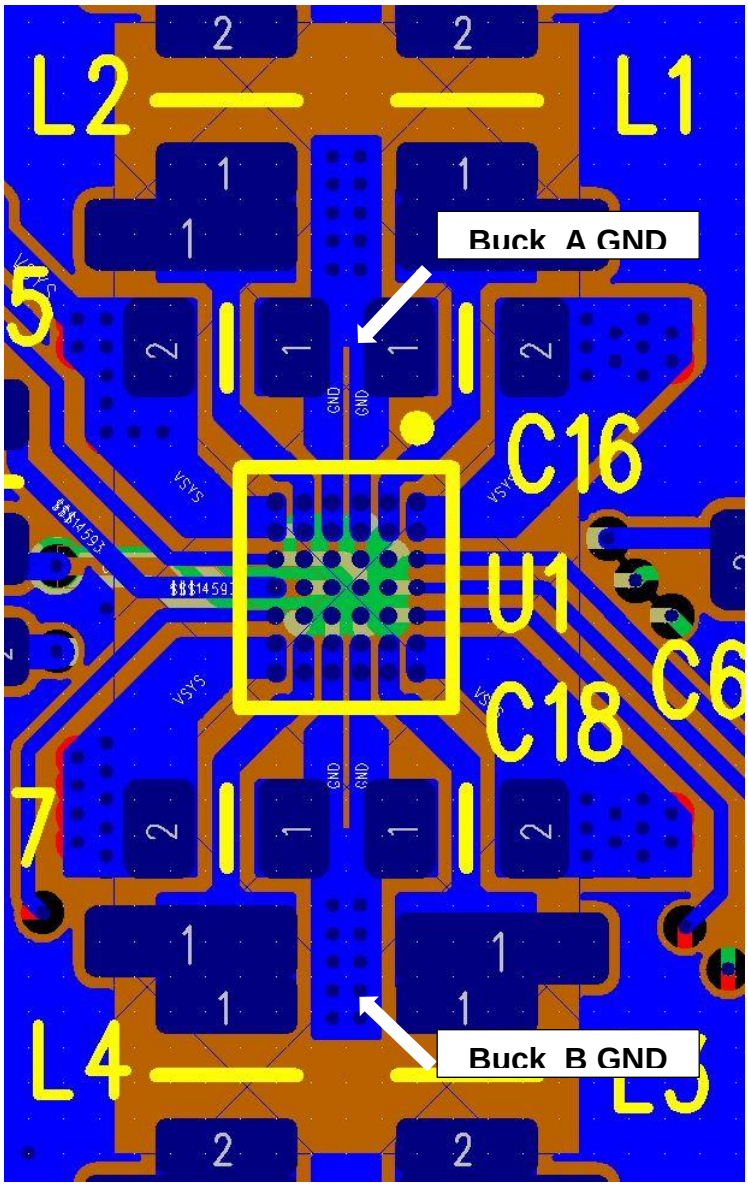


Figure 7: Device ground connection

Additional vias for other signal than ground must be carefully placed around the device, to guarantee that the plane is not degraded by multiple holes and that the copper area is large enough, as is shown on Figure8.

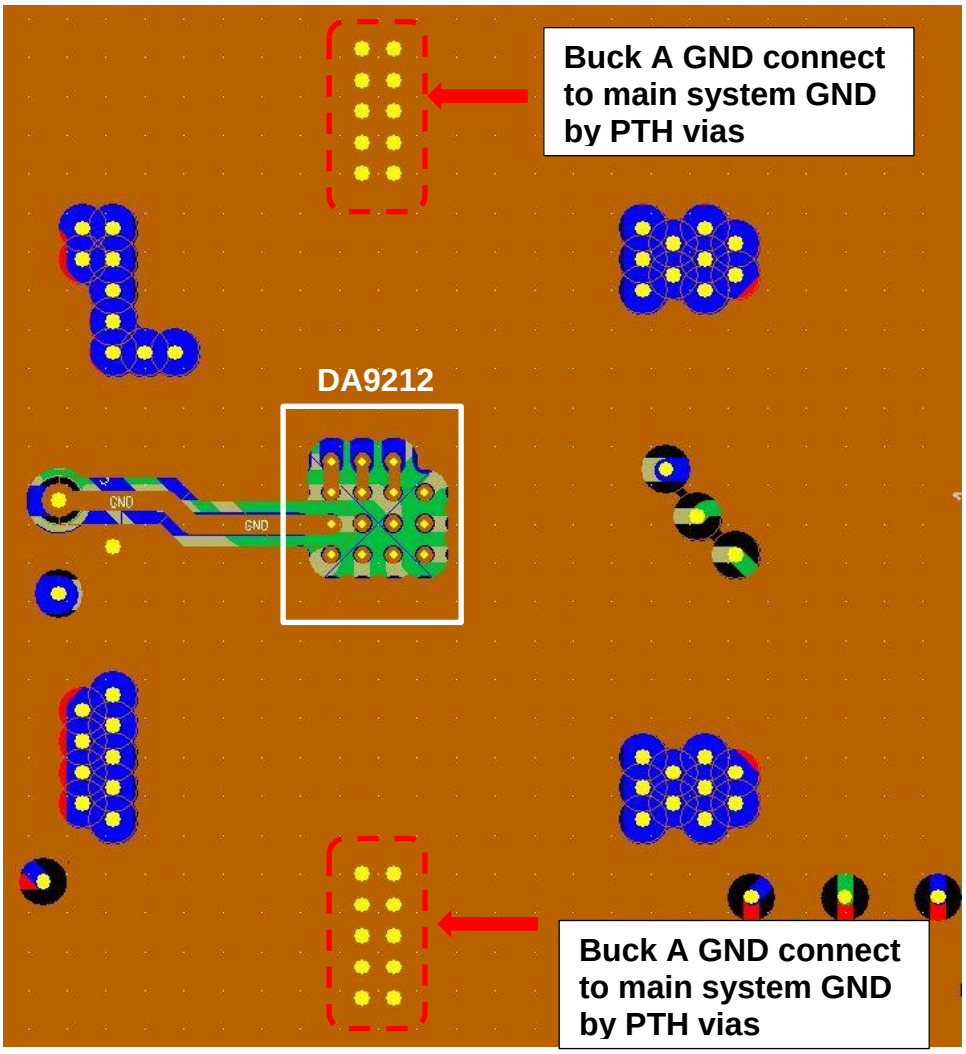


Figure 8: Device ground connection with PTH vias (Internal GND layer)

Return ground patterns of Buck_A and Buck_B should be kept separated, in order to reduce interferences due to ground bounce of each channel.

Dialog Evaluation Board (212-04-C) uses layer 5 for the return ground (see Figure 9).

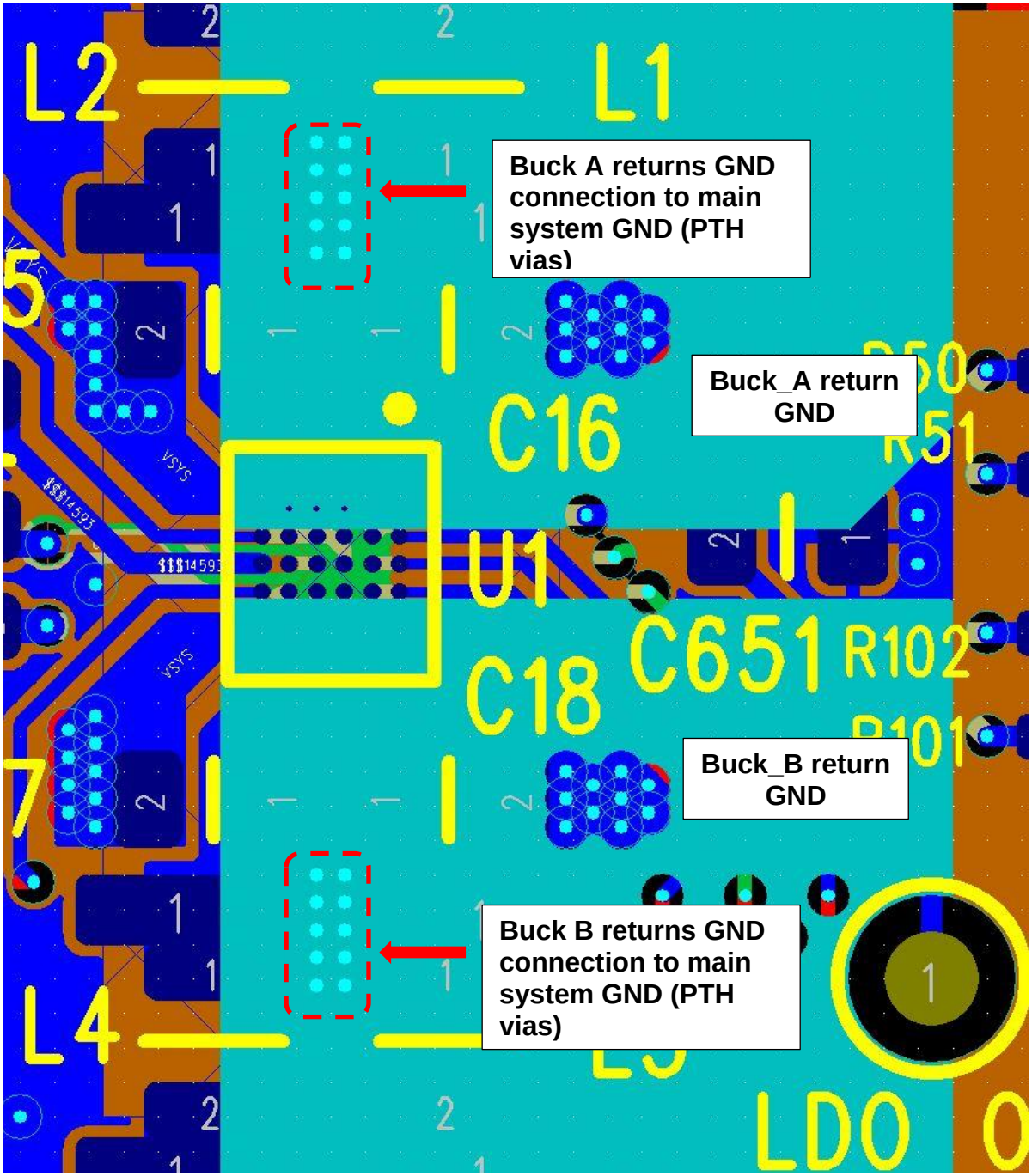


Figure 9: Buck return ground and ground connection with PTH vias

Ground pins of DA9212 are separated into VSS_Ax / VSS_Bx and VSS_ANA pins, where VSS_Ax / VSS_Bx are the ground pins for the noisy power circuits and VSS_ANA is the analogue quiet ground.

Therefore VSS_ANA should be connected to a quiet ground area to achieve the best performance and stability. Figure 10 shows that VSS_ANA is optimally connected to the ground terminal of the VSYS capacitor C63.

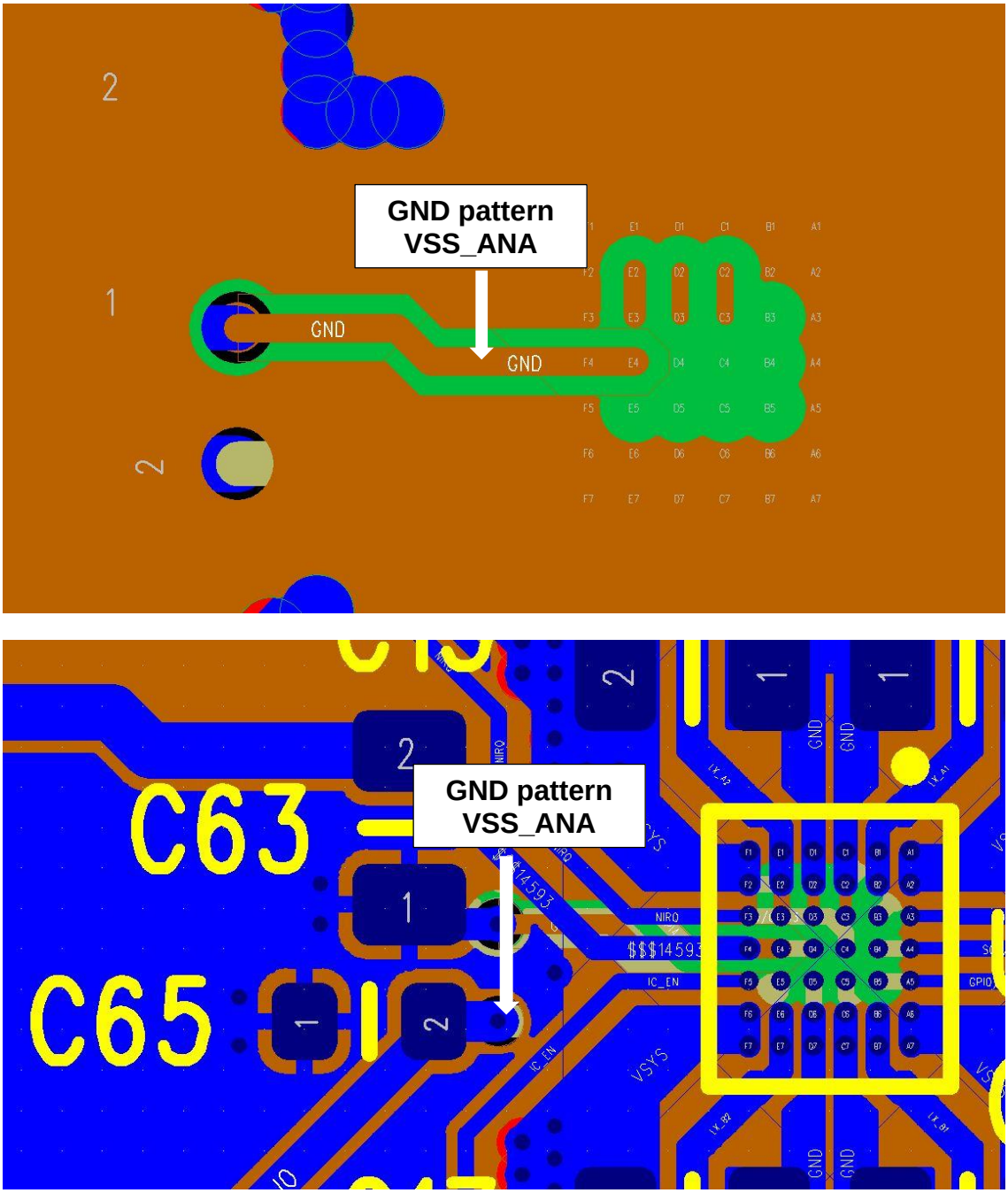


Figure 10: Connection of VSS_ANA

4.2.2 Buck power supply

Similar to what discussed for the ground, special attention is required when connecting the input supply voltage.

Four capacitors are needed, each at the VDD input of the relative phase. We recommend capacitor values of at least 10 µF with the lowest possible DC bias degradation of the capacitance value. In the example of Figure 11 we use 6.3V-rated, 0603 X5R capacitors (C15, C16, C17 and C18).

You should place at least 4 PTH vias for each phase, to connect the positive pin of the input capacitor from the top layer to the VSYS plane (see Figure 11). Similarly, you should place at least 4 PTH vias to connect the ground pin of the input capacitor to the ground plane.

Note that the parasitic impedance between the positive terminal of the input capacitor and DA9212 input pins must be as low as possible, in order to minimize the output ripple and improve the performance. Thus you should place the input capacitor as close as possible to DA9212 and connect with a wide trace, as shown in Figure 11.

The quiet VSYS supply pin (F4) for internal sensitive analogue circuits has a separate capacitor (C63 on Figure 11), with recommended value of 1 µF. In the example below, a component 10V-rated, 0402 X5R has been selected. Please refer to the datasheet for a complete list of suggested external components.

It's recommended to place a decoupling capacitor C65 (100nF, 6.3V, 0402 footprint, X5R) for the VDD_IO input, to suppress noise.

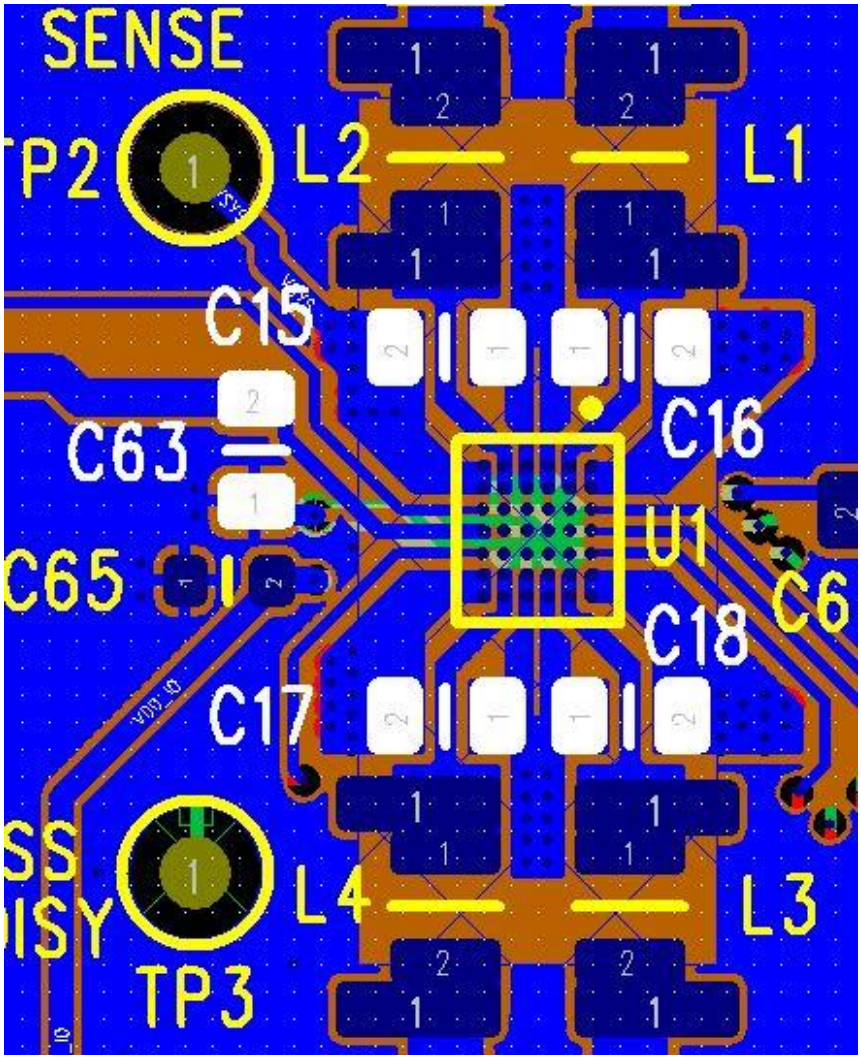


Figure 11: Input capacitors, placement and routing

You should carefully consider the connection of the quiet VSYS to the VSYS plane. This should happen in a quiet area of the plane, see Figure 12.

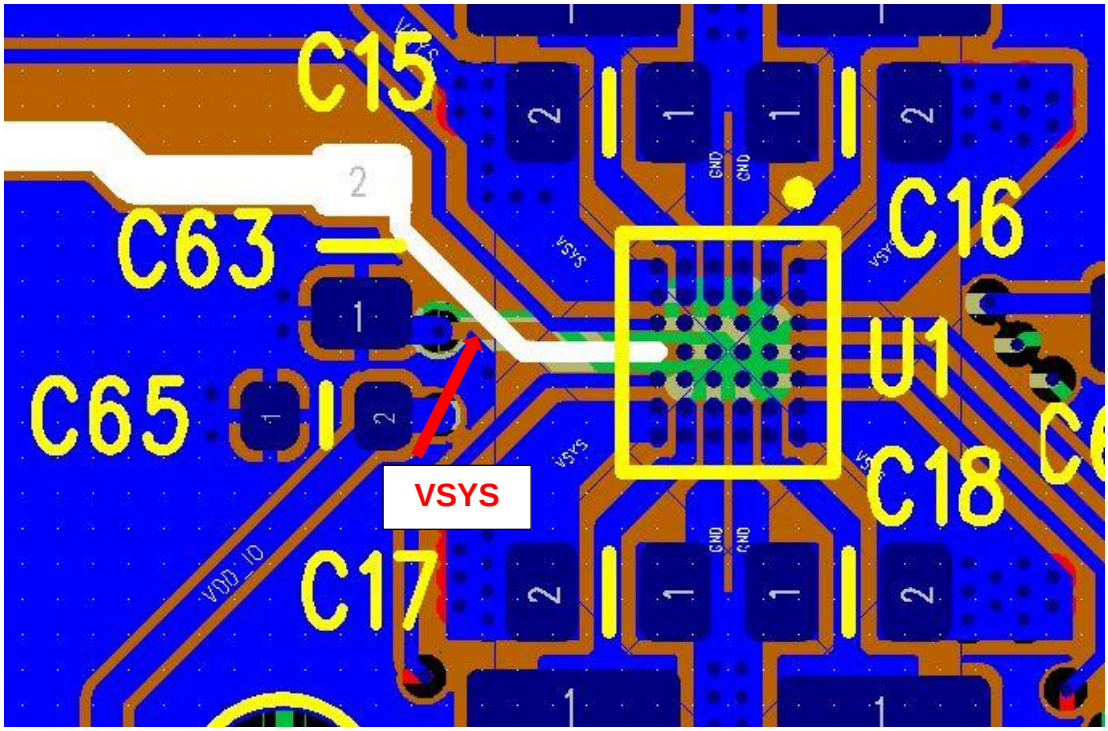


Figure 12: VSYS power supply pattern

4.2.3 Buck output (Vout)

We recommend to users to place the output inductors as in Figure 13. Traces between the LX pins and the inductor terminals should be routed with as the shortest possible distance, in order to reduce emission effects and disturbance to the neighbor circuits. Particular care must be taken in planning a sufficient line thickness that minimizes the parasitic resistance and supports the high current at each phase, up to 4 A. An increased parasitic resistance has bad consequences on the efficiency too.

The example of Figure 12 is taken from Dialog Evaluation Board 212-04-C. The jumpers and the bigger pads around the inductors are unnecessary in a real application board and are used here only for evaluation purposes.

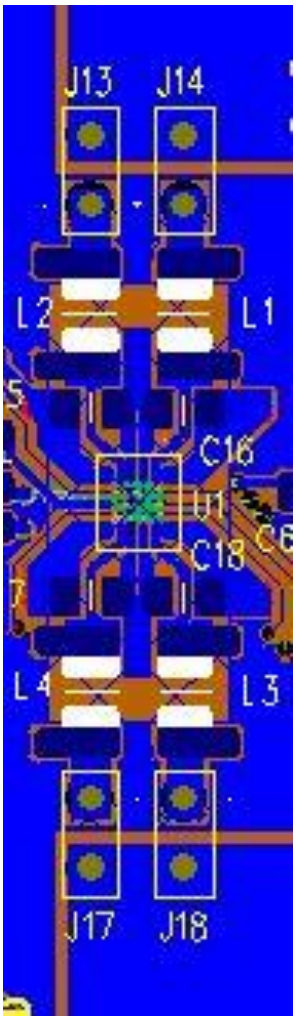


Figure 13: Inductors placement and routing

Select the components according to the list reported in the datasheet. Shielded inductors of 0.47µH and at least 4 A of saturation current are recommended. You should route the power LX lines directly on the top layer, without using any additional vias for changing layer

The output (Vout) track lenght should be minimised for the optimum performance. The example below is taken from Dialog Evaluation Board 212-04-C..

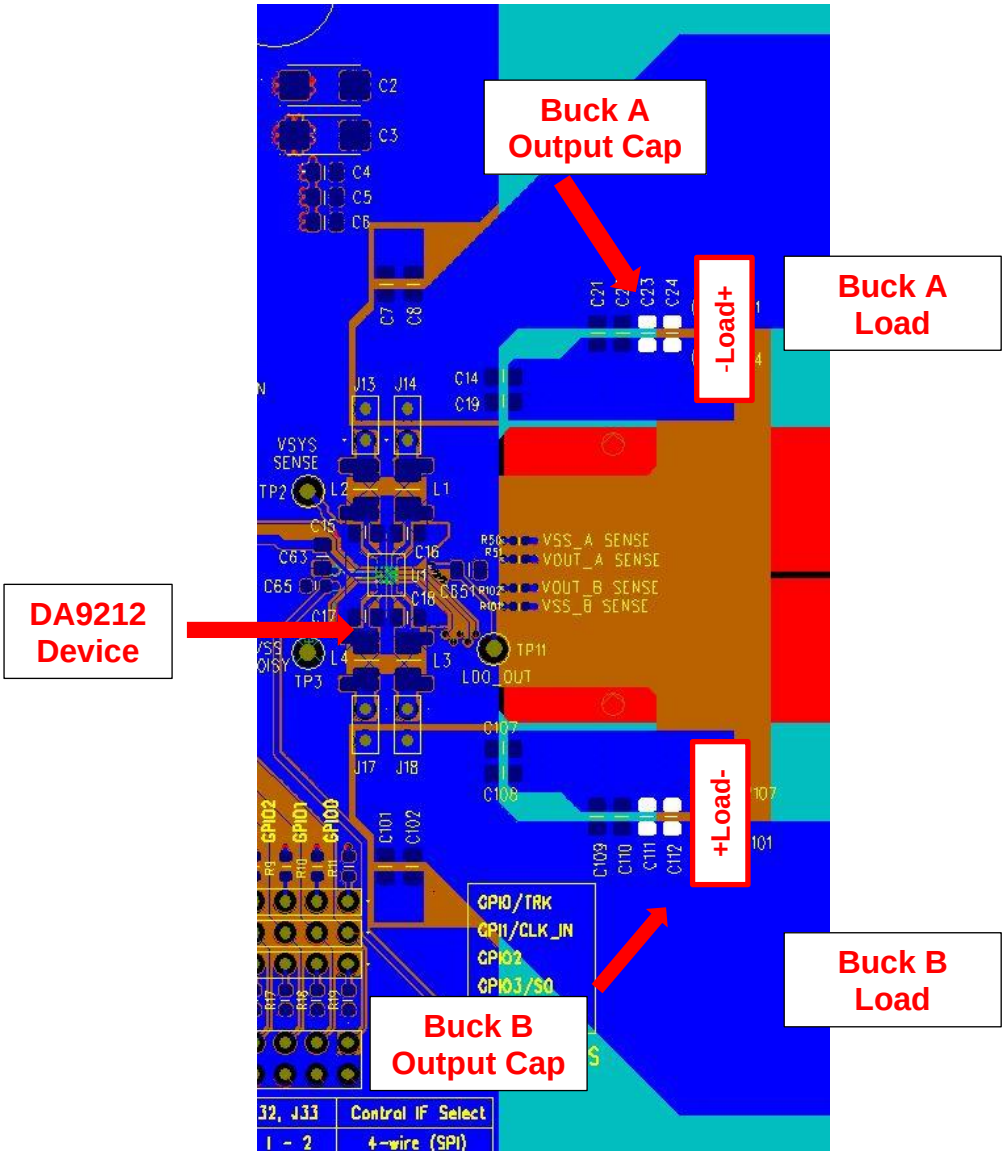


Figure 14: Output capacitors placement

The selection of the specific output capacitance value should be done considering the trade off between PCB footprint and transient response. Although smaller values of 10 µF or 22 µF can be used for each phase, you should place 47µF for each phase if you want to optimize the performance. As suggested in the datasheet, there are 4V-rated, 0603 X5R capacitors available on the market.

4.2.4 Feedback lines

DA9212 has independent feedback lines for each of Buck. FBAP & FBAN are differential sensing lines for Buck A, and FBBP & FABN are differential sensing lines for Buck B.

They are probably the most sensitive traces in the DA9212-related design. Therefore they must be routed far from any noise source (inductors, communication interfaces, etc.). They should never overlap or run in parallel to any noisy traces or areas (e.g. LX traces and VDD traces, etc.). They should be best routed according the differential rules.

Note that the negative feedback is close to the ground potential, but you should not connect it to any part of the ground plane. The feedback lines must be routed directly from the load point in order to achieve the best voltage accuracy and stability at load point. On a 6-layer PCB, the recommended layer is layer 6 (bottom), but in general at least one insulation plane (ground, or power) between the noisy top components and the feedback signals must be present.

The routing of the feedback lines should happen outside of the current loops shown in Figure 15 and away from the buck switching noise sources.

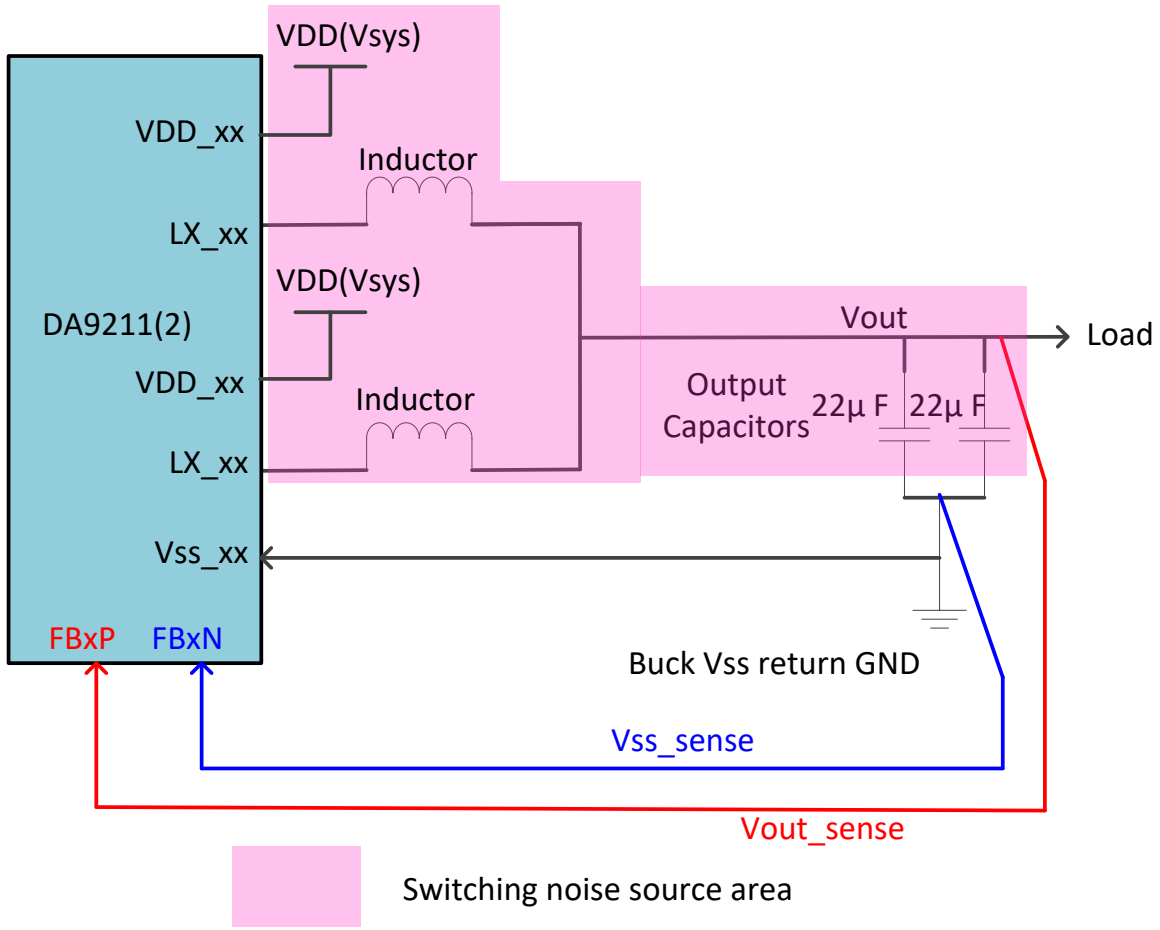


Figure 15: Concept of feedback routing

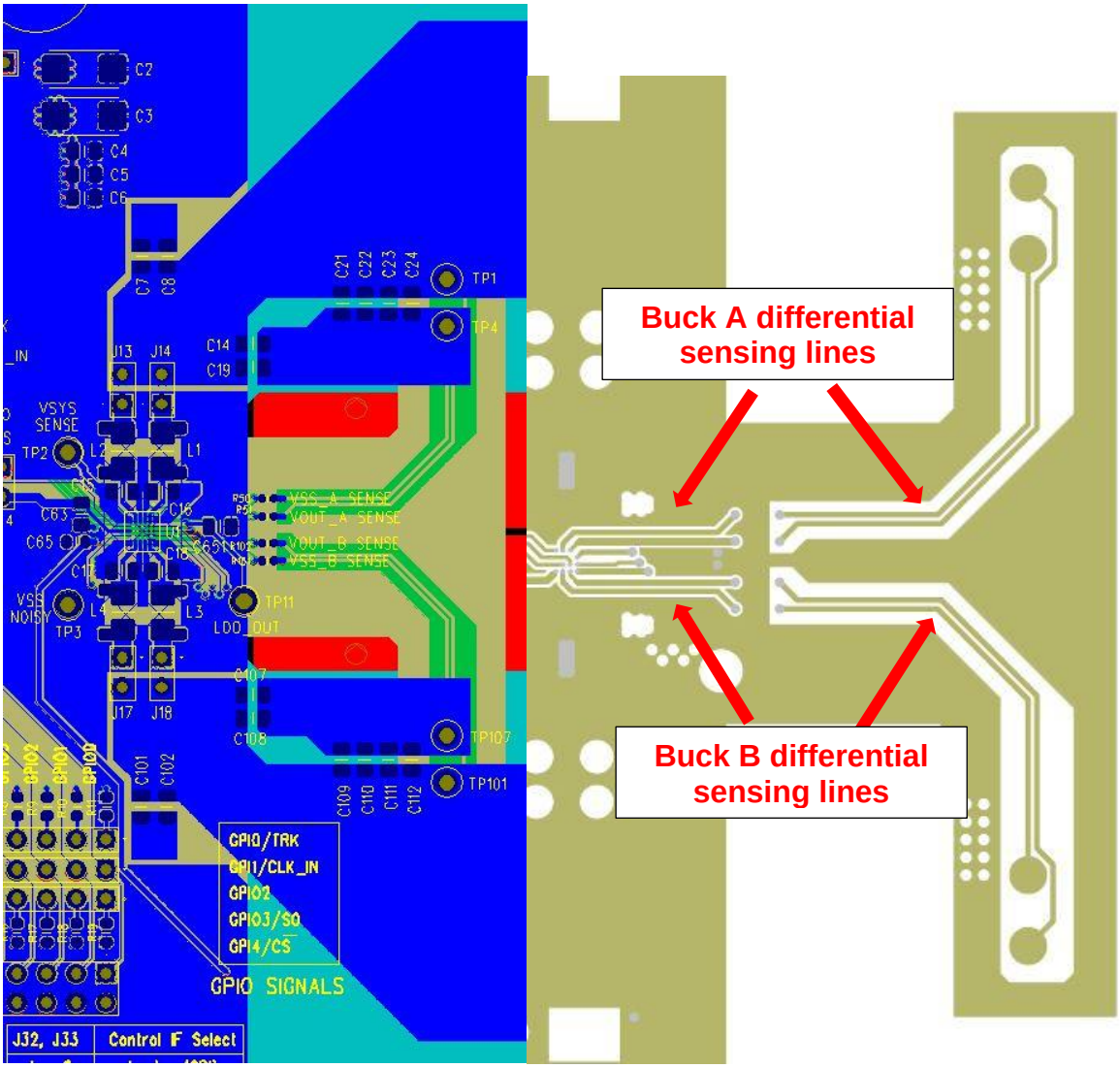


Figure 16: Example of feedback routing

The example above is taken from Dialog Evaluation Board 212-04-C.

4.2.1 Output Capacitors

At PCB level, there is parasitic inductance related to the LX trace (Lpcb shown in Figure 17). You should place all the output capacitance at the point of load, after the Lpcb.

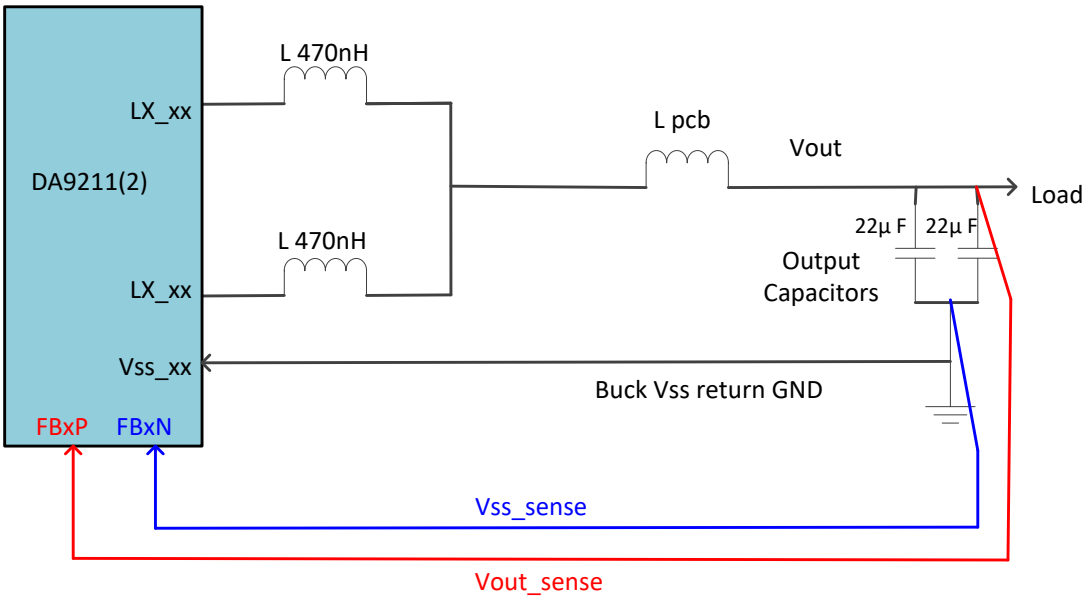


Figure 17: LC equivalent circuit

Do not split the output capacitance into a local and a remote one, because this may affect the stability of the buck converter by introducing additional poles on top of the output LC filter.

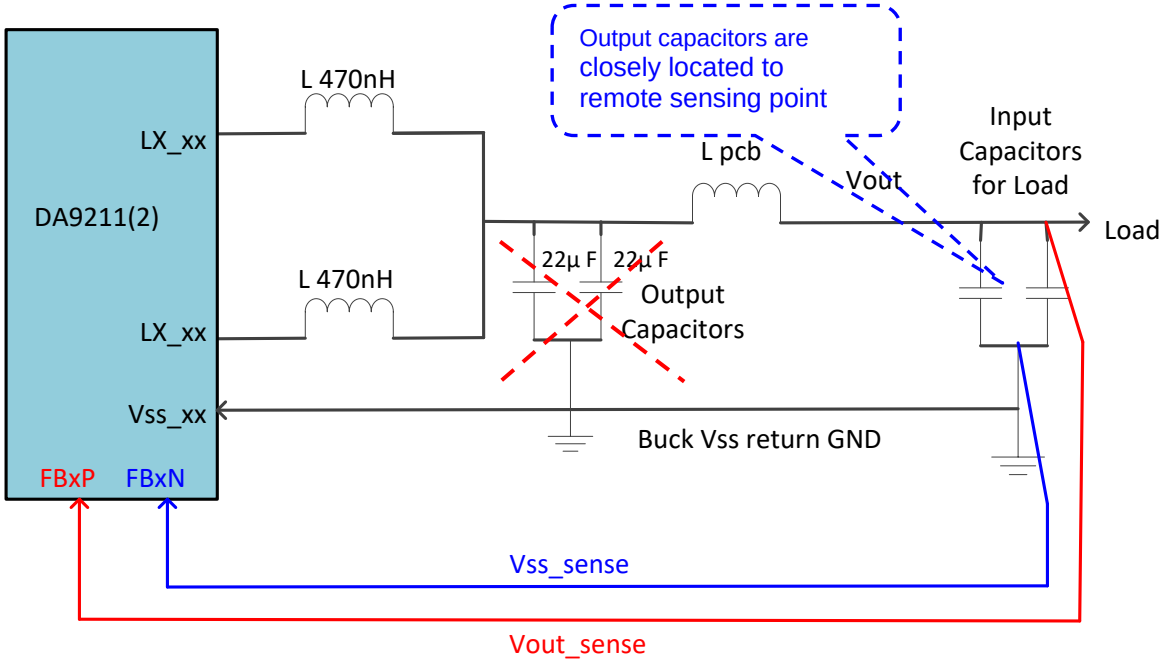


Figure 18: Avoid splitting the output capacitors between local and remote

4.3 NC (B3) pin

NC (B3) pin is not connected pin, so should be left floating.

4.4 Communication Interfaces (I2C)

There aren't any strong rules regarding the interface routing strategy. All of the signals are digital and immune to noise. Care must be taken regarding the noise produced by the interface signal, in order to avoid coupling to the sensitive analogue references and feedbacks.

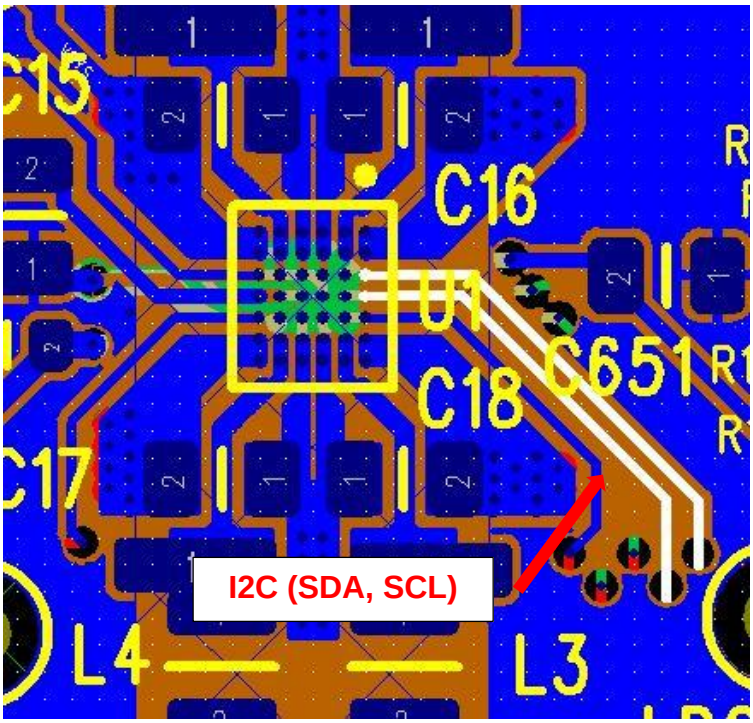


Figure 19: I2C (SDA, SCL) interface lines

4.5 GPIOs signals

Generally GPIOs has the lowest routing priority. Any layer can be used for routing these signals.

5 Revision history

Revision	Date	Description
2.1	25-Feb-2022	Document rebranded to Renesas
2.0	02-Dec-2014	Updated to add notice of split output capacitors
1.0	02-Sep-2014	Initial version.

Status definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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