Digital-DC™ FREQUENTLY ASKED QUESTIONS (FAQ)

Update 1/19/11

1. What is Digital-DC?

   Digital-DC is an innovative mixed-signal power management and conversion architecture that combines a compact, efficient, synchronous buck controller, adaptive drivers and key power and thermal management functions in one IC. Digital-DC devices also incorporate an I^2C/SMBus hardware interface with full PMBus compliance, including support for over 100 PMBus commands.

2. What is PMBus™?

   PMBus is a power management protocol that allows users to easily configure and monitor all aspects of the DC-DC converter circuit through an I^2C or SMBus™ hardware interface. Digital-DC devices support over 100 PMBus commands. For PMBus specifications and more information, please see the official PMBus web site at http://pmbus.info/index.html.

3. Are Digital-DC devices compatible with extended temperature environments?

   Yes. Digital-DC devices are specified for an operating junction temperature of -40 to 125 ˚C. The absolute maximum junction temperature is 150 ˚C.

4. What is the reference tolerance (and output accuracy) on Digital-DC devices?

   The initial tolerance of the internal voltage reference is less than 0.4% and is guaranteed to be 1% over line, load, and temperature conditions. The total output accuracy is guaranteed to be within 3% of configured output voltage including transient variations given adequate design of the output filter stage.

5. What is the maximum output current? Is it capable of 5A, 10A, 15A and 30A ?

   The ZL9101MIRZ power module with integrated MOSFETs, discrete components, and the inductor can supply up to 12A. The ZL9101M modules can also be connect together for >12A, up to 6 modules in parallel. For output currents greater than 15A, additional attention to thermal design is recommended in order to assure the application circuit will operate reliably within the recommended thermal guidelines. For more information, please use the device datasheet.

6. Are Digital-DC devices compatible with DDR2 memory applications?

   Yes. The internal synchronous driver is capable of sinking and sourcing current, and ratio-metric voltage tracking is supported.

7. What is the typical output ripple of a Digital-DC device?

   Output voltage ripple is primarily determined by the switching frequency and the design of the power train, including the output inductor and filter capacitance.

Digital-DC devices will typically exhibit an output ripple that is less 1% of the output voltage given good design techniques.

8. Does the ZL9101M support current sharing between devices?

   Yes. Please refer to the product datasheet for more information.

9. Do Digital-DC devices support phase interleaving between devices?

   Yes. Digital-DC devices can be configured to start its switching cycle at 22.5° increments. This allows multiple devices connected in parallel to draw their input current at different intervals, thus reducing the instantaneous current drawn from the input and allowing the use of fewer input capacitors.

10. Do you offer pre-bias start-up capability?

    Yes. With a pre-bias condition present on the output prior to start-up, the module will begin to track the pre-configured start-up ramp period but will inhibit the PWM signals until the start-up ramp intersects the pre-bias voltage already present on the output. At that point, the controller turns on both driver outputs to the duty cycle that corresponds to the input supply and target output voltage and continues the start-up ramp until the target output voltage has been achieved.

11. Do Digital-DC devices offer soft-start capability?

    Yes. Digital-DC devices can be configured to achieve its target voltage instantaneously (limited by capacitance present) or to ramp monotonically to its target voltage within a period up to 200ms. A start-up delay, with an initial minimum time, can also be configured up to 200 ms.

12. Do Digital-DC devices offer start-up sequencing?

    Yes. Using the start-up ramp procedure discussed above, multiple devices can be configured to start at any desired rate and/or sequence. Sequencing can be time based or event based and can be re-configured using PMBus commands without any hardware modifications.

13. Do Digital-DC devices offer output margining?

    Yes. The default limits are set to ±5% but can be modified as low as ±1% or as high as +10%/-100% using PMBus commands. The +10% margin limit is a hardware limit intended to protect sensitive circuitry from being subjected to an over-voltage condition.

14. Do Digital-DC devices offer output tracking?

Yes. Any Digital-DC device can track any other supply by connecting the VTRK pin of the following device to the output that is to be tracked. Tracking can be coincidental or ratio-metric. The ratio-metric default is for the tracking device to follow at 50% of the voltage being tracked. This ratio may be modified using a voltage divider.

15. Do Digital-DC devices offer input and output monitoring?

Yes. Digital-DC devices can monitor a wide variety of input and output parameters as well as power conversion parameters. A partial list of parameters that can be monitored include input voltage, output voltage, output current, internal temperature, load device temperature, duty cycle, MOSFET dead-time, and fan speed. Please contact the factory for a full list of parameters that can be monitored.

16. What protection features are supported in Digital-DC devices?

Digital-DC devices support protection features including input under-voltage protection, output pre-bias protection, output over-voltage protection, output current limiting, and device over-temperature limiting. Please contact the factory for other protection features.

17. How is current limiting implemented on Digital-DC devices? What is the sensing accuracy?

Digital-DC devices incorporate several methods for implementing current limiting. The methods available include low-side MOSFET $R_{DS(ON)}$ sensing, current sense resistor measurement, inductor DCR sensing, and inductor average current (series R/C) sensing. The current limit circuit can respond to an over-current condition within 1 switching cycle. The response time to an over current event can be adjusted by the user. Current sensing accuracy depends on the method used. Excluding external tolerances, the current sensing accuracy is approximately ±5%. Using MOSFET $R_{DS(ON)}$ sensing, the device can use the internal or external temperature sensor to calibrate for the typical temperature coefficient of the MOSFET(s) used. High-side current sensing is not available when producing an output greater than 4V.

18. What is the thermal capability of the QFN package?

Digital-DC devices are packaged in QFN packages. The 15mm x 15mm QFN package specifies a Θ_{JA} of approximately 12.5˚C/W and a Θ_{JC} (Junction to case) of 2.2˚C/W. These values will mainly depend on board layout, copper thickness. For more detailed information on the QFN package, please refer to Application Note *AN10: ZL2005 and ZL2105 Thermal and Layout Guidelines*.

19. How is thermal limiting implemented on Digital-DC devices? Can the thermal shutdown limit be modified?

Digital-DC devices are pre-configured to shut down at an internal junction temperature of 125°C. Once the internal junction temperature reaches 125°C, the device will shut down and allow the device to cool. Once the junction temperature drops approximately 10°C below the pre-configured thermal limit, the device will turn on again. If the fault condition that is forcing the over-temperature condition still exists, the device will cycle through this process until the fault is removed. It is possible to change the thermal shutdown limit to any value up to 130 ˚C. Setting the thermal limit above 130°C is prohibited to prevent thermal overstress to the device.

20. How do you set the device address when using multiple parts on the SMBus?

Digital-DC devices include either one or two pins for setting the SMBus address. By pin-strapping these pins the user can set unique bus addresses for multiple devices that are being used on the same physical bus.

21. How is current limit implemented?

Several methods for implementing current limit are available to the user:
This can be accomplished by sensing either the $RDS_{(ON)}$ of the low side switch, inductor series resistor or a resistor in series with the output inductor.
The current limit circuit can respond to an over-current condition within 1 switching cycle. The response time to an over current event can be adjusted by the user

22. How to set current limit threshold?

Divide the desired setpoint by (1-x%), where x% is the total range of variance including $R_{DS(on)}$ tolerance and setpoint error.
In the above example, x%=30%, divide 20A/(1-30%)=20A/0.7=28.6A.
Set current limit to 28.6A to guarantee lower protection setpoint at 20A. Note that a part without temperature compensation would also have to factor in the increase of $R_{DS(on)}$ due to temperature which can result in a highest protection setpoint over 200% of Imax!

23. How to use the temperature compensation for current limit?

The equation implementing the temperature compensation is
$R_{SEN} = R_{25} * (1 + TC * (T-25))$, where R_{SEN} is the effective value of the current sense resistor at temperature T and R_{25} is the value of the current sense resistor at T = 25°C.

Typical values are TC = 300 ppm/°C for thick film resistors, TC = 3930 ppm/°C for copper, and TC = 4800 ppm/°C for typical trench MOSFETs.

24. Provide details on fault thresholds and the timing of monitoring activities.

The faults monitored are the following:

- Input Overvoltage (IOV) is monitored by the Aux ADC on a 4ms sampling basis against a 10-bit programmable threshold.
- Input Undervoltage (IUV) is monitored by a hardware comparator against a 6-bit programmable threshold. Shutdown is accomplished within gate propagation delays after a programmable number of undervoltage violations.
- Output Overvoltage (OOV) is monitored by a hardware comparator against a 10-bit programmable threshold. Shutdown is accomplished within gate propagation delays after a programmable number of overvoltage violations.
- Output Undervoltage (OUV) is monitored by a hardware comparator against a 10-bit programmable threshold. Shutdown is accomplished within gate propagation delays after a programmable number of undervoltage violations.
- Overcurrent (OCP) is monitored by a mixed-signal implementation which checks the current limits on alternate switch cycles. The threshold is set as a positive or negative multiple of 3% of full-scale current.
- Undercurrent (UCP) (for negative current) is monitored by a mixed-signal implementation which checks the current limits on alternate switch cycles. The threshold is set as a positive or negative multiple of 3% of full-scale current.
- Overtemperature (OTP) is monitored by the Aux ADC on a 4ms sampling basis against a 10-bit programmable threshold. The measured temperature is then filtered which slows the response from the 4 ms loop time.

25. What is the range for the output voltage droop?

The table below shows the max. supported value for VOUT_DROOP as a function of the target voltage:

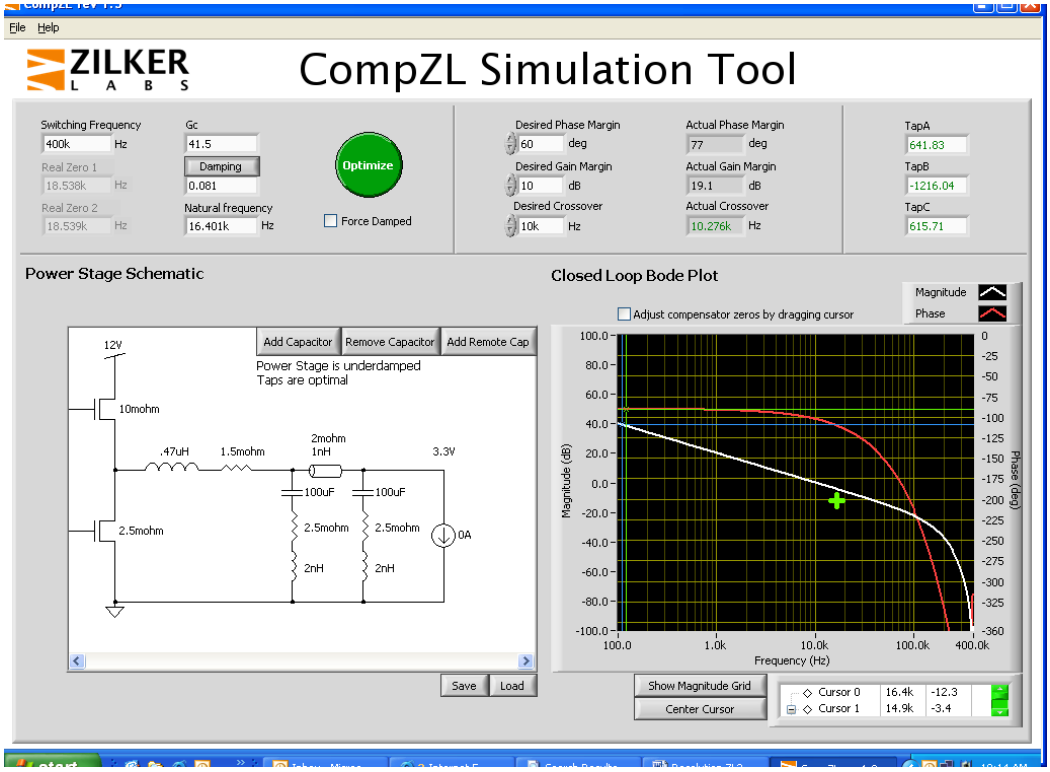
Target Voltage:	Max. VOUT_DROOP
0.000 to 0.988	2.0 * IOUT_SCALE
0.988 to 1.383	2.8 * IOUT_SCALE
1.383 to 1.975	4.0 * IOUT_SCALE
1.975 to 2.398	4.8 * IOUT_SCALE
2.398 to 3.753	7.6 * IOUT_SCALE
3.753 to 4.938	10 * IOUT_SCALE
4.938 to 5.500	14 * IOUT_SCALE

These max values are based on nominal bandgap values.

26. How can we determine the compensation coefficients A, B, C

Zilker Labs provides a tool, ComPZL, that has been developed to provide an automatic calculation of the 3 coefficients based on the power train selected and the

target cross over frequency, gain and phase margin. The software will provide resulting bode plot and adjust automatically the PID coefficient for optimal performance. Please contact your sales office for a copy of the latest software revision



27. How to determine f_{zesr} to choose FC0 and FC1?

    You can use Equation 2 in the application note AN16,

    f_{zesr}=1/(2*pi*C*Rc), where Rc is the Capacitor ESR, divided by the number of capacitors.

    AN16 defines the procedure for choosing one of the six general pin-strap options for compensation, whereas the intent of this MathCAD tool is to help the user create custom taps for his specific application. Pinstrap compensation options are provided for customers who don't use PMBus.

28. Can we change the PID taps on the fly without cycling power?

    Yes, changing PID settings on the fly is allowed. The PMBus command to do this writes all three PID tap settings simultaneously. This is not however recommended to change the PID taps during operation.

29. How do you implement fault spreading between multiple Digital-DC devices?

Fault spreading is turned on when sequencing is turned on as described in the device data sheet. Fault spreading requires the devices to be connected through the SMBus.

Fault spreading can also be turned on through the PMBus. SMBus_TX_Inhibit needs to be set to 'Transmit Enabled' so the device will transmit faults and Fault_Spread_Control needs to be set to 'Act On Fault' so the device will not ignore the faults. Enabling sequencing by resistor on the CFG pin sets both of these bits appropriately.

30. How many devices can be use in a group?

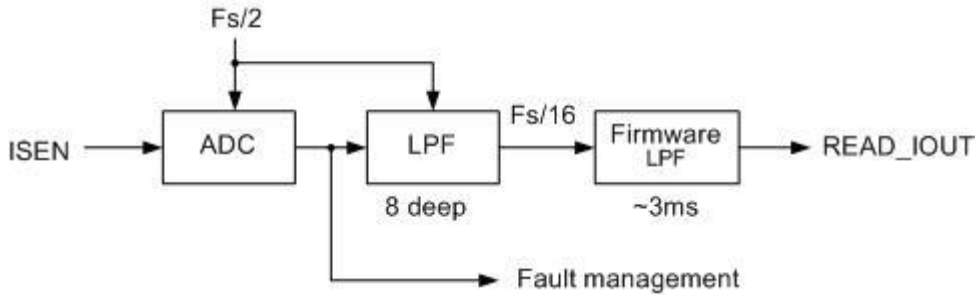
The address group for fault spreading and event based sequencing is limited to 8 addresses. This was chosen to reduce internal firmware code size. A device receiving a Power Fail message from any other device in its group will shutdown immediately and wait for the proper sequencing order of a restart to occur. A device determines if a message is from another device in its group by masking the lower three address bits of the other device's address (contained in the message) and comparing the result to its own address.

31. Do Digital-DC devices need to be power cycled after the CPU sets a custom device configuration?

No, power cycling is not required. Almost all of the configuration commands can be issued real-time without requiring any power cycle, including the PID tap settings. Issuing a STORE_USER_ALL command after loading these new values will save the new settings in flash and the device will then load these settings every time it powers up thereafter.

32. What is the monitor ADC sample rate?

The hardware measures current at a rate of $Fsw_{/2}$ (the min and max current are read every half switching cycle) through the ADC, and the output of this ADC is used for fault management. The ADC output then goes into some filtering stages before storing the measured value, which can be read using the READ_IOUT command. The SMBus throughput is limited to 100us/byte, and it takes roughly 1ms to perform a read-back function using the PMBus command READ_IOUT. The current value measured by our device is updated every 3 ms to 5 ms, so issuing the command faster than every 3ms will result in the same value being reported. See diagram below.



33. Can we provide a “max hold” function for current measurement?

    Digital-DC devices do not have any threshold intended for this function, but an external CPU could monitor the current reading at regular intervals and provide the max current data over a specific time period. This is also something that we can easily incorporate into future devices as a standard function.

34. How does our dead-time algorithm work?

    Typical analog PWMs with this feature try to minimize the dead-time, but in doing so may get so low that they start to encounter cross-conduction due to variations in the capacitive nature of the MOSFETs used (this can vary from lot to lot). Our Digital-DC architecture instead is continuously trying to optimize the efficiency by looking for the minimum duty cycle based on a given input/output voltage ratio (this minimum duty cycle corresponds to the highest efficiency). The optimal efficiency point doesn’t always occur at the lowest dead-time setting. Additionally, our algorithm closes its loop around the power train components, so variations in the FET capacitance or other parameters are captured and compensated for in our calculation.

35. Can you reconfigure a part for tracking or to regulate at its own target without modifying hardware?

    Yes, all Digital-DC parts can be modified using a simple PMBus command to vary between tracking another voltage at a specific percentage or regulating at its own target voltage. No hardware changes needed if the required tracking input voltage connection is incorporated into the board design.