SLG4W41403

Vertical Marketing GPIO Expander

General Description

Silego SLG4W41403 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

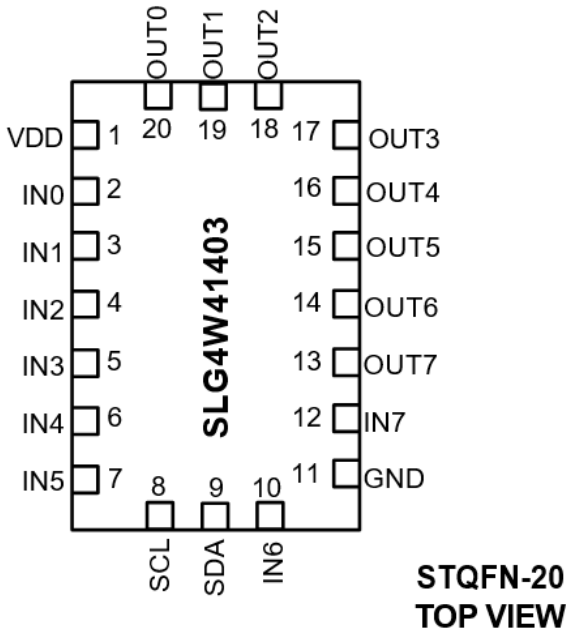
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

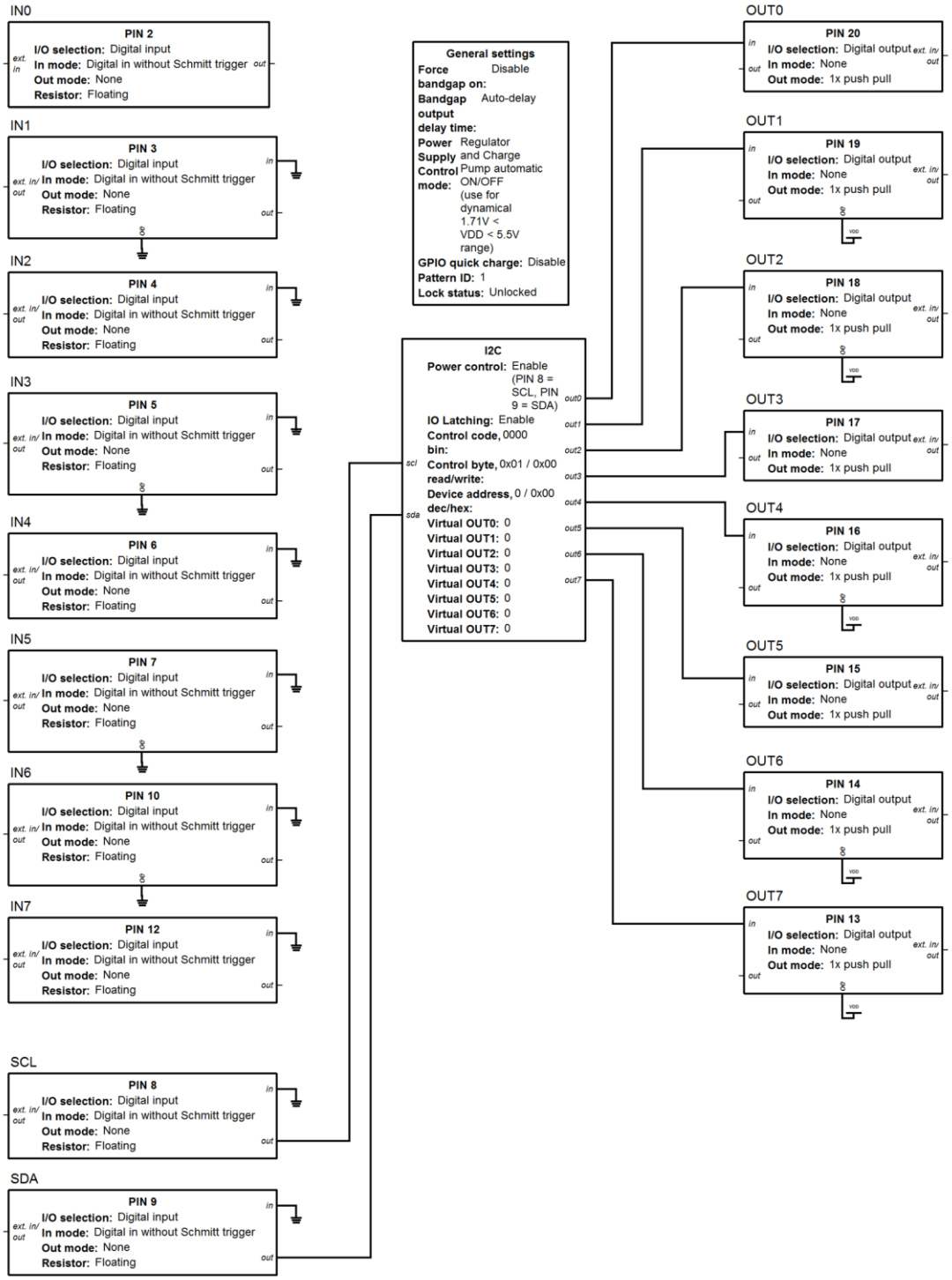
Output Summary

- 8 Outputs — Push Pull 1X

Pin Configuration



Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	IN0	Digital Input	Digital Input without Schmitt trigger
3	IN1	Digital Input	Digital Input without Schmitt trigger
4	IN2	Digital Input	Digital Input without Schmitt trigger
5	IN3	Digital Input	Digital Input without Schmitt trigger
6	IN4	Digital Input	Digital Input without Schmitt trigger
7	IN5	Digital Input	Digital Input without Schmitt trigger
8	SCL	Digital Input	Digital Input without Schmitt trigger
9	SDA	Digital Input	Digital Input without Schmitt trigger
10	IN6	Digital Input	Digital Input without Schmitt trigger
11	GND	GND	Ground
12	IN7	Digital Input	Digital Input without Schmitt trigger
13	OUT7	Digital Output	Push Pull 1X
14	OUT6	Digital Output	Push Pull 1X
15	OUT5	Digital Output	Push Pull 1X
16	OUT4	Digital Output	Push Pull 1X
17	OUT3	Digital Output	Push Pull 1X
18	OUT2	Digital Output	Push Pull 1X
19	OUT1	Digital Output	Push Pull 1X
20	OUT0	Digital Output	Push Pull 1X

Ordering Information

Part Number	Package Type
SLG4W41403V	V=STQFN-20
SLG4W41403VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

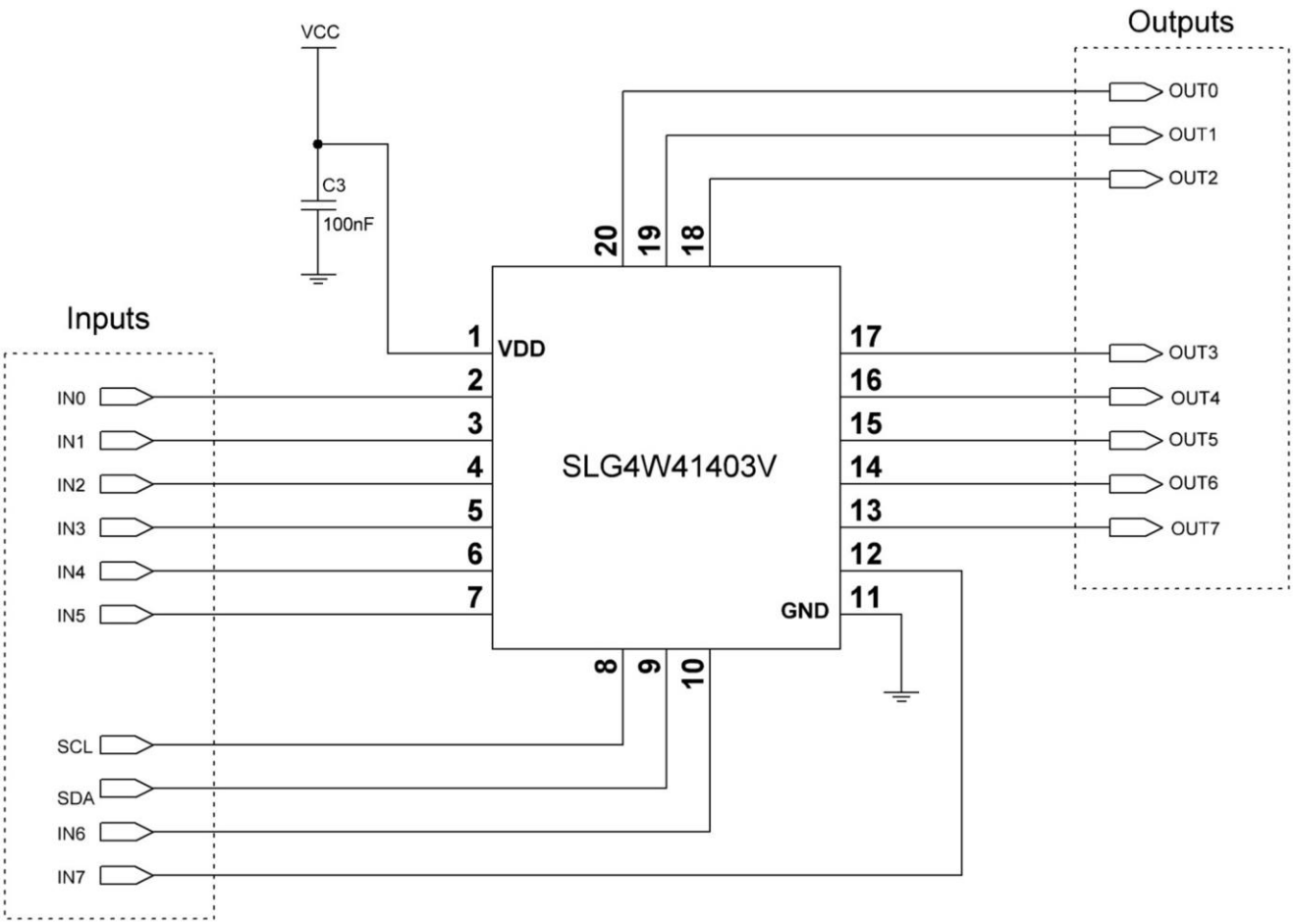
Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.7	3	3.3	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs VDD=5.5V	--	0.95	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=1.8V	1.06	--	VDD	V
		Logic Input, at VDD=3.3V	1.81	--	VDD	
		Logic Input, at VDD=5.0V	2.68	--	VDD	
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=1.8V	0	--	0.76	V
		Logic Input, at VDD=3.3V	0	--	1.31	
		Logic Input, at VDD=5.0V	0	--	1.96	
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push Pull & PMOS OD, I_{OH} = 100uA, 1X Driver, at VDD=1.8 V	1.69	1.79	--	V
		Push Pull & PMOS OD, I_{OH} = 3mA, 1X Driver, at VDD=3.3 V	2.70	3.12	--	
		Push Pull & PMOS OD, I_{OH} = 5mA, 1X Driver, at VDD=5.0 V	4.15	4.76	--	
V_{OL}	LOW-Level Output Voltage	Push Pull, I_{OL} = 100uA, 1X Driver, at VDD=1.8 V	--	0.009	0.013	V
		Push Pull, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.13	0.23	
		Push Pull, I_{OL} = 5mA, 1X Driver, at VDD=5.0 V	--	0.19	0.24	
I_{OH}	HIGH-Level Output Current	Push Pull & PMOS OD, V_{OH} = VDD-0.2, 1X Driver at VDD=1.8 V	1.07	1.70	--	mA

		Push Pull & PMOS OD, VOH = 2.4 V, 1X Driver, at VDD=3.3 V	6.05	12.08	--	
		Push Pull & PMOS OD, VOH = 2.4 V, 1X Driver, at VDD=5.0 V	22.08	34.04	--	
IOL	LOW-Level Output Current	Push Pull, VOL = 0.15V, 1X Driver, at VDD=1.8 V	0.92	1.69	--	mA
		Push Pull, VOL = 0.4V, 1X Driver, at VDD=3.3 V	4.88	8.24	--	
		Push Pull, VOL = 0.4V, 1X Driver, at VDD=5.0 V	7.22	11.58	--	
TSU	Start up Time	From VDD rising past 1.6 V	--	1	--	ms
FSCL	Clock Frequency, SCL		--	--	400	kHz
tLOW	Clock Pulse Width Low		800	--	--	ns
tHIGH	Clock Pulse Width High		200	--	--	ns
tI	Input Filter Spike Suppression (SCL, SDA)		--	--	168	ns
tAA	Clock Low to Data Out Valid		--	--	900	ns
tBUF	Bus Free Time between Stop and Start		1300	--	--	ns
tHD_STA	Start Hold Time		448	--	--	ns
tSU_STA	Start Set-up Time		5.8	--	--	ns
tHD_DAT	Data Hold Time		0	--	--	ns
tSU_DAT	Data Set-up Time		89	--	--	ns
tR	Inputs Rise Time		--	--	300	ns
tF	Inputs Fall Time		--	--	300	ns
tSU_STD	Stop Set-up Time		9.1	--	--	ns
tDH	Data Out Hold Time		444	--	--	ns
tst_out_delay	State Machine Output Delay Time		67	--	275	ns
tst_out	State Machine Output Transition Time		--	--	165	ns
tst_pulse	State Machine Input Pulse Acceptance Time		9.2	--	--	ns
tst_comp	State Machine Input Compete Time		--	--	29	ns

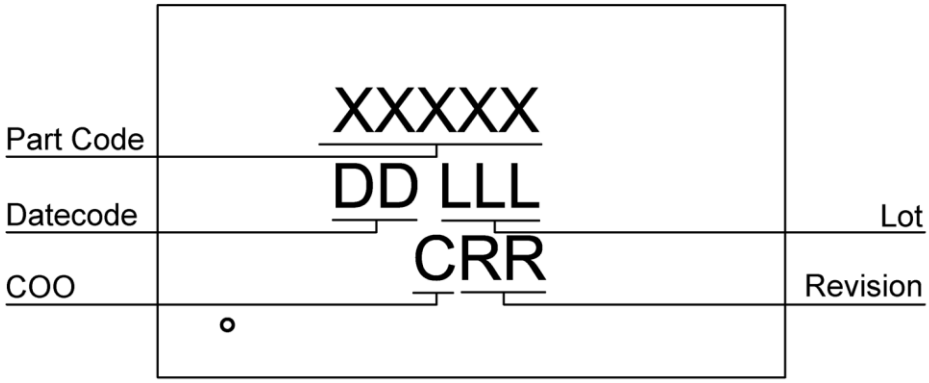
Description

This device uses Silego's GreenPAK5 chip (SLG46531V) demonstrates I2C GPIO Expander in GPAK. I2C speed supported by GPAK is 400kHz and can have up to 16 unique addresses (0000b default in current design). IO are set to latch during writing or updating values.

Typical Application Circuit



Package Top Marking



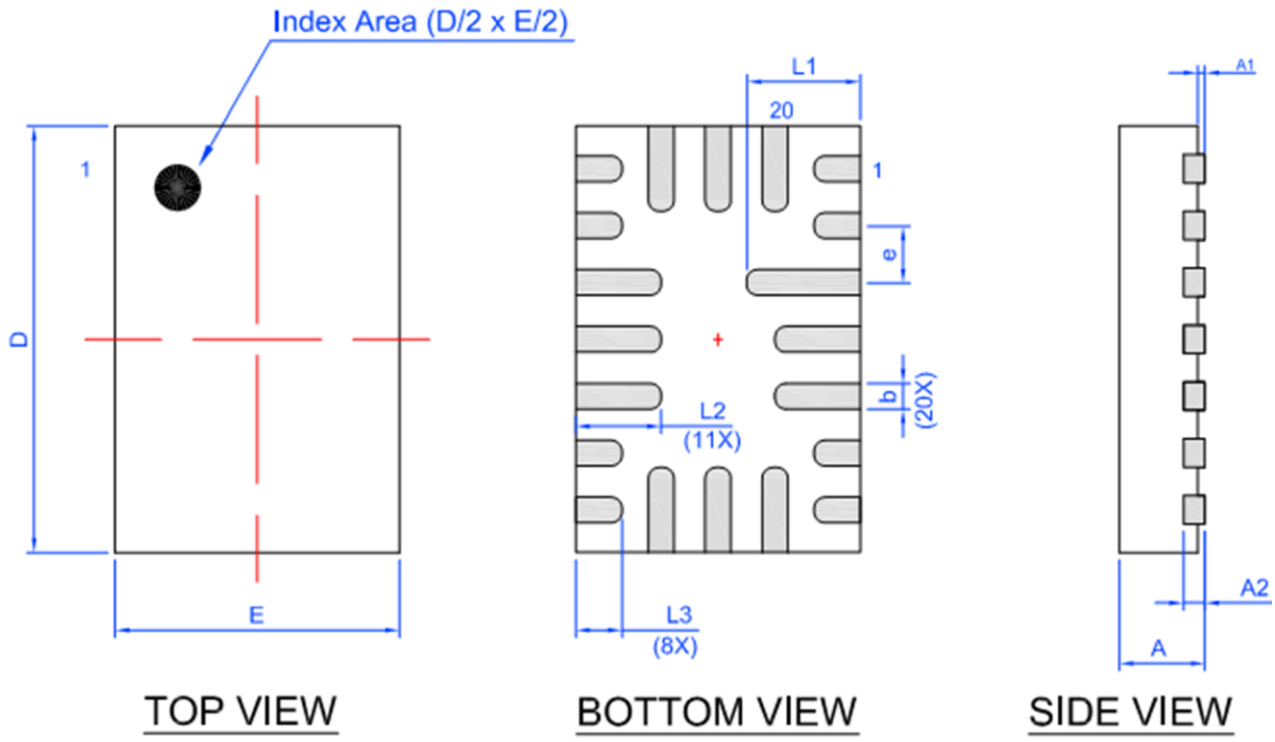
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
0.10	001	U			09/08/2016

The IC security bit is locked/set for code security for production unless otherwise specified. Revisionnumber is not changed for bit locking.

Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE
IC Net Weight: 0.0090 g



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

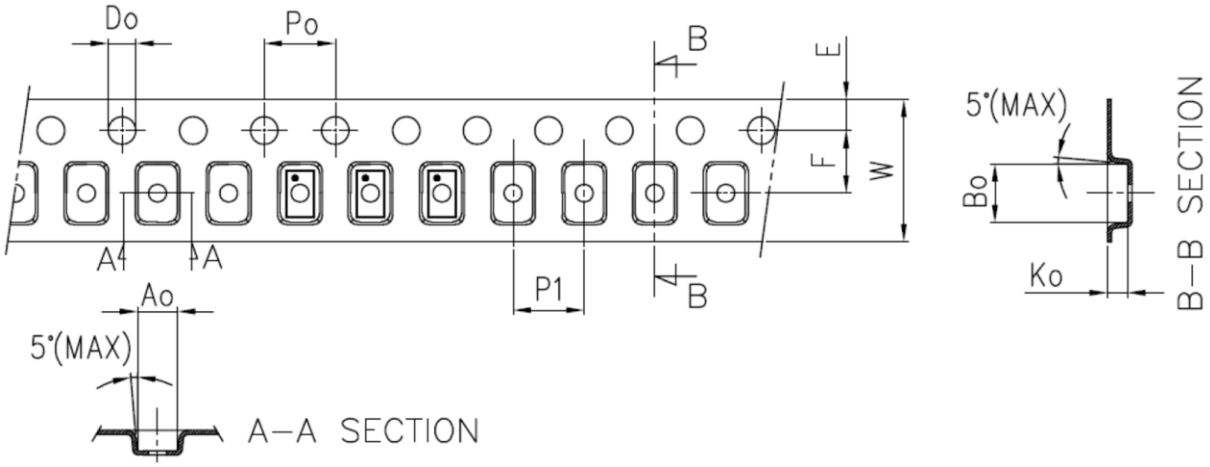
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal).More information can be found at www.jedec.org.

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